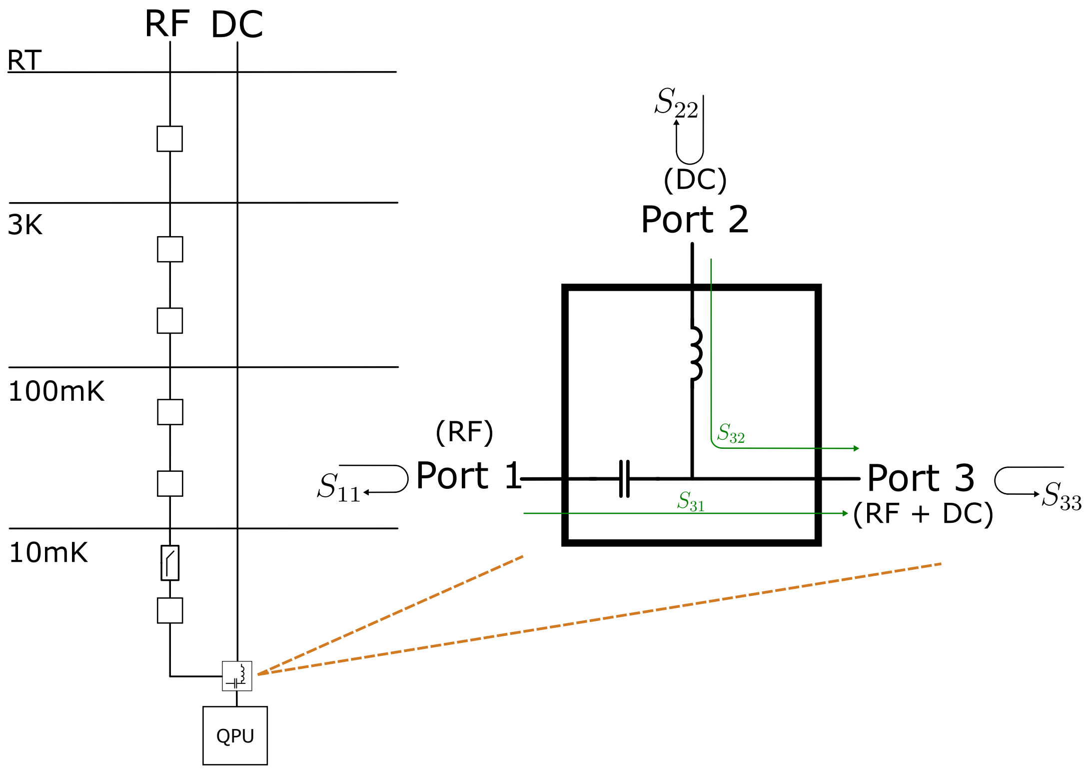

Design of a Superconducting Bias-Tee

RF and DC Signal Diplexer for Quantum Computing Applications

Master's thesis in Wireless, Photonics and Space Engineering

LANDAGE RAVINDU KANISHKA PIYAPEMA

DEPARTMENT OF MICROTECHNOLOGY AND NANOSCIENCE
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2025
www.chalmers.se

Master's thesis 2025

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Supervisor: Robert Rehammar
Examiner: Jan Grahn, Department of Microtechnology and Nanoscience

Master's Thesis 2025
Department of Microtechnology and Nanoscience
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: Bias-Tee used in a signal chain with a zoomed illustration of the bias-tee as a 3 port device

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Abstract

The tight integration of qubits is a significant challenge for the development of modern quantum computers. Closely placed qubits will be subjected to frequency crowding. Flux tuning of qubits can reduce the frequency crowding by changing the resonance frequency of a qubit by changing the magnetic flux, which requires the coupling of DC and RF signals. A bias-tee implements the diplexing of DC power and RF signals.

In this thesis, We report findings on a microwave bias-tee designed to be fabricated as an integrated passive device in a superconducting process on silicon or quartz.

A bias-tee requires an inductive branch and a capacitive branch to diplex DC signals and RF signals. Therefore, passive components such as inductors and capacitors have been modelled and simulated. Moreover, the effect of the wafer, dielectrics, and packaging techniques are studied to describe the non-ideal performance of passive components.

One of the challenges of simulating thin film devices in the Finite Element Method (FEM) solvers is the issue of dielectric thickness compared to the rest of the structure. The large difference in dimensions leads to erroneous mesh elements. This thesis also introduces a novel detailed explanation of the meshing of thin films in FEM solvers that has not been thoroughly covered in the existing literature.

The simulation results show capacitors with a quality factor of 7000 realised in a silicon process and a quality factor of 4000 realized in a quartz process. We also report the design of planar coils, which have a quality factor of 2400 for the silicon process and 2000 for the quartz process.

Keywords: bias-tee, passive components, parasitic elements, critical current, waveguide, physical model, equivalent circuit model.

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I am a result of lot of love and generosity of many. I would like to think of you all right now. Hope you are proud of me.

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Someone once told me I was brave enough to leave my loved ones to pursue ambition. In reality, the people around me kept me company so the coward behind the mask would not creep out. My thanks go out to the friends I made in Sweden. I would like to remember Hans, Dennis, Victor, Elsa, Amanda, Rickard, Filip, and Johannes for showing me the Swedish way of life and their warm hospitality. I am also grateful for my surrogate family: Supun, Nilantha, Sumi, Geo, Ashutosh, Ramya, Charitha, Tilani, Sachi, Nik and Abhijith. My thanks go out to Lasantha Aiyya for helping me to apply to Chalmers.

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L.R.K. Piyapema, Gothenburg, August 2024

List of Acronyms

Below is the list of acronyms that are being used throughout the thesis listed in alphabetical order:

3D FEM	Three-Dimensional Finite Element Method
AC	Alternating Current
CAD	Computer Aided Design
CPW	Coplanar Waveguide
DC	Direct Current
GCPW	Grounded Coplanar Waveguide
IPD	Integrated Passive Device
MMIC	Monolithic Microwave Integrated Circuit
MIM	Metal Insulator Metal
PEC	Perfect Electrical Conductor
QPU	Quantum Processing Unit
RF	Radio Frequency
SQUID	Superconducting Quantum Interference Device
TEM	Transverse electromagnetic

Nomenclature

Below is the nomenclature of indices, sets, parameters, and variables that are being used throughout the thesis.

Indices

i,j	Indices for scattering parameter

Parameters

$\vec{E}$	Electric field, in volts per meter
$\vec{H}$	Magnetic field, in amperes per meter
$\vec{D}$	Electric displacement field, in coulombs per meter squared
$\vec{B}$	Magnetic flux density, in webers per meter squared
$\vec{J}$	Electric current flux density, in amperes per meter squared
ρ	Electric charge density, in coulombs per meter cubed
T_c	Critical temperature of superconductor
k_B	Boltzmann constant
h	Planck constant
λ_L	London penetration depth

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1

Introduction

This chapter will start with a very brief introduction to quantum computing. Then, the use of DC signals in the context of quantum computing is explained. Moving on, an explanation for why a superconducting bias-tee is required will be presented. Finally, a summary of the rest of the thesis is given.

1.1 Quantum Computing

Classical computers, which represent information as "1" s and "0” s, have dominated the information age thus far. With humanity's search for more computing power, the world of science has plunged into the pursuit of realising a quantum computer A quantum computer leverages quantum mechanical effects for computation. These quantum mechanical phenomena enable significant computation speed to solve a definite set of problems. One such famous example is Shor's Algorithm, which can only be executed on a quantum computer [1].

Qubits enable this paradigm-shifting computation. Qubits in a quantum computer are the analogue of bits in a classical computer. A qubit is a multi-level quantum mechanical resonator. Unlike harmonic oscillators or linear resonators, qubits are non-linear, making the different energy levels non-equally spaced. The said qubit above behaves as an artificial atom where the resonance frequencies are discretised with a spacing which would resemble the energy levels of electrons in an atom[2].

There are many ways to realise a qubit. Some sought-after approaches are superconducting qubits [3], photonic qubits [4], trapped ion qubits [5], and quantum dot qubits [6]. Companies such as Google and IBM and universities such as Chalmers University of Technology are pursuing superconducting qubits. The focus of this thesis work will be to design a supporting device for superconducting qubits.

As discussed before, a non-linear resonator is required to realize a qubit. One such non-linear device would be the "Josephson junction", formed from an insulator sandwiched between two superconductors [7]. However, for junction operation, the requirement for the superconductivity of the metals should be met. The dimensions of the said junction determine the resonance frequency, naturally in the microwave regime f_{μ}. However, at room temperature, the microwave photon energy is drowned by the thermal noise energy (Johnson–Nyquist noise)[8]. Hence, the system should be cooled down to a temperature T such that the energy of photon is more than the thermal noise energy $k_B T << hf_\mu$. The rest of the electronics supporting the qubit, such as the packaging solution, filters, and bias tees, should be ideally superconducting to prevent heat generation.

1.1.1 DC signals for qubits

The frequency at which the state transition occurs in a qubit can be different from what was expected due to the fabrication process. The inaccuracy of the transition frequency can cause frequency collision with a neighbouring qubit [9]. With an increasing number of qubits, more frequency collisions would take place. The issue of frequency collision can be mitigated by with a SQUID transmon, where its transition frequency can be tuned with an external flux [10]. The flux should also be changed dynamically; hence, an oscillating current is also required. Furthermore, magnetic flux can be used to tune the coupling between a waveguide and a qubit [11]. Hence, additional lines should accommodate DC signals.

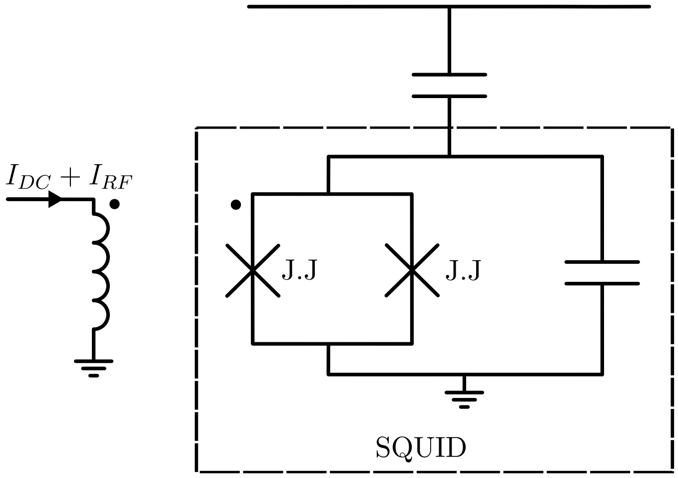


Figure 1.1: A squid with a flux bias line. Components J.J are the Josephson Junctions.

1.2 Bias-tee

To attain dynamic flux tuning, AC and DC signals must be coupled together. Bias-tees functions such that DC signals, which are inserted from a port, and AC signals, which are inserted from another port, are combined and fed through a third different port. On a fundamental level, the desired operation can be presented in the figure 1.2.

To realize this operation, one can draw knowledge from basic circuit theory and conclude that the branch where DC should only flow should be inductive. The branch that should only conduct AC should be capacitive (The idea of capacitance

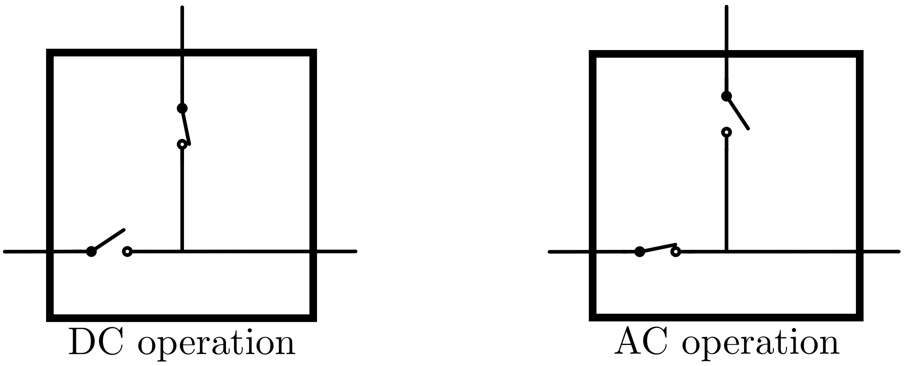


Figure 1.2: Bias tee operation in DC and AC.

and inductance will be discussed at length throughout this work). With these two concepts in mind, the fundamental passive network can be presented in the figure 1.3.

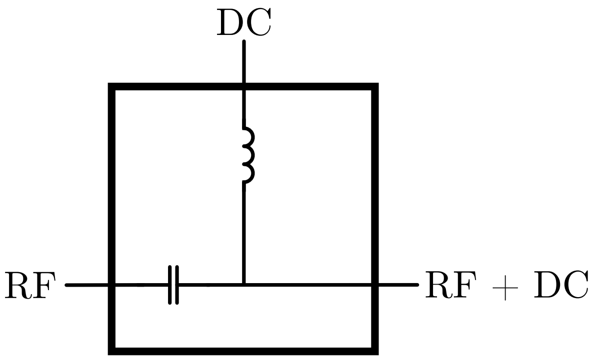


Figure 1.3: Bias tee schematic symbol.

1.3 Motivation of the thesis work

A fault-tolerant quantum computer will require physical qubits in the range of 10000 [12]. Scaling up the current architecture to the said required number is not trivial. Coaxial cables are used to control and read out since they yield minimum crosstalk. These coaxial cables carry the signals down to the quantum processing unit (QPU). If dynamic flux control is needed, as described previously, both RF and DC signals ought to be routed. It would seem to be an attractive solution to have a bias tee on the room temperature side and couple the RF and DC signals before entering into the cryostat.

However, there will be attenuators along the RF signal chain. Resistive networks are typically used to realise these attenuators. Suppose DC is also sent in the same cable. In that case, unnecessary losses will be experienced in heating the system, which will be a huge drawback. Schemes to couple RF and DC should be implemented to scale up the computing power for quantum computers. One such method is to implement a bias-tee on an integrated passive device (IPD) to combine the RF signal to control the qubit and the DC signal to bias the qubit.

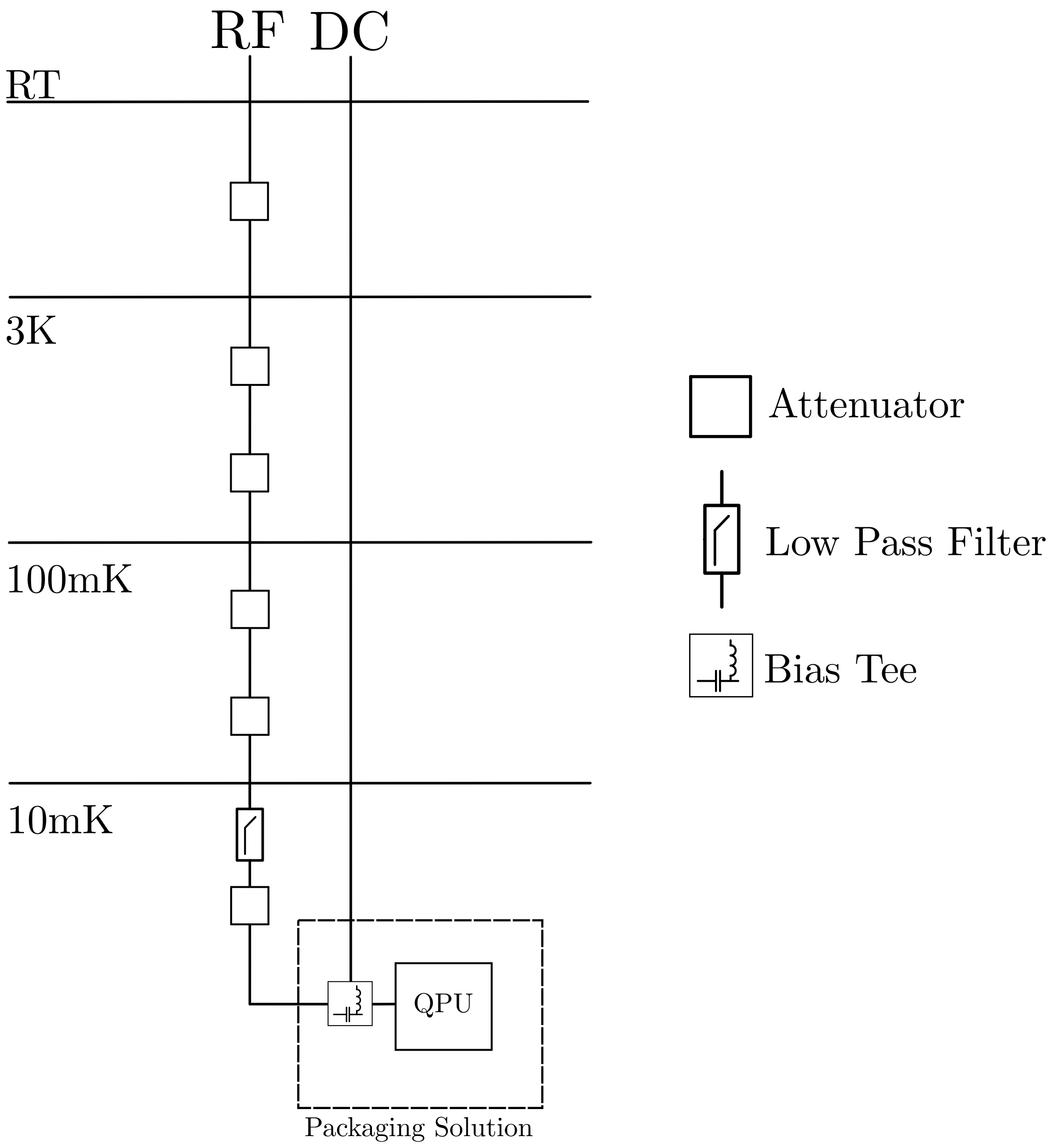


Figure 1.4: Coupling RF and DC using a bias tee.

As shown in Figure 1.4, RF and DC signals are made by different control apparatuses and carried into the packaging solution in two pathways. Moreover, inside the packaging solution, both RF and DC could be combined since it will be the last stage in the cryostat, and the combined signal would not encounter attenuators anymore.

None of the bias tees available off the shelf provide superconducting solutions. Hence, they generate unwanted heat at the lowest temperature stage of the cryostat, which is a huge drawback. This thesis aims to provide a solution where the bias-tee is superconducting and miniaturised as an IPD to support scalability.

One of the key players who should address the issue of scaling up are vendors who design packaging solutions for QPUs. For a packaging solution to be attractive, the scaling up of coax lines should be addressed, along with additional connectivity for DC signals.

1.4 Design requirements

The following design goals are needed to be met:

- The DC branch shall support up to a cutoff frequency of 10 MHz.
- The RF branch shall have a bandwidth starting from 100MHz to 20GHz.
- It shall be operable at 10mK and superconduct.
- It shall withstand a direct current of 10mA without losing superconductivity
- It shall withstand RF power of -50 dBm without losing superconductivity.

The design target would be to miniaturise the bias-tee as small as possible. Hence, it should be realised as an IPD.

1.5 Summary of chapters

The rest of the chapters in this work are presented below to build up the thesis:

2. Theory: This chapter will introduce theoretical concepts that will aid in the design in later c
3. Methods: How each device will be modelled will be introduced in this chapter, along with design
4. Results: The results of the design are presented in this chapter.
5. Conclusion: Concluding the work done and reflecting upon possibilities for future improvements.

2

Theory

In this chapter, the theoretical framework for the research work is investigated and developed. The first section is dedicated to electromagnetic theory, which lies at the heart of this work. Next, the superconducting phenomena are investigated to determine how they change the characteristic behavior of electromagnetic waves to suit our application. Then, we venture into passive components, which will be used in this work. The interconnect structures for this IPD are transmission lines; hence, a brief description of those is presented at the end.

2.1 Electromagnetic theory

Fundamental concepts of electromagnetism brought forward by Gauss, Ampere, Faraday, and others were unified by Maxwell with his contribution in 1873. His contribution to physics is now widely studied as Maxwell's macroscopic equations [13].

$$\nabla \times \vec{E} = \frac{-\partial \vec{B}}{\partial t} \tag{2.1}$$

$$\nabla \times \vec{H} = \frac{\partial \vec{D}}{\partial t} + \vec{J} \tag{2.2}$$

$$\nabla \cdot \vec{D} = \rho \tag{2.3}$$

$$\nabla \cdot \vec{B} = 0 \tag{2.4}$$

The equations (2.1) and (2.2) are coupled to each other. That means a time-varying electric field will give rise to a time-varying magnetic field, which in return will birth another electric field.

2.1.1 Fields in media

When electric fields propagate through media, their nature differs according to the properties of the media. For a dielectric material, atoms will polarize in the presence of an applied electric field $\vec{E}$, which will change the total displacement $\vec{D}$. The polarization is quantified as a vector $\vec{P_e}$.

$$\vec{D} = \epsilon_0 \vec{E} + \vec{P_e} \tag{2.5}$$

The polarization $\vec{P_e}$, which is also known as the electric dipole moment, is linearly related to the applied electric field in a linear medium. Which can be expressed as,

$$\vec{P_e} = \epsilon_0 \chi_e \vec{E} \tag{2.6}$$

The quantity χ_e is denoted as the electric susceptibility.

$$\vec{D} = \epsilon_0 \vec{E} + \vec{P_e} = \epsilon_0 (1 + \chi_e) \vec{E} = \epsilon \vec{E} \tag{2.7}$$

The complex permittivity of the medium, which denoted as ϵ can also be written as,

$$\epsilon = \epsilon_0 (1 + \chi_e) = \epsilon' - j\epsilon'' \tag{2.8}$$

The imaginary part of ϵ represents the dielectric loss occurring in the material. If the material has some conductance σ, a conduction current density will arise:

$$\vec{J} = \sigma \vec{E} \tag{2.9}$$

Above equation can also be identified as the Ohm's law in the field domain. We assume that waves are monochromatic, i.e., has a single frequency. Then, the basic sinusoidal form is a solution to Maxwell's equations (time-harmonic fields). Any arbitrary solution can be constructed by superposing solutions of different frequencies since Maxwell's equations are linear for simple media. For a plane wave propagating an arbitrary $\vec{r}$ direction, it can be written as,

$$\vec{D}(t) = |D| \cos(\omega t - \vec{k} \cdot \vec{r} - \theta) \tag{2.10}$$

The displacement field $\vec{D}$ written above can be presented in phasor form as (Underlined notations are denoted as the phasor form representation of their respective quantities.),

$$\vec{D}(t) = \Re\{|D| \cdot e^{j\theta} e^{j\omega t - k \cdot \vec{r}}\} = \Re\{\underline{\vec{D}} \cdot e^{j\omega t - k \cdot \vec{r}}\} \tag{2.11}$$

Equation (2.2) can be now modified in the phasor form will be,

$$\begin{aligned} \nabla \times \underline{\vec{H}} &= j\omega \underline{\vec{D}} + \underline{\vec{J}} \\ &= j\omega\epsilon \underline{\vec{E}} + \sigma \underline{\vec{E}} \\ &= j\omega\epsilon' \underline{\vec{E}} + (\omega\epsilon'' + \sigma) \underline{\vec{E}} \\ &= j\omega \left(\epsilon' - j\epsilon'' - j\frac{\sigma}{\omega} \right) \underline{\vec{E}} \end{aligned} \tag{2.12}$$

The ratio of the real to the imaginary part of the displacement current can be defined as the loss tangent.

$$\tan \delta = \frac{\omega\epsilon'' + \sigma}{\omega\epsilon'} \tag{2.13}$$

This electric loss, written as a form of angle, will be more apparent in the section where the capacitor will be discussed. Also, the ϵ' can be written relative to the permittivity of the free space $\epsilon' = \epsilon_r\epsilon_0$. Hence, equation (2.8) can be re-written in the following form:

$$\epsilon = \epsilon' - j\epsilon'' = \epsilon'(1 - j\tan\delta) = \epsilon_r\epsilon_0(1 - j\tan\delta) \tag{2.14}$$

Above treatment of electric fields in material is rather similar to how magnetic fields interact with the media. The magnetic dipoles of the material will align according to the applied magnetic field.

$$\vec{B} = \mu_0(\vec{H} + \vec{P_m}) \tag{2.15}$$

The magnetic polarization vector $\vec{P_m}$ can be expressed for a linear magnetic material as,

$$\vec{P_m} = \chi_m\vec{H} \tag{2.16}$$

The quantity χ_m can be defined as the magnetic susceptibility. Similarly like equation (2.7) this can be re written as,

$$\vec{B} = \mu_0(1 + \chi_m)\vec{H} = \mu\vec{H} \tag{2.17}$$

These definitions will become useful when we later model in a FEM solver to have defined boundary conditions.

2.1.2 Fields at material interface

A theoretical understanding of how electromagnetic fields behave at the material interface is required. This study will be required when trying to approximate superconductors, which are macroscopic quantum phenomena, as classical field theory. For any given material interface, the interaction of fields will be presented below.

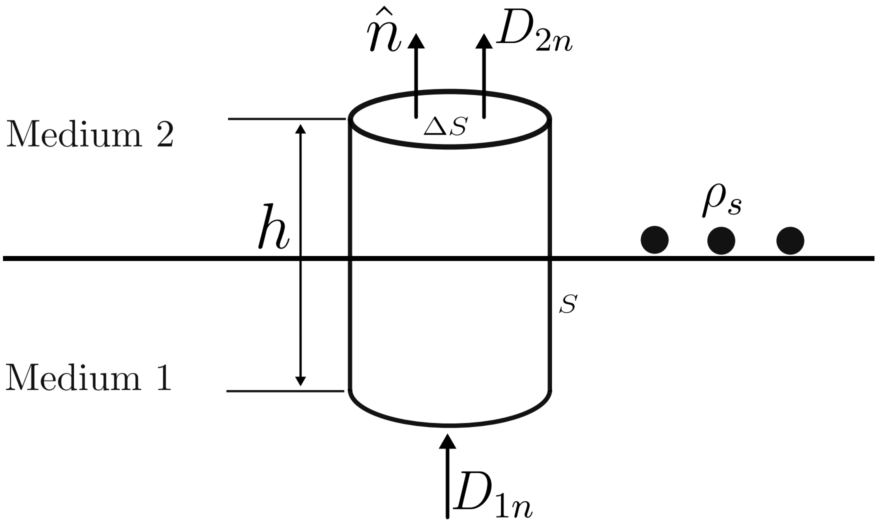


Figure 2.1: For a closed surface S enclosing the material interface.

The integral version of Maxwell's equation can be used to study the effect of normal and tangential fields on the interface. Here is the time-harmonic analog of equation (2.3).

$$\oint_s \vec{D} \cdot \mathrm{d}\vec{s} = \int_V \rho \cdot \mathrm{d}v \tag{2.18}$$

When the height h of the conceptual cylinder approaches zero, the contribution from the tangential displacement field will go to zero. Hence, the above equation can be rewritten as

$$\begin{gathered} \Delta S D_{2n} - \Delta S D_{1n} = \Delta S \rho_s \\ D_{2n} - D_{1n} = \rho_s \end{gathered} \tag{2.19}$$

Here, ρ_s is surface charge density. Converting to vector form,

$$\hat{n} \cdot (\vec{D}_2 - \vec{D}_1) = \rho_s \tag{2.20}$$

The same line of thought can be given to the $\vec{B}$ (under the physical condition that there is no free magnetic charge density), which will lead to,

$$\hat{n} \cdot \vec{B}_2 = \hat{n} \cdot \vec{B}_1 \tag{2.21}$$

For the tangential component of the electric field, the integral version of equation (2.1) can be used in phasor form,

$$\oint_C \vec{E} \cdot d\vec{l} = -j\omega \int_S \vec{B} \cdot d\vec{s} - \int_S \vec{M} \cdot d\vec{s} \tag{2.22}$$

The above equation is best described in the figure 2.2.

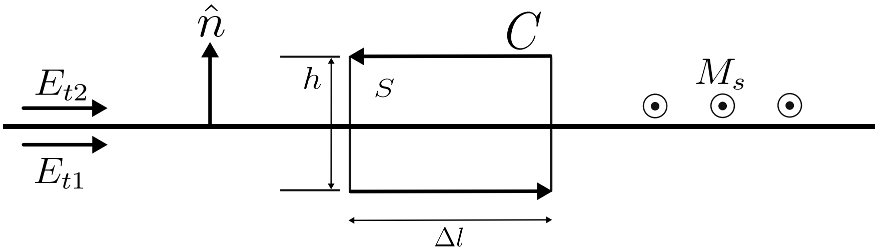


Figure 2.2: For a contour C enclosing the material interface.

When the height h of the closed contour C approaches zero, the surface integral of $\vec{B}$ disappears. If $\vec{M}_s$ exists on the surface, the contribution from the surface integral $\vec{M}$ would be non-zero. Therefore, the above equation can be rewritten as,

$$\begin{gathered} \Delta l E_{t1} - \Delta l E_{t2} = -\Delta l M_s \\ E_{t1} - E_{t2} = -M_s \end{gathered} \tag{2.23}$$

Again in vector form,

$$(\vec{E_{t1}} - \vec{E_{t2}}) \times \hat{n} = \vec{M_s} \tag{2.24}$$

For the magnetic field, we implement a similar train of thought, which results in,

$$\hat{n} \times (\vec{H_2} - \vec{H_1}) = \vec{J_s} \tag{2.25}$$

Equations (2.20), (2.21), (2.24), and (2.25) describe how electromagnetic fields behave at any given material interface.

2.2 Superconductivity

A conductor will lose all of its resistance when it transitions to a superconductor. The resistance approach zero takes place when the temperature is lowered compared to a specific temperature known as the critical temperature T_c[14]. However, another interesting phenomenon takes place when a material reaches a superconducting state.

Superconductors will also repel magnetic fields from entering the interior, known as the Meissner's effect[15]. The mechanism is analogue to how electric fields are at the interface of a good conductor. In fact, a penetration depth λ_L exists where a minute fraction of the incident magnetic field will enter the material and die down exponentially (London penetration depth)[16].

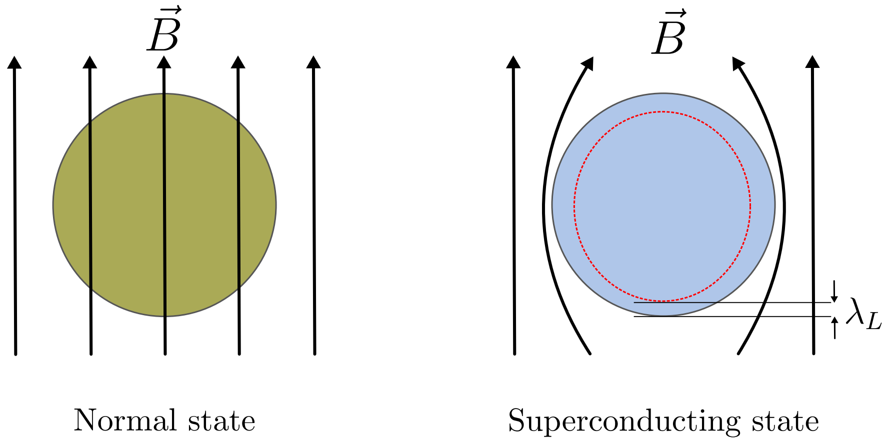


Figure 2.3: Meissner's effect occurs upon transition; hence, magnetic flux does not penetrate the material's interior. The London penetration depth is marked in a red dashed line.

The said behaviour comes with a caveat. If the temperature exceeds the critical temperature T_c, the material will lose its superconducting state. Similarly, a critical current density $\vec{J_c}$ and a magnetic field $\vec{H_c}$ also exist [17]. The material will lose superconductivity if the current density or the magnetic field increases than a specified critical amount. Also, these parameters are not independent of each other. Thus, the maximum critical temperature will be achieved when the critical current and critical magnetic field are the lowest.

As discussed above, the behaviour of superconductors can be two-fold. This nature of infinite conductance and repelling magnetic fields can be approximated in the setting of classical electromagnetic wave theory (from section 2.1.2), although superconductivity is a quantum mechanical phenomenon.

2.2.1 Perfect Electrical Conductor

Since the conductance approaches infinity in a superconductor, one way to model it would be as a Perfect Electrical Conductor (PEC) since it is lossless ($\sigma \rightarrow \infty$). Hence all electric field components in the interior of conductor should be zero. Therefore equations (2.20), (2.21), (2.24), and (2.25) will be reduced to,

$$\hat{n} \cdot \vec{D} = \rho_s \tag{2.26}$$

$$\hat{n} \cdot \vec{B} = 0 \tag{2.27}$$

$$\vec{E} \times \hat{n} = 0 \tag{2.28}$$

$$\hat{n} \times \vec{H} = \vec{J_s} \tag{2.29}$$

2.3 Passive Elements

Passivity in an element can be defined as either thermodynamic passivity or incremental passivity. Thermodynamic passivity dictates that passive elements consume energy rather than produce it[18]. Another way to define passive elements is that these elements are not capable of power gain as per the incremental passivity definition[19].

2.3.1 Capacitor

The fundamental electronic passive element which can store energy in the form of electric fields is a capacitor. The most basic structure would be an insulator within two electrodes. There is a linear relation between the charge accumulated Q and the potential applied V, which can be written as

$$Q = CV \tag{2.30}$$

The basic structure can be graphically represented in Figure 2.4.
The total electric charge accumulated between the plates using the integral form of Gauss's law can be written below.

$$Q = \oint_s \epsilon_0 \epsilon_r E_x \cdot ds = \epsilon_0 \epsilon_r E_x A \tag{2.31}$$

The electric field E_x from applied potential V can expressed as V/d. A is for the surface area. Therefore,

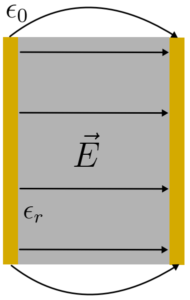


Figure 2.4: Cross section of a parallel plate capacitor

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \tag{2.32}$$

It should be noted that the above formulation does not consider the fringing fields which occur at the edges of the plates. This effect can be neglected if the area of the plates is larger than the separation between them.

As formulated before, the dielectric sandwiched between the plates will have some minor conduction due to the imaginary part of ϵ. Hence, there can be minor leakage between the plates.

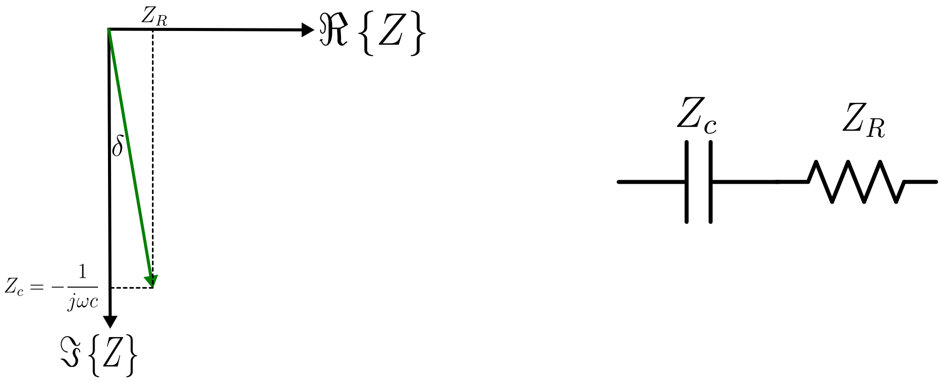


Figure 2.5: Impedance of a capacitor with a lossy dielectric.

2.3.2 Inductor

An inductor is a passive element that stores electromagnetic energy through magnetic fields. The inductance L can be written per equation (2.33) for a simple current-carrying loop.

$$\begin{aligned} L &= \frac{1}{I} \oint_s \vec{B} \cdot ds = \frac{\Psi}{I} \\ &= \mu_0 \mu_r \frac{1}{I} \oint_l H \cdot dl \end{aligned} \tag{2.33}$$

Where I is the current propagating through the conductor, Ψ is the magnetic flux, and S is the surface area covered by the loop of wire with a length of l.

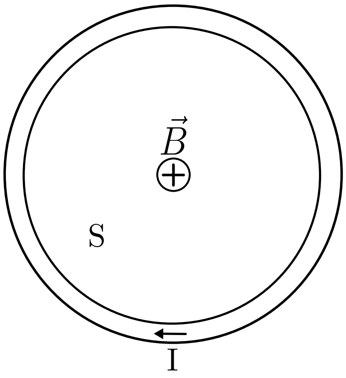


Figure 2.6: Current carrying loop

2.3.3 Quality Factor

Although metals used in this study are lossless, the dielectrics will have complex permittivity, which would contribute to the loss. Quality factor (also known as Q-value) can be used to consider the loss of passive elements and to gauge their merit. This formulation, in its essence, is the ratio between the average energy stored and the energy lost[20].

$$Q = \omega \frac{W_m + W_e}{P_{loss}} \tag{2.34}$$

W_e and W_m are the average energy stored as electric and magnetic fields.

2.3.4 Lumped elements

A lumped element is one of the ways to realize a passive element whose physical dimensions in any direction are much smaller than the wavelength it is operated on such that there will be no significant phase shift between the input and output terminals. The rule of thumb for this dimension is that they will be electrically smaller than one-tenth of the guided wavelength.

The main advantages over distributed elements (discussed in a later section) are that they cover a wider bandwidth[21] and are applicable in lower RF frequencies since wavelength-wise distributed elements will be larger given that the implementation is done as an integrated passive device. These, however, showcase a lower quality factor and considerable parasitic elements at higher frequencies[21]. The specific implementation of such devices will be discussed at length in the "Method" chapter.

2.4 Passive networks

As discussed in the previous chapter, lumped elements are helpful at lower frequencies since the relative phase difference between the terminals of such devices is negligible. Hence concepts from circuit analysis could approximate the electromagnetic field theory. The circuit analysis approximation becomes useful when multiple lumped elements are connected to form a passive network since solving Maxwell's equations for every device and discontinuity is not trivial.

2.4.1 Scattering matrix

The scattering matrix is the relationship between the incident and the reflected waves, taking voltage as the amplitude of the waves. The matrix description wave scattering on a N-port network where V_n^+ is the amplitude of the incidence voltage on the nth port while V_n^- is the amplitude of the reflected voltage can be presented as follows,

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1N} \\ S_{21} & \ddots & & \vdots \\ \vdots & & \ddots & \vdots \\ S_{1N} & \cdots & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{bmatrix} \tag{2.35}$$

$$[V^-] = [S][V^+]$$

The definition for a given element in the S-matrix (When other ports are in open termination) would be,

$$S_{ij} = \frac{V_i^-}{V_j^+} \tag{2.36}$$

For a three-port bias tee device, the elements are graphically represented in figure 2.7.

2.4.2 Idea of reciprocity and lossless

In a reciprocal system, current at one port of the circuit due to some voltage will be the same in another port if the same voltage is applied. If the S matrix for the passive network is symmetric, i.e., $S_{ij} = S_{ji} \quad \forall \quad i, j$, the network is reciprocal [20].

$$[S] = [S]^t \tag{2.37}$$

In a lossless system, no real power will be consumed by the network. It can be shown that the S matrix for a lossless network would be[20],

$$[S][S]^{*t} = [U] \tag{2.38}$$

Where $[U]$ is the unitary matrix.

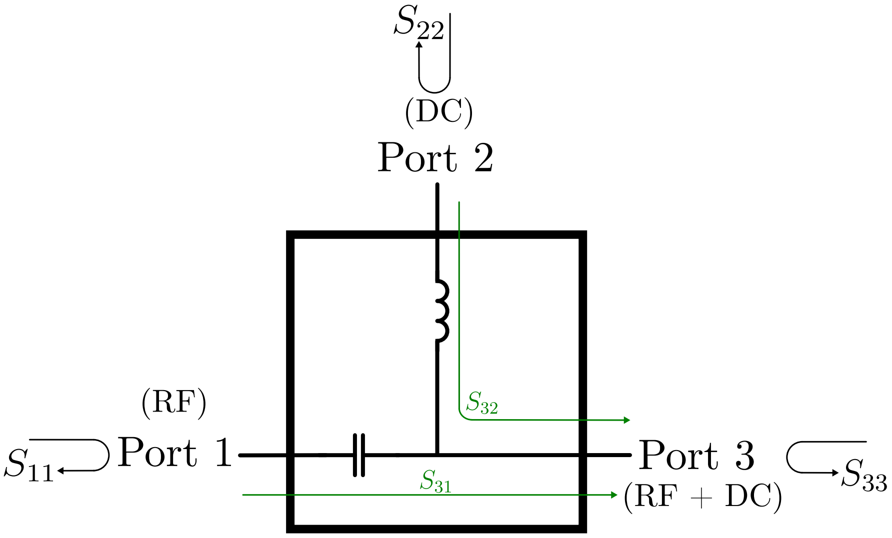


Figure 2.7: Bias tee as 3-port device

2.4.3 Proof of an ideal bias-tee as a three-port device

With these theories introduced before, the bias-tee can be given the network analysis treatment to deduce how it will behave. We first define the S matrix for a 3-port device since the bias-tee is one such.

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{2.39}$$

It can be shown that for a three-port network it is unable to be lossless, reciprocal, and matched simultaneously[20]. Since We know that only the ports which are RF and RF+DC should be matched, we can relax the condition that only two ports will be matched.

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & 0 \end{bmatrix} \tag{2.40}$$

Here, the second port is considered the DC-only port. Hence, we can relax the matching condition $S_{22} \neq 0$. From the unitarity property to be lossless (from equation 2.40) we can also write below conditions.

$$|S_{12}|^2 + |S_{13}|^2 = 1 \tag{2.41}$$

$$|S_{12}|^2 + |S_{22}|^2 + |S_{23}|^2 = 1 \tag{2.42}$$

$$|S_{13}|^2 + |S_{23}|^2 = 1 \tag{2.43}$$

$$S_{13}^* S_{23} = 0 \tag{2.44}$$

$$S_{23}^* S_{12} = 0 \tag{2.45}$$

$$S_{12}^* S_{13} = 0 \tag{2.46}$$

Suppose we assume perfect transmission from the RF port (port 1) to the RF+DC port (port 3) since the ideal model is shorted between ports 1 and 3 ($|S_{13}| = 1$).

$$|S_{12}|^2 = 0 \tag{2.47}$$

$$|S_{22}|^2 = 1 \tag{2.48}$$

$$|S_{23}|^2 = 0 \tag{2.49}$$

Here, we can deduct from the above conditions that port 2 is not matched, which benefits the bias-tee since we do not want any DC power supply ripple to flow into the network. Also, there will be no transmission between the DC port and the remaining port, which is also what we desire in a bias tee for perfect isolation between ports 1-2 and 3-2. Hence, we can show that theoretically an ideal bias-tee does exist under such lossless, reciprocal, and partially matched conditions.

2.5 Waveguide structures

So far, the discussion has been about individual elements and how they would work together in a network. Not much emphasis was given to how passive lumped elements would be connected to form a network. This section focuses on the interconnects that would bring them together. These interconnects should guide the wave without hindrance. Hence the term waveguide structures.

2.5.1 Basic transmission line

We start from the telegraph equation[20], where an infinitesimally short transmission line segment can be presented in Figure 2.8.
We arrive at the travelling wave solution after a much-detailed derivation provided in [20].

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.50}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \tag{2.51}$$

Where γ is the complex propagation constant which can be expressed as,

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.52}$$

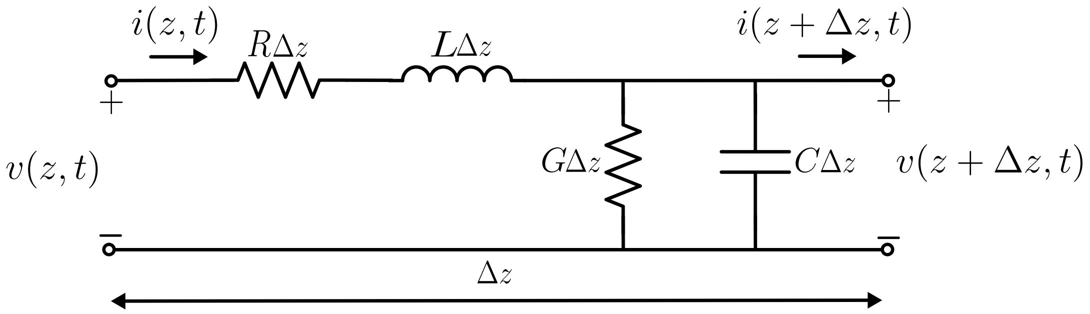


Figure 2.8: Short segment of a transmission line

The characteristic impedance Z_0 can expressed as,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.53}$$

For a superconducting transmission line, there will be no metallic losses. There can be dielectric losses through the substrate.

$$Z_0 = \sqrt{\frac{L}{\frac{G}{j\omega} + C}} \tag{2.54}$$

There are many ways to realize transmission lines. One can investigate the work done in MMICs to understand which suits the best. A microstrip is a metal trace on a dielectric substrate with an infinite ground plane on the back[22]. Graphically, it could be presented as Figure 2.9.

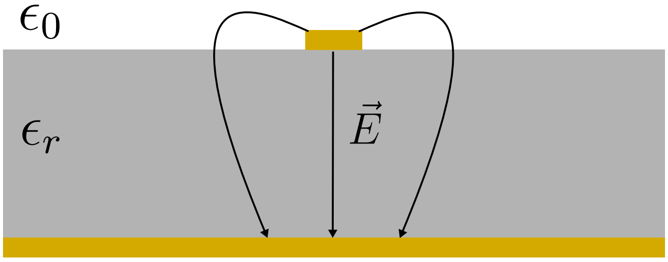


Figure 2.9: Cross section of microstrip line and the $\vec{E}$ distribution

The next most popular one is called the Coplanar waveguide. Here, the metal trace and the ground plane will be on the same side of the dielectric substrate. The width of the centre metal trace and its separation gap with the surrounding ground plane will dictate the line impedance. Its computation will be discussed in the next section. Below is a field profile of such a CPW.

If the $\vec{E}$ and the $\vec{H}$ are orthogonal to the direction of propagation, such waveguide modes are coined as Transverse Electromagnetic (TEM). Observe that in both CPW

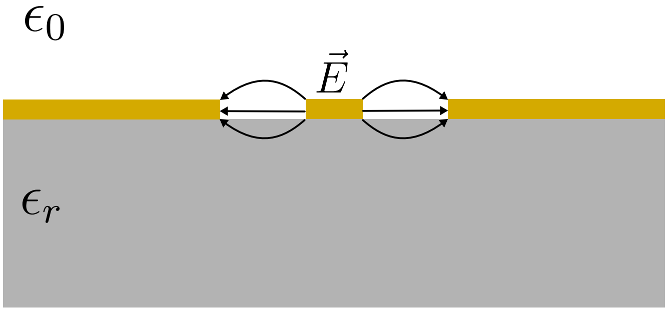


Figure 2.10: Cross section of CPW line and the $\vec{E}$ distribution

and microstrip waveguides, the mode is quasi-TEM[23][24]. This phenomenon is due to the difference between the substrate's dielectric constant and the top space (Mostly air/vacuum). A graphical intuition can be drawn by looking at the E-field. For this work, CPWs are used. The exact design decision for it will be discussed in the next chapter.

2.5.2 Distributed elements

The concept of a passive element was introduced at the beginning of this chapter. Lumped elements were discussed as an approach to realising them. Another way to manifest would be distributed elements. Consider a lossless (in the case of a superconductor) transmission line with a line impedance Z_0 where a load impedance Z_L has terminated it. It can be shown that the impedance looking into Z_{in} one such configuration varies with the length l of the termination[20].

$$Z_{in} = Z_0 \left(\frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \right) \tag{2.55}$$

Here β is the propagation constant. If we are to give a short circuit condition at the termination $Z_L = 0$ the above equation simplifies as:

$$Z_{in}|_{Z_L=0} = jZ_0 \tan(\beta l) \tag{2.56}$$

Similarly when it is open circuited,

$$Z_{in}|_{Z_L=\infty} = -jZ_0 \cot(\beta l) \tag{2.57}$$

These conditions can be used to engineer passive elements which rely on the operating wavelength. An example of one such element would be a shunted capacitor. If we are to use an open-circuited load termination with a termination length such that it corresponds to a quarter wavelength, then $Z_{in} \to 0$ when $\lambda \to 4l$.

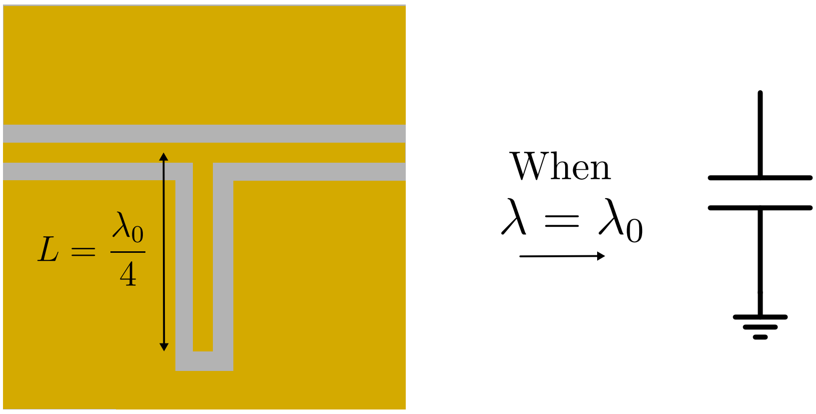


Figure 2.11: Shunted capacitor realized through open stub

Likewise, If we are to use a short circuited load termination with a termination length such that it corresponds to a quarter wavelength, $Z_{in} \to \infty$ when $\lambda \to 4l$.

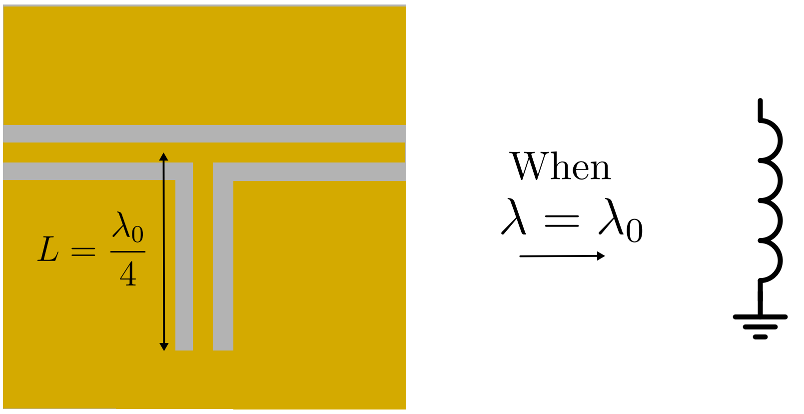


Figure 2.12: Shunted inductor realized through open stub

3

Methods

In previous chapters, the required theoretical foundation was laid to understand physics and mathematics, enabling engineering a bias-tee. It was shown mathematically that an ideal bias-tee does exist. In reality, what will be achieved is an approximation of the ideal. In this chapter, the engineering design choices that have been made are discussed and motivated.

As discussed in the first chapter, there exists a need in the quantum computing market for superconducting bias-tees. The IPD approach poses both attractive advantages and disadvantages and relies on the clean room facilities in the fab house.

3.1 Fabrication limitations

Limitations or design rules follow from the equipment which we deem useful. The exact design steps are out of the scope of this thesis work. How these exact tools work can be found in [25]. The following tool descriptions are intended to highlight the design rules.

3.1.1 Laser writer

This tool will be used to pattern structures for the IPD. The laser will beam on the photoresist according to the desired pattern. Examples of these patterns could be the gap between the signal trace for the CPW and ground and the rectangular pads (electrodes) of a capacitor. From the design perspective, this sets the limit to the minimum size of a structure, whether it be a waveguide structure or a lumped component.

3.1.2 Sputter

The sputter tool will deposit the chosen metal onto the substrate.

3.1.3 Reactive ion etcher

This tool is used to etch the dielectrics indented for this IPD design.

3.2 Material selection

The most suitable material should be chosen to realize the bias-tee as an IPD. In short, we require metals that can superconduct as metal traces dielectrics with less loss.

3.2.1 Metal

The metals chosen for the bias-tee should superconduct when cooled down. There are several choices in selecting metal. One of the key criteria would be the critical temperature. Lower T_c means less strain will be demanded on the cryostat since that can be placed at a higher stage. The following are key characteristics of promising materials.

Table 3.1: Candidates for the superconductor

Superconductor	Al	TiN	Nb
T_c (K)	1.175	5.1	9.25
Oxidation	Yes	Highly resistant	Yes
Reaction with Au	Corrodes	Diffusion barrier	Intermetallic compound
Melting Temperature (C)	660.0	2950	2477
Ref	[26][27][28][29]	[30][31][32]	[33][34][35][36]

From the above-tabulated data, the most attractive solutions would be TiN and Nb since Al has lower T_c than aluminium. However, some studies show that fabricating Nb and reaching a superconductive state is not that trivial, given that the purity of Nb is of concern [37]. Oxides will induce surface loss on the superconducting metal [38]. Furthermore, TiN is highly resistant to oxidation.

3.2.2 Dielectric

There are many materials to use when selecting a dielectric. AlN was selected, taking its low-loss tangent and fabrication compatibility into consideration.

Table 3.2: Candidates for insulators

Dielectric	ϵ_r	loss tangent	Ref
AlN	10.4	0.002	[39]
Polyimide	3	0.005	[40]

The material stack-up needs to be oxide-free [38]. Hence, choosing an oxide-free dielectric would be optimal. To realise MIM capacitors, a dielectric with a higher dielectric constant is ideal for increasing area efficiency.

A printed inductor will have inter-winding capacitance (which will be discussed in the next chapter). Therefore, the coil should be printed on a substrate with a less dielectric constant to reduce this capacitive coupling. Polyimide has been used as an insulation material for inductors in prior work[41].

3.2.3 Substrate

All the structures must be built on top of a supporting structure. The supporting base layer, called the carrier or the wafer, will also function as the substrate for the waveguide structures.

Table 3.3: Candidates for Substrate

Wafer	ϵ_r (K)	loss tangent	Ref
High-Resistivity Si	11.7	2.7e-6	[42]
Quartz	3.7	4e-4	[43]

Silicon seems attractive given its popularity, but attention must also be given to the wafer's dielectric constant since it will be one of the critical components contributing to parasitic capacitive coupling for the components. More details of this will be provided in the capacitor results section.

3.3 Comsol Simulations

The 3D FEM tool used in this thesis work is COMSOL. The general procedure for COMSOL simulations is first to design a model of the passive component or waveguide structure in the built-in CAD environment. Next is to assign boundary conditions. Next, we proceed to mesh, where the model's 3-dimensional space is discretised in the form of minute polyhedrons (e.g., tetrahedrons, bricks, prisms, pyramids). Using around ten linear mesh elements per wavelength is required to resolve a wave correctly. Finally, EM fields will be evaluated for each element, and data will be presented.

3.3.1 Meshing

The meshing tool in COMSOL struggles when the structure modelled consists of stark differences in dimensions. For example, the stack-up described in the previous section includes structures with thicknesses of 300um and 20nm stacked on top of each other. Meshing techniques exist for symmetrical structures, such as swept mesh. The geometry to be meshed should have a source and a destination face, and the path between them will be meshed using bricks or triangles. Also, the cross-section between these faces should not be changed for a successful swept mesh. Furthermore, manual meshing is not trivial when the structure is not symmetrical. A practical workaround for this dilemma is to approximate a thin sheet of metal as a 2-dimensional object or, in other words, an infinitesimally thin sheet.

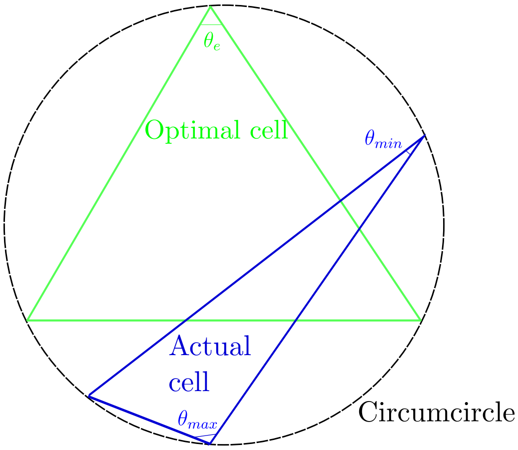


Figure 3.1: Optimal vs Actual mesh cells

3.3.1.1 Quality of the mesh

The skewness parameter can be used to gauge the quality of the mesh [44]. The said metric is easy to visualize for 2D mesh elements, which are triangular and quadrilateral.
Skewness can be expressed analytically as,

$$\text{Skewness} = 1 - \max\left(\frac{\theta_{max} - \theta_e}{180 - \theta_e}, \frac{\theta_e - \theta_{min}}{\theta_e}\right) \tag{3.1}$$

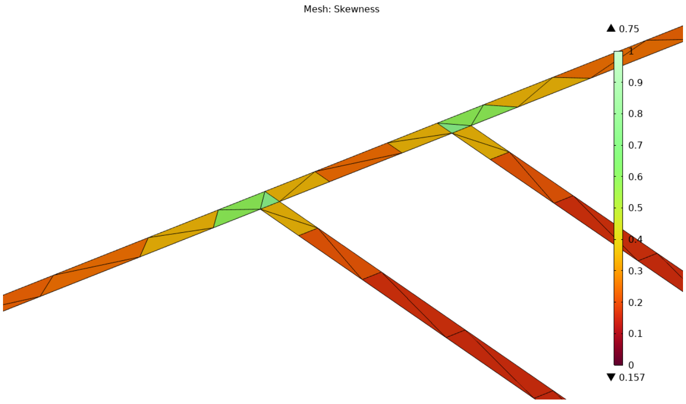
θ_e is the angle for an equiangular cell (e.g., 60 for triangle and 90 for square), while θ_{max} and θ_{min} are the largest and the smallest angles in the cell. The value can be between 0 and 1, where 1 represents a perfectly regular element. 0 represents a degenerate element[44]

The Skewness of mesh elements can change according to the size of the mesh element and the specific dimensions it needs to be meshed. In Figure 3.2, gaps between the signal trace and the ground have been meshed with two different mesh sizes. The finer the mesh, the less skewed the elements will be. Hence, the sizing of the mesh depends on the feature size it needs to cover.

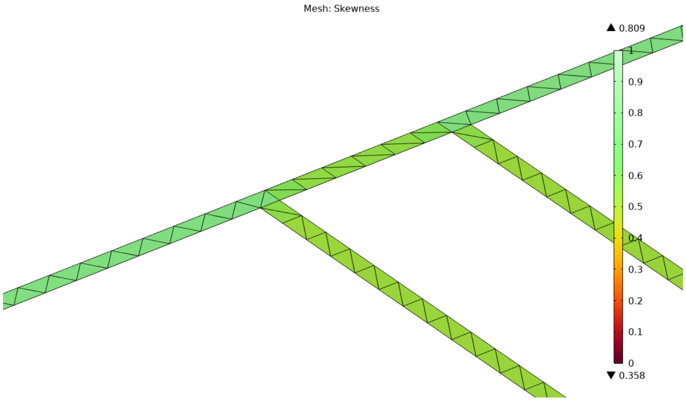
3.3.1.2 Thin film metal layers

As discussed in the theory chapter, superconducting metals will be modelled as PEC. Furthermore, COMSOL has PEC as a boundary condition for its electromagnetic solver. We first start with a cross-section of the CPW (specifically the metal interface) at the port interface to investigate the incident ($\vec{E}_i$,$\vec{H}_i$) and reflected fields ($\vec{E}_r$,$\vec{H}_r$). The port is excited as TEM mode (quasi-TEM, to be precise).

From the PEC boundary condition, it can be said that no fields will enter the metal. In fact, it "shorts out" the incoming electric field. Hence, the reflection coefficient



(a) Coarse triangular mesh



(b) Finer triangular mesh

Figure 3.2: Quality of mesh changing due to feature size mapped

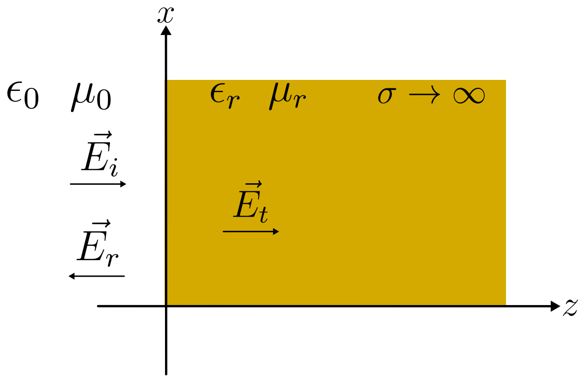


Figure 3.3: Normal incidence from a wave onto a superconductor

will be –1. The total wave can be expressed as below.

$$\vec{E} = \vec{E}_i + \vec{E}_r = \hat{x}E_0(e^{-jk_0z} - e^{jk_0z}) = -\hat{x}2jE_0\sin(k_oz) \quad (3.2)$$

$$\vec{H} = \vec{H}_i + \vec{H}_r = \hat{y}\frac{1}{\eta}E_0(e^{-jk_0z} + e^{jk_0z}) = -\hat{y}\frac{2}{\eta}E_0\cos(k_oz) \quad (3.3)$$

A more detailed description of this is provided in [20]. The volume current density can be found by,

$$\vec{J} = \hat{n} \times \vec{H} = -\hat{z} \times \left(\hat{y}\frac{2}{\eta}E_0\cos(k_oz)\right) \quad (3.4)$$

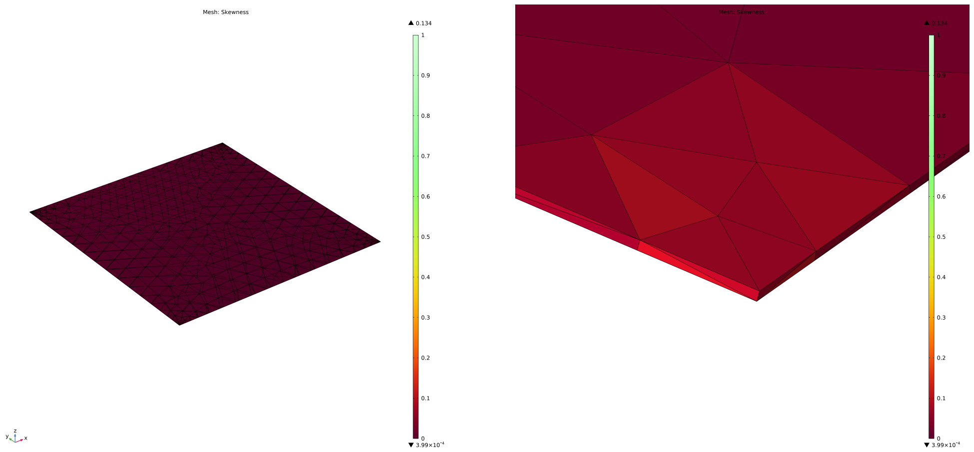
At the interface where $z = 0$, it is reduced to an infinitesimally thin sheet of surface current,

$$\vec{J}_s = \hat{x}\frac{2}{\eta}E_0 \quad A/m \quad (3.5)$$

The perimeter of the cross-section in a waveguide structure is of concern rather than the area of the cross-section. Therefore, when the dimensional contrast between the width and thickness is high, a 3D metal sheet can be approximated as a 2D sheet (when the metal is modeled as a PEC).

3.3.1.3 Thin film dielectric layers

Electromagnetic waves will penetrate dielectric layers. Hence, it cannot be approximated as a 2D layer since we are interested in how fields behave inside the media. However, having a high aspect ratio (e.g., Both width and length at 250um while thickness is 20nm), structures will result in mesh elements with poor quality.



(a) Overall Volume **(b)** Zoomed in view at edge

Figure 3.4: Quality of mesh using free tetrahedral mesh for thin films

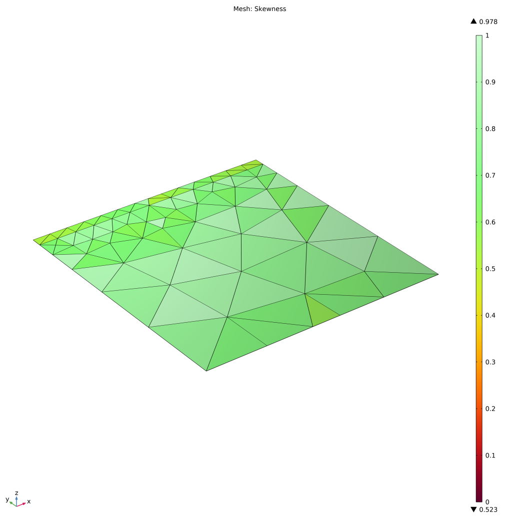


Figure 3.5: Quality of mesh using swept mesh for thin films

The thin film shown in Figure 3.4, when simulated, will either give inaccurate results or will not converge at all. The best way to mesh such a structure would be to use a swept mesh where the thin film will be approximated with either prisms or bricks.

3.3.1.4 Meshing Sequence

We start with a thin structure that is a few nanometers but wide in the several micrometre ranges, which is also deposited on the wafer, which is several hundred micrometres in thickness and encased in an air volume, which is also thick compared to the deposited structure. Graphically, it can be represented as Figure 3.6.

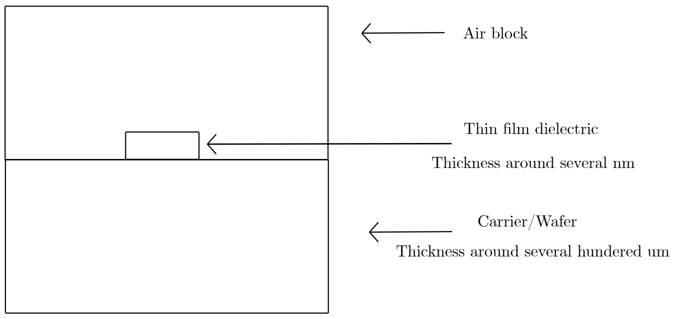


Figure 3.6: Cross section of a thin film structure deposited on a wafer

Next, the volume of which the thin film structure is part of(air in this scenario) is separated into two sub-volumes, as shown in Figure 3.7.

Furthermore, the swept mesh is employed to mesh the thin film along the thickness axis. We also have a surrounding air volume with a thickness as the thin film structure, which is meshed using a swept mesh along the thickness axis. If the surrounding area is wide enough compared to the thin structure, one can have coarser element sizes for the second swept mesh, as shown in Figure 3.8.

Finally, per Figure 3.9, the rest of the volume can be meshed using free tetrahedrals.

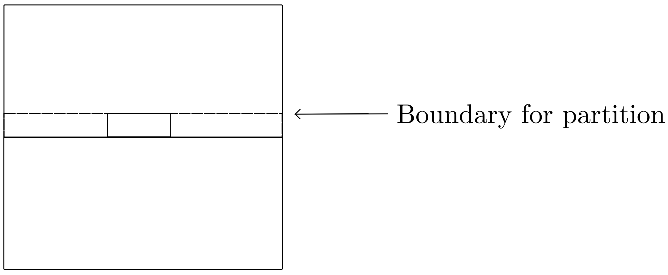
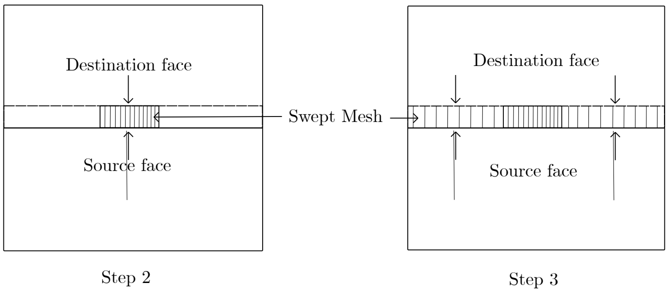


Figure 3.7: Step 1: Partitioning the volume thin film structure encased in



Step 2

Step 3

Figure 3.8: Step 2 and 3: Swept mesh of volumes which are thin

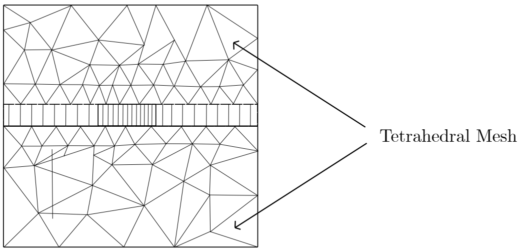


Figure 3.9: Step 4: Free tetrahedral mesh for the rest of the volume

3.3.2 Other Boundary Conditions

Apart from the perfect electrical conductor boundary condition (which was used to model the lossless metals), We also require two more boundary conditions to solve the 3D FEM problem. These boundary conditions are used to model the boundaries of the model, which are not metalized, and also the boundaries that will be used to feed electromagnetic waves into the model.

3.3.2.1 Scattering

The scattering boundary condition can make a boundary transparent for a scattered wave when the wave is at normal incidence to the boundary. Any incoming plane waves will be absorbed [45].

The material adjoining the scattering boundary can be lossy. Hence, it can be used to model non-metalized walls of a lossy dielectric (e.g., wafer material)

3.3.2.2 Port

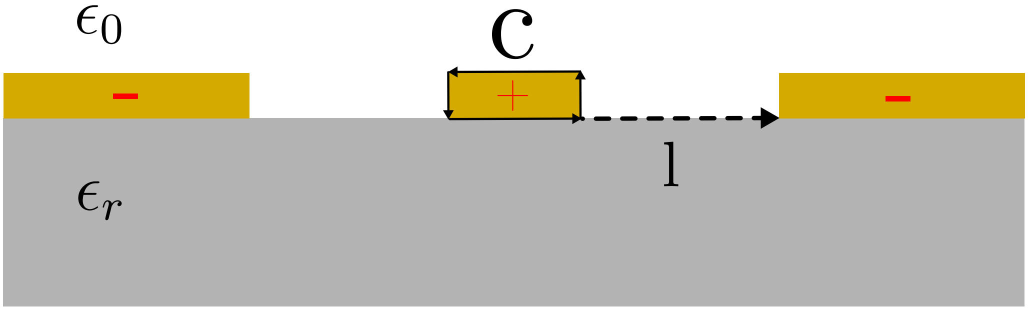


Figure 3.10: CPW port with integration contour c in solid line and integration line l in dashed lines

A port boundary condition excites or absorbs electromagnetic energy distributed as a specific mode. Among many port conditions available in COMSOL, Numeric parts are chosen with the option to ”Analyze as a TEM Field". The waveguide structure is a two-conductor system with different dielectric constants separating the conductors. Hence, the option evaluates the quasi-TEM mode the structure can support. The "Integration Line for Voltage" subfeature is required to evaluate the port mode impedance [45].

$$V = \int_{+}^{-} \vec{E} \cdot d\vec{l} \tag{3.6}$$

$$Z_0 = \frac{V^2}{P} \tag{3.7}$$

The integration line for voltage starts from the + conductor and ends on the - conductor. Then impedance can be calculating using power. "Integration Line for Current " sub feature is also available although it is optional[45].

$$I = \oint_C \vec{H} \cdot d\vec{l} \tag{3.8}$$

$$Z_0 = \frac{V}{I} \tag{3.9}$$

Here, the integration pathway is a loop enclosing the positive conductor. The path for the integration line for voltage and contour for current are highlighted in Figure 3.10.

3.4 Passive lumped components

In the theory chapter, we discussed the concept of a passive element described as storing energy and having losses. We then introduced lumped elements and distributed elements as means to realize them. Finally, in this chapter, we now focus on how to manifest them physically.

When realizing passive elements as lumped components, we are bound to manifest undesired extra passive elements due to the structural elements of the component. These passive elements in the lumped components impede the behaviour of the desired operation. Hence, they are called parasitic elements. Almost all dielectric materials will incur a loss. Metals also have finite conductivity hence inducing a skin effect which acts as resistance.

3.4.1 Monolithic Capacitors

In the previous chapter, the passive element known as the capacitor was introduced. This section will focus on realizing a passive lumped component from that idea. Monolithic or integrated capacitors are threefold. The easiest to implement would be a small length of an open-circuited CPW, which is a distributed element and will be helpful only at the design frequency used to calculate the length. Since we require a broadband operation, those will not be considered. For moderate capacitance, interdigital capacitors can be used, while MIM capacitors provide the highest capacitance per unit area[21]. However, MIM capacitors do require a multilevel process.

3.4.1.1 Interdigital capacitor

At a glance, interdigital capacitors can be seen as comb structures. The capacitance is formed between the gaps of this multifinger periodic structure.
Capacitance can be improved by increasing the number of fingers or depositing a thin dielectric layer with a higher permittivity between the fingers. The length of the fingers l can be increased, or the gap between the fingers s can be decreased to more capacitance [46], albeit one should be paying attention to the maximum operating wavelength of the respective bandwidth. Since at higher frequencies it may not be considered as a lumped element.

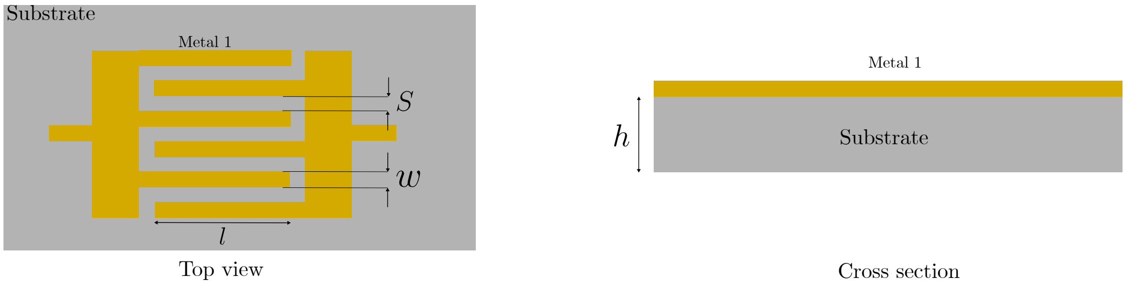


Figure 3.11: Interdigital capacitor physical model

3.4.1.2 MIM capacitor

MIM capacitors are the closest approximation for parallel plate capacitors. It is simply a thin film of dielectric material sandwiched between metals. Fabrication does add an extra level of complexity since it requires etching away specific shapes of the added dielectric and later adding more metal to form the other plate of the capacitor.

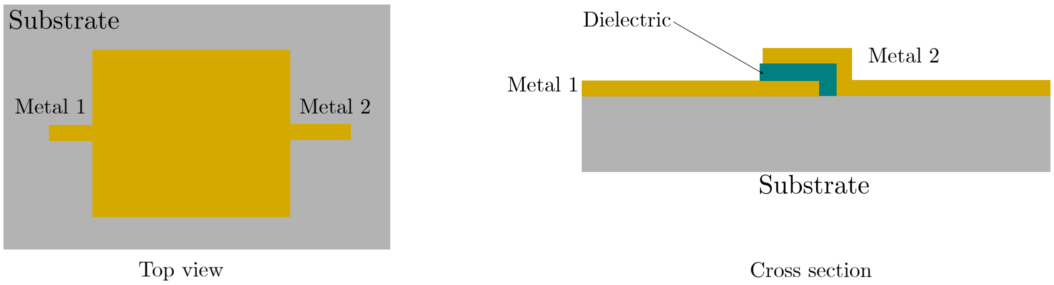


Figure 3.12: MIM capacitor physical model

As per literature[47], the equivalent circuit for an MIM at high frequencies can be presented in Figure 3.15. Resistivity R_{skin}, which occurs due to skin effect can also be neglected since the electrodes will be superconducting. What remains will be the inductive nature of the electrodes L_p which must be addressed at high frequencies. The parallel resistance G_1 is due to the undesired conductivity of the dielectric. The shunted parasitic branches manifests due to two reasons. One is because of the undesired coupling to the ground plane. The remaining parasitic elements are due to the metallic impurities in the dielectric[48].

The 3D model is depicted in Figure 3.13, while Figure 3.14 shows the mesh quality histogram plotted regarding the skewness of the mesh elements. The physics-controlled mesh generates many mesh elements that are low in skewness parameters. A user-controlled mesh was used to ensure an accurate solver result, and the majority of mesh elements have a quality exceeding 0.6.

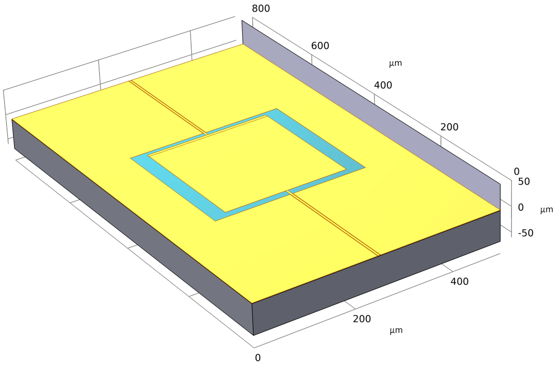


Figure 3.13: MIM capacitor modelled in COMSOL

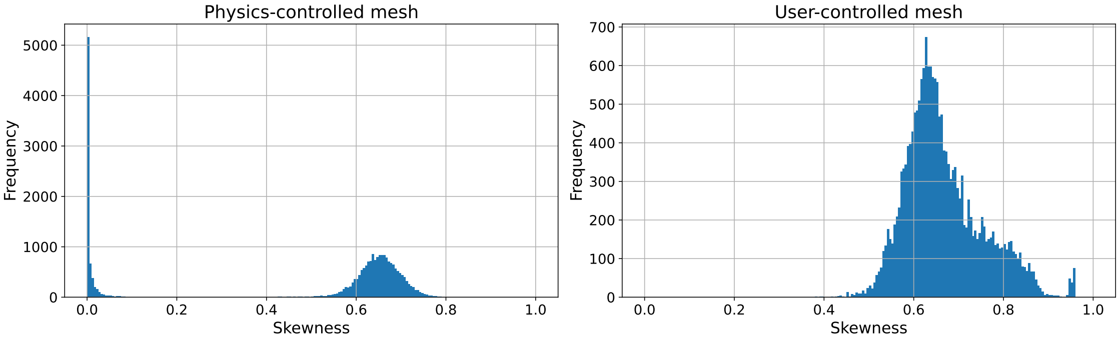


Figure 3.14: Skewness of the MIM capacitor model mesh for physics and user controlled mesh

3.4.2 Printed Inductor

Inductors can be on the substrate as two-dimensional structures with minor thicknesses. The shape can be either meandering or spiral. Meander lines typically have lower inductance[21]. In the early days of MMIC design, rectangular spirals were used. However, with time, 90 degree angles were avoided, and octagonal spiral shape was used with more enabling technologies. These days, circular spirals are used chiefly with less parasitic since avoiding sharp corners leads to less charge accumulation[21].

A formulation to calculate a coil inductor was first proposed by Wheeler[49]. The model for the inductor fabricated on silicon is shown in Figure 3.18 [50].

The skewness of the mesh for the 3D model can be plotted as a histogram in Figure 3.17. The built-in physics-controlled meshes in COMSOL fail to generate the required mesh where most mesh elements are low. User-controlled mesh, however, is far superior, with most mesh elements meshed with a skewness of more than 0.6.

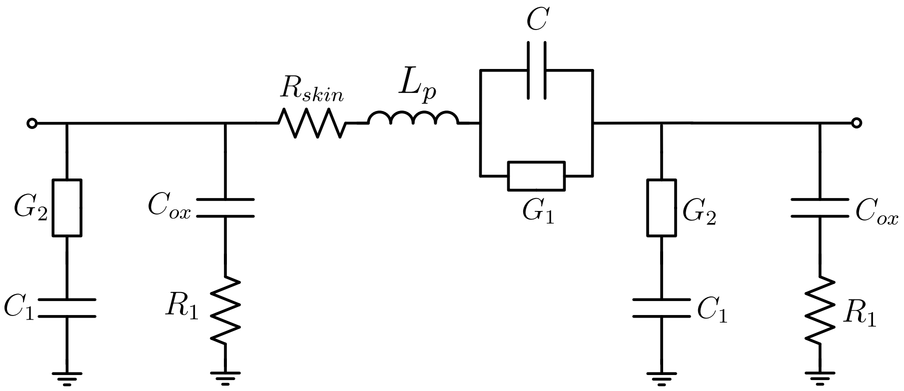


Figure 3.15: MIM capacitor equivalent circuit model

Top view

Cross section

Figure 3.16: Printed inductor physical model

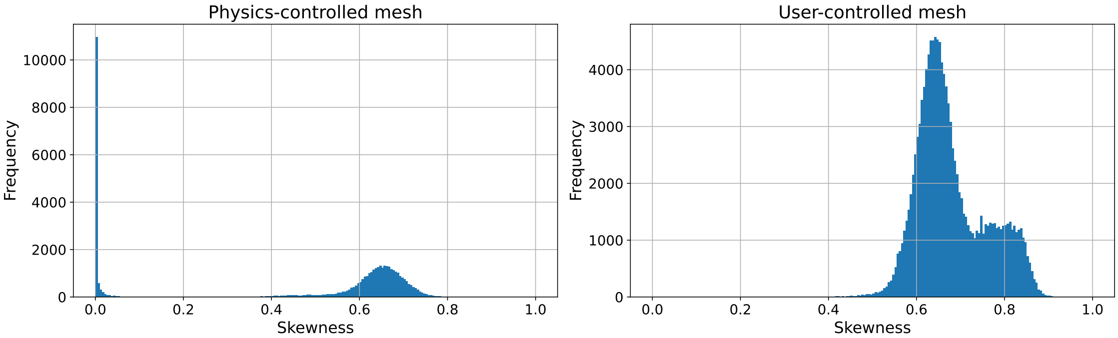


Figure 3.17: Skewness of the inductor model mesh for physics and user controlled mesh

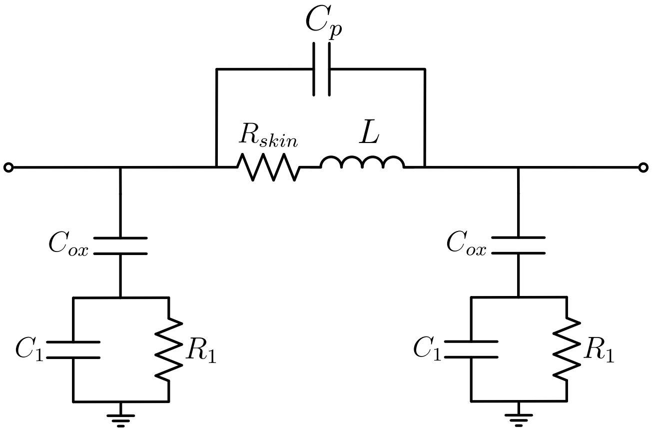


Figure 3.18: Printed inductor equivalent circuit model

The inductance of a planar coil is given below as per[21],

$$L \quad (nH) = 0.03937\frac{a^2n^2}{8a+11c} \cdot K_g \tag{3.10}$$

The parameter n denotes the number of coil turns. When the inner diameter D_i and the outer diameter D_o of the coil are known, parameters a and c can be calculated as below[21],

$$a = \frac{D_0 + D_i}{4} \tag{3.11}$$

$$c = \frac{D_0 - D_i}{2} \tag{3.12}$$

Meanwhile, parameter K_g encapsulates the ground plane effect. The K_g value will decrease when the ground plane is brought nearer, and it is a function of the width of the trace W and the distance to the ground plane h [21]. The parameter K_g is formulated as,

$$K_g = 0.57 - 0.145ln\frac{W}{h} \tag{3.13}$$

The parasitic capacitance C_p occurs due to the capacitive coupling between the windings, which is given by the following form[21].

$$C_p \quad (pF) = 3.5 \times 10^{-5}D_0 + 0.06 \tag{3.14}$$

3.4.3 Parasitic extraction

The equivalent circuits described here can be approximated to be a pi-network. Its components can be shown as impedances and admittances in Figure 3.19.

To analyze how these parasitic elements behave one can export the s-parameters from COMSOL and convert it to respective admittance components. A formal introduction to admittance parameters is given in the reference [20].

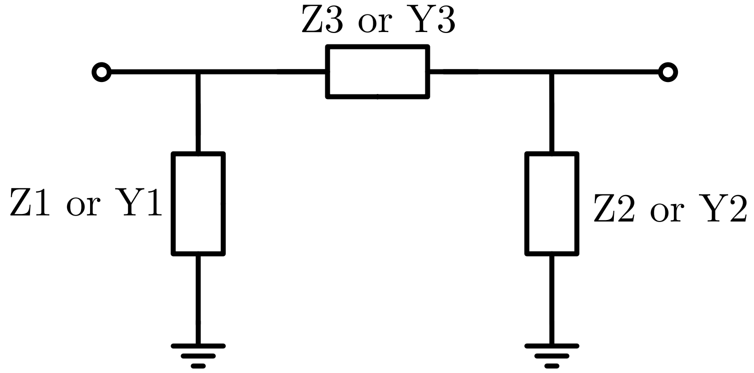


Figure 3.19: Π circuit model

$$
\begin{gathered}
[S] \Rightarrow [Y] \\
\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_1 + Y_3 & -Y_3 \\ -Y_3 & Y_2 + Y_3 \end{bmatrix}
\end{gathered} \tag{3.15}
$$

Impedances of each component can be written in terms of Y-parameters as bellow,

$$Z1 = \frac{1}{Y_{11} + \text{AVERAGE}(Y_{12}, Y_{21})} \tag{3.16}$$

$$Z2 = \frac{1}{Y_{22} + \text{AVERAGE}(Y_{12}, Y_{21})} \tag{3.17}$$

$$Z3 = \frac{-1}{\text{AVERAGE}(Y_{12}, Y_{21})} \tag{3.18}$$

3.4.4 Quality factor calculation

Once a full wave simulation is done, the quality factor can be evaluated using S parameters. We first start with defining the Q factor using the reference [51].

$$Q = \frac{\omega L}{R} = \frac{1}{\omega C R} \tag{3.19}$$

Equation (3.19) can be written as the ratio of the imaginary component to the real impedance component.

$$Q = \frac{\text{Im}(Z)}{\text{Re}(Z)} \tag{3.20}$$

S parameters are converted from two ports to one port, as shown in Figure 3.20. Then, Z-parameters are converted from the one-port S-parameters.

$$[S] \Rightarrow [Z] \tag{3.21}$$

$$Q = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} \tag{3.22}$$

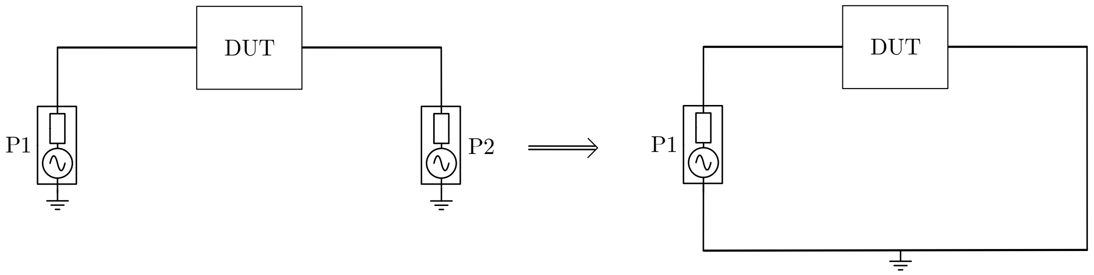


Figure 3.20: Two port to one port configuration

3.5 Design choices

From the information given above, we can now select devices and structures and motivate the design choices.

3.5.1 Component and structures

3.5.1.1 Waveguide structure

The typical waveguide structures realized on MMICs are two conductor systems[52]. Hence, a ground plane will be present. Moreover, as per the previous discussion, it will create parasitic shunting branches. The said effect can be minimized if there were to be fewer parallel surfaces to the signal trace. Therefore, CPW structures are much suited as interconnects.

3.5.1.2 Waveguide dimensions

The requirement for waveguide dimensions is twofold. First, we require the waveguide to have a characteristic impedance of 50 Ω. Also, it should be able to withstand a current of 10 mA without exceeding the critical current density such that the waveguide would lose the superconducting state. Given the minimum feature size of the laser writer, the line impedance will be 49.95 Ω.

3.5.1.3 Capacitor of choice

The capacitance per inch area of interdigital capacitors is less than 1% of the total MIM capacitance[21]. Hence, the MIM capacitor is the capacitor of choice.

3.5.1.4 Inductor of choice

For the inductor, a circular shape was chosen since they have the highest self-resonance frequency compared to rectangular or octagonal counterparts[21].In addition, the track width of the inductor was selected to be the lowest width the laser writer could pattern, which is less than the trace width of the 50 Ohms line. Hence, the line itself will be more inductive.

3.5.2 Proposed stackup

From the motivated design choices, a stackup can be proposed as below.

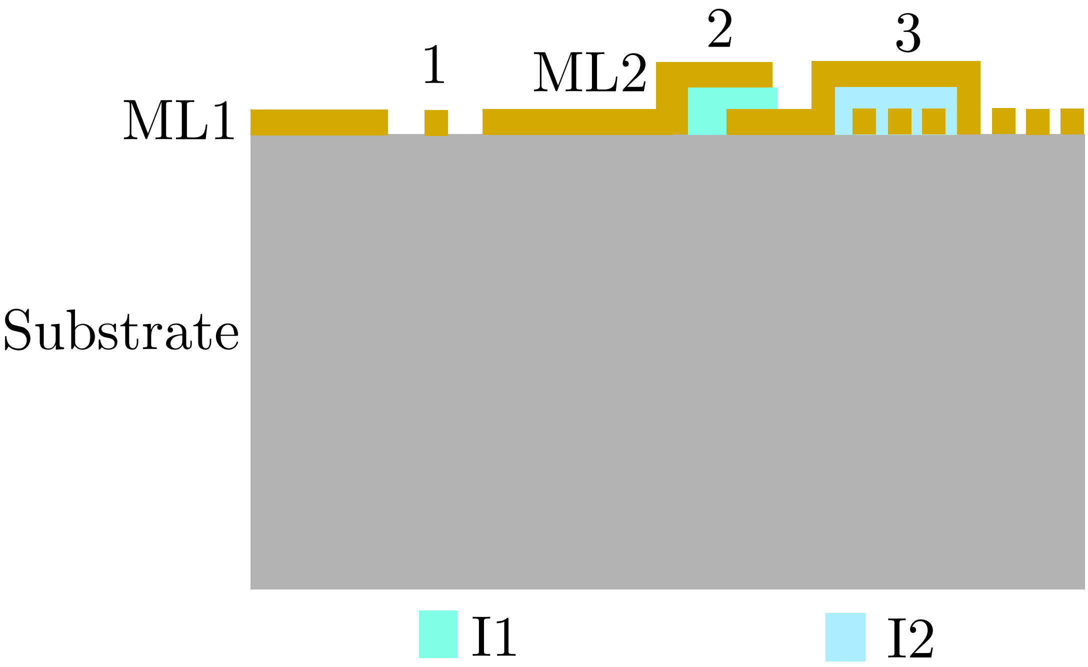


Figure 3.21: Proposed stackup with required features

The features required will be:

1. 50 Ω coplanar waveguide
2. MIM capacitor
3. Cicular coil inductor
4. ML1 - Metal Layer 1
5. ML2 - Metal Layer 2
6. I1 - Insulator for MIM capacitor
7. I2 - Insulator for inductor

4

Results

We first start with how the bias-tee would perform with ideal elements. Next, passive components will be designed to attain those impedances. Moreover, their characteristics will be discussed. Finally, those results will be combined to attain S-parameters of the bias-tee with real components.

4.1 Bias tee with lumped elements

The initial design of the bias-tee will be with ideal lumped elements. Design done from ideal components will be the starting point for the design of lumped components. The target is a DC cutoff at 10 MHz and an AC coupling frequency of 100 MHz. A schematic-level representation is provided in Figure 4.1.

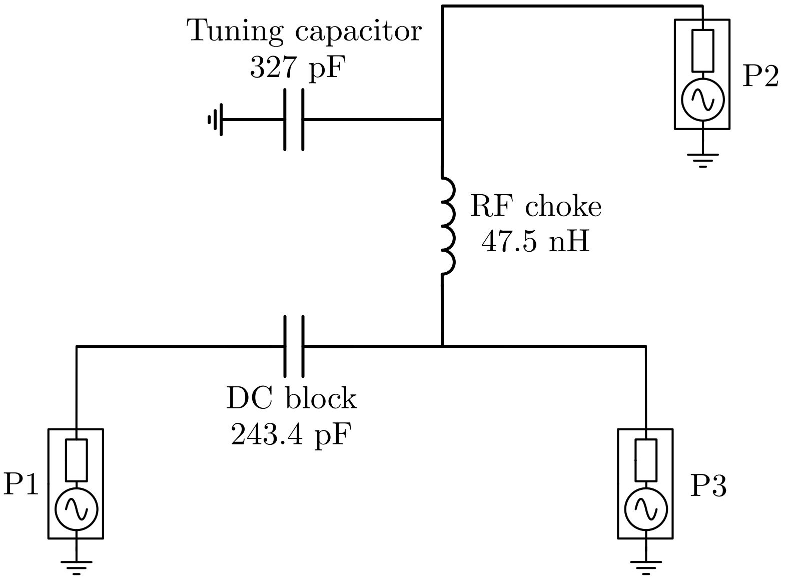


Figure 4.1: Bias tee design with ideal lumped elements

All the ports are measured relative to 50 Ohms of impedance. An additional capacitor is used in the inductive branch to tune the circuit to ease the inductor (RF choke) requirement. Physically, the power supply noise will be short to ground through this shunting capacitor. The required cutoff frequencies and the ideal element performance are shown in Figure 4.2. $S[3,1]$ signifies the insertion loss of the bias tee and $S[2,1]$ signifies the isolation between the DC and the RF branch.

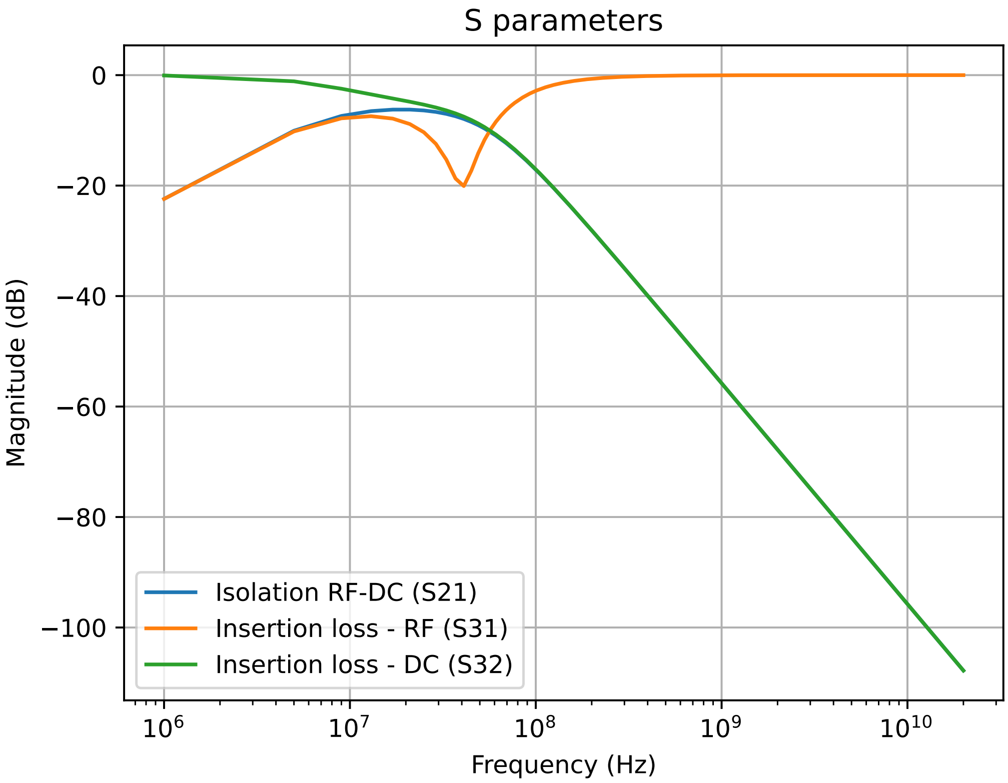


Figure 4.2: Performance of bias-tee design with ideal lumped elements

4.2 Capacitor performance

We first start with modelling the capacitors required. As discussed earlier, the MIM capacitance can be approximated as a parallel plate capacitor. If the plates of these capacitors are to be a square, the length per side can be given as,

- DC block(243.4 pF): 230um, which is actually 243.7 pF
- Tuning capacitor(327 pF): 266um, which is actually 326 pF

Since we are limited to a minimum feature size as discussed in the previous chapter, these closest numbers will be used. For a much more accurate capacitance evaluation, COMSOL was used to simulate. The electric field, $\vec{E}$ can be seen in Figure 4.3.

4.2.1 Effect of the substrate

As discussed in the previous chapter, the effect of the substrate should be considered since it can dictate the parasitic coupling between the capacitor and the ground. The same capacitor can be simulated in both substrate to shed light on this phenomenon. Figure 4.4 shows the s-parameter performance of these MIM capacitors

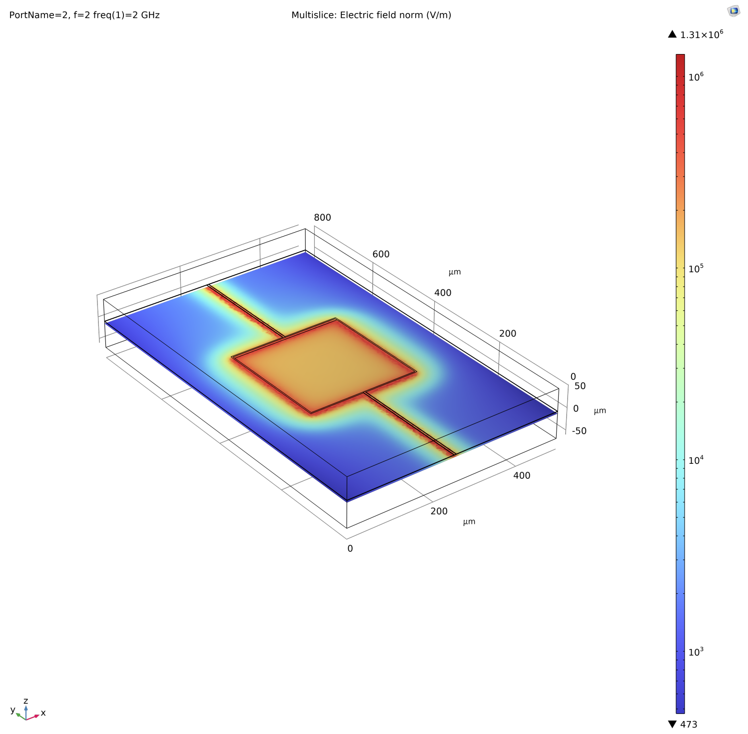


Figure 4.3: E-field distribution of MIM capacitor. Logarithmic colour mapped

in two different wafers.

MIM capacitors realized on quartz have less transmission loss (S_{21}) than when realized on silicon substrate. This parasitic shunt coupling can be lessened if implemented on a wafer with a lower dielectric constant.

As per the reflection data on the Smith chart (Figure 4.4), the MIM capacitor realized on Silicon crosses the real axis at 23 GHz, where it transits from the capacitive zone to the inductive zone. Hence, a MIM capacitor made on a silicon substrate will reach the self-resonance frequency much earlier than a capacitor made on quartz.

4.2.2 Quality factor of the realised MIM capacitors

The quality factor for a capacitor is a figure of merit that determines how well it can store energy in the form of electric fields. Although both capacitors discussed above use AlN as the dielectric, they are made of different substrate materials. Since the electrodes are superconducting, the only changing variable are the dielectric constant, the loss tangent of the substrate. Since the scattering boundary condition was used for the air and dielectric boundaries, radiation losses also impact the Q factor.

Figure 4.5 shows that the capacitor realised on silicon has the highest Q value of 1247.5 at 2.5 GHz, while the capacitor realised on quartz has a peak of 1212.5 at 4.5 GHz. However, after its highest peak, the capacitor made on silicon will have

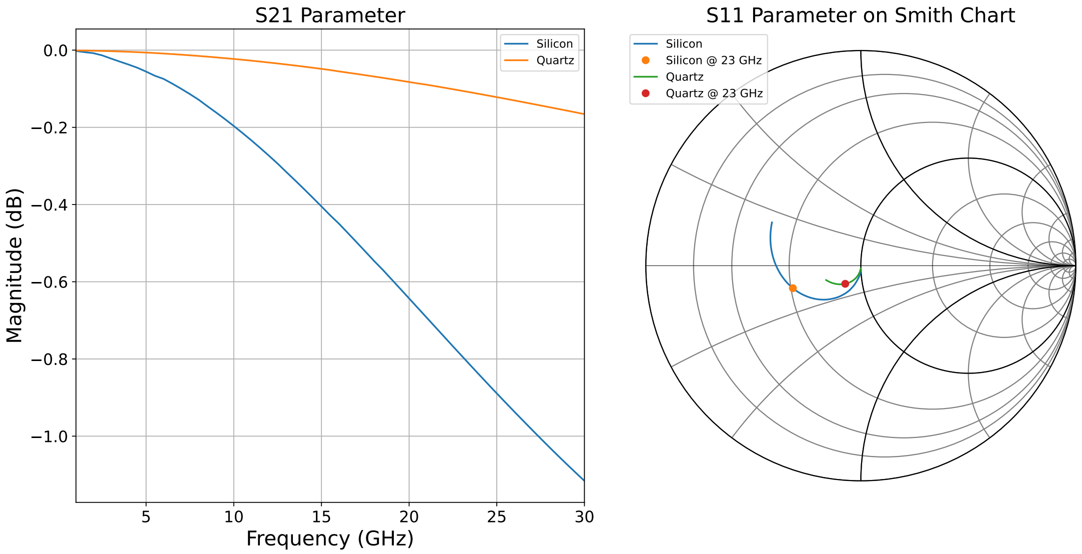


Figure 4.4: S parameter performance of MIM capacitors on different substrates

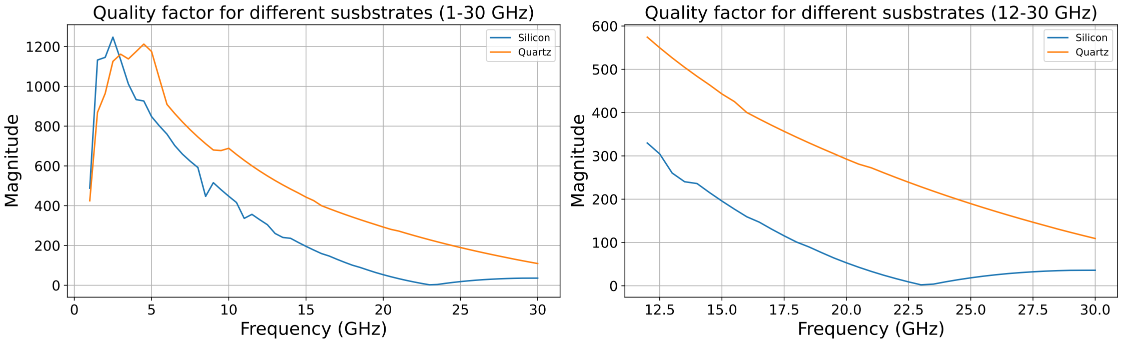


Figure 4.5: Q factor of MIM capacitors in different substrates

a lower Q value than the capacitor realised on quartz. The contrast is much more evident in high frequencies.

As discussed before, the self-resonance frequency of the capacitor made on silicon at 23 GHz is also evident in terms of the Quality factor, where the value dips to 0 since it is only resistive at that frequency point.

4.2.3 Parasitics of MIM capacitors

As per the discussion so far, the moment a capacitor is created, unwanted inductances and resistances are embedded with the wanted passive element. These can be dismantled and studied separately by approximating the capacitor to be a pi network. Such elements can be analyzed by embedding Z1,Z2, and Z3 components as listed in section 3.4.3.

4.2.3.1 Shunt elements

We start by analysing the coupling to the ground plane regarding shunt elements.

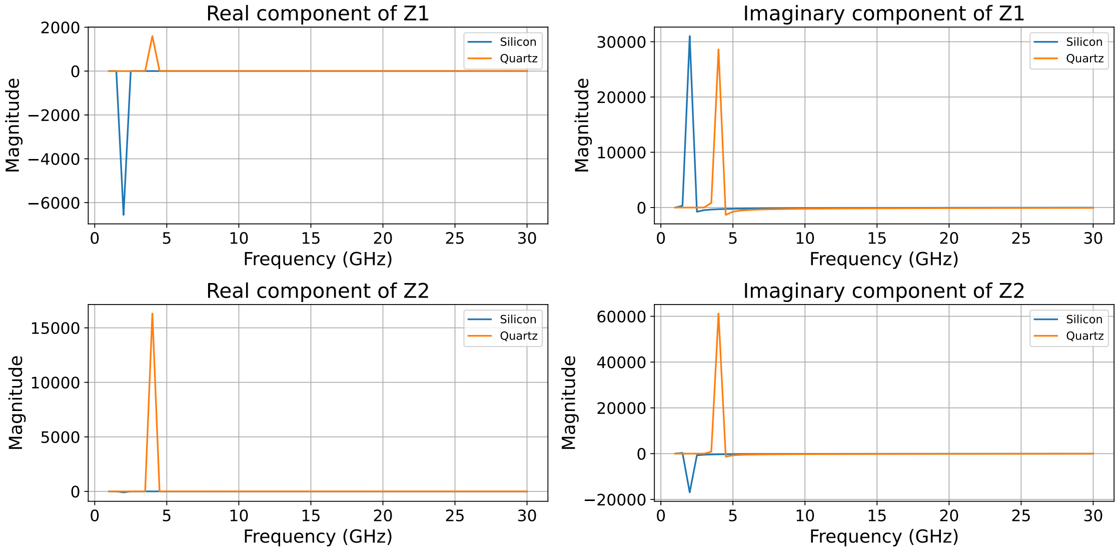


Figure 4.6: Shunt elements of MIM capacitors on different substrates

The shunt elements reach infinity when both designs reach the highest Q value (as per Figure 4.6). Hence, there is no resistive or capacitive coupling to the ground. To obtain clarity on the rest of the frequencies, we can redraw these figures, omitting the peaks as plotted in Figure 4.7.

By observing the imaginary components in Figure 4.7, it can be determined that the higher dielectric constant of the Silicon strongly couples the capacitor plates to the ground since the imaginary impedance is lower than that of Quartz.

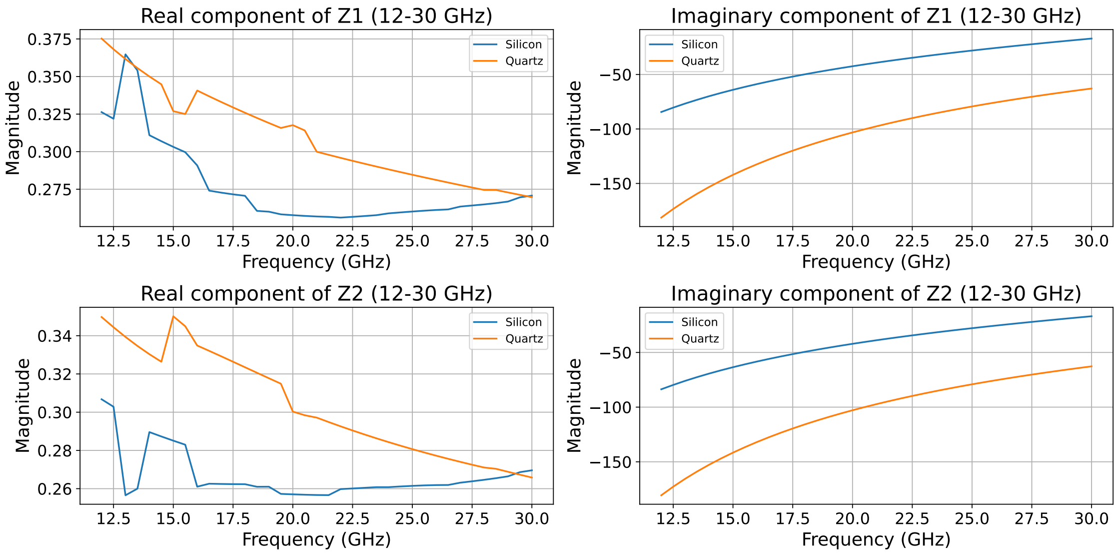


Figure 4.7: Shunt elements of MIM capacitors on different substrates at high frequencies

4.2.3.2 Series elements

Series elements of the pi-network can be plotted to understand how the parasitic inductance or series resistance increases.

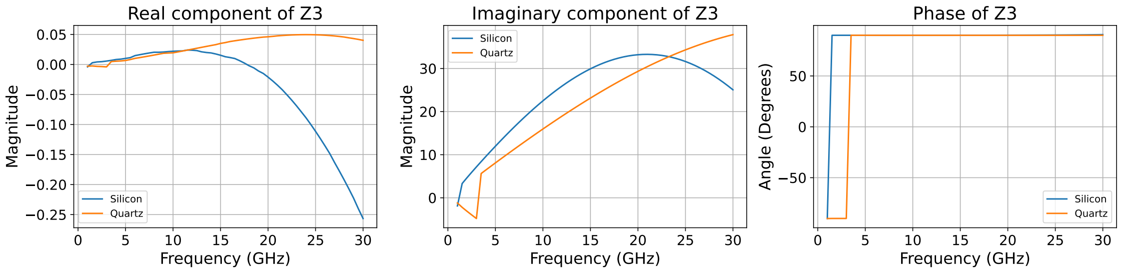


Figure 4.8: Series elements of MIM capacitors in different substrates

The imaginary component of the series element of the capacitor made on silicon showcases more imaginary impedance than its quartz counterpart, as shown in Figure 4.8. At 23 Ghz, imaginary impedance reaches a maximum and starts to decay, which correlates with the Smith chart in Figure 4.4.

Figure 4.8 also depicts how the series resistance increases with frequency due to loss tangent. Since Quartz has a higher loss tangent than Silicon, the series resistance is higher in that capacitor than one made of Silicon. However, from 18 Ghz, real impedance values take negative values for Silicon, which is unphysical. Hence, the pi-model would not suit from that frequency point to evaluate series components.

4.3 Inductor performance

The inductor required for the bias-tee is 47.5 nH. The magnetic flux density $\vec{B}$ of the planar inductor modelled can be seen in Figure 4.9. Inductance calculation does not depend on the dielectric constant as per the equations discussed in section 3.4.2. Hence, the parameters used in modelling are:

- Number of Turns: 9
- Outer Coil Diameter: 1580 um
- Inner Coil Diameter: 82 um
- Wire width: 5 um
- Wire thickness: 45 nm

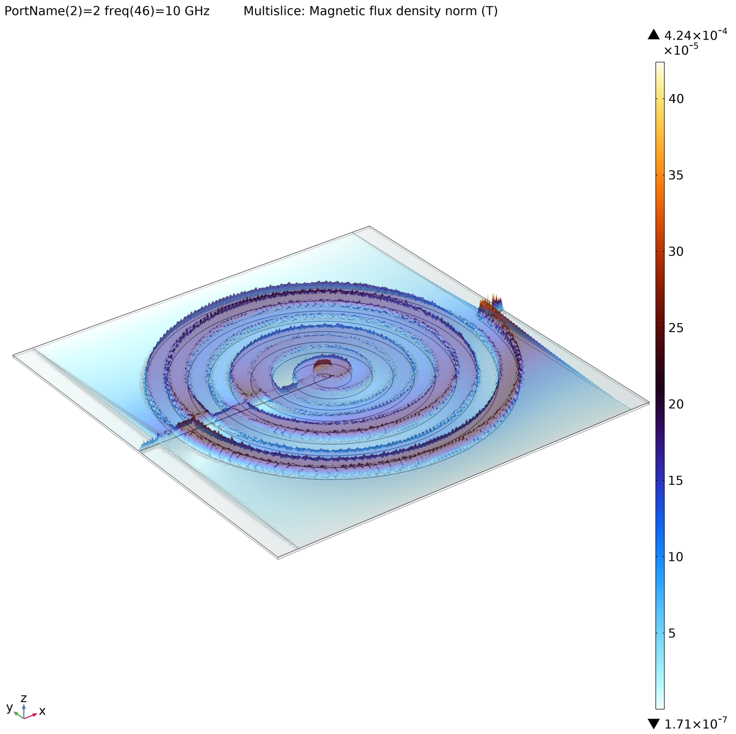


Figure 4.9: $\vec{B}$ distribution of a planar coil. Linearly colour mapped

4.3.1 Effect of the substrate and the dielectric bridge

Although the wafer's dielectric constant does not determine the inductance, it does give rise to the interwinding capacitance. Apart from the wafer, there will also be capacitive coupling through the dielectric bridge. Hence, the full wave simulation is needed to study the actual performance.

As per the design mentioned before, an ideal Inductor will suppress any frequency in the studied band. Nevertheless, the parallel capacitance that forms due to the interwinding capacitance will let some frequencies pass through. As Figure 4.10

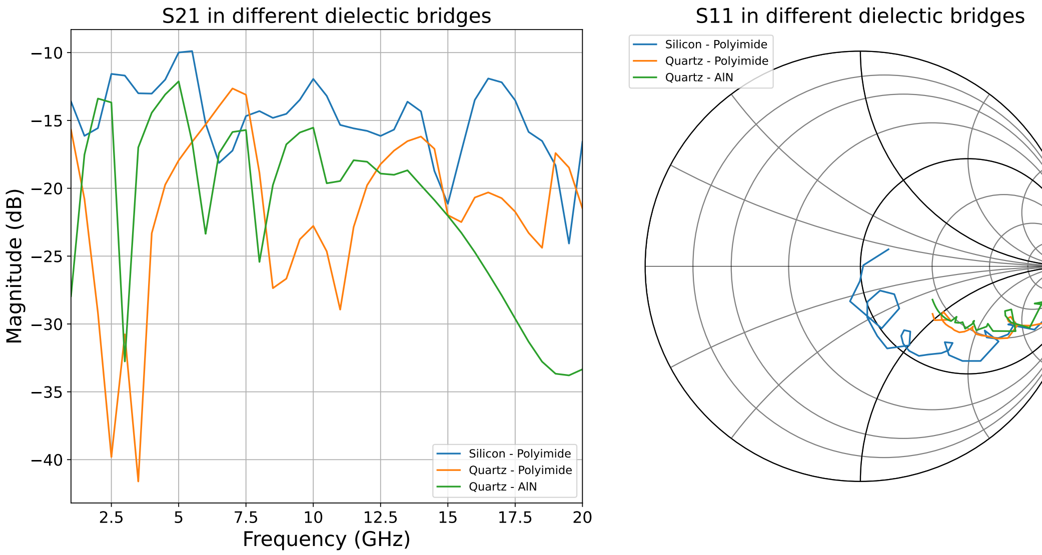


Figure 4.10: Effect of the substrate and the dielectric bridge

depicts, less transition can be seen with the design, which uses materials with the least dielectric constants among the combinations.

4.3.2 Q factor of the realised inductor designs

The quality of the designs is studied to investigate how well they are suited to store electromagnetic energy.
Figure 4.11 conveys that the design with AlN as the dielectric bridge will yield a maximum Q factor. However, similar to the capacitor design at high frequencies, the design with the least dielectric constants dominates since there will be more parasitic capacitive coupling to the ground.

4.3.3 Parasitics of inductors

The behaviour shown in S parameters can be further studied by looking at individual passive elements and approximating them as pi-network as before.

4.3.3.1 Shunt elements

We start by analysing the coupling to the ground plane regarding shunt elements.
Figures 4.12 and 4.13 depict somewhat similar behaviour to coupling to the ground, where the design which uses materials with less dielectric constant has less impedance compared to a design with a high dielectric constant. However, the Z1 and Z2 branches do not show similar imaginary impedance to that of a capacitor.

4.3.3.2 Series elements

Series elements of the pi-network can be plotted to understand how the parasitic inductance or series resistance increases.

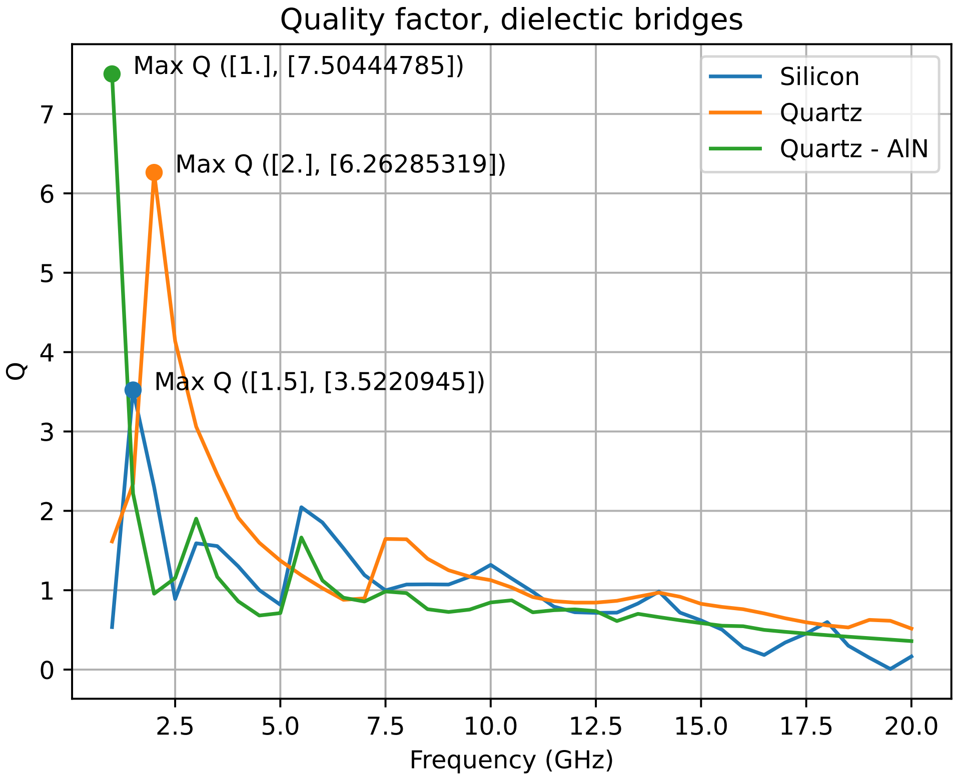


Figure 4.11: Q factor of inductors in different substrates

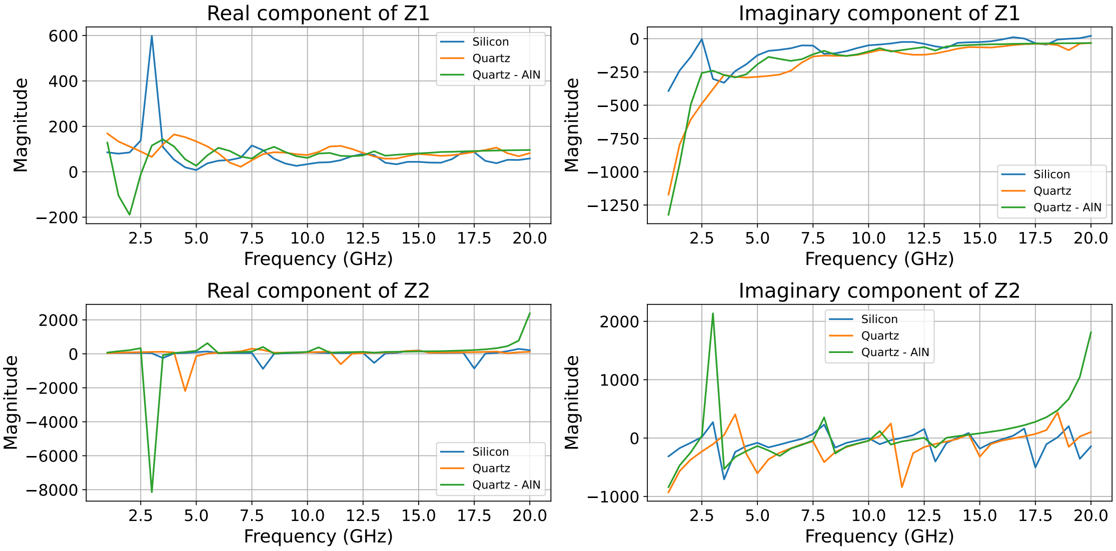


Figure 4.12: Shunt elements of inductors in different substrates

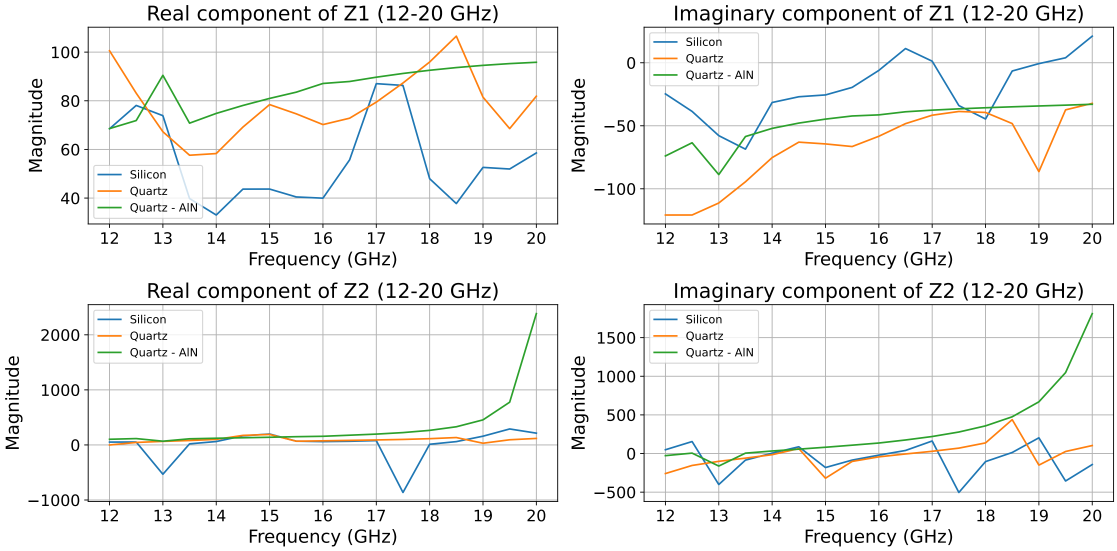


Figure 4.13: Shunt elements of inductors in different substrates from 12 GHz

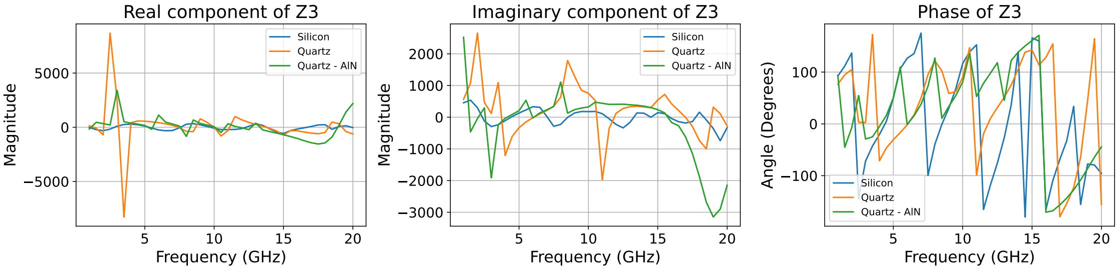


Figure 4.14: Series elements of inductors in different substrates

Self-resonance points where the series inductor behaves as a series capacitor can be seen in Figure 4.14. However, the exact points are hard to determine due to fewer frequency points. Since the phase change is abrupt, it can be noticed that the design with AlN has more oscillations between capacitive operation and inductive operation due to its higher die electric constant, although it yields the highest Q value due to its less loss tangent compared to Polyimide.

4.4 Packaging Considerations

The modelling so far consisted of the chip and an upper air block. Apart from metallic surfaces, every dielectric (wafer and air block) surface was modelled as a scattering boundary. The scattering boundary reduces the simulation time, and there are no parasitic shunting branches apart from the ground plane (which is used to form the CPW structure). In other words, it is as if the chip is suspended in space where all electromagnetic energy is dissipated into the void.

The said approach lowers the Q factor of the passive components, and the boundary condition is artificial. Moreover, in implementation, one needs to have metallic walls to shield the chip from electric fields that do not originate from the circuit itself.

The discussed scenarios can be mitigated with additional metal layers that can be introduced at dielectric boundaries, which can be modelled as PEC boundary conditions.

4.4.1 Upper Cavity

We start with introducing the PEC boundary conditions to the upper air block (where fringing fields occur between metal gaps), forming a cavity.

4.4.1.1 Effect on capacitors

With the addition of the upper PEC cavity, the Q value has increased by twice, as shown in Figure 4.15. The variation of the Q factor across frequency does, however, follow a similar trend as the without packaged component.

Introducing this new cavity has increased the resonance frequency of the shunted branches of the approximated pi-network, as depicted in Figure 4.16. However, Figure 4.17 shows that the shunt impedances are the same for both scenarios at high frequencies since most of the fields are coupled to the ground plane through the wafer. As per the series branch in Figure 4.8, the real part of the impedance has decreased since the fringing fields are now not lost to the artificial scattering boundary. Although the series imaginary impedances are the same for both solutions, the exact frequency at which the parasitic inductance dominates has increased by 2.5 GHz.

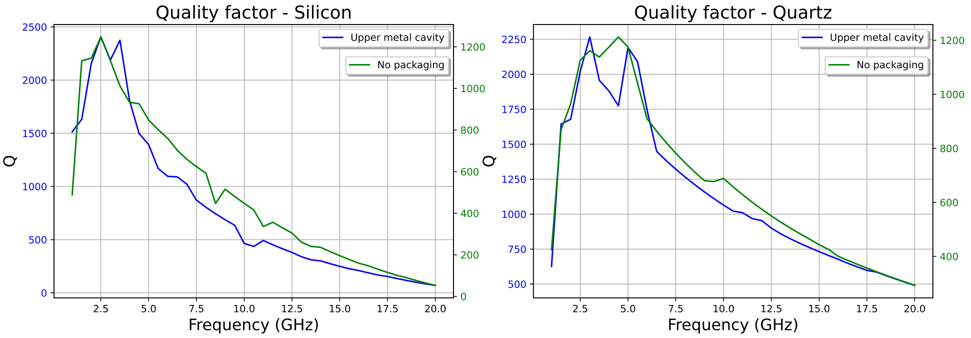


Figure 4.15: Q factor enhancement with an upper cavity for capacitor

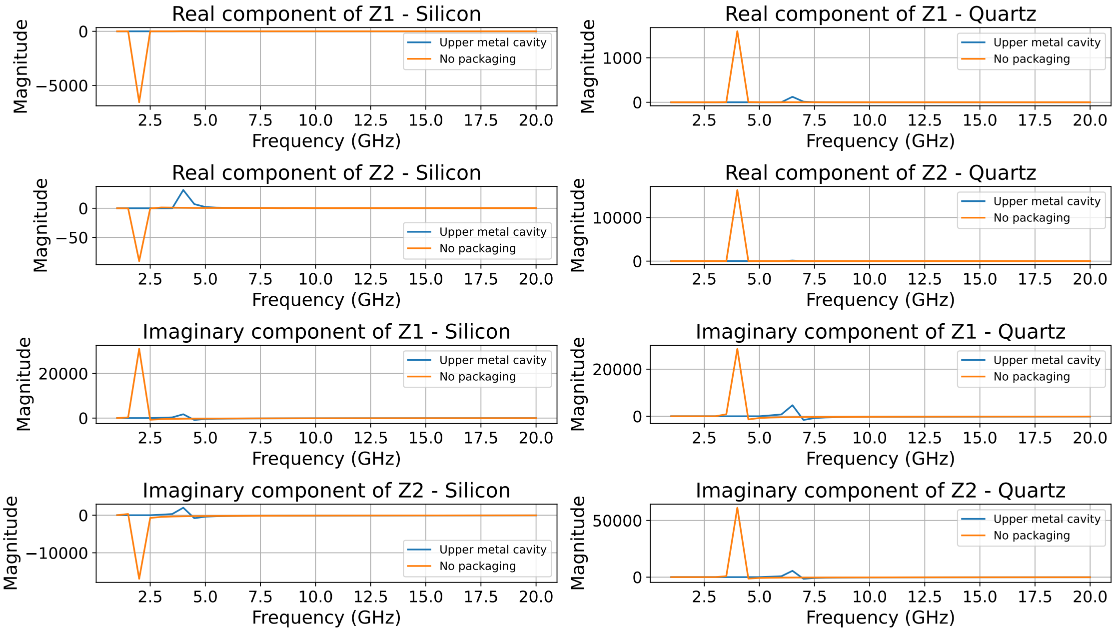


Figure 4.16: Shunt elements of capacitors with upper cavity

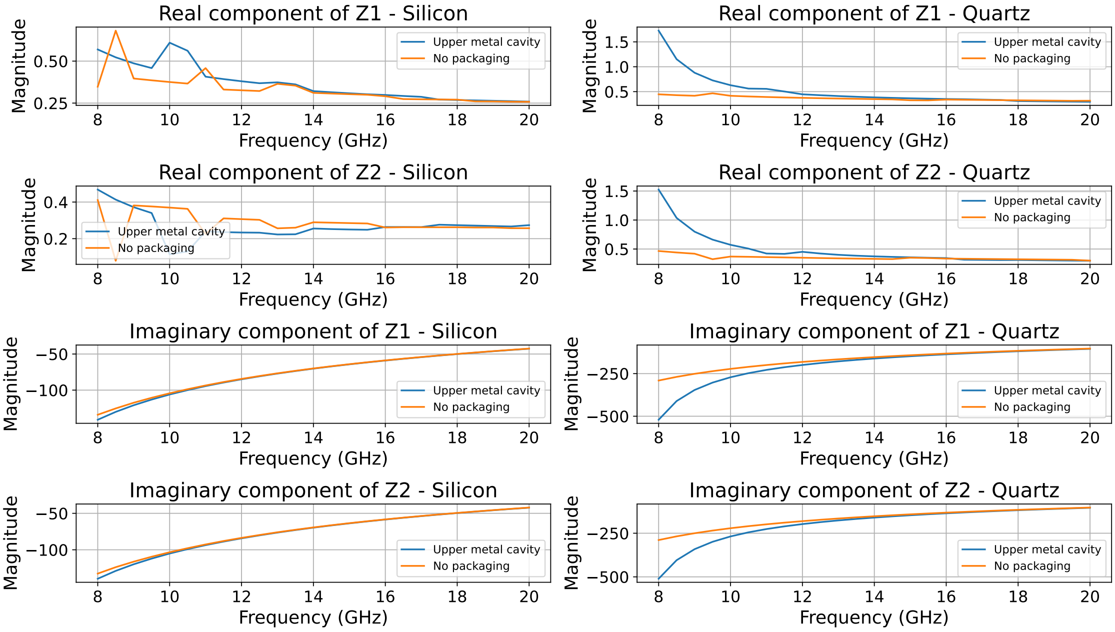


Figure 4.17: Shunt elements of capacitors with upper cavity from 8 GHz

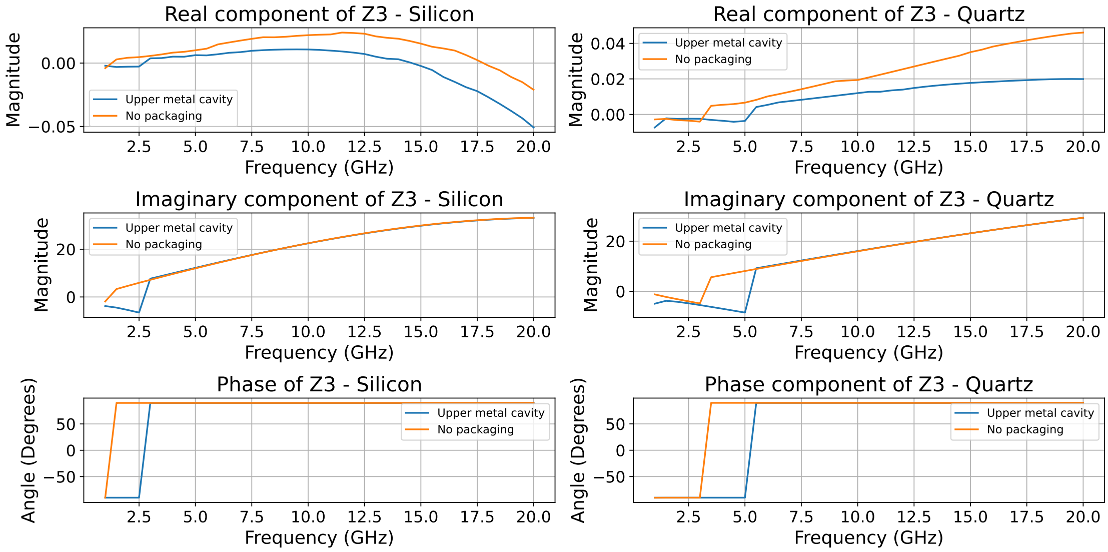


Figure 4.18: Series elements of capacitors with upper cavity

4.4.1.2 Effect on inductors

As per Figure 4.19, the quality factor of inductors has grown significantly higher with the introduction of the top cavity. However, there are also more instances where it reaches zero, a sign of self-resonance.

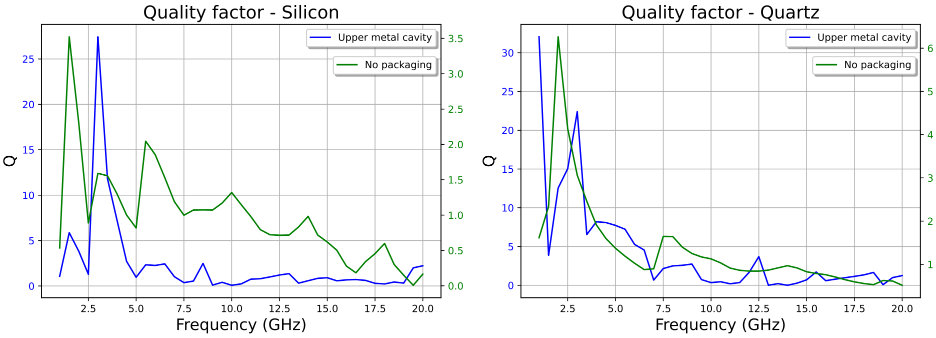


Figure 4.19: Q factor enhancement with an upper cavity for inductors

Figure 4.20 shows that more resonances can be seen by the introduction of the top cavity, which forms an extra shunting component.

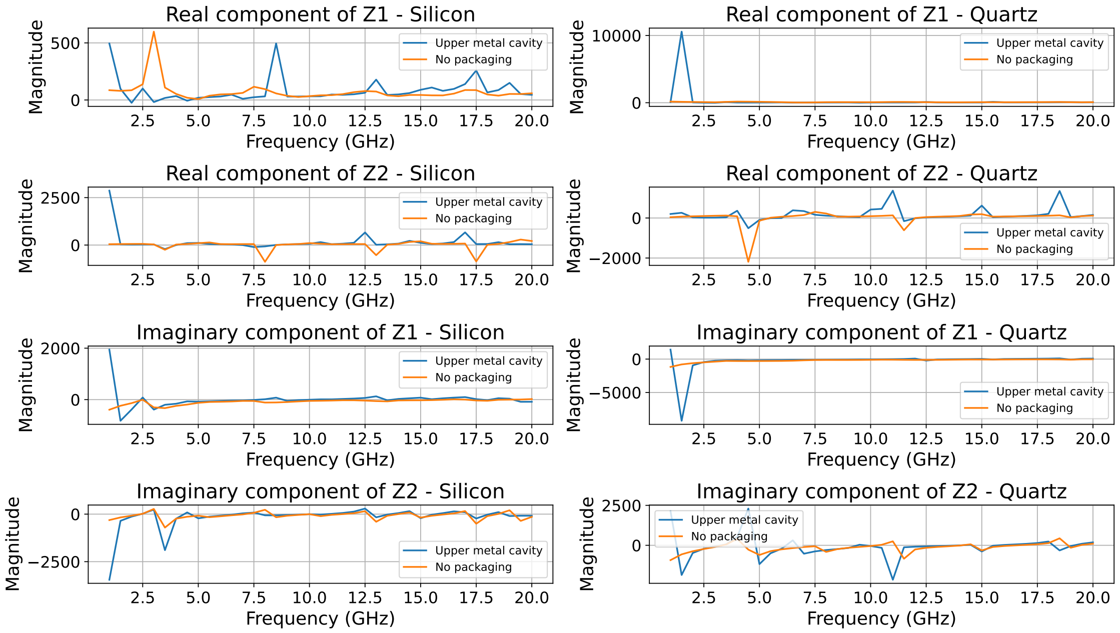


Figure 4.20: Shunt elements of inductors with upper cavity

According to the impedance characters of the series component in Figure 4.21, an operational zone for the passive components changes between the inductive zone and the capacitive zone much more rapidly in the silicon design than in the quartz design. The variations for the design on Quartz are similar, but there is a downward shift in the frequencies where the transitions would occur and a difference in exact impedance values.

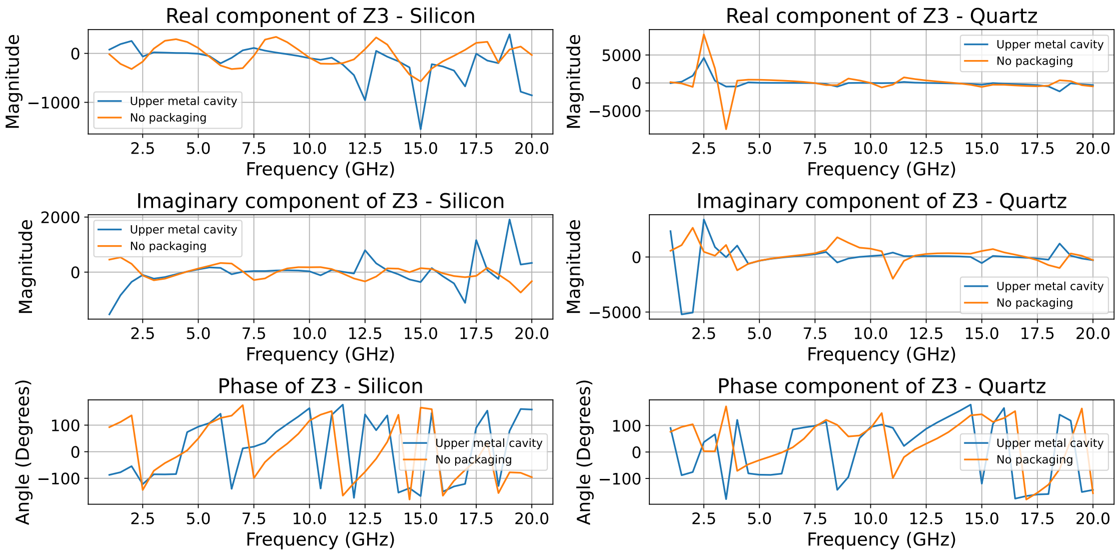


Figure 4.21: Series elements of inductors with upper cavity

4.4.2 Back metalization of the wafer

The loss of electromagnetic radiation from the top surface of the wafer is reduced using the top metalic cavity. To further increase the quality factor, the bottom layer of the wafer can be metallized. For these simulations, the dimensions of the waveguide structures are changed since the extra ground plane forms a grounded CPW.

4.4.2.1 Effect on capacitors

Compared to having only a top cavity, more gains in the quality factor are reported in Figure 4.22 by introducing the extra metal layer.

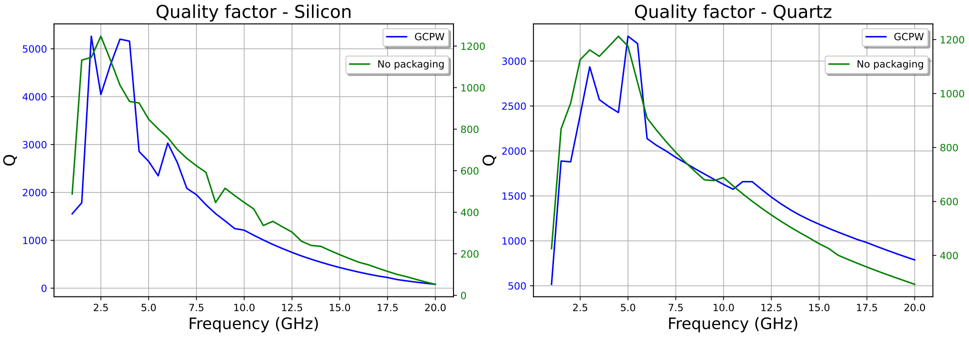


Figure 4.22: Q factor enhancement with a grounded CPW for capacitors

No resonance can be seen in the Silicon design's shunted elements with the back metal's introduction. For the design on Quartz, the resonance frequency has experienced an upward shift. Also, as per Figure 4.24, the design on Quartz exhibits more shunt capacitance than expected with a grounded CPW configuration.

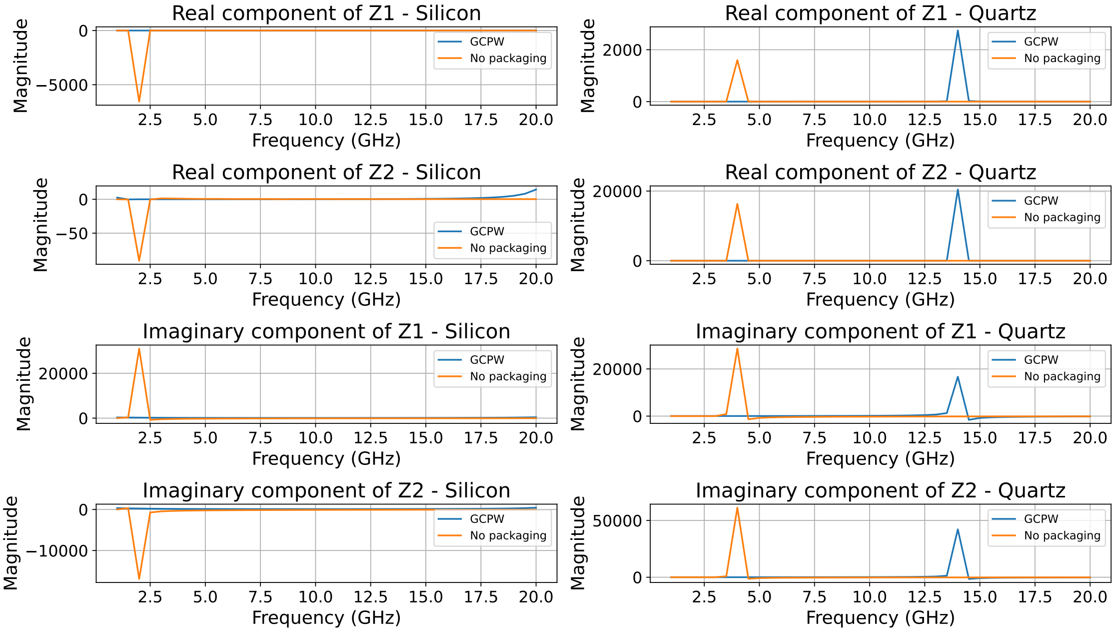


Figure 4.23: Shunt elements of capacitors with a grounded CPW

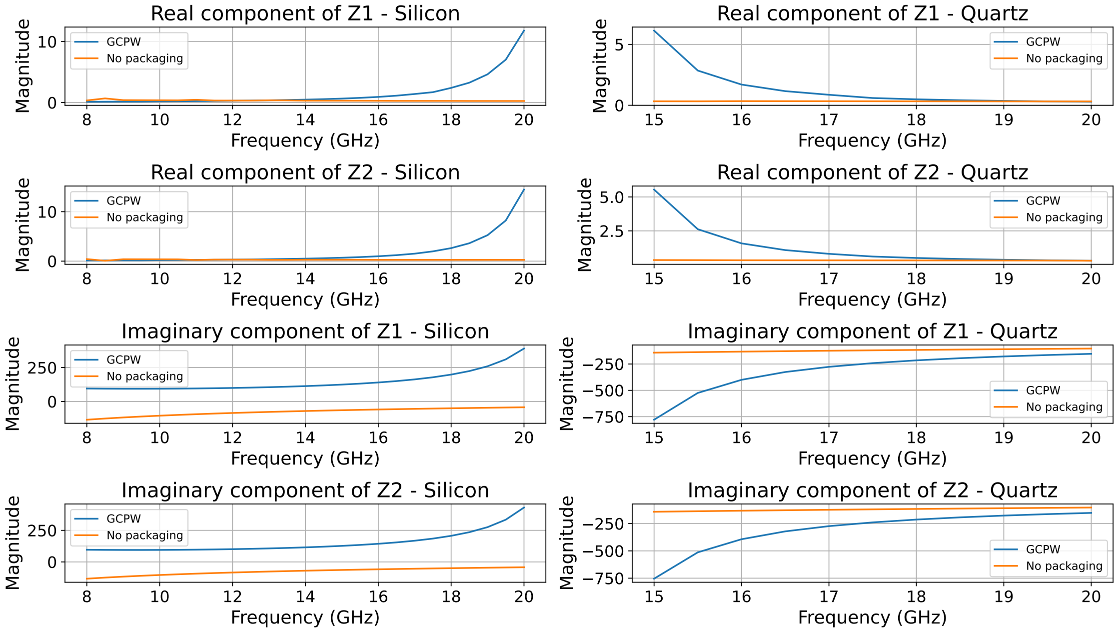


Figure 4.24: Shunt elements of capacitors with a grounded CPW at high frequency

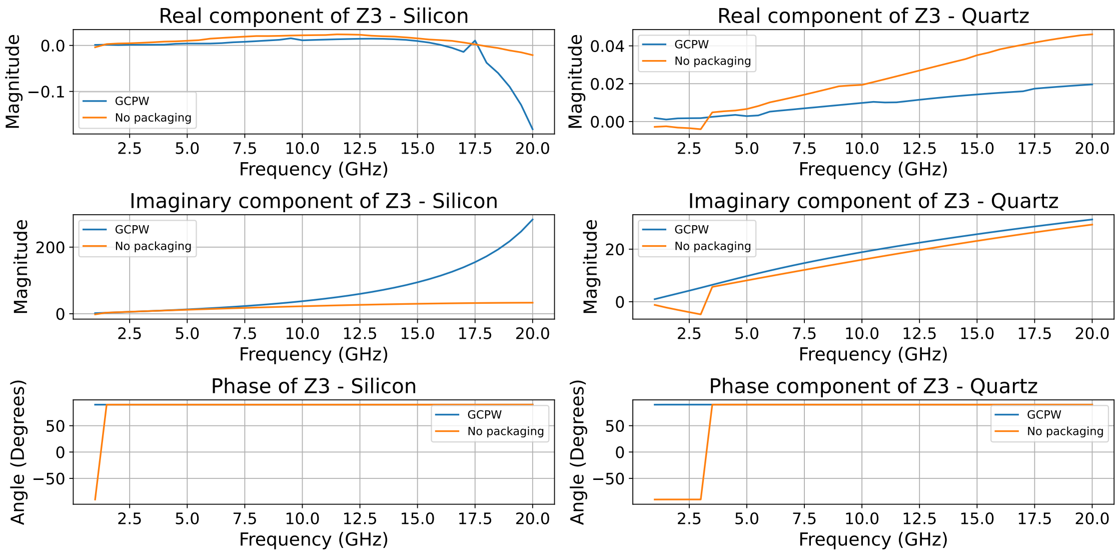


Figure 4.25: Series elements of capacitors with a grounded CPW

According to the series impedance characterisation in Figure 4.25, the frequency at which parasitic inductance dominates starts earlier in the frequency scale for both substrate designs. A reduction in the real component is also visible since the electric fields are not lost to the scattering boundary as before.

4.4.2.2 Effect on inductors

Adding the extra metal layer has increased the Q factor 20 times, as per Figure 4.26. However, similar drops to zero are noticeable, as discussed in Figure 4.19.

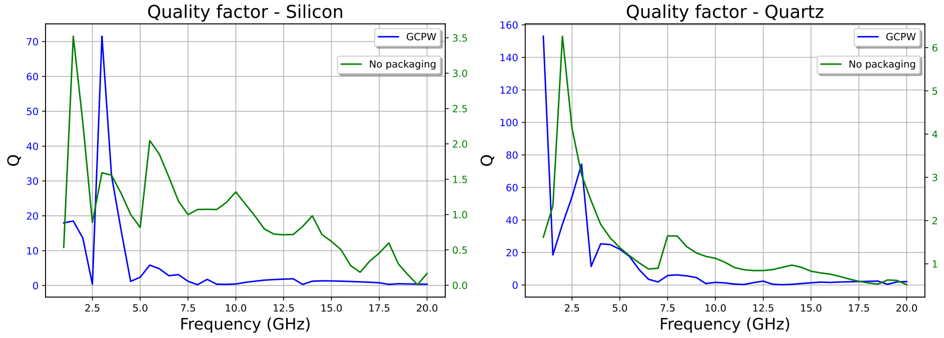


Figure 4.26: Q factor enhancement with a grounded CPW for inductors

A similar trend in resonance follows in both scenarios in Figure 4.27 but with increased shunt capacitance. Sharper resonances can be seen for series elements when an extra ground plane is introduced.

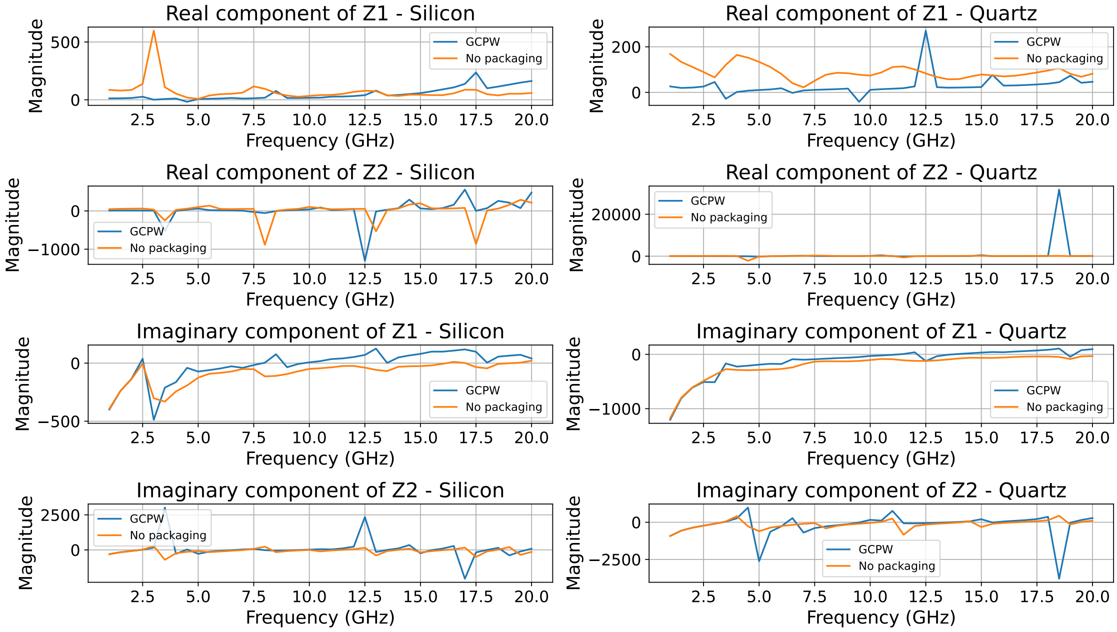


Figure 4.27: Shunt elements of inductors with a grounded CPW

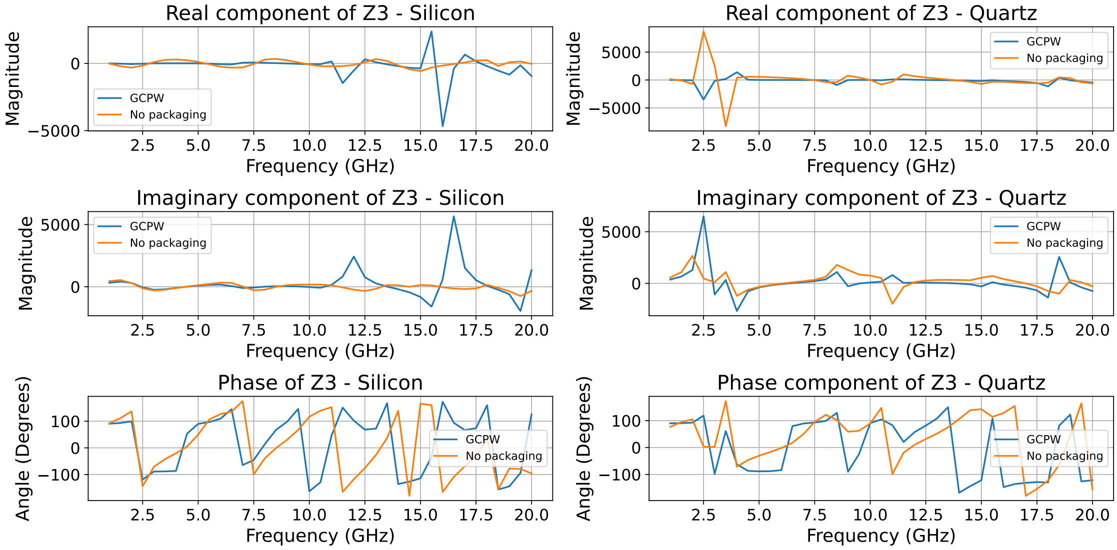


Figure 4.28: Series elements of inductors with a grounded CPW

4.4.3 Upper and Bellow Cavity

With the metallized back side of the wafer, we observed huge gains in the quantity factor combined with an upper air cavity. However, the said implementation results in increased capacitance to ground. We will now introduce a bottom air cavity alongside the top air cavity.

4.4.3.1 Effect on capacitors

With the introduction of a bottom air cavity, there is a significant gain in the quality factor, as plotted in Figure 4.29.Figure 4.30 shows that the shunt elements' real component is less than the amount present when no cavities exist. The imaginary part of the shunting elements is inductive, as per Figure 4.30. It can also be observed that in Figure 4.32 the phase shift back to the capacitive region occurs within the frequency band in question.

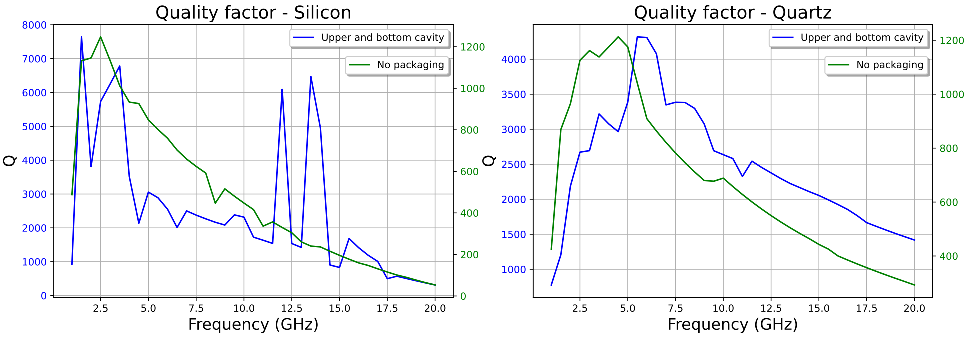


Figure 4.29: Q factor enhancement with upper and bottom cavity

4.4.3.2 Effect on inductors

While introducing a bottom cavity, the height of the top cavity was also increased to reduce shunt elements in this iteration. The said modification has resulted in a superior Q factor value, as shown in Figure 4.33. There is a noticeable drop in the resistive component of the shunt elements with the introduction of cavities at the top and bottom as depicted in Figure 4.34. However, metallic cavities introduce resonances, which is expected from before.

Figure 4.34 shows that the shunt elements' real component is less than the amount present when no cavities exist. Also, it shows cases in which the imaginary shunt branches experience more resonances with introducing the cavities. As for the characteristics shown in Figure 4.35 of the series components of the pi network, more resonances are now present as there are more changes in the phase.

4.4.4 Transmission through capacitors

Another way to analyze the effect of the packaging is to plot s-parameters, as shown in Figures 4.36 and 4.37.

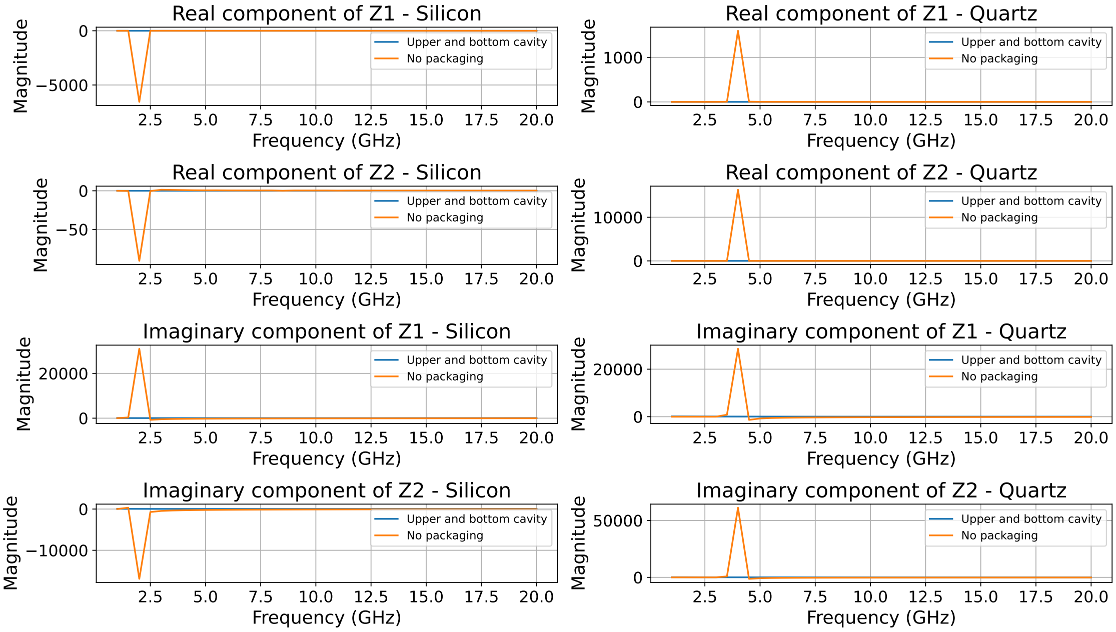


Figure 4.30: Shunt elements of capacitors with upper and bottom cavity

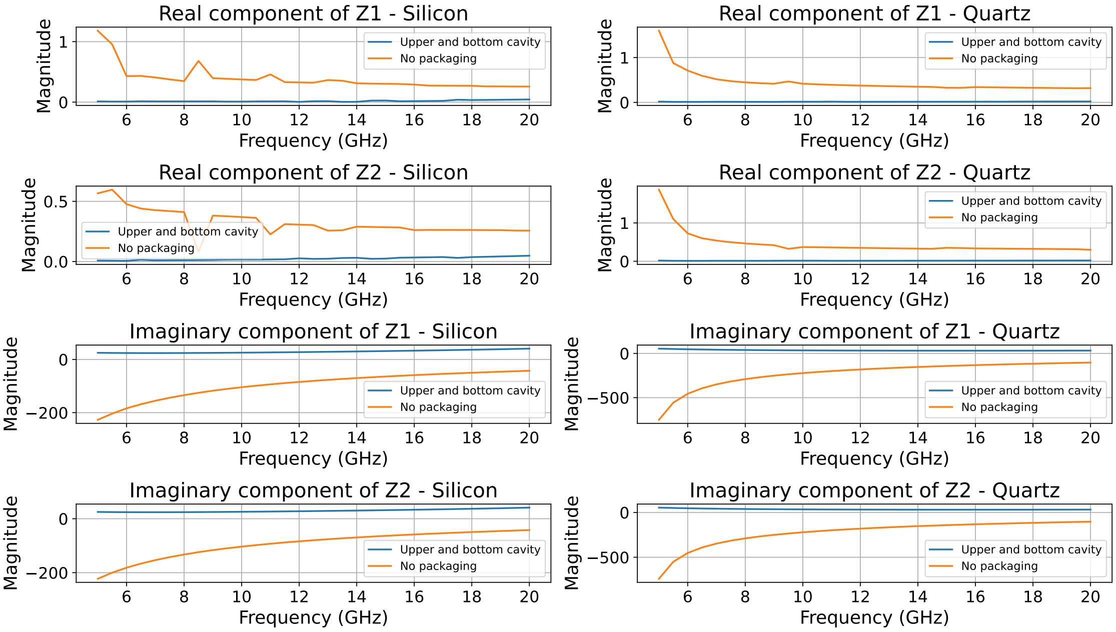


Figure 4.31: Shunt elements of capacitors with upper and bottom cavity from 5 GHz

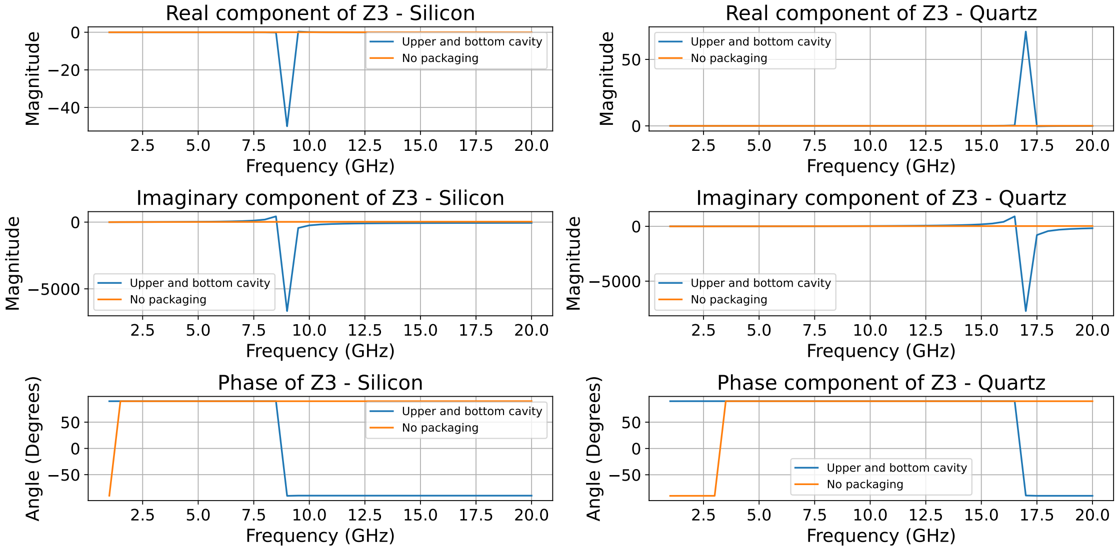


Figure 4.32: Series elements of capacitors with upper and bottom cavity

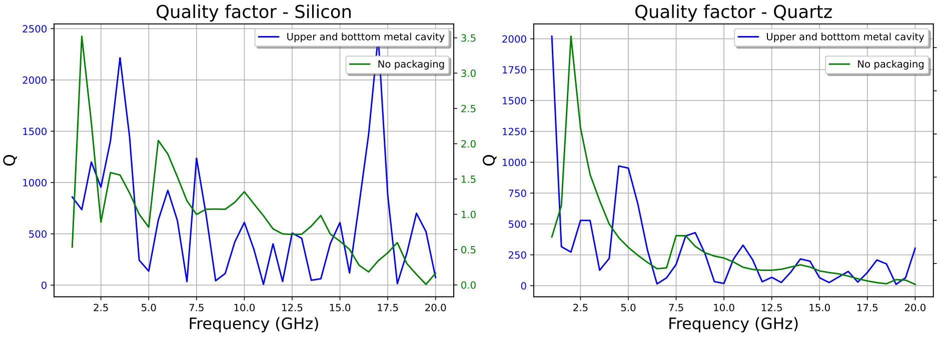


Figure 4.33: Q factor enhancement with an upper and bottom and bottom cavity for inductors

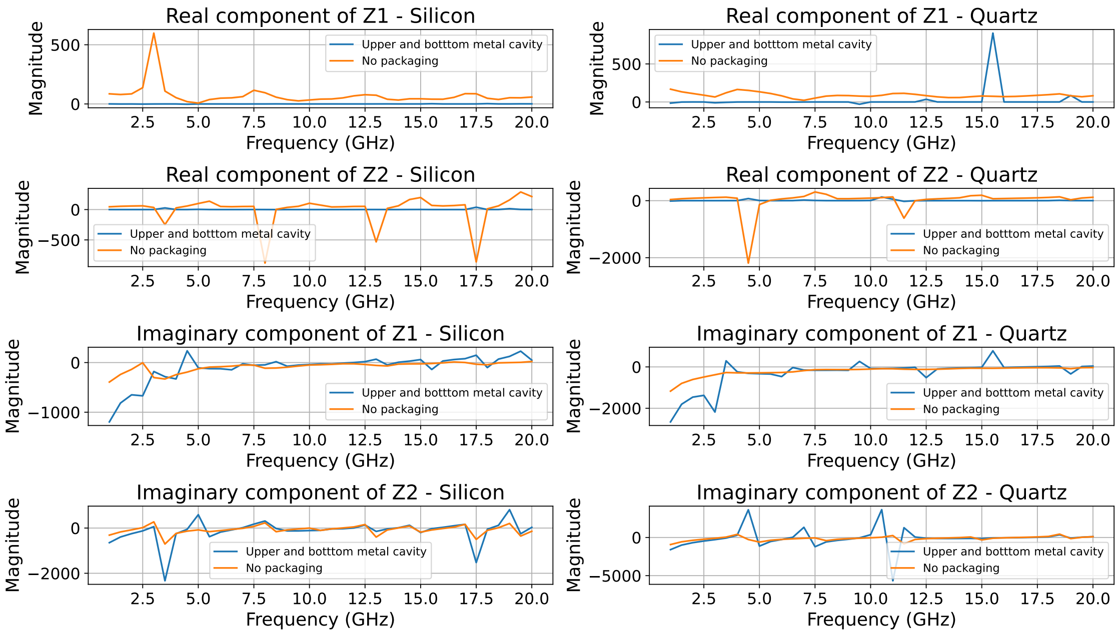


Figure 4.34: Shunt elements of inductors with upper and bottom cavity

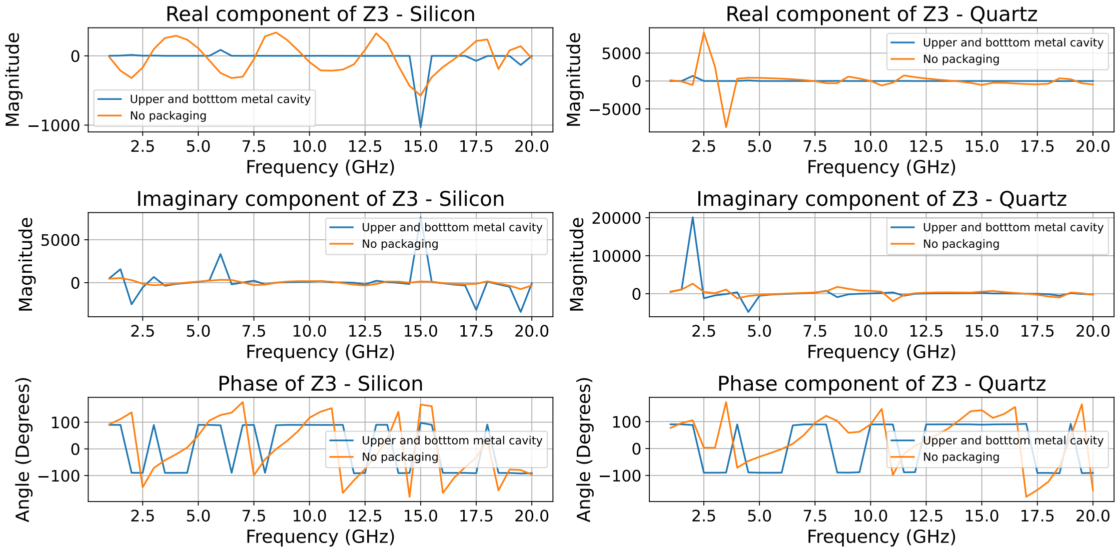


Figure 4.35: Series elements of inductors with upper and bottom cavity

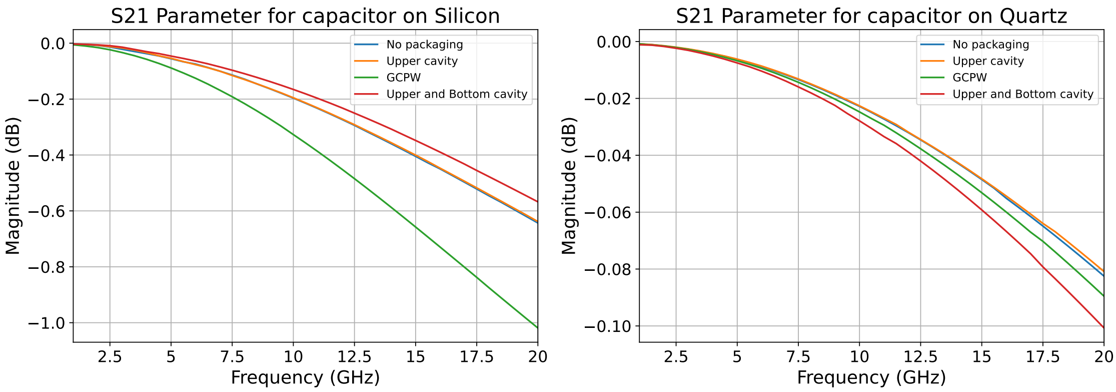


Figure 4.36: Transmission through capacitor designs

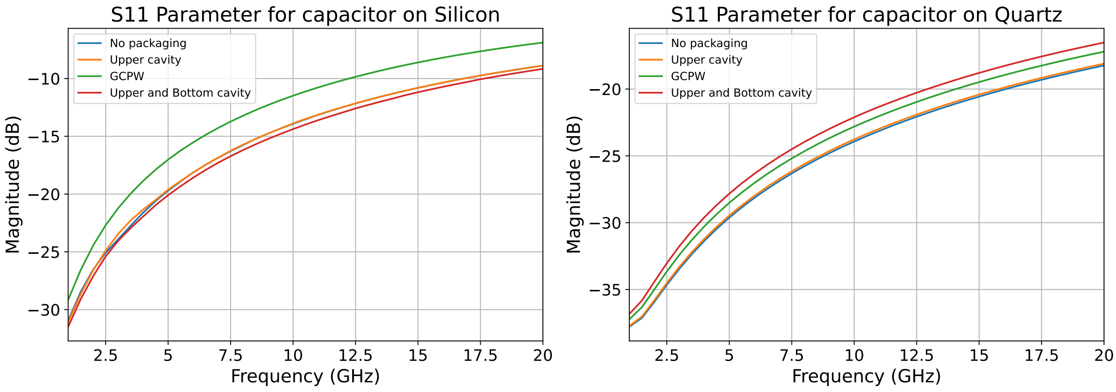


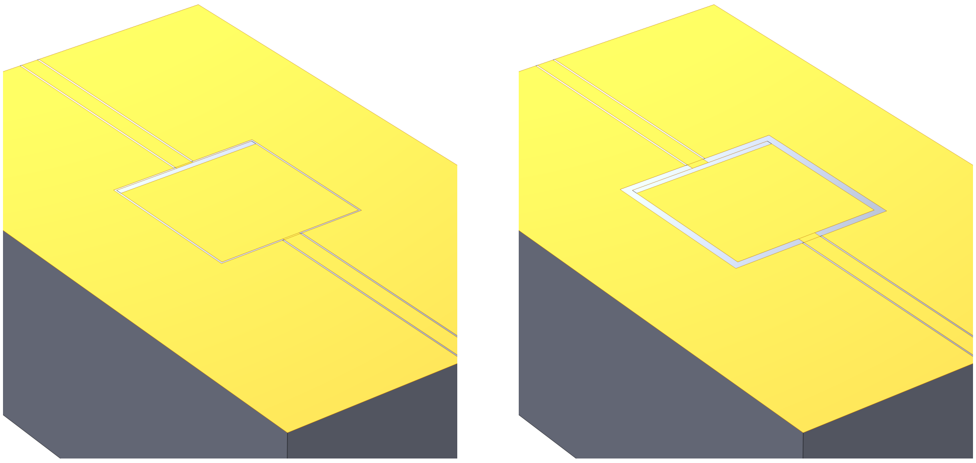
Figure 4.37: Reflection from capacitor designs

It can be seen that the S21 transmission degrades with frequency when more metalling boundaries are added for Quartz. However, for capacitors realized on Silicon transmission, it improves.

4.5 Capacitor optimization

Since we can forecast the issue of parasitic shunt capacitance, we can mitigate it by having more distance between the ground plane and the electrodes of the capacitor. The capacitor plates' distance to the ground plane is widened, as depicted in Figure 4.38. The larger the separation, the lower the capacitive coupling to the ground plane through the substrate.

Although the insertion loss through the capacitor is lowered, the Q-factor has also lowered, as per Figure 4.41.



(a) opening same as the gap width **(b)** opening increased than the gapwidth

Figure 4.38: Varying the capacitor plate clearance to the ground plane

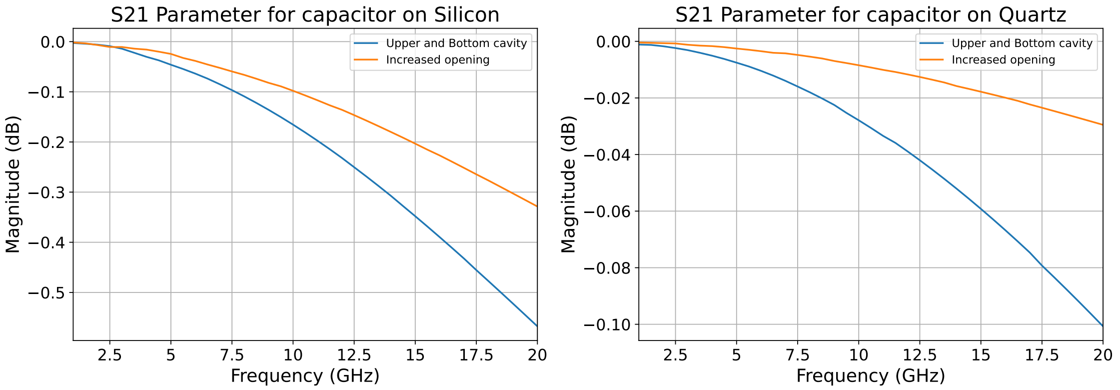


Figure 4.39: Transmission through optimized design

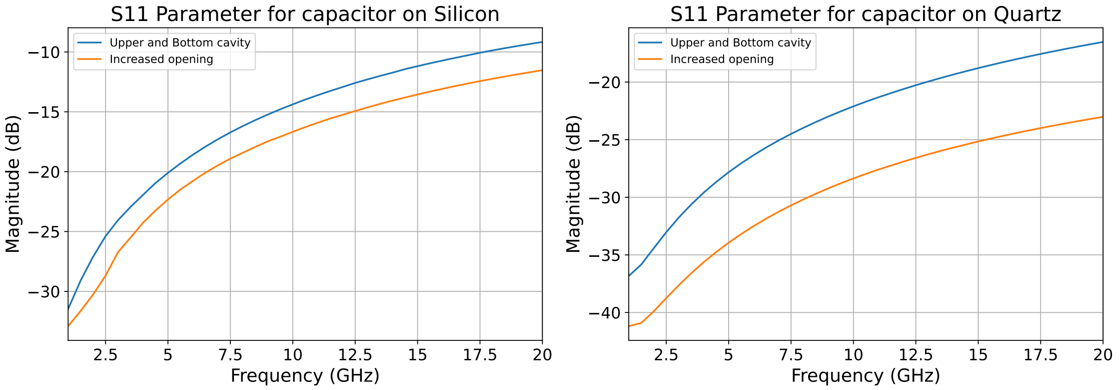


Figure 4.40: Reflection from optimized designs

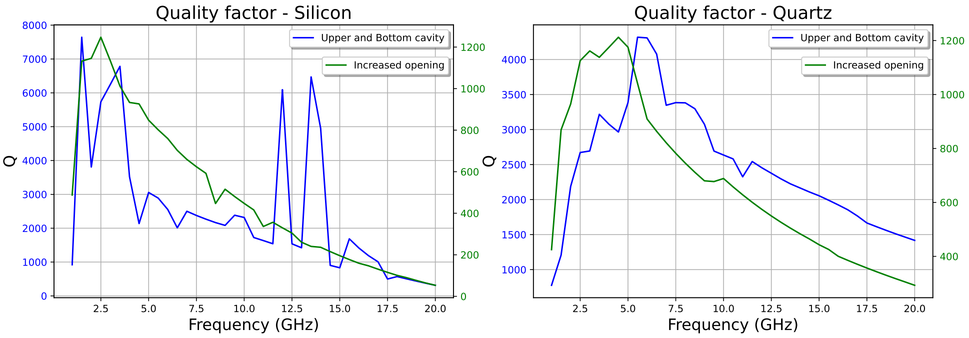


Figure 4.41: Reduction of Q-factor from optimized designs

4.6 Complete bias-tee design

We are now able to simulate the total response of the circuit using the field data. The simulation was performed by combing the touchstone files in Qucs in the configuration shown in Figure 4.42.

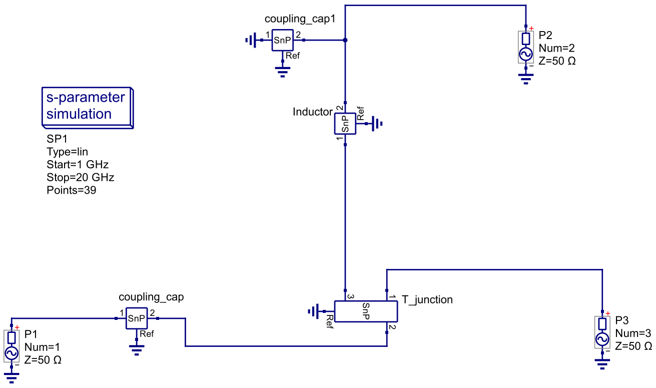


Figure 4.42: Circuit schematic for S-parameter simulation

In Figures 4.43 and 4.44, isolation is below -30dB until 4Ghz. Then, the interwinding capacitance of the inductor dominates and the RF signals are no longer blocked. The resonance behaviour can be seen in both configurations. The design done on silicon has less isolation since the electric field is strongly coupled between spiral arms because of its high dielectric constant.

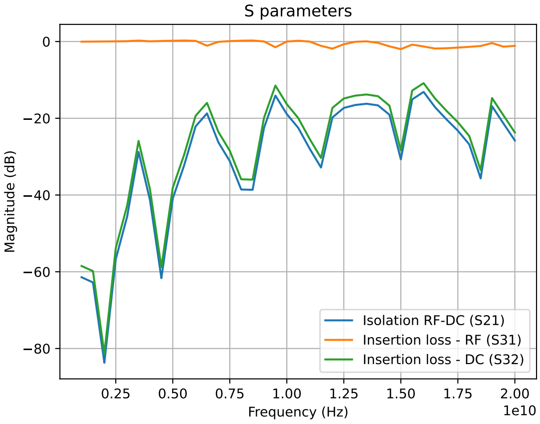


Figure 4.43: Bias-T response from devices in Quartz process

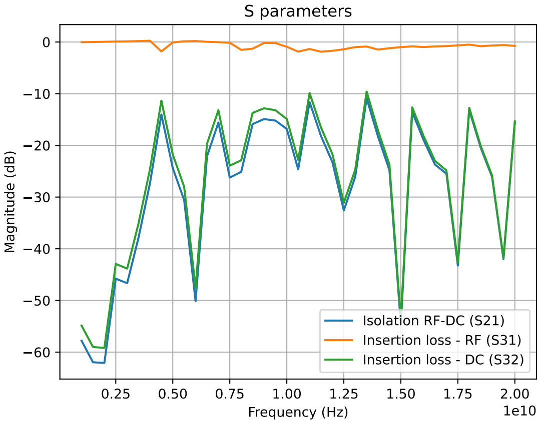


Figure 4.44: Bias-T response from devices in Silicon processs

5

Conclusion and future work

This work started with developing a theoretical foundation to define passive elements and their characteristics. These methodologies were developed with logical reasoning when choosing waveguide structures, required dielectrics, and superconductors. Waveguide structures were chosen to superconduct without exceeding the critical current density. Passive components were selected to model from prior work done in the literature.

These models were then simulated using COMSOL further to gain insights into their operation and parasitic behaviour. A unique way to mesh thin films was developed, considering the skewness of mesh elements. This thesis work was able to design relatively high-Q passive components. The performance, of course, would not reflect the fabricated process due to variances in fabrication, such as surface roughness. Also, the metallic cavity walls would not superconduct if copper is used, which will induce metalic losses. It was observed that the Q factor can be increased by reducing the scattering losses. However, the tradeoff was an increase in shunt capacitance.

Another tradeoff observed was when trying to fine-tune the transition through capacitors. The opening of the ground plane was widened to lessen the parasitic element, resulting in electric fields that were tightly constrained in the dielectric capacitor. Since the insulator's dielectric loss tangent is higher than the substrate, it will experience more dielectric losses. For future iterations, the substrate around the capacitor plates can be etched away to have air. Thereby reducing the parasitic shunt coupling.

Inductors should be studied further with more frequency resolution because the resonances are rapid. They are non-observable between the sampled frequency windows. The bottleneck for this process is the long simulation time due to the large degrees of freedom caused by the smaller mesh element size.

The self-resonance frequency spacing can be lessened by increasing the distance between spiral turns while having a smaller coil. The number of turns can also be lowered to have less interwinding capacitance. The said implementations will lower the inductance. Hi-permeability materials can increase the inductance to meet the required cutoff.

Overall, isolation of the bias-tee is also non-ideal compared to the state of the art. The design will also require further study to mitigate parasitic capacitance (which forms between windings). Furthermore, the entire circuit must be simulated to capture the effects of crosstalk.

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A

Co-planar Waveguide

Co-planar Waveguides were first introduced by C.P.Wen are one physical realization of transmission lines[53]. The characteristic impedance of CPW is usually made for 50 ohms. The exact derivation of the characteristic impedance is done using conformal mapping and is out of the scope of this thesis work. Nevertheless, for completion, equations to compute the impedance will be given in the appendix. Interested readers can refer to [54][55]. First, we define the complete elliptic integral of the first kind.

$$K(m) = \int_0^{\frac{\pi}{2}} \frac{1}{\sqrt{1 - m\sin(t)^2}} \tag{A.1}$$

With conformal mapping, a CPW realized on an infinitely deep substrate can be mapped into a parallel plate capacitor with some dielectric filling. The electric fields between the centre conductor and adjacent ground planes will have electric fields, which can be seen as capacitive coupling. This capacitance per unit length consists of two capacitors in parallel, where one is air C_a and the other is the dielectric of the substrate C_d.

$$C_d = 2 \cdot \epsilon_0 \cdot \epsilon_r \cdot \frac{K(k_1)}{K'(k_1)} \tag{A.2}$$

$$C_a = 2 \cdot \epsilon_0 \cdot \frac{K(k_1)}{K'(k_1)} \tag{A.3}$$

Here $K'(k_1) = K(1 - k_1^2)$ is the complement of the $K(k_1)$ which is defined above. While k_1 can be expressed as,

$$k_1 = \frac{W}{W + 2s} \tag{A.4}$$

This ratio of $K(k_1)$ and $K'(k_1)$ can be computed as follow,

$$\frac{K(k_1)}{K'(k_1)} = \begin{cases} \frac{\pi}{\ln 2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}}, & \text{for } 0 \leq x \leq \frac{1}{\sqrt{2}} \\ \frac{\ln 2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}}{\pi}, & \text{for } \frac{1}{\sqrt{2}} \leq x \leq 1 \end{cases} \tag{A.5}$$

Effective permittivity is given by,

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} \tag{A.6}$$

When Z_{vaccum} is approximated to be 377Ω the impedance of the CPW can be found by,

$$Z = \frac{0.25 \cdot Z_{vaccum}}{\sqrt{\epsilon_{eff}}} \cdot \frac{K(k_1)}{K'(k_1)} \tag{A.7}$$

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