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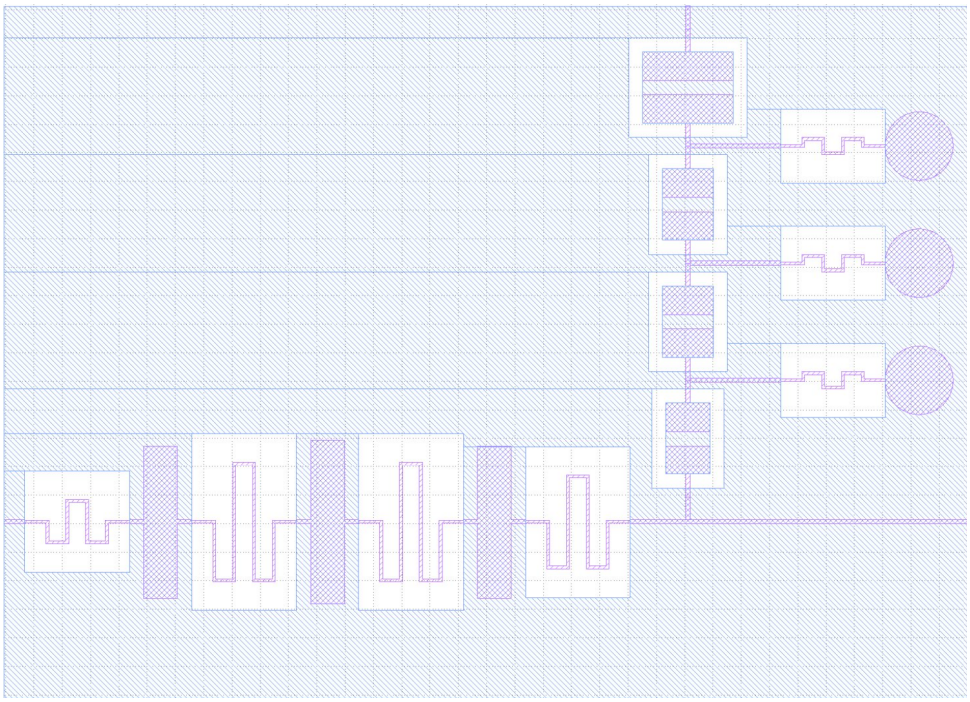

On-Chip Diplexer Design for Travelling Wave Parametric Amplifiers for Quantum Computers

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Abstract

This report presents the design and simulation of an on-chip diplexer intended for Traveling-Wave Parametric Amplifier (TWPA) applications. The device targets a 4–8 GHz source signal and a 10 GHz pump frequency, with the objective of maximizing the pump suppression and minimizing the insertion loss for the source signal. A cut-off frequency of 9 GHz was established to satisfy matching criteria of $S_{11} < -20$ dB and pump suppression of $S_{21} < -25$ dB.

The final series-first diplexer design successfully meets the pump suppression requirement of at least -25 dB at 10 GHz but does not fully maintain the -20 dB matching across the entire bandwidth. Simulations performed in both ADS and Sonnet confirm that, despite not meeting the matching goal, the diplexer likely maintains acceptable performance, suggesting that the initial matching requirement may have been overly stringent.

As the design has not yet been fabricated, practical measurements are pending. The close agreement between the ADS and Sonnet simulations demonstrates that fast preliminary simulations in ADS can effectively guide and streamline the design process. Future work involves fabricating the device, measuring its real-world performance, and iterating the design. An elliptical filter approach is proposed for subsequent design iterations to potentially achieve improved matching and suppression.

Contents

1 Introduction

Quantum computers are a hot topic because of their promise of exponential speed-up for some algorithms compared to classical computers [1]. One example is Shor's algorithm, which is proven to have an advantage over classical methods. This algorithm is about factoring large numbers [2]. However, to realize machines that can run these algorithms, the hardware needs to improve [3]. With better hardware, we can build a so called fault-tolerant (FT) quantum computer, which means that errors on the quantum bits (qubits) can be corrected [4]. One important aspect of a quantum computer is the number of qubits. Currently, these numbers are in the hundreds for state of the art devices [5]. But to run Shor's algorithm [2] and factor a 2048 bit number we would need approximately 20 million qubits [6]. To achieve such a large number of qubits we need to ensure that the structures that we build are scalable. One step towards this is to build as many of the components as possible on-chip instead of using external devices [3].

One way to realize qubits is with superconductivity, such as the ones we build at Chalmers [7]. For these qubits to work we need very low temperatures, in the order of magnitude of mK [8]. If we aim to build an on-chip structure, this means that the components need to have the correct properties at this temperature.

Quantum computers are highly susceptible to noise, necessitating the use of weak signals to minimize disturbances to the quantum processing unit (QPU). However, when these signals are read out, amplification is required to ensure reliable measurement [9]. One possibility to achieve this is a Travelling Wave Parametric Amplifier (TWPA). Implementing this amplifier on-chip requires additional components, such as a diplexer. The diplexer facilitates the combination of the signal from the QPU with a pump signal, which is used to enhance the signal strength for effective amplification.

The goal of the project is to design an on-chip diplexer for a TWPA made by Alcalde-Herraiz *et al.* [10]. We will treat the QPU as a source of signal at radio frequency (RF), more specifically at 4-8 GHz, the filters will be designed for a pump frequency at about 10 GHz.

2 Theory

In this section, we will discuss the underlying theoretical framework needed to create an on-chip diplexer in a superconducting circuit.

2.1 Superconductivity

The electrons in a non-superconducting metal can be described according to the Drude model [11]. This allows us to write the current $\mathbb{J}(x,t)$ as

$$\mathbb{J}_n(x,t) = \frac{n_n \tau q^2}{m} \mathbb{E}(x,t) \tag{1}$$

where n_n is the charge carrier density, q is the electron charge, m is the electron mass, $\mathbb{J}$ is the current at point x and time t, $\mathbb{E}$ is the electrical field at point x and time t and τ is the mean free time between collisions. Since the conductivity is the current divided by the electrical field, we obtain the following equation.

$$\sigma_n = \frac{\mathbb{J}_n(x,t)}{\mathbb{E}(x,t)} = \frac{n_n \tau q^2}{m} \tag{2}$$

For superconducting metals, Eq. 2 has a temperature dependence as some electrons will transition to the superconducting state n_s while the others will remain in the non-superconducting state n_n, when cooled down to below its critical temperature T_C [12]. The relation between n_n and n_s is always satisfied by $n_n + n_s = 1$ since the electrons are either in the superconducting or non-superconducting state. This superconducting state emerges from the special case where the attractive interaction between electrons, derived from the absorption and emission of virtual phonons within the electron lattice, is nearly equivalent to the repulsive Coulomb interaction [13, 14]. Treating the superconducting and non-superconducting electrons as two separate fluids, as according to the Ginzburg-Landau theory [15], allows us to model how the amount of electrons in each state changes with the temperature. We then get that

$$\frac{n_s}{n} = 1 - \left(\frac{T}{T_c}\right)^4, \qquad \frac{n_n}{n} = \left(\frac{T}{T_c}\right)^4 \tag{3}$$

for any temperature T below the critical temperature T_c. If we apply a δ-function impulse of the electric field at $t = 0$, and assume a relaxation time of τ for the non-superconducting electrons and no scattering of the superconducting electrons, then the current in a superconductor takes the form

$$\mathbb{J}(x,t) = \mathbb{J}_n(x,0)e^{-t/\tau} + \mathbb{J}_s(x,0) = \frac{n_n q^2}{m_e} e^{-t/\tau} + \frac{n_s q^2}{m_e}. \tag{4}$$

It is possible to obtain the conductivity through a Fourier transformation from the current in Eq. 4.

$$\tilde{\sigma}(\omega) = \frac{n_n q^2 \tau}{m_e(1+\omega^2\tau^2)} + \frac{\omega n_n q^2 \tau^2}{j m_e(1+\omega^2\tau^2)} + \frac{n_s q^2}{j\omega m_e} \tag{5}$$

where the real part corresponds to the classical conductivity of a metal for a system with low relaxation time and frequency ($\omega\tau \ll 1$) [16, 12]. Treating the conductivity in the microwave regime ($\omega\tau \ll 1$), and with temperature well below T_c the conductivity becomes the following

$$\tilde{\sigma}(\omega) = \frac{n_n q^2 \tau}{m_e} + \frac{n_s q^2}{j\omega m_e} \tag{6}$$

which is similar to the form of the impedance $Z^{-1} = R^{-1} + (i\omega L)^{-1}$ and we can extend the definition for a superconductor to work for circuits as well. As a result, we can view a superconducting material as a resistor and inductor in parallel.

A superconducting circuit also exhibits a magnetic field, the strength of which decreases exponentially the closer we get to the centre of the superconducting material. The London penetration depth, λ_L, is defined as the depth where the magnetic strength has decreased to e^{-1} of its maximum value and is given by

$$\lambda_L = \sqrt{\frac{\varepsilon_0 m_e c^2}{n_s q^2}} \tag{7}$$

where ε_0 is the vacuum permittivity and c is the speed of light [17]. If this magnetic field varies in time, then an electric field will be induced and the non-superconducting electrons will move according to the electric field and give rise to an alternating current resistance [18]. Combining Eq. 7 with Eq. 3 do we get the following dependence on temperature for the London penetration depth

$$\lambda_L(T) = \frac{\lambda_L(0)}{\sqrt{1 - \left(\frac{T}{T_c}\right)^4}}. \tag{8}$$

As the temperature decreases, so does the amount of electrons in the non-superconducting state, and the resistance for the direct current approaches zero [19]. The London penetration depth

will, on the other hand, will increase, as according to Eq. 8, which results in a stronger magnetic field inside the superconductor [18]. The relation between the curl of the electric field and the time-derivative of the magnetic field $\mathbb{B}$ as described by Maxwell [20] is

$$\nabla \times \mathbb{E} = -\frac{\partial \mathbb{B}}{\partial t} \tag{9}$$

and since the AC resistance depends on the electric field will we obtain a non-zero AC resistance, given that the magnetic field varies in time. Since the DC resistance approaches 0, and the AC resistance do not, can we treat the measured impedance as consisting entirely of inductance. For materials such as NbTiN, can the kinetic inductance exceed 90% of the total inductance, allowing us to treat all inductance as kinetic [21]. This kinetic inductance depends on the length of the element, and can therefore be optimized to achieve the inductance we want.

2.2 Transmission Line

The current of the circuit will travel in transmission lines. These transmission lines will be placed on a layer of substrate on the same plane together with all other conducting elements in a coplanar fashion. This configuration is known as a coplanar waveguide (CPW). This has a few advantages compared to waveguides where the conducting elements are not on the same plane. For one, if the relative dielectric constant is large compared to unity, then the magnetic field at the interface is circularly polarized with the plane that is nearly perpendicular to the surface, allowing for easy connections of external shunt elements [22]. Another advantage is that if the dielectric constant of the substrate is high, then the loading effect of the grounded cover is negligible for RF-circuits [22].

Assuming the transmission line travels in the z-direction, Kirchhoff's laws can be written as

$$\begin{aligned} \frac{\partial v(z,t)}{\partial z} &= -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t} \\ \frac{\partial i(z,t)}{\partial z} &= -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t} \end{aligned} \tag{10}$$

where $v(z,t)$ and $i(z,t)$ are the microscopic voltage and current respectively [23]. The parameters R, L, G and C are the series resistance, series inductance, shunt conductance and the shunt capacitance. For the superconducting circuit, superconducting transmission lines will be used. These transmission lines are lossless [24], and assuming steady state, Kirchhoff's laws in Eq. 10 give rise to the following differential equations

$$\begin{aligned} \frac{d^2V(z)}{dz^2} - \gamma^2 V(z) &= 0 \\ \frac{d^2I(z)}{dz^2} - \gamma^2 I(z) &= 0, \end{aligned} \tag{11}$$

with $\gamma = j\omega\sqrt{LC}$ [23]. Solving the equation for voltage, we get

$$V(z) = V^+ e^{\gamma z} + V^- e^{-\gamma z} \tag{12}$$

with V^+ being the voltage that enters the transmission line at $z = 0$ and V^- is the voltage entering the transmission line at the end of the line. The relation between V^+ and V^- for any N-port junction is given by the scattering matrix and the S-parameters [25].

2.3 S-parameters

In an N-port junction, some voltage waves will be transmitted or scattered into other ports. If V_n^+ is the voltage that enter port number n, then V_n^- is the voltage that leaves the same port. In general, for an N-port system the relation between V_n^+ and V_n^- is given by

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_n^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1n} \\ S_{21} & S_{22} & \cdots & S_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ S_{n1} & S_{n2} & \cdots & S_{nn} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_n^+ \end{bmatrix}, \tag{13}$$

where S_{ii} is the reflection coefficient for port i and S_{ji} is the transmission coefficient for port $i \to j$ [23, 25]. The central matrix of Eq. 13 is called the scattering matrix and has definite values for all frequencies. While there is no well-defined equation that can calculate the exact value of S_{ij} the reflection at port i can be calculated as

$$\frac{V_i^-}{V_i^+} = \frac{\overline{Z}_i + 1}{\overline{Z}_i - 1} \tag{14}$$

where $\overline{Z}_i$ is the normalized impedance [25]. Note that the reflection can be written as either a function of impedance, which depends on the inductance, or as a function of the S-parameters. The S-parameters therefore depends on the inductance as well.

In the diplexer, some current will go through the low-pass filter, while the rest will go through the high-pass filter. When a sweep of all possible frequencies is performed, there will be an interval where the current switches from the low-pass to the high-pass filter and insertion loss will occur as a result.

Consider the following toy case by Beatty [26]. Assume that we have an ideal, non-reflective junction or connector ($S_{11} = S_{22}$), with a phase shift of an integer multiplied by 2π. If we then switch to another waveguide junction the net power to the load usually change. The ratio of the initial load power P_L and the final load power P_F expressed in decibels would be

$$10\log_{10}\left(\frac{P_L}{P_F}\right) = 10\log_{10}\left(\frac{Z_{01}}{Z_{02}}\left|\frac{(1 - S_{11}\Gamma_G)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_G\Gamma_L}{S_{21}(1 - \Gamma_G\Gamma_L)}\right|^2\right) \tag{15}$$

with Γ_G and Γ_L being the reflection coefficient for the generator and load respectively, and Z_{0i} is the real characteristics impedances of the input and output wave arm i. It is this difference, that is known as the insertion loss.

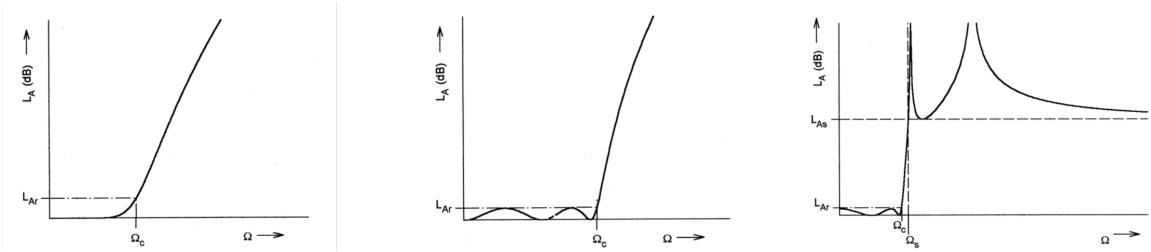
2.4 Filter Theory

Filters play a crucial role in RF circuits, enabling frequency selective isolation of signals or suppression of unwanted signal components. Filters are categorized into four basic groups. These are low-pass, high-pass, band-pass and stop-band filters [23, 27]. In order to realize the diplexer, designed in this project, we only need a low-pass and a high-pass filter. Hence, we will only discuss these two types in more detail.

Each filter can be mathematically described by a response function like

$$|S_{21}(j\Omega)|^2 = \frac{1}{1 + \epsilon^2 F_n^2(\Omega)}, \tag{16}$$

where ϵ is the ripple constant, F_n is the characteristic function of the filter and Ω is the frequency. Depending on the filter type the filter response function is adjusted. For our filter design, there



(a) Butterworth (b) Chebyshev (c) Elliptic

Figure 1: Response behaviour of the different filter types, shown with the insertion loss. Ω_c is the cut-off frequency with $S_{21} = -3\,\text{dB}$ [27].

are three relevant types of mathematically defined filters. The Butterworth, Chebyshev and Elliptic filters.

The response function of a Butterworth filter, also called Maximally flat filter, is

$$|S_{21}(j\Omega)|^2 = \frac{1}{1+\epsilon^2\Omega^{2n}} \ , \tag{17}$$

where n is the order of the filter [27]. As the name suggests, Butterworth filters have a flat response. However, their roll-off is relatively slow, which makes them unsuitable for our diplexer, as a steep roll-off is desired. The behaviour of the insertion loss of a Butterworth filter is depicted in Fig. 1a.

Another filter type is the Chebyshev filter, with its response function being

$$|S_{21}(j\Omega)|^2 = \frac{1}{1+\epsilon^2 T_n^2(\Omega)} \ , \tag{18}$$

where ϵ is related to the given passband ripple and T_n is a function of $\cos(\Omega)$, defining the Chebyshev function. Chebyshev filters have ripples in the passband (visualized in Fig. 1b), but they also have a steeper roll-off. By choosing a low ripple constant, a good filter can be constructed for our diplexer design.

The third filter presented here is the Elliptic filter with the response function

$$|S_{21}(j\Omega)|^2 = \frac{1}{1+\epsilon^2 F_n^2(\Omega)} \ . \tag{19}$$

Here F_n is a function that describes the oscillation in the stop- and passband. Elliptic filters have the steepest possible roll-off. The downside is the more complicated circuit design compared to both Butterworth and Chebyshev filters [27].

2.5 Lumped Element Filters

Lumped elements are defined as passive components whose size across any dimension is much smaller than the operating wavelength [28]. For quantum computing in particular does lumped element filters have some advantages compared to non-lumped elements, as it allows for both a sharper frequency selectivity and roll-off. Other advantages includes a smaller size [28, 29], simpler topology [29], and a wider broadband [30].

Another reason to consider lumped elements filter is that, because of the discrete components, simple filter synthesis can be applied [31]. This allows for representation in simple equivalent circuits that can be simulated using various simulation software. For example, a 5th order

low-pass filter can be depicted as in Fig. 2

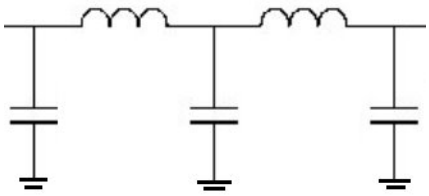


Figure 2: Circuit schematic of an arbitrary 5th order low-pass filter with shunt first topology.

where both the capacitors and inductors are considered as lumped elements.

Our filters can be treated as lumped elements, as the largest dimension is in the µm with a signal in the GHz regime, corresponding to an operating wavelength in the decimetres.

3 Methodology

In this section, the design and construction of the diplexer is explained. We go through the fundamentals of a diplexer and the specific construction requirements, as well as the design process and both the fabrication and stack layout.

3.1 Requirements and Fundamentals

The aim of this project is to design a diplexer as an additional on-chip element for the TWPA chip. The main requirements for the diplexer are the suppression of the pump frequency as well as minimal insertion loss for the signal coming from the QPU. With the given QPU signal frequency f_{RF} and pump frequency f_p seen in Fig. 3 the cut-off frequency for the diplexer was set to 9 GHz.

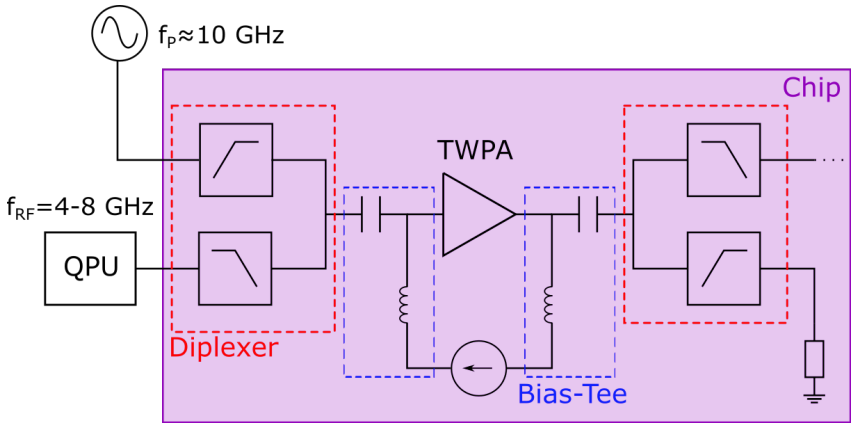


Figure 3: Schematic layout of the circuit. The QPU and pump are outside the chip whilst the diplexer (labelled in red) and Bias-Tee (labelled in blue) are on the chip together with the TWPA. For the S-parameters we have that 1 — QPU port, 2 — Pump port, 3 — TWPA port.

The complete structure consisting of the diplexer, the bias-tee for the TWPA biasing and the TWPA will be on-chip and located adjacent to the quantum unit. Hence, the space needed for the design should be minimal.

The diplexer consists of two filters. A low-pass filter connected to the QPU and a high-pass filter connected to the pump. The low-pass filter is the critical part of the diplexer, as it is responsible

for forwarding the signal while minimising losses. At the same time, it must guarantee that the pump frequency is suppressed in order to protect the QPU. With a matching of $S_{11} < -20\,\mathrm{dB}$ we get a transmission of over 90% in the passband of the low-pass filter. This ensures that the information in the quantum signal can be further processed. A steep roll-off is essential to achieve the suppression of the pump frequency. To ensure the safety of the QPU, the goal for the suppression of the pump frequency is set to $S_{21} < -25\,\mathrm{dB}$. The high-pass filter has to reject the quantum signal and pass the pump frequency to avoid losses from the pump and the quantum signal power. All design requirements are listed in Tab. 1. To achieve a compact design, lumped elements are used for the diplexer design.

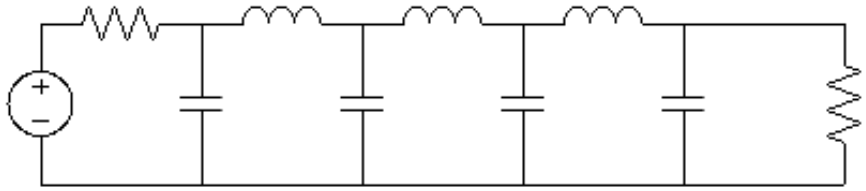
The design for the TWPA is already finalized and provides us with a given layer stack for our design work. The layer structure is schematically shown in Fig. 5. The TWPA is designed in microstrip technology; hence, we use the same technology for the diplexer. The layer structure we use is schematically shown in Fig. 5. To provide compatibility, we used an input impedance of $50\,\Omega$ for all ports. In the given stack, this can be achieved with a microstrip width of $1.5\,\mu\mathrm{m}$.

	Matching LP	Transmission LP	Matching HP	Transmission HP	Crosstalk
Bandwidth	$1-8\,\mathrm{GHz}$	$9.5-15\,\mathrm{GHz}$	$9.5-15\,\mathrm{GHz}$	$1-8\,\mathrm{GHz}$	$1-15\,\mathrm{GHz}$
S-parameters	$-20\,\mathrm{dB}$	$-20\,\mathrm{dB}$	$-20\,\mathrm{dB}$	$-20\,\mathrm{dB}$	$-25\,\mathrm{dB}$

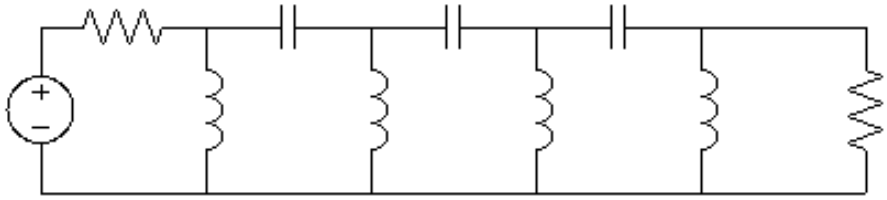
Table 1: Goal properties of the diplexer to achieve suppression of the pump frequency and minimal insertion loss for the QPU signal.

3.2 Design Process

A first sketch of the low-pass and high-pass filters was designed and simulated using the Marki Microwave online tool. This was done to see if there existed a filter that could obtain the desired properties. This simulation revealed that a Chebyshev filter of 7th order gave rise to the desired properties. The resulting circuit schematics is presented in Fig. 4.



(a) Low-pass filter



(b) High-pass filter

Figure 4: Schematics of 7th order Chebychev filters.

The Chebyshev filter uses only two kinds of circuit components: capacitors and inductors. As explained in Sec. 2.5, these elements have to be realised as lumped elements on the chip. Because of this the second step was to design some candidates for both lumped capacitors and lumped inductors using rough estimates for what kind of shapes and sizes that were likely to work. The designs of these elements were done in K-layout using a Python script to generate

a binary GDSII-file that the software Sonnet could use to simulate different frequencies and check if the elements were in the right range for the diplexer. The Sonnet simulation was done in correspondence with Keysights Advanced Design System (ADS) which slightly changed the dimensions of the element in order to find the optimal size. Once this was done the individual elements were put together and the low-pass and high-pass filter were simulated using Sonnet.

3.3 Fabrication and Stack Layout

While the physical diplexer was never constructed, a suggested construction process is presented in this sub-section. The fabrication process is suggested to follow a process similar to Alcalde-Herriaz *et al.* [10].

In order to fabricate the physical chip and the diplexer, an insulator should be used as a substrate. In this case, the substrate is made out of sapphire. The waveguide, constructed by niobium titanium nitride (NbTiN) is then sputtered on the chip, before a thicker layer of aluminium oxide (AlO_x) is deposited on top. The aluminium is applied in air, as to give the aluminium ample time to oxide. Finally, a layer of niobium is applied before etching to the specification needed. The suggested stack layout can be seen in Fig. 5.

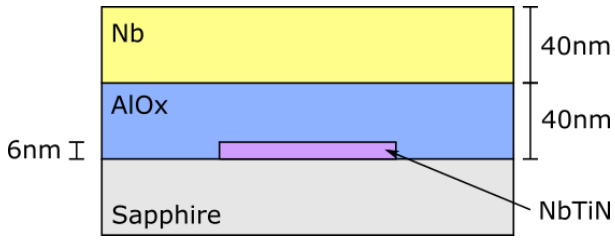


Figure 5: Example of film structure to construct diplexer. A dielectric substrate made of sapphire. Niobium titanium nitrogen (NbTiN) as waveguide, height of 6 nm. Aluminium oxide (AlO_x) as a dielectric between the waveguide and the Niobium (Nb) both with a height of 40 nm.

4 Results & Discussion

This section discusses and presents the results obtained from the Sonnet sweep. Comparisons are made between the final design and alternative designs. These alternative designs include both different dimensions on the specific elements and an analysis on series-first versus a shunt-first filter.

The design of the diplexer was constructed according to the limitations and constraints put on by the quantum processor unit (QPU) and the pump, as according to Fig. 3. The high-pass filter was therefore designed to allow frequencies above the cut-off frequency of 9 GHz and returning the rest, while the low-pass filter was designed to allow frequencies below the cut-off frequency and deny the rest.

4.1 Element Design and Analysis

As explained in 3.2, we started creating the layout of the elements needed for the filters. Due to the layout structure, the low-pass and high-pass filters need partly different elements. For the low-pass filter, a series capacitor and a series inductor are needed (depicted in Fig. 6).

The same series inductor layout can be used for both filters. We chose a basic layout of three turns for the inductor. To obtain a higher inductance is the ground plane over the meandering area removed. Again, the height of the element was used as the adaptable parameter (Fig. 7b).

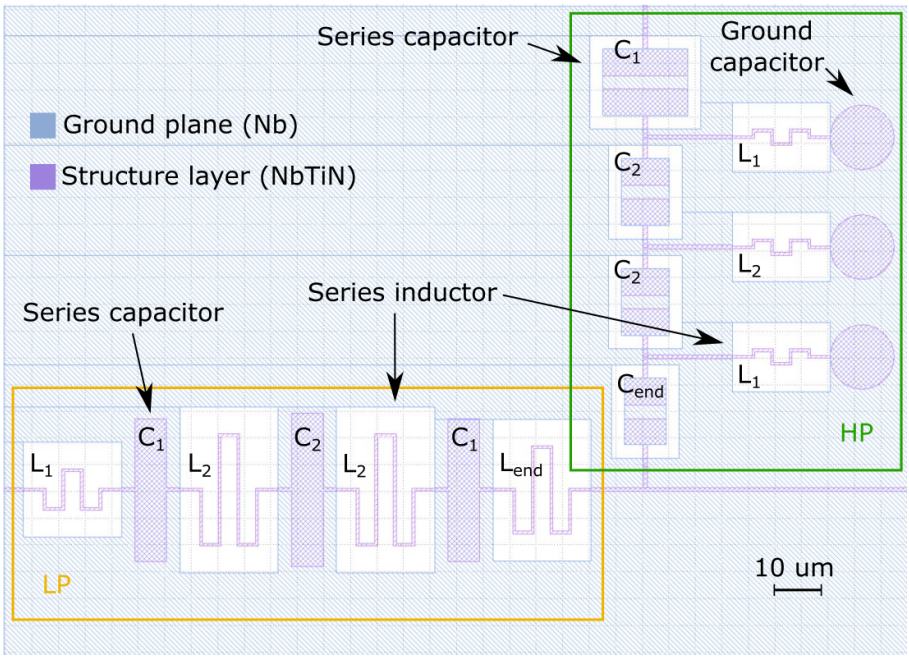


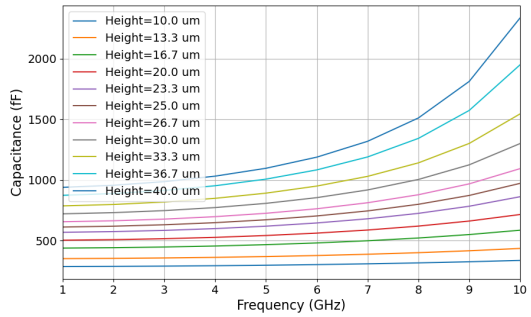
Figure 6: Layout of the final diplexer design consisting of the low-pass filter (orange) and the high-pass filter (green), with indications of the capacitances and inductance. However, L,$C_{i,LP} \neq L$,$C_{i,HP}$.

For the high-pass filter is the required inductance lower than for the low-pass filter, hence the height was adjusted accordingly.

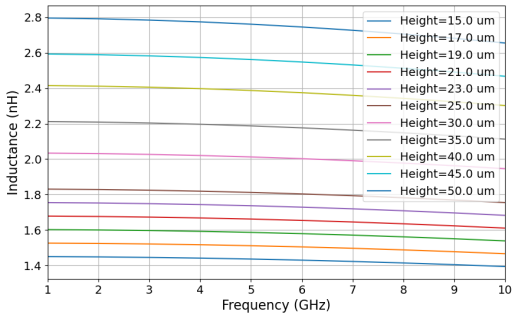
The circuit schematic in Fig. 4b shows, that for the high-pass filter, a series capacitor is needed. This capacitor is created by placing two rectangles, each connected to different microstrip lines, and leaving a small gap of 5 µm between them. Above them, in a larger rectangle centred in the middle of the two plates is a part of the ground plane is removed, but above the two rectangles is a connecting area of the ground plane kept. This creates a structure consisting of two capacitors in series. We choose this structure to avoid multi-layer capacitor structures, as for example presented in [23, 28]. As a consequence of the two capacitances in series, the achievable total capacitance of the series capacitor is lower than of the shunt capacitor. Different values of the series capacitor when changing the gap or the height of the capacitor are shown in Fig. 7d and 7c, respectively. The sweep over different gap sizes prove that the gap size has no relevant influence on the performance of the capacitor. This can be explained by the difference in one order of magnitude between the gap size (µm) and the substrate layer thickness (40 nm).

The shunt capacitor is a NbTiN area which creates a capacity to ground (Nb layer). It has a fixed width of 12 µm and only the height was changed in order to optimize the area needed for the capacitor. In Fig. 7a, the simulation results of different heights are plotted.

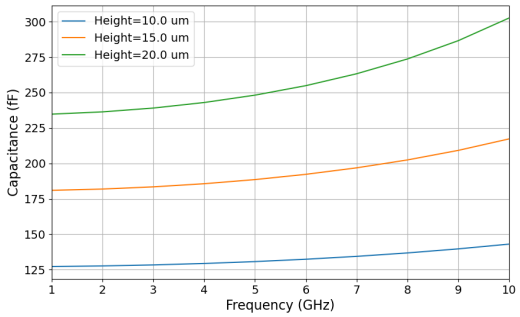
Regarding the circuit schematic of the high-pass filter (Fig. 4b), an additional capacitance had to be added between the shunt inductor and the ground to allow the realization in the given layer structure. This capacitance acts as low impedance connection to the ground. The impedance $Z = 1/j\omega C$ is minimised by using a large capacitance. Our ground capacitor has a diameter of 24 µm with a capacitance of around 1.5 pF. We found, that a larger diameter of the capacitor would lead into a resonance in our working bandwidth of $0 - 15$ GHz, hence it would be not functioning any more. With the diameter of 24 µm the resonance is located at approximately 11 GHz. Since, the high frequencies above the cut-off frequency of 9.5 GHz are passed by the high-pass filter only frequencies below reach the ground capacitor. Those frequencies are below the resonance frequency of the ground capacitor and hence experience a real capacitance.



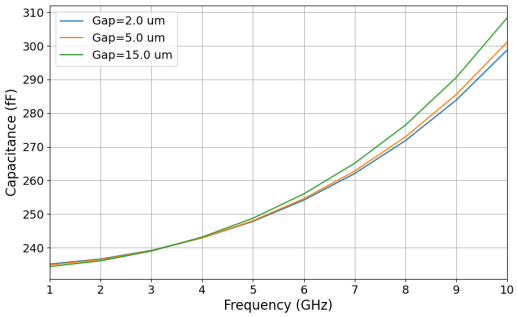
(a) Shunt capacitor



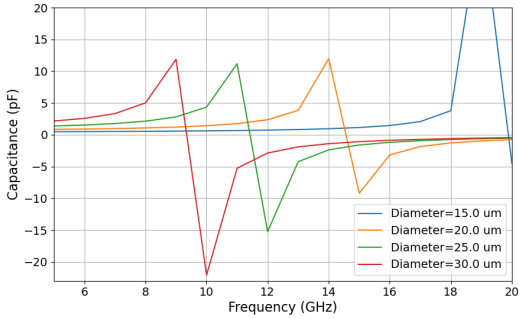
(b) Meandered inductor



(c) Series capacitor - height



(d) Series capacitor - gap



(e) Ground capacitor

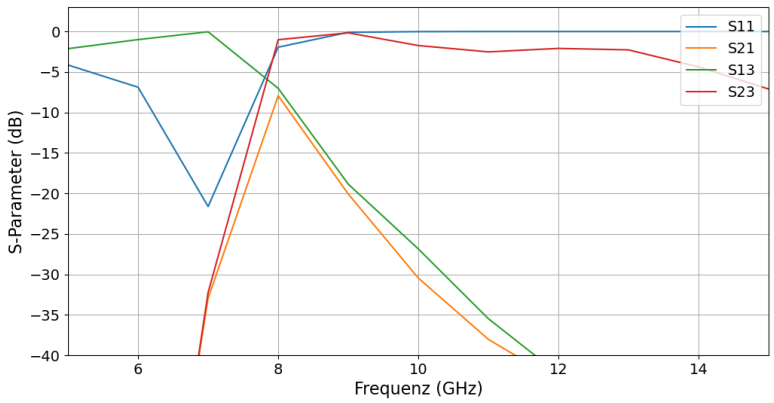
Figure 7: Variable sweeps performed on the different lumped element geometries.

The resonance in the capacitor arises, when the requirement of element size $\ll \lambda$ for lumped elements, presented in Sec. 2.5, is not fulfilled any more. Due to the shape of the graph for the height of 40 µm in Fig. 7a, it is expected that a resonance will also occur for a shunt capacitor shortly after 10 GHz. Therefore, also the shunt capacitor has a maximum achievable capacity in the given stack as a lumped element.

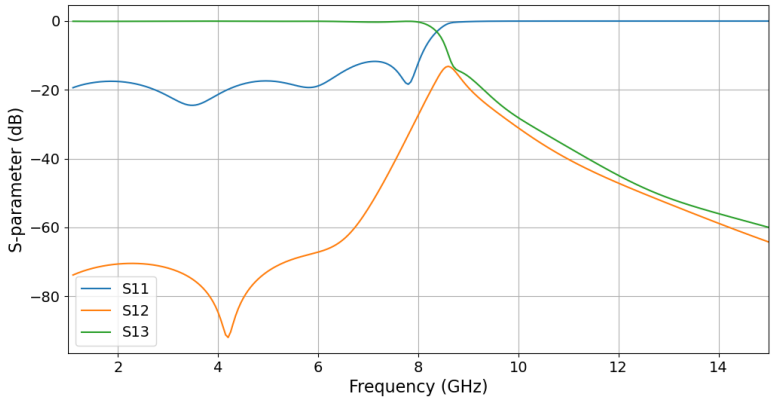
4.2 Shunt-first and Series-first Layout Analysis

In this section, we analyse the performance of shunt-first and series-first layouts for the diplexer. The initial design utilized a shunt-first approach for both the low-pass and high-pass filters. However, this configuration exhibited significant issues, as shown by the S-parameter plots in Fig. 8a. The shunt-first design resulted in poor matching for the QPU signal and bad transmission characteristics. Especially for frequencies lower than 7 GHz. Similar problems were observed for the S_{23} parameter, which represents the path from the pump to the TWPA. Over the whole range above the cut-off frequency, only a transmission of around −3 dB is

achieved.



(a) Shunt-first design



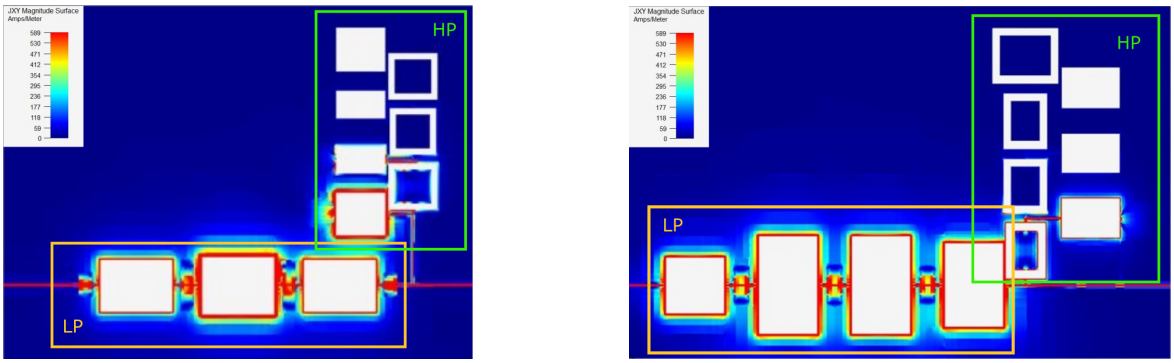
(b) Series-first design

Figure 8: S-parameter simulation results from Sonnet for the shunt- and series-first diplexer designs. 1 — QPU port, 2 — Pump port, 3 — TWPA port.

To address these issues, the design was revised to a series-first layout. This new design enabled a significantly improved the performance, as shown in the S-parameter plot of the final diplexer design in Fig. 8b. The series-first layout provided better transmission characteristics, effectively resolving the problems encountered in the shunt-first design.

A closer investigation into the cause of these issues was conducted using current density plots from Fig. 9 . These current density plots illustrate the isolation issues encountered in the shunt-first diplexer design. These plots show the current density on the ground plane, with the empty white rectangles indicating areas where the ground plane is removed above the inductors. In the high-pass filter, the ground plane with the surrounding slit represents the series capacitors. The impedance to ground over the first inductor ($Z = j\omega L$) is low for the QPU signal, leading to poor isolation. This results in significant portions of the low-frequency signals from the low-pass filter being diverted through the high-pass filter and grounded via the inductor, rather than reaching the output port. Consequently, this causes undesirable signal leakage and poor transmission characteristics.

In contrast, the series-first layout, as shown in Fig. 9b, demonstrates improved isolation. By placing the series elements first, the impedance mismatch at the junction of the high-pass and low-pass filters is minimized, reducing the interaction between the two paths. Hence, the current



(a) Shunt-first layout

(b) Series-first layout

Figure 9: Current density plots from diplexer simulation in Sonnet. The power is injected into the left port of the low-pass filter. The top port of the high-pass filter is the connection to the pump, and the port to the amplifier is on the right.

density in the first shunt element in the high-pass filter is significantly reduced. The series-first layout effectively directs the low-frequency signals from the QPU through the low-pass filter to the output port, while high-frequency signals are appropriately routed through the high-pass filter.

4.3 Series-first Diplexer

Due to the isolation issues with the shunt-first filter configuration, we decided to continue with the series-first filter configuration. However, new challenges arose with this design. Constructing filters that could achieve both $-20\,\mathrm{dB}$ matching and a steep roll-off to reach the target cut-off frequency simultaneously, proved to be much more difficult with the series-first filter than for the shunt-first filter.

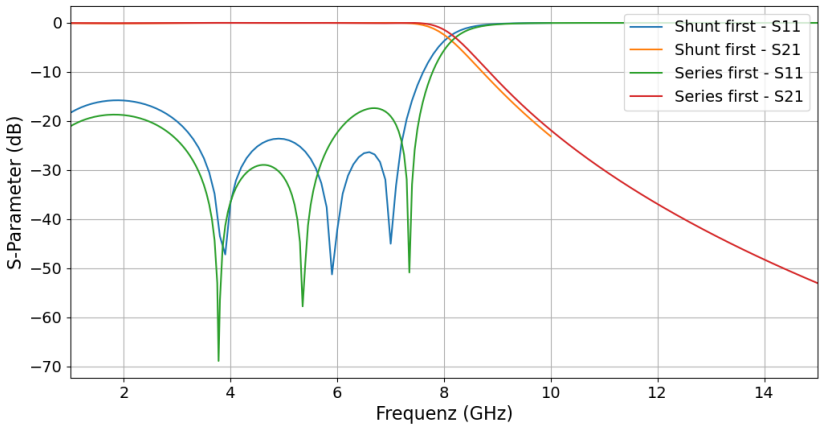
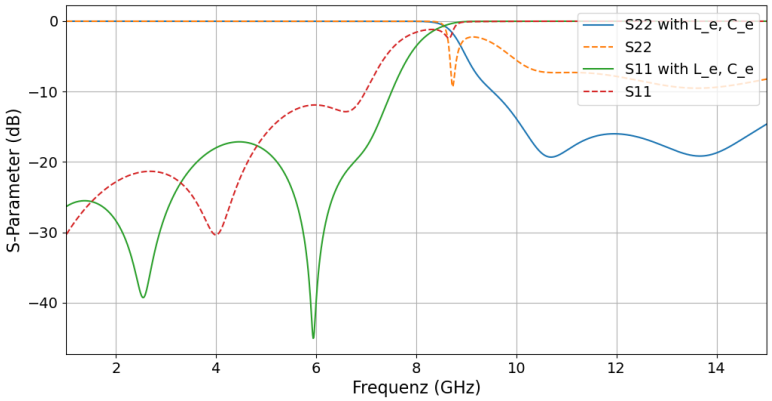


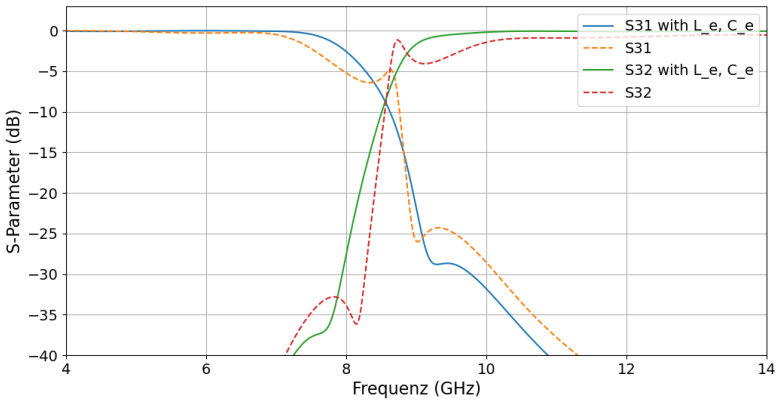
Figure 10: Sonnet simulation results of the shunt- and series-first low-pass filters.

Fig. 10 illustrates the differences in the S-parameters. In particular, the requirements for matching were difficult to fulfil. The S_{11} parameter for the series-first layout exceeds the limit of $-20\,\mathrm{dB}$ in the region around $6.5\,\mathrm{GHz}$. Although, the shunt-first layout exceeds the limits at the frequency of $2\,\mathrm{GHz}$ this is a less critical reign, since the QPU signal ranges from $4-8\,\mathrm{GHz}$. The aim for the roll off of S_{11} at $8\,\mathrm{GHz}$ fail both layouts. This results from the requirements of the pump suppression of $-20\,\mathrm{dB}$ at $10\,\mathrm{GHz}$. A trade-off had to be made between the two

requirements. The difficulties for designing the series-first high-pass filter might result from the fact that a shunt or π configuration can be more robust against fluctuations in inductance and capacitance [32].



(a) Lowpass filter shunt capacitor first



(b) Low-pass filter series inductor first

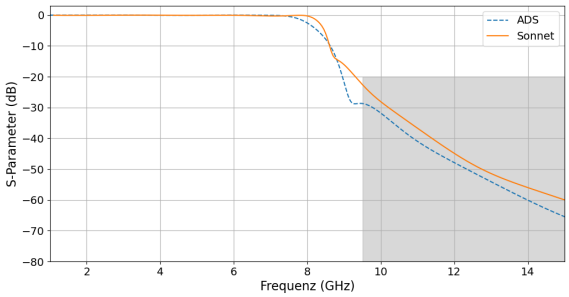
Figure 11: Comparison of ADS simulation results without and with optimized end elements L_{end} and C_{end}. 1 — QPU port, 2 — pump port, 3 — TWPU port.

The new diplexer, composed of the new series-first low-pass and high-pass filter, did not show the expected behaviour in the simulations either. For a better analysis with faster simulation times, we recreated the layout as a equivalent circuit diagram in ADS (Appendix Fig. 15b). The results of the S-parameter simulation are depicted in Fig. 11. These simulations indicate a resonance at the cut-off frequency. The resonance likely originates from an interaction between the final elements of each filter. To eliminate this, the last two elements were replaced with the optimized components. L_1 at the end of the low-pass filter is replaced by L_{end} and C_1 at the end of the high-pass filter is replaced by C_e (as shown in Fig. 6). With these end elements, the behaviour of the diplexer could be significantly improved. This design fundamentally fulfils the requirements for the diplexer. However, the difficulties of the filter design are still evident in the simulations of optimized diplexer design. The matching goal of $-20\,\mathrm{dB}$ cannot be achieved for the whole bandwidth of the QPU and pump port. This also becomes apparent in the transmission of the QPU signal (S_{31} in Fig. 11b), where the transmission begins to drop already before the higher end of the bandwidth range of $8\,\mathrm{GHz}$. However, the aim of at least $-25\,\mathrm{dB}$ suppression of the pump frequency at $10\,\mathrm{GHz}$ is achieved. These simulations emphasize the fundamental challenge that repentantly arose during the design process. The passband of the QPU signal ($4-8\,\mathrm{GHz}$)

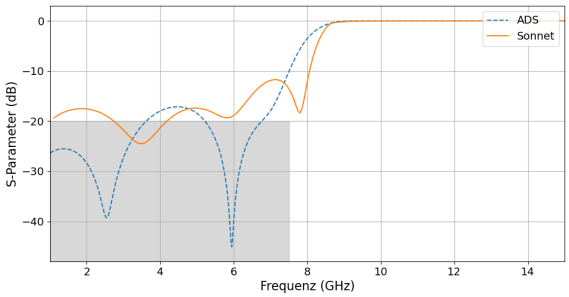
is very close to the stop band for the low-pass filter, which starts at around 9 GHz. With the given design, using 7th order Chebyshev filters, the set requirements are difficult to fulfil.

Figure 12 presents the simulation results from both ADS and Sonnet, illustrating the performance of the diplexer. The diplexer demonstrates functionality close to meeting its primary design requirements. Key parameters, including QPU signal transmission (S_{31}), QPU port matching (S_{11}), and crosstalk suppression (S_{21}), show acceptable levels of performance. The consistency between ADS and Sonnet results further reinforces the reliability of the theoretical models and their successful implementation in the physical design.

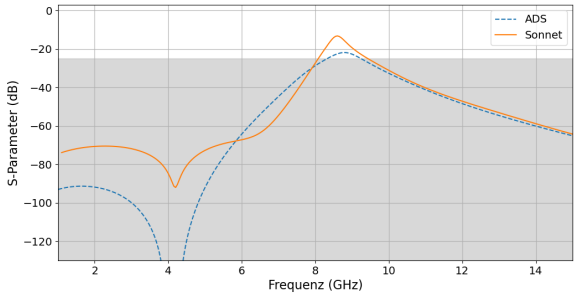
The results of ADS simulations, based purely on electrical circuit components, and Sonnet simulations, incorporating modelled physical elements, demonstrate the effectiveness of the design workflow. The similarity in values indicates that quick initial simulations in ADS can serve as a reliable foundation. Once an optimized filter is synthesized in ADS, it can be refined and validated in Sonnet using physical element models. This streamlined process significantly reduces the time and effort required for filter design and optimization.



(a) S_{31}: Transmission of the QPU Signal to the TWPA.



(b) S_{11}: Matching of the QPU port.

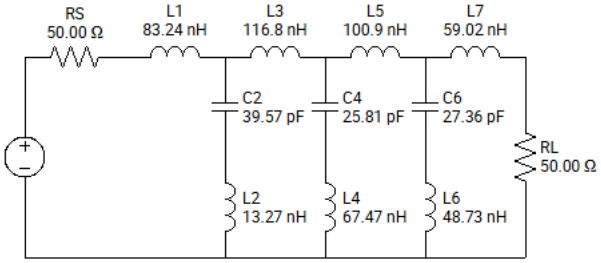


(c) S_{21}: Crosstalk between the QPU and the pump port.

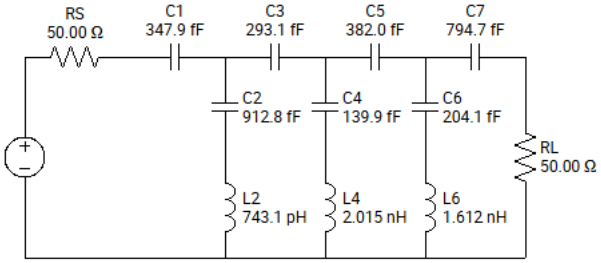
Figure 12: Comparison of simulation results after optimization in ADS and Sonnet.

4.4 Elliptical Filters

To improve the performance of our diplexer, an elliptical filter design could be adopted. Elliptical filters have the sharpest roll-off of any filter type, which would likely result in better performance, since other parameters can be more relaxed while still achieving the desired steepness. Improved filters would enhance the diplexer's overall performance. However, adopting an elliptical filter design introduces challenges, including a more complex circuit structure with a larger number of elements, as shown in Fig. 13. This complexity makes optimization and fabrication more difficult.



(a) Low-pass filter



(b) High-pass filter

Figure 13: Schematics of 7th order elliptical filters.

Despite these challenges, the results of our optimized circuits in ADS and Sonnet, as discussed in the previous section, are very similar. This suggests that thorough initial optimization in ADS can provide a strong foundation. Once promising results are achieved in ADS, it would simplify the process of constructing the actual diplexer with physical components in Sonnet.

Additionally, the high-pass filter circuit can be identified as an elliptical filter design due to the inclusion of a capacitor coupled to ground. While the elements are currently arranged in the wrong order, they can be rearranged in a series circuit without altering the overall performance. However, achieving the required component values remains a significant challenge. As shown in Figure 13, the inductors in the elliptical filter must reach values of approximately 116 nH, whereas our current design achieves only up to 2.8 nH. Similarly, for the series capacitor, the required value is approximately 800 fF, but our current design reaches only about 270 fF. For the ground capacitor, the required value is about 39 pF, while our existing design achieves only up to 2 pF. These discrepancies emphasize the need for new component designs to successfully implement the elliptical filter configuration.

4.5 Bias-Tee

For a functioning TWPA, a pre-connected bias-tee is necessary, as shown in the schematic of Fig. 6. It consists of a series capacitor and an inductor. To bias the TWPA, the inductor should pass the DC current, while the capacitor should block the DC current and direct it to the TWPA. We conducted some simulations in ADS to determine the necessary order of magnitude of the values for the two elements. From previous element sweeps, we know that

the capacitors used for the filters are already close to their resonance. Therefore, the design was optimized to have minimal capacitance while still being sufficient to block the DC current from entering the diplexer. This resulted in a capacitance of around 3 pF and an inductance of 23 nH. With these values, the cut-off frequency is at 600 MHz. At this frequency is also the lowest isolation between DC current source and the diplexer of −10 dB.

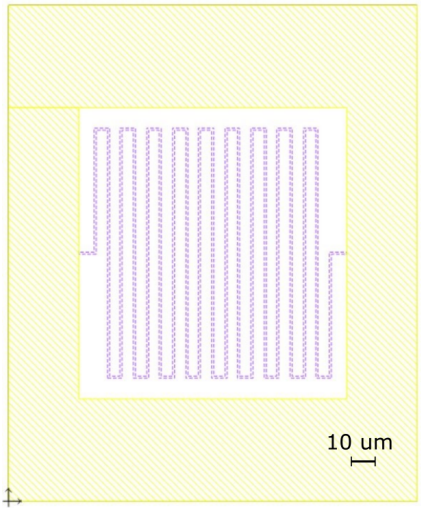


Figure 14: Layout of an 18-turn inductor for the bias-tee.

For these values we designed an 18-turn inductor as shown in Fig. 14. With this layout an inductance in the range of 28.6 nH at 500 MHz to 23.5 nH at 5500 MHz is achieved. Therefore, the existing design should allow the development of a suitable inductor. Also, the necessary series inductor was simulated. For this design, it was more challenging to design an element with the correct capacitance. Due to the resonance, which moves to lower frequencies as the capacitor increases in size, the capacitance of the series capacitor can be increased up to around 2.5 pF at 10 GHz. However, at lower frequencies the capacitance is only at around 850 pF. Therefore, it might be necessary to change the design of the capacitor or investigate a layout with multiple capacitors in parallel. To validate these ideas, further Sonnet simulations will be necessary.

4.6 Measurements

Due to tools being broken in the clean room, the fabrication of the device had to be delayed. Since no physical device has been fabricated, measurements have not yet been possible. The simulation results discussed above are a good indication of what to expect from the physical implementation of the proposed design once it has been fabricated, but due to both imperfections stemming from the fabrication process and the fact that simulations has to rely on some approximations, the characteristics of the final device might be a bit different.

5 Conclusion

The aim of the project was to design an on-chip diplexer for a TWPA, working for a source signal at 4-8 GHz and a pump frequency at about 10 GHz, with maximal suppression of the pump frequency and minimal insertion loss for the source signal. To realize this, the goal requirement for the cut-off frequency was set to 9 GHz, matching of $S_{11} < -20$ dB and suppression of the pump frequency of $S_{21} < -25$ dB.

With the final series-first diplexer design proposed in this report, the matching goal of −20 dB

couldn't be achieved for the whole bandwidth of the QPU and pump port, while, the goal of at least -25 GHz suppression of the pump frequency at 10 GHz was achieved. However simulation results from both ADS and Sonnet showed how the functionality of the diplexor is still likely to be within acceptable levels of preformance, indicating perhaps how the matching goal might have been set to high. Since the design has not yet been fabricated, no measurement on a physical device has been possible, which means that the real characteristics of the design is not known.

The similarity in values between ADS and Sonnet results showed in this report, indicates that quick initial simulations in ADS can serve as a reliable foundation, and help with a more streamlined and less time consuming design process.

This project has dealt with the first steps of designing a well suited on-chip diplexer for a TWPA. The next steps consist of fabrication and measurements. In this report we have shown a design that will likely work relatively well. Future work should lead to a second iteration of the design based on the measurements results. For this second iteration we propose a design based on elliptical filters instead of Chebyshev filters.

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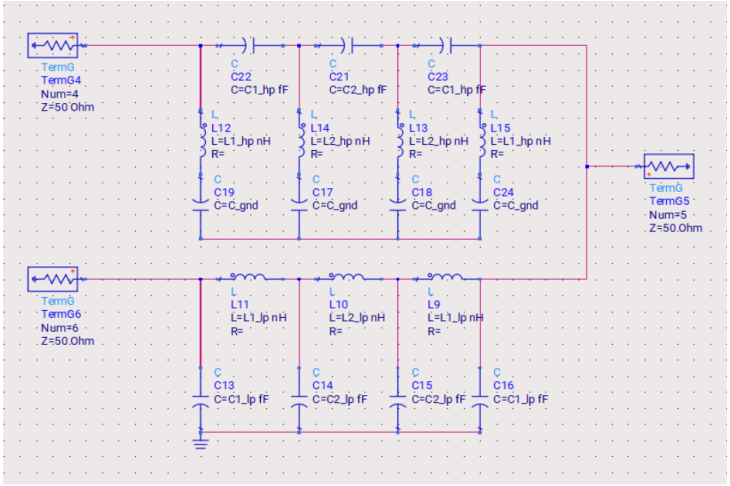
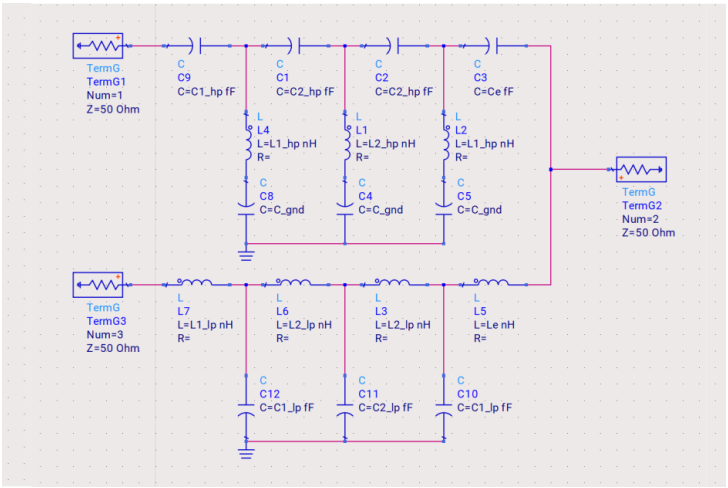
A Appendix

A.1 ADS simulation schemes



(a)



(b)

Figure 15: Diplexer design with (a) shunt first filters and (b) series first filters.