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Performance and Cost Analysis of GaN and Si Devices in Two-Level and Three-Level NPDC Voltage Source Inverter Topologies

Thesis Report

Master's thesis in Sustainable electric power engineering and electromobility, MPEPO

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Final report

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Abstract

This thesis presents a comparative study of two-level and three-level three-phase inverter topologies utilizing Silicon MOSFETs and Gallium Nitride HEMTs. The analysis focuses on performance metrics, including power loss, total harmonic distortion, common mode currents, and cost-effectiveness. The investigated system is a low-voltage (< 60 V DC) inverter intended to drive a permanent magnet synchronous machine-based water pump in data center cooling applications.

All simulations are conducted in *LTspice* and the results show that the Gallium Nitride-based two-level inverter operating at 16 kHz achieves a system efficiency of 98.27 %, and a total harmonic distortion of 2.87 %. In contrast, the corresponding Silicon-based two-level inverter exhibits a lower efficiency, 97.79%, and a total harmonic distortion of 2.88 %. When the switching frequency of the Gallium Nitride two-level inverter is increased to 200 kHz, the total harmonic distortion is reduced significantly to 0.25 %, while the power loss increases slightly.

Three-level neutral-point diode clamped inverters exhibit lower common mode currents due to reduced amplitude of the switching voltage. However, the three-level Gallium Nitride inverter at 200 kHz shows a slightly increased total harmonic distortion of 0.78 % compared to its two-level counterpart at the same frequency, which can be attributed to the non-ideal behavior of clamping diodes and voltage variations over the DC-link capacitors.

Analyzing the theoretical and simulated power losses in the semiconductors, Gallium Nitride transistor showed a reduction of 86.21% in switching losses when compared to Silicon MOSFETs in a two-level inverter. The three-level Gallium nitride inverter further reduced the switching losses by 69.92% compared to the two-level Gallium nitride inverter. However, the conduction and diode losses in the neutral-point diode clamped inverter increased the total power loss, making the two-level inverter more efficient in comparison. At high switching frequencies, above 723 kHz, the theoretical model predicts that the three-level inverter will be more efficient.

The cost analysis shows that although the Gallium Nitride-based two-level inverter has a higher initial cost, its improved efficiency offsets this over time. At a switching frequency of 16 kHz, the break-even point is approximately six years, after which the accumulated energy savings equal the additional upfront investment.

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We are also very grateful to *Aros Electronics AB* for giving us the chance to carry out this work in an industrial setting. A special thank you goes to our company supervisor, Dimitrios Meintanis, for his helpful advice, technical support, and steady encouragement during our time at Aros.

Lastly, we want to thank our families for their patience, support, and belief in us every step of the way. This journey would not have been possible without them.

To all of you, thank you for being part of this project.

Jawed Hakimi and Alexander Rehnberg, Gothenburg, June 2025

List of Acronyms

2DEG	Two-dimensional Electron Gas
2L3P	Two-Level Three-Phase
3L3P	Three-Level Three-Phase
AlGaN	Aluminum Gallium Nitride
BOM	Bill of Materials
CMC	Common Mode Current
CMV	Common Mode Voltage
EM	Electrical Machine
EMF	Electromotive Force
EMI	Electromagnetic Interference
FET	Field-effect transistor
FFT	Fast Fourier Transform
FOM	Figure of merit
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
LISN	Line Impedance Stabilization Network
MCSPWM	Multi-carrier Sinusoidal Pulse Width Modulation
MLI	Multilevel Inverter
MOSFET	Metal-oxide field effect transistor
NPDC	Neutral-Point Diode Clamped
NPCMI	Neutral-Point Clamped Multilevel Inverter
NPP	Neutral Point Potential
PCB	Printed Circuit Board
PD-SPWM	Phase Disposition Sinusoidal Pulse Width Modulation
PMSM	Permanent Magnet Synchronous Machine
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
Si	Silicon
$\text{THD}_{I_{phs}}$	Total Harmonic Distortion
VSI	Voltage Source Inverter
WBG	Wide Bandgap

Contents

1

Introduction

1.1 Background

Power electronics, particularly solid-state switch-based converters, play an important role in modern society and industry. These devices are, for instance, inverters, responsible for converting DC from a source into AC, which is essential for powering a variety of loads, including electric machines utilized in electric vehicles, vessels, robotic arms, pumps, fans, and more. In recent years, the usage of inverters has significantly increased due to the growing integration of renewable energy sources such as photovoltaic cells, wind energy, smaller energy storage systems in smart homes, and vehicle-to-grid applications [1, 2].

In some of these instances, especially for low-power applications, two-level inverters are commonly employed due to their simplicity and cost-effectiveness [3]. However, two-level inverters encounter several challenges, including high voltage/current distortions in the output waveforms, high voltage change rates (dv/dt) that can induce stress on both the switches and the load, and the potential for Electromagnetic Interference (EMI) in the absence of appropriate filters [4]. Harmonic contents of the supplied voltage, in particular, cause efficiency and performance reduction in electrical machines [5]. Additionally, two-level inverters have significant Common Mode Voltage (CMV) and, as a result, Common Mode Currents (CMCs). CMCs pose a potential fault risk for motor-driven applications, due to currents conducting to the chassis through the bearings, eventually causing bearing failures [6]. A common solution to address these challenges is to incorporate filters on the inverter's input and output. Examples of such filters include EMI filters, AC load reactors, dv/dt filters, and sine wave filters [7]. The design and implementation of these filters, however, can become more complex and costly depending on the frequency and harmonic distortion present in the output waveforms.

While the implementation of filters is viable in certain applications, it may not always be the most efficient, compact, or cost-effective solution. An alternative strategy involves the use of multilevel inverters (MLIs), which can effectively reduce the adverse effects of harmonic distortion and high dv/dt [8]. In these inverters, power Si-MOSFETs can be used as electrical switches; however, these devices typically exhibit higher switching losses compared to wide-bandgap transistors (WBGTs) when operating at the same switching frequency [9]. The combination of WBGTs with a multilevel inverter, in theory, should be a direct improvement in terms of power

efficiency and quality of AC output, compared to a two-level inverter.

To validate whether WBGTs and multilevel inverters solve the issues with two-level inverters, this thesis explores their application in a low-voltage (<60 V DC) inverter. The inverter examined in this study is developed by *Aros Electronics AB*, a company specializing in motor drives, electrical machines, and other related products. Specifically, this work focuses on a Permanent Magnet Synchronous Machine (PMSM) with an integrated Two-Level Three-Phase (2L3P) inverter designed by *Aros Electronics AB*. The PMSM, powered by an AC mains supply, has a rated power of approximately 1 kW. Its intended application is to pump coolant water for computers in data centers.

1.2 Thesis aim

The aim of this thesis is to evaluate the performance of Two-Level Three-Phase (2L3P) and Three-Level Three-Phase (3L3P) Neutral Point Diode Clamped (NPDC) inverters, using two different, but similarly power-rated, transistor technologies: Si-HEXFET and Gallium Nitride-High Electron Mobility Transistor (GaN-HEMT) WBGT. The performance metrics evaluated to determine non-ideal inverter effects are: CMC, EMI, and harmonic distortions. Furthermore, the economic trade-offs of the topologies are evaluated by the following performance metrics for the inverters: accumulated cost due to power losses over time and production cost.

1.3 Specifications of the investigated issues

In order to achieve the aim of the thesis, the following areas are studied.

1. Investigate the performance metrics in 2L3P and 3L3P Neutral-Point Diode Clamped (NPDC) with Si-HEXFET, i.e, analyze CMC, EMI, harmonic content output, as well as accumulated cost for switching- and conduction losses over time and initial component cost.
2. How does GaN-HEMT impact performance metrics compared to Si-HEXFET switches for the mentioned inverters?
3. How are the performance metrics of the inverters influenced by different switching frequencies?

1.4 Scope

This thesis investigates the performance of two different inverter topologies, 2L3P and 3L3P NPDC, and two different transistor technologies: Si-HEXFET and GaN-HEMT. The selection of the NPDC 3L3P inverter is due to its simplistic design and low-cost. GaN-HEMT switches are selected as the WBGTs to study the performance and behavior of GaN-HEMTs, with the Si-HEXFET used as a benchmark. The switches are chosen such that both switches have similar power ratings and have

an existing *Spice* model. While results may differ with other inverter topologies and switch types, the results are comparative in terms of inverter and switch configurations. As such, a comparative study using different switches and topologies would most probably be similar to the comparisons done in this study. These constraints are applied to keep the project within the thesis time frame.

The study is limited to steady-state operation and does not include dynamic behavior or control strategies. Instead, the inverter control is implemented through Sinusoidal Pulse Width Modulation (SPWM) for the two-level topology and Phase Disposition Sinusoidal Pulse Width Modulation (PD-SPWM) for the three-level topology. While multiple different Multi-Carrier SPWM techniques exist, the tradeoffs are generally between the inverter losses and harmonic contents of the output voltage [10]. The Electrical Machine (EM) is modeled as a non-salient PMSM, operating in steady state with fixed torque and speed, and is implemented in *LTspice* as an RL circuit with sinusoidal back Electromotive Force (EMF) sources. The inverter input is modeled as an ideal DC voltage source, and the front-end AC-DC conversion stage is not considered.

All simulations are performed in *LTspice*, with behavioral voltage sources used to generate gate signals. The same gate-driving logic and modulation parameters are applied across both inverter types to ensure fair comparisons. Performance metrics such as Total Harmonic Distortion (THD), CMC, EMI, and overall system efficiency are evaluated for each configuration. These are compared against a baseline two-level inverter using Si-MOSFETs.

Power losses are theoretically calculated using models for conduction, switching, diode recovery, and parasitic effects, and are compared to *LTspice* simulation data. The cost analysis includes both the initial component cost, based on Bill of Materials (BOM) values from *Aros Electronics AB*, and operational cost, estimated from simulated power loss and regional electricity prices.

Parasitic effects such as stray capacitances contributing to CMC and EMI are estimated from the physical layout of an existing Printed Circuit Board (PCB) for the two-level design and extrapolated for the three-level inverters. While the simulations provide accurate relative performance comparisons, the thesis does not include dynamic load scenarios or grid-connected inverter operation.

The PWM signal controls inverter switching, where fast transitions can cause voltage overshoots due to factors such as motor impedance, cable length, switch rise time, and switching voltage magnitude [7]. Since this thesis focuses on inverter topology and design, detailed modeling of overshoot and its impact on the EM is beyond its scope. As for the switches, gate resistors are used to minimize voltage ringing during switching.

The overall goal is to isolate and assess the influence of inverter topology and switch technology on performance and cost-effectiveness in low-voltage, motor-drive appli-

cations.

2

DC to AC converters and EM Modeling

This chapter provides the theoretical background required to analyze and compare 2L3P and 3L3P inverter topologies, which form the basis of this thesis work. It begins with an explanation of the operating principles of a 2L3P Voltage Source Inverter (VSI), followed by an introduction to multilevel inverter concepts, with a focus on the 3L3P NPDC inverter. A comparison between two-level and three-level inverter structures is then presented to highlight their respective advantages and limitations.

The chapter further discusses important design aspects such as DC-link capacitor sizing and voltage balancing techniques. Key phenomena affecting inverter performance, including voltage overshoot, EMI, harmonic distortion, and CMC, are also examined. Additionally, the modeling approach for the EM used in the simulations is described. This theoretical foundation supports the subsequent analysis and evaluation of inverter performance carried out in later chapters.

The terms *two-level* and *three-level* inverters have been mentioned frequently up to this point. It is therefore important to clarify their meaning. The number of levels in an inverter refers to the number of discrete phase output voltage levels it can produce [11]. Specifically, a two-level inverter generates two discrete voltage levels, while a three-level inverter produces three. This concept is further detailed in the following sections.

2.1 2L3P Voltage Source Inverter

This section introduces the basic operation of the 2L3P VSI, a widely used inverter topology in motor drive applications [12]. In such inverters, the main purpose is to convert a DC input voltage into a three-phase AC output voltage that can be used to drive EMs such as PMSMs. To achieve this, the inverter uses power electronic switches to control the direction of the current flow. A minimum of six switches is needed for a 2L3P inverter, with two switches per phase. Additionally, the three-phase output voltages are 120° apart from each other to form a balanced three-phase AC supply. The instantaneous output voltage for each phase depends on the switching state and the DC-link voltage.

Figure 2.1 shows the detailed schematic of a 2L3P inverter. In this inverter configuration, each leg of the inverter (phase A, B, and C) consists of two switches connected in series between the positive and negative terminals of the DC-link input. The output to each phase is taken from the midpoint between the two switches. Each switch is paralleled with a freewheeling diode (intrinsic) to protect against reverse current caused by inductive loads [13, 14]. The fictitious neutral point, o, between the two input capacitors, C_{in}, does not exist in a real inverter; it is included here as an example.

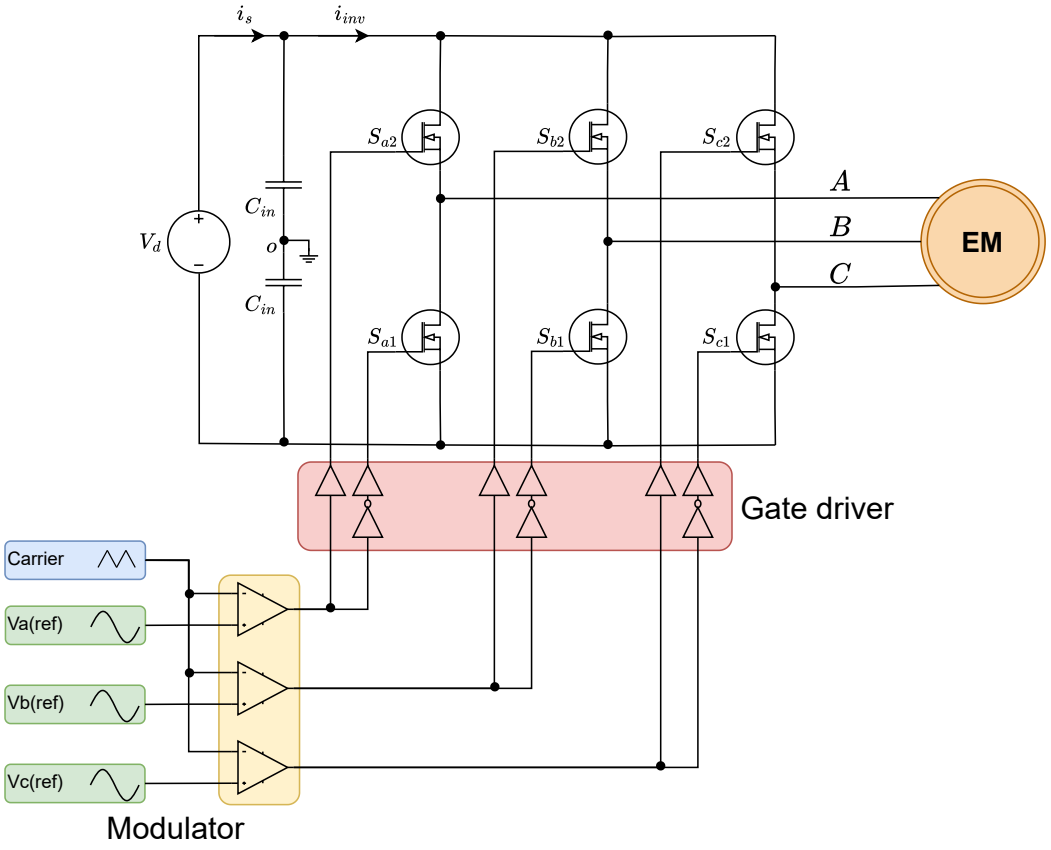


Figure 2.1: 2L3P inverter with fictitious neutral point o.

To control the output voltage waveform, the modulator utilizes a technique called sinusoidal pulse-width modulation (SPWM). The main idea behind SPWM is to compare a sinusoidal reference signal, which represents the desired phase voltage, with a higher-frequency triangular carrier signal, and this is performed by a modulator. The modulator operates as follows: For each phase, when the reference signal (sinusoidal wave) is greater than the carrier signal (triangular wave), the upper switch in that leg is activated, i.e. $S_{x2} = 1$. If the reference is lower than the carrier, the lower switch is activated, i.e. $S_{x1} = 1$. As illustrated in Figure 2.1, the gate signals for the lower switches are inverted, since turning on the upper and lower switches simultaneously would cause a short circuit. This process generates a series

of voltage pulses whose average over each carrier wave period approximates a sinusoidal waveform. The inverter then performs this switching operation continuously for each phase. Table 2.1 lists the possible switching states and the resulting output voltages for different operation intervals within one electrical cycle, the output voltage is shown only for the two phases A and B.

Table 2.1: Operation states of phase switches for a 2L3P VSI using SPWM technique. In this inverter, the phase voltage has two states ($\pm\frac{V_d}{2}$) and the phase-to-phase voltage has three states ($-V_d, 0, +V_d$). In the switching states (gate signals), (1) indicates the switch is turned on.

Operation interval	**Switching states**						v_{ao} level	v_{aN} level	v_{ab} level
	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}			
1	0	1	1	0	0	1	$+V_d/2$	$+V_d/3$	$-V_d$
2	0	1	1	0	1	0	$+V_d/2$	$+2V_d/3$	$-V_d$
3	0	1	0	1	1	0	$+V_d/2$	$+V_d/3$	0
4	1	0	0	1	1	0	$-V_d/2$	$-V_d/3$	$+V_d$
5	1	0	0	1	0	1	$-V_d/2$	$-2V_d/3$	$+V_d$
6	1	0	1	0	0	1	$-V_d/2$	$-V_d/3$	0

The inverter repeats these switching sequences/intervals every electrical cycle to produce the desired sinusoidal output. During each interval, three of the six switches conduct, forming the necessary line-to-line voltages to drive the load. Figure 2.2 further clarifies the SPWM process, showing how the carrier and reference signals determine the gate pulses and the resulting phase-to-phase voltages described in Table 2.1.

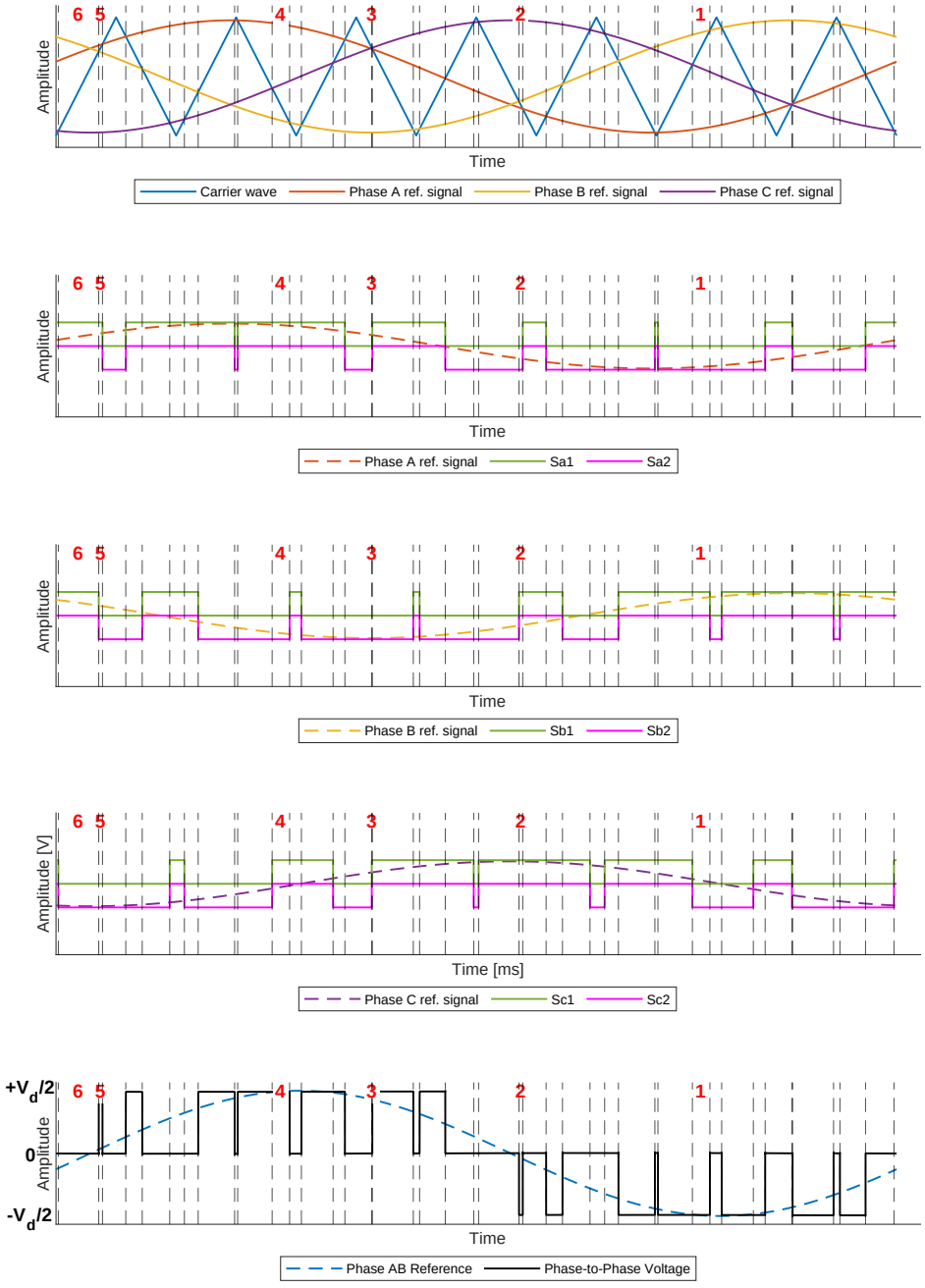


Figure 2.2: Carrier signal, reference signals, and phase-to-phase voltages in a two-level SPWM inverter. Gate signals for lower switches are inverted for visualization. The amplitude of the phase-to-phase voltage is within $\pm\frac{V_d}{2}$. The red numbers, 1-6, mark the operation intervals of the inverter explained in Table 2.1. Here, the operation intervals are shown only once for better clarity.

As can be seen in the Figure 2.2, the duty cycle of the switches depends on the relative position of the reference and carrier signals. When the reference signal is higher than the carrier, the corresponding upper switch stays on, which increases the average output voltage and current. This method effectively generates a sinusoidal output waveform with controllable amplitude and frequency.

The switching frequency of the inverter is defined by the frequency of the triangular/carrier signal. Two important parameters that define the behavior of SPWM are the modulation factors:

- **Frequency Modulation factor** (m_f): This is the ratio of the carrier wave frequency (f_c) to the reference signal frequency (f_n):

$$m_f = \frac{f_c}{f_n} \tag{2.1}$$

- **Amplitude Modulation factor** (m_a): This is the ratio of the peak amplitude of the reference voltage ($\hat{V}_r$) to the peak amplitude of the carrier wave ($\hat{V}_c$):

$$m_a = \frac{\hat{V}_r}{\hat{V}_c} \tag{2.2}$$

According to [15] the amplitude modulation factor m_a directly affects the peak value of the fundamental component of the output phase voltage, which can be expressed as:

$$(\hat{V}_{a0})_1 = m_a \frac{V_d}{2}, \quad \text{for } m_a \leq 1 \tag{2.3}$$

The frequency modulation factor m_f affects the distribution of harmonic components in the output voltage. These harmonics typically appear as sidebands around integer multiples of the switching frequency. The general expression for the harmonic frequency is:

$$f_h = (jm_f \pm k)f_n \tag{2.4}$$

that is, the order of harmonics h is the k_{th} sideband of j times the frequency modulation factor m_f. Selecting m_f as an odd integer ensures that the output waveform has odd ($f(-t) = -f(t)$) and half-wave symmetry ($f(t) = -f(t - \frac{1}{2}T_n)$) which helps to eliminate even harmonics and improves waveform quality [16].

In any inverter-EM configuration, achieving the desired operation involves a sequence of processes within both the inverter and the EM. These processes include user input, control logic, and DC to AC conversion, among others. A general operation flow for such a system is illustrated in Figure 2.3, which shows the signal path from torque and speed commands to the generation of gate signals used to control the EM. The desired torque, speed, and feedback signals from the EM are sent to the controller, which produces a reference voltage to the modulator. The modulator then regulates the switching states of the inverter by controlling the on/off states of the switches, as outlined in Table 2.1 to generate a phase voltage over the load that, on average, over one switching period, is equal to the current reference voltage.

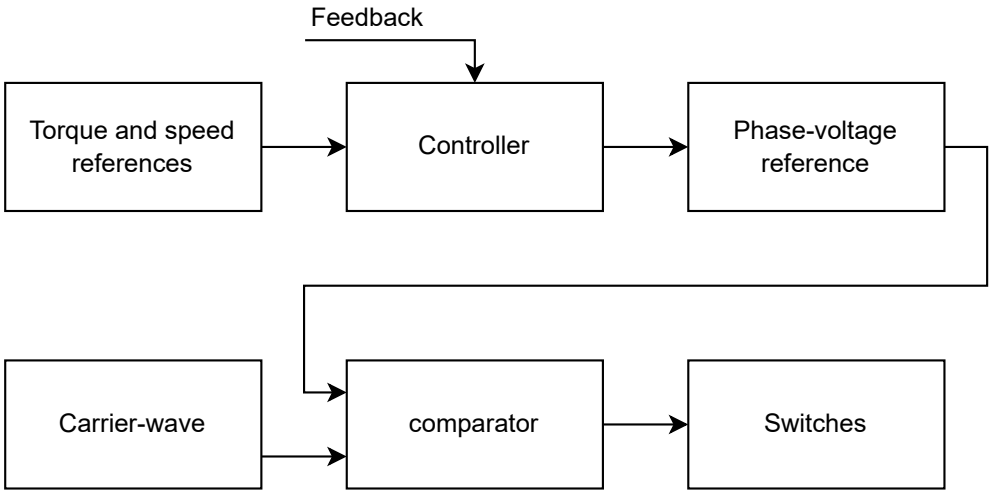


Figure 2.3: Signal flowchart of an inverter where the switching states of the switches are determined given a reference via modulators.

2.2 3L3P NPDC voltage source inverter

The 3L3P NPDC, illustrated in Figure 2.4, divides the input DC bus voltage into multiple levels using a series of capacitors C_1 and C_2. These capacitors establish intermediate voltage points, allowing the inverter to generate three output voltage levels. The clamping diodes are incorporated to ensure that each semiconductor switch withstands only half of the total DC bus voltage, which is also equal to the voltage of a single capacitor. These diodes help distribute voltage evenly across the switches, preventing excessive voltage stress and ensuring proper operation [17]. Each switch in the 3L3P NPDC inverter is paralleled with a freewheeling diode (intrinsic) to protect against reverse current caused by inductive loads [13, 14], in the same way as for the 2L3P inverter.

In this configuration, Point o, which is the same as the ground potential, serves as the reference point for the inverter's phase voltage output. By switching between different voltage levels, the inverter produces a multi-level AC waveform, reducing harmonic distortion [17]. Even in the three-level inverter, the SPWM modulation technique can turn the switches on/off to get the desired output voltages described in Table 2.2. However, to control the different switches of each phase, two carrier signals are used (compared to only one carrier signal in a 2L3P inverter). The reference signals of each respective phase are compared to these carrier signals. Since multiple carrier signals are used, this technique is called Multi-carrier Sinusoidal Pulse Width Modulation (MCSPWM) [18]. Figure 2.4 illustrates how the carrier and reference signals are used to generate gate voltages.

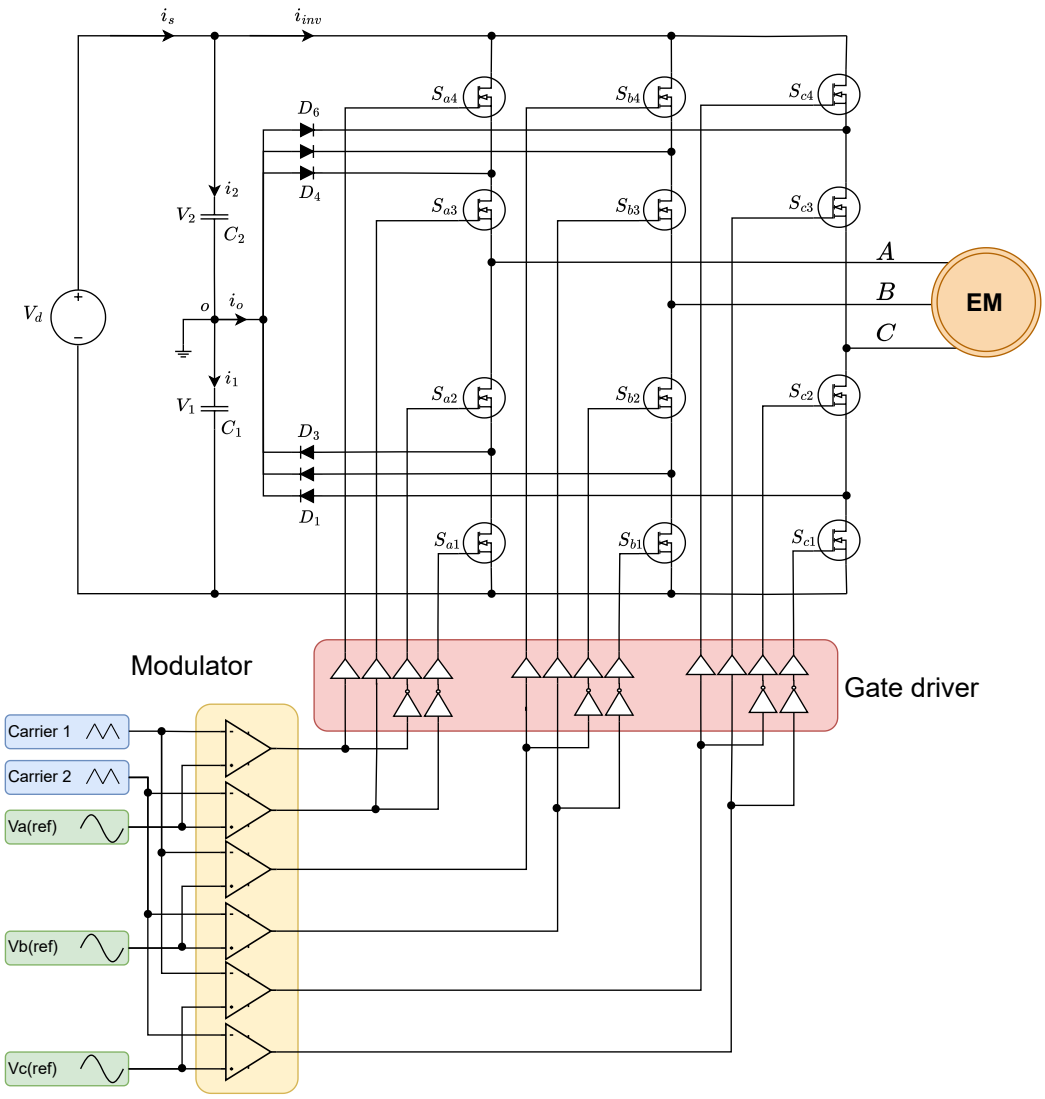


Figure 2.4: Schematic of voltage source 3L3P NPDCMI. The yellow region highlights the comparators/modulator, and the red region highlights the gate drive circuitry.

As in the two-level inverter, the modulator generates gating signals or operation intervals for the switches to achieve the desired output voltage. These signals are detailed in Table 2.2. In this configuration, the phase-to-neutral point o has three distinct voltage levels: $+\frac{V_d}{2}$, 0, and $-\frac{V_d}{2}$. The operation intervals are shown for phases A and B; however, phase C follows the same sequence with a phase delay.

Table 2.2: Operation states of phase switches for a 3L3P VSI using PDSPWM technique. In this inverter, the phase voltage has three states $(-\frac{V_d}{2}, 0, +\frac{V_d}{2})$ and the phase-to-phase voltage has three states $(-V_d, -\frac{V_d}{2}, 0, +\frac{V_d}{2}, +V_d)$. In the switching states, (1) indicates the switch is turned on.

Operation Interval	**Switching States**								v_{ao} Level	v_{bo} Level	v_{ab} Level
	S_{a4}	S_{a3}	S_{a2}	S_{a1}	S_{b4}	S_{b3}	S_{b2}	S_{b1}			
1	0	0	1	1	1	1	0	0	$-V_d/2$	$+V_d/2$	$-V_d$
2	0	0	1	1	0	1	1	0	$-V_d/2$	0	$-V_d/2$
3	1	1	0	0	1	1	0	0	$+V_d/2$	$+V_d/2$	0
4	0	0	1	1	0	0	1	1	$-V_d/2$	$-V_d/2$	0
5	0	1	1	0	0	0	1	1	0	$-V_d/2$	$+V_d/2$
6	1	1	0	0	0	0	1	1	$+V_d/2$	$-V_d/2$	$+V_d$

In this thesis, the three-level inverter is controlled using a variation of the MCSPWM technique known as PD-SPWM. In PD-SPWM, the two carrier signals are in phase and aligned vertically. Figure 2.5 shows the operation intervals and corresponding signals described in Table 2.2.

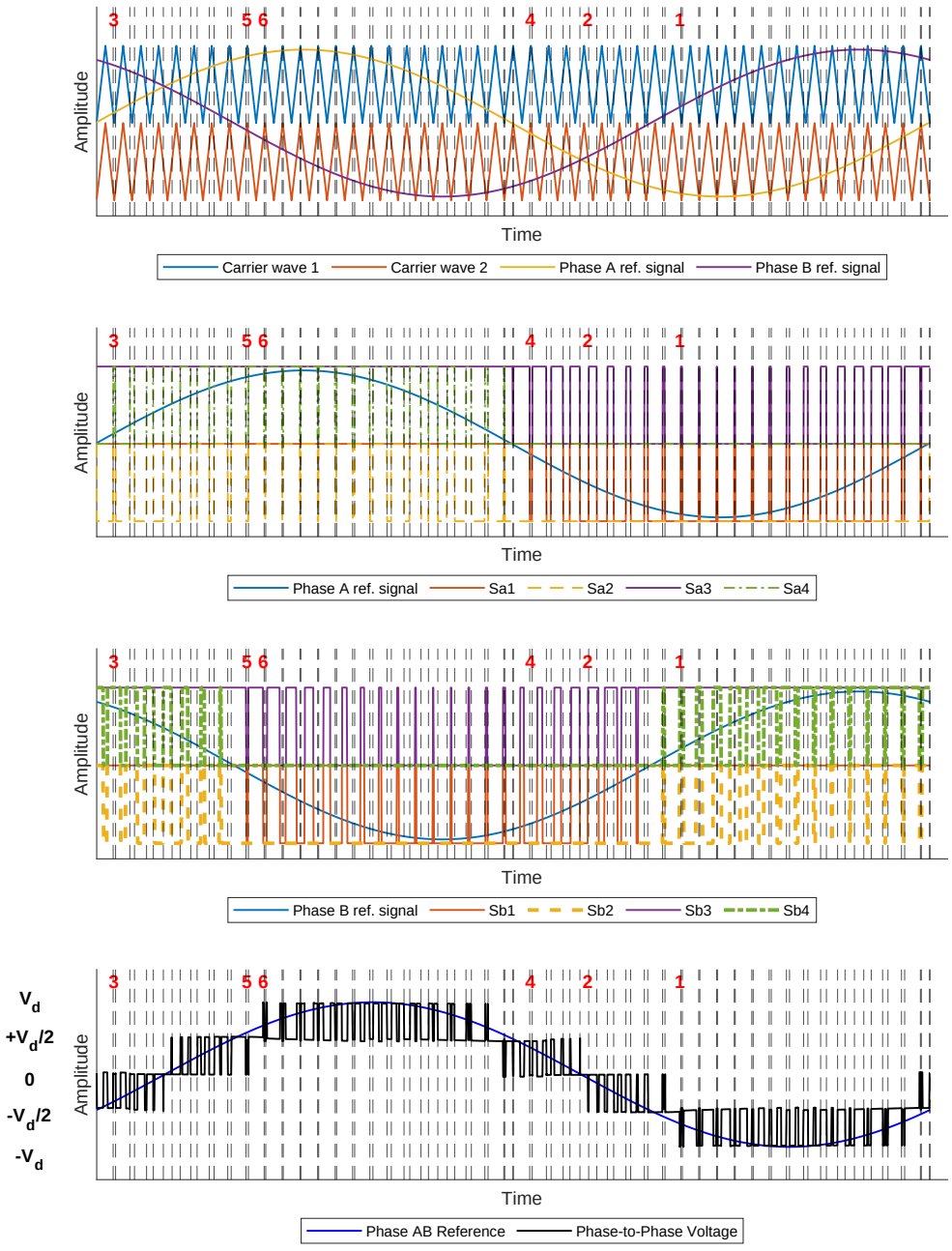


Figure 2.5: 3L3P voltage source NPDC inverter's carrier and reference single for phases A and B, including the gate signals of switches in the mentioned phases. Furthermore, the operation intervals as in Table 2.2 are highlighted. The gate signals for switches S_{x1} and S_{x2} are inverted for better visualization

Here, the operation of the inverter is similar to that of the two-level counterpart when it comes to generating the gating signals. Same as in the two-level case, the speed and torque references are used to generate the reference signal for the modulator illustrated in Figure 2.3. Another difference apart from what has been mentioned before is that every switch stays on for at least half of a fundamental period, leading to fewer switching actions per fundamental period per switch, which leads to lower switching losses.

2.3 DC-link capacitors

The DC-link capacitors in an inverter act as energy storage components, helping to maintain a stable DC-link voltage. Their primary function, when placed between the power module and the rest of the circuit, is to minimize voltage overshoot caused by abrupt current changes through parasitic inductances present in the circuit. An insufficient DC-link capacitance can lead to inverter instability, potentially resulting in over-voltage or under-voltage faults [19]. Figure 2.6 illustrates a simplified equivalent model of an inverter under load, which is used to estimate the required DC-link capacitance. The system is modeled under load conditions, as any under-voltage and/or over-voltage faults occurs during operation.

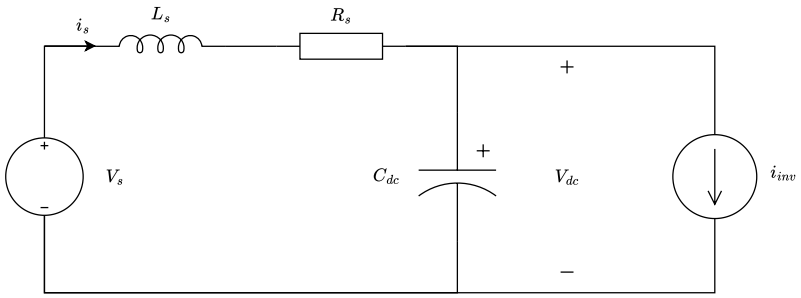


Figure 2.6: Equivalent model of the power source and inverter under load.

In Figure 2.6, the series resistance and inductance (R_s and L_s) are included to describe the properties of the conductor between the inverter and the power source. The system's dynamic equations are expressed as:

$$L_s \frac{di_s}{dt} = V_s - R_s i_s - V_{dc} \tag{2.5}$$

$$C_{dc} \frac{dV_{dc}}{dt} = i_s - i_{inv} \tag{2.6}$$

Here, V_s, i_s, L_s, and R_s denote the source voltage, current, inductance, and resistance. The current i_{inv} denotes the inverter current, and C_{dc} is the DC-link capacitors. If the load power, P_l, is constant, the inverter current can be expressed as[20]:

$$i_{inv} = \frac{P_l}{V_{dc}} = \frac{P_l}{V_{dc0} + \tilde{V}_{dc}} \tag{2.7}$$

where V_{dc0} is the mean DC-link voltage, and $\tilde{V}_{dc}$ represents its variation. If $\tilde{V}_{dc}$ is relatively small compared to V_{dc0}, a *Taylor* series expansion can be used to linearize the inverter current:

$$i_{inv} = \frac{P_l}{V_{dc0} + \tilde{V}_{dc}} \approx \frac{P_l}{V_{dc0}} - \frac{P_l}{V_{dc0}^2}\tilde{V}_{dc} \tag{2.8}$$

Applying *Laplace* transformation to (2.5), (2.6), and (2.8), the characteristic equation in the *Laplace* domain is obtained as:

$$s^2 + (\frac{R_s}{L_s} - \frac{P_l}{C_{dc}V_{dc0}^2})s + (\frac{V_{dc0}^2 - R_sP_l}{L_sC_{dc}V_{dc0}^2}) = 0 \tag{2.9}$$

Applying *Routh-Hurwitz* Stability Criterion for second-order systems:

$$(\frac{R_s}{L_s} - \frac{P_l}{C_{dc}V_{dc0}^2}) > 0 \tag{2.10}$$

$$(\frac{V_{dc0}^2 - R_sP_l}{L_sC_{dc}V_{dc0}^2}) > 0 \tag{2.11}$$

This results in the minimum required DC-link capacitance and voltage conditions:

$$C_{dc} > \frac{P_lL_s}{V_{dc0}^2R_s} \tag{2.12}$$

$$V_{dc0}^2 > R_sP_l \tag{2.13}$$

Equation (2.12) provides the minimum value of DC-link capacitance required to ensure system stability. However, this equation does not take into account EMI, which is another important consideration in inverter design. In the simulation setup used for this thesis, both the source inductance (L_s) and resistance (R_s) are assumed to be zero. As a result, the system is inherently stable, without any input capacitors. However, input capacitors are included in the design for several reasons. First, they help in reducing EMI by filtering out high-frequency noise. Second, in the case of the 3L3P inverter, these capacitors are also used to divide the DC-link voltage evenly. To ensure a fair comparison between the two-level and three-level inverter topologies, the same input capacitors are used in both systems. This approach eliminates the influence of the capacitor configuration on the performance comparison.

As shown in Figure 2.11, the input filter occupies a significant portion of the PCB area in the existing two-level inverter design. These filters typically consist of a combination of bulk electrolytic capacitors, which provide high energy storage capacity, and ceramic capacitors, which have low ESR. Together, they stabilize the DC-link voltage and reduce high-frequency noise caused by rapid switching transients. This type of EMI mitigation strategy is discussed in the next section.

2.3.1 Effects of Decoupling Capacitors on EMI

According to [21], the DC-link capacitors (bulk and decoupling) not only reduce the voltage stress across the switches but can also be used to mitigate EMI, or,

in some cases, even increase it. For a high-frequency differential-mode noise peak, if the combined impedance of the DC-link capacitor and busbar parasitic inductance exceeds that of the decoupling capacitor, most of the noise current will flow through the decoupling capacitor, thereby reducing high-frequency EMI. However, adding capacitors may introduce resonances among the decoupling capacitors, DC-link capacitors, and the busbar's parasitic inductance. As the capacitance of the decoupling network increases, the low-frequency noise peak is diminished but shifts to even lower frequencies. Thus, although decoupling capacitors reduce voltage stress, they can lead to increased EMI at lower frequencies.

The optimal values for input capacitors to achieve maximum EMI suppression depend on several physical parameters of the circuit: the inverter's switching frequency, layout parasitic inductances and capacitances, and the series resistance of traces and components. These factors are highly layout-dependent and require detailed physical modelling. Since exhaustive simulation for precise capacitor sizing exceeds the scope of this thesis, the DC-link (including decoupling) capacitors are held constant across all inverter topologies, and EMI performance is compared relative to the reference two-level Si-based inverter.

2.3.2 DC-Link Capacitor Sizing for the NPDI 3L3P

Additional considerations must be taken into account when selecting the DC-link capacitor size for a 3L3P NPDC inverter. One of the most critical aspects is maintaining voltage balance across the two series-connected DC-link capacitors. This section focuses on analyzing the sizing of DC-link capacitors.
In Figure 2.4, the currents flowing through the top and bottom capacitors are separated into their AC and DC components:

$$i_2 = i_{2(AC)} + i_{2(DC)} \tag{2.14}$$
$$i_1 = i_{1(AC)} + i_{1(DC)} \tag{2.15}$$

Since the power supply provides only a DC voltage, any AC voltage component observed across capacitors C_1 and C_2 arises due to the AC portions of the currents i_1 and i_2. These AC voltage components can be expressed as:

$$V_{2(AC)} = \frac{1}{C_2} \int i_{2(AC)}\, dt \tag{2.16}$$
$$V_{1(AC)} = \frac{1}{C_1} \int i_{1(AC)}\, dt \tag{2.17}$$

The total DC-link voltage, as well as the voltage deviation at the neutral point (often referred to as the Neutral Point Potential, or NPP), can be defined from Figure 2.4 as:

$$V_d = V_{1(DC)} + V_{1(AC)} + V_{2(DC)} + V_{2(AC)} \tag{2.18}$$
$$\Delta V_{NPP} = \Delta V_1 = \max[V_{1(AC)}] - \min[V_{1(AC)}] \tag{2.19}$$

From this, it is evident that selecting suitable capacitor values for the DC-link requires careful evaluation of two main factors:

1. The ripple current that flows through each capacitor, often evaluated as the RMS of the current.
2. The voltage fluctuation at the neutral point

Minimizing the NPP is important to prevent overstressing or damaging the power semiconductor switches. At the same time, the ripple current must be kept within the capacitor's rated current limits to avoid overheating and premature aging. Therefore, both parameters plus the sizing of decoupling capacitors must be considered during the design process to ensure the reliable and efficient operation of the 3L3P NPDC inverter [22].

2.3.3 Voltage Balancing in NPDC Multi-Level Inverters

A drawback of NPDC multi-level inverters is the voltage imbalance of the series-connected DC-link capacitor. The DC-link capacitors charge and discharge dependent on the switching states. At certain switching states, the charge/discharge contribute to a non-zero displacement current, which results in unequal DC-link capacitor voltage. This reduces the quality of the output line current, which in turn increase the THD. Additionally, the voltage imbalance could induce breakdown of the components due to varying dv/dt [23, 24]. Multiple techniques can address this issue, such as:

- Neutral Point Voltage Balancing using equivalent states
- Neutral Point Voltage Balancing with feedback voltage control
- Neutral Point Voltage Balancing with feedback DC-current sign detection
- Utilizing a different PWM method such as virtual space vector pulse width modulation (VSVPWM)

Evaluation of optimized neutral point voltage balancing is outside the scope of this thesis, as such the voltage imbalance is regarded as an affect of the NPDC MLI.

2.4 Common Mode Voltage and Current

In a balanced, three-phase sinusoidal power supply, the neutral point normally has zero potential. However, when using a PWM-switched power supply with a DC input, maintaining a neutral point voltage of zero is not possible [6, 25]. Although the fundamental frequency of each phase remains equal, the use of only two or three output voltage levels results in a non-zero neutral point, leading to the induction of CMV. Some of the issues that arise from the CMV are the CMCs. These currents can, for instance, flow through the bearings and cause bearing failures or generate EMI. Several factors contribute to this issue, including: the motor size, the grounding method of the motor shaft and frame, the parasitic capacitances between phase windings and the rotor, the type of cable and shielding, as well as the dv/dt rate of the AC drive power stage [26, 27].

The bearing currents are generated when there is a voltage difference between the rotor and the phase windings. The amplitude of this current depends on the ampli-

tude and frequency of the voltage difference [28]. Other factors that can generate CMC are the stray capacitances. Capacitance forms when two conductors are separated by an insulator, and the value of this capacitance can then be calculated as [29]:

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \tag{2.20}$$

here, $\epsilon_0 \approx 8.854 \times 10^{-12}\ F \cdot m^{-1}$ is the electric constant (permittivity of vacuum), ϵ_r is the relative permittivity of the material between the capacitor plates, A is the area of the capacitor plates and d is the distance between the capacitor plates.

In PCBs, stray capacitances result from design factors such as PCB layout and the layers stack of the PCB, including what materials are used in those layers. Some examples of these stray capacitances include: capacitance between DC-link traces to ground and chassis, between source and drain to ground and chassis, etc. These capacitances are typically relatively small, meaning they have high impedance at low frequencies and block low-frequency stray currents. However, at higher frequencies, they provide a low-impedance path, allowing high-frequency currents to flow. Since the focus of this thesis is the inverter design, only the CMCs caused by the inverters are studied.

2.4.1 CMC in the two-level inverter

A simple schematic of the stray capacitances for a single phase in a 2L3P inverter is presented in Figure 2.7

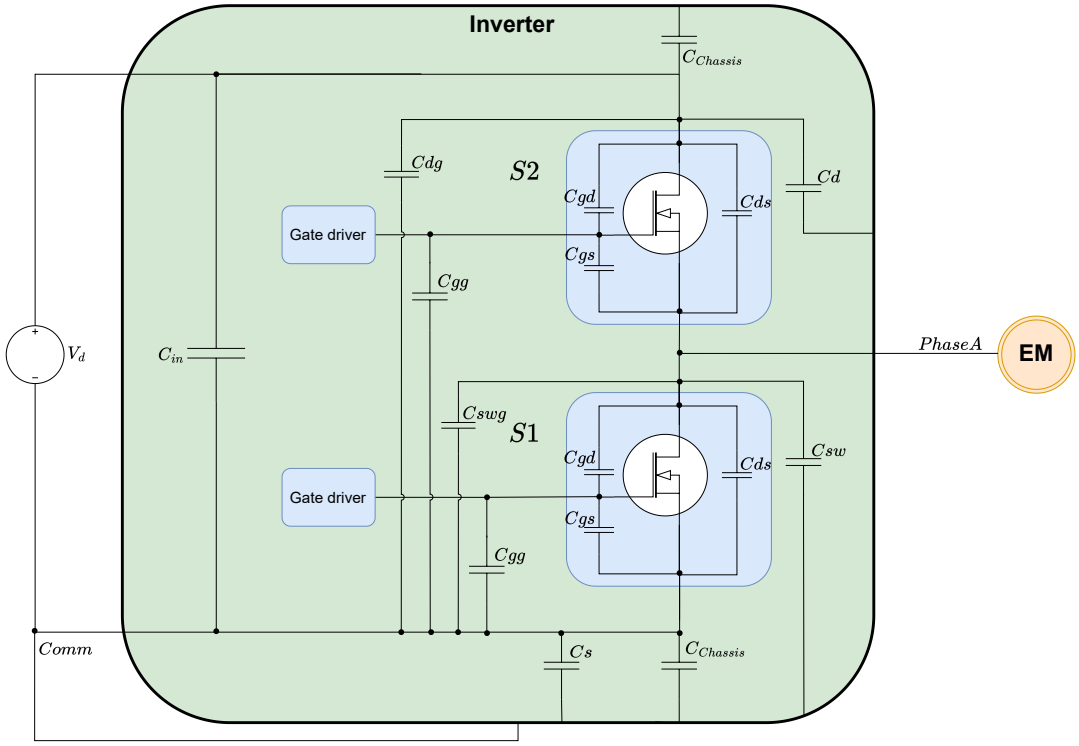


Figure 2.7: Stray capacitances in a two-level inverter. The capacitances are defined as follows: C_{gg} (gate-to-ground), C_{dg} (drain-to-ground), C_d (drain-to-chassis), C_{sw} (switch-node-to-chassis), C_s (source-to-chassis), and C_{in} (input bulk capacitors).

The internal parasitic capacitances of the switches (highlighted in blue) are included in the simulation model. However, the external parasitic capacitances vary depending on the design of the PCB. Using (2.20) and studying the PCB of the existing inverter, the values for the parasitic capacitances in Figure 2.7 can be estimated according to the following:

Gate to ground parasitic capacitance (C_{gg})

These capacitances are created when the traces and pads of the gate driver signal are placed on top of the ground (GND) plane in the PCB. In Figure 2.8, the pads that contribute to the external gate parasitic capacitance are highlighted in red.

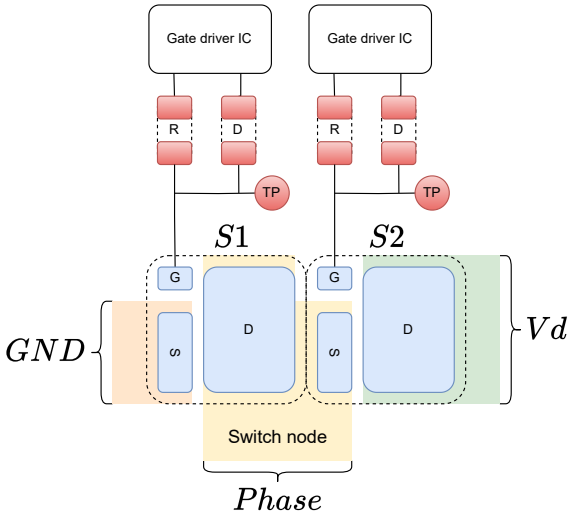


Figure 2.8: Switch node copper-pour and components that contribute to the gate parasitic capacitances (highlighted in red). R denotes the gate resistor, and D denotes the gate diode.

As described in (2.20), the value of the capacitance depends on three factors (A, d, ϵ_r). In this case, the highlighted areas were measured on the PCB which added to a total of 4mm^2, the distance d between the pads and the GND plane is 70μm and the type of material used for this separation is *Prepreg*. Figure 2.9 illustrates the different layers of the PCB in relation to the heat sink and the thermal grease.

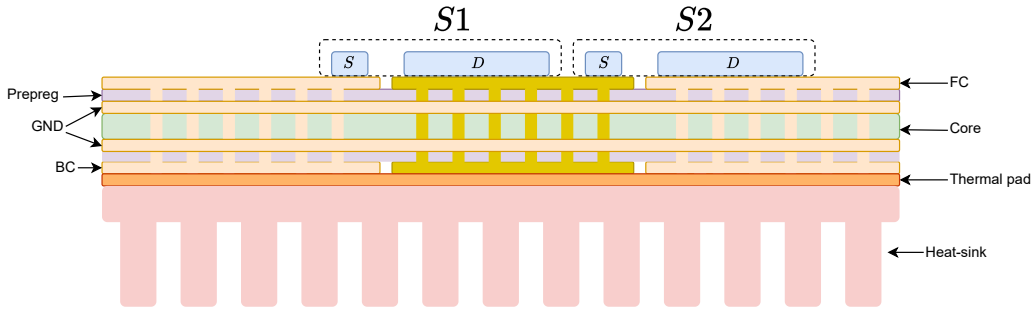


Figure 2.9: Different layers of the PCB and its relation to the thermal grease and heat-sink. The dark-yellow area indicates the switch node at which the phase output is connected. The vertical traces are the vias used to transfer heat from the top layer to the bottom layer. The thermal pad in this case also acts as insulator between the PCB and heat-sink

The *Prepreg* used in this PCB is of type 370HR, with a relative permeability of approximately 4.5. Inserting these values in (2.20), the external gate-to-ground parasitic capacitance can be calculated; this gives $C_{gg} \approx 2.27$ pF.

Switch node to chassis parasitic capacitance (C_{sw})

The switch node parasitic capacitance is significant, as this is due to the large copper-pour area needed to cool the switch. The switches are mounted on the upper layer of the PCB and the heat is transferred to bottom copper pour highlighted in yellow in Figure 2.8, through vias. The heat is then transferred from the PCB to the heat-sink via the thermal pad. This area (yellow region) in the existing PCB is around 2 cm^2. The thermal pad used in this case is of type *Electrolube HTC35SL* with a relative permeability of approximately 4.2, and the distance between the heat-sink and PCB is assumed to be 0.1 mm. Inserting the mentioned values in (2.20), the switch node parasitic capacitance becomes: $C_{sw} = 74.37$ pF.

Drain to ground parasitic capacitance (C_{dg})

Copper pours are used to keep the inductance and resistance of the traces delivering power to the drain of the upper switches low; however, this copper pour results in capacitances between this node and the ground. This capacitance, even though called parasitic, can be utilized as a high-frequency input filter. Since this capacitor is connected in parallel with the DC-link capacitors, it can be counted as an input filter rather than a parasitic element. Since this capacitance does not contribute to CMV, it is omitted.

Switch node to ground parasitic capacitance (C_{swg})

This node exists on both the Front Copper (FC) and Back Copper (BC) of the PCB, thus creating two parallel capacitors. This copper pour has an area of around 2 cm^2 and the *Prepreg* is acting as the insulator material. The value of this capacitance is calculated; $C_{sw} = 227.67$ pF.

Drain to chassis parasitic capacitance (C_d)

The area of this copper pour can also be extracted from the exiting PCB to circa 500 mm^2. The thermal grease is the insulator between the drain node and the heat sink and the resulting parasitic capacitance using (2.20) can be calculated; $C_d = 186$ pF.

Source to chassis parasitic capacitance (C_s)

The BC of the PCB is approximately 80% GND which is the same as the lower node of the input voltage. In this case, this area is around 100×700 mm and it creates a parasitic capacitance with the heat-sink beneath it. The insulator for this capacitor too is also the thermal grease with a relative permeability of roughly 4.2. Inserting these values in (2.20) the resulting capacitance becomes; $C_s = 2.6$ nF.

If not properly managed, these CMCs can flow back into the inverter through the ground (GND) node, potentially causing EMI issues. To confine these currents within the inverter, capacitors $C_{chassis}$ are added between the positive and negative inputs of the inverter and the chassis, providing a return path for the CMCs (see Figure 2.7). As a rule of thumb, the capacitance of C_{chassis} is typically 10 to 50 times greater than the total parasitic capacitances that contribute to CMCs in the system [1]. This is to insure that all the CMCs can return via the C_{chassis} back to the inverter.

2.4.2 CMC in the three-Level Inverter

The parasitic capacitances of a three-level inverter are illustrated in Figure 2.10.

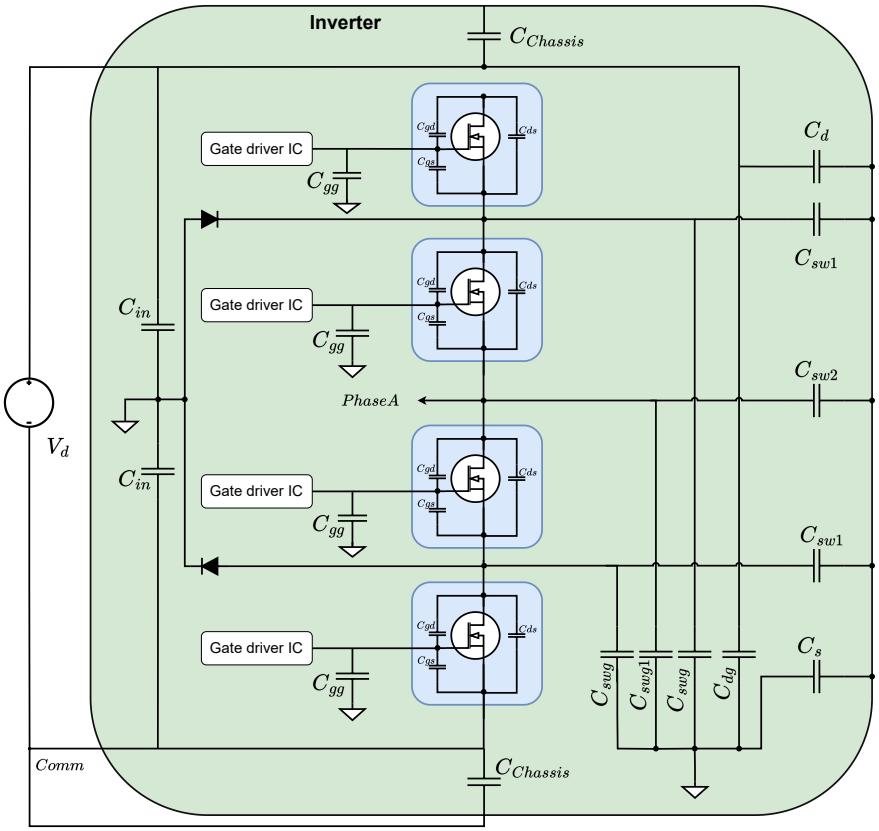


Figure 2.10: Stray capacitances in a three-level inverter. The capacitances are defined as follows: C_{gg} (gate-to-ground), C_{dg} (drain-to-ground), C_d (drain-to-chassis), C_{sw} (switch-node-to-chassis), C_{swg} (switch-node-to-ground), C_s (source-to-chassis), and C_{in} (input bulk capacitors).

Since there is no physical reference PCB available for this inverter at *Aros*, the parasitic capacitances are estimated based on assumptions. These assumptions are derived from extrapolating the dimensions of the existing two-level inverter PCB and the additional components, such as switches, diodes, and gate drive circuitry. While

[1] These values are used at *Aros Electronics AB* in some of the existing inverters

some errors may be present in these estimations, they are necessary for modeling of the inverter. Figure 2.11 illustrates the relative sizes of key component blocks in the existing two-level inverter. Notably, the gate drive circuitry and switches occupy a relatively small area, whereas the input filter takes up nearly one-third of the PCB.

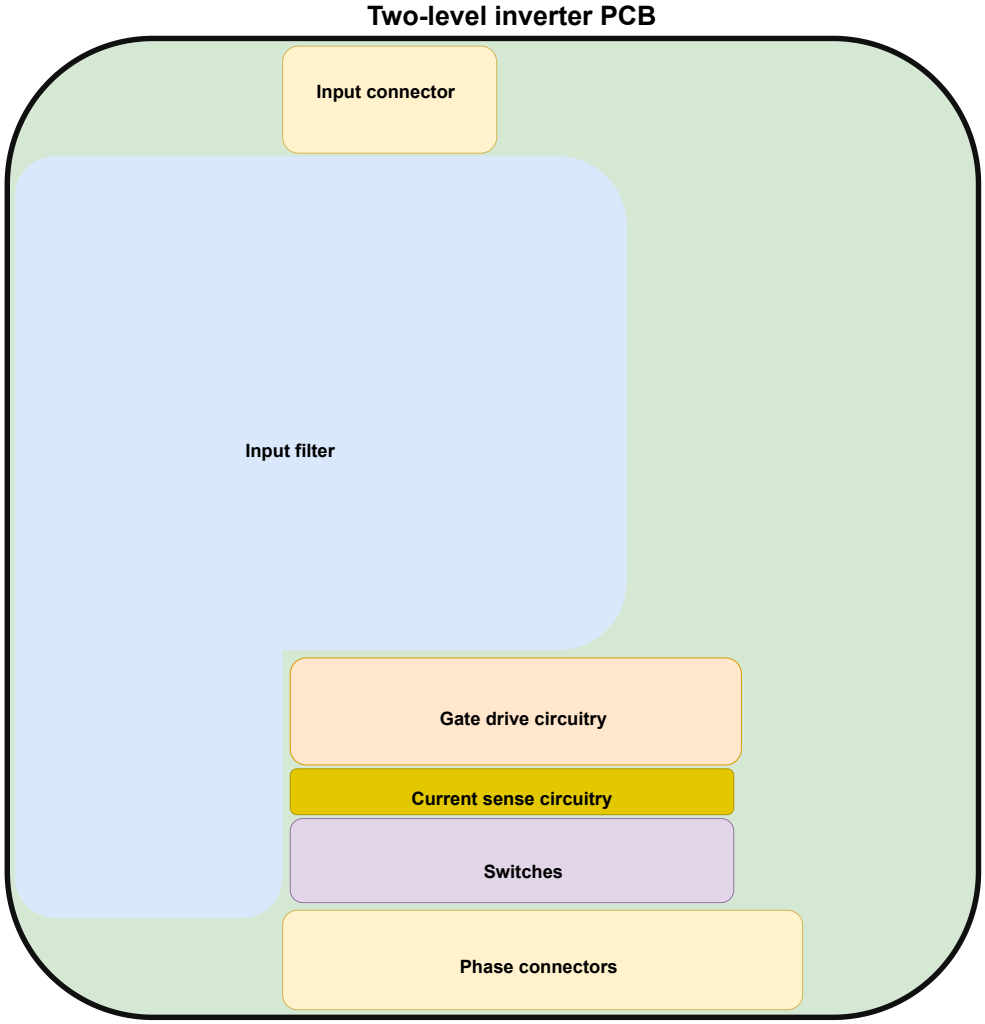


Figure 2.11: Relative sizes of component blocks in the existing two-level inverter.

Since MLIs generally exhibit lower EMI compared to two-level inverters [30], it is assumed that a reduction in the input filter area can offset the additional area required for extra switches and gate drive circuitry. Additionally, it is assumed that the traces that deliver power from the input connector to the switches remain unchanged, or the change has insignificant effects on the parasitic capacitance. Figure 2.12 illustrates the various nodes and components contributing to the parasitic capacitances.

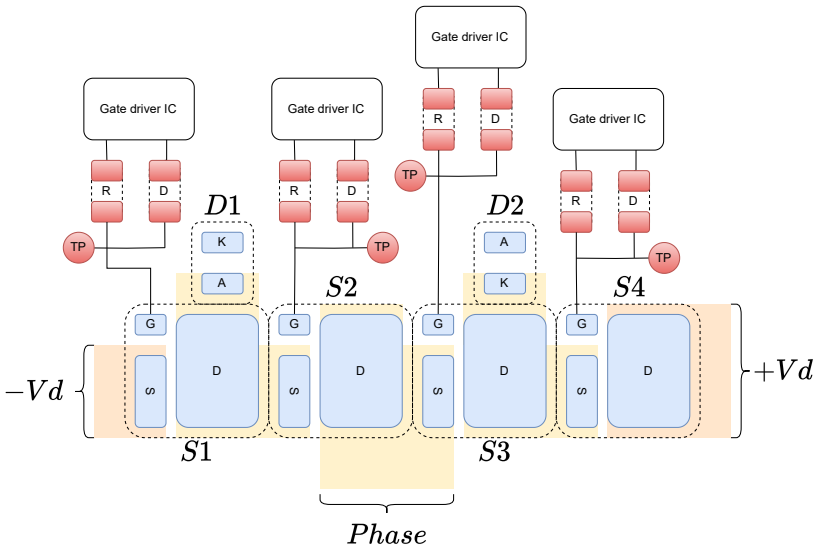


Figure 2.12: Switch layout of a single phase in a three-level inverter, highlighting the nodes and components contributing to parasitic capacitances.

Based on the assumptions outlined above, the stray capacitances of the three-level inverter can be estimated as follows:

Gate to ground parasitic capacitance C_{gg}

Since the same gate driver, diode, and resistors are used in the gate drive circuit, the gate to ground capacitance remains unchanged compared to the two-level inverter.

Switch-node to chassis parasitic capacitances C_{sw1} and C_{sw2}

The node C_{sw1} is connected to high-power diodes requiring cooling, necessitating a larger copper area for heat dissipation. Similarly, C_{sw2} is linked to the phase connector, which also requires a larger copper area, as shown in Figure 2.12. In a two-level inverter, the total power loss of the switches is divided by six, whereas in a three-level inverter, it is divided by twelve. Since the copper area used for cooling depends on switch power loss, halving the per-switch power loss should reduce the required cooling area by half. Consequently, the total cooling area remains the same between the two- and three-level inverters. Even though in theory the same copper area can be kept, in reality, there might be some layout challenges that might increase the total area. Examining the two-level inverter, the phase connectors occupy roughly half of the switch node's copper area. Although this portion contributes to switch cooling, it also introduces stray capacitances.

Switch-node to ground parasitic capacitances C_{swg} and C_{swg1}

The copper areas for these nodes are assumed to be approximately 60% and 80% of the switch node in the two-level case, respectively. C_{swg2} can be neglected, as this

capacitor is in parallel with the input capacitors.

Drain to chassis parasitic capacitance C_d

The EMI characteristics of the three-level inverter allow for a reduction in the input capacitor size. The primary contributors to the stray capacitance between the upper switch's drain and the chassis are the drain itself and the DC-link capacitors, which connect to the BC through vias. Consequently, this stray capacitance decreases in the three-level inverter. The extent of the reduction depends on EMI suppression and PCB design. Here, a 30% reduction is assumed, leading to an estimated value of $C_d \approx 130$ pF.

Based on the above information, the estimated stray capacitances for different nodes are presented in Table 2.3.

Table 2.3: Estimated stray capacitances of a three-level inverter based on the two-level inverter using the same switches

Two-level	**C [pF]**	**Three-level**	**C [pF]**	**Ratio**
C_{gg}	2.27	C_{gg}	2.27	1
C_{sw}	74.37	C_{sw1}	44.62	0.6
C_{sw}	74.37	C_{sw2}	59.49	0.8
C_{swg}	227.7	C_{swg1}	182.16	0.8
C_{swg}	227.7	C_{swg}	136.62	0.6
C_d	186	C_d	186	1
C_{sw1}	74.4	C_{swg}	44.64	0.6
C_{sw1}	74.4	C_{sw2}	59.52	0.8
C_s	2600	C_s	2600	1

2.5 Modeling the Electrical Machine

As previously mentioned, the inverter does not incorporate any control system, and thus, the Electrical Machine (EM) is modeled in steady-state operation. To accurately represent the behavior of the EM, certain parameters must be determined. This section explains the modeling of the EM, which is assumed as a Permanent Magnet Synchronous Machine. Figure 2.13 illustrates the equivalent circuit of a PMSM in the dq-coordinate system [31].

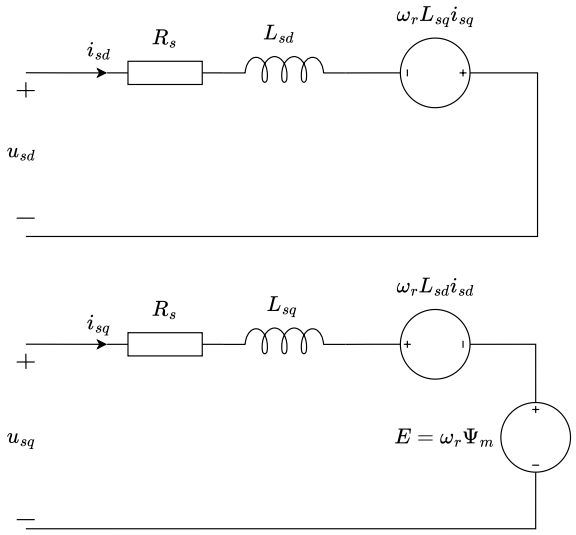


Figure 2.13: The equivalent circuit of the EM in the dq-coordinate system.

The stator voltages in the dq-coordinate system are given by [32]:

$$u_{sd} = R_s i_{sd} + L_{sd}\frac{di_{sd}}{dt} - \omega_r L_{sq} i_{sq} \tag{2.21}$$

$$u_{sq} = R_s i_{sq} + L_{sq}\frac{di_{sq}}{dt} + \omega_r L_{sd} i_{sd} + \omega_r \psi_m \tag{2.22}$$

The electrical torque produced by the machine is given by:

$$T_e = \frac{3n_p}{2}(\Psi_m i_{sq} + (L_{sd} - L_{sq}) i_{sd} i_{sq}) \tag{2.23}$$

The equations describing the mechanical part of the machine are as follows:

$$\frac{d\theta_r}{dt} = \omega_r \tag{2.24}$$

$$\frac{J}{n_p}\frac{d\omega_r}{dt} = T_e - T_L \tag{2.25}$$

$$\omega_r = 2\pi f_n \tag{2.26}$$

$$\Omega_r = \frac{\omega_r}{n_p} \tag{2.27}$$

The descriptions of the parameters in (2.21) to (2.27) are as the following;

Parameter	Description
R_s	stator phase resistance
i_{sd}, L_{sd}	d-axis current and inductance
i_{sq}, L_{sq}	q-axis current and inductance
ω_r	rotor speed
J	Inertia of EM
T_e	EM produced torque
T_L	Load (load torque)
Ω_r	mechanical speed of the rotor
f_n	electrical frequency/speed
Ψ_m	magnet flux linkage
n_p	number of pole pairs

In steady-state operation, the *dq*-axis currents are constant, meaning their derivatives are zero. Consequently, the stator voltage equations simplify to:

$$u_{sd} = R_s i_{sd} - \omega_r L_{sq} i_{sq} \tag{2.28}$$

$$u_{sq} = R_s i_{sq} + \omega_r L_{sd} i_{sd} + \omega_r \psi_m \tag{2.29}$$

The stator voltage in vector format is given by:

$$\overline{u}_s^{dq} = R_s \bar{i}_s + j\omega_r L_s \bar{i}_s + j\omega_r \Psi_m \tag{2.30}$$

$$\tag{2.31}$$

where:

$$\overline{u}_s^{dq} = u_{sd} + j u_{sq} \tag{2.32}$$

$$\bar{i}_s^{dq} = i_{sd} + j i_{sq} \tag{2.33}$$

For a non-salient machine, the phase inductance can be calculated as:

$$L_s = L_d = L_q \tag{2.34}$$

According to the torque equation in (2.23), the reluctance torque is zero since the inductances of the d and q-axes are equal. Thus:

$$i_{sd} = 0 \tag{2.35}$$

From (2.23) and (2.35), the q-axis current can be calculated as:

$$i_{sq} = \frac{2T_e}{3n_p \Psi_m} \tag{2.36}$$

In this case, the required output torque and speed are requested, and the corresponding currents are calculated based on that.

The back-emf of the PMSM, as in Figure 2.13, is given by:

$$\overline{e}^{dq} = j\omega_r \Psi_m \tag{2.37}$$

Given the output torque and speed, the output power can be calculated as:

$$P_e = T_e \Omega_r \tag{2.38}$$

Given the presence of losses within the PMSM, the input power exceeds the output power. Consequently, for an amplitude-invariant transformation, the output power, which represents the sum of the input power and resistive losses, is calculated as:

$$P_s = \frac{3}{2} R_s |\bar{i}_s^{dq}|^2 + P_e \tag{2.39}$$

The reactive input power is calculated as:

$$Q_s = \frac{3}{2} (\omega_r L_s |\bar{i}_s^{dq}|^2 + \omega_r \Psi_m i_{sd}) \tag{2.40}$$

Given the active and reactive powers, the power factor, which is the angle between the stator voltage and current, can be calculated as follows:

$$cos(\varphi) = \frac{P_s}{\sqrt{P_s^2 + Q_s^2}} \tag{2.41}$$

Writing (2.30), (2.33) and (2.37) in polar format results in:

$$\bar{u}_s^{dq} = \hat{U}_s \angle \theta_u \tag{2.42}$$

$$\bar{i}_s^{dq} = \hat{I}_s \angle \theta_i = \hat{I}_s \angle 90^\circ \tag{2.43}$$

$$\bar{e}^{dq} = \hat{E} \angle \theta_e = \hat{E} \angle 90^\circ \tag{2.44}$$

Transforming the equations (2.42)-(2.44) in $\alpha\beta$-coordinate system using *Park* transformation, results in:

$$\bar{u}_s^{\alpha\beta} = \hat{U}_s e^{j(\theta_r + \theta_u)} \tag{2.45}$$

$$\bar{i}_s^{\alpha\beta} = \hat{I}_s e^{j(\theta_r + \theta_i)} = \hat{I}_s e^{j(\theta_r + 90^\circ)} \tag{2.46}$$

$$\bar{e}^{\alpha\beta} = \hat{E} e^{j(\theta_r + \theta_e)} = \hat{E} e^{j(\theta_r + 90^\circ)} \tag{2.47}$$

The $\alpha\beta$ to *abc* is given by *Clarke* transformation as:

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix}$$

The resulting three-phase *abc-phase* voltages are given by:

$$u_a = \hat{U}_s cos(\omega_r t + \theta_u) \tag{2.48}$$

$$u_b = \hat{U}_s cos(\omega_r t + \theta_u + 120^\circ) \tag{2.49}$$

$$u_c = \hat{U}_s cos(\omega_r t + \theta_u + 240^\circ) \tag{2.50}$$

In steady state, $\theta_r = \omega_r t$. Similarly, the three-phase stator currents, i_a, i_b, i_c, can be calculated using (2.46), and the three-phase back-EMFs, e_a, e_b, e_c, can be calculated using (2.47). This completes the electrical machine modeling, where the non-salient PMSM is modeled as phase-resistances, R_s, in series with phase inductances L_s, including the back-EMF voltage sources. Since the DC-link voltage is fixed, the amplitude of the phase voltage is varied using the amplitude modulation factor m_f as:

$$\hat{U}_{an} = \frac{m_a V_d}{2} \tag{2.51}$$

thus, the maximum amplitude of the phase voltage can be half the DC-link voltage.

2.6 Electromagnetic interference

Since the current drawn from the power supply is not constant, the switching actions of the inverter introduce EMI on both the input and output sides. A Line Impedance Stabilization Network (LISN) is employed to measure the conducted EMI between the unit under test and the power supply. The LISN provides a low-impedance path for high-frequency noise, enabling accurate measurement of high-frequency ripples.

In this thesis, the DC-link and decoupling capacitors are kept identical across all inverter topologies to ensure a consistent input capacitance from the source's perspective. This standardization isolates the effects of the inverter topology and switching frequency on EMI generation. Each inverter's EMI performance is compared relative to a baseline two-level silicon-based inverter operating at 16 kHz. Figure 2.14 shows the LISN configuration used for these simulations. EMI is evaluated as the voltage drop across a 1 kΩ resistor in parallel with a 50 Ω probe resistance.

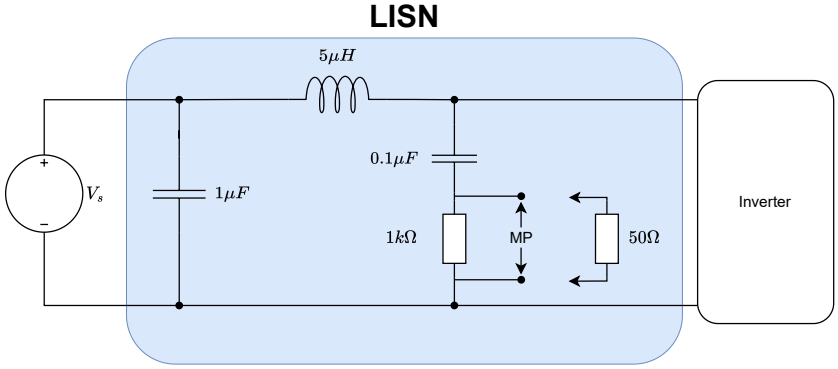


Figure 2.14: Line Impedance Stabilization Network

Since the inverters are intended for industrial applications, conducted EMI was evaluated using a LISN setup in accordance with the CISPR 32 standard [33], with the Class A Quasi-Peak limit values used as the reference, which provide an appropriate benchmark for evaluating emissions in this context. It is important to note, however, that the results are derived from *LTspice* simulations in which not all parasitic

elements and filtering components, such as PCB parasitics and decoupling capacitors, are fully modeled. Consequently, the simulated EMI levels may vary compared to the actual conducted emissions, and in practice, the system may not exceed the Class A limits.

2.7 Harmonic components

In an inverter configuration with non-linear loads, i.e, semiconductor switches, the generated AC current will differ from the fundamental sinusoidal wave pattern in the form of distortions. Such distortions cause non-ideal effects on motor applications, increasing power dissipation on load and EMI in motor windings [34]. One of these distortion metrics is THD, which is studied in the following section.

2.7.1 Total Harmonic Distortion

Harmonic distortion in the stator current leads to torque ripple and induces vibrations in the EM. Each harmonic current component interacts with the machine's magnetic field, resulting in pulsating torques that lead to elevated vibrations and acoustic noise [35]. As described in (2.23), any distortion or ripple in the current directly contributes to torque ripple. Therefore, minimizing current distortion is of significant importance in motor drive applications.

One of the commonly used metrics to quantify current distortion, specifically the distortion in the phase current, is the Total Harmonic Distortion (THD). It is defined as:

$$\%\mathrm{THD}_{I_{phs}} = 100 \cdot \sqrt{\frac{\sum_{h=2}^{\infty} I_h^2}{I_n^2}} \tag{2.52}$$

where I_n is the amplitude of the fundamental component of the phase current (I_{phs}), and I_h represents the amplitude of the h^{th} harmonic component (for $h \geq 2$). The summation excludes the fundamental and accounts for all higher-order harmonics present in the current waveform.

2.7.2 Losses due to current distortion

Aside from the torque ripple induced by harmonic distortion in the stator current, these harmonics also contribute to increased power losses in the EM. The presence of harmonic currents increases both copper losses and stray load losses in the stator. As discussed in [35], the combined stator copper and stray load losses due to harmonic distortion can be estimated using the following expression:

$$P_{\text{cuss}} = 3\left(I_{\text{phs}}^2 + I_h^2\right)\left(R_s + R_{\text{sssl}}\right) \tag{2.53}$$

$$R_{\text{sssl}} = \frac{\left(\omega_r L_{\ell s}\right)^2 R_s}{R_s^2 + \left(\omega_r L_{\ell s}\right)^2} \tag{2.54}$$

where:

R_{sssl} : Frequency-dependent stray load loss resistance per phase
L_{ls} : Phase leakage inductance

The stray load losses arise from hysteresis and eddy currents induced by the leakage flux in the stator. In this analysis, the machine's leakage phase inductance $L_{\ell s}$ is assumed to be approximately 10% of the total phase inductance. Additional harmonic-related losses, including iron-core, P_{ich}, and mechanical (friction and windage) losses, P_{fwh}, are estimated by:

$$P_{\text{ich}} = 3\frac{V_g^2}{h^2 R_{\text{ich}}} \tag{2.55}$$

$$P_{\text{fwh}} = 3\frac{V_g^2}{h^2 R_{\text{fwh}}} \tag{2.56}$$

where:

R_{ich} : Iron core resistance
R_{fwh} : Mechanical resistance of the electrical machine
V_g : Airgap voltage

Since this thesis does not include a detailed EM model required to accurately characterize iron-core and mechanical losses, the analysis focuses solely on losses due to harmonic currents interacting with the machine's leakage inductance [2].

[2]More reasoning about this is done in the discussion; in Section 6.1

3
Power electronic switches

This section qualitatively evaluates the properties and theoretically derives the dissipated power of two different power FETs, Si-HEXFET and GaN-HEMT, for both a two-level inverter and a three-level NDCP inverter with Schottky barrier diodes. Losses are derived based on the properties and composition of the semiconductor switches at constant room temperature.

3.1 Qualitative evaluation

The following sections describe the functionality and differences between the two power FETs and how the properties of the devices can be qualitatively determined based on a portion of the normalized properties of Si- and GaN semiconductor material from [36], which are presented in Table 3.1.

Table 3.1: Normalized Si- and GaN-semiconductor characteristics for power electronic devices [36].

Material	**Si**	**GaN**
Bandgap energy (eV)	1.1	3.49
Mobility (cm^2/Vs)	1500	2000
Peak electron velocity ($\times 10^7 cm/s$)	1	2.7
Thermal conductivity ($W/(cm-K)$)	1.5	>1.7
Dielectric constant (ϵ_r)	11.8	9

In the table, mobility (μ) represents the distance a charge carrier is moved dependent on an E-field in a given material; peak electron velocity ($V_{ds,sat}$) is the electron velocity when applied V_{ds} reaches current saturation; Thermal conductivity determines the heat dissipated in relation to temperature and the dielectric constant (ϵ_r) the relative permittivity of the material [37].

3.1.1 Silicon-based Transistor

The n-type enhancement mode Si-HEXFET functions similarly to a Si-MOSFET, where the gate voltage (V_{gs}) exceeds the threshold voltage (V_{th}) and generates an electric field between gate and source, which induces an electron inversion layer that inverts the p-type channel. Allowing the electron majority charge carriers to travel from source-to-drain, causing a current (I_d) from drain-to-source when a positive drain-to-source voltage V_{ds} is applied [38]. However, the structure is different as

shown in Figure 3.1. Notably, there are multiple sources and channels; the electrons flow laterally from the source through the channel, then vertically to drain.

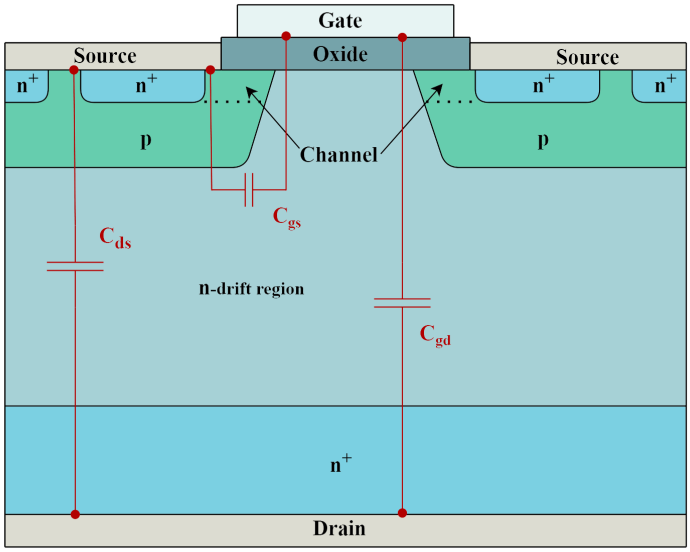


Figure 3.1: The general vertical structure of a N-channel Si-HEXFET with parasitic capacitances C_{gs}, C_{ds} and C_{gd} between the device layers

The Si-HEXFET is a power MOSFET with a double-diffused MOS structure, fabricated with large channel widths with a repetitive pattern of hexagonal source cells that operate in parallel. This, in conjunction with a vertical structure, ensures that the I_d current handling capabilities and V_{ds} blocking voltage are sufficiently high for the intended use-case [39]. A body-diode is attached to the semiconductor package, which allows for reverse conduction as $0 > V_{ds} > V_f$ where V_f represents the diode forward voltage.

3.1.2 Wide bandgap Transistor

WBG semiconductor materials have a wide energy separation between the valence and conduction bands compared to materials such as Si. As such, charge carriers in WBG transistors are more resistant to random thermal excitation, reducing the effects of lattice scattering and allowing for increased mobility, peak electron drift velocity, and breakdown voltage. A simplified cross-channel structure of a general GaN-HEMT is illustrated in Figure 3.2.

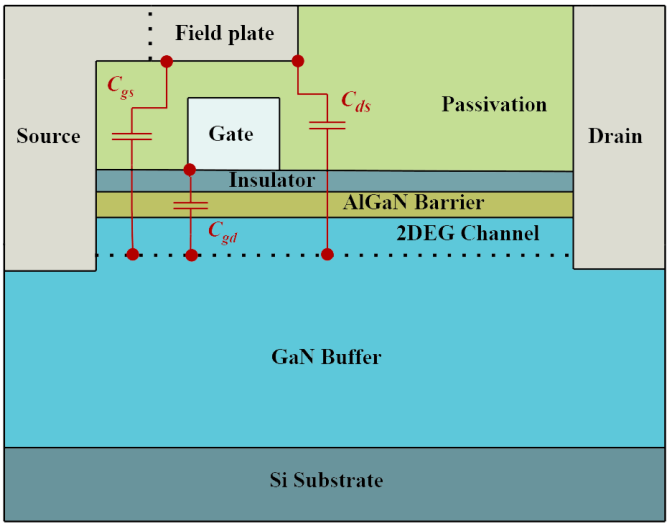


Figure 3.2: The general lateral structure of a GaN-HEMT with parasitic capacitances C_{gs}, C_{ds} and C_{gd} between the device layers

The GaN-HEMT utilizes GaN as the WBG material in its lateral structure, which consists of a Two-dimensional Electron Gas (2DEG) channel from drain-to-source. The 2DEG channel is formed due to an electric field between positive and negative polarization charges at the top and bottom of the Aluminum Gallium Nitride (AlGaN) barrier layer, which results in electron charge carriers to flow into the GaN layer, which creates the 2DEG [40]. Applied V_{gs} influences the conductivity of the 2DEG and subsequently allows conduction through the drain-to-source. If negative V_{ds}, i.e, a positive source-to-drain voltage (V_{sd}), is applied, the polarity is switched, which allows for reverse conduction through the channel. The condition for reverse conduction is expressed as

$$V_{gd} = V_{gs} + V_{sd} > V_{th} \tag{3.1}$$

$$V_{sd} \approx (V_{th} - V_{gs}) + I_{sd}R_{ds} \tag{3.2}$$

where V_{th} represents the threshold voltage inherent to the transistor, I_{sd} the source-to-drain current and R_{ds} the drain-to-source resistance [41, 42]. In (3.2), the motor back EMF supplies I_{sd} that increases V_{sd} which fulfills the reverse conduction condition. During turn-off for a GaN HEMT, a negative V_{gs} can be applied to increase the safety margin of a false turn-on [43].

3.1.3 Cut-off frequency

The maximum switching frequency of a hetero-junction FET, biased on saturation drain-current ($I_{d,sat}$), is determined, in part, by the Figure of merit (FOM) called the cut-off frequency (f_{cutoff}). Defined as the frequency at which the input current

is equal to the ideal output current, which is derived from an equivalent ideal small-signal circuit diagram from [38], and presented as:

$$f_{cutoff} = \frac{g_m}{2\pi C_g} \approx \frac{g_m}{2\pi(C_{ox}WL)} \tag{3.3}$$

The width and length of the channel between source and drain in the FET is represented by W,L, respectively. The gate capacitance per cm^2 (C_g) is determined by the intrinsic oxide capacitance (C_{ox}), representing the capacitance between the gate-metal plate and the substrate of the device where the channel is formed. Assuming an ideal constant electron mobility, the trans-conductance (g_m) is defined as the partial differential drain current over the corresponding gate voltage as:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{WC_{ox}\mu_n}{L}(V_{gs} - V_{th}) \tag{3.4}$$

where μ_n represents the electron mobility cm^2 per volt-second. Combining (3.3) and (3.4), f_{cutoff} is expressed as:

$$f_{cutoff} = \frac{\mu_n(V_{gs} - V_{th})}{2\pi L^2} \tag{3.5}$$

Non-ideal electron mobility is proportional to ionized impurity doping concentration and temperature, due to the effects of lattice- and ionized impurity scattering [44]. The electric field generated at the gate leads to surface scattering, which affects electron mobility depending on oxide thickness. Scattering effects induce velocity saturation at high electric fields, which causes a constant cut-off frequency [37]. For the purpose of qualitative evaluation, μ_n is regarded as constant. As such, f_{cut} is used to evaluate the inherent delay of the device. An increased f_{cut} results in increased maximum switching frequency as the output current of the device reaches the supplied input current at a faster rate.

3.1.4 Gate charge

The total gate charge (Q_g) is relevant to evaluate switching frequency of the device, as Q_g is dependent on the relative permittivity, i.e the dielectric constant (ϵ_r) and thickness (t_{ox}) of the material layer(s) between the gate field plate and channel layer [38]. The permittivity determines the material capacitance used to determine the gate charge as described by:

$$Q_g \propto C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_r\epsilon_o}{t_{ox}} \tag{3.6}$$

where ϵ_{ox} is the permittivity between the gate field plate and the channel layer whilst ϵ_o is the permittivity of vacuum. As can be observed in Figures 3.1 and 3.2, the GaN-HEMT device does not have an oxide layer between the gate and 2DEG, instead it is occupied by the insulator- and AlGaN barrier layer. To simplify the qualitative analysis, the combined layer capacitances are collectively refereed to as C_{ox} for GaN HEMTs. The material used to create the oxide layer in Si-MOSFETs is SiO_2 through passivation, whilst the AlGaN barrier layer is an alloy. The insulator

layer in GaN HEMTs is typically created using Si_3N_4 film, but can use a wide range of materials that function as insulators. Therefore, to accurately derived Q_g, an in-depth analysis is required which is dependent on; device layer dimensions; doping concentrations and dynamic analysis of the voltage applied at the gate. Which is beyond the scope of this thesis. Therefore, the ϵ_r of the substrate material used to form the oxide and barrier layer in Si-MOSFETs and GaN-HEMTs are, respectively, assessed.

The Q_g can be used to approximate the transient response time t_g of the gate expressed as:

$$C_g \approx \frac{Q_g}{V_{gs}} \tag{3.7}$$

$$t_g = R_g C_g \tag{3.8}$$

where C_g and R_g represents the approximate gate capacitance and total gate drive resistance respectively.

3.1.5 Drain-to-source resistance

During an on-state in the ohmic region, i.e the FET device functions as a linear resistor inversely proportional to g_m as $V_{gs} > V_{th}$ and $V_{ds} < V_{gs} - V_{th}$, the created channel conducts with I_{ds} through the internal drain-to-source pn resistance ($R_{ds(on)}$). As such, dissipated power during conduction is proportional to $R_{ds(on)}$, which is represented by:

$$R_{ds(on)} = R_s + R_{ch} + R_d \tag{3.9}$$

where R_s and R_d are the source- and drain contact resistances, which are inversely proportional to μ_n. The resistance in the channel R_{ch} is characterized in [39] by:

$$R_{ch} = \frac{L}{W \mu_n C_{ox} (V_{gs} - V_{th})} \tag{3.10}$$

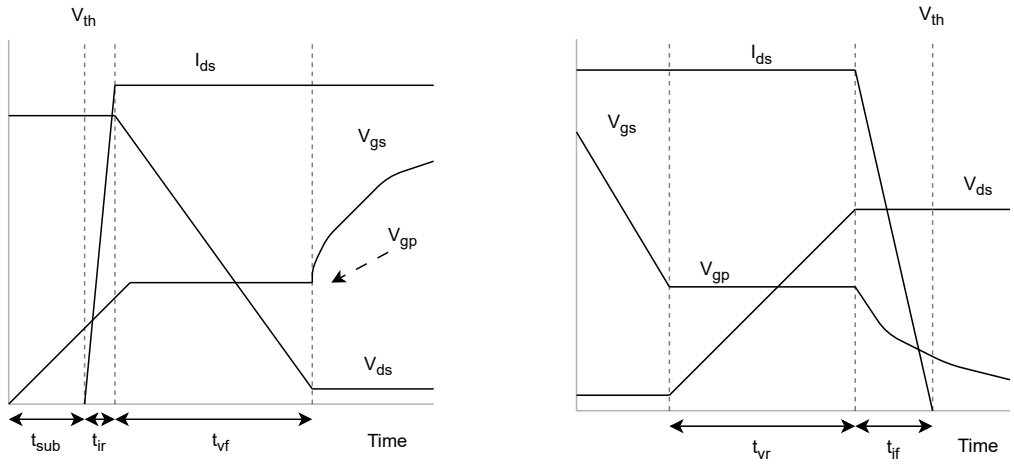
3.2 Semiconductor losses

The following sections theoretically express all semiconductor losses for the presented inverter configurations. The analysis regards any switch for any phase legs for both 2L3P and 3L3P in Figures 2.2 and 2.4. However, as the analysis depends on current and voltages levels dictated by the reference and carrier waves shown in Figures 2.2 and 2.5, the loss analysis presented requires a model of the current and voltage values to determine the total loss for each device. The power loss regards the accumulated energy over a single fundamental line current period equal to f_n.

3.2.1 Transient switch losses

The power dissipated during turn-on and turn-off states in FET devices are determined by estimating the hard-switched transient switch time of drain-to-source

current/voltage overlap. Figures 3.3a and 3.3b illustrates an ideal qualitative turn-on/off transient of applied gate-to-source voltage V_{gs} and I_{ds}/V_{ds} characteristics.



(a) **(b)**

Figure 3.3: Qualitative characteristics of I_{ds},V_{ds} and V_{gs} for a power FET device during hard turn-on (a) and hard turn-off (b)

Current rise time (t_{ir}) and voltage fall time (t_{vf}) for I_{ds}/V_{ds} in Figure 3.3a are derived from [45] and determined by:

$$t_{ir} = R_{g,on} C_{iss}\ ln(\frac{V_{gs} - V_{th}}{V_{gs} - V_{gp}}) \tag{3.11}$$

$$t_{vf} = R_{g,on} \frac{Q_{gd}}{V_{ds}} \frac{V_{ds}}{(V_{gs} - V_{gp})} \tag{3.12}$$

where; $R_{g,on}$ represents the effective sum of internal gate resistances in the FET with the external circuit gate resistance for turn-on, C_{iss} represents the sum of C_{gd} and C_{gs} input capacitances at the gate, Q_{gd} represents gate-drain charge at V_{ds} peak, V_{th} threshold voltage and V_{gp} *Miller* plateau voltage.

The process of a hard turn-on in Figure 3.3a begins as $V_{gs} > V_{th}$, the I_d increases as the channel is formed and begins to conduct at $t > t_{sub}$. During this t_{ir}, the C_{gs} and C_{gd} capacitances are charged, but as $C_{gs} > C_{gd}$ most of the drive current applied at the gate flows into C_{gs}, causing an increase in V_{gs}. During this time, the device is kept in reverse conduction either through its body-diode or 2DEG. When the channel is partially formed and reverse conduction ends, the device is in the saturation region. The I_d peaks at the beginning of t_{vf} whilst V_{ds} decreases and the majority of the drive current charges C_{gd}. Whilst C_{gd} charges, V_{gs} is kept constant at V_{gp} due to the linear relationship of g_m and the *Miller* effect, up until V_{ds} reaches its minimum at the end of t_{vf}. At this point the device enters the ohmic region, all

drive current charges C_{gs} while V_{gs} increases until it has achieved its applied gate voltage value [46]. Total energy loss during a switch turn-on is then expressed as:

$$E_{ton}(V_{ds}(t), I_d(t)) = \frac{1}{2} V_{ds}(t) I_d(t)(t_{ir} + t_{vf}) \tag{3.13}$$

Similarly, ideal turn-off transient is presented in Figure 3.3b where voltage rise time and current fall time are represented by t_{vr} t_{ir} respectively.

$$t_{vr} = R_{g,off} \times \frac{Q_{gd}}{V_{ds}} \times \frac{V_{ds}}{V_{gp}} \tag{3.14}$$

$$t_{if} = R_{g,off} C_{iss} \times ln \frac{V_{gp}}{V_{th}} \tag{3.15}$$

The transient turn-off in Figure 3.3b begins by V_{gs} dropping up until it reaches V_{gp}, the device exists the ohmic region and enters saturation as $V_{gs} > V_{th}$ and $V_{ds} > V_{gs} - V_{th}$. The C_{gd} discharges whilst V_{ds} increases during t_{vr}. At t_{if} the I_d falls by the discharging C_{gs} until $V_{gs} < V_{th}$ where the device enters the cut-off region and is turned off. The energy loss during switch turn-off is then expressed as:

$$E_{toff}(V_{ds}(t), I_d(t)) = \frac{1}{2} V_{ds}(t) I_d(t) \times (t_{vr} + t_{ir}) \tag{3.16}$$

Dissipated power for switch turn-on/off transients is calculated by:

$$P_{trans} = f_n \sum_{i=1}^{N_{on}} (E_{ton,i}(V_{ds}(t), I_d(t)) + f_n \sum_{j=1}^{N_{off}} E_{toff,j}(V_{ds}(t), I_d(t)) \tag{3.17}$$

where N_{on} and N_{off} are the total switch-on and switch-off actions, which expresses the accumulated switch energy over a line current period with the frequency equal to the reference frequency f_n. The $E_{ton,i}(t)$ and $E_{toff,j}(t)$ are separately determined for each switching action in regards to $I_{ds}(t)$ and $V_{ds}(t)$ determined by the reference and carrier waveforms in Figures 2.2 and 2.5. As an example, transistors $(S_{a2}, S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3})$ in Figure 2.4 will conduct for half a period without switching. The other half of the period the transistor switches whilst the serially connected DC-link transistor is in cut-off, providing current only from the anti-parallel diode and thereby a low transient switch loss.

3.2.2 Parasitic losses

Parasitic capacitances will affect the I_{ds} transient characteristics during voltage commutation. During transistor turn-on, the voltage across gate-to-drain C_{gd} and drain-to-source C_{ds} capacitors[1] drop whilst the stored charge is discharged from the capacitors through the channel in the form of a displacement current I_{oss}. This results to a momentary I_{ds} overshoot which contributes to instantaneous power during switching. This effect is expressed as:

$$P_{oss} = f_n \int_0^{V_d} V_{ds} C_{oss(V_{ds})} dV_{ds} \tag{3.18}$$

[1]Capacitors refer to equivalent parasitic capacitance intrinsic to the component

where V_d is the supplied DC voltage across the transistor and C_{oss} is the parasitic capacitances at the drain output, which are non-linearly dependent on V_{ds}. As the drain capacitor is charged during turn-off and subsequently discharged during turn-on, the P_{oss} is regarded as an internal switching loss for the two-level inverter configuration. The I_{oss} will instead discharge through the channel, as an inductive load blocks the conduction path to the motor. However, for the NPDC 3-level configurations, the C_{oss} leads to displacement currents conducting through other components, leading to an external loss. In Figure 3.4a, the I_{oss} from S_2 conducts through the serially connected transistor's S_1 open channel, resulting in P_{oss} switching loss during turn-on. Similarly, as S_2 remains closed and S_1 is turned-on in Figure 3.4b, the I_{oss} is discharged as the inductive ripple current conducts through the body-diode/channel.

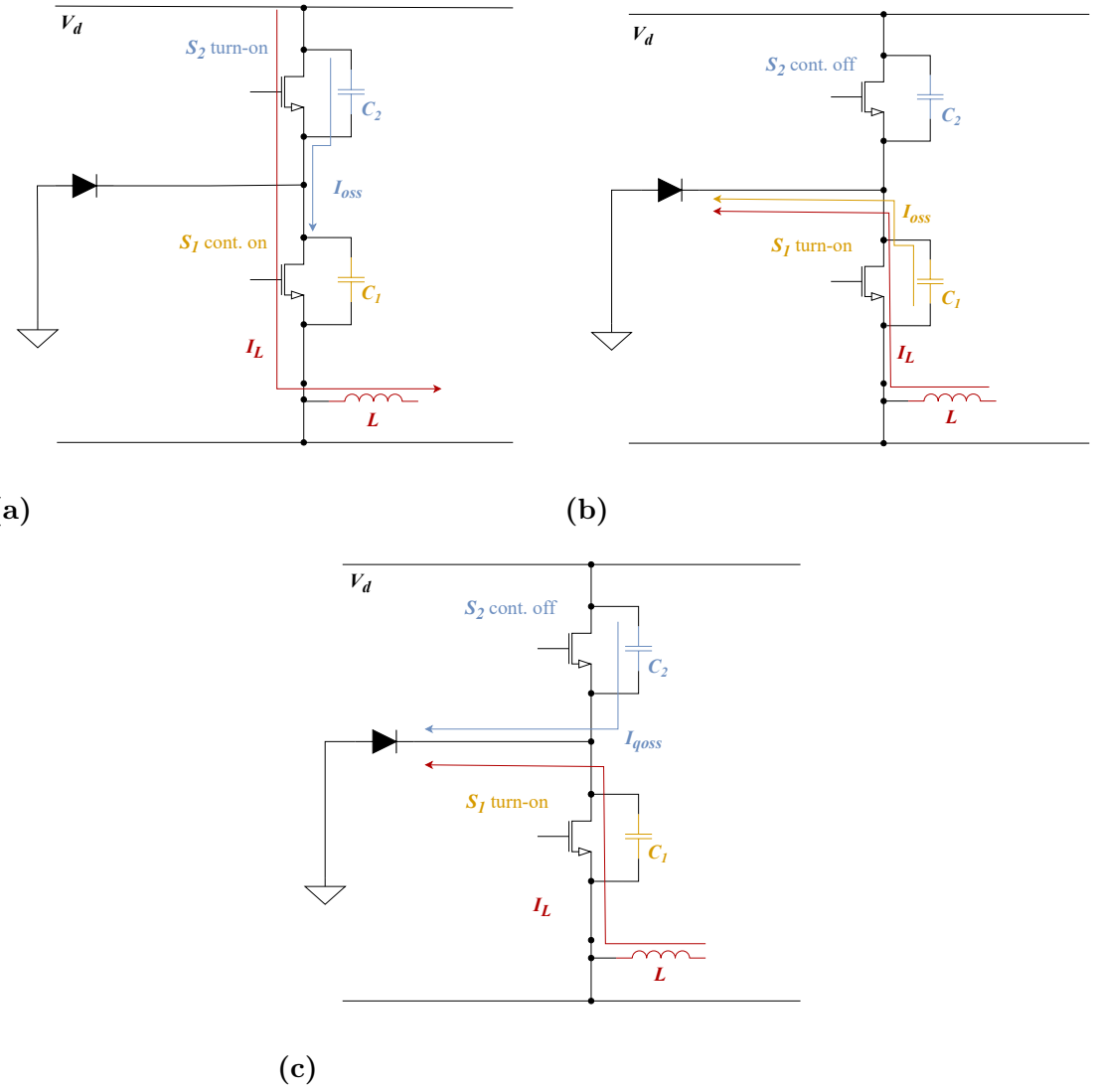


Figure 3.4: Example of displacement currents from parasitic capacitance, resulting in external losses due to serially connected transistors attached to an inductive load. (a) Represents a top switch S_2 turn-on with continuously turned-on bottom switch S_1. (b) shows a S_1 turn-on with S_2 being continuously off in regards to the bottom-switch. (c) a S_1 turn-on with S_2 being continuously turned-off in regards to the top-switch.

In addition to I_{oss}, in Figure 3.4c when S_2 is off during S_1 turn-on, the upper drain capacitor C_2 is charged by the bus current, which causes the device's charging current I_{qoss} to also conduct through the diode during S_1 turn-on. This results in a P_{qoss} loss to occur, characterized as a sudden displacement current bump and is expressed in [47]:

$$P_{qoss} = f_n \int_0^{V_d} (V_{dc} - V_{ds}) C_{oss(V_{ds})} dV_{ds} \tag{3.19}$$

where V_d is the bus voltage applied over the switch [47–49].

3.2.3 Subthreshold conduction

In Figure 3.3a, I_d is assumed to be zero in time period t_{sub} as $V_{gs} \leq V_{th}$. However, at applied V_{gs} that does not equal the flat-band voltage V_{fb}, such that $V_{fb} \neq V_{gs} < V_{th}$ results in weak inversion. Band-bending for conduction, valence, and intrinsic *Fermi* level energy bands induces an inversion layer of charge carriers that produce the fully-extended channel between drain and source in the FET structure for $V_{gs} \geq V_{th}$. When V_{gs} is equal to V_{fb}, there is no inversion layer of carriers.[2] However, during t_{sub}, a channel is partially created, lowering the potential barrier between junctions, resulting in charge carriers diffusing from source to drain and generating a channel current. Subthreshold current $I_d(sub)$ is proportional to V_{gs} and V_{ds} based on the general relation from [37] and [50] for PN- and hetero-junction FETs

$$I_{d(sub)} \propto [\exp(\frac{eV_{gs}}{kT})][1 - \exp(\frac{-eV_{ds}}{kT})] \tag{3.20}$$

where k is the *Boltzmann* constant, e represents the *elementary charge* of an electron and T represents the temperature of the semiconductor material in *Kelvin*. For ideal conditions, $I_{d(sub)}$ increases approximately by an order of magnitude for every 60 mV of V_{gs} applied. For $V_{gs} = V_{fb}$ the device is off and the drain-to-source leakage current I_{dss} equals $I_{ds(sub)}$. To stay within the bounds of the thesis scope, subthreshold conduction is estimated using the relation in (3.20). As such, the dissipated power during t_{sub} is estimated by:

$$t_{sub} = R_g C_{iss} \ln(\frac{1}{1 - \frac{V_{th}}{V_{gs}}}) \tag{3.21}$$

$$P_{switch(sub)} = f_n \sum_{i=1}^{N_{sub}} \frac{1}{2} V_{ds}(t) I_{d(sub),i}(t) t_{sub} \tag{3.22}$$

where N_{sub} represents each sub-threshold instance during a line-current period.

3.2.4 Conduction losses

The dissipated power during the on-state due to conduction is represented by:

$$P_{cond,on} = f_n \sum_{i=1}^{N_{cond}} I_{ds,i}^2 R_{ds} t_{on,i} \tag{3.23}$$

where $t_{on,i}$ is the varied on-time interval for each switch in the inverter, $I_{ds,i}$ is the drain current during each $t_{on,i}$ instance and N_{cond} represents the total amount of conduction instances during a line current period. During the off-state for a FET device, i.e $V_{gs} < V_{th}$, the space charge width that forms the channel is reduced, increasing the V_{ds} potential as I_d approaches zero. Off-state conduction losses generated in the channel are expressed as:

$$P_{cond,off} = f_n \sum_{i=1}^{N_{condoff}} \frac{1}{2} \hat{V}_{ds} I_{d(sub)} t_{off,i} \tag{3.24}$$

[2]For enhancement mode FETs $V_{fb} = V_{gs} = 0$, assuming no trapped charge carriers in the passivation material [38].

with $\hat{V}_{ds}$ is the peak applied drain-to-source voltage, $N_{condoff}$ represents each non-conduction and non-switching instance during a line current period, with the corresponding time for each instance represented by t_{off}.

3.2.5 Dead time losses

During a transistor turn-on for the 2L3P configurations, it is necessary to keep the top- and bottom transistor in an off-state beforehand to avoid a shoot-through effect. Shoot-through occurs when both the top and bottom transistors are in an on-state, such that the supply voltage is short-circuited through the drain-to-source channels. The dead time t_{dead} is a specified interval where both serially connected transistors are in the off-state before a subsequent turn-on of either top or bottom. An inductive load's current during this turn off-state, however, requires a reverse conduction path to avoid generating inductive over voltages across the transistors. The GaN HEMTs are capable of reverse conduction across source-to-drain in their third quadrant operation, as explained in Section 3.1.2. Using the voltage drop across the channel in (3.2), the dead time losses can be expressed as [51]:

$$P_{dead,GaN} = f_n \sum_{i=1}^{N} V_{sd} I_{sd} t_{dead} \tag{3.25}$$

The Si-HEXFET utilizes a body-diode for reverse conduction, which similarly induces a voltage drop in the form of V_f, The dead time losses for the Si-HEXFET can be expressed as:

$$P_{dead,Si} = f_n \sum_{i=1}^{N} 2 V_f I_{sd} t_{dead} \tag{3.26}$$

Similarly for 3L3P configurations, the dead time losses occur at intervals where the inductive current from the motor is reverse conducted through the transistor. However, due to the neutral point clamping diodes, the inductive current is conducted through the diodes a majority of the time. Observing the operational intervals in Table 2.2 together with Figure 2.5, one instance of the dead time loss is observed approximately between operational intervals 2-1 for switch S_{b4}. This occurs to S_{b3} being turned-on and S_{b1} is turned-off for the remainder of the period shown in Figure 2.5. During dead time both S_{b4} and S_{b2} are turned-off, whilst the negative inductive current through S_{b3} will conduct through S_{b4}. This occurs similarly for S_{b1} in a separate timed interval[3] where S_{b2} is turned continuously on and S_{b4} continuously off. This occurs for all phase legs, however, as the time interval where dead time losses occur is minor compared to the time interval of a line current period, the dead time losses for 3L3P configurations are considered negligible. As such, the dead time power loss is assumed to be zero for transistors in a 3L3P configuration.

3.2.6 Reverse recovery losses

Dead time t_{dead} is used to avoid the shoot-through effect in the inverter, as explained in Section 3.2.5. A FET device with a body-diode connected between source and

[3]Close to operational state 5 in Figure 2.5

drain functions as a reverse conduction path for an inductive load. As such, the diodes used are the body-diodes in Si-MOSFET inverter configurations and the clamping diodes used in 3L3P inverters. Figure 3.5 illustrates the qualitative characteristics of current through- ($I_D(t)$) and voltage over ($V_D(t)$) the diode during diode turn-off.

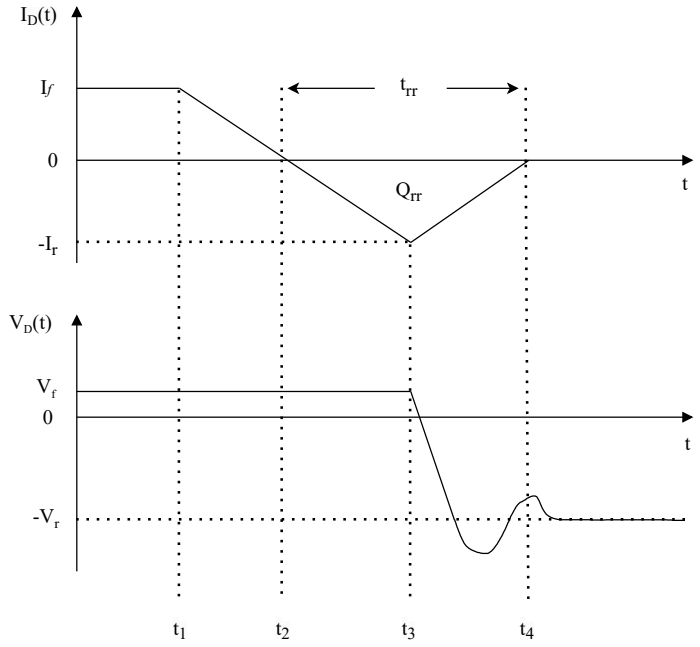


Figure 3.5: General $I_D(t)$ and $V_D(t)$ characteristics during a diode turn-off

Observing the figure, at $t < t_1$ the diode is continuously on with the forward voltage V_f and conducts with the forward current I_f. During t_1, the I_f supplied from the circuit to the diode decreases while the V_f remains constant. At t_2 the I_f is zero whilst the charge carriers stored in the diode retain a constant voltage over the diode V_f. As I_f equals the maximum reverse current I_r for the diode at t_3, minority charge carriers evacuate, causing the diode voltage to approach the applied reverse voltage V_r in t_4. The reverse recovery charge Q_{rr} represents the the time it takes for the charge carriers in the diode to evacuate t_{rr}, expressed as [52]:

$$Q_{rr}(I_f(t)) = \frac{1}{2} t_{rr} I_f(t) \tag{3.27}$$

where $I_f(t)$ is dependent on the current supplied from the circuit. The reverse recovery charge- and loss (P_{rr}) for a diode device is estimated using [52]:

$$P_{rr} = f_n \sum_{i=1}^{N_{rr}} V_{ds}(t) Q_{rr,i} \tag{3.28}$$

where N_{rr} is the total amount of turn-off instances of a diode during a line current period.

3.2.7 Clamping diode losses

Losses due to Schottky clamping diodes (Present only in the 3L3P configurations) are derived by conduction P_{Dcond} and switching $P_{Dswitch}$ losses. The conduction loss is determined by the dynamic resistance of the diode R_{diode} that is dependent on the V_f-I_f characteristic, which is shown for a Schottky barrier diode in Figure 3.6.

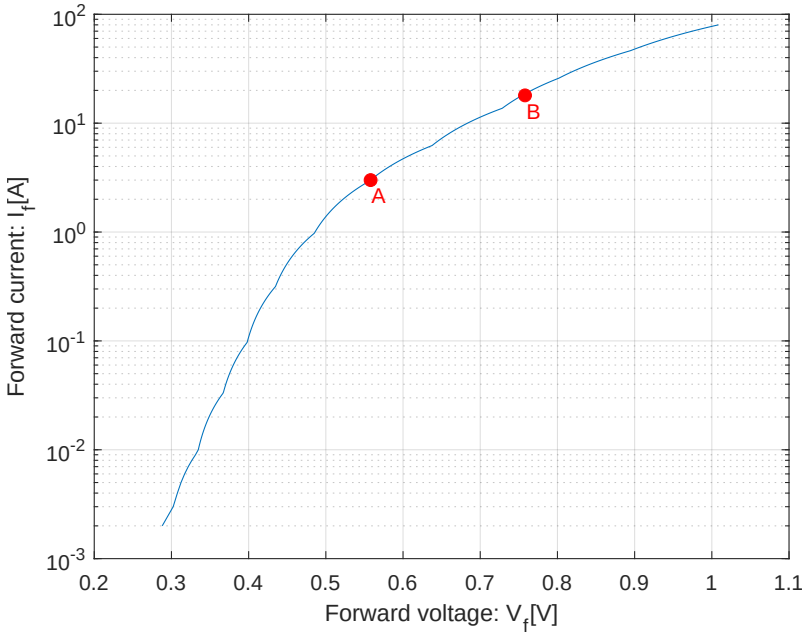


Figure 3.6: Characteristics of $V_f - I_f$ for a Schottky barrier diode at constant temperature $T = 25°C$

Observing the Figure, the two points are A and B are used as an example to determine R_{diode} and V_f. The A point is chosen such that it exceeds the knee-point, i.e turn-on voltage, for the diode. The B point is chosen to represent the zero-to-peak current through the diode. The R_{diode} and V_f can then be expressed as:

$$R_{diode} = \frac{V_{f,B} - V_{f,A}}{I_{f,B} - I_{f,A}} \tag{3.29}$$

$$V_f = V_{f,A} - I_{f,A} R_{diode} \tag{3.30}$$

With the conduction loss determined by:

$$P_{Dcond} = I_{RMS}^2 R_{diode} + V_f I_{AVG} \tag{3.31}$$

where I_{AVG} and I_{RMS} represent the average and RMS current through the diode. The switching losses are determined by analyzing the reverse recovery $P_{Doff,rr}$ and junction capacitance $P_{Doff,c}$ loss as the diode is switched off. Conceptually similarly to Section 3.2.6, $P_{Doff,rr}$ is caused by minority charge carriers retaining a voltage over the diode during diode turn-off. However, due to the unipolar Schottky diode structure, there are no minority charge carriers that contribute to the reverse recovery loss, resulting in $P_{Doff,rr} = 0$ [53]. $P_{Doff,c}$ caused by the parasitic capacitance

between the semiconductor material and metal layer C_r is expressed as:

$$P_{Doff,C} = f_n \sum_{i=1}^{N} \frac{1}{2} C_r V_r^2 \tag{3.32}$$

where C_r is dynamically dependent on applied V_f [54].

3.2.8 Total switch loss

The total semiconductor loss for each inverter configuration during a line current period depends on the types of switches used. The losses are differentiated into losses due to conduction, losses due to switching and losses due to clamping diodes. Losses in two-level GaN HEMT inverter are expressed as

$$P_{cond,2GaN} = P_{cond,on} + P_{cond,off} \tag{3.33}$$

$$P_{switch,2GaN} = P_{trans} + P_{trans(sub)} + P_{dead,GaN} \tag{3.34}$$

$$P_{loss,2GaN} = P_{cond,2GaN} + P_{switch,2GaN} \tag{3.35}$$

Power dissipated in GaN HEMT three-level NDCP inverter determined by

$$P_{cond,3GaN} = P_{cond,on} + P_{cond,off} \tag{3.36}$$

$$P_{switch,3GaN} = P_{trans} + P_{trans(sub)} + P_{oss} + P_{qoss} \tag{3.37}$$

$$P_{D,3GaN} = P_{Dcond} + P_{Doff,c} \tag{3.38}$$

$$P_{loss,3GaN} = P_{cond,3GaN} + P_{switch,3GaN} + P_{D,3GaN} \tag{3.39}$$

Loss calculation for Si-HEXFET two-level inverter described as

$$P_{cond,2Si} = P_{cond,on} + P_{cond,off} \tag{3.40}$$

$$P_{switch,2Si} = P_{trans} + P_{trans(sub)} + P_{dead,Si} + P_{rr} \tag{3.41}$$

$$P_{loss,2Si} = P_{cond,2Si} + P_{switch,2Si} \tag{3.42}$$

Power loss for Si-HEXFET three-level NDCP inverter formulated with

$$P_{cond,3Si} = P_{cond,on} + P_{cond,off} \tag{3.43}$$

$$P_{switch,3Si} = P_{trans} + P_{trans(sub)} + P_{oss} + P_{qoss} + P_{rr} \tag{3.44}$$

$$P_{D,3Si} = P_{Dcond} + P_{Doff,c} \tag{3.45}$$

$$P_{loss,3Si} = P_{cond,3Si} + P_{switch,3Si} + P_{D,3Si} \tag{3.46}$$

4

Methodology

4.1 *LTspice* simulation setup

In the simulation setup, certain components and blocks remain consistent across all simulations. These include: the EM model and load, parasitic elements within a given topology, dead-time for a specific switch technology, and signal generators such as gate drivers, carrier wave generators, and sinusoidal reference wave generators. This consistency ensures that the simulation results are influenced solely by variations in the designated parameters under study.

The implementation details and configurations of some of these blocks are explained in the following sections. To further clarify the simulation setups, Figure 4.1 and Figure 4.2 are included. These figures highlight the different blocks mentioned above for two inverter cases, each with a different topology and switch technology. Only two cases are shown in the presented figures, as all variations of two- and three level inverter simulations utilize the same circuit structure for a given topology and switch technology.

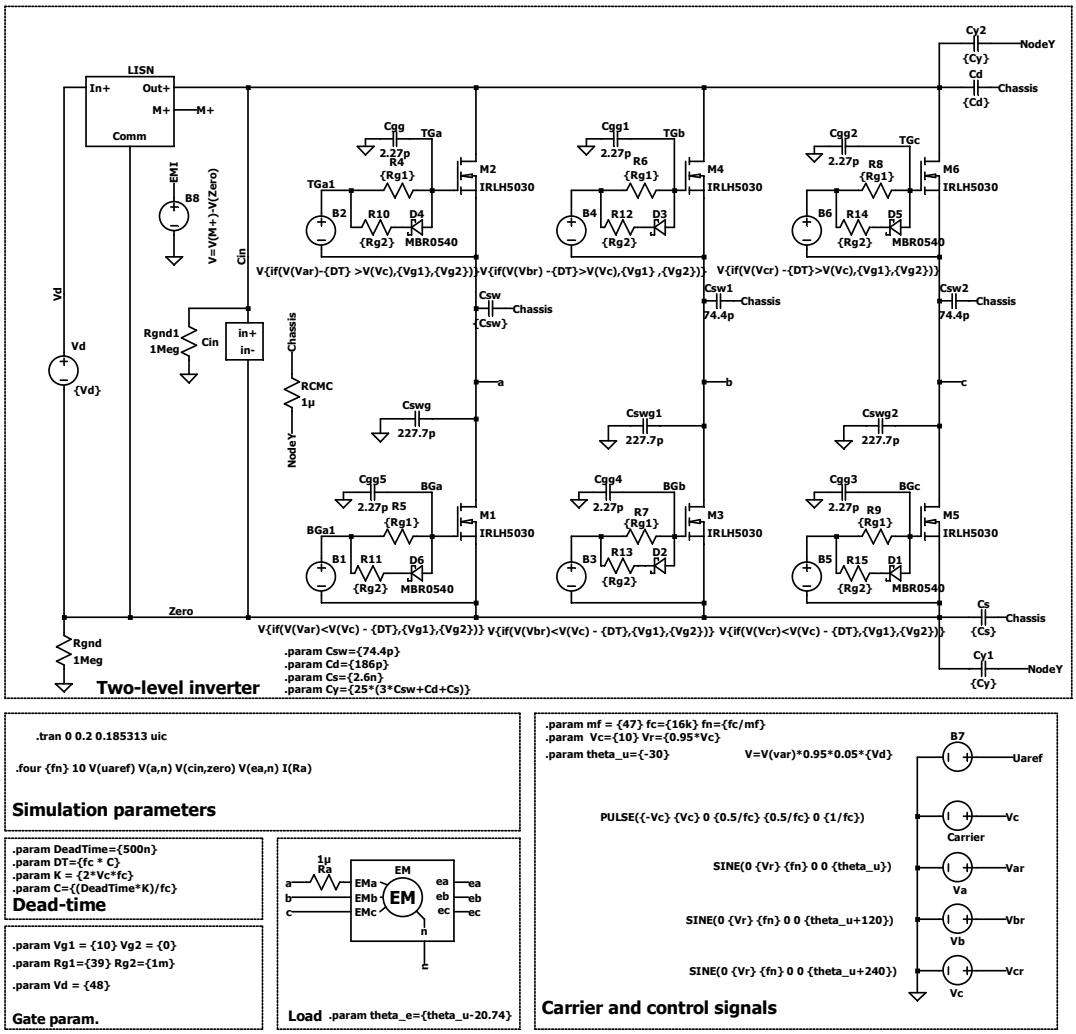


Figure 4.1: Simulation setup of 2L3P Si-based VSI in *LTspice*. The switches used here are the Si-MOSFETs. CMC is measured through the RCMC component and the EMI is measured over the voltage source B8.

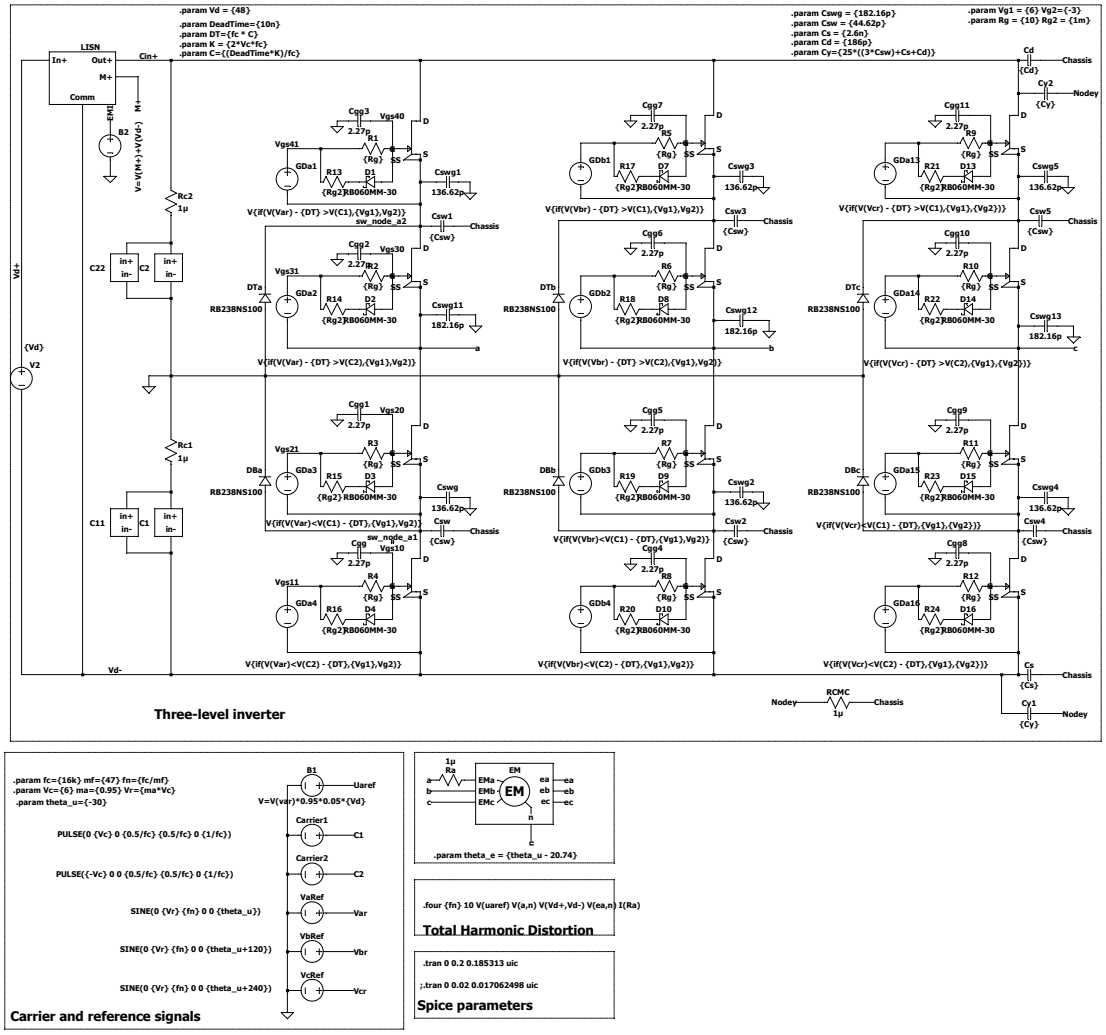


Figure 4.2: Simulation setup of the 3L3P GaN-based VSI in *LTspice*. In this case, the GaN-HEMTs are used as switches. The CMC is measured through the RCMC component, whilst the EMI is measured over the B2 component.

4.1.1 Gate Drivers

In *LTspice*, the gate-drive signals are generated using the *arbitrary behavioral voltage source* component, which allows for the generation of signals based on user-defined conditional expressions.

For the 2L3P inverter, two types of behavioral expressions are used to generate the gate signals. These expressions produce two distinct gate voltages per switch. The functional logic of each block is as follows:

Block 1:

$$\begin{aligned} &\text{if } (V_r > V_c + C): \\ &\quad S_{x2} = V_{\text{gate1}} \\ &\text{else}: \\ &\quad S_{x2} = V_{\text{gate2}} \end{aligned}$$

Block 2:

$$\begin{aligned} &\text{if } (V_r < V_c - C): \\ &\quad S_{x1} = V_{\text{gate1}} \\ &\text{else}: \\ &\quad S_{x1} = V_{\text{gate2}} \end{aligned}$$

As shown in Figure 2.1, TG_x and BG_x correspond to the top and bottom gate signals, respectively, for each phase leg. The values V_{gate1} and V_{gate2} represent the gate voltages in the ON and OFF states of the switches. The constant C serves as a control parameter for adjusting the dead-time between switching transitions. The *arbitrary behavioral voltage source* effectively acts as a comparator in this configuration.

For the 3L3P inverter, four such behavioral blocks are required per leg to control the switching. In this case, two different carrier signals are compared with the sinusoidal reference to determine the states of the upper switches. This arrangement is illustrated in Figure 2.4.

4.1.2 Implementation of electrical machine in *LTspice*

The EM, whose parameters are calculated in Section 2.5, is implemented in *LTspice* as a three-phase RL circuit with a sinusoidal signal generator used to emulate the back EMF of the EM. The implemented circuit in *LTspice* is shown in Figure 4.3. The measured EM parameters, including dq-axis inductances and phase resistance, are presented in Table 4.1.

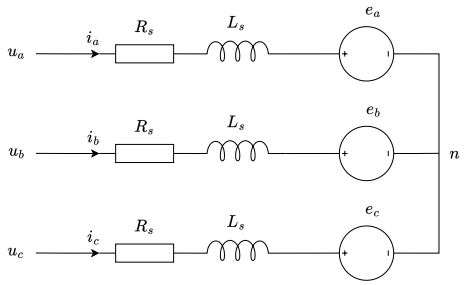


Figure 4.3: Implementation of EM in *LTspice*. Here, R_s and L_s represent the phase resistance and inductance of the EM, while $e_{a,b,c}$ denotes the back EMFs.

Table 4.1: EM parameters used in *LTspice*

Parameter	Value
L_d	186.60 μH
L_q	233.00 μH
R_s	39.00 mΩ
Ψ_m	9.45 mWb
n_p	4

Since the EM is modeled as a non-salient machine, the stator inductance as given in (2.34), is put equal to the average value of the dq-inductances detailed in Table 4.1. The operating point for the machine is a function of the output torque and the rotor speed. Here, the output torque is set to the rated torque of the EM, which is 1Nm, and the speed is chosen so that the DC-link voltage is less than or equal to 48 volts, which is the voltage supplied by the power supply. Thus, the operating point of the machine is set to;

$$T_e = 1\text{Nm}$$
$$\Omega_r \approx 5100\text{rpm}$$

These values and (2.21) to (2.50) are then used to compute the back EMFs, phase voltages, and phase currents, which result in:

$$u_{a,b,c} = 22.67\cos(2\pi f_n t + 112.81^\circ + 0^\circ, 120^\circ, 240^\circ) \tag{4.1}$$
$$e_{a,b,c} = 20.21\cos(2\pi f_n t + 90.00^\circ + 0^\circ, 120^\circ, 240^\circ) \tag{4.2}$$
$$i_{a,b,c} = 17.64\cos(2\pi f_n t + 90.00^\circ + 0^\circ, 120^\circ, 240^\circ) \tag{4.3}$$

To verify the performance of the EM, sinusoidal signal generators are used as an inverter, the output of these generators are adjusted such that the phase voltages have the same amplitude and phase as in (4.1), and then the simulated values are compared with the theoretical values in Section 5.3.4.

4.1.3 Electrical switches

The selection of the switches are constrained by two factor:

1. Both Si-based and WBG-based switches should have manufacturer-built *LTspice* models.
2. The switches' power ratings should be similar to keep the inverter's power density the same for a given topology.

Based on these two criteria, two switches are chosen and they are presented in Table 4.2 together with their respective electrical parameter.

Table 4.2: Electrical parameters of the switches used in the simulations

Parameter	GS61008P (GaN Systems)	IRLH5030PbF (Infineon)
Type	GaN HEMT	Silicon MOSFET
Drain-to-Source Voltage (V_{DS})	100 V	100 V
On-State Resistance ($R_{DS(on)}$)	7 mΩ (typ.), 9.5 mΩ (max.)	7.2 mΩ (typ.), 9.9 mΩ (max.)
Continuous Drain Current (I_D)	90 A (T_{case} = 25°C)	88 A (T_{mb} = 25°C)
Gate-to-Source Voltage (V_{GS})	-10 V to +7 V	±16 V
Gate Threshold Voltage ($V_{GS(th)}$)	1.1 V (min.), 1.7 V (typ.), 2.6 V (max.)	1.0 V (min.), 2.5 V (max.)
Total Gate Charge (Q_G)	8 nC	44 nC (typ.)
Input Capacitance (C_{ISS})	600 pF	5185 pF
Output Capacitance (C_{OSS})	250 pF	300 pF
Reverse Recovery Charge (Q_{RR})	0 nC (Zero reverse recovery loss)	190 nC (typ.), 285 nC (max.)
Thermal Resistance Junction-to-Case ($R_{\theta JC}$)	0.55 °C/W	0.5 °C/W (typ.), 0.8 °C/W (max.)
Diode Type	No body diode (reverse conduction via channel)	Intrinsic body diode
Diode Forward Voltage (V_{SD})	Conducts at $R_{DS(on)}$	1.0 V (max.)
Diode Reverse Recovery Charge (Q_{RR})	0 nC (no reverse recovery)	190 nC (typ.), 285 nC (max.)
Diode Reverse Recovery Time (t_{rr})	N/A	32 ns (typ.), 48 ns (max.)

4.1.4 DC-Link Capacitors

In 3L3P inverters, the DC-link capacitors function as voltage dividers. To ensure comparable EMI performance across different inverter topologies, DC-link capacitors are also included in the two-level inverter configuration. In *LTspice*, the DC-link capacitors are implemented such that the effective capacitance seen from the source remains the same for both two-level and three-level inverter setups. The DC-link capacitors are modeled collectively as C_{in}, as shown in Figure 4.1. This block comprises multiple individual capacitors. To improve simulation speed, the series inductance of the capacitors was omitted, as its inclusion significantly increased simulation time. The composition of C_{in} in terms of quantity, capacitance, and equivalent series resistance (ESR) is summarized as the following:

Type	**Quantity**	**Capacitance** [nF]	**ESR** [mΩ]
Bulk capacitors	10	47,000	566
Low-ESR capacitors	30	10	67

4.1.5 Line Impedance Stabilization Network

To measure the conducted EMI, the LISN device described in Section 2.6 is used in *LTspice*. The voltage can be measured at the marked Measuring Point (MP), and performing FFT on this signal outputs the EMI versus frequency of the inverters. Since in this study only a relative EMI comparison is performed, the EMI of the different inverter topologies are compared to that of the 2L3P Si-based inverter with a switching frequency of 16 kHz.

4.1.6 Harmonic distortion

The harmonic distortion is evaluated solely for the phase current, as it directly contributes to torque ripple. Also, as derived in Section 2.7, harmonic overtone content contributes to an increased power loss over load, whilst $\text{THD}_{I_{phs}}$ is the FOM

of that content. As such, only the $\text{THD}_{I_{phs}}$ index is considered in the analysis in regards to a qualitative increase in dissipated power in the motor windings. $\text{THD}_{I_{phs}}$ is calculated using the built-in Fourier analysis tool in *LTspice*, which provides the harmonic components, their respective phases and orders, and the $\text{THD}_{I_{phs}}$ value.

4.1.7 Common-mode current

As described in Section 2.4, the CMCs are induced through the parasitic capacitors described in Figure 2.9. These capacitors, denoted as C_{sw}, are connected to the chassis as shown in Figure 4.1 and Figure 4.2. The values of these capacitors are outlined in Table 2.3. The CMC current is measured through the RCMC component in each inverter. Furthermore, the RMS and peak values of the CMC are extracted from the data using MATLAB.

4.2 Switch performance evaluation

The semiconductor switch parameters in Section 4.1.3 are analyzed in terms of function and material properties. Switches chosen are then analyzed in terms of datasheet characteristics in conjunction with the inverter configurations to determine a switch loss model.

4.2.1 Semiconductor evaluation

To evaluate WBGT compared to power Si-MOSFETs in two and three level inverters, the power Si-HEXFET is chosen due to the similarities in rating and characteristics to the Si-MOSFETs used in the integrated two-level inverter designed by *Aros Electronics*. The WBG GaN-HEMT is chosen due to the GaN material properties presented in Table 3.1 in comparison to Si. Increased μ_n resulting in a theoretically higher f_{cut}, according to (3.5), resulting in the possibility of an elevated switching frequency. Similarly, as μ_n is proportional to g_m in (3.4), indicating a reduction in R_{on} according to (3.9). Peak electron velocity determines the mobility during $I_{d,sat}$ and g_m is constant, determining the upper limit of f_{cut} as higher for GaN. Higher thermal conductivity indicates that adverse affects, such as lattice scattering from heat-buildup, are inherently mitigated more compared to Si. Lower ϵ_r results in lower capacitance between gate-source-drain, decreasing Q_g according to (3.6). In turn, lower Q_g decreases transient switch losses and parasitic losses in Sections 3.2.1 and 3.2.2.

Finally, GaN HEMTs do not exhibit reverse recovery losses as explained in Section 3.1.2. Note that the dimensions and doping concentrations of the transistors are unknown, which affects the properties seen in Section 4.1.3. As such, the assessment is qualitative and used to indicate the reason why properties of the transistor materials differ. Schottky diodes are used as clamping diodes in the three-level inverter due to the zero reverse recovery loss derived in Section 3.2.7.

4.2.2 Semiconductor loss model

The semiconductor loss models are written as *Matlab* scripts, utilizing the loss calculation from the four different inverter topologies presented in Section 3.2.8. To accurately model the current and voltage levels at the correct time intervals, the model is based upon the reference and carrier signal(s) used to determine the gate signals in Section 4.1.1. During turn-off $V_{ds} = V_d$ and during turn-on the V_d voltage is divided by a inductive load that mimics the load attached to the inverter, generating an AC I_d current through the switch.

For each turn-on/off, the time and index appropriate to I_d and V_d are logged, such that that the average conduction, switching and diode loss during each time-interval are determined. All losses are calculated separately and determined by the accumulated energy during multiple reference wave periods, averaged such that the dissipated power over one fundamental period is achieved. Of note, the datasheet value of $R_{on} = 7m\Omega$ provided for GaN-HEMT GS61008P in Table 4.2 is incongruent with the *LTspice* model provided by *GaN Systems* at constant $T = 300K$. Therefore the semiconductor loss model utilizes the *LTspice* $R_{on} = 4.4m\Omega$ to remain consistent in the evaluation.

4.3 Measurement of the existing 2L3P Si-based inverter

Although the simulations used in this thesis do not perfectly represent the actual system, it remains important to evaluate how closely the simulation results align with real-world measurements. In particular, comparisons are made against the physical 2L3P inverter driving the water pump. To this end, measurements of gate voltage, phase-to-phase voltage, and phase current were taken using an oscilloscope.

The gate voltage reveals details about gate parasitics, as well as the rise and fall times[1]. The phase-to-phase voltage provides insights into voltage ripple and overshoot characteristics, while the phase current allows analysis of current ripple and the calculation of $\text{THD}_{I_{phs}}$. The collected data is then imported into *MATLAB* for plotting, harmonic analysis, and further post-processing.

4.4 Estimated Cost

This section outlines the methodology used for evaluating and comparing the economic feasibility of different inverter configurations. The cost analysis includes two major components: the initial component cost and the operational cost, also referred to as cost-in-use. While R&D costs are also relevant in practical product development, they are excluded here due to confidentiality. Additionally, R&D costs are

[1]The simulated switches are not identical to those used in the physical inverter. However, both are Si-based MOSFETs, which generally exhibit similar characteristics in terms of parasitic behavior, body diode properties, etc.

assumed to be approximately equal across all topologies due to comparable PCB complexity and software requirements.

Initial Component Cost

The initial cost reflects the one-time cost to manufacture a single inverter unit and is calculated using BOM data provided by *Aros Electronics AB*. It includes:

- Power semiconductor devices (Si-MOSFETs or GaN HEMTs) and Gate driver ICs
- Clamping diodes (for three-level topologies only)
- Passive components (including input filter) and connectors
- Microcontroller, onboard Buck-converter, and protection circuitry
- PCB and assembly costs

A production volume of 1000 units is assumed to represent a typical medium-scale manufacturing scenario, enabling volume-based pricing and the amortization of fixed setup costs. To estimate the cost of different inverter topologies, the baseline is defined as the cost of the existing inverter excluding the gate drivers and power transistors (MOSFETs), as the remaining circuit components are shared across all inverter variants evaluated in this thesis. This base cost is uniformly applied to all configurations, with additional costs for semiconductor switches, clamping diodes, and gate drivers added according to the specific topology. Although the input filter capacitors in three-level inverters operate at half the input voltage and therefore require only half the voltage rating of those in two-level inverters, their capacitance are doubled to maintain equivalent energy storage. Consequently, the cost of the input capacitors is assumed to be equal across all inverter types, or negligible in terms of variation.

Cost-in-Use (Operational Cost)

Cost-in-use refers to the accumulated cost of power losses in the inverter during normal operation, assuming a fixed electricity rate. It provides a measure of how efficiently each inverter uses power over time and it is calculated as:

$$\text{Cost-in-use} = \frac{P_{\text{loss}}}{1000} \cdot C_{\text{kWh}} \quad [\text{SEK/h}] \tag{4.4}$$

where:

- P_{loss}: Total inverter power loss in watts, obtained from *LTspice* simulations
- C_{kWh}: Electricity cost per kilowatt-hour, fixed at 1.24 SEK/kWh (based on Gothenburg 2025 prices for industry usage)

Break-Even Time Analysis

To determine when a more efficient but costlier inverter becomes economically justified, the break-even time t_{BE} is calculated using:

$$t_{\text{BE}} = \frac{C_{\text{init, expensive}} - C_{\text{init, reference}}}{C_{\text{use, reference}} - C_{\text{use, expensive}}} \quad [\text{hours}] \tag{4.5}$$

Where:

- C_{init}: Initial component cost of the inverter [SEK]
- C_{use}: Operational cost per hour [SEK/h]
- t_{BE}: Number of hours required to recover the extra initial cost through power savings

This metric is particularly useful for data center and industrial applications where continuous operation over long periods is expected. A configuration with a shorter break-even time is economically more favorable for long-term use.

5
Results

In this chapter, the performance of the two inverter topologies (2L3P and 3L3P NPDC) combined with two semiconductor technologies (Si-MOSFET and GaN HEMT) is evaluated. Both simulation results from *LTspice* and theoretical calculations are presented. The main performance metrics compared are power losses, efficiency, $\text{THD}_{I_{phs}}$, EMI, CMC, and economic factors, including initial and running costs.

5.1 2L3P *LTspice* simulations and measurements

This section presents *LTspice* simulation and measurements results for the 2L3P inverter. The analysis covers both Si-MOSFET and GaN HEMT at switching frequencies of 16 kHz and 200 kHz. Performance metrics include power loss, efficiency, $\text{THD}_{I_{phs}}$, CMC, and EMI. Waveforms analyses are shown to illustrate the inverter's operation and switching characteristics clearly.

5.1.1 2L3P Si inverter (reference inverter)

The performance of the Si-based two-level inverter described in this section serves as a reference for comparing the performance of the other inverters mentioned earlier. The *LTspice* simulation parameters for the reference inverter in Figure 4.1 are:

$V_d = 48\text{V}$	$t_{dead} = 500\text{ns}$	$f_c = 16\text{kHz}$	$m_f = 47$
$m_a = 0.95$	$f_n = 340.4255$	$\hat{U}_{an} = 22.35$	
$R_{g1} = 30\Omega$	$R_{g2} = 1\text{m}\Omega$	$V_{g1} = 10\text{V}$	$V_{g2} = 0\text{V}$

As described in Section 2.1, the reference signal is compared to the carrier signal, and the resulting gate signals are generated. Figure 5.1b illustrates the carrier signal and the gate voltages of phase A. The shaded gray area represents t_{dead}, implemented to prevent simultaneous switch conduction, which could lead to a short circuit of the DC-link.

Figure 5.1 presents the waveforms of the 2L3P Si-based inverter operating at a switching frequency of 16 kHz. Specifically, the figure includes the gate voltages, drain-to-source voltages, phase currents, power losses, and phase voltages. These waveforms serve as a benchmark for subsequent comparisons with other inverter configurations and switching technologies.

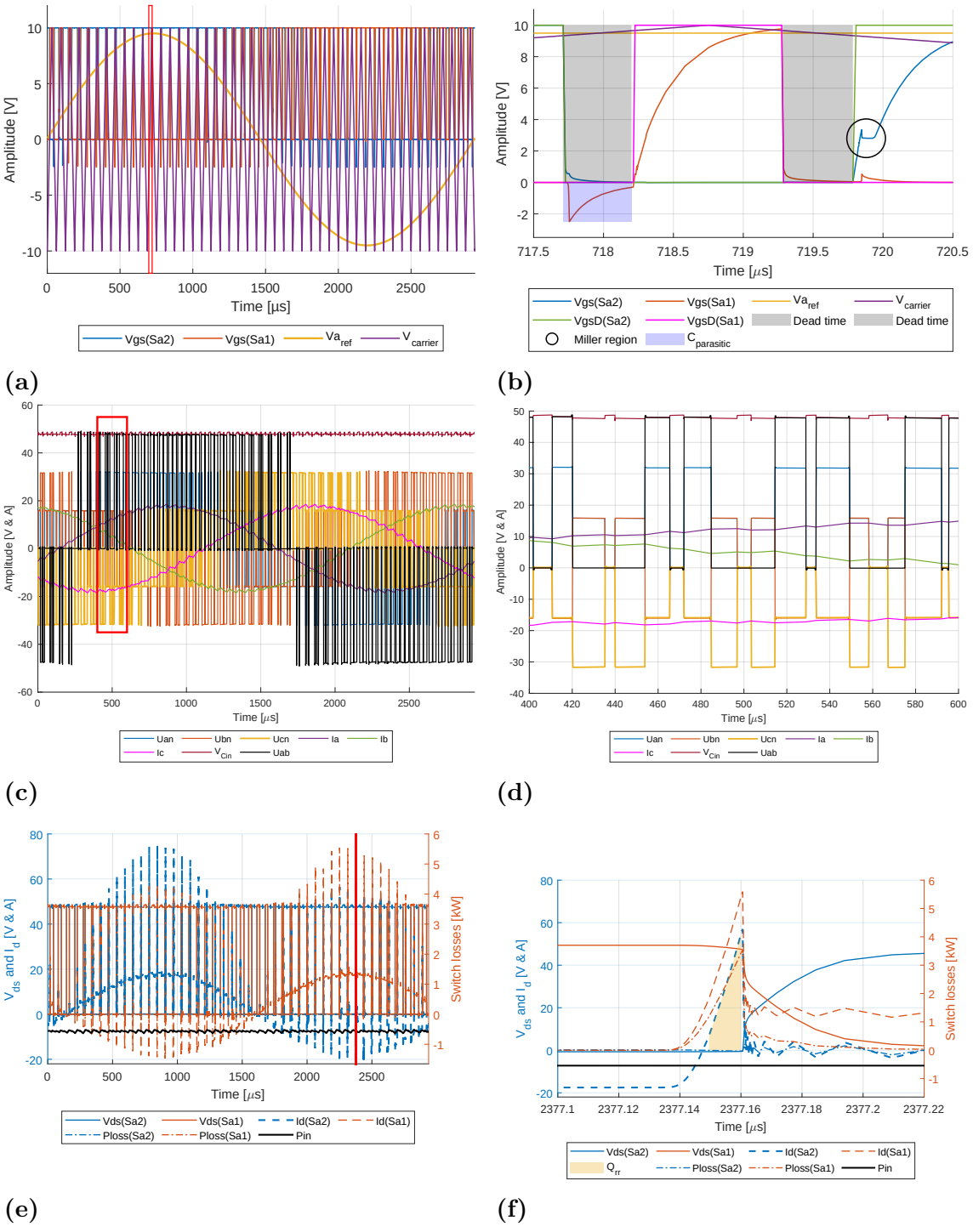


Figure 5.1: Performance of the Two-level Three-phase Si-based inverter with switching frequency of 16 kHz. **(a)** shows the carrier, reference, and gate signals. **(b)** is a zoomed-in version of **(a)**; here, VgsD is the signal output of the gate driver. **(c)** illustrates phase voltages, currents, and the DC-link voltage. **(d)** is a zoomed-in version of **(c)**. **(e)** shows the Vds, Ids, and power loss of phase-a switches. **(f)** is a zoomed-in version of **(e)** which highlights the reverse recovery region.

The blue-highlighted gate voltage in Figure 5.1b originates from the gate-to-source

parasitic capacitance, C_{gs}. In this scenario, the gate of S_{a1} is held low, and when S_{a2} turns off, the body diode of S_{a1} begins to conduct, as indicated by the negative drain current in Figure 5.1f.

Consider the initial condition where S_{a1} is off and its gate is tied to the source via the gate driver through the resistor R_{g2}, as shown in Figure 4.1. When S_{a2} turns off, its drain-to-source voltage increases, while the drain-to-source voltage of S_{a1} decreases (refer to Figure 3.3 for the corresponding waveforms). As a result, the following relation for S_{a1}:

$$V_{ds} = V_{dg} + V_{gs} \tag{5.1}$$

also decreases. The fall time of the drain-to-source voltage for S_{a1}, as observed in Figure 5.1f, is approximately 7.5 ns. Assuming the gate charge remains roughly constant during this transition, the voltage drop from V_{Cin} to roughly zero across the drain-to-gate capacitance (C_{dg}) leads to a charge redistribution, inducing a negative voltage across C_{gs} as:

$$V_{gs} = -\frac{C_{gd}}{C_{gs}} V_{Cin} \tag{5.2}$$

as V_{ds} reaches its minimum value. According to the Si-HEXFET datasheet, the input, output, and reverse transfer capacitances at $V_{ds} \approx 48$ V are:

$$C_{iss} = C_{gd} + C_{gs} \approx 5105 \text{ pF} \tag{5.3}$$
$$C_{oss} = C_{gd} + C_{ds} \approx 305 \text{ pF} \tag{5.4}$$
$$C_{rss} = C_{gd} \approx 145 \text{ pF} \tag{5.5}$$

Using the values from Table 3.1, the gate-to-source voltage at the moment when the drain-to-source voltage of S_{a2} reaches its peak can be calculated as:

$$V_{gs} = -\frac{C_{rss}}{C_{iss} - C_{rss}} V_{Cin} = -1.40 \text{ V} \tag{5.6}$$

This theoretical gate-to-source voltage is less negative than the simulated value of approximately -2.7 V. The discrepancy may stem from two main factors: (1) the datasheet values are approximations and may not represent actual dynamic behavior precisely, and (2) the *Spice* model does not dynamically adapt the parasitic capacitances based on the operating voltage. For instance, from (5.3)-(5.5), C_{gs} is estimated at approximately 4960 pF, while the value used in the *Spice* model is 6681 pF. The rapid decrease of $V_{ds}(S_{a1})$ induces an initial negative spike in V_{gs} due to the parasitic interaction. Since the gate is connected to the source through the gate driver, C_{gs} discharges through R_{g2}, gradually bringing V_{gs} back toward zero.

By comparing the waveforms of the 2L3P Si-based inverter in Figure 5.1 with the ideal case shown in Figure 2.2, it becomes evident that the waveforms (gate signals, phase voltages) of Si-based inverter deviates from the theoretical model due to the

presence of parasitic elements, as discussed previously. In addition, the dead time (t_{dead}) and the voltage drop over the switching devices result in a reduced output voltage and increased ripple. The effects of the voltage ripple can be seen in Figure 5.1c, and the voltage drop effects are reflected in Table 5.3, where the Si-based inverter demonstrates a lower phase voltage compared to the theoretical values (21.62 V, 22.35 V) [1]. Nevertheless, the 2L3P Si-based inverter in Figure 5.1 generally behaves as expected, considering the inevitable differences between theoretical and practical implementations.

[1]The methodology for obtaining these values are explained in Section 5.3.4

5.1.2 2L3P Inverter measurements

To assess that the simulation results align with a real implemented circuit, measurements were taken from the existing inverter. The MOSFETs driving the inverter in this case are different from those used in the simulations. This comparison aims to illustrate the general behavior of a Si-based inverter implemented in a product, as opposed to an exact match to the simulated setup. The electrical EM's operating point and the DC-link input voltage are maintained in the same way as in the simulations. The measured parameters include: Switch gate voltage S_{a1}, Phase current, and inverter phase-to-phase voltage which are shown in Figure 5.2.

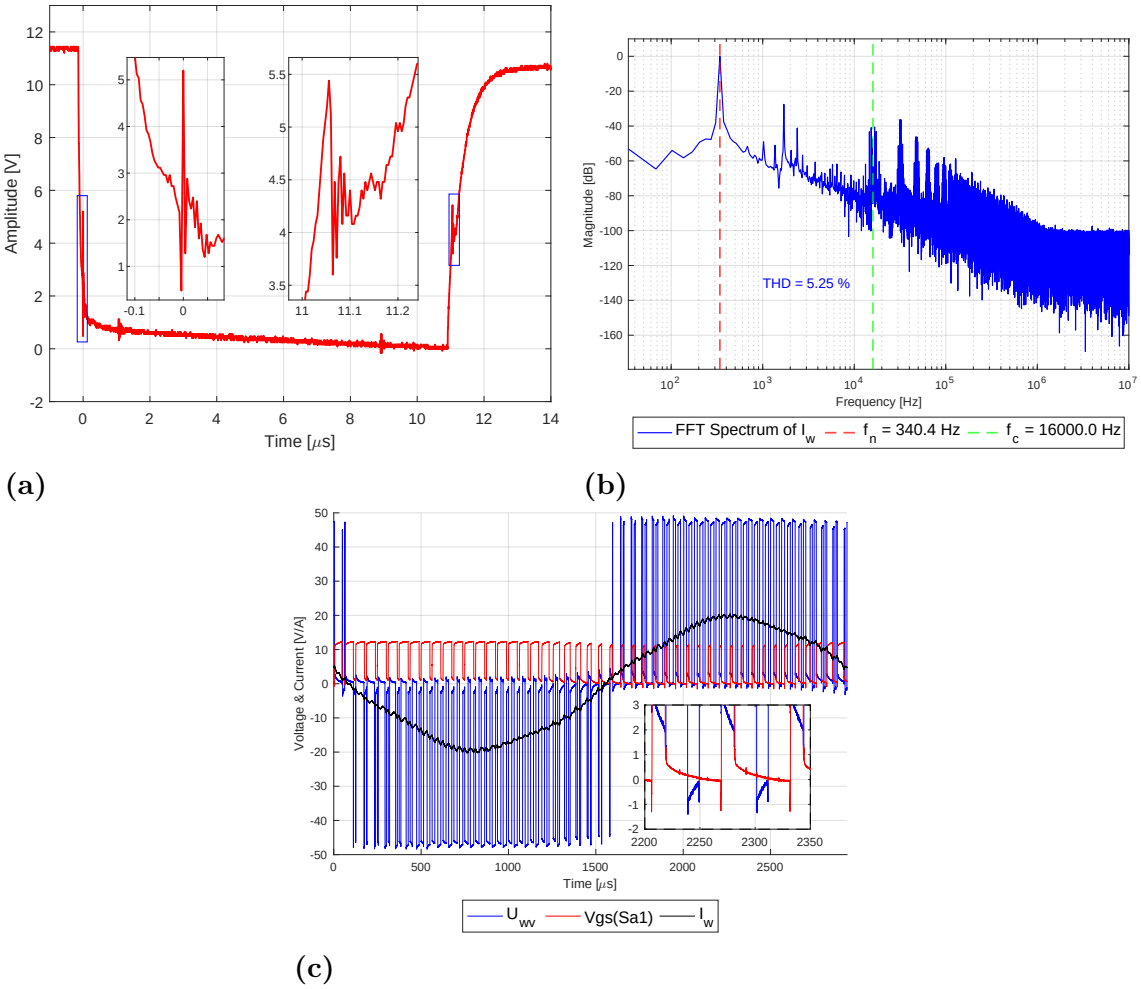


Figure 5.2: Measured performance of the existing 2L3P inverter. **(a)**: gate voltage of $Sa1$, **(b)**: frequency spectrum of the phase-current, and **(c)**: phase-to-phase voltage, phase current, and gate voltage.

In Figure 5.2a, two regions are highlighted for clarity: the left window captures oscillations caused by parasitic gate capacitance during phase voltage transitions (also visible in the zoomed-in window in Figure 5.2c), while the right window shows the *Miller* plateau, attributed to the *Miller* capacitance. A similar behavior is also visible for the simulated version in Figure 5.1b.

Figure 5.2b presents the frequency spectrum of the measured phase current, clearly showing both the fundamental and switching frequency components. The total harmonic distortion of the phase current, $\mathrm{THD}_{I_{\mathrm{phs}}}$, in the physical 2L3P inverter is measured to be 5.25%, compared to 2.8% in the simulated 2L3P Si-based inverter under the same switching frequency and EM load conditions. This indicates that the actual inverter performs significantly worse than the simulation.

This discrepancy could be attributed to several practical non-idealities, such as power supply voltage ripple, insufficient input capacitance, and disturbances introduced by the EM and load, all of which are more idealized or neglected in the simulation.

Additionally, the phase-to-phase voltage of the physical inverter exhibits more oscillations, manifested as sharp transients and ramped waveforms at voltage peaks, when compared to the ideal square waveforms shown in Figure 2.2, and the slightly less distorted waveforms in the simulation results of Figure 5.1d. This discrepancy can be attributed to the fact that, in simulation, power is delivered directly to the switches without transmission losses, whereas in the physical setup, the power cable introduces additional inductance and resistance, contributing to waveform distortion. Moreover, the stray inductance between the DC-link capacitors and switches adds additional switching ripple and distorions.

The comparison demonstrates that the simulation model captures the key dynamic behaviors of the inverter, such as switching characteristics, harmonic content, and voltage transitions. Although some differences exist due to parasitics not modeled in detail, the simulation results are sufficiently accurate for evaluating design trends, control strategies, and performance metrics. Therefore, the simulation model can be considered valid for analysis and design purposes, providing meaningful insights before hardware implementation.

5.1.3 2L3P GaN Inverter at 16 kHz Switching Frequency

As GaN HEMTs support increased switching frequencies and lack body diodes used in Si-MOSFETs, several parameters were adjusted to optimize performance and utilize the rated capabilities of these devices. The adjusted parameters are listed below:

$V_d = 48\,\mathrm{V}$	$t_{dead} = 10\,\mathrm{ns}$	$f_c = 16\,\mathrm{kHz}$	$m_f = 47$
$m_a = 0.95$	$f_n = 340.4255$	$\hat{U}_{an} = 22.35$	
$R_{g1} = 10\,\Omega$	$R_{g2} = 1\,\mathrm{m}\Omega$	$V_{g1} = 6\,\mathrm{V}$	$V_{g2} = -3\,\mathrm{V}$

Figure 5.3 illustrates the waveforms of 2L3P GaN-based inverter switching at 16kHz. This inverter, in general, resembles the 2L3P Si-based inverter explained previously. However, due to the significantly reduced t_{dead} and R_g, the gate voltage exhibits faster rise time. Furthermore, GaN HEMTs have no body diode, which causes the reverse recovery behavior to be primarily determined by the device's parasitic capacitances. Figure 5.3 highlights two main distinctions of the GaN-based inverter

compared to traditional Si-based designs as in Figures 5.1b and 5.1f. The following observations can be made from these results:

1. Comparing Figure 5.1b and Figure 5.3a, since both figures share the same x-axis window, it is evident that the gate voltage rise time, in $V_{gs}(Sa1)$ as an example, for the 2L3P GaN inverter is significantly shorter than in the 2L3P Si inverter. This is due to the reduced gate charge, compare the values in Table 4.2, and gate drive resistance, see the values of R_{g1} in Sections 5.1.1 and 5.1.3, resulting in decreased gate voltage rise time, represented by (3.8). This supports the use of significantly lower t_{dead} for the GaN-HEMTs compared to Si-HEXFETs.

2. The switching energy loss during transitions between on/off states is considerably lower in GaN-based inverters compared to their silicon counterparts, thereby improving overall efficiency. This can be observed in Figure 5.3b, where the voltage fall time in $V_{ds}(Sa2)$ and current rise time in $I_{ds}(Sa1)$ overlap is approximately 6 ns. In contrast, the voltage rise time in $V_{ds}(Sa1)$ and current fall time in $I_{ds}(Sa1)$ overlap for the 2L3P Si-based in Figure 5.1f inverter is roughly 40 ns. Corresponding approximately to the theoretical calculation done in (3.11) and (3.12). Showcasing that lowered input capacitance reduces energy switch loss.

3. Reverse conduction of the GaN-HEMTs described in (3.1) can be noted in 5.3b where $I_d(Sa2)$ is negative whilst $V_{ds}(Sa2)$ indicates that the device is in cut-off. Showcasing that no body-diode is required which significantly reduces transistor turn-on losses.

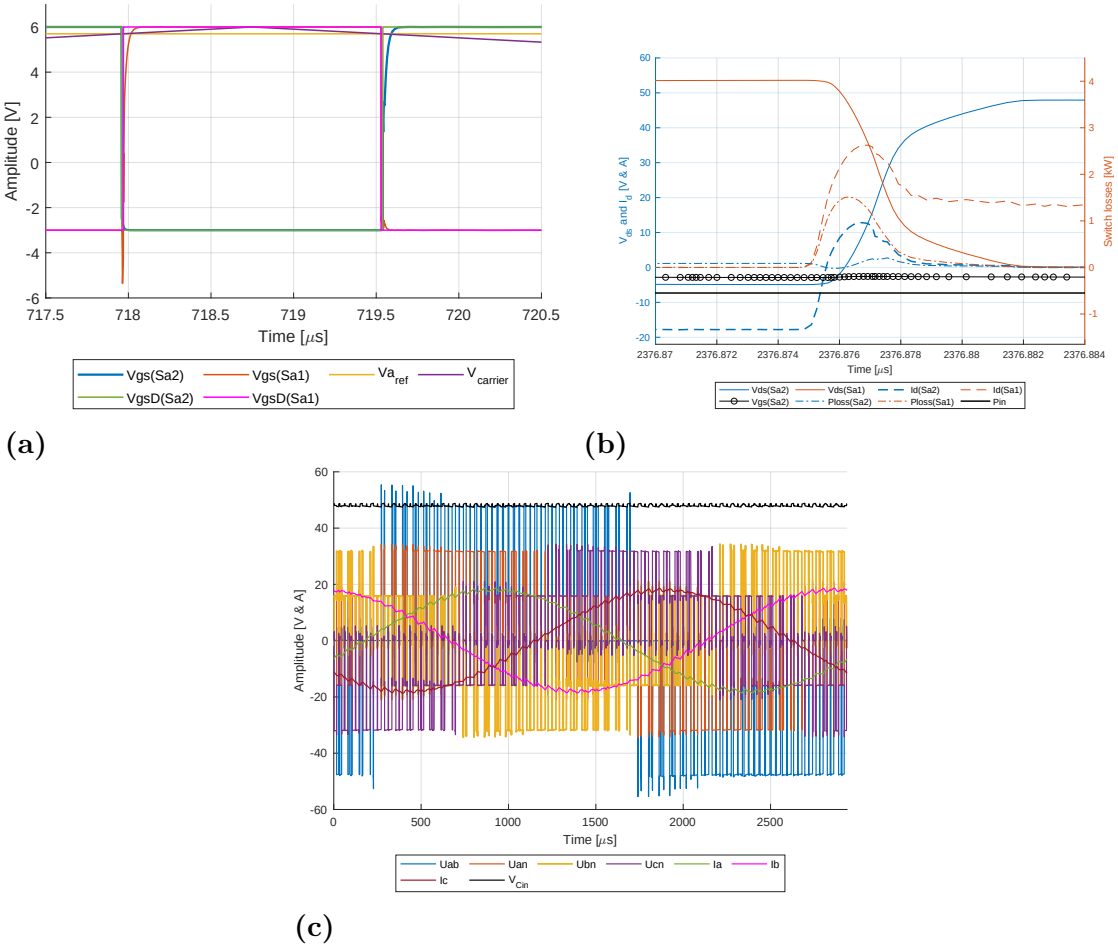


Figure 5.3: Performance of the 2L3P GaN-based inverter operating at 16 kHz. **(a)** shows the gate voltage waveforms of phase-A switches. **(b)** Shows the corresponding power loss, drain-source voltage (V_{ds}), and drain current (I_d) for the same phase. **(C)** illustrates the phase voltages and phase currents.

5.1.4 2L3P GaN Inverter at 200 kHz Switching Frequency

GaN-HEMTs are capable of operating at switching frequencies in the MHz range. As such, the switching frequency is increased to 200 kHz to investigate the impact of higher switching frequencies on the inverter performance. Figure 5.4 illustrates the behavior of the inverter at this frequency. Since the t_{dead} and R_g remain unchanged from the 16 kHz case, the gate voltage rise time also remains similar, as seen previously in Figure 5.3a.

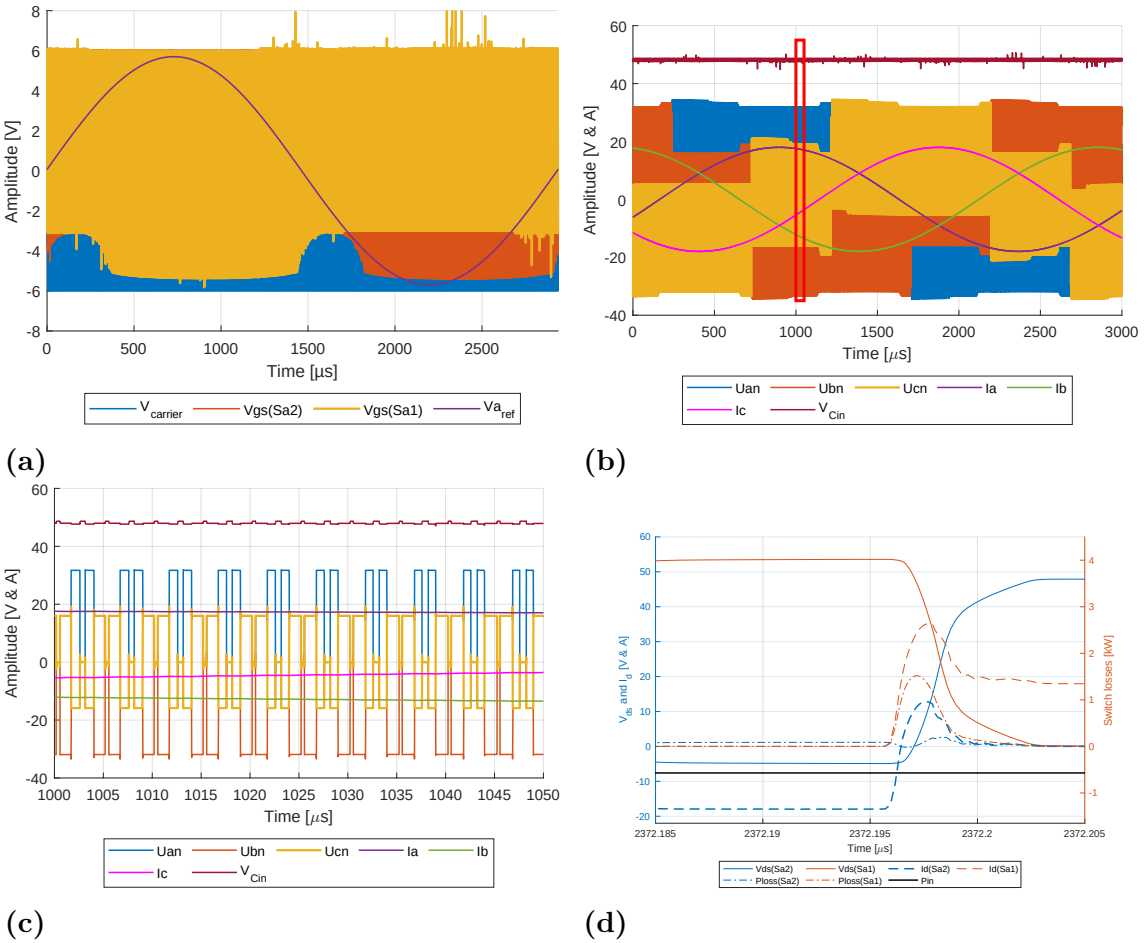


Figure 5.4: Performance of the two-level three-phase GaN-based inverter operating at 200 kHz. **(a)** shows the high-frequency carrier and gate signals, **(b)** presents the phase voltages and currents, **(c)** is a zoomed-in version of (b), and **(d)** shows the switching behavior and power loss of phase-a switches.

As illustrated in Figure 5.4b, the increased switching frequency leads to a significant reduction in the ripple of the phase current when compared to the 16 kHz case illustrated in Figure 5.3c. This results in improved output current quality and lower harmonic distortion, contributing to better overall power quality.

However, this improvement comes at the cost of increased switching losses, as the number of switching events within the same time window is higher. A higher switching frequency results in more frequent transitions, causing greater energy dissipation per unit time. This inverter, like the 2L3P Si-based inverter, exhibits similar behavior, with the key difference being the elevated switching frequency. This results in a cleaner current waveform, but also leads to increased power loss due to more frequent switching events.

5.2 3L3P NPDC inverter simulation results

This section presents the simulation results of the 3L3P NPDC VSI using both Si MOSFETs and GaN HEMTs. All configurations employ the PD-SPWM scheme to ensure a fair comparison. Performance is evaluated at switching frequencies of 16 kHz and 200 kHz, focusing on switching behavior, waveform quality, and loss characteristics. The analysis begins with the Si-based inverter, followed by GaN-based implementations.

5.2.1 3L3P Si-Based Inverter

The simulation parameters used for the three-level Si-based inverter are consistent with those applied in the two-level counterpart described in Section 5.1.1, allowing a fair comparison between the two topologies. Similar to the two-level case, this inverter also exhibits voltage drops across the switches and clamping diodes (note that clamping diode losses apply only to the three-level configurations) when compared to the theoretical waveforms illustrated in Figure 2.5. Nevertheless, the 3L3P Si-based inverter closely resembles the theoretical model, particularly in the phase-to-phase voltage levels, carrier signals, and gating signals. A comparison between the simulation results in Figure 5.5, with a switching frequency of 16 kHz, and the theoretical explanation in Figure 2.5 further confirms that the carrier and reference signals match as expected. Additionally, the phase-to-phase voltages exhibit five discrete levels in both cases, verifying the correct operation of the inverter, aside from the minor voltage ripple observed in the Si-based simulation.

As introduced in Section 2.2, the 3L3P NPC inverter employs two carrier signals in a PD-SPWM scheme. This control strategy is shown in Figure 5.5a, where the two in-phase carriers are used to generate gate signals for the four switches in each phase leg. Unlike the two-level topology, which generates three distinct output states, the three-level inverter produces five discrete voltage levels in the phase-to-phase output waveform, as seen in Figure 5.5c.

Figure 5.5b provides a detailed view of the switching behavior by displaying the gate voltages during transitions. Compared to the two-level case, the *Miller plateau* is significantly shorter, marked in the circle, compared to the longer plateau as in Figure 5.1b. This is attributed to the lower voltage stress on each switch in the three-level configuration, where each device only blocks half of the total DC-link voltage. Consequently, the energy required to traverse the *Miller* region is reduced, enabling faster transitions. Moreover, the reduced voltage swing diminishes the influence of parasitic gate-to-source capacitance, resulting in cleaner switching edges and minimal gate overshoot seen in Figure 5.5b which seems to be roughly half the amplitude noted in Figure 5.1b.

These characteristics positively impact the quality of the output waveform. The smaller voltage step size leads to a lower voltage slope (dv/dt), which helps suppress high-frequency components and reduces ripple in the phase currents. This is

clearly illustrated in Figure 5.5c, where the phase currents are more sinusoidal and exhibit fewer high-frequency oscillations compared to the two-level case shown in Figure 5.1c.

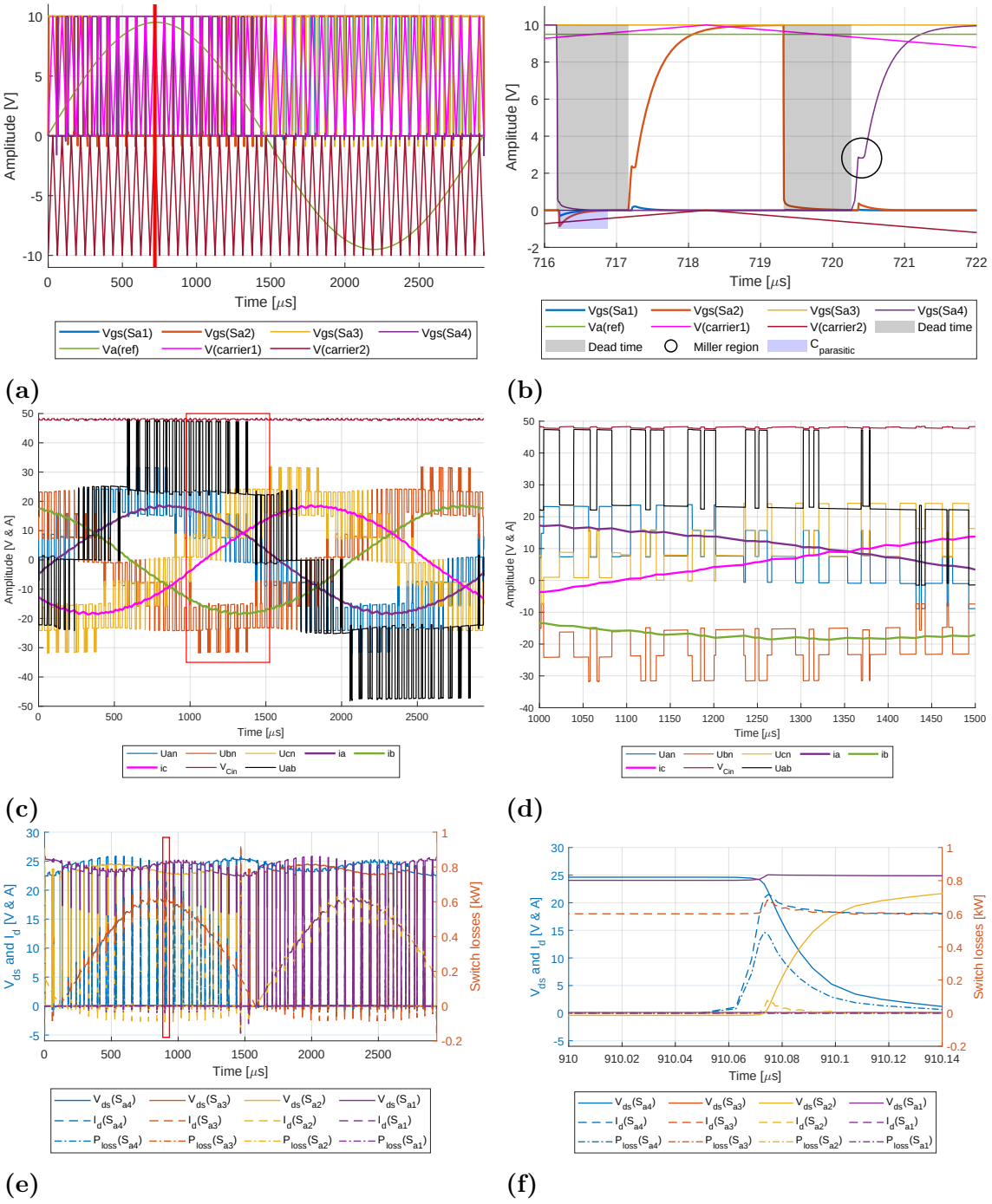


Figure 5.5: Performance of the three-phase three-level Si-based inverter at 16 kHz switching frequency. **(a)** Gate, carrier, and reference signals; **(b)** Zoomed-in view highlighting t_{dead} and Miller plateau; **(c)** Output phase voltages and currents; **(d)** Detailed view of (c); **(e)** Drain-source voltage, current, and switching losses for phase A; **(f)** Zoomed-in version of (e).

In the 3L3P inverter, the inclusion of clamping diodes introduces additional power losses that are comparable to those of the switching devices, as will be demonstrated in Table 5.1 in a later section. The voltage, current, and corresponding power losses of a representative clamping diode over one switching period are illustrated in Figure 5.6.

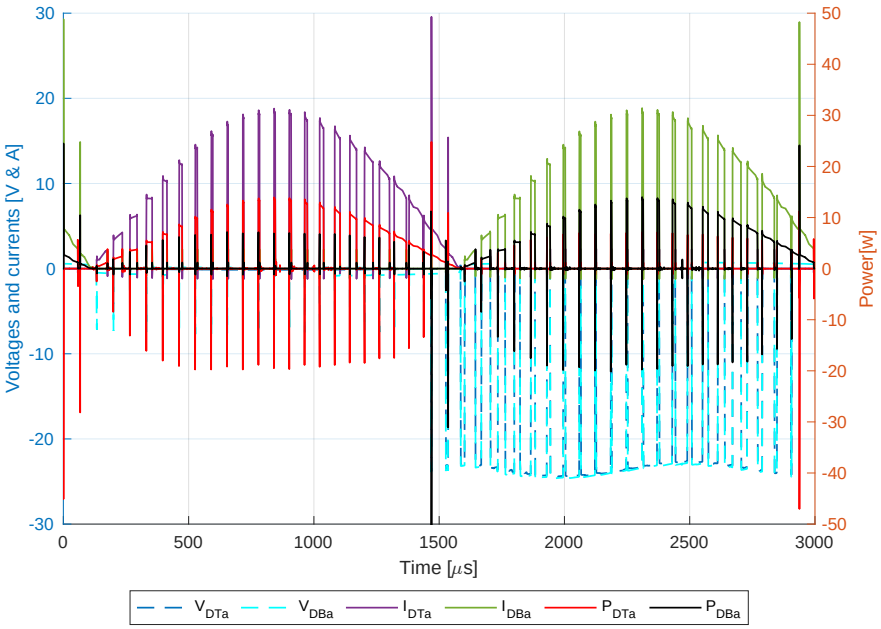


Figure 5.6: Clamping diode voltages, currents, and power-loss of 3L3P Si-based inverter. Here, DTa and DBa denote the clamping diodes in the upper and lower halves of phase A as illustrated in Figure 4.2.

5.2.2 3L3P GaN Inverter at 16 kHz switching frequency

This inverter adopts the same PD-SPWM modulation strategy as the Si MOSFET topology shown in Figure 5.5, but replaces the switching devices with GaN HEMTs. Figure 5.7 presents the simulated performance of the 3L3P GaN inverter operating at a switching frequency of 16 kHz.

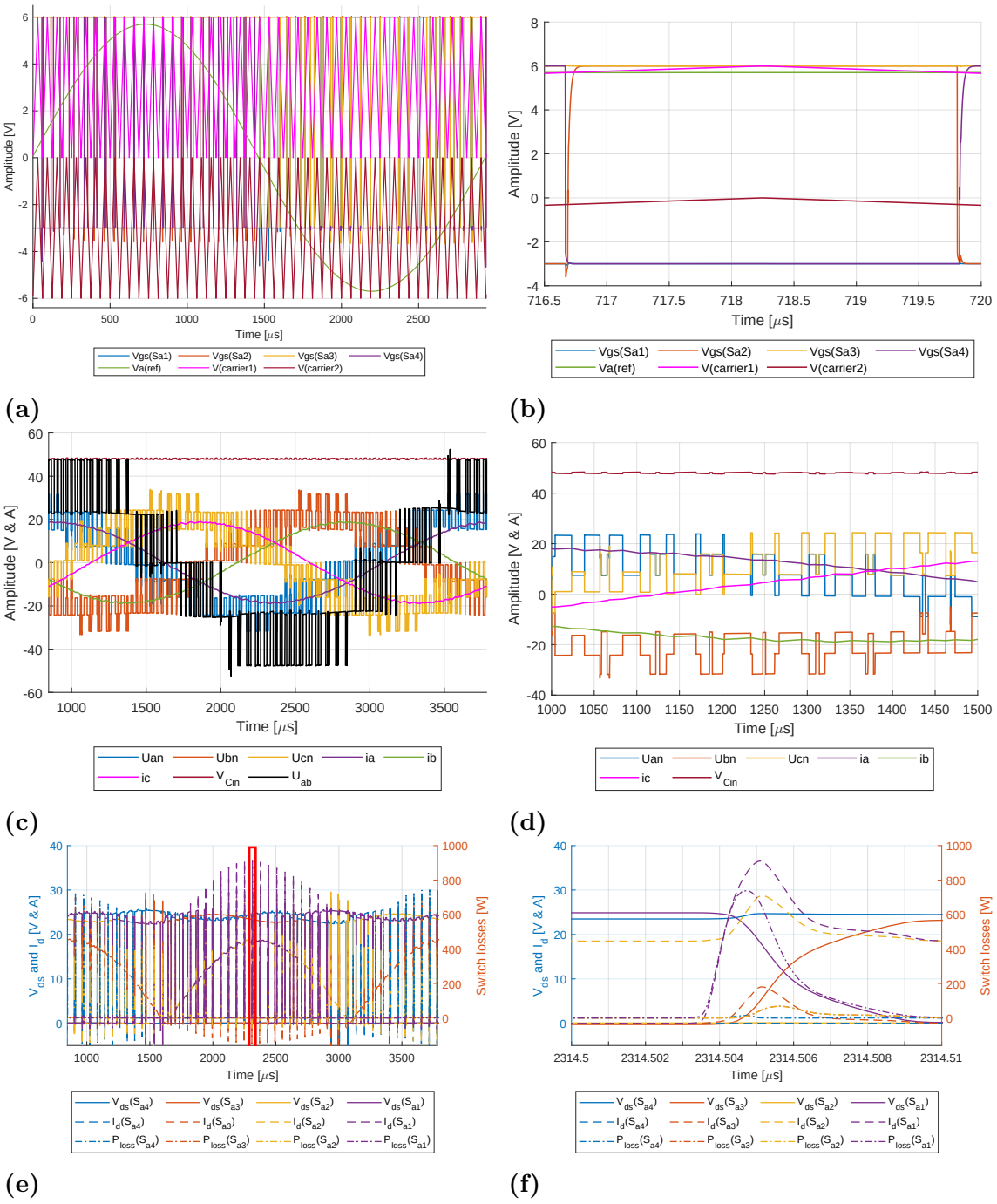


Figure 5.7: Performance of the three-phase three-level GaN-based inverter at 16 kHz switching frequency. **(a)** Gate voltages given the carrier and reference signals; **(b)** Zoomed-in version of (a); **(c)** Output phase voltages and currents; **(d)** Zoomed-in detail of (c); **(e)** Drain-source voltage, current, and losses for phase A; **(f)** Zoomed-in detail of (c).

The gate voltage behavior is illustrated in Figure 5.7a, where the t_{dead} and switching transitions closely resemble those observed in the two-level GaN inverter, since the gate turn-on resistor and the gate voltage are the same. Compared to the Si-based case in Figure 5.5b, the GaN switches exhibit substantially faster rise and fall times

(59 ns vs 4 ns), resulting in a shorter and sharper Miller plateau. This improvement is attributed to the lower gate charge and input capacitance of GaN transistors, which enable faster traversal through the Miller region and reduce switching losses. Moreover, same as in the comparison between the two and three-level Si-based inverters, the effects of the parasitic, such as gate overshoot and Miller plateau, are reduced significantly in the 3L3P GaN-based inverter compared to its two-level counterpart.

In terms of output performance, Figure 5.7c shows five-level phase voltages with clean transitions, with slightly higher overshoot compared to the Si-based counterpart in Figure 5.5c, which can be related to the GaN switches faster operation. Aside from this, the waveforms are similar to the 3L3P Si-based inverter, described in Section 5.2.1, and the theoretical one described in Section 2.2.

The zoomed-in view in Figure 5.7d highlights the phase voltages and currents. Aside from slightly increased voltage overshoots, particularly noticeable at the peaks of U_{bn} between $t = 1050$ and $t = 1100$, the phase currents do not appear to be significantly affected when compared to the Si-based counterpart shown in Figure 5.5f. This observation suggests that simply increasing the switching speed does not significantly impact the phase current waveform.

The switching dynamics in Figure 5.7e and the zoomed-in trace in Figure 5.7f further confirm the efficiency of the GaN HEMT operation. The drain-source voltage and current transitions are sharp and well-defined, with switching losses concentrated over shorter intervals, compared to the Si-based inverter, which leads to lower switching power losses.

5.2.3 3L3P GaN Inverter at 200 kHz switching frequency

The last configuration evaluated is the GaN-based three-phase three-level inverter operating at a switching frequency of 200 kHz. It employs the same PD-SPWM scheme and GaN-HEMTs as the 16 kHz version, but runs at a significantly higher switching frequency to assess the combined effects of multilevel modulation and fast-switching devices. In the time domain, the voltage and current waveforms closely resemble those of the 3L3P GaN inverter at 16 kHz, with the primary distinction being the increased switching activity. This leads to higher total switching losses due to the greater number of transitions, despite each individual event being more efficient. Since the waveform characteristics largely mirror those of the 3L3P GaN inverter at 16 kHz, and the differences align with those observed between the 2L3P GaN inverter operating at 16 kHz and 200 kHz, the waveform plots for the 3L3P GaN inverter at 200 kHz are omitted.

While higher switching frequencies typically lead to reduced ripple and improved waveform smoothness, this improvement is more pronounced at higher harmonic orders. At lower frequencies, however, the 2L3P GaN inverter at 200 kHz outperforms

the 3L3P counterpart in terms of phase current distortion. This counterintuitive result highlights the properties of three-level inverters and the influence of non-ideal clamping diodes. This topic is further analyzed in Section 5.3.3.

5.2.4 DC-Link Capacitor Voltages in 3L3P Inverters

As discussed in Section 2.3.3, due to the symmetric load and identical switching devices, the voltages across the DC-link capacitors remain stable and within acceptable limits during simulation. Consequently, a Neutral-Point Potential balancing controller is not required. However, during startup the DC-link capacitors are charged resulting in a significant voltage difference. As the scope of this thesis is restricted to steady-state, such voltage difference will be shown but not accounted for.

Figure 5.8 shows the voltage variation across the input capacitors of the 3L3P NPDC Si-based inverter operating at a 16 kHz switching frequency. As observed, the capacitor voltages rise quickly during startup and stabilize within a few milliseconds. Although minor oscillations in the voltage difference persist, they remain within the range defined by $\max(V_{c1} + V_{c2})$ and $\min(V_{c1} + V_{c2})$, and do not indicate any instability. Here, $(V_{c1} + V_{c2})$ is the voltage difference over the DC-link capacitors, where, V_{c1} is the potential difference between V_d- and ground, and V_{c2} is the potential difference between $C_{in}+$ and ground illustrated in Figure 4.2.

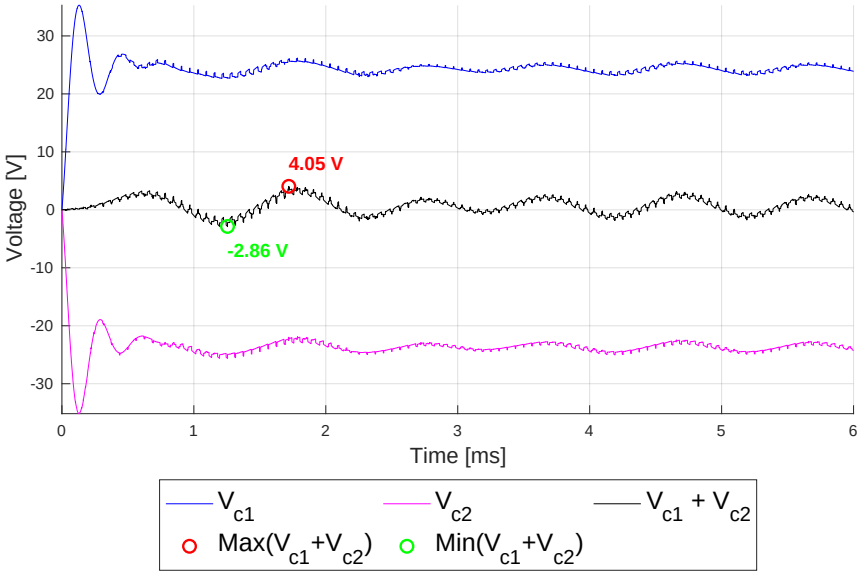


Figure 5.8: Voltages across the DC-link capacitors in the 3L3P NPDC Si-based VSI at 16 kHz switching frequency in *LTspice*. In the potential measurements, the ground is used as a reference. Potential over C_2 is V_d+ to ground, and V_d- to ground over C_1, see Figure 2.4.

5.3 Comparing 2L3P and 3L3P NPDC simulation results

Table 5.1 presents a summary of key results obtained from *LTspice* simulations, including power losses, inverter efficiency, $\text{THD}_{I_{phs}}$, and CMC levels. For the three-level inverter topology, the losses associated with clamping diodes and switches are listed separately. Furthermore, EMI performance across different inverter topologies and switching technologies is compared through plotted results. For all the simulations, the operating point of the EM is the same as described in Section 4.1.2. Due to a lack of feedback-loop, the operating point of the system changes even though the operating point of the machine is set to a constant value, and as a result, the input power varies roughly 30 Watts between the different inverters .

Table 5.1: Simulation results from LTspice for different inverter topologies and switching technologies.

Metric	MOSFET (16 kHz)	GaN (16 kHz)	GaN (200 kHz)
Two-Level Inverter			
P_{loss}(Sw/EM/tot)[W]	5.23/7.28/12.52	2.41/7.47/9.88	4.74/7.42/12.16
P_{in} [W]	567.39	571.24	571.97
Power efficiency (system)[%]	97.79	98.27	97.87
CMC (RMS/Peak) [A]	0.29 / 3.01	0.41 / 2.68	0.42 / 6.57
$\text{THD}_{I_{phs}}$ [%]	2.88	2.87	0.25
Three-Level Inverter			
P_{loss}(Sw/CDiode/EM/tot)[W]	7.09/6.8/7.67/21.57	4.17/6.92/7.97/19.07	4.96/6.93/7.94/19.83
P_{in} [W]	588.59	599.41	599.1
Power efficiency (system)[%]	96.34	96.82	96.69
CMC (RMS/Peak) [A]	0.04 / 0.64	0.16 / 0.85	0.16 / 3.27
$\text{THD}_{I_{phs}}$ [%]	1.63	1.50	0.78

Here, the power loss of electrical switches, EM, and total system losses are denoted as P_{loss} (Sw/EM/tot). Correspondingly, for the three-level inverters, the power loss of the switches, clamping diodes, EM and the total power loss of the system is denoted by P_{loss} (Sw/CDiode/EM/tot). The CMC, which is measured through the RCMC component, is calculated and described in Section 4.1.7.

From Table 5.1, it is clear that GaN-based two-level inverters have significantly lower power losses and higher efficiency compared to their silicon counterparts, this can be related to their reduced switching losses and absence of reverse recovery currents as shown in Figure 5.3b. Increasing the switching frequency of the GaN inverter from 16 kHz to 200 kHz further decreases $\text{THD}_{I_{phs}}$ substantially, improving waveform quality significantly; however, it leads to a slight increase in switching losses. In contrast, the three-level inverters provide lower CMC due to smoother voltage transitions and lower voltage stress per switch. However, they have higher overall power losses primarily due to additional switches and clamping diode conduction losses denoted by $P_{loss}(CDiode)$ in Table 5.1. The clamping diodes, essential in NPDC configurations, contribute significantly to total losses, highlighting a trade-off between lower CMC and increased power dissipation.

5.3.1 Average losses (theoretical results)

Table 5.2 presents the results derived from the theory based power loss model from Section 4.2.2 compared to the simulated results in Section 5.3. These models include conduction losses, switching losses, and diode losses (where applicable) using the notation from Section 3.2.8. The simulated conduction P_{cond} and switching P_{switch} losses are separated from the total loss P_{loss} by observing the differential gate voltage $\frac{\partial V_g}{\partial t}$ over each switch. Losses incurred as $\frac{\partial V_{gs}}{\partial t} \approx 0$, with appropriate tolerance dependent on small V_{gs} variations, are determined to be P_{cond} whilst the other losses are regarded as P_{switch}.

It is important to note that no closed-loop control mechanism is implemented in the simulations to maintain constant shaft power across all configurations, as shown for P_{in} in table 5.1. The theory based results however, assume the same $I_d(t)$ waveform through each device for both 2L3P and 3L3P, which is constructed based upon the simulated $I_d(t)$ for the 2L3P inverter. The most significant discrepancies between simulated and theoretical results appear between P_{cond} and P_D for the 3L3P inverters. However, the most significant percentage difference between theory and simulated is $\approx 6\%$ for the three-level GaN at 16kHz, indicating that the voltage/current variation due to non-constant shaft power affects the loss comparision between inverters, but not to a significant degree that it affects the overall performance analysis. Discrepancies between simulated and theoretical results for P_{switch} in both inverters could be due to charge/discharge of stray capacitances in the simulated model shown in Figures 4.1 and 4.2.

Overall, the simulated and calculated values are similar in comparison to each-other even with the known discrepancies presented. As such, the theoretical calculations are shown to accurately represent the simulated inverter configurations.

Table 5.2: Theory based (T)- and simulated (S) results of power losses (W) of semiconductors in simulated inverter configurations during the line current period $f_n = 340.4$ kHz.

	GaN (16 kHz)	**GaN (200 kHz)**	**Si (16 kHz)**
Two-Level Inverter			
P_{loss}(3.35)(3.42)(T/S)	2.37/2.41	4.84/4.74	5.28/5.23
P_{switch}(3.34)(3.41)(T/S)	0.239/0.233	2.69/2.64	1.735/1.77
P_{trans}(3.17)(T)	0.212	2.35	1.33
$P_{trans(sub)}$(3.22)(T)	0.0002	0.0011	0.0004
P_{dead}(3.25)(3.26)(T)	0.0266	0.332	0.192
P_{rr}(3.28)(T)	0	0	0.212
P_{cond}(3.33)(3.40) (T/S)	2.14/2.17	2.15/2.10	3.55/3.47
$P_{cond,on}$(3.23)(T)	2.14	2.15	3.55
$P_{cond,off}$(3.24)(T)	≈0	≈0	≈0
Three-Level Inverter			
P_{loss}(3.39)(3.46) (T/S)	10.88/11.09	11.74/11.89	14.07/13.90
P_{switch}(3.37)(3.44) (T/S)	0.0719/0.0702	0.878/0.881	0.398/0.414
P_{trans}(3.17)(T)	0.0414	0.504	0.246
$P_{trans(sub)}$(3.22)(T)	0.0001	0.0012	0.0006
P_{oss}(3.18)(T)	0.0109	0.134	0.0164
P_{qoss}(3.19)(T)	0.0195	0.239	0.0284
P_{rr}(3.28)(T)	0	0	0.106
P_{cond} (3.36)(3.43) (T/S)	3.87/4.11	3.87/4.08	6.56/6.68
$P_{cond,on}$(3.23)(T)	3.87	3.87	6.56
$P_{cond,off}$(3.24)(T)	≈0	≈0	≈0
P_D(3.38,3.45) (T/S)	6.94/6.92	6.98/6.93	7.11/6.8
P_{Dcond}(3.31)(T)	6.94	6.98	7.11
$P_{Doff,C}$(3.32)(T)	0.0006	0.0072	0.0006

Comparing the **GaN (16 kHz)** and **Si (16 kHz)** configurations shows that GaN HEMTs, compared to Si MOSFETs, have lower P_{switch} due to reduced C_{iss}, C_{oss}, Q_g ,t_{dead} and no Q_{rr}. GaN HEMTs also provides a reduced P_{cond} as $R_{ds(on)}$ is lower compared to Si MOSFETs[2]. Similarly, comparing the **GaN (200 kHz)** against **Si (16 kHz)** the P_{loss} for GaN-HEMTs is lower compared to Si-MOSFETs even at significant increase in switching frequency and P_{switch}. This is due to the reduced $R_{ds(on)}$ for GaN HEMTs, in theory, even if the GaN-HEMTs and Si-MOSFETs would have similar $R_{ds(on)}$ and P_{cond}, the P_{loss} would be comparatively similar due to relatively low P_{switch} for GaN-HEMTs at high switching frequencies. Generally, GaN-devices compared to Si-based devices in inverter configurations provide a significant reduction in switching losses [55], which is corroborated with P_{switch} for 2L3P GaN inverter being 86.21% lower compared to the P_{switch} in 2L3P Si. Indicating that GaN-HEMTs are optimally used at high switching frequencies.

[2]Note that $R_{ds(on)}$ for *LTspice* model is incongruent with the datasheet of the same device

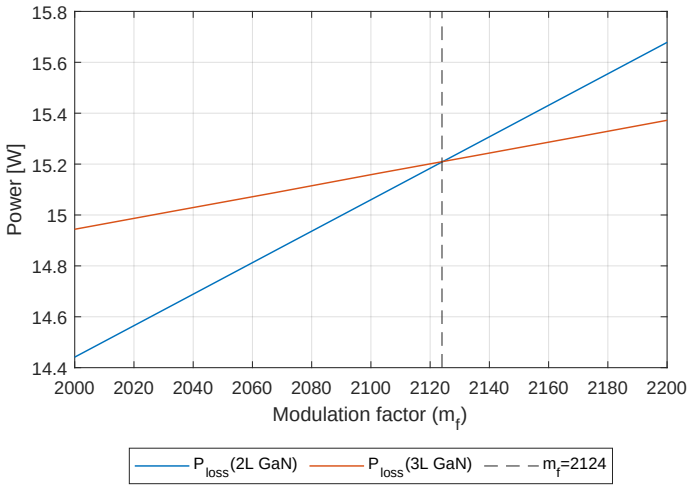


Figure 5.9: Semiconductor loss model determining P_{loss} for two- and three-level GaN inverters across iterative m_f

Observing the Table, P_{loss} is considerably higher for three-level compared to two-level configurations. This is due to the three-level inverter design, which cause half of the transistors to conduct continuously during half of the line current period, increasing P_{cond}. The Schottky clamping diodes used also results in additional P_D loss. However, P_{switch} is 69.92% lower for 3L3P GaN compared to 2L3P GaN inverters. This indicates that at a sufficiently high switching frequency, the P_{loss} for two-and three-level inverters are approximately equal. In Figure 5.9 the semiconductor loss model is used to find the m_f where $P_{loss,2GaN} = P_{loss,3GaN}$. Resulting in three-level GaN dissipating less power than two-level GaN as $f_c > 723$ kHz and $f_n = 340.4$ Hz.

5.3.2 EMI performance

The relative EMI comparisons of the different inverter topologies and different switching frequencies are presented in Figures 5.10.

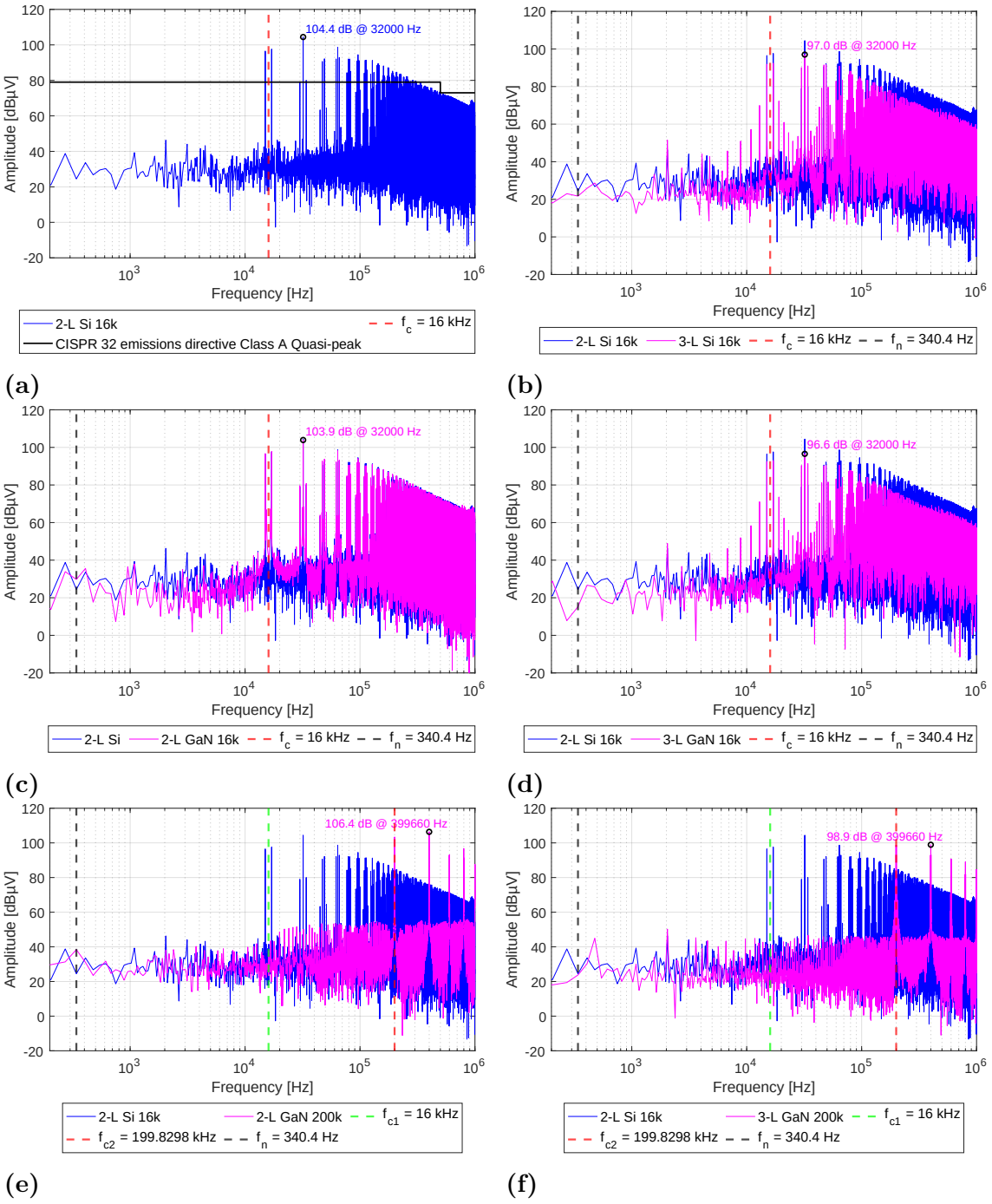


Figure 5.10: EMI comparisons of different inverter topologies at various switching frequencies in dBμV. For each plot, the amplitude of the highest harmonic is marked with a black circle and is described in terms of amplitude and frequency. The color of the text indicates which plot the maximum amplitude is marked on. **(a)** is the reference inverter (two-level Si at 16kHz) with the CISPR 32 emissions directive Class A Quasi-peak limits shown by the black plot, compared with: **(b)** two-level GaN inverter at 200kHz, **(c)** two-level GaN inverter at 16kHz, **(d)** three-level Si inverter at 16kHz, **(e)** three-level GaN inverter at 16kHz, and **(f)** three-level GaN inverter at 200kHz.

The EMI performance of each inverter configuration was evaluated by performing an FFT on the output voltage measured through the LISN, as described in Section 2.6. The results are shown in Figure 5.10, with the two-level Si inverter operating at 16kHz serving as the baseline reference. As illustrated in Figure 5.10a, all inverter configurations exceed the CISPR 32 Class A quasi-peak EMI limits. This can be attributed to the lack of sufficient filtering, as previously discussed in Section 2.3. Despite this, the comparison provides useful insight into the relative conducted EMI characteristics of the different inverter topologies and switching technologies.

Figure 5.10a illustrates the EMI spectrum of the reference inverter including the CISPR 32 emissions directive Class A Quasi-peak limits. When comparing the reference inverter with the two-level GaN inverter at the same frequency (16 kHz) in Figure 5.10c, it is observed that the GaN inverter exhibits similar EMI characteristics, indicating limited EMI reduction from simply changing the transistor technology at this frequency.

However, increasing the switching frequency of the GaN inverter to 200 kHz significantly alters the EMI behavior, as shown in Figure 5.10e. The EMI spectrum shows that the harmonics are moved towards higher frequencies according to (2.4). Furthermore, it can be noted that the maximum amplitude of the harmonic is at double the switching frequency and the side-bands of the switching frequency have significantly lower amplitudes compared to the 16 kHz counter part in Figure 5.10c.

Comparing the two-level reference inverter to the three-level Si inverter at 16 kHz in Figure 5.10b, the EMI spectrum demonstrates a clear advantage for the three-level configuration, with lower harmonic magnitudes across the frequency range. This result is due to the additional intermediate voltage level in the three-level inverter, which leads to smoother switching transitions and subsequently reduces EMI emissions. This result is further confirmed by [56, 57]. The EMI spectrum of the three-level GaN inverter at 16 kHz (Figure 5.10d) further confirms this advantage, showing similar performance as its Si-based counterpart. This indicates that at moderate frequencies, the three-level topology effectively reduces EMI independently of transistor technology.

Finally, Figure 5.10f shows the three-level GaN inverter operated at 200 kHz. Same as in the case of 2L3P inverter at 200 kHz switching frequency in Figure 5.10e, the harmonics are moved further into higher frequencies.

These results confirm that using a three-level topology substantially reduces EMI, particularly at moderate switching frequencies. GaN technology compared to Si primarily provides advantages at high operating frequencies to minimize distortion on the output waveform.

5.3.3 Phase Current Spectrum

To explain the unexpected result observed in Table 5.1, where the $\text{THD}_{I_{phs}}$ of the two-level GaN inverter is lower than that of the three-level GaN inverter at a switching frequency of 200kHz, the phase current spectra is analyzed. Figure 5.11 shows the FFT spectra of the phase-a current for various inverter topologies and switching frequencies.

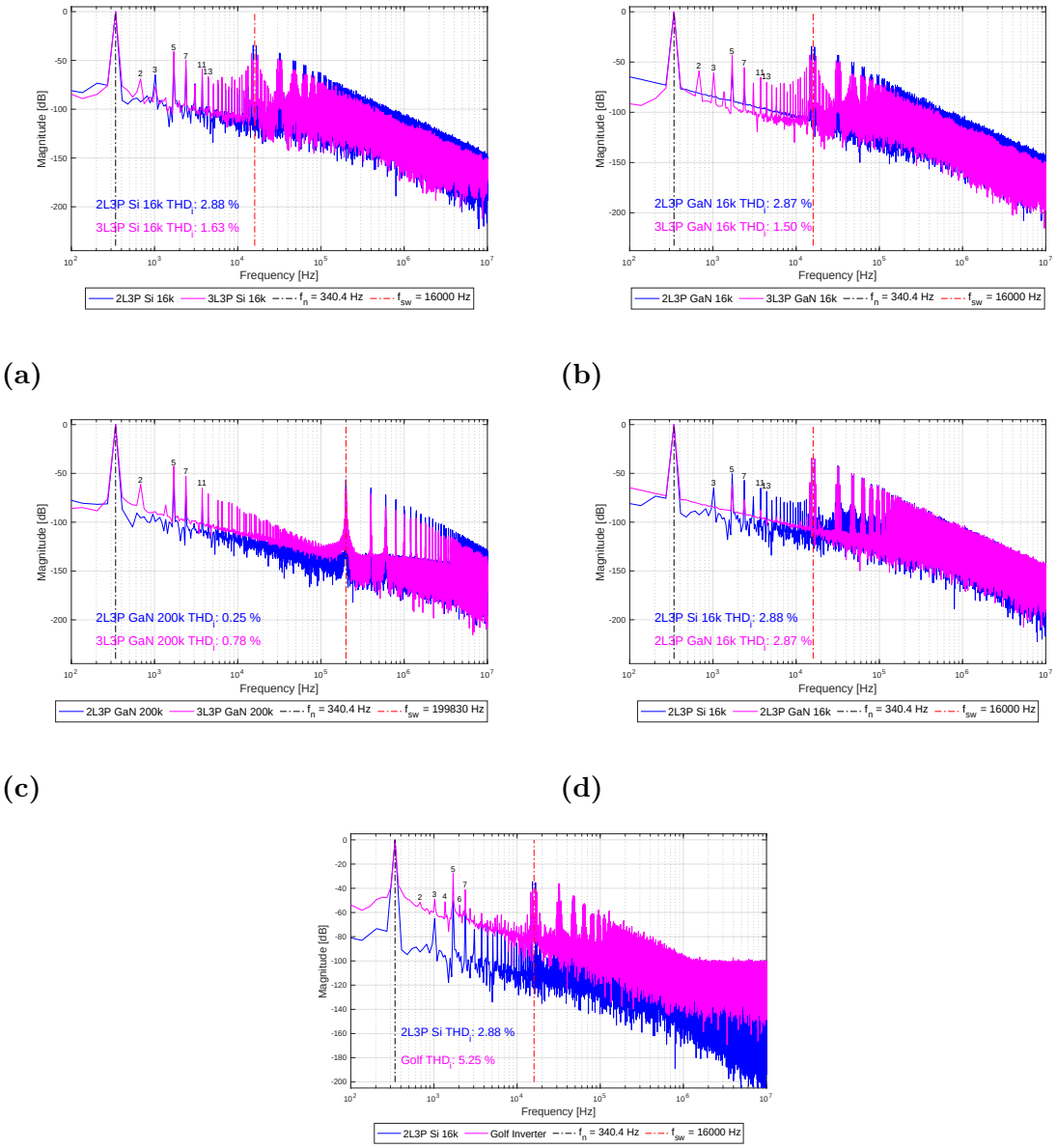


Figure 5.11: Comparison of frequency spectra of phase-a current for different inverter configurations. In each plot, the harmonics of the fundamental frequency are marked with the corresponding harmonic number. (a) Two-level vs. three-level Si inverters at 16 kHz, (b) Two-level vs. three-level GaN inverters at 16 kHz, (c) Two-level vs. three-level GaN inverters at 200 kHz. (d) Two-level Si inverter vs two-level GaN inverter at 16 kHz (e) Two-level Si inverter vs the existing inverter (Golf).

In Figure 5.11a, the two-level and three-level Si inverters operating at $f_c = 16$ kHz are compared. Observing the figure, the three-level Si inverter exhibits lower harmonics beyond the switching frequency compared to the two-level case. Although the three-level introduces slightly more low-frequency distortion, its better high-

frequency attenuation results in an overall lower $\text{THD}_{I_{phs}}$ of 1.63% compared to 2.88% for the two-level inverter.

In Figure 5.11b, the comparison between two-level and three-level GaN inverters at 16 kHz is shown. Due to the faster switching transitions of GaN devices, the two-level GaN inverter already demonstrates a relatively clean spectrum. The three-level GaN inverter achieves slightly better high-frequency attenuation but shows marginally increased distortion around low-order harmonics. Nevertheless, the three-level case maintains a lower $\text{THD}_{I_{phs}}$ of 1.50% compared to 2.87% for the two-level case.

In Figure 5.11c, both inverters are operated at a switching frequency of roughly 200 kHz. Both spectra exhibit a dominant peak at the fundamental frequency ($f_n = 340.4$ Hz). However, the two-level GaN inverter displays significantly lower low-frequency harmonic content, resulting in a very low $\text{THD}_{I_{phs}}$ of 0.25%. In contrast, the three-level GaN inverter shows noticeably low-frequency distortion between the fundamental frequency and the switching frequency, and lower high-frequency harmonics above the switching frequency. However, the low frequency components have greater amplitudes, yielding a higher $\text{THD}_{I_{phs}}$ of 0.78% for the three-level inverter.

Figure 5.11d illustrates the phase spectrum of the phase-current for 2L3P Si-based inverter and 2L3P GaN-based inverter at 16 kHz switching frequency. As noted, the 2L3P GaN-based inverter has significantly lower distortion below the switching frequency, which can be related to the reduced deadtime and voltage loss over the switches of this inverter. From the switching frequency and above, the two inverters have very similar harmonics. This leads to the $\text{THD}_{I_{phs}}$ of the GaN-based inverter being 2.87% and for the Si-based inverter 2.88%.

Finally, in Figure 5.11e, the 2L3P Si inverter's phase-current spectrum is compared to the existing 2L3P inverter (Golf), which drives the water pump. The phase current spectrum for the existing inverter was obtained by performing an FFT analysis of the measured phase current. The result shows that the existing inverter has much higher distortion across the spectrum, with a $\text{THD}_{I_{phs}}$ of 5.5% compared to 2.88% in the simulated case.

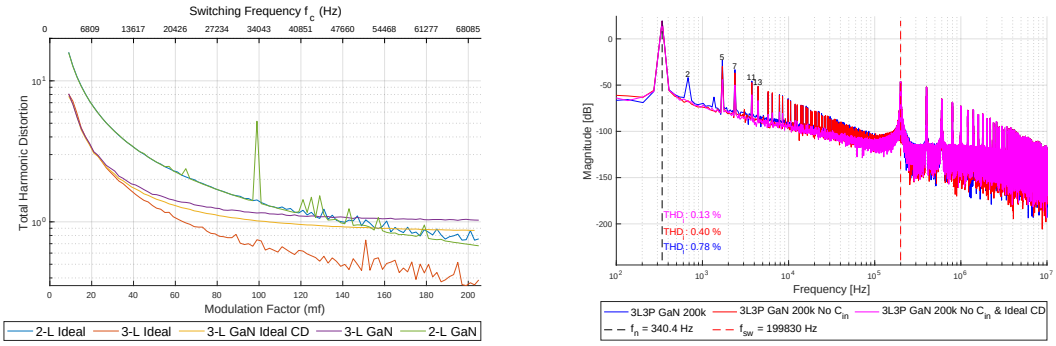
As explained in Section 2.1 in (2.4), choosing the modulation factor as an odd number results in the even harmonic elimination. This can clearly be noted across all the figures in Figure 5.11, where only odd harmonics have clear peak values. This is except for the 2nd harmonic, which is the only even harmonic visible in the figure. The 2nd harmonic usually originates from the voltage drop across the switches and the dead time [58]. The effect of these on the output voltage and thereby their effect on the phase current depends on the sign of the current and therefore results in a 2nd harmonic component..

To complement the spectral analysis, Figure 5.12a presents the evolution of $\text{THD}_{I_{phs}}$ as a function of the modulation factor (m_f) for both two-level and three-level GaN

inverters. Furthermore, the effects of clamping diodes and DC-link capacitors are illustrated in Figure 5.12b. The descriptions of the legends in the following figures are:

2-L Ideal	2L3P inverter with ideal switches, excluding parasitic elements.
3-L Ideal	3L3P NPDC inverter with ideal switches and clamping diodes, excluding parasitic elements.
3-L GaN Ideal CD	3L3P GaN-based inverter with ideal Clamping Diode (CD).
3-L GaN	3L3P GaN-based inverter.
2-L GaN	3L2P GaN-based inverter.

Furthermore, *No* C_{in} indicates the absence of DC-link capacitors, meaning the inverter is supplied directly by voltage sources, each providing half of the total DC-link voltage. *Ideal Clamping Diode (CD)* implies that the clamping diodes exhibit no forward voltage drop or on-resistance.



(a) **(b)**

Figure 5.12: (a) Comparison of $\text{THD}_{I_{phs}}$ of the phase-a current as a function of modulation factor for two-level and three-level GaN inverters. (b) show the effects of input capacitance and clamping diode on the phase current spectrum of a three-level NPDC inverter.

Note: In Figure 5.12a, the observed spikes (for example, at mf=99 for the 2-L GaN curve) are primarily caused by numerical tolerances in the simulations. Reducing the tolerance further leads to the error *Analysis Failed: iteration limit reached* and generates a significantly larger amount of data. Additionally, since the scale in the mentioned figure is logarithmic, even small variations appear exaggerated. Rounding errors or numerical errors may also contribute to these spikes.

Examining Figure 5.12a, it is observed that at low modulation indices ($m_f < 130$), the three-level GaN inverter consistently exhibits lower $\text{THD}_{I_{phs}}$ compared to its two-level counterpart. This behavior aligns with theoretical expectations, as the multilevel voltage waveform reduces the voltage steps, thereby decreasing harmonic content, as discussed in Section 2.7.

However, when the modulation index exceeds $m_f > 130$, the $\text{THD}_{I_{phs}}$ of the three-level inverter surpasses that of the two-level inverter. Ideally, a three-level inverter should maintain a lower $\text{THD}_{I_{phs}}$ across the entire switching frequency range. The deviation from this ideal behavior is attributed to the DC-link capacitor voltage imbalance, as in Figure 5.8, and detailed in Section 2.3.3, as well as to the non-ideal characteristics of the clamping diodes. Simulations confirm that replacing the clamping diodes with ideal components and substituting the DC-link capacitors with voltage sources significantly improves $\text{THD}_{I_{phs}}$ performance, resulting in better attenuation of current distortion, as shown in Figure 5.12b. Furthermore, making the three-level inverter completely ideal reduces the $\text{THD}_{I_{phs}}$ further at higher modulation indices, so that it outperforms the two-level inverter for all the simulated modulation indices, even the ideal two-level inverter.

Reference [59] also investigates the influence of switching frequency on $\text{THD}_{I_{phs}}$ for two- and three-level NPC inverters, concluding that $\text{THD}_{I_{phs}}$ generally decreases with increasing switching frequency. However, their study considers a maximum switching frequency of only 12 kHz, in contrast to the 68 kHz used in Figure 5.12a. Consequently, the effects of DC-link capacitor imbalance and clamping diode non-idealities are less pronounced in their results.

These results demonstrate that an increase in the number of voltage levels or switching frequency does not directly correlate to improved current quality. Particularly at high switching frequencies, non-ideal effects such as clamping diode behavior, t_{dead} effects, and voltage imbalance of the DC-link capacitors can result in higher harmonic distortion for multilevel topologies.

5.3.4 Electrical Machine model validation

To validate the performance of the EM model independently of inverter effects, it is first driven by a three-phase sinusoidal voltage sources. Each phase maintains the same amplitude and phase relationship as defined in (4.1). This setup ensures that the evaluation focuses solely on the EM model's behavior, free from any influence introduced by the inverter. For comparison, the EM model is subsequently driven by the 2L3P Silicon-based inverter, with the same fundamental phase voltage amplitude as specified in (4.1).

The phase currents and back-EMFs are compared with theoretically calculated values, and the resulting waveforms are analyzed. Table 5.3 presents both the theoretical values from (4.1) and the actual values obtained from the model using Fourier analysis. In Table 5.3, the row labeled *Simulated (sine wave generator)* refers to the scenario where the EM model is fed directly by ideal sinusoidal sources. Meanwhile, *Simulated (2L3P)* corresponds to the case where the EM model is powered by the 2L3P inverter, using a modulation strategy that matches the fundamental amplitude described in (4.1).

Table 5.3: Performance evaluation of PMSM: Calculated vs. simulated values of phase voltage, back EMF, and current in steady-state

Source	$\hat{U}_{an}\angle\theta_u$	$\hat{E}_{an}\angle\theta_e$	$\hat{i}_a\angle\theta_i$	$\theta_u - \theta_e$	$\theta_u - \theta_i$	$\theta_e - \theta_i$
Calculated	22.35 ∠110.74°	20.21 ∠90°	17.64 ∠90°	20.74°	20.74°	0°
Simulated (sine wave generator)	22.35 ∠110.74°	20.15 ∠131.47°	17.63 ∠132.91°	−20.73°	−22.17°	−1.44°
Simulated (2L3P)	21.62 ∠110.22°	20.21 ∠131.48°	17.40 ∠125.94°	−21.26°	−15.72°	−5.54°

In the simulation with the two-level inverter, the input voltage, V_d, was set to the value specified in (2.51), and the phase of the reference voltage was set to the calculated θ_u. As observed, the q-axis current ($\hat{i}_a$ in Table 5.3) has the same phase as the back EMF ($\hat{E}_{an}$ Table 5.3), and the phase difference between these two and the phase voltage is approximately 20.74°. This difference remains relatively constant in the case of simulation using sine wave generators. However, in this scenario, the current and the back EMF lead the phase voltage. This can be attributed to how *LTspice* handles the angle in the *Fourier* transform. As evident from the waveforms presented in Figure 5.13, the phase voltage indeed leads as expected. In the case of the two-level inverter, additional errors accumulate due to voltage drop across the LISN and transistors, as well as the dead time, which has the most significant impact on the phase voltage amplitude, which affects the current magnitude and angle.

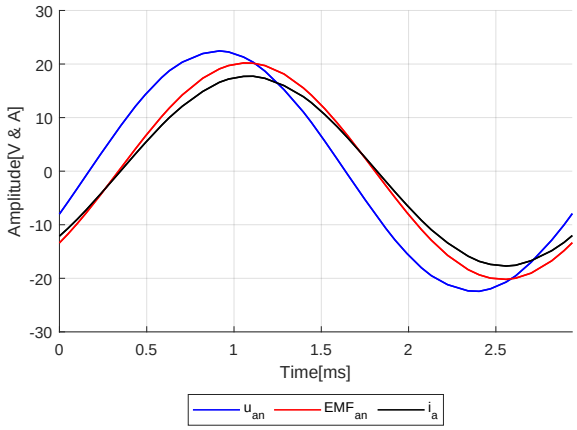


Figure 5.13: PMSM phase voltage, back EMF, and current waveforms when fed with three sinusoidal voltage generators

5.4 Cost Comparison

This section presents a cost analysis of the simulated inverter configurations, in accordance with the methodology outlined in Section 4.4. The assessment includes both the initial cost and the operational costs associated with each topology. To provide a fair basis for comparison; the discrepancy of P_{in} presented in table 5.1 is addressed such that, the power losses of each inverter configuration is scaled to correspond to a uniform input power level, defined by the Si-based two-level inverter case ($P_{\text{in}} = 567.39$ W). This normalization assumes that each inverter operates with a constant efficiency at its respective operating point. Using this

efficiency, the expected power loss for each inverter is recalculated based on the fixed input power of $P_{\text{in}} = 567.39$ W. Table 5.4 presents the unscaled and scaled power losses, estimated component costs, and derived operational costs for each inverter. Additionally, break-even time, defined as the period required to offset the higher initial cost of advanced configurations through reduced operational expenses, is also calculated.

Table 5.4: Comparison of cost and power losses for each inverter configuration, including scaled losses based on a normalized input power of $P_{extin} = 567.39$ W. The efficiency represents the system efficiency, which is the combined inverter and EM. The losses P_{motor}, which are only due to leakage inductance, are explained in Section 2.7.2.

Inverter	P_{inv} [W]	P_{motor} [W]	P_{loss} [W]	Scaled P_{loss} [W]	Efficiency [%]	Init Cost [SEK]	Cost-in-Use [SEK/h]	Break-Even [years]
GaN_2L_16k	2.4055	7.4701	9.8756	9.8091	98.27	253.59	0.0122	6.02
GaN_2L_200k	4.7379	7.4238	12.1616	12.0643	97.87	253.59	0.0150	36.02
Si_2L	5.2324	7.2847	12.5171	12.5171	97.79	76.41	0.0155	Reference
GaN_3L_16k	11.0948	7.9720	19.0668	18.0484	96.82	594.17	0.0224	-
GaN_3L_200k	11.8885	7.9403	19.8288	18.7793	96.69	594.17	0.0233	-
Si_3L	13.8955	7.6743	21.5697	20.7928	96.34	239.82	0.0258	-

From a cost-effectiveness standpoint, the two-level GaN-based inverter operating at 16 kHz emerges as the most favorable solution. It offers a well-balanced trade-off between efficiency, power quality, and economic viability. Notably, it exhibits the lowest cost-in-use and a relatively short payback period, making it an attractive option for applications that demand both high performance and long-term affordability.

It is important to note that all inverter configurations utilize identical DC-link capacitors. However, due to the inherently lower EMI of the three-level inverters, they require less filtering on the DC-link side. As a result, the initial cost of the input filter for the three-level topologies is lower, a factor not accounted for in the current cost analysis. Moreover, increasing the switching frequency further reduces the size and cost of the input filter, contributing to additional potential savings in the initial investment.

Overall, the results demonstrate clear trade-offs between complexity, cost, efficiency, and power quality. GaN-based two-level inverters at moderate switching frequencies provide a balanced improvement for all performance metrics, whereas three-level configurations are beneficial mainly when CMC reduction is prioritized.

6
Discussion and conclusion

6.1 Discussion

The following sections discusses insight, discrepancies, and difficulties present in analyzing the performance metrics of the inverter configurations.

6.1.1 LTspice as a Simulation Tool

LTspice proved to be a robust and accessible tool for circuit-level simulations, enabling detailed waveform analysis and basic performance evaluation of inverter configurations. However, several limitations impact its modeling accuracy. Firstly, the component models in *LTspice* do not fully represent real-world behavior. Phenomena such as temperature dependence, thermal coupling, and detailed parasitics are either simplified or entirely omitted. In some cases, even the parameter values differ from those provided in manufacturer datasheets, leading to overly optimistic estimations of system performance. For example, the GaN HEMTs used in the simulations were modeled with an on-resistance of 4.4 mΩ, whereas the corresponding datasheet specifies a typical value of 7 mΩ. This discrepancy can significantly affect the accuracy of power loss and efficiency calculations.

Secondly, *LTspice* lacks the flexibility required for simulating complex systems such as electrical machines with non-linear dynamics or external controllers. Although the steady-state behavior of the PMSM was approximated using an RL model with sinusoidal back-EMFs, this approach is inadequate for dynamic or real-time analyses. For such cases, simulation platforms like *MATLAB/Simulink* offer better support.

Thirdly, *LTspice* employs a dynamic data sampling frequency, which varies throughout the simulation. While this approach reduces unnecessary data and conserves memory, it complicates post-processing in tools like *MATLAB* that require uniformly sampled data to perform *FFT*. Resampling can lead to information loss and reduced signal fidelity, particularly when analyzing fast transients or high-frequency content.

Furthermore, as model complexity and the number of components increase, simulation times rise significantly, introducing a trade-off between accuracy and practicality. To manage simulation duration, several simplifications were implemented. These include omitting the equivalent series inductance of the input capacitors and reducing the input filter capacitance to half of its real-world value. While these

adjustments considerably reduced simulation time, they also compromised model fidelity, particularly with respect to EMI behavior and current ripple characteristics. As a result, the simulations exhibit less effective EMI attenuation compared to what would be expected in a more accurate physical implementation.

6.1.2 Inverter Performance and Modeling Accuracy

The inverter performance observed in *LTspice* aligns well with theoretical expectations in terms of waveform generation and switching behavior. However, the simulated inverter efficiency often exceeding 99%, is slightly higher than what would be observed in a practical implementation. Real-world systems typically operate at 98%, depending on the designed system and topology [1]. This discrepancy is primarily due to idealized assumptions. The power source in simulations is considered ideal: free from harmonics and capable of providing infinite current. In real systems, source distortion and impedance contribute to additional distortions in the inverter output [60].

Furthermore, parasitic effects were only partially included. For example, stray capacitances were estimated based on the two-level PCB layout, while frequency-dependent behavior and temperature sensitivity were ignored. Capacitance values were fixed, even though real capacitive parasitics vary with switching frequency and surrounding circuit dynamics. Furthermore, the parasitic inductances were ignored, which could lead to resonance and increase the EMI if included.

The EM model is ideal and does not include any parasitics or asymmetries, nor does it consider loss parameters such as iron and friction losses. This naturally results in a more efficient system, which may further extend the break-even time between the different inverter types. The inclusion of leakage losses, although insufficient, represents a step in the right direction.

Despite these limitations, the comparative results remain valid and insightful. The relative differences between Si and GaN switches, as well as between two-level and three-level topologies, clearly illustrate performance trends. GaN inverters consistently demonstrated lower switching losses and improved $\text{THD}_{I_{phs}}$, particularly at higher switching frequencies, which aligns with the theoretical advantages of WBG transistors.

6.1.3 Evaluation of theoretical model

Although the semiconductor loss model remains consistently accurate to the simulated results at different frequencies, the simulation as well as the model assume an ideal $R_{ds(on)}$. To more accurately model the characteristics of the inverter configurations to implemented the circuit, a thermal model would be required to describe the dynamic behavior of the physical devices. Additionally, the parameters used in the semiconductor loss model are based on the datasheet values for the devices, except

[1] Some inverters designed by *Aros AB* operate at such efficiencies

for $R_{ds(on)}$ for GaN HEMTs as explained in Section 4.2.2. This discrepancy could possibly be due to the lack of proper thermal modeling, as such all results based on conduction losses for GaN could differ significantly compared to an implemented circuit. Increased accuracy could also be achieved by modeling displacement currents from stray capacitances present in the circuit.

6.1.4 Insights from 2L3P and 3L3P NPDC VSI Topology Comparison

One notable result is that although the same power switches were used across different topologies, the effective power ratings of the inverters varied. The three-level topology inherently supports higher DC-link voltages and thus offers greater output power capacity. This advantage was not exploited in the presented case study due to the fixed low-voltage PMSM application, but it implies that the three-level GaN inverter offers greater scalability and flexibility for high-power applications.

An interesting observation is that the $\text{THD}_{I_{phs}}$ of the three-level GaN inverter plateaus beyond a certain switching frequency. This behavior is primarily attributed to the use of clamping diodes and the voltage imbalance of the DC-link capacitors. Upon replacing these with ideal clamping diodes, and feeding the inverter with two voltage sources, the $\text{THD}_{I_{phs}}$ decreases significantly.

As noted in Table 5.1, the clamping diodes exhibit relatively high power losses. Replacing these diodes with electrical switches, such as GaN HEMTs or Si MOSFETs, can potentially reduce the overall inverter losses and $\text{THD}_{I_{phs}}$. Moreover, the dead time and voltage drop across the switches differ depending on the switch technology. This results in variations in the phase voltage amplitude, and consequently, the operating point of the electric machine (EM) differs for each topology and switch type.

To ensure a fair comparison, a viable solution is to first adjust the input voltage so that all inverters produce the same phase voltage amplitude. Once this condition is met, meaningful comparisons between different inverter topologies and switch technologies can be conducted.

6.1.5 Conclusion

This thesis presented a comparative study of two-level and three-level inverter topologies using Si-MOSFETs and GaN HEMTs. The analysis focused on performance metrics including power loss, $\text{THD}_{I_{phs}}$, EMI, and CMC, with a practical application in PMSM-based data center cooling systems.

Simulations in *LTspice* demonstrated that two-level GaN inverters, particularly at a switching frequency of 16 kHz, offer the most favorable balance between efficiency, waveform quality, and cost. The switching loss of two-level GaN at 16 kHz is 86.21% lower compared to the two-level Si switching loss at 16 kHz. The inverter achieves a

system efficiency exceeding 98%, a $\text{THD}_{I_{phs}}$ as low as 2.79%, and a break-even time of 6 years. This implies that the energy savings accumulated over 6 years offset the additional production cost, making them an ideal choice for compact, low-cost applications.

The three-level NPDC GaN inverter, although more complex and costly, excels in reducing EMI and CMC. It also offers superior waveform shaping at moderate switching frequencies. However, due to diode- and conduction-related losses, its power efficiency at the simulated switching frequencies did not exceed that of the two-level GaN inverter (96.69% vs. 97.87% at a switching frequency of 200 kHz). The switching power loss of the three-level GaN however, is comparatively 69.92% lower compared to the switching loss of the 2L3P GaN inverter. Indicating that for a switching frequency > 723 kHz, a three-level NPDC GaN would be more efficient compared to a two-level GaN.

The cost analysis confirmed that the additional cost of GaN devices is justified in long-term use due to lower operational losses. Nevertheless, for cost-sensitive applications where EMI and CMC are not critical, the two-level GaN inverter operating at 16 kHz remains the optimal choice.

Wide Bandgap devices offer significant advantages in terms of efficiency and enable the use of higher switching frequencies. Although the 2L3P GaN-based inverter involves a higher initial cost, the energy savings over time compensate for this expense. On the other hand, 3L3P inverters, while also associated with a high initial cost, support higher power ratings as they can withstand twice the voltage of their two-level counterparts. Therefore, 3L3P inverters are suitable for a broader range of applications.

6.1.6 Ethics

The system analyzed in this thesis operates at low DC input voltages and as such, is classified as a low-risk system in terms of electrical safety. Nonetheless, appropriate safety precautions must always be followed when handling power electronic circuits, particularly during prototyping, debugging, and measurement phases. These include the use of personal protective equipment, proper isolation, and grounding procedures.

From an environmental ethics standpoint, the findings of this thesis support the transition toward more energy-efficient inverter designs. The use of GaN-based switches significantly reduces switching losses, enabling higher power density and efficiency. This translates to reduced energy consumption and, by extension, lower carbon emissions during operation. Especially in high-duty applications like data center cooling systems, even modest efficiency improvements can result in substantial cumulative energy savings.

Furthermore, increased switching frequency enabled by WBG devices allows for the

downsizing of passive components such as inductors and filters. This contributes to more compact inverter designs and reduces the quantity of raw materials required, especially copper and magnetic core materials, thereby lowering the environmental footprint of manufacturing and logistics.

However, it is also important to acknowledge that GaN devices currently involve higher production complexity and cost, with material sourcing and end-of-life recycling still maturing compared to traditional Si devices. Ethical considerations in future work should address the full life cycle of these components, including sustainable sourcing, recyclability, and supply chain transparency.

In conclusion, while this thesis promotes the adoption of advanced semiconductor technologies for sustainability gains, ethical engineering demands that such improvements also consider safety, environmental impact, and material resource management holistically.

6.2 Future work

While this thesis provides a simulation-based evaluation of two- and three-level inverters using both Si-MOSFETs and GaN HEMTs, several areas remain open for future investigation:

- **Hardware Validation:** The entire analysis is based on *LTspice* simulations and analytical modeling. Future work should involve building and testing hardware prototypes for both two-level and three-level GaN inverters. This would allow validation of efficiency, $\text{THD}_{I_{phs}}$, and EMI performance under realistic operating conditions, and uncover practical issues such as PCB layout effects, thermal constraints, and noise coupling paths.

- **Clamping Diode Optimization:** The three-level inverter's efficiency was shown to suffer due to losses in the clamping diodes. Replacing these passive diodes with actively controlled GaN-FETs or Si-MOSFETs could potentially reduce conduction and switching losses and improve $\text{THD}_{I_{phs}}$ at high frequencies. This modification could also enable smart balancing of DC-link voltages.

- **$\text{THD}_{I_{phs}}$ plateau:** Theoretically, the three-level inverter is expected to exhibit a lower $\text{THD}_{I_{phs}}$ in the phase current across varying switching frequencies, owing to the reduced rate of change of the applied voltage across the switches. However, this was not observed in the present case. Exploring alternative modulation techniques or varying the switching device parameters may help uncover the reasons behind this unexpected behavior, which can be studied in the future.

- **DC-Link Voltage Balancing:** In simulation, DC-link voltages were inherently balanced due to ideal component matching and symmetric loads. In real hardware, mismatches and load variations can cause voltage drift across the

capacitors. Future studies should model component tolerances and unbalanced loads and investigate feedback-based balancing techniques.

- **Control Strategy Integration:** The inverter control in this work is limited to SPWM and PD-SPWM without feedback. Implementing closed-loop controllers, such as FOC or direct torque control, could provide insights into dynamic performance, disturbance rejection, and current tracking under variable load and speed conditions. However, adding this in *LTspice* might be more complicated compared to *Simulink*.

- **High-Power Scaling:** Although this thesis targets a low-voltage application, the findings are relevant to higher power domains, such as electric vehicles or grid-tied inverters. Future work could investigate the same topologies at 400 V or 800 V levels, where GaN's benefits in dv/dt control and power density become even more pronounced.

- **High-frequency switching** The result showcasing that three-level GaN provides less switching losses compared to two-level GaN at switching frequencies exceeding 723 kHz, indicates that GaN based MLIs are optimally utilized in high-frequency applications. According to [61] the size of attached EMI and ripple current filters could be reduced with f_c in the MHz range, which could be further improved using a hardware implemented PWM control system [62]. As such, performance analysis on high-frequency inverters would require further study, which is outside the bounds of this thesis, to ascertain if a high f_c would be a practical improvement compared to lower f_c implementations.

Overall, the findings of this thesis serve as a good foundation for further experimental development and refinement of high-performance, WBG-based inverter systems.

References

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