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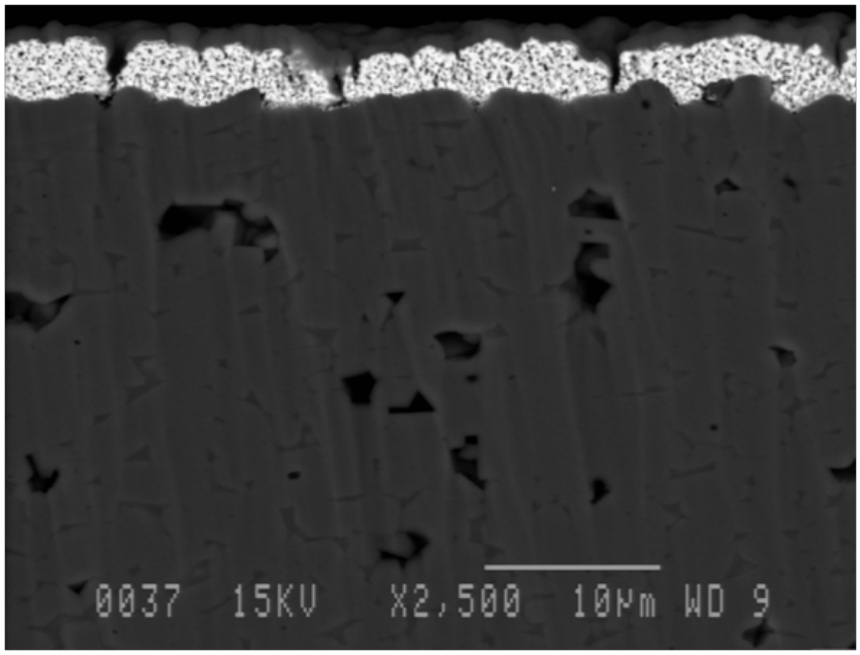

Substrates for Packaging of Silicon Carbide Power Electronics

Master of Science Thesis

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CHALMERS UNIVERSITY OF TECHNOLOGY
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MASTER'S THESIS

Substrates for Packaging of Silicon Carbide Power Electronics

One year (60 hp) Master's Thesis within the *Microtechnology* master's programme

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ABSTRACT

Silicon based power semiconductor devices are the fundamental components of electronic systems and circuits today. The need for high voltage devices that can operate at high ambient temperatures and switching speeds are growing; especially for the military, automotive and aerospace industries. Si based power electronics dominate the current market. However, Si suffers from limitations such as low band gap and low thermal conductivity, leading to limitations in switching speeds, blocking voltages and operating temperatures. Due to these limitations, there is an increasing interest in wide band gap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN). To meet the future demands of high power and high temperature components based on wide band gap semiconductors, new packaging concepts are also required. Materials such as aluminium nitride (AlN) and alumina (Al_2O_3) are appropriate for high power packaging, due to their high thermal conductivity and superior mechanical stability. In this master thesis project I have evaluated a new packaging concept for power electronics based on substrates of Al_2O_3 and AlN. A method to deposit nano silver ink by ink jet printing directly on Al_2O_3 is developed and the nano silver ink performance has been evaluated. It is shown that parameters like surface preparation and sintering conditions are essential for the final result. The resistivity of the printed ink is evaluated and results indicate that the resistivity is close to bulk silver. Experiments show that the nano silver can be sintered at temperatures as low as 250 °C to achieve sufficient electrical conductivity. Further, a packaging concept based on existing substrate technology (Direct Bonded Copper (DBC) with AlN core) is designed, simulated and manufactured by conventional etching technology.

Key words: Packaging, silicon carbide, SiC power electronics, printed electronics, substrates for power electronics

List of abbreviations

E_g = energy gap

N_i = intrinsic carrier concentration

N_d = concentration of ionized donors

N_a = concentration of ionized acceptors

E_c = highest critical field

V_b = breakdown voltage

HALT = Highly Accelerated Life Test

HAST = Highly Accelerated Stress Test

CTE = Coefficient of Thermal Expansion

SEM = Scanning Electron Microscopy

SAM = Scanning Acoustic Microscopy

Al_2O_3 = Aluminium oxide/Alumina

AlN = Aluminium nitride

DBC = Direct Bonded Copper

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1 INTRODUCTION

The use of silicon carbide (SiC) as a base material in power electronics has many advantages including high breakdown voltage and excellent temperature endurance. However, the packaging of such electronics presents major challenges. It must prevent discharges and handle the high temperature gradients that arise from high power dissipation. Thermal conductivity, thermal expansion coefficients, stiffness of the materials in the transistor chip, and electrical interconnections are important parameters to consider in the design of the package.

A preliminary package design developed at Swerea IVF exists. This master thesis focuses on the substrates used in this high power package design for SiC transistors. The experimental work concentrates on developing Al_2O_3 substrates suitable for SiC high power components. As an alternative method, a package concept was designed and etched based on existing aluminum nitride (AlN) DBC technology.

The aim of the project is to:

- Increase the knowledge about SiC power electronics today and understand why SiC is interesting as a future semiconductor material.
- Describe important theory involved in packaging fundamentals.
- Evaluate the package design by using thermo-mechanical simulations.
- Investigate how substrates based on Al_2O_3 for SiC power electronics may be developed and experimentally evaluate and develop chosen technologies.
- Investigate if ink-jet printed nano silver may be used to manufacture metalized substrates based on Al_2O_3.
- Evaluate if the ink-jet-printed nano silver has potential to be used on alumina as a conducting material.
- Evaluate a SiC packaging concept by thermo-mechanical simulations.
- Design and etch DBC substrates based on the existing packaging concept.

This thesis consists of two main parts: a theoretical background and the experimental part. Chapter 2 summarizes theory concerning packaging, semiconductor materials and substrates to provide necessary background for the reader. The experimental chapter 3 describes the work and experiments done during this thesis and in chapters 4 and 5 results are analyzed and discussed. The report ends with conclusions and recommendation for future work.

2 BACKGROUND

Today power electronics technology is used in a wide area of applications. The need for high power devices capable of operating at high ambient temperatures are growing, especially for the military, automotive and aerospace industries.

Power electronics components include bipolar junction transistors (BJTs), Metal-Oxide-Semiconductor field-effect transistors (MOSFETs), diodes, thyristors and insulated-gate bipolar transistors (IGBTs). Today, components based on Si are dominating the market. In common for all components is that they suffer from limitations that are directly derived from the material properties of Si. For example, the development of high power Si MOSFETs has lately been problematic due to high blocking voltage and high on-resistance, which in turn, results in high conduction losses (1).

By introducing wide band-gap semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN) the development of high performance power electronics can continue. SiC based semiconductors and circuits are presently developed for use in high-power/temperature, high frequencies and high switching speeds. The introduction of wide band gap semiconductors will contribute to better performance of components in high power environments and result in energy savings in public electric power distribution and motor drives. The market for high power devices is steadily growing and is assumed to have a market size of 25000M USD in 2015 (2).

2.1 SILICON CARBIDE

Silicon is the main semiconductor material used in the power electronics industry today. Due to its multiple advantages such as great ease of processing, low cost, high electron mobility and its suitable semiconductor properties, Si is a superior material – but only in lower voltage regions, less than about 200 volts (1). This is due to the fact Si suffers from limitations that are inherent to its material properties and will restrict the development of future power electronics.

This section will further explain the fundamental material properties of Si and SiC.

2.1.1 MATERIAL PROPERTIES

Silicon Carbide is one of the hardest and thermally most stable materials. This result in high reliability of high temperature devices but at the same time it is more challenging when coming to device processing, particularly crystal growth. Concerning Si, the successful Czochralski process is used to form single crystal boules. This is possible because Si melts at a manageable temperature (1412 ˚C). SiC on the other hand, does not melt, but will sublimate at temperatures above 2000 ˚C. Hence, SiC boules are grown using a much more elaborate process, where SiC source material is sublimed onto a seed crystal at about 2200˚C. This causes high manufacturing costs.

SiC is an IV-IV semiconductor comprised of an equal number of Si and C atoms. SiC occurs in many different crystal structures (polytypes). Today there are over 150 known polytypes, but only a few are available commercially as bulk wafers or custom epitaxial layers. The most common polytypes used as semiconductors are 6H-SiC and 4H-SiC both with hexagonal crystal structure. Of these two, 4H-SiC has become the polytype mostly used in power electronics. This

is due to the more isotropic nature of its electrical properties, its high carrier mobility and the low dopant ionization energy. The high dielectric strength of SiC enables the possibility to use thinner epitaxial layers (approximately 10 times smaller than Si-based components) in high power devices. A thinner epitaxial layer results in low drift resistance and low conduction losses (2) (3).

In comparison with Si, SiC have many favourable material properties:

- Wide energy band gap
- High dielectric strength
- Low intrinsic carrier concentration
- High thermal conductivity
- High carrier saturation velocity

See Table 1 for details.

These properties of SiC are important in power electronic components. The wide band gap and low intrinsic carrier concentration allows SiC components to operate at much higher temperatures and currents than traditional Si based components. The small intrinsic carrier concentration makes it possible to exceed junction temperatures of 800 ˚C and there have been experimental results showing SiC device operation in 600 ˚C (2). Theoretically this can be understood by studying the fundamental equation describing n_i, the intrinsic carrier concentration (Equation 1).

$$n_i = 2{,}5 \cdot 10^{25} \frac{T}{300}^{3/2} \cdot e^{-E_g/2kT} \qquad (1)$$

where E_g is the band gap, T the temperature and k the Boltzmann constant. As the temperature increases, the concentration of carriers increase exponentially resulting in high leakage currents and finally as the temperature reaches a certain point, the conductivity becomes uncontrolled (1) (2). This is mainly due to the sliding of Fermi-levels towards the middle of the band-gap with increasing temperature.

The built-in voltage, $V_{bi,}$ is another important property to take into consideration when comparing Si and SiC. For a forward biased junction, $V_{bi,}$ has to be exceeded before a significant current can flow. As shown in equation 2, the lower intrinsic carrier concentration, n_i, in SiC results in a higher built in voltage than in Si (1). This is the reason to the high possible blocking voltage of SiC. N_d and N_a are the concentrations of donors and acceptors and q is the elementary charge of an electron.

$$V_{bi} = \frac{kT}{q} \cdot \ln\left(\frac{N_D \cdot N_A}{n_i}\right) \qquad (2)$$

Table 1 Material properties of Si and SiC

Propertie	**Si**	**4H-SiC**	**6H-SiC**
Band gap (eV)	1.1	3.2	3.0
Breakdown field (Nd = 10^17 cm-3) (MV/cm)	0.6	3.0 (// c-axis)	3.2 (// c-axis)
Thermal conductivity (W/cm-K)	1.5	3-5	3-5
Intrinsic carrier concentration (cm–3)	1e10	1.8e6	1e-7
Saturation velocity (cm/s)	1e7	2e7	2e7

2.2 PACKAGING FUNDAMENTALS

Microelectronic packaging is an important and fundamental part of microelectronics technology today. All electrical components or microsystems need to be packaged to retain and achieve their essential functions in the means of power supply, mechanical protection and stability, cooling, and electrical and mechanical connections. Today, it's not only the semiconductor devices that limit future power system development – rather it is the packaging of these new components that creates the technology barrier (4).

Microsystems packaging can be divided into a three-level packaging hierarchy (3):

First level: packaging of Integrated Circuits (ICs) involving interconnection, powering, protection of the IC, cooling, and substrate that carries the chip.
Second level: connection of components onto a system lever board, typically called motherboard. This board, PCB (Printed Circuit Board) carries components (passive and active) and electrical interconnects between these to form the system level board.
Third level*:* Several boards connected to an entire system, by cables and mechanical cabinets.

This thesis will focus on first level packaging particularly in the SiC Power electronics field and its reliability, thermal management and suitable materials used for mechanical support and electrical connections.

2.3 INTRODUCTION TO RELIABILITY

Reliability may have different meanings depending on the situation. Requirements vary with the type of product – Cell phones, cars or pacemakers – all products has their own requirements based on environmental -, economical- or safety aspects. Failure of consumer products may cause some inconvenience, but the failure of a pacemaker or airplane system may be fatal.

The failure of a system, for example a laptop not starting up or a TV with random picture problems, normally has underlying hardware problems. The system failure can be caused by thermally induced stresses, cracks in solder joints, a shorting due to moisture, etc. A mismatch in the thermal expansion of different materials is often the cause of the failure.

Reliability is the ability of a system, component or device to perform its required function under a stated period of time and in a specified environment. Reliability is defined as the probability that the component or system will be operational within acceptable limits for a given period of time (3). There are different definitions of reliability, of which two common ones are stated below (4):

- The ability of an item to perform a required function under stated conditions for a specified period of time.
- The probability that a functional unit will perform its required function for a specified interval under stated conditions.

Depending on the type of component or product, there are different important failure *mechanisms*. In electronic packages they can be thermo-mechanical, electrical or environmentally caused mechanisms. These failure mechanisms arise because of exposure to for example humidity, voltage, temperature or mechanical shock. Failure *modes,* on the other hand*,* may be cracking, electrical short-circuits or solder joint failures.

In this master thesis I analyze the reliability of a high power package where several failure mechanisms and modes are possible. When reliability is studied the analysis gives answers to one or more questions concerning (5):

- When failure occurs
- What causes failure
- How to avoid failure
- The expected life time of the product/component

There are two main approaches to ensure that the component meets the reliability requirements. The first approach is to analyze potential failure mechanisms that could result in failure during the early stages by optimizing materials, structures and processes. The second approach is to use accelerated tests on the final product, to be able to analyze and predict the long term reliability of a product during a reasonable period of time.

When reliability tests are performed and the failure modes are detected different kinds of data have to be analyzed. When electronic components or packages are tested, the data is used to demonstrate that no delamination, cracking or other failure modes has occurred after long-term testing. Normally, methods such as HAST (85°C and 85% relative) high humidity for 1000 hours, thermal bake tests at 150°C for 1000 hours, and/or thermal cycling tests of various duration from -40 to 125°C are used to investigate the reliability.

In general, for power electronics, it is also of interest to perform power cycling, to see how the component behaves while exposed to high fluctuations in regard to power densities. (6) Due to the circumstances for SiC components, where a high power and harsh environment is targeted, the test variables need to be more extreme.

2.3.1 TESTING METHODS

Accelerated tests are used to simulate long term stress or reliability issues. Manufacturers or researchers cannot wait to obtain reliability results under normal operating conditions which could take several years. Accelerated tests may be split into two types; qualitative accelerated testing and quantitative accelerated life testing. The first one aims to give information about failure modes and to identify these. Quantitative testing is about to predict the life of a specific product or component. Example of some accelerated tests:

- High Temperature Storage (HTS),
- Accelerated Stress Test (HAST)
- Highly Accelerated Life Test(HALT)
- Temperature/Power cycling.
- Temperature/Humidity Testing, 85/85

These tests aim to give information on the products reliability in different environments with consideration to humidity, constant temperatures or cyclic temperature. Which kind of test is used depends on the component itself and the application. There is a big difference when testing components for harsh automotive industry compared to consumer electronics. There are different requirements on the reliability and also different requirements on the environment the component is designed for (6).

The reliability of a semiconductor device is commonly measured by the *hazard function*, also called *failure rate*. The failure rate in regard to time is often illustrated by the so-called *bathtub curve*, see Figure 1. As shown in the figure, the curve has three regions: Initial-, random- and wear-out failures. The failures derive from different mechanisms depending on the region in which they occur.

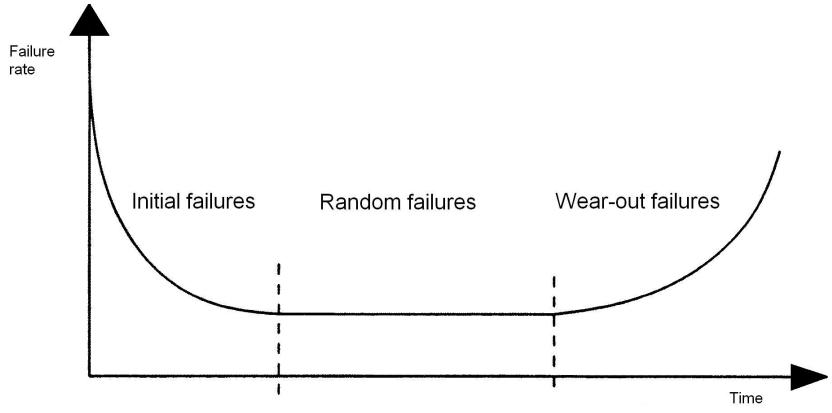

Figure 1 Schematic description of the failure rate of a semiconductor device in regard to time.

Initial failures
The first part of the curve represents the early failure period. Failures here are called initial failures or infant mortality failures. The main reason for initial failures is material or manufacturing defects.

Random failures
when the initial failures have stagnated, the failure rate becomes almost constant for a long period of time. During this period, devices with no early defects operates successfully, unless some randomly initiated stress (i.e. power surges, external shock, radioactive rays, etc) affect the device.

Wear-out failures
during the wear-out failure period the failure rate tends to increase rapidly due to the aging of the device by wear and fatigue. The reason for these failures is plainly the physical limitations of the semiconductor material (5).

2.3.2 FAILURE MECHANISMS

Failure mechanisms often occur at the lowest hardware level, i.e. the semiconductor device or the package of the semiconductor. A fundamental understanding of the mechanisms that lead to failure of components is important to achieve high reliability. There are many failure mechanisms that cause failure. In Figure 2 the most common (99,9% of all failures in microelectronics) are shown (7).

Failures in microelectronic packages can be divided into two groups: *Overstress mechanisms* and *wear out mechanisms* (as seen in Figure 2). Overstress mechanisms are characterized by a single high load, electrical or mechanical, causing a failure. Wear-out mechanisms on the other hand, are present during the whole life time of the product. Low stresses, often by cyclic mechanisms will result in cumulative (the material will not recover during rest) damages, slowly leading to failure in form of fatigue, delamination or creep.

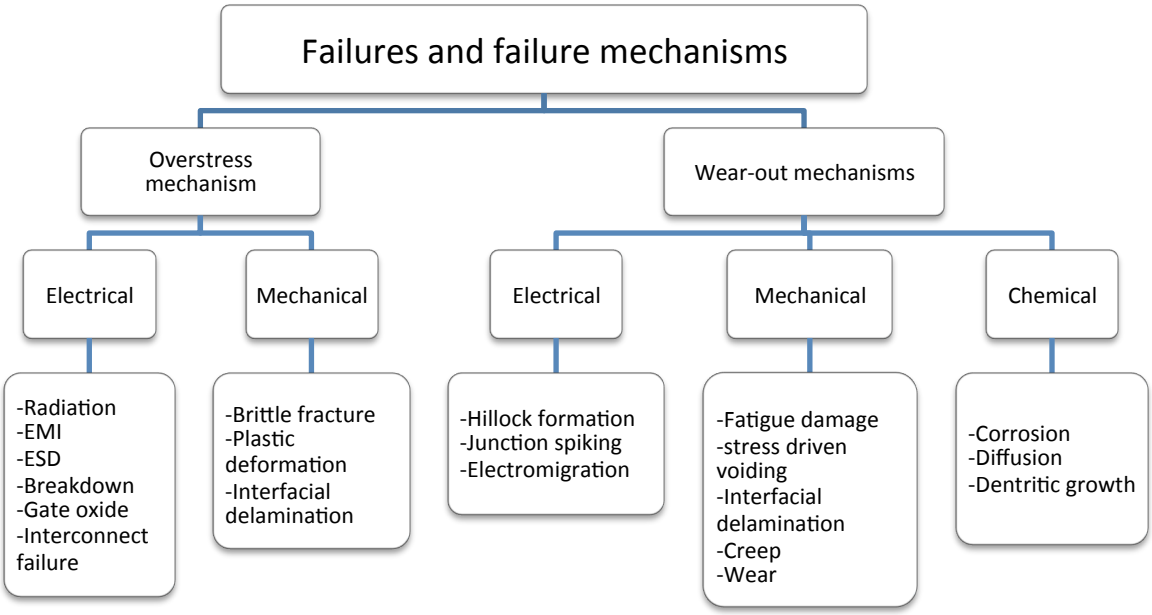

Figure 2 Failure mechanisms in semiconductor devices

2.3.2 THERMO MECHANICALLY-INDUCED FAILURES

Thermo mechanically-induced failures in power electronics originate from the temperature generated from the system. Particularly in high power electronics, the generated temperature causes high stresses. Thermally induced stresses and strains are often generated due to the mismatch in the CTE (coefficient of thermal expansion) of the packaging materials, see Figure 3. Consider the substrate (B) with CTE larger than the chip (A). When the temperature increases from the equilibrium, the materials will expand dissimilarly resulting in shear stress. The substrate with higher CTE will expand more than the chip as the temperature increases, and *vice versa* if the temperature decreases. As electronic equipment often has cyclic temperature behaviour, due to powering on and off, thermo-mechanical stresses often cause reliability issues.

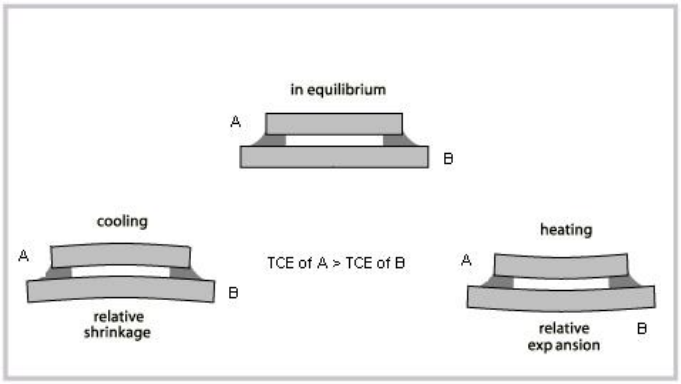

Figure 3 Stress caused by CTE-mismatch

Fatigue

Fatigue is a structural damage which affects materials subjected to cyclic loads, both elastic and plastic. About 90 % of all failures, both structural and electrical are believed to arise due to fatigue (7). When a material is influenced by cyclic loads the crystallographic perfection of the material is degraded by increasing dislocations and eventually micro-cracks starts to form (3). Fatigue may cause a serious threat to the reliability of a system as it eventually causes most materials to fail at loads far lower than they would under a single loading.

Cyclic fatigue in the region where the material is not exceeding the elastic regime, i.e. the yield point, is called *high-cycle fatigue*. If the material is exposed to cyclic fatigue where the load is so large that the material has plastic (irreversible) behaviour, it is called *low cycle fatigue*.

To predict the low cycle fatigue life, N_f, of metallic materials, for example solder joints or interconnects, there is one main approach:

The Coffin-Manson model:

The Coffin-Manson (C-M) model is used to predict the fatigue life, Nf, in terms of the plastic strain range, $\Delta\varepsilon_p$ according to:

$$N_f^m \cdot \Delta\varepsilon_p = C \qquad (3)$$

where C and m are material dependent numerical constants.

The Coffin-Manson equation has many versions depending on the actual area of use. The C-M equation can be expressed as a function of inelastic shear strain range, delta, to suit solder joint fatigue:

$$N_f = 0.5\left(\frac{\Delta\gamma}{2 * \varepsilon_f'}\right)^{\frac{1}{c}} \qquad (4)$$

where ε_f' is the fatigue ductility coefficient and c is the fatigue ductility exponent.

In the case of thermal cycling, the C-M relationship may be expressed by the means of the range of the thermal cycle, ΔT.

$$N = \frac{C}{(\Delta T)^\gamma} \qquad (5)$$

2.4 SUBSTRATES

Substrates in electronics are used as a carrier where the chips and components are mounted on the first level of the package. The substrate provides electrical interconnections (Printed Circuit Boards), mechanical stability and cooling of the electronics mounted onto it. In power electronics, compared to low power electronics, the requirements of the chosen substrate material is stricter due to higher currents and voltages, and high temperatures of several 100 °C (10).

The materials used as substrates for first level packages vary depending on the application. When new electronic packages are developed many factors has to be considered, including electrical properties and characteristics, environment (reliability demands) and cost. Two major groups of materials are used: Organics (including polyimide and epoxy) and ceramics (predominantly Al_2O_3, SiC, AlN) (11). In this project ceramic substrates are used, because of the electrical and mechanical properties.

The ceramic substrate needs a conducting layer. The conductor or material is selected in regard to electrical and mechanical properties like electrical conductivity, CTE, thermal conductivity and stability, processing temperatures and reliability (11).

In power electronics, where temperatures and current densities are high, the need of reliable and tolerant substrates is essential. However, the commonly used substrates today will not manage the higher currents and temperatures required to reach the full potential of SiC power electronics and new substrates needs to be developed.

2.4.1 DIRECT BONDED COPPER

Direct Bonded Copper (DBC) substrates are commonly used in power electronics. The substrates are composed of a ceramic core (usually alumina (Al_2O_3), aluminium nitride (AlN) or beryllium oxide (BeO)) where copper layers are directly bonded to both sides of the ceramic. The bonding is achieved by a high-temperature melting and diffusion process (in oxygen atmosphere) where a eutectic bond is formed (copper-oxygen), see Figure 4. DBC substrates can be plated with nickel or gold if necessary.

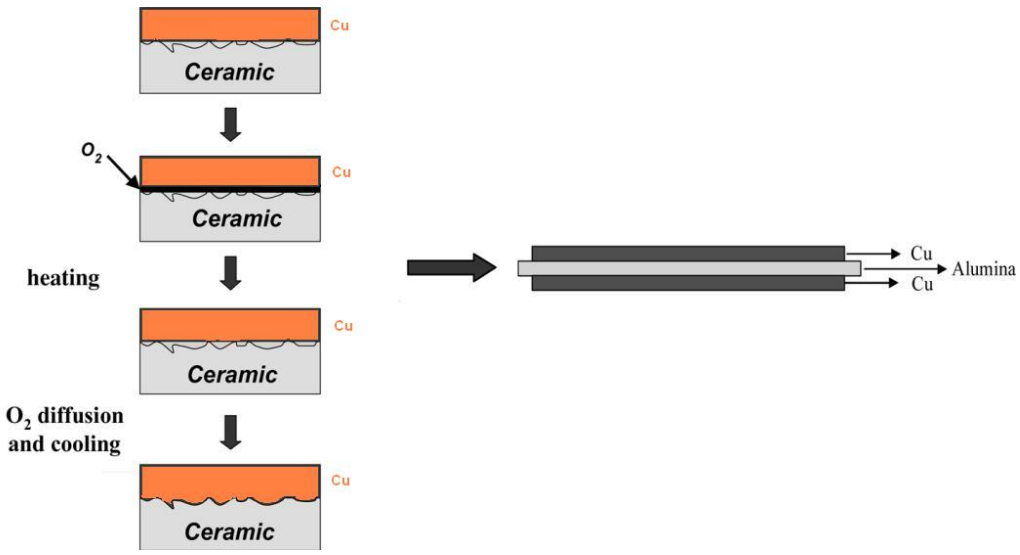

Figure 4 DBC Manufacturing process

The main properties that makes DBC substrates suitable for power electronics are:

- Low thermal resistance
- High insulation voltage
- High thermal conductivity and good heat spreading characteristics
- Low Coefficient of Thermal Expansion (CTE)

These are important properties in power electronics, where temperatures and power densities usually are high. The low CTE (which matches Si) results in high reliability in the means of thermal cycling performances due to the lower mechanical stress between chip and substrate (13).

Materials used in DBC substrates (14):

- **Alumina (Al_2O_3)** is widely used as a substrate material because of its low price/performance ratio. The thermal conductivity is low (24-28 W/mK) and is enough for general power electronics or other non demanding electronics.
- **Aluminum Nitride (AlN)** Is more expensive and used in applications where the operational voltages are high and the prerequisite of reliability are high. AlN combines excellent thermal conductivity (> 150 W/mK) with good mechanical stability. AlN has better CTE-matching with SiC, resulting in less thermal tensions between the chip and the substrate.
- **Beryllium Oxide (BeO)**, which has good thermal performance, but is often avoided because of its toxicity when the powder is ingested or inhaled.

In the design track of this project we have chosen Alumina DBC to manufacture substrates. This is due to the best price/performance ratio.

2.5 NANO-SILVER

Nanoscale silver paste, or just nanosilver, has received attention recently due to its promising material properties (17) (18) (19). Compared to pure silver, nanosilver has comparable electrical and thermal properties which make it appropriate for die attach and device interconnection, particularly in high power electronics. The sintering temperature of 230-250 °C establishes nanosilver as an alternative lead-free solution for electronics devices.

The low sintering temperature compared to other silver pastes is due to the small particle size, often 8-10 nm in diameter. The ratio between the surface area and the volume is high and results in high surface energies which make it possible to easily bind to neighbouring particles (17). To prevent nanosilver particles from aggregating at room temperature, they have to be coated with a dispersion agent. During the sintering this coating is removed and the particles can connect by atomic movements (19).

Sintering is a fundamental process to achieve electrical and mechanical functionality of the nano silver material. The sintering process affects the microstructure such as grain size and grain boundaries, and has great impact on the final performance of the nanosilver. Fundamentally, the driving force in sintering is surface energy. When sintering occurs, the total surface area decreases (the density of the compact increases). This results in a larger area between particles, and there is a “neck” formed between the two particles (see Figure 5 (a) and (b)). The neck-

formation is caused by different processes depending on the material. In amorphous materials, the process is viscous flow and in crystalline materials, such as nanosilver, the material transport process is self-diffusion. The neck-formation explains the shrinkage of the sintered material (20).

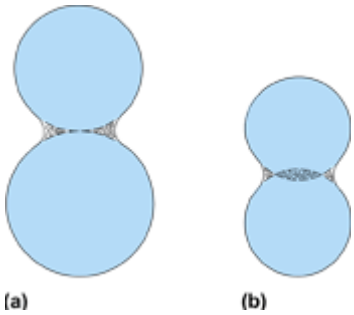

Figure 5 Neck formation during sintering process. (a) Neck growth through movement of defects from the neck surface to the adjacent flat surface. (b) During sintering the neck formation is increased (20).

Important parameters to consider when sintering nanosilver are:

Temperature

The sintering temperature will affect the morphology of the material. When the temperature is raised, the nanosilver atoms diffuse across the boundaries of the particles. It has been shown that the sintering process of nanosilver begins already at 160 °C (19). SEM pictures show that the grain size is larger than the initial grain size after one hour in 160 °C. See Figure 6 and Figure 7 (19).

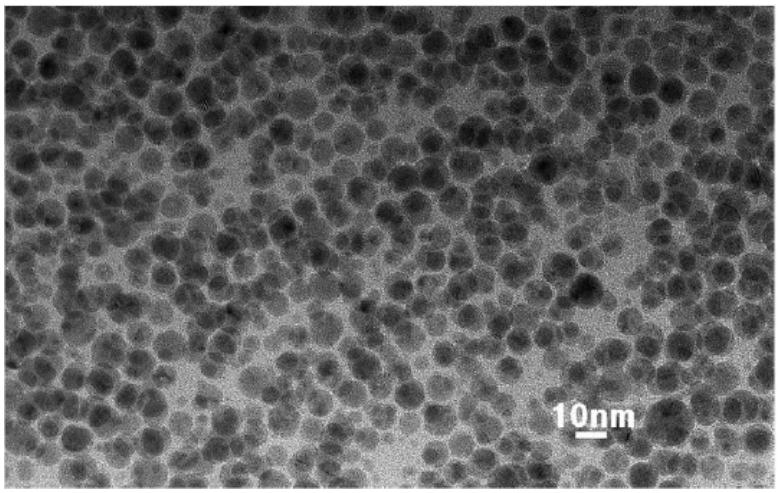

Figure 6 TEM Structural analysis of nano silver particle distribution (not sintered) (19)

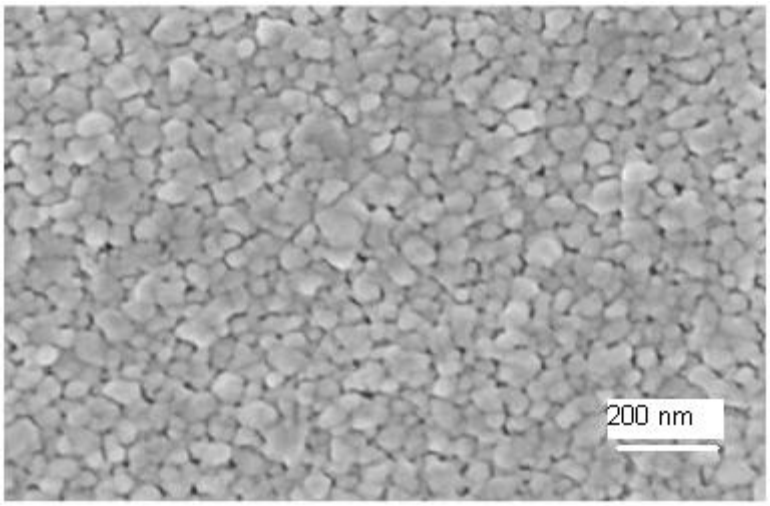

Figure 7 SEM picture of nanosilver sintered 1 hour at 160 °C (19)

Time

Moreover, the sintering time is an important factor affecting the grain size. S. Joo and F. Baldwin show that the grain size increases from 80 to 150 nm as the sintering time increases from 30 minutes to 60 minutes.

Cooling

To maintain the grain structure of the sintered nanosilver even at room temperature, it may be necessary to cool the sample. The cooling rate is important for the size of the grains. It is presumed that the lack of cooling may result in recrystallization of the sintered nanosilver particles as the temperature decreases slowly (19).

2.6 INK-JET TECHNOLOGY

Ink-Jet or printed electronics (PE) is of increasing importance in materials processing and production of modern microelectronics devices. The technology could simplify processes and reduce costs for microelectronics manufacturers and has the potential to replace standard methods used in the industry today (21). Printed electronics may be seen as an additive process, and has many advantages compared to today's traditional subtractive methods. The technology is data-driven, there is no need for masks, and the turnaround time compared to lithographic processes is shortened. It may reduce the number of fabrication steps as well as the amount of material used. Ink-jet technology can be used on nearly all kinds of substrates regardless of composition and morphology. Compared to other additive methods the printed electronics has a so-called non-contact approach, which decreases the chance of contamination during fabrication. These advantages could speed up the production and result in higher throughput (21).

In the future products such as RFID tags, inexpensive displays, electronic papers, other flexible electronics and different kind of sensors may be based on printed electronics. Ink-jet printed electronics could even replace traditional PCBs used today and/or be used to interconnect electronics (17). This could totally change the way electronics are manufactured in the future.

Ink-jet printers can arrange almost all kinds of patterns. By arrangement of dots, or droplets, with a small overlap, the printer can obtain conductive patterns. The printer ejects extremely small droplets of ink from the ink-jet head while moving in two dimensions. Precision even better than 30 µm with a printing speed as high as 2000 dots/sec has been reported. The precision depends on the printer nozzle diameter and the properties of the ink (21) (22).

2.6.1 IMPORTANT PROPERTIES OF CONDUCTIVE INK

The ink-jet printers require advanced materials, or ink, to be able to print electronics. The ink is based on a liquid with nano sized conductive fillers. To avoid sedimentation or separation the molecular fluid parameters has to be optimized in such a way that the ink achieves a very homogenous structure. Further, the ink has to contain a certain percentage of conductive filler to maintain the electrical conductivity after printing. The most important properties for ink used in PE are presented in Table 2. Nanosilver appears to be one of the best candidates for this purpose (22).

Table 2 Important Properties for ink used in Printed electronics

Viscosity	Very low, 1,4-1,55 mPas
Nanosilver filler	40-60%
Thixoprophy index	About 1,0
Surface tension value	28,5 – 32,5 dynes/cm
Sintering conditions	230-250 °C, 30-60 min
Electrical resistivity	1-3 10e-5 Ωcm

2.7 THERMAL MANAGEMENT

Thermal management of microsystems is important and may be crucial for the function of the system. This short chapter gives a small background to the problem.

When a current flows through leads and transistors in electronic components, heat is generated. The internal heat generation depends on the type of component, but fundamentally it depends on the electrical resistance and the current flowing through the component. If the heat generated by the component can't escape the temperature will rise until failure occurs.

The avoidance of failure is the primary aim of thermal management in electronic products. Failure of a component is often associated with a sharp increase in temperature. Figure 8 illustrates the importance of the temperature for the failure rate (12). Thus, it is important to use a substrate which has a high thermal conductivity to remove the dissipated heat.

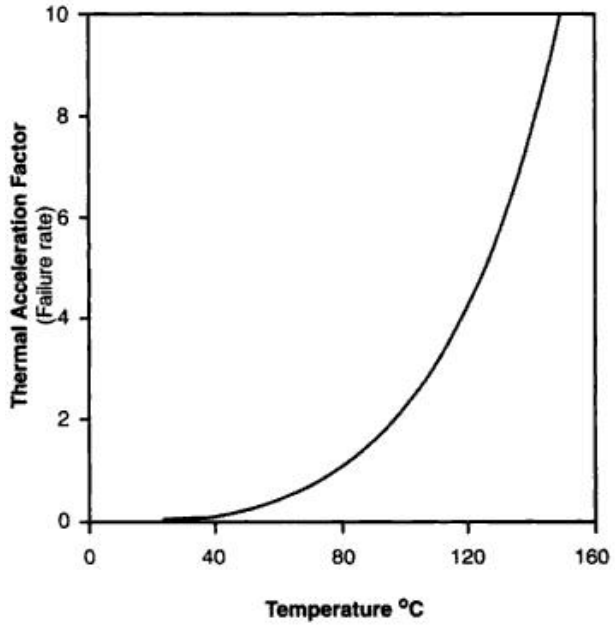

Figure 8 Effect of temperature on failure rate in microelectronic components.

3 EXPERIMENTAL

The aim of this thesis is to develop a new, innovative package designed for SiC transistors with focus on the substrate material. The experimental part of this project focuses on how the substrates used in the package may be developed and manufactured. To some extent, the experimental part will also investigate the performance of the developed materials.

There are two main approaches within this project regarding the substrate:

- To investigate how a new substrate based on Al_2O_3 aimed for high power electronics may be developed.
- To manufacture DBC-substrates according to the existing design.

The first approach will investigate how Al_2O_3 may be plated with conducting metals in an appropriate way. A lot of experiments were made to investigate which materials are suitable for use together with Al_2O_3. The second approach is based on already excising DBC-substrates. In this case the challenge is to design the mask used for etching. This part also includes a thermo-mechanical simulation, to find possible weak points or errors in the design.

This chapter will describe the experiments carried out during this project and present the results in conjunction with each experiment.

3.1 PLATING OF TITANIUM ON AL_2O_3

In the first attempt to plate silver on Al_2O_3, the approach according to Figure 9 was used. The Ti layer will work as an adhesion layer and the palladium as an activation layer for the Ag plating process. Different methods were investigated to achieve a Ti layer onto the Al_2O_3 substrate, described in the following subchapters.

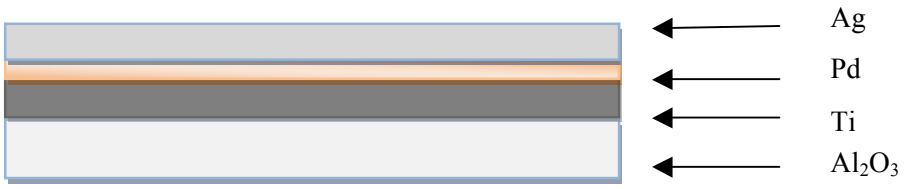

Figure 9 substrate design

3.1.1 EXPERIMENT 1 –TETRAETHYL ORTHOTITANATE.

An Al_2O_3 substrate was plated with different concentrations of Tetraethyl Orthotitanate (TEOT). Four concentrations of TEOT were dropped onto an Al_2O_3-wafer and put into an oven at 525 °C, nitrogen environment. The concentrations are summarized in Table 3.

Table 3 Concentrations of TEOT used in experiment 1

Nr.	TEOT, (C8H20O4)Ti	2-propanol	Isopropyl-tri(N-ethylenediamino)ethyl-titanate
1	-	40%	60%
2	60%	40%	-
3	80%	20%	-
4	100%	0%	-

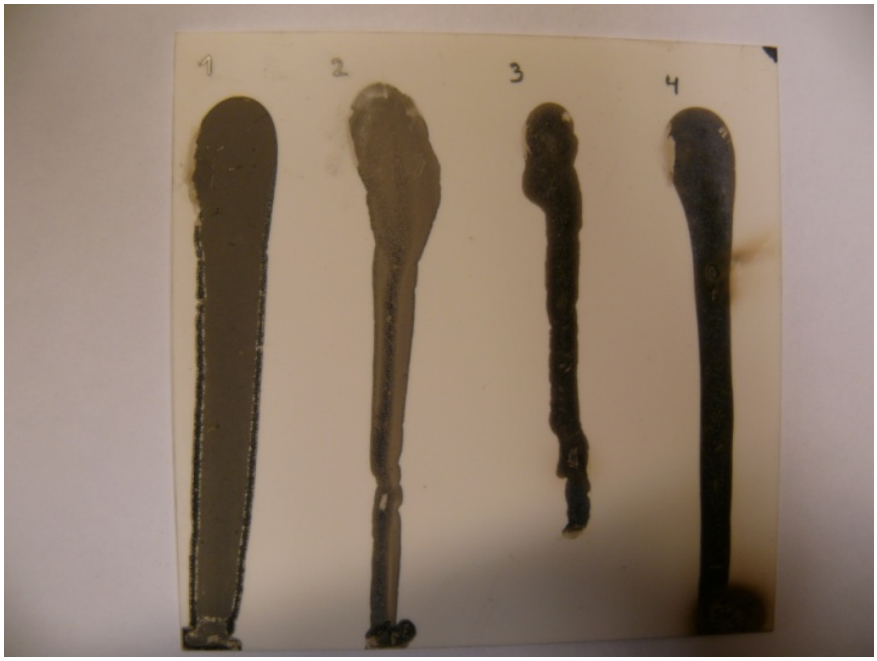

Figure 10 Result of experiment 1. Different concentrations of Tetraethyl Orthotitanate on Al_2O_3 after 1 hour in furnace.

To investigate if metallic titanium was formed after heat treatment, the Al_2O_3 substrate was investigated with a SEM (JSM-840A at Swerea IVF). The analysis (Figure 11) shows that the surface is not coherent and has poor adhesion to the Al_2O_3-surface

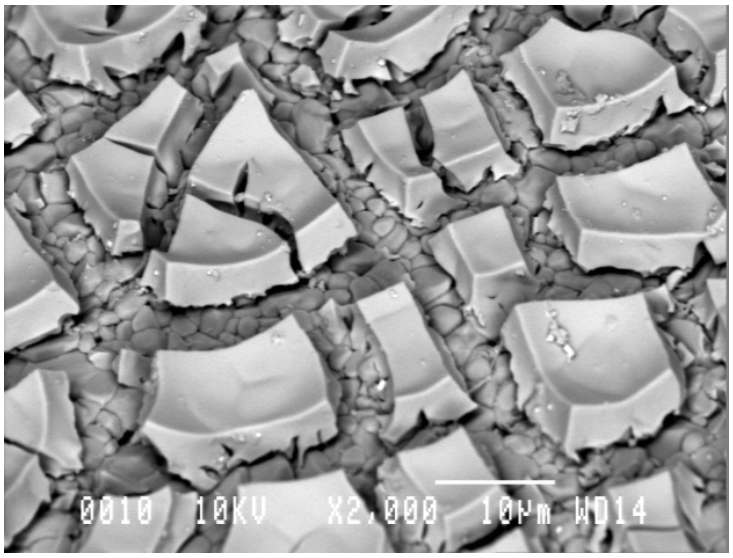

Figure 11 SEM picture of TEOT on Al_2O_3

Further, the same SEM was used to do an elemental mapping by EDS (Energy Dispersive Spectroscopy), to analyze if the surface contains titanium. As seen in Figure 12, there is a distinct amount of titanium (purple) represented in the analyzed surface. However, as the adhesion is poor and the surface is not metallic, the result is negative

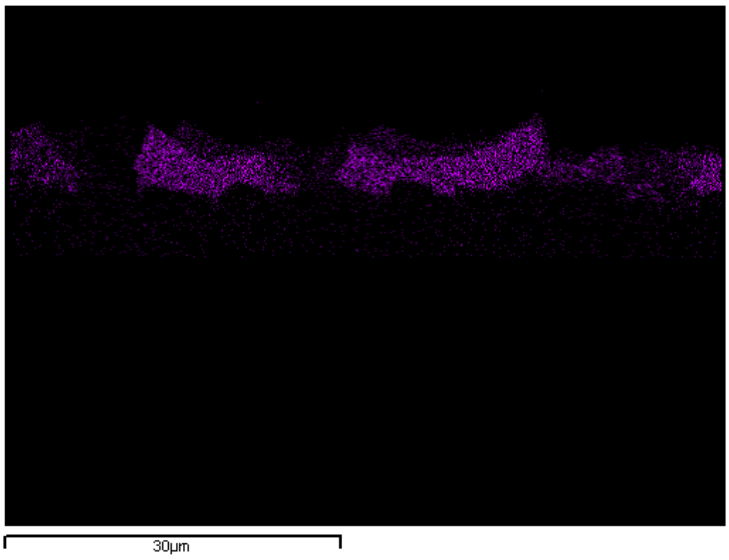

Figure 12 Elemental mapping (EDS) to see if the reduced TEOT contain titanium (purple).

3.1.2 EXPERIMENT 2 –TITANIUM POWDER.

By combining Ti powder and water (Ti concentration of 15% by weight) we achieve titanium grease which can be used to create a layer of titanium on the Al_2O_3 surface. The grease was applied with a brush to the ceramic surface and dried at room temperature. To achieve a metallic surface the grease was sintered in a high vacuum furnace.

The Ti power sediments quickly and makes the application process problematic, hence the concentration is an important factor. We found out that the most appropriate concentration is about 15% to achieve an applicable surface. See Table 4 for details.

Table 4 Summary of titanium powder mixtures used in experiment 2.

Sample	Ti, Tilop-54 (<45 μ) (g)	H2O (g)	Concentration (%)	atmosphere/temperature	Sintering time (h)
1	2	2	18,16	-	-
2	2	2,5	15,07	Vacuum/1200°C	1
3	2	2,5	15,07	Vacuum/1200°C	2

The furnace used is high vacuum sintering furnace at Swerea IVF. Sample 1 was not possible to use due to sedimentation. Samples 2 and 3 were successful and a metallic titanium surface was achieved after sintering, see Figure 13. The adhesion to the alumina was good, but the surface roughness was too high. Furthermore the thickness was hard to control due to the unwieldy manufacturing process. Due to these factors, the conclusion is that this type of titanium surface is not applicable for the purpose of this project. To use this approach another application method is needed, e.g screen printing. However it is not within the scope of this project to evaluate this approach further.

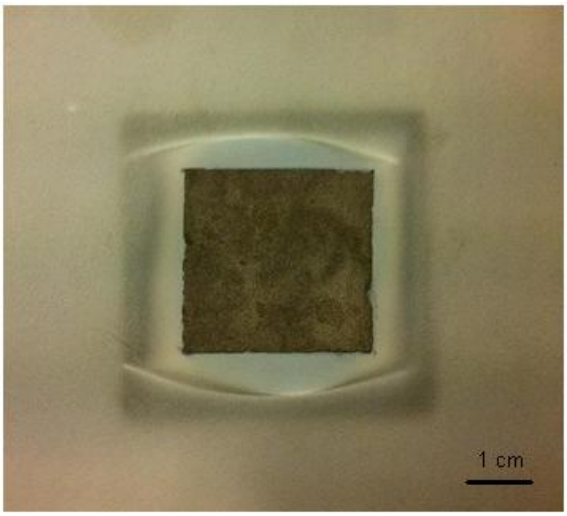

Figure 13 Metallic titanium was achieved after sintering

3.2 NANO SILVER INK PRINTED DIRECTLY ON AL_2O_3 BY INK JET TECHNOLOGY

To avoid the complicated manufacturing process of the substrate (i.e deposition of metals onto Al_2O_3, etching procedure, etc) this chapter investigates if it is possible to use ink jet printing of nano silver ink directly onto the Al_2O_3 substrate. As described in chapter 2.6, this type of process may revolutionize the electronics manufacturing market.

In this chapter, the possibility to print nano silver ink directly onto ceramic substrates is evaluated. Important properties are identified as:

- Quality and resolution of the printed samples
- Sintering behaviour of nano Ag-ink
- Adhesion to Al_2O_3 after sintering
- Electrical conductivity after sintering

3.2.1 PRINTING PROCEDURE

The printer used in this project is a prototype developed at Swerea IVF, see Figure 14. The ink used is developed by *Methode Development Company*, type #3800. Ink properties are listed in Table 5.

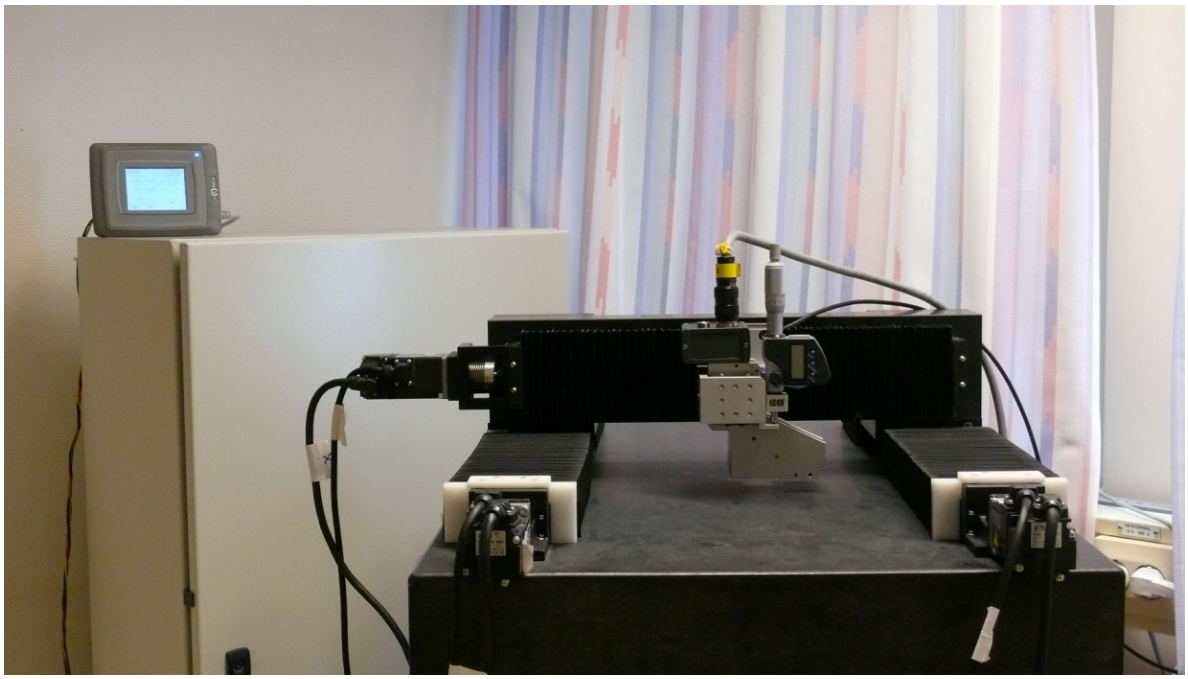

Figure 14 Prototype ink-jet printer developed at Swerea IVF

Table 5 Properties of inkjet ink #9101

Print thickness	1-2 µm
Viscosity	5-7 cps @ 25 °C
Density	1,2 g/ml
Surface energy	40-50 dynes/cm

A 2-bit test pattern was created in a pixel graphics program (Figure 15) and loaded into the printer software. To reduce nozzle errors, the printer head was cleaned and a number of "spits" were shot. The ceramic substrate is cleaned and aligned into the printer. Before printing, the distance from the substrate to the printer head is set to about 0,5 cm.

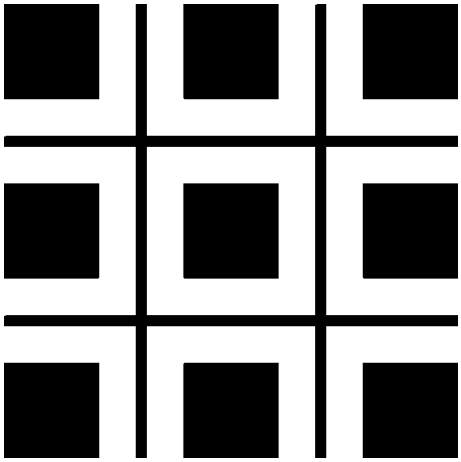

Figure 15 Test pattern used during ink-jet printing experiments. One square corresponds to 0,5 x 0,5 cm.

3.2.2 INITIAL RESULTS

After the printing procedure the sample was sintered 30 minutes at 300 °C. The sample was investigated in regard to printing quality, adhesion to substrate and conductivity. The first observations (see Figure 16, Figure 17 and Figure 18) indicated poor edge definition and bad adhesion. The sintered ink was easily removed by mechanical impact and the printed ink was of low resolution. A non standardized tape test indicated that the adhesion was extremely low.

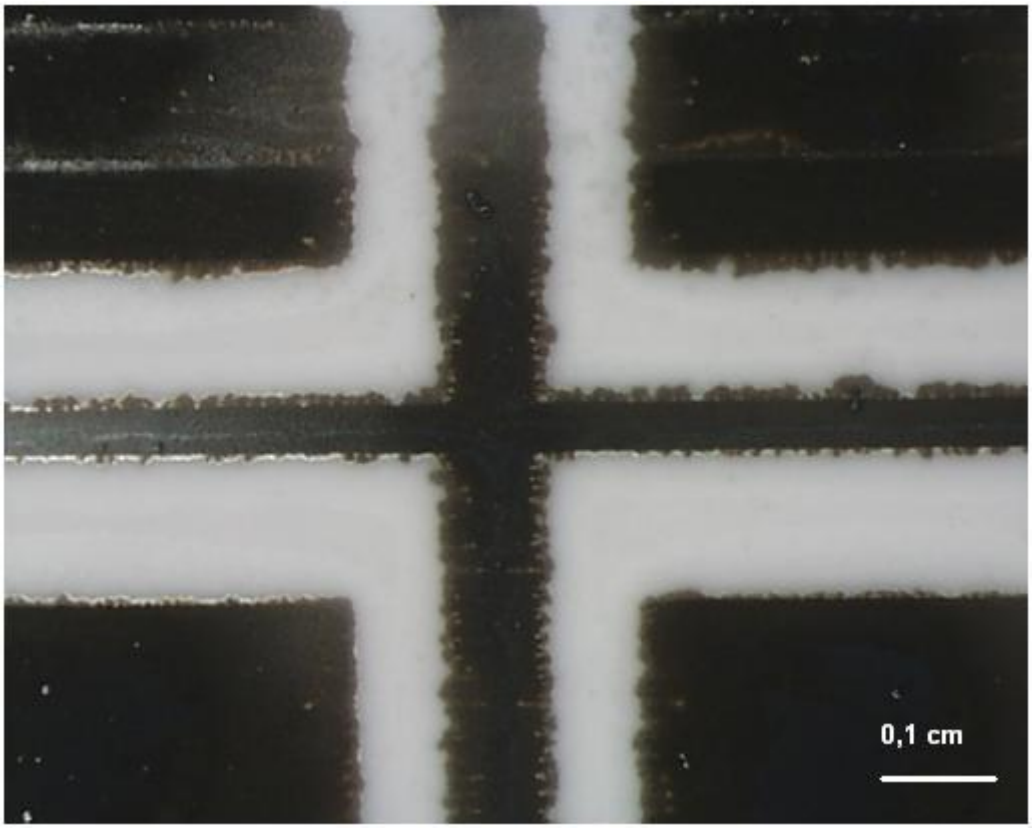

Figure 16 Not sintered Nano silver ink printed on Al_2O_3.

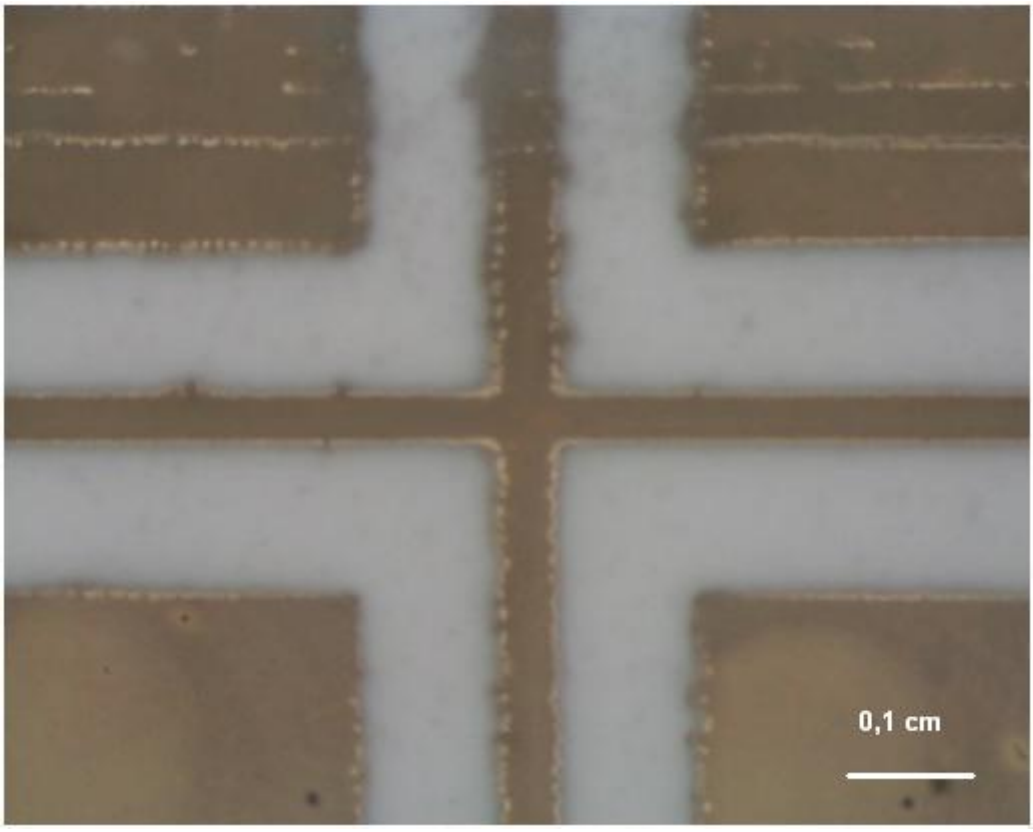

Figure 17 Sintered nano silver ink on Al_2O_3.

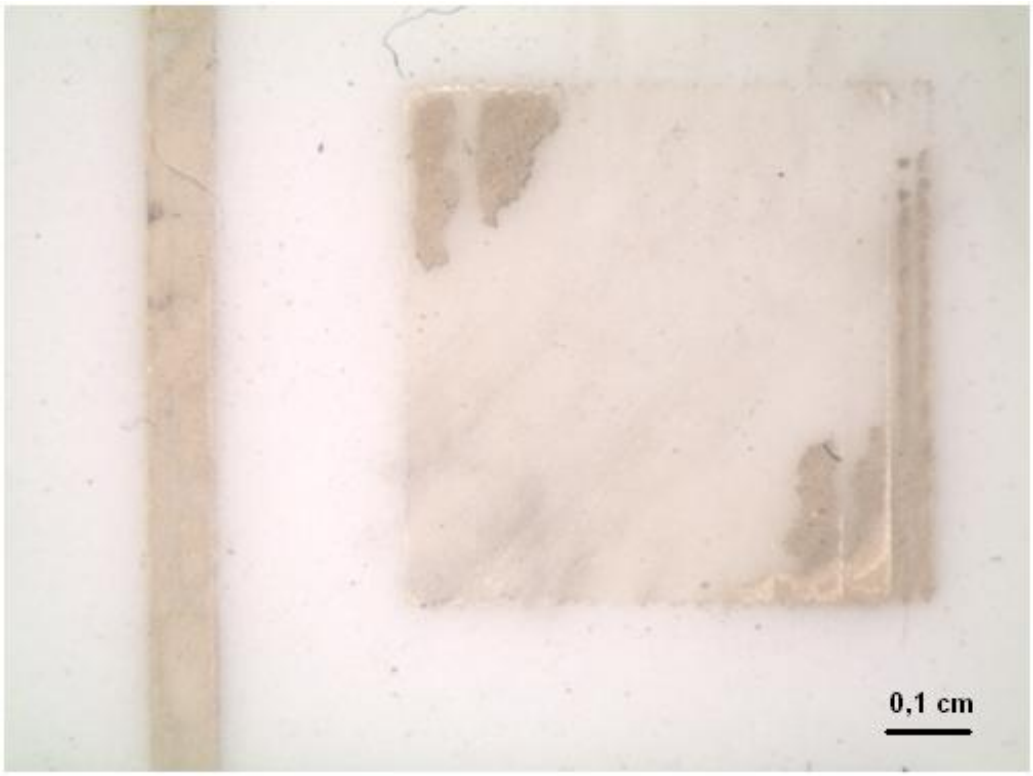

Figure 18 By Mechanical impact/tape test, the sintered nano ink was easily removed.

3.2.3 SURFACE PREPARATION

To improve the printing results and ink adhesion, proper surface preparation may be critical. As seen in chapter 3.2.2 it may be assumed that the wetting properties are not optimal. The wetting properties are regulated by the surface energies between the ink and the Al_2O_3 substrate as well as by the surface roughness. To optimize the ink wetting, two approaches were evaluated:

- Influence the surface roughness by blasting
- Chemically treat the Al_2O_3 surface to optimize the wetting between ink and substrate.

BLASTING OF AL_2O_3 TO IMPROVE ADHESION TO NANO SILVER INK

To blast the Al_2O_3 surface, standard industrial equipment was used. The blasting material was glass. The experimental procedure was repeated from 3.2.1 and sintered with same conditions and evaluated as earlier. The results show that the blasting treatment did not improve the ink adhesion. It may be due to low cleanliness of the blasting equipment or due to the fact that the adhesion is not promoted by a rough surface.

CHEMICAL TREATMENT OF AL_2O_3 TO IMPROVE ADHESION TO NANO SILVER INK

The present approach has taken inspiration from the gluing industry and uses a primer to treat the Al_2O_3 surface. It is common that metallic surfaces are treated with chemical primers before something is glued on them. It is believed that this kind of treatment may change the surface energies and/or help the ink to bind to the silane component of the primer.

The primer used in this experiment is based on methyl alcohol and amino silane. Before applying the primer, the Al_2O_3 surface was cleaned with alcohol and dried. The primer was

applied as thin as possible onto the surface with a cue tip**.** The primer was then allowed to dry for a minimum of one hour in room temperature before the printing procedure takes place.

Before the sample was sintered, it was investigated in an optical microscope. Compared to the initial results in 3.2.2, the primer appears to improve the printing result dramatically. As seen Figure 19, the definition of the ink is remarkably better than without the primer.

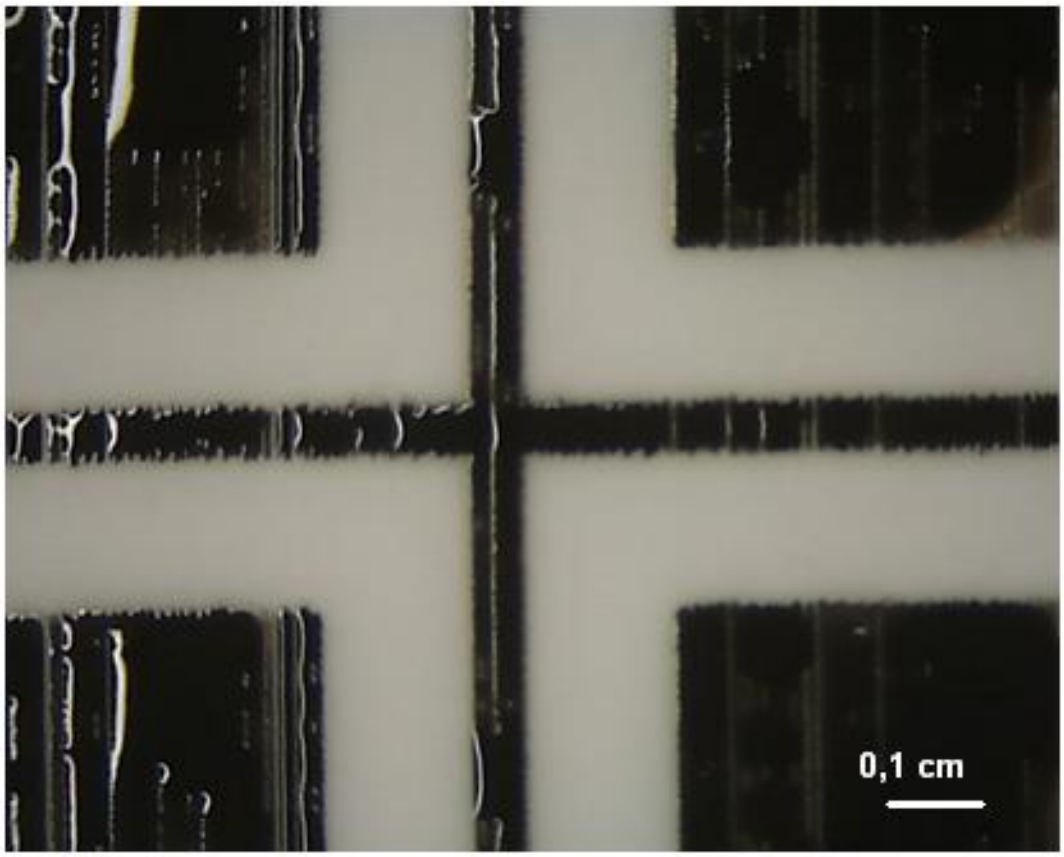

Figure 19 Not sintered nano silver ink on primer treated Al_2O_3.

The sample was then sintered for 30 minutes in 250 °C. The temperature is allowed to decrease slowly to room temperature after the sintering process is finished. Investigation of the sintered surface also shows great improvement. The printed silver is more defined and resists mechanical impact better. Scraping with tweezers and a provisional tape test indicates that the silver has good adhesion to the ceramic surface.

Resistance measurements show that the surface is conductive. There are some areas, shown as dark lines in figure Figure 20, where current cannot flow. These are due to printer nozzle errors.

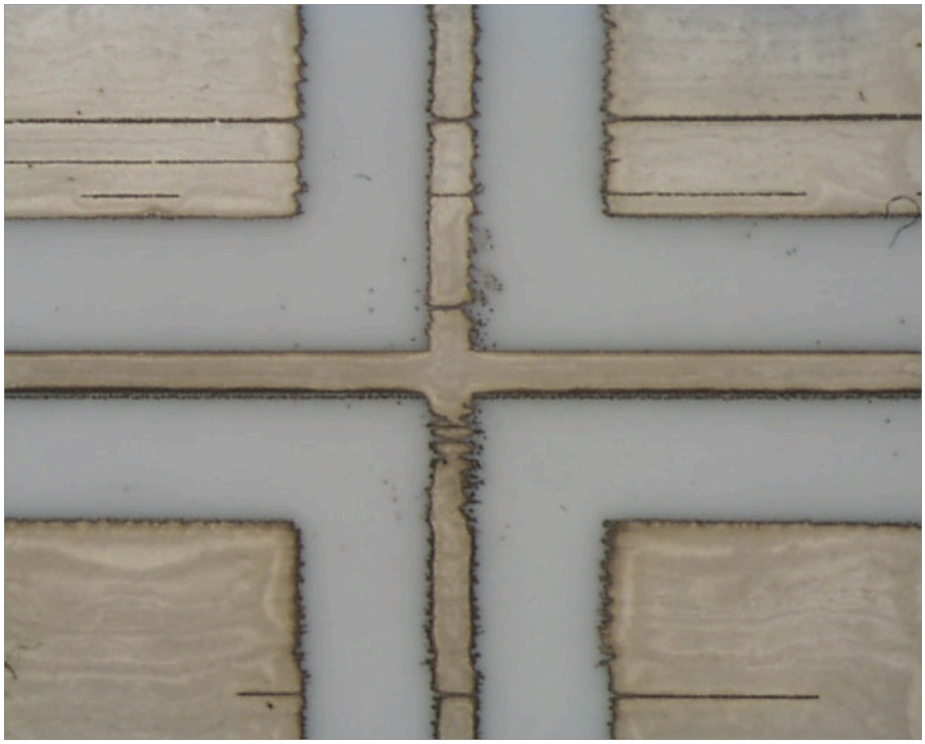

Figure 20 Sintered nano silver ink on primer treated Al_2O_3.

To further evaluate the effect of the silane primer in combination with the current ink, a glass substrate was treated with primer. The procedure was the same as earlier: clean, apply a thin layer of primer and dry in room temperature for one-two hours. As a reference, the same procedure was applied on a glass substrate without primer treatment. After printing, both samples were photographed in an optical microscope. See Figure 21 and Figure 22

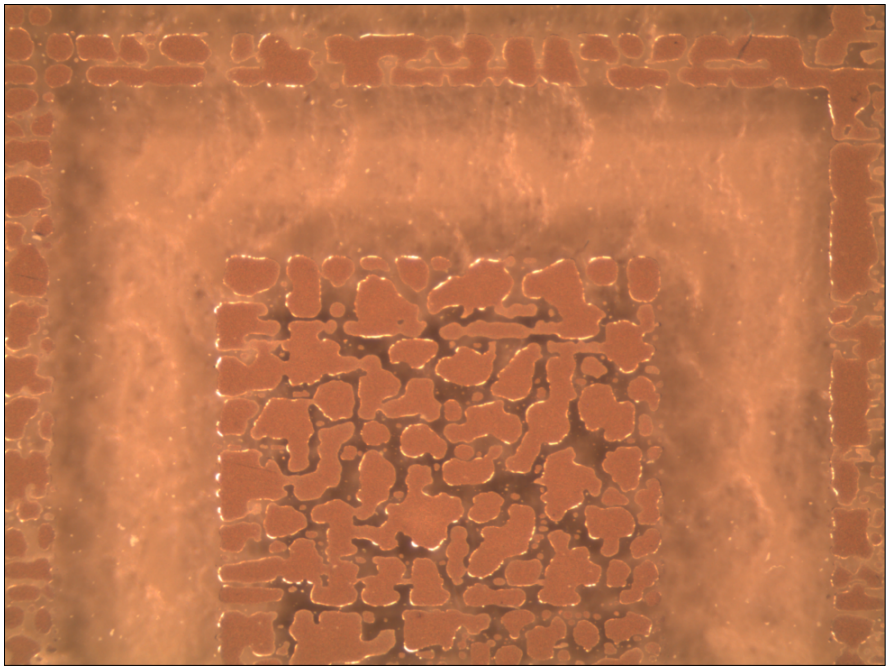

Figure 21 nano silver ink printed on to glass substrate

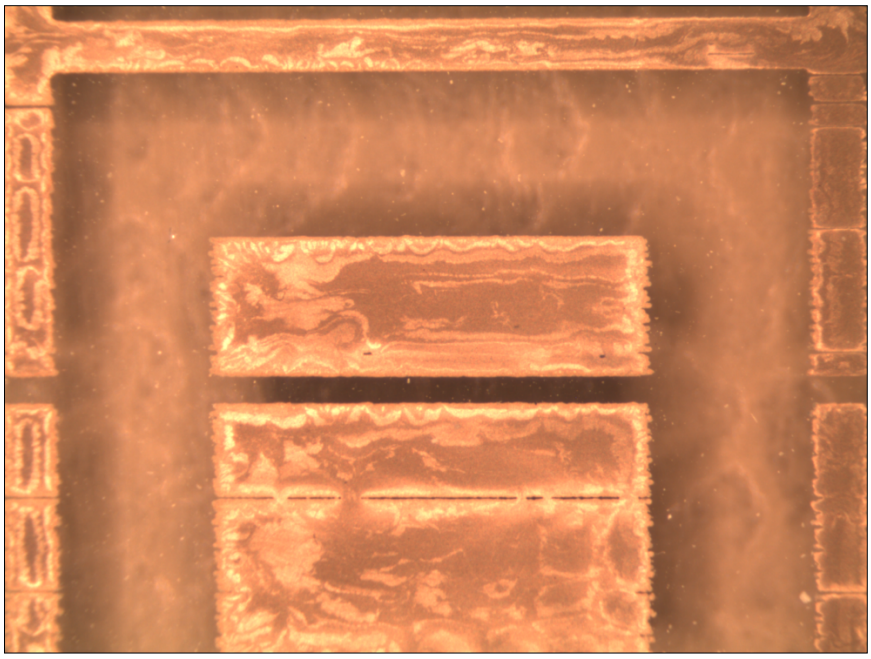

Figure 22 Nano silver ink printed on primer treated glass substrate.

It is obvious that the primer treatment has influence on the ink. The ink wets the treated glass substrate better due to the silane. Probably, the effect of the primer has a similar influence on the ink when applied on Al_2O_3.

3.2.4 SINTERING CONDITIONS

The sintering procedure of the ink is necessary to achieve electrical conductivity and mechanical stability. Different sintering conditions such as maximum temperature, temperature ramp and time at maximum temperature have been evaluated. This chapter describes how the nano silver ink responds to different sintering conditions and to state the most preferable sintering conditions in regard to electrical conductivity and adhesion to Al_2O_3.

TEMPERATURE TO OBTAIN ELECTRICAL CONDUCTIVITY

It is of interest to find out at which temperature the sintering process begins, i.e. to find the lowest possible process temperature of the actual ink. This is of great interest when applying the ink in future applications, where other involved components may restrict the process temperature. In this project, we evaluate the sintering temperature by measuring the conductivity of the ink. If the ink is conductive, it is considered to be sintered (i.e sintered adequately to achieve electrical conductivity (< 150 ohm) the sintering process will still go on if temperature or time is increased, though this is not of interest in this chapter.)

To evaluate the critical sintering temperature, resistivity measurements was made after different sintering temperatures. A sample of the Al_2O_3 with a printed test pattern was manufactured (as described in 3.2.1). Silane primer was applied to the surface. The sample was sintered in temperatures starting from 100 °C, in steps of 50 degrees, up to the temperature where conductivity was achieved. After each temperature step, the sample was removed from the furnace and resistivity measurements performed. A summary of measurements is shown in

Table 6.

The experiments indicate that the ink is sufficiently sintered at somewhere between 200 and 250°C.

Table 6 Data showing at which temperature the ink becomes conductive.

Temperature [°C]	Conductive [resistance < 150 Ω]
100	No
150	No
200	No
250	Yes
300	Yes

TEMPERATURE RAMP

In this experiment the temperature ramp used in the previous sintering experiment has been varied, to evaluate if it has impact on the final result. If no ramp function is programmed the furnace will heat up to the specified temperature with full power. All samples were prepared as described in 3.2.1 and silane primer was used. Initially, the samples were sintered without a specified temperature ramp, which gives a temperature ramp about 80 °C/min. Further, in total six samples have been sintered with two different temperature ramps; three samples at 10 °C/min and three samples at 3 °C/min. The first ramp is the fastest controlled ramp that the furnace can handle; the second one is chosen with regard to time (if a too slow ramp is chosen the experiments take too long time).

After the sintering process all samples were cooled down by natural cooling (oven shut down). To evaluate the quality of the samples, a non standardized tape-test was performed. If the sample passed the tape test, it was assumed "good". Among the samples that were sintered with the higher temperature ramp, only one was considered good. All samples sintered with low temperature ramp were successful. See Table 7 for details.

Table 7 Table showing the results from samples sintered with different temperature ramps.

Sample [nr]	Max temperature [°C]	Temperature ramp [°C/min]	Adhesion
1	250	80	Bad
2	250	80	Bad
3	250	80	Bad
4	250	10	Bad
5	250	10	Good
6	250	10	Bad
7	250	4	Good
8	250	4	Good
9	250	4	Good

3.2.5 SCANNING ACOUSTIC MICROSCOPE (SEM) ANALYSIS OF THE SINTERED NANO SILVER INK.

To get further knowledge about the sintered nano silver ink a SEM analysis investigation was made. The equipment used was a SEM (JSM-840A) at Swerea IVF.

A printed sample was prepared. Silane primer was applied onto the Al_2O_3 before printing and immediately sintered at 250 °C (4 °C/min, 30 min). The sample was cut to achieve a cross-section and prepared with ion etching equipment, to increase the surface smoothness.

The SEM analysis show that the surface has a thickness of about 2-3 µm and that the wetting to the surface is for the most part good (as seen in Figure 23). However, there are areas which have less wetting (see Figure 24). In the SEM pictures the silver layer reveals imperfections similar to cracks; these are pores and small irregularities in the surface, which could be due to the cutting of the substrate.

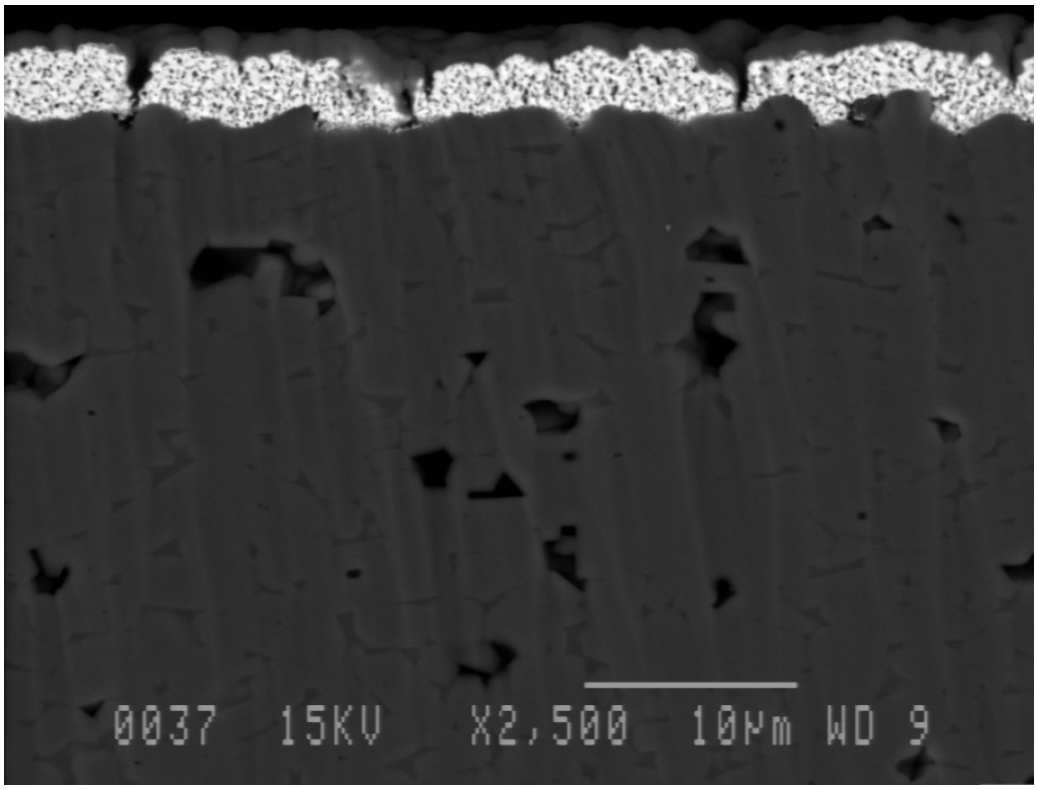

Figure 23 SEM picture of sintered nano silver ink.

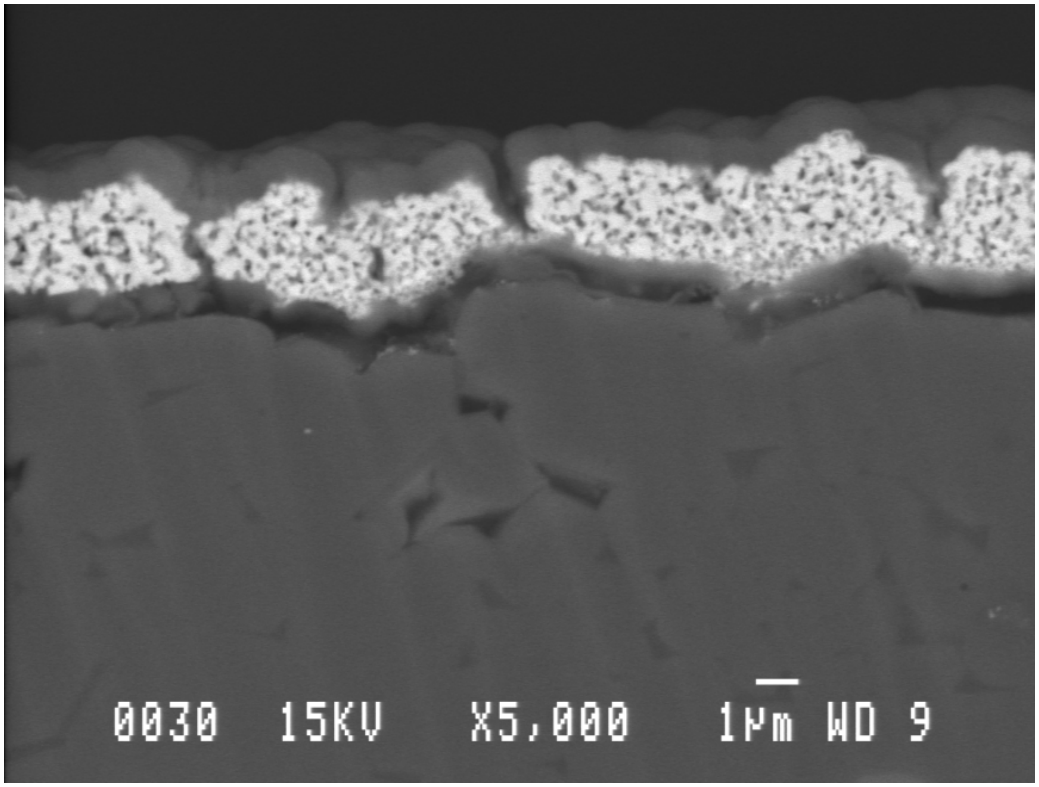

Figure 24 SEM picture of sintered nano silver ink. This picture is from the same sample as figure 28, but another area.

3.2.6 RESISTIVITY OF THE SINTERED NANO SILVER INK

To evaluate the resistivity of the nano silver ink, a new test pattern was developed (see Figure 25). The pattern was designed to suite for a 4-probe resistivity measurement. To increase measurement points and to avoid measurement errors due to bad printing, there are several conductors to measure on. The pattern was printed on Al_2O_3 (the same procedure as described in 3.2.1 and with silane primer) and sintered at 250 °C (4 °C/min, 30 min).

The resistance measurement was made with a Hewlett Packard 34401A Multimeter in 4-wire mode. 10 values were achieved from each silver conductor and a mean value was calculated. The line width and length was measured with a vernier caliper to be able to calculate the resistivity of the ink (to see details about measurement data and calculations, see appendix B). The thickness of the conductor was based on SEM results in chapter 3.2.5. The line widths are specified in pixels because the ink-jet printer is programmed with pixels as units. However, all measurements and calculations are based on SI-units.

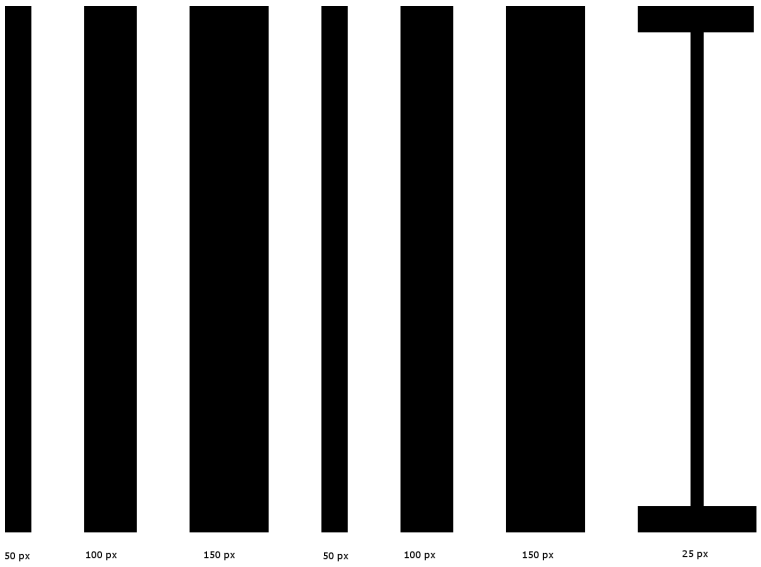

Figure 25 Test pattern for 4-probe resistance measurement.

As expected the resistance decreases while the thickness/area of silver ink increases. The resistivity (specific electrical resistance) of the nano silver ink was calculated and the results are shown in Table 8. The mean value of the resistivity is calculated to 8,75e-7 Ωm which can be compared with bulk Ag 1,59e-8 Ωm.

This experiment contains many potential sources of error:

- The thickness of the nano ink is based on the SEM analysis in chapter 3.2.5 and may not be constant over the measured area and may vary depending on the printing process.
- The cross section area of the conductor is extremely small, which gives big variations in the final resistivity calculation.
- Measurements are made by hand.
- The instruments used are not recently calibrated.

Table 8 The table summarizes the measured resistance values of the nano Ag ink and the calculated resistivity values, compared to tabulated silver.

Line width [pixels]	Resistance [Ω]	Resistivity [Ωm]	Conductivity [S/m]
50	13,0865	1,2e-6	8,02e5
100	6,724	7,68e-7	1,3e6
150	3,5615	6,1e-7	1,64e6
Pure Ag (from table)	-	1,59e-8	6,3e7

3.3 BONDING OF SIC CHIP:

To evaluate how the printed nano silver behaves during bonding, an initial bonding test with a SiC chip was made. The SiC chip used is a MOSFET (Part No. CMPF-1200-S160B) supplied by SemiDice Inc. A sample of printed nano silver on Al_2O_3 was prepared and sintered according to earlier results. The pattern consisted of two pads; one silver pad to bond the chip on and one for reference. To bond the chip, nano silver paste (nanoTach silver paste from Virginia Tech) was used. A small amount of nano paste was applied onto the pad and the chip was assembled by placing it by hand with a light pressure. The nano silver paste has a slightly higher sintering temperature than the ink and the sample was sintered at 400 °C in a nitrogen atmosphere.

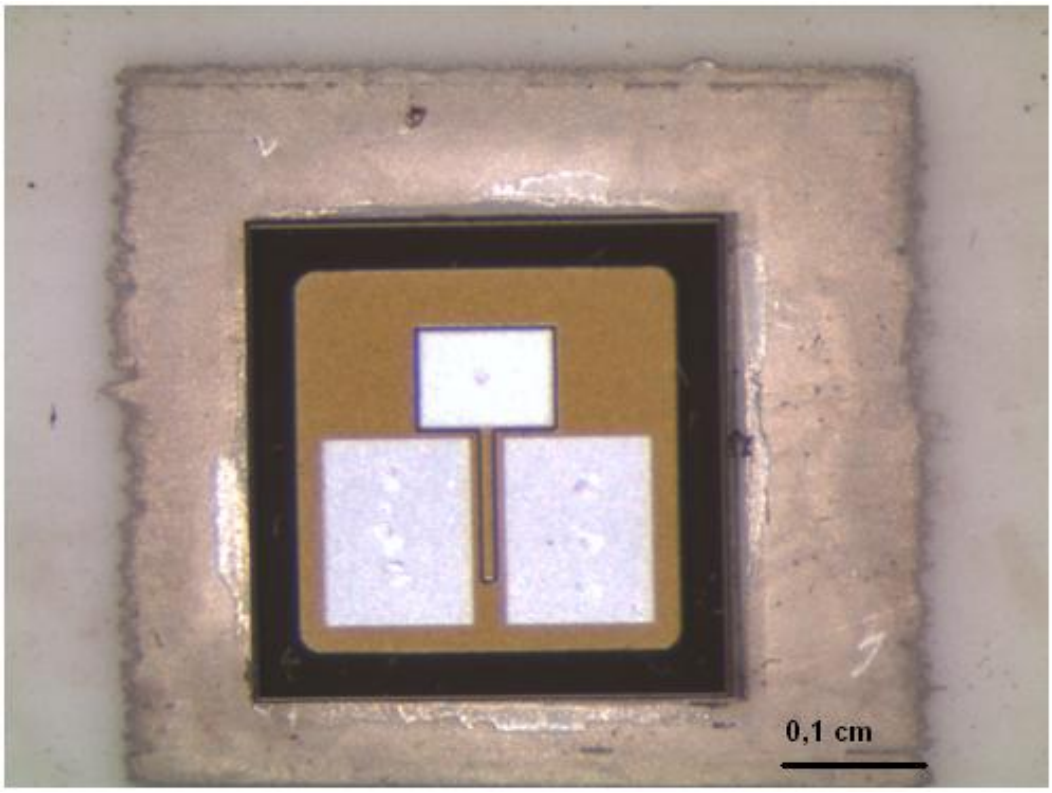

Figure 26 Si Carbide chip bonded with nano silver paste to the substrate.

To investigate the bonding between the chip and the substrate a Scanning Acoustic Microscopy (SAM) analysis and X-ray analysis was made, see Figure 28 and Figure 28. It can be seen that the nano silver paste is unevenly dispensed. During the analysis the chip fell off from the substrate. To investigate the fracture surface of the substrate and chip (see Figure 29 and Figure 30) a SEM analysis was made. The SEM analysis shows that the fracture surface of the substrate contains no silver while the chip has silver on it. See Figure 31 Figure 32.

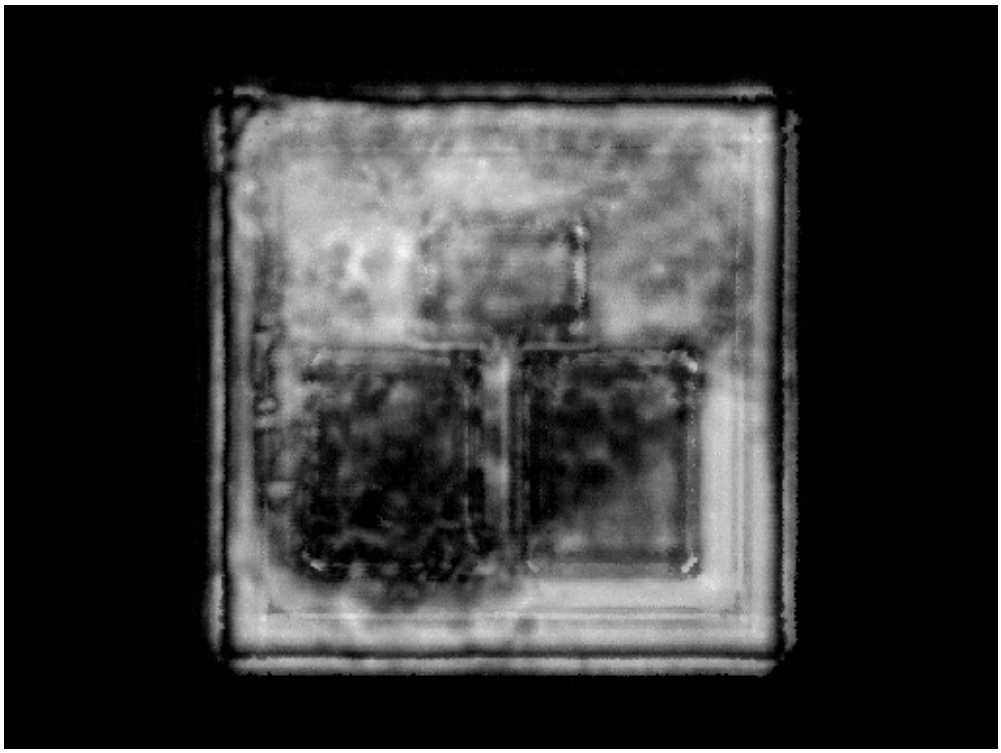

Figure 27 SAM analysis of the bonded SiC chip.

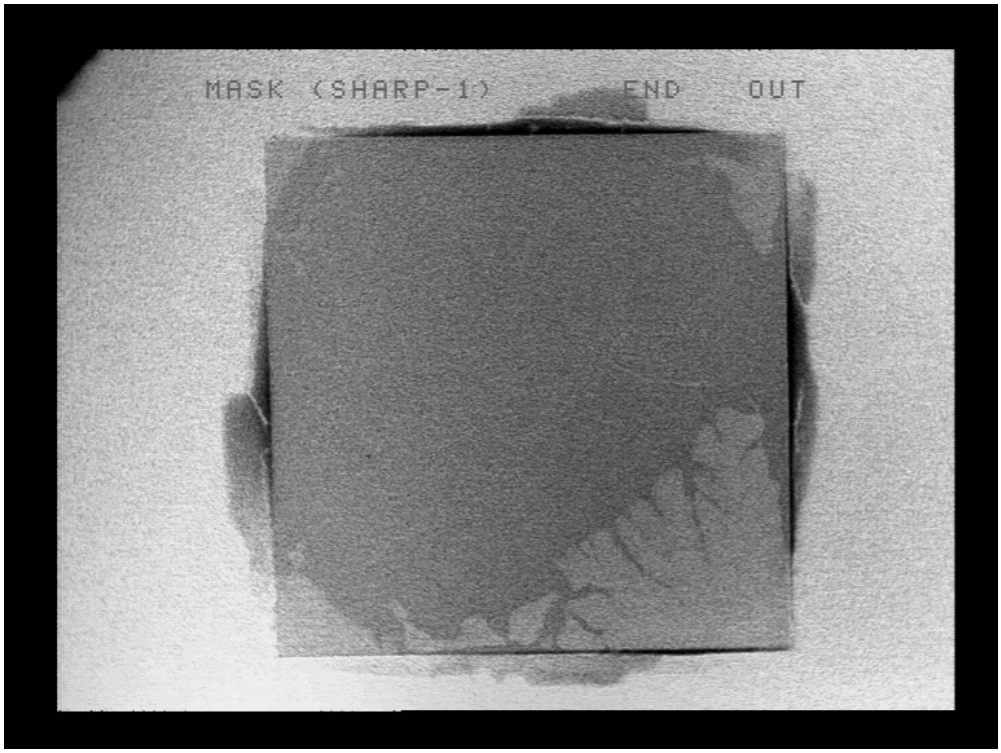

Figure 28 X-ray picture of the bonded Sic chip

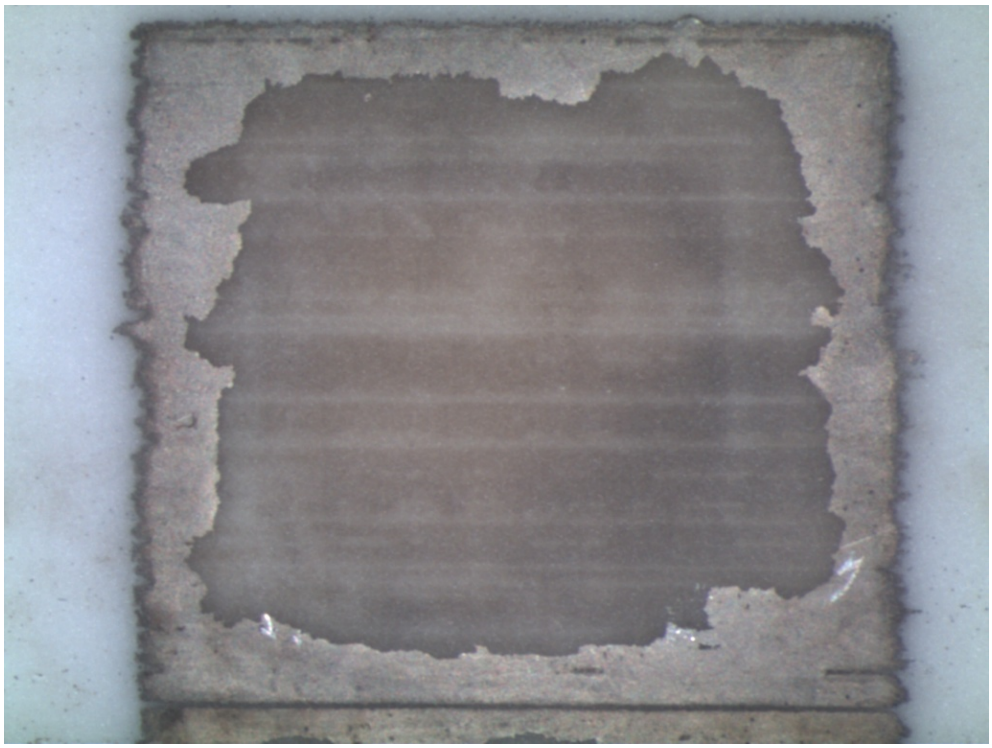

Figure 29 The fracture zone on the substrate. It can be assumed that the silver has released from the Al_2O_3.

Figure 30 The lower surface of the released SiC chip.

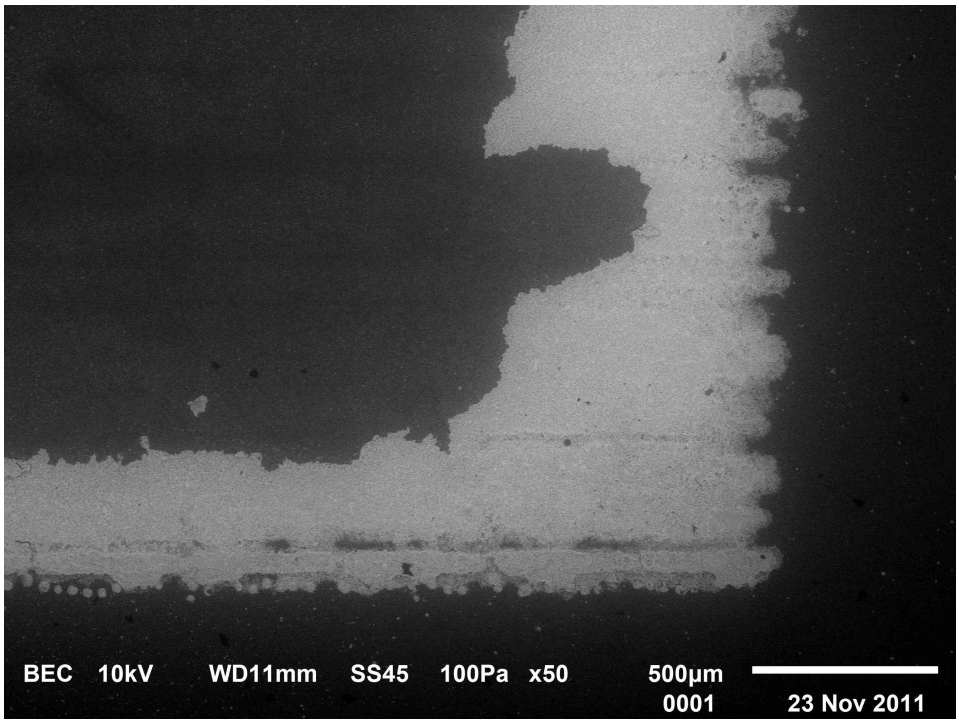

Figure 31 SEM (BSE) picture showing the fracture surface of the Substrate. The light area contains silver.

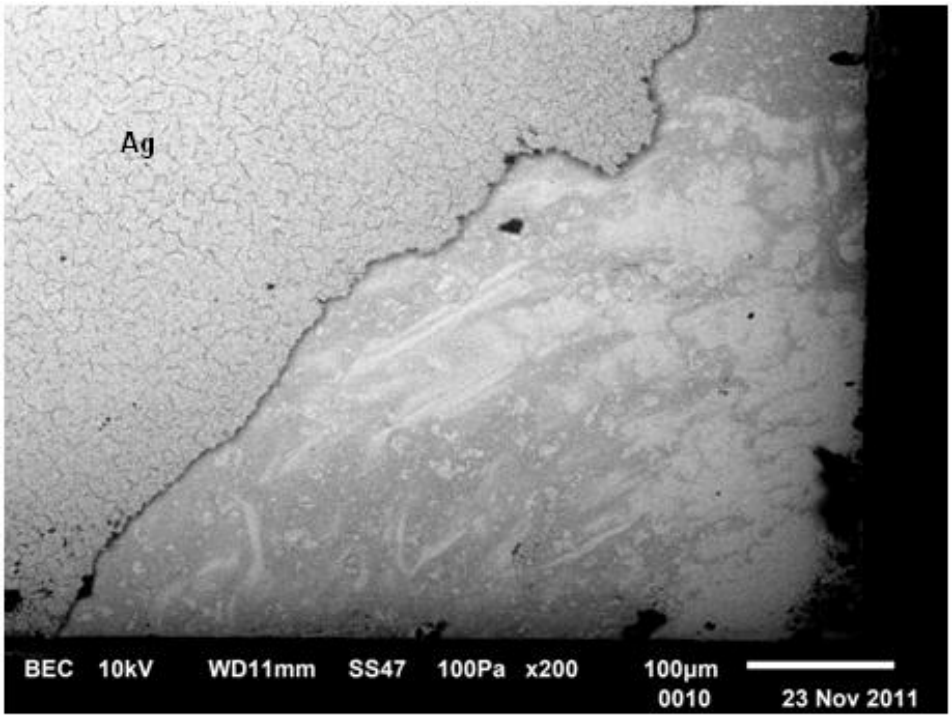

Figure 32 SEM (BSE) picture of the fracture surface of the chip.

3.4 MANUFACTURING OF DBC-SUBSTRATES

The second aim of this project has been to manufacture the substrates by etching already existing DBC-substrates. By this method the development of substrate materials is avoided and focus can be put on design and manufacturing. As the preliminary design already exists, an initial thermo mechanical analysis was performed in Ansys. The simulation results and simulation parameters are attached in Appendix B. The simulation indicates that this design is feasible. From the simulation it is seen that the maximum temperature is calculated to 368 °C from the steady-state thermal simulation with simulated air cooling, see Figure 33. To evaluate where stress is induced due to CTE mismatch, a static structural normal stress simulation was made. It can be seen in Figure 33 and Figure 34 the highest temperatures and stresses are caused around the SiC chip. The higher temperature around the vias indicates correct thermal conduction between the substrate layers. Material parameters and details are found in the appendix.

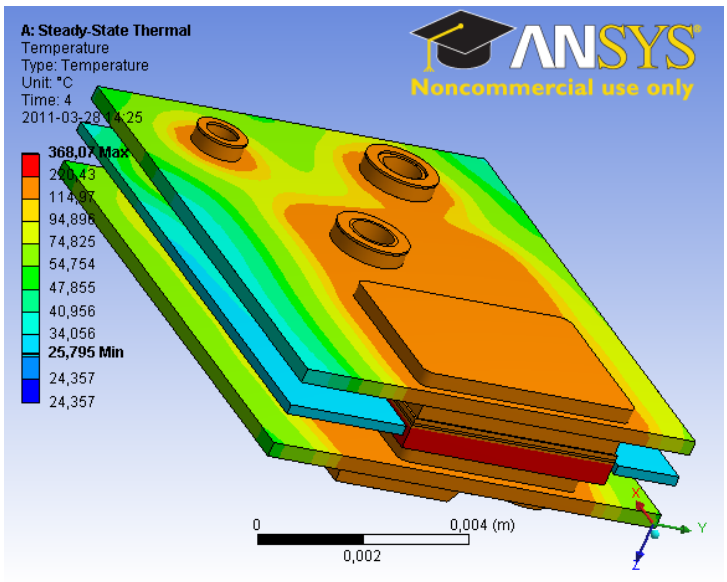

Figure 33 Steady-State thermal analysis.

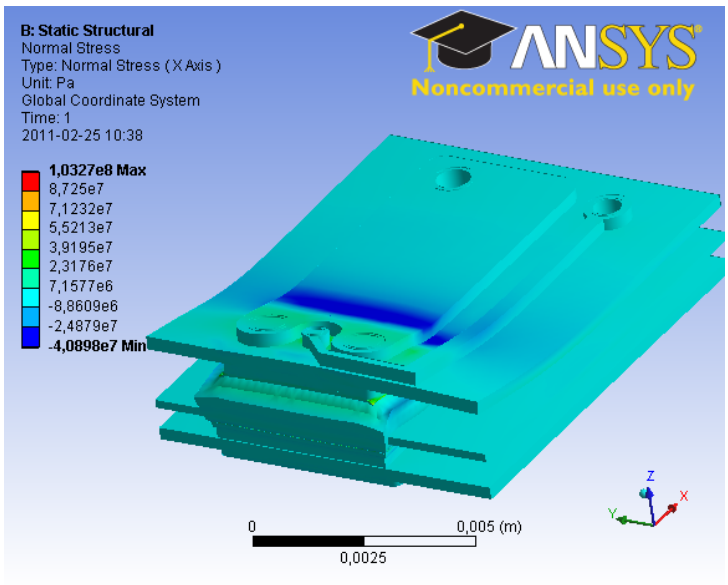

Figure 34 Static structural normal stress simulation.

To manufacture the substrates the material used is Direct Bounded Copper (DBC) substrates consisting of two copper foils (300 µm) bonded to an AlN core. The DBC:s are ordered from an industrial company (Curamic).

The preliminary design had to be evaluated in regard to the chip size and isolation distance. The DBC-substrate has extremely thick Cu layers, which complicates the etching process. During the redesign process, it was realized that the design is too complicated for etching and manufacturing. Due to the circumstances, the design has been simplified and suited for manufacturing. The new design is shown in Figure 35.

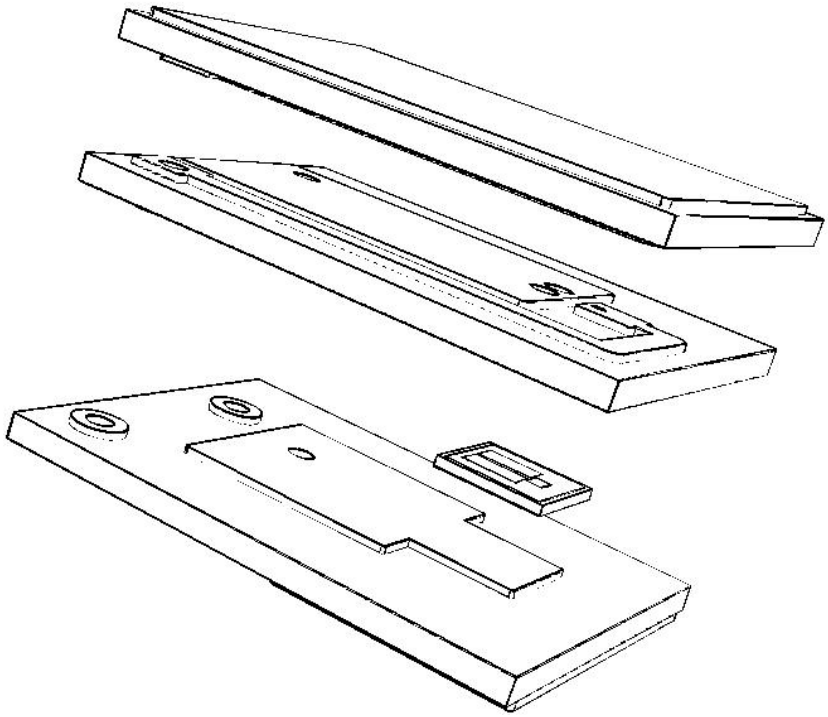

Figure 35 New design of future SiC package

Further, the 3D-cad needs to be transformed into a mask used for etching. See Figure 36 and Figure 37**.**

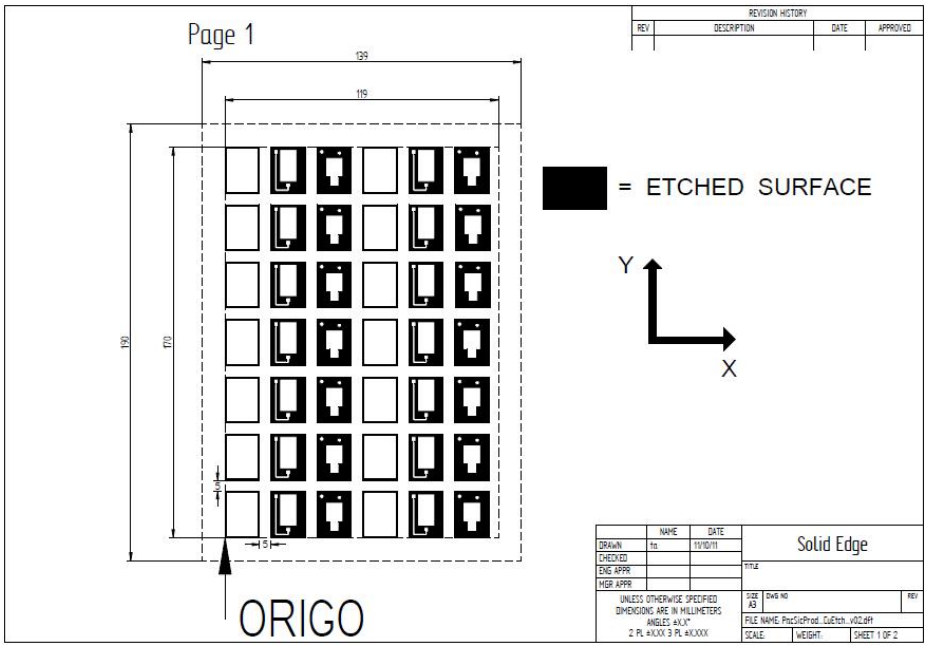

Figure 36 The mask used for etching the DBC substrates. This is the first side of the substrate.

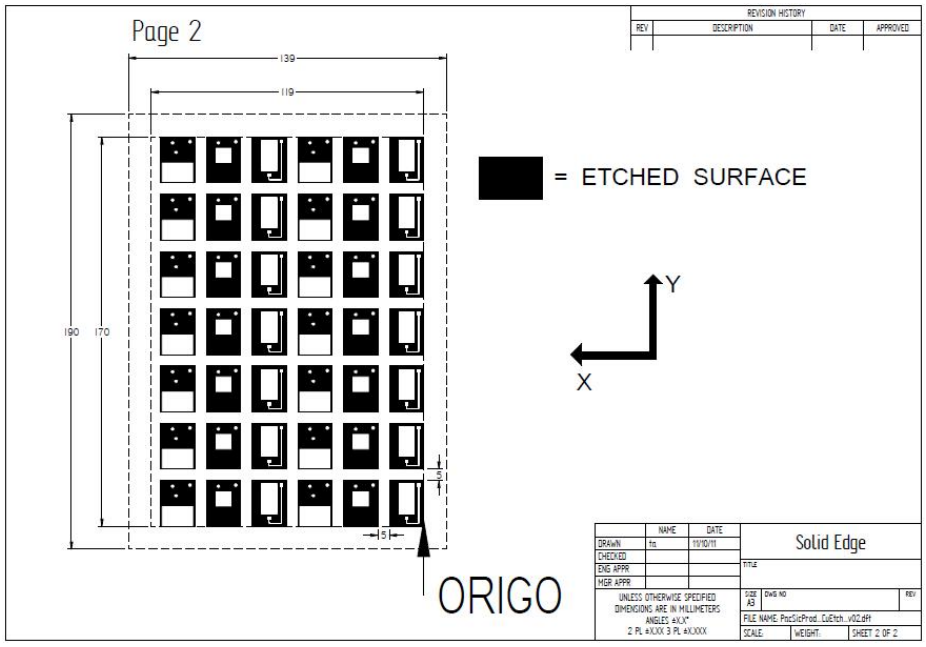

Figure 37 The mask used for etching the DBC substrates. This is the second side of the substrate.

4 DISCUSSION OF RESULTS

Many experiments have been performed during this project. This chapter will discuss the experiments and results presented in chapter 3.

4.1 TITANIUM PLATING ON AL_2O_3

The main focus during this project has been to develop substrates for SiC power electronics based on Al_2O_3. Initial attempts, with TEOT, were considered too complicated and experiments showed that it was unsuccessful to coat Al_2O_3 with TEOT to achieve titanium. SEM analysis 3.1.1 made it clear that the TEOT coating was not metallic after the sintering procedure and the coating did not attach to the surface. However, the second approach considering titanium was actually successful. The titanium (powder mixed with water) did bind to the Al_2O_3 and a metallic layer was formed during sintering. Unfortunately the application process was problematic and the thickness of the titanium was difficult to control, so we did not further develop this technique.

4.2 INK JET PRINTING OF NANO SILVER ON AL_2O_3

The most successful experiment during this project has been the ink-jet printed nano silver. This technology is of extraordinary interest, on the basis of the high potential this technology has within electronics manufacturing. The approach to print nano silver directly on Al_2O_3 is rather unique today and to the best of our knowledge similar experiments have not been made before.

Initially the tests were not successful, both regarding printing quality and results after sintering. The resolution was low and the silver ink did not attach to the Al_2O_3 surface during the sintering process. During the project our understanding of the behaviour of the nano silver ink has increased, and the most interesting observations will be discussed in the following sub chapters.

4.2.1 INFLUENCE OF SURFACE TREATMENT

First, a mechanical treatment was achieved by blasting the Al_2O_3 substrate. The mechanical treatment did not show any influence on the printing result. This may be due to the unclean industrial blasting process or due to the fact that the surface roughness has low impact on the final result.

The chemical surface treatment was successful. After a number of attempts and experiments we understood that the primer had crucial influence on the result. It is shown in chapter 3.2.3 that the primer changes the surface in a way that the wetting properties are improved. This effect is improving the quality of the printed structure, already before it is sintered. It is necessary to be able to print structures in high resolution, and in this aspect the wetting needs to be optimized. It is believed that the primer changes the surface energy in a way that the primer acquires a smaller wetting angle to the surface.

Beyond the aspect of wetting, the primer seems to contribute to a better binding between the ink and the Al_2O_3. The results indicate that primer treated samples have much better adhesion between ink and Al_2O_3 compared to samples not prepared with primer. It may be due to the improved wetting properties, but in addition to that there may be other chemical mechanisms that provide to a better binding. One hypothesis is the amino silane component binds to the ink,

but exactly which mechanisms that are involved must be further investigated and is not in the scope of this project.

The SEM analysis (chapter 3.2.5) did not give any clear information about the silane primer effects. Though, it may be possible that the difference in Figure 23 and Figure 24 can be a result of uneven application of the primer. As seen in the second SEM picture (Figure 24), it seems the silver coating has no or less contact with the substrate in some areas. If it could be shown that this area has lack of silane, then the effect of the primer could be clear. Unfortunately, the primer is impossible to see in the SEM pictures and no conclusions can be made. It is important that the primer is applied thin and evenly over the printing area. Our method was to apply the primer by hand, which may lead to uneven coverage. To develop a more controlled process would be favourable. Noteworthy is that it was impossible to do a SEM analysis of a sample not prepared with silane, because the adhesion of the ink was so low that the SEM preparation was not possible.

4.2.2 Influence of sintering conditions

In chapter 3.2.4 the influence of sintering temperature and temperature ramp was investigated. The results show that both these parameters are important to take into consideration. It is shown that the nano silver ink is sintered already at temperatures as low as 250 °C (for 30 minutes). This is important information to consider if the ink will be used in the manufacturing of temperature sensitive components. Further, higher sintering temperatures did not seem to give any advantage. The sintering time has not been evaluated during this project; focus has been on the maximum temperature. The sintering time is an important parameter but due to the thin ink layers (3-5 µm) it is likely to have less influence than the maximum temperature.

The temperature ramp had a clear influence on the result after sintering. With a slower temperature ramp used during the sintering, the adhesion was better between the ink and the substrate. This may be explained by the fact that the nano silver particles are coated with a dispersion agent to prevent aggregation. During the sintering process, the heat removes the dispersion agent and if the temperature increases too fast, it may lead to solvents shut-in into the ink. Further, the sintering process causes shrinkage of the sintered material and may cause cracking due to stress. A low temperature ramp should be considered to be favourable.

4.2.3 Conductivity of the sintered nano silver ink

The results from the resistance measurement and the calculations of the resistivity, indicates that the nano silver ink has sufficient performance. The result that was achieved from the experiment is giving a resistivity value slightly higher than pure silver. This has to be considered as a good result. The sintered nano silver ink cannot have a performance as good as pure silver, due to several reasons. From the SEM study (Figure 23), we know that the nano silver has pores inside which limits the current to flow through the material and should lead to higher resistivity than for pure silver. This may be improved by increasing the sintering time. Further, the nano silver ink contains solvents and other chemicals that will affect the resistivity negatively.

The calculated mean value from 3.2.6 is 8,75e-7 Ω/m which can be compared with bulk silver with the resistivity of 1,59e-8/Ωm. To reflect the influence of measurement errors some assumptions are made:

If the thickness of the silver ink has an error of ± 2 µm and the resistance value ±10 Ω, the final result would give an resistivity value varying about 0,875 ± 0,8 µΩ/m. This indicates that the calculated value including error estimation may be close to bulk silver and the ink is considered to have a great electrical performance.

4.2.4 Other aspects involving the adhesion of nano silver ink to Al_2O_3

It has been observed that the result may sometimes be inadequate, independently of the chosen process parameters. This may have been an effect of bad primer coverage explained in the last chapter, but there is no obvious answer. During the printing experiments, a surface phenomenon has been identified, see Figure 38. This is probably due to sedimentation of nano silver particles in the ink. The sedimentation effect is a result of the sample not being sintered directly after printing. A contributing reason may also be the thickness of the printed ink. Since we use a prototype printer, the control of the thickness may be inadequate.

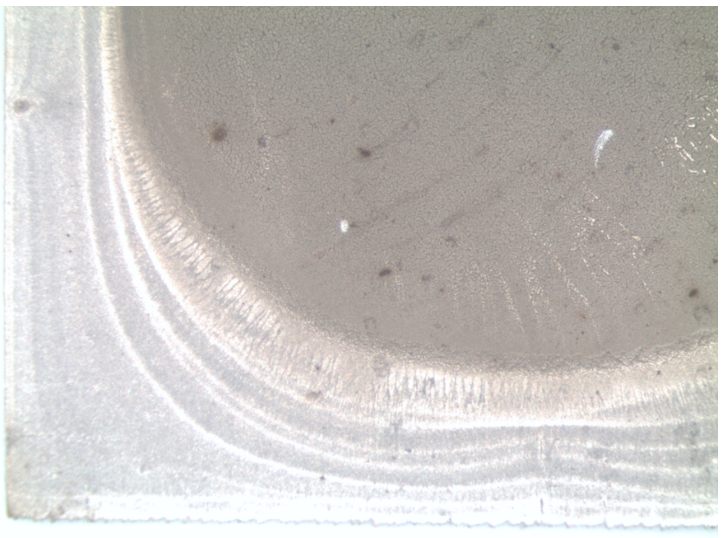

Figure 38 Sedimentation of silver nano particles. In the dark are particles has gathered and the distribution of particles is not under control.

4.3 Bonding of SiC chip to nano silver printed substrates

The bonding between the SiC chip and the substrate was not sufficient. After the sintering it initially had adhesion, but a fracture happened during the analysis. As can be seen in the SAM and x-ray pictures, the nano silver paste was unevenly applied. Probably this is not the cause of the failure, as the SEM analysis and microscopy pictures from chapter 3.3 indicates that the fracture has occurred between the Al_2O_3 and the printed silver. That is to say, the fracture is not between the chip and the nano silver. This theory is confirmed by the SEM analysis where it can be seen that the Al_2O_3 surface has a total lack of silver content. The printed silver has probably lost its adhesion to the substrate during the second sintering process, i.e. an interfacial fracture has happened. Before the bonding experiment, the silver had good adhesion to the Al_2O_3 which indicates that the substrate did not manage the second sintering. A possible reason to this could be that the primer did not manage higher temperatures.

5 CONCLUSIONS

There is a need of a new material in tomorrow's high power components. Si, which today is the common material, will not be able to meet the future demands of the high power/temperature electronics market due to its fundamental material properties: low band gap energy and poor thermal conductivity. SiC, on the other hand, has a larger band gap, resulting in a higher break down voltage and potential to handle higher blocking voltages and currents. Moreover, SiC handles high temperature better than Si due to its superb thermal conductivity. Though, it's not only the semiconductor devices that limit future power system development – rather it is the packaging of these new components that creates the technology barrier. Substrates based on AlN are identified as optimal for SiC components, due to the match of thermal expansion coefficient and the good thermal conductivity. If price is taken into consideration substrates based on Al_2O_3 gives the best value for most applications.

This master thesis presents a method to print nano silver directly on Al_2O_3 for manufacturing of substrates. To achieve good results there are some critical process parameters identified:

- The surface preparation of the Al_2O_3 substrate is fundamental for a successful result. The surface cleanliness is important and it has been shown that silane based primer is successful in achieving a good result for printing quality and adhesion between silver and Al_2O_3.
- The sintering process parameters are important for the adhesion between the silver and Al_2O_3. Sintering parameters which influence the result are: temperature, time and temperature ramp.
- Sedimentation of nano particles in the ink is a problem. If the sample is not sintered directly after printing, sedimentation effects which lead to poor adhesion after sintering may occur.
- Experimental results indicate that the electrical resistivity of the sintered nano silver ink is good and comparable with pure Ag.

The alternative to ink jet printed substrates has been AlN based DBC substrates. Conclusions from this approach have been:

- Simulation results indicate that the design of package is feasible and could handle the future demands of high power SiC components.
- It is important to consider the thick Cu layers when designing the substrates. Otherwise is may lead to problems during etching.
- This method may be a faster way to create the substrate due to conventional etching technology. On the other hand, future manufacturing processes will be more expensive as well as suffer from longer "time to market" compared to ink jet printed substrates.
- There is no need to develop the substrates in house; DBC-substrates are industrially manufactured.

5.1 SUGGESTIONS FOR FUTURE WORK

The overall long term aim of this work is to develop a new, innovative, package for SiC chips. This work has developed a method to manufacture the substrates. This section presents some important parts where more studies are needed to proceed with this work.

Regarding the silver printed Al_2O_3 substrates:

- Deeper investigation of the mechanisms influencing the adhesion of nano silver to Al_2O_3, including optimization of sintering conditions and preparation of the Al_2O_3 substrate.
- Evaluate the long term reliability of the ink jet printed substrates. How does the silver respond to high temperature/power cycling?
- Investigate whether it is possible to bond components to the Ag metalized substrate by nano silver paste.

Regarding the AlN DBC substrate:

- Evaluate if the etching process has been successful. Is the isolation distance in the current design adequate? Are there problems related to under-etch, due to the thick Cu layers?
- Proceed with the assembly process: water cutting, die attach and cooling.
- Investigate the reliability of the package by long and short term test. As a suggestion initially by HALT and HASS testing.

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Appendix A

Table 1. Physical properties of common semiconductor materials.

Material	E_g (eV)	n_i (cm^{-3})	ε_r	μ_n ($cm^2/V \cdot s$)	E_c (MV/cm)	v_{sat} (10^7 cm/s)	λ ($W/cm \cdot K$)	*Direct/ Indirect*
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7×10^{-1}	11.1	350	1.3	1.4	0.8	I
InN	1.86	$\sim 10^{3}$	9.6	3000	1.0	2.5	-	D
GaN	3.39	1.9×10^{-10}	9.0	900	3.3	2.5	1.3	D
3C-SiC	**2.2**	**6.9**	**9.6**	**900**	**1.2**	**2.0**	**4.5**	**I**
4H-SiC	**3.26**	**8.2×10^{-9}**	**10**	**720^a 650^c**	**2.0**	**2.0**	**4.5**	**I**
6H-SiC	**3.0**	**2.3×10^{-6}**	**9.7**	**370^a 50^c**	**2.4**	**2.0**	**4.5**	**I**
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20	I
BN	6.0	1.5×10^{-31}	7.1	5	10	1.0*	13	I
AlN	6.1	$\sim 10^{-31}$	8.7	1100	11.7	1.8	2.5	D

Note: *a* — mobility along a-axis, *c* — mobility along c axis, *— estimate.

Appendix B

Data from resistivity measurements and resistivity calculations belonging to chapter 3.2.6

Resistivity, ρ [Ωm] $\rho=R*A/L$

Conductivity, σ [S/m] $\sigma=1/\rho$

Table 1 Resistance values measured in experiment 3.2.6

50 pixlar	**50 pixlar (2)**	**100 Pixlar**	**100 pixlar (2)**	**150 pixlar**	**150 pixlar (2)**	**25 pixlar**
10,98	18,13	7,2	7,72	7,09	5,22	51,27
16,92	19,32	9,9	6,27	9,02	4,67	23,55
11,03	13,99	6,97	10,65	5,07	3,98	50,26
14,2	19,84	7,3	9,92	4,31	5,55	50,24
14,23	17,53	9,45	11,72	5,98	7,97	49,25
16,23	12,54	9,21	10,01	4,52	3,31	49,37
11,44	13,03	6,73	7,32	5,29	3,38	63,52
19,54	20,02	10,31	8,11	5,07	5,41	47,53
17,36	12,45	6,15	10,13	4,97	4,02	49,91
12,23	12,72	7,12	5,29	8,11	4,29	51,17

Pixels	50	100	150
Resistance mean [ohm]	15,1865	8,374	5,3615
Höjd [m]	4,00E-09	4,00E-09	4,00E-09
Bredd [m]	0,002	0,004	0,006
Längd, L [m]	0,042	0,042	0,042
Tvärsnittsarea, A [m2]	8E-12	1,6E-11	2,4E-11
Resistance [Ω]	15,1865	8,374	5,3615
Resistivity [Ωm]	**2,9E-09**	**3,19E-09**	**3,1E-09**
Conductivity [Sm-1]	3,46E+08	3,13E+08	3,26E+08

Appendix C

in table 1 material selections and properties are shown. Materials are manually specified in Ansys Workbench in regard to relevant properties for the simulation.

The model of the package includes one SiC-chip that produce heat. A steady-state thermal analysis is used to study the resulting temperatures caused by the heat developed in the chip.

Table 1 material selections and specified properties of the materials

	Material	**Isotopic Coefficient of thermal expansion (K^{-1})**	**Isotopic thermal conductivity (W/m*K)**	**Density (kg/ m^3)**	**Young's Modulus (Pa)**	**Poisson's Ratio**
Top ceramic board	AlN	5,27e-6	0,0285	3255	3,08e+11	0,287
Middle ceramic board	AlN	5,27e-6	0,0285	3255	3,08e+11	0,287
Bottom ceramic board	AlN	5,27e-6	0,0285	3255	3,08e+11	0,287
Solder	Ag	1,89e-5	429	10490	1,552e+11	0,37
Transistor SiC bulk	SiC	3,4e-6	F(T), tabulated, se *fig 1*	3210	6e+09	0,495
Transistor source metallization	Ag	1,89e-5	429	10490	1,552e+11	0,37
Transistor drain metallization	Ag	1,89e-5	429	10490	1,552e+11	0,37

Transistor gate metallization	Ag	1,89e-5	429	10490	1,552e+11	0,37
Filled vias	Ag	1,89e-5	429	10490	1,552e+11	0,37
Gate vias	Ag	1,89e-5	429	10490	1,552e+11	0,37
Source vias	Ag	1,89e-5	429	10490	1,552e+11	0,37

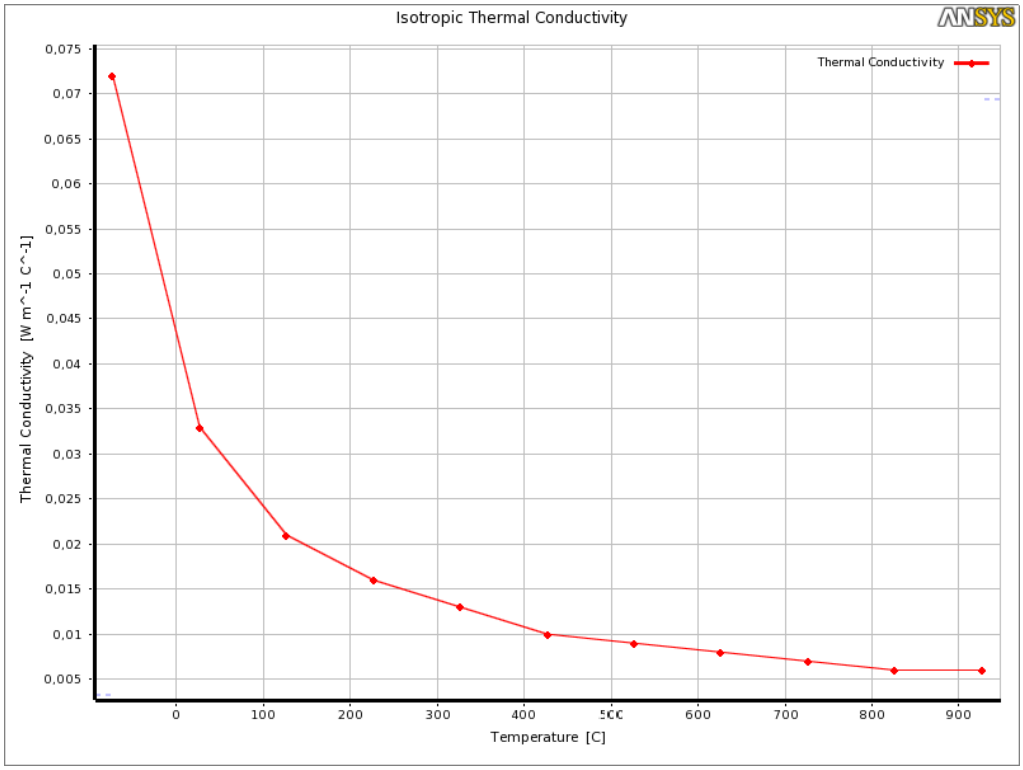

Figure 1. SiC temperature dependence.

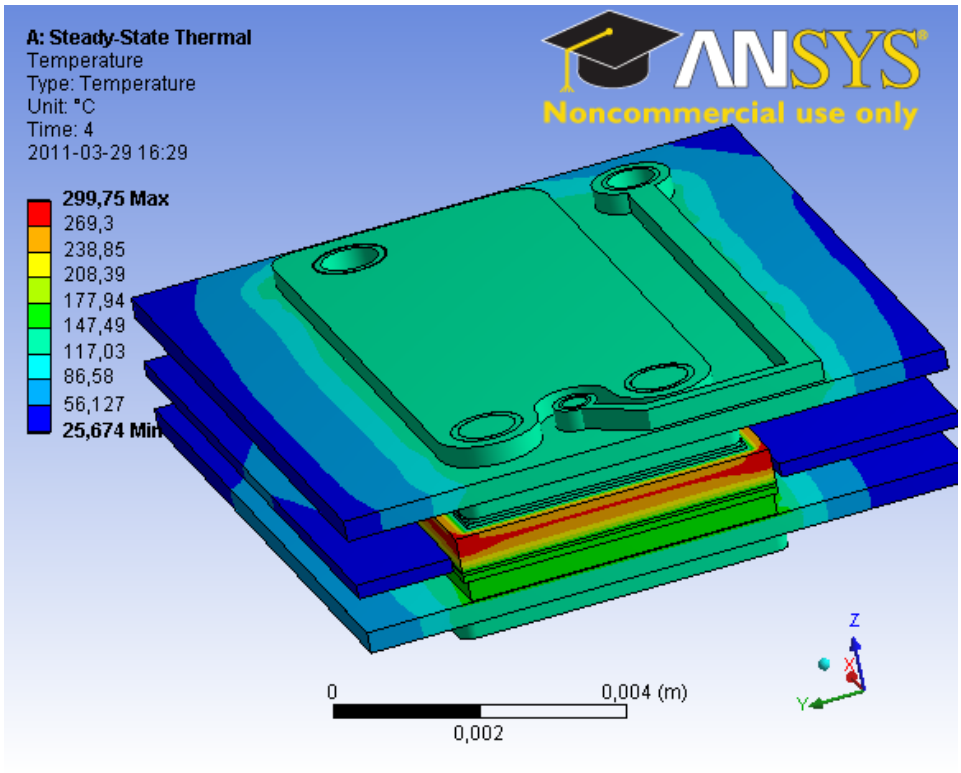

Figure 39 Simulation result of the preliminary SiC package design.

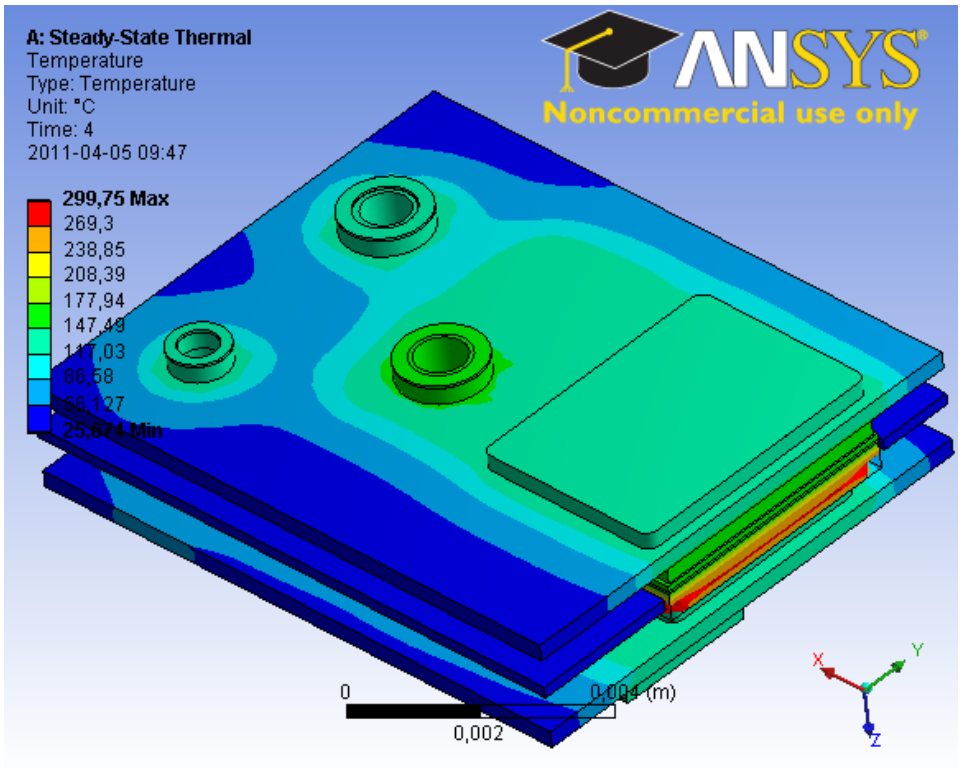

Figure 40 Simulation result of the preliminary SiC package design. Bottom view.