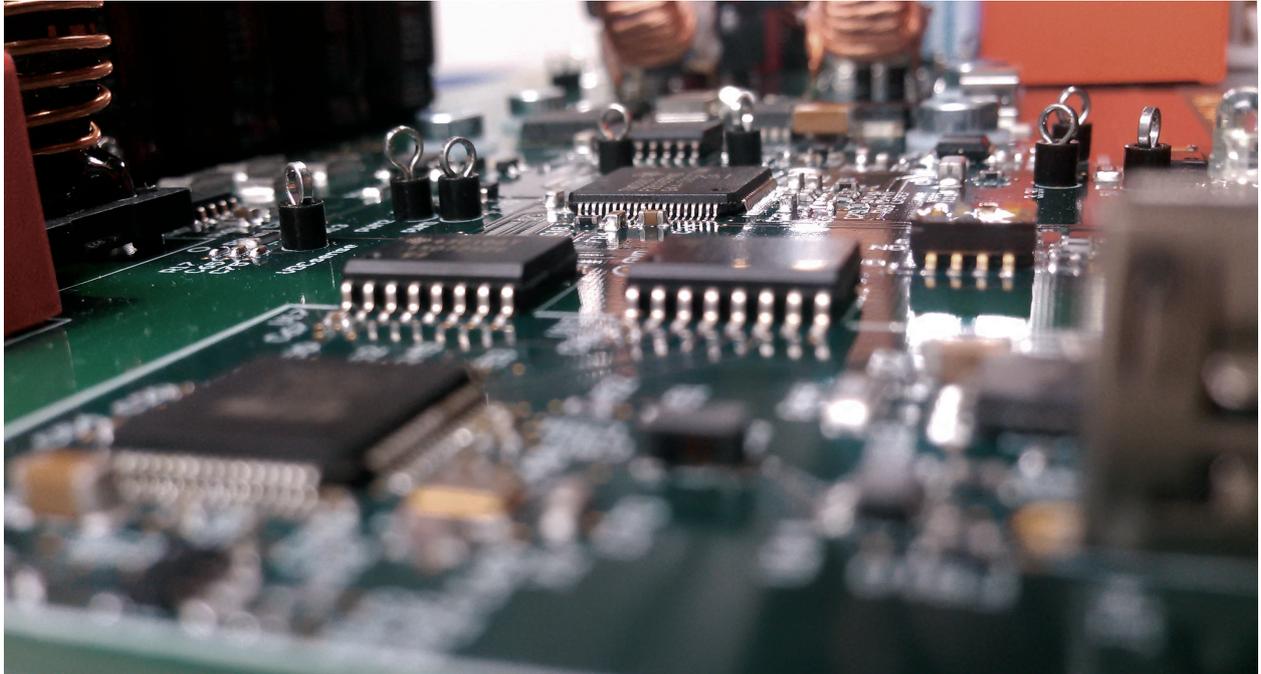




**CHALMERS**  
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# **Design of a high switching frequency interleaved step-up converter with digital interface for Power Factor Correction applications**

A Master of Science thesis in which a step-up converter, capable of supplying 1 kW at 400 VDC using 230 VAC while operating at a switching frequency of 1 MHz, has been developed

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Cover: Close up photo of the assembled converter with mounted test points.

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## Abstract

Power Factor Correction (PFC) circuits can be used to mitigate problems with harmonics associated with rectifying AC to drive a DC load. A two channel step-up converter with correctly controlled switches can be used as a PFC. High frequency switching gives the advantage of physically small boost stage inductors and filters. The purpose of this thesis was to investigate the possibilities of utilizing high switching frequencies while maintaining a high efficiency.

A short literature study about the subject was made which was followed by component choices based upon the studies and relating calculations. This was succeeded by the design and manufacturing of a circuit board. All surface mounted components were attached and the verification of the circuit was carried out by systematically mounting the remaining through hole components and writing testing software. Performance evaluation was the last thing to be done.

The main result is a working dual channel step-up converter capable of providing 1 kW at 400 V using 1 MHz switching frequency, however at the expense of the efficiency which dropped to just above 94 %. More work, especially software related work, is needed before the device can be used as a PFC and there are also possible improvements that can be implemented in order to increase the efficiency.

Given that the switching frequency aimed for was reached and that there are possible improvements to the efficiency, smaller boost stage inductors and filter components are possible which can increase the power density of devices utilizing PFCs.

**Keywords:** PFC, step-up converter, boost converter, high frequency, SiC, interleaved, digital control



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# 1

## Introduction

### 1.1 Background

Power electronics are used in many common appliances today. Common household products such as computers, TVs and mobile phone chargers but also modern light bulbs, stoves and fridges all use power electronics. The use of power electronics have brought more efficient, smaller and cheaper products to the market. However, many electronic devices run on direct current, DC, in contrast to alternating current, AC, which is available in the household outlets. To be able to connect a DC powered device to the grid, a rectifier along with a smoothing capacitor are commonly used [1].

A simple rectifier with a smoothing capacitor can consume current containing high levels of harmonics. If the grid's source impedance is non zero, the distorted current will inject harmonics onto the grid voltage, which can propagate to other grid connected devices and in the worst case cause them to malfunction [1]. Harmonics can create heating problems in the transmission system and interfere with small-signals [1]. Currents with high levels of harmonics will also increase the need for greater current handling capabilities in components and thus decreasing device power density.

One solution to these issues is spelled Active Power Factor Correction, APFC - hereby only PFC, which is a power electronic device which is connected between the problematic load and the rectified grid. The job of the PFC is to control the current in such a way that it resembles the sine wave of the grid voltage. This is, in this case, done by controlling two switches of boost stages.

Boost inductors as well as EMI filter, bulk capacitors etc. takes up significant space which in turn reduces the power density of the power electronic device that the PFC is installed in [2]. An increased switching frequency allows for smaller boost inductance values as well as smaller EMI filters. It is therefore highly relevant and interesting to study if it is possible to increase the switching frequency of a PFC module without compromising other performance aspects.

A quick investigation shows that there are many integrated PFC controllers available

on the market where the vast majority are designed to operate at frequencies of 500 kHz or below. The use of an integrated controller is however less flexible than using a microprocessor which can be programmed to operate exactly as the designer want it to do. This is convenient in the design process when different operation modes are tested, but it is also useful in the manufacturing stage where changes and fixes quickly can be implemented.

### 1.2 Aim/Purpose

The purpose of this project is to develop and build the hardware to a digital active PFC which should operate at a switching frequency of 1 MHz and shall be able to deliver 1 kW of power at a voltage level of 400 VDC. The main functionality of the PFC is controlled by a digital microprocessor.

The project is done in order to investigate if it is possible to operate such a PFC hardware at the stated switching frequency, built by as of today commercially available components. The result of the project will be a printed board assembly, PBA, complete with an enclosure and interface.

### 1.3 Problem description

The digital active PFC should provide 1 kW of power at a voltage 400 VDC using a single phase 230 V 50 Hz input while maintaining a power factor above 0.98. However, the hardware will only be tested with various DC input voltages as the PFC software needs to be ready in order to test with AC voltage. The efficiency should not drop below 96 %. The switching frequency of the boost circuit should be 1 MHz and the layout should be a two channel interleaved design. The circuit should be cooled using air. In case of power supply interruptions of 20 ms the output voltage should not drop below 300 V. A test code for the processor will have to be written in order to test the hardware.

### 1.4 Scope

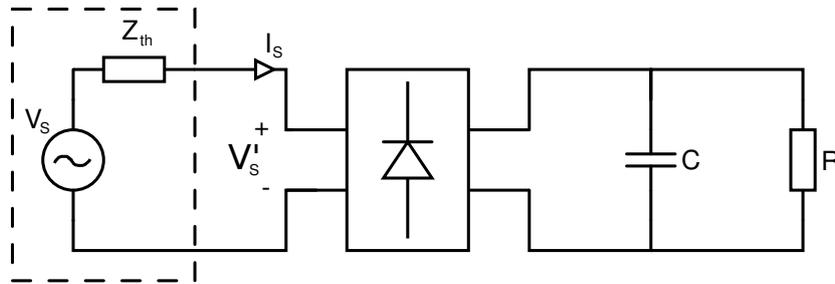
In order to be able to finish the thesis in time it is important to clarify what will not be done or investigated. Only one PFC topology will be investigated in order quickly start the design process. The printed circuit board, PCB, will have no size restrictions since it will not be designed as a commercial product and therefore does not have to compete on the market. A important design delimitation is that the PFC only needs to be able to handle 230 VAC as input and that the final construction does not need to pass a conducted EMI test as it only is a prototype and not a commercial product. The software that the microprocessor need in order to operate as a PFC will be investigated but not fully implemented.

# 2

## Theory

### 2.1 Issues with AC rectification and solution using PFC

To illustrate the problems with only using a rectifier and smoothing capacitor to power a DC load, the simple circuit and wave forms presented in figure 2.1 and 2.2 are to be analysed. The rectifier will only conduct when a pair of diodes is forward biased, thus the shape of the current can not be one pure sine wave and harmonics are therefore introduced into the system. This can be seen by investigating the current, red waveform, and one can easily confirm that it deviates from a sine wave. Because of the introduced harmonics and a non zero equivalent Thevenin impedance ( $Z_{th}$ ) the voltage at the connection ( $V'_S$ ) point will deviate from the 50 Hz sine ( $V_S$ ) as depicted by the blue lines in figure 2.2.

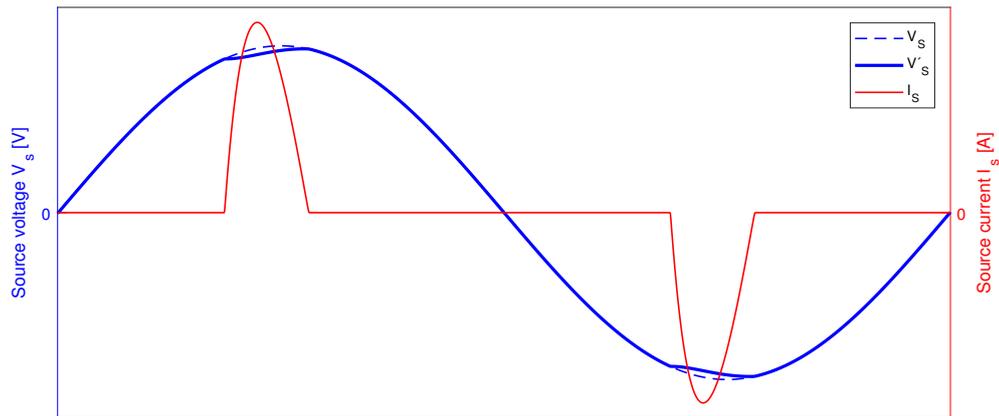


**Figure 2.1:** A simple AC rectification circuit connected to the grid with a non zero Thevenin equivalent source impedance.

The resulting power factor (PF) can be calculated by investigating the harmonic content of the current and using [1]

$$PF = \frac{1}{\sqrt{1 + THD^2}} DPF \quad (2.1)$$

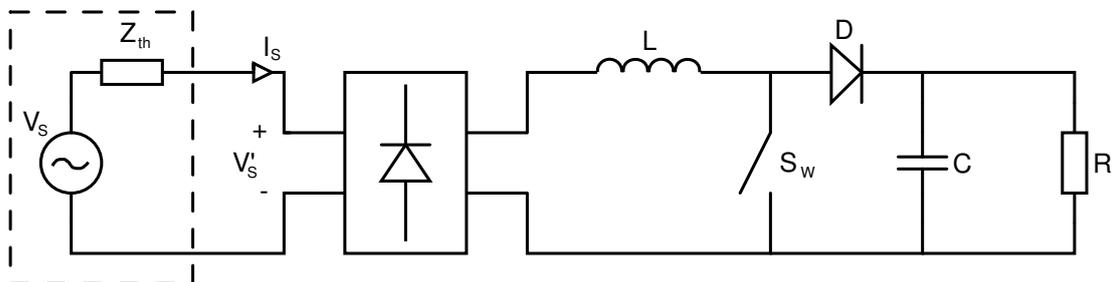
where THD is the Total Harmonic Distortion and DPF is the Displacement Power Factor. The THD can in turn be calculated as [1]



**Figure 2.2:** Corresponding current and voltage waveforms to the simple rectifying solution.

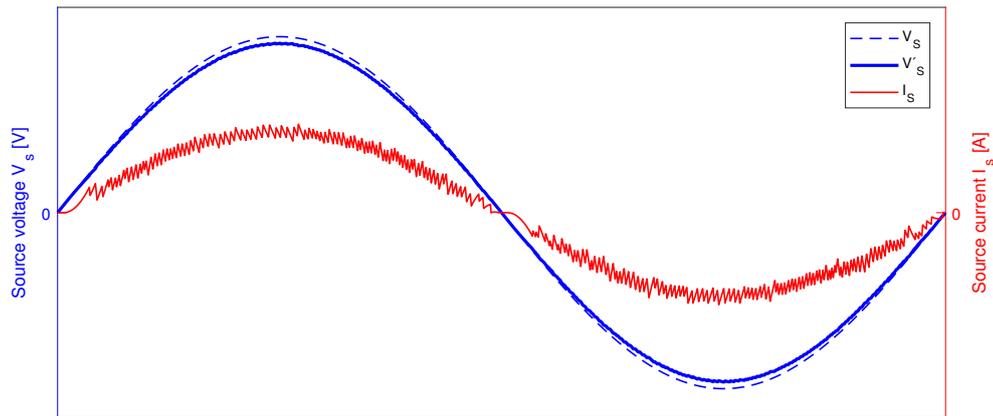
$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \quad (2.2)$$

where subscript  $h$  indicates the order of the harmonic. As mentioned in the introduction it is possible to control the current drawn by a load by implementing a boost stage in series in between the load and the rectified grid voltage. The operation of a boost converter is off course well known to the reader but the main point in this case is that the current can be controlled and actively shaped by operating the switch and taking advantage of the inductors inherent resistance to change of current. This is demonstrated in figure 2.3 which depicts the same circuit as shown in figure 2.1, but with an implemented boost stage. The waveforms with the new implementation is shown in figure 2.4.



**Figure 2.3:** Implementation of a boost stage between the Grid and the simple rectifier and load.

Closing and opening of the switch corresponds to the indicated positive and negative slopes respectively and by timing the switch correctly it is possible to mimic a sine wave with a superimposed high frequency ripple. The switching speed of the boost

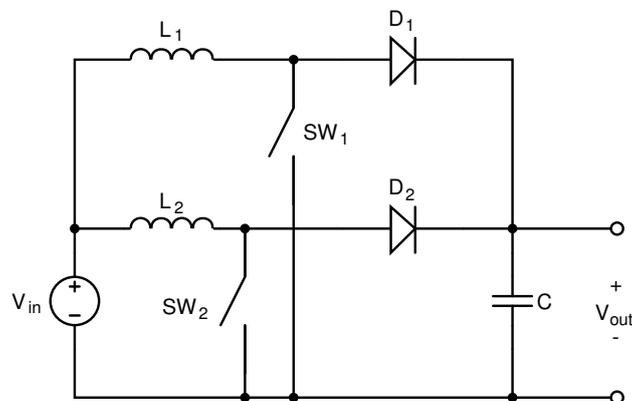


**Figure 2.4:** Corresponding current and voltage waveforms to the simple rectifying solution with boost stage.

switch will hereafter only be referred to as switching frequency ( $f_s$ ). The higher the switching frequency, the lower the high frequency ripple amplitude will be. If the ripple is allowed to be constant the inductance can instead be reduced. An increased switching frequency also allows for smaller values, and therefore size, of the filter components used for filtering the ripple [2].

## 2.2 Interleaved step-up booster circuit

A booster which is designed to work in interleaved operation have two (or several) channels. This is done by adding another switching stage in parallel with the original stage in parallel with the original stage. One stage consists of an inductor, a diode and a switch. Such a booster configuration is depicted in figure 2.5. Even though the complexity of the circuit



**Figure 2.5:** Simple sketch over a dual interleaved boost converter.

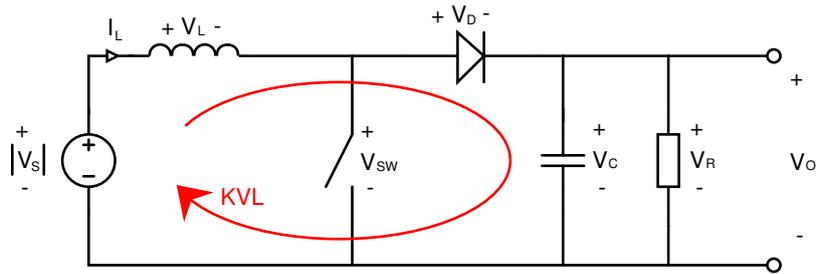
increases when two channels are used, it also implies several advantages: The two switches are operating  $180^\circ$  out of phase from each other, which allows the stages to divide the load current evenly between them. This gives a more distributed heat dissipation which decreases the requirements of active cooling. The power handling requirements of the solid state components are not as narrow as if only one channel is used. Two smaller inductors can be used instead of one large and as the peak current per inductor is lower than using only one inductor increases the possibilities of core material choice. The use of two channels also decreases the current ripple from the input source.

## 2.3 Inductor design

One important component in any step-up converter is the inductor. It needs to be able to handle the peak current while still have low losses and (depending on requirements) be as physically small as possible. It may not be possible to buy a suitable power inductor 'off the shelf' as the requirements can vary a lot. In that case it is necessary to design an inductor from scratch. But in any case the necessary inductance needs to be calculated first.

### 2.3.1 Inductance value needed based on allowed ripple

A single channel step-up converter of a PFC circuit assuming ideal rectification and components can be drawn according to figure 2.6.



**Figure 2.6:** KVL in boost stage in order to find inductance value design equations.

Applying KVL when the switch is open results in the following expression,

$$V_L + V_D + V_o - |V_s| = 0 \quad (2.3)$$

where

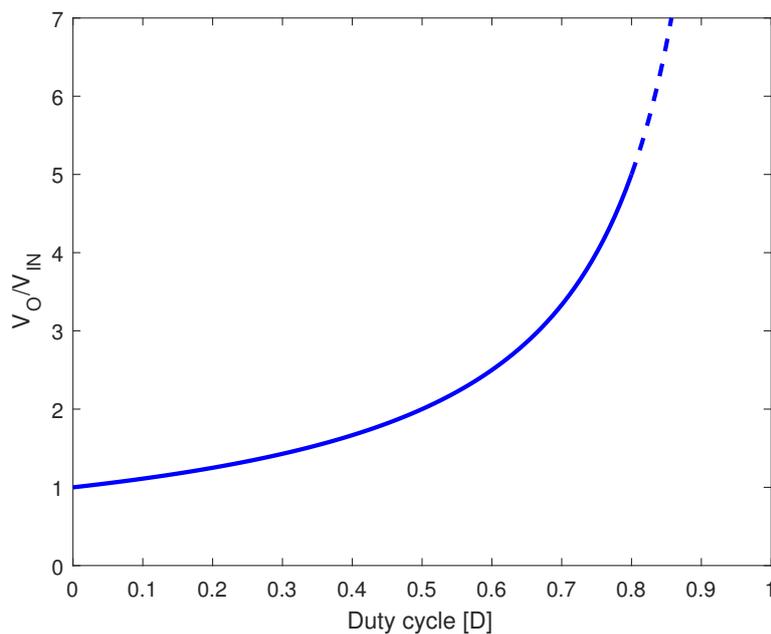
$$V_L = L \frac{di_L}{dt} = -L \frac{\Delta i_L}{\Delta t} = -L \frac{\Delta i_L f_s}{1 - D} \quad (2.4)$$

The maximum inductor ripple ( $\Delta i_L$ ) occurs on the peak of the input voltage [3]. Knowing this, ignoring the diode voltage drop and combining (2.3) and (2.4) gives

$$L = \frac{V_o - \sqrt{2}V_{s,RMSmin}}{\Delta i_L} \frac{1 - D}{f_s} \quad (2.5)$$

where  $D$  is the duty cycle of the step-up converter and  $V_{s,RMSmin}$  is the RMS voltage of the grid during low line operation. Low line operation is the lowest RMS grid voltage that can occur on the line without being considered as a fault. So in order to find the inductance needed the duty cycle of a two channel step-up converter needs to be investigated. The duty cycle impact on the output/input voltage for a single channel step-up converter is depicted in figure 2.7 and the duty cycle at the peak of the supply voltage can be calculated using

$$D = \frac{V_o - \sqrt{2}V_{s,RMSmin}}{V_o} \quad (2.6)$$



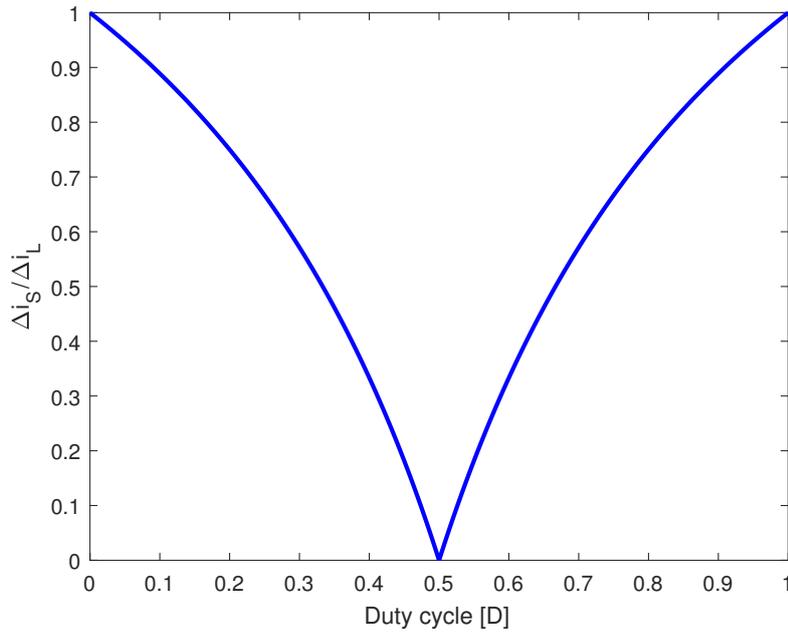
**Figure 2.7:** Voltage boosting characteristics of a single channel step-up converter.

The inductor ripple in the single channel step-up converter is the same as the input ripple ( $\Delta i_s$ ) but when using two channels the input ripple as a function of the duty cycle can be written as [3]

$$\Delta i_s = \Delta i_L \frac{1 - 2D}{1 - D} \quad , \text{ for } D \leq 0.5 \quad (2.7)$$

$$\Delta i_s = \Delta i_L \frac{2D - 1}{D}, \text{ for } D > 0.5 \quad (2.8)$$

since operating the two channels 180° phase shifted from each other leads to partial/full ripple cancellation of the ripple. This is one of the benefits of using two channels instead of one and the duty cycle dependence between the input and inductor ripple is depicted in figure 2.8.



**Figure 2.8:** Two channel step-up converter ripple reduction as a function of the duty cycle.

One way to design the inductors in the PFC is to state a maximum percentage input ripple of the nominal peak input current that is allowed during low line operation, this can be expressed in the following way

$$\Delta i_s = \frac{\sqrt{2}P_o}{\eta V_{s,RMSmin}} \Delta i_{\%,Design} \quad (2.9)$$

in which  $\eta$  is the efficiency of the converter and  $P_o$  is the output power.

### 2.3.2 Core choice

The correct choice of core is essential for the inductor's performance. There are many unknown parameters regarding the cores, and the design work needs to take on an iterative approach. As there are many different types of cores available on the

market, the selection range have to be narrowed down in order to be able to find a core to begin to design around.

The first step is to determine the amount of current the inductor needs to be able to handle. The RMS value of the current going through the circuit at full load can be determined by

$$I_{rms} = \frac{P_o}{\eta V_{s,RMSmin}} \quad (2.10)$$

Since there are two channels each inductor only carries half the total RMS current, i.e.  $I_{L,rms} = I_{rms}/2$ . The peak of the inductors' RMS current is given by

$$\hat{I}_{L,50Hz} = \sqrt{2}I_{L,rms} \quad (2.11)$$

where  $\hat{I}_{L,50Hz}$  is the peak of the pure sinusoidal current that ideally would be drawn from the grid. The current peak in the inductor ( $\hat{I}_L$ ) in absolute values is given by

$$\hat{I}_L = \hat{I}_{L,50Hz} + \frac{\Delta I_{L,max}}{2} \quad (2.12)$$

where  $\Delta I_{L,max}$  is the maximum ripple current in the inductor. This is the minimum current that the inductor needs to be dimensioned for.

The amount of energy that should be stored in the inductor is a fundamental property affecting the choice of core and which indicates how physically large the inductor will be. Core manufacturers may provide guides for the core size needed for different materials. The stored energy ( $E$ ) in the inductor is given as

$$E = \frac{L\hat{I}_L^2}{2} \quad (2.13)$$

although core manufactures tend to omit the division and compensate for it in their charts.

Each core material have different properties which impacts the characteristics of the inductor. As this PFC circuit utilize a high switching frequency, only good performing metal powder and ferrite materials can be used. Iron cores would have to large eddy current losses at the particular operating frequency. Ferrite cores have the advantage of low core losses which is crucial at high frequency operation, but they have low saturation limit [1] which limits the current handling capability. There is also a material called VitroPerm which offers very high relative permeability which allows for low copper losses due to few turns, but it has too have low saturation limit. Metal powder cores on the other hand, have higher core losses but can generally handle a higher current per volume unit than the ferrite cores.

As the core losses solely depends on the frequency and the current ripple magnitude [4] it may be a good choice to pick a core material with a positive temperature coefficient, which means that the core permeability increases with temperature within the

core's operation range. If the inductor temperature rises, the inductance will also increase which in turn decreases the current ripple magnitude and thus decreases also the losses and temperature. Not all core materials have this property.

The shape of the core affect the behaviour of the core such as thermal properties and shielding. Good shielding is important as it limits electromagnetic interference, EMI. By picking a core shape that emits low EMI, one can mitigate the need of other shielding components such as a metal encapsulation. Cores with good shielding properties are for example toroids and pot cores [5]. Toroids have better heat dissipation performance than pot cores, but are on the other hand more expensive to wind in series production [5].

The number of turns of wire,  $N$ , required to reach the desired inductance is given by

$$N = \sqrt{\frac{L}{A_L}} \quad (2.14)$$

where  $A_L$  is a magnetic property with unit  $\frac{nH}{I^2}$  defined by the core manufacturer for each core. This will give the correct inductance at no load state.

The permeability of the core material will decrease as the current through the inductor increases, why the inductance also must be calculated at full load. This is done by

$$H_{max} = \frac{N\hat{I}_L}{l_e} \quad (2.15)$$

where  $H_{max}$  is the magnetic field strength with unit ampereturns per centimeter,  $At/cm$ , and  $l_e$  is the core's magnetic path length with unit  $cm$ . By investigating the core datasheet information about how much the permeability will roll off in percentage for the current bias level can be found. The roll off multiplied with the no load inductance will give the full load inductance [4]. If the deviation is too large, the number of turns must be increased. By dividing the initial number of turns by the percentage roll off, a new suitable amount of turns is found. The process is then iterated from (2.15) until the full load inductance is high enough [4]. The permeability also depends on the frequency of the current going through the inductor, which is why a similar procedure needs to be conducted if the core material has a significant roll off at the operating frequency.

### 2.3.3 Core loss

The losses in the core depends on the switching frequency and the magnetic flux swing within the core [4], thus the current ripple. The flux swing ( $B_{pk}$ ) is given by

$$B_{pk} = \frac{\Delta B}{2} \quad (2.16)$$

where  $\Delta B$  is the difference between the highest and lowest core flux. The core flux depends non-linearly on the magnetic field strength,  $B = f(H)$ . The flux difference can be expressed as

$$\Delta B = f(H_{max}) - f(H_{min}) \quad (2.17)$$

where  $H_{max}$  is the maximum field strength as calculated in (2.15) and  $H_{min}$  is the local minimum field strength.  $H_{min}$  is given by a slightly modified version of (2.15) as

$$H_{min} = \frac{N\check{I}_L}{l_e} \quad (2.18)$$

where  $\check{I}_L$  is the local minimum of the peak current, given by

$$\check{I}_L = \hat{I}_{L,50Hz} - \frac{\Delta I_{L,max}}{2} \quad (2.19)$$

The function  $f$  is sometimes given by a magnetization curve in the core datasheet, but can also be approximated by

$$f(H) = H\mu_0\mu_i\%_{roll-off} \quad (2.20)$$

where  $\mu_0$  is the absolute permeability,  $\mu_i$  is the intrinsic relative permeability of the core and  $\%_{roll-off}$  is the permeability roll off of the core at the DC bias and frequency level. At no load,  $\%_{roll-off}$  is 100.

$B_{pk}$  gives the core loss density ( $P_L$ ) which can be extracted from the core datasheet.  $P_L$  have unit  $mW/cm^3$ . The core loss,  $P_{core}$ , with unit  $mW$ , can be calculated by

$$P_{core} = P_L A_e l_e \quad (2.21)$$

where  $A_e$  is the equivalent magnetic area of the core. This calculation is however based on the maximum current ripple and is therefore the worst case scenario and most of the time the core loss will be lower.

### 2.3.4 Wire dimensioning

The inductor needs of course a wire that is wound around the core. The wire dimension depends on how large the power loss in the wire is allowed to be along with the available space given by the core shape and dimensions. By using a thick wire the copper losses ( $P_{cu}$ ) will be low but on the other hand the core might not be able to accommodate the necessary number of turns. As a starting point the copper loss may be set to a reasonable value, like  $500 \text{ mW}$ . To be able to calculate a suitable cross section area of the wire, the length of the wire ( $l_w$ ) must first be known. Assuming a toroid core, the winding circumference ( $O_w$ ) of the core is given by

$$O_w = \varnothing_o - \varnothing_i + 2H_t \quad (2.22)$$

where  $\varnothing_o$  is the outer diameter of the core,  $\varnothing_i$  is the inner core diameter and  $H_t$  is the core height. If the amount of turns require the wire to be wound in several layers around the core, the turn mean length increases.

The required cross section area of the wire ( $A_w$ ) can be calculated by

$$A_w = \frac{\rho_{cu} l_w I_{L,rms}^2}{P_{cu}} \quad (2.23)$$

where  $\rho_{cu}$  is the resistivity for copper, which is  $\rho_{cu} = 1,68 * 10^{-8} \text{ } \Omega m$  at room temperature. The resistance in the wire does however increase with temperature. The resistance increases with about 30 % [6] if the temperature is increased to  $100 \text{ }^\circ C$ , so the cross section area should be increased with the same percentage to make sure the losses are kept under control when the wire temperature increases.

The skin effect at switching frequencies as high as 1 MHz is significant. This means that only the outer part of the wire will conduct current, why the effective resistance off the wire increases significantly. To mitigate this problem a litz wire should be used. A litz wire is a wire consisting of many small strands, each isolated from the others. The skin depth ( $\delta$ ) is big compared to the diameter of each strand, resulting in a more well distributed current and a DC like resistance. The effective cross section area of the litz wire needs to be equal to the calculated needed cross section area which only is valid for DC.

The skin depth can be calculated by using

$$\delta = \frac{1}{\sqrt{f \mu_0 \mu_{r,cu} \pi \rho_{cu}^{-1}}} \quad (2.24)$$

where  $f$  is the frequency and the relative copper permeability ( $\mu_{r,cu}$ ) is 1 [6].  $\delta$  is calculated to  $65,2 \text{ } \mu m$  given  $f = 1 \text{ MHz}$ . The skin effect can be neglected if  $\varnothing_w \leq 2\delta$ , where  $\varnothing_w$  is the diameter of the wire [1]. The diameter of each strand in the litz wire should therefore not exceed  $2\delta$ .

### 2.3.5 Heating considerations

The temperature rise in the inductor is important. Not only does it affect the inductance, the core and the litz wire have also specifications for maximum allowed operating temperature. The exact steady state temperature can not easily be calculated as it is dependent on unknown environment variables such as air flow rate, air temperature, humidity, air pressure and so on. The temperature rise in completely still air can however be estimated and used for designing purposes. The temperature rise of the inductor ( $\Delta T_L$ ) can be calculated as

$$\Delta T_L = \left( \frac{P_{cu} + P_{core}}{S_{component}} \right)^{0.833} \quad (2.25)$$

where  $S_{component}$  is the total surface area of the whole inductor given in square centimeter, and the power losses are given in milliwatt [4]. The total surface area of the component depends on the number of turns wound around the core as many turns give a physically larger component. In this case the core-fill is very low so the total surface area can be approximated by the surface area of the core ( $S_c$ ) itself. The core area is calculated by

$$S_c = \frac{\pi}{2}(\varnothing_o^2 - \varnothing_i^2) + \pi H_t(\varnothing_o + \varnothing_i) \quad (2.26)$$

## 2.4 MOSFET design considerations

### 2.4.1 Voltage rating

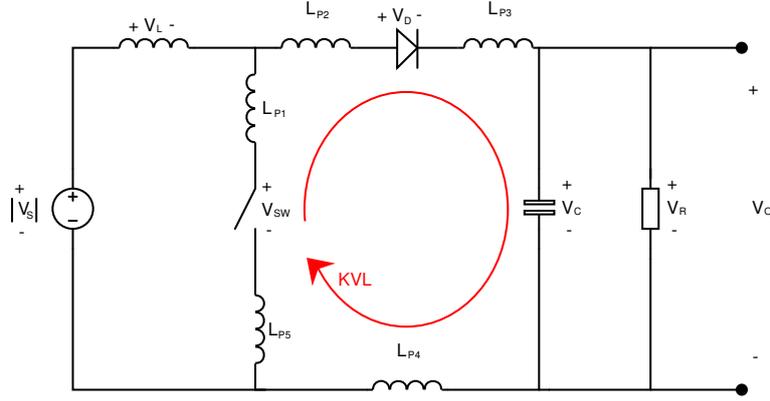
Because of parasitic inductances in the so called critical loop of the boost converter, shown looped in red in figure 2.9 where the parasitic inductances are named  $L_{P1}$ - $L_{P5}$ , an overvoltage will occur at turn-off of the switch [1, 7].

During turn-off when the diode starts carrying the current KVL can be applied in the critical loop as depicted in the figure which yields the following expression assuming that all the parasitic inductances can be lumped together as  $L_p$  and that the forward diode voltage drop is zero.

$$V_{SW} = V_o - L_p \frac{di}{dt} \quad (2.27)$$

### 2.4.2 Current rating

Assuming that the PFC will meet the specifications of requirement the power factor will be close to 1 (0.98). The peak of the current through the switches ( $I_{SW,max}$ )



**Figure 2.9:** KVL applied in the critical loop of the boost converter which contains parasitic inductances.

are therefore half the nominal peak current during low line operation plus half the current ripple of the inductor, which can be expressed as

$$I_{SW,max} = \sqrt{2} \frac{P_o}{2\eta V_{s,RMSmin}} + \frac{\Delta i_L}{2} \quad (2.28)$$

### 2.4.3 Loss calculation switch

The total losses off the switch is the sum of the conduction losses  $P_{MOSFET,conduction}$ , the switching losses  $P_{MOSFET,switching}$  and the losses dissipated in the drain-source channel because of the intrinsic output capacitance  $P_{MOSFET,Coss}$  of the MOSFET. The conduction losses can be calculated using

$$P_{MOSFET,conduction} = I_{DS,RMS}^2 R_{DS,on} \quad (2.29)$$

where  $R_{DS,on}$  is the on state resistance of the switch.

The switching losses in turn can be written as

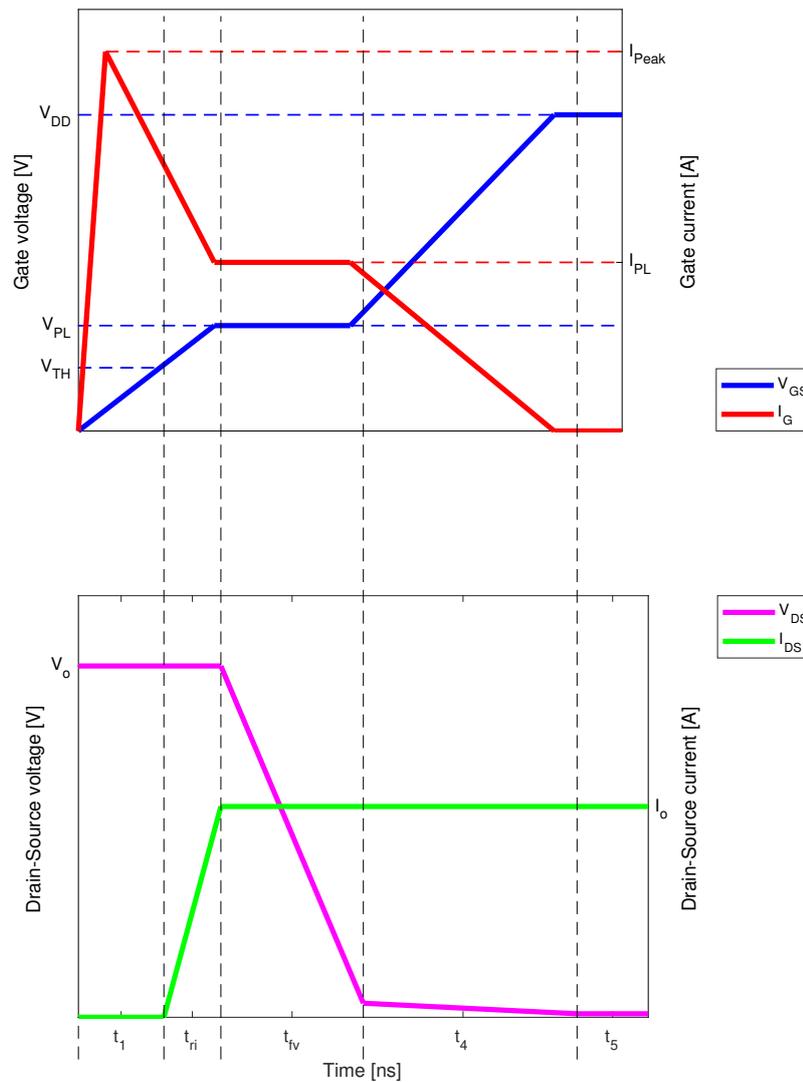
$$P_{MOSFET,switching} = (E_{on} + E_{off}) f_s \quad (2.30)$$

where  $E_{on}$  and  $E_{off}$  are the turn-on and turn-off energies lost during one switching cycle. These energies can be approximated using [8]

$$E_{on} = \frac{1}{2} V_{DS} I_{DS} t_{c(on)} \quad (2.31)$$

$$E_{off} = \frac{1}{2} V_{DS} I_{DS} t_{c(off)} \quad (2.32)$$

where  $t_{c(on)}$  and  $t_{c(off)}$  are the cross over times when the current and voltage across the switch is non zero simultaneously. These times can be determined by investigating the MOSFET switching waveforms. Figure 2.10 depicts a simple piecewise linear model of the turn-on patterns of a MOSFET with an inductive load [9].



**Figure 2.10:** Piece wise linear model of a MOSFET turn-on waveforms.

The cross over times can be calculated using [1]

$$t_{c(on)} = t_{ri} + t_{fv} \quad (2.33)$$

$$t_{c(off)} = t_{rv} + t_{fi} \quad (2.34)$$

where  $t_{ri}$  and  $t_{fv}$  are indicated in figure and  $t_{rv}$  and  $t_{fi}$  can be found by investigating the same waveforms reversed.

The voltage  $V_{DD}$  indicated in the figure is the gate driver operating voltage. Voltage  $V_{PL}$  is the so called plateau voltage, or Miller voltage, and  $I_{PL}$  is the current during the Miller plateau.

Given the gate charge characteristic, which can be found in the data sheet of the MOSFET, it is possible to calculate the rise and fall times using [9]

$$t_{ri} = \frac{Q_{GS2}}{I_{G,tri}} \quad (2.35)$$

$$t_{fv} = \frac{Q_{GD}}{I_{G,tfv}} \quad (2.36)$$

$$t_{rv} = \frac{Q_{GD}}{I_{G,trv}} \quad (2.37)$$

$$t_{fi} = \frac{Q_{GS2}}{I_{G,tfi}} \quad (2.38)$$

where  $I_G$  for the different times is the current into the gate during the different times of the transitions. The charges  $Q_{GS2}$  and  $Q_{GD}$  can be extracted from the gate charge characteristics which is shown in figure 2.11 [9].

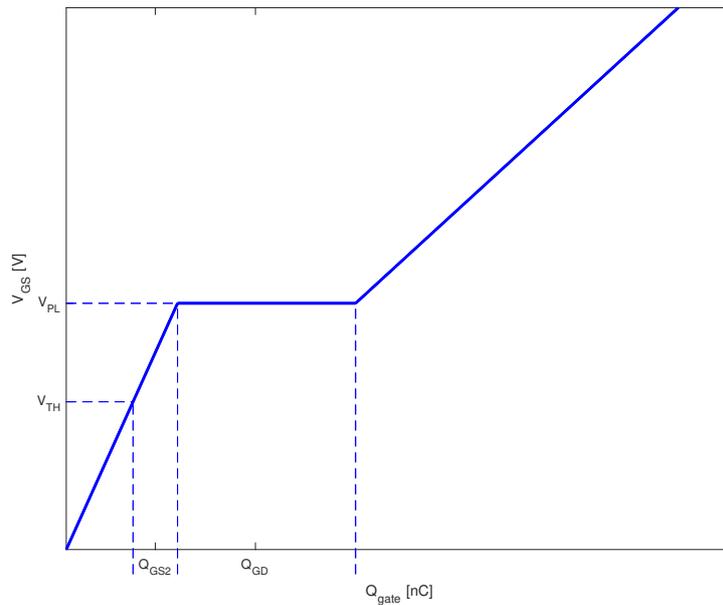
The output capacitance  $C_{oss}$  will be discharged through the channel once every switching cycle during turn-on [10]. The energy stored in  $C_{oss}$  can be read from the graphs in the data sheets and is named  $E_{oss}$  which varies with  $V_{DS}$ . The resulting loss can be written as [8]

$$P_{MOSFET,Coss} = E_{oss}f_s \quad (2.39)$$

### 2.4.4 Loss calculation driver

The gate is charged and discharged every switching cycle. The amount of charges injected into the gate can be read from the gate charge characteristics. Current is defined as Coulomb per second, which means that the average driver gate current ( $I_{driver}$ ) can be calculated using [9]

$$I_{driver} = Q_{G,max}f_s \quad (2.40)$$



**Figure 2.11:** Example of a MOSFET gate charge characteristic with indicated voltages and corresponding charge level.

where  $Q_{G,max}$  is the gate charge at the driver operating voltage. The driver current times the driver voltage gives the power loss of the driver, hence

$$P_{MOSFET,driver} = V_{DD}Q_{G,max}f_s \quad (2.41)$$

### 2.4.5 Parasitic source inductance

Because of the non zero length of the conduction paths involved there will be a resulting inductance between the source of the switch to the ground. When the switch is turned off, the source inductance will induce a negative voltage since  $V_L = L \frac{di}{dt}$ . Depending on the fall time of the current, the negative voltage at the source might trick the MOSFET to start to conduct since the gate voltage is kept low and induced negative voltage at the source effectively gives a positive  $V_{GS}$ , which might be above the threshold voltage.

Take a TO-220 package for example where the inductance of the pins are between 10-20 nH [10]. Since the switching frequency is going to be high, the  $di/dt$  can in this case exceed 0.5 A/ns resulting in an induced source voltage of -5 V given the inductance of only the pin. This is already unacceptable since the resulting  $V_{GS}$  would be 5 V which is above the threshold voltage of many MOSFETs.

## 2.5 Boost diode design considerations

### 2.5.1 Current rating of the boost diode

The peak current through the diode will be the same as for the MOSFET, because of the layout of the step-up converter, and the peak current rating can be calculated using (2.28).

### 2.5.2 Losses attributed to the boost diode

The boost diode contributes to two kinds of losses. Conduction losses  $P_{Dconduction}$  which are dissipated in the diode and the switching losses  $P_{Dswitching}$  associated with capacitive charge ( $Q_C$ ) or reverse recovery charge ( $Q_{rr}$ ) [8].

The conduction losses can be expressed as [8]

$$P_{D,conduction} = I_{D,avg} V_f \quad (2.42)$$

where  $V_f$  is the forward voltage drop and  $I_{D,avg}$  is the average current through the diode which, in this case with two channels, can be calculated as  $I_{D,avg} = P_o/2V_o$  under the assumption that the output capacitor is large enough to keep the output voltage constant.

The switching losses occur because of the trapped charge in the diode which in this case can be expressed as [8].

$$P_{D,switching} = \frac{1}{2} V_o Q_c f_s \quad (2.43)$$

During hard commutation, the switching losses of the diode will be dissipated in the diode and its corresponding switch. The distribution of these losses depend on the times  $t_a$  and  $t_b$ , represented in figure 2.12, which makes up the reverse recovery time  $t_{rr}$  [11].

The switching/commutation loss dissipated in the diode is directly proportional to  $t_b$ . This means that most of the switching/commutation losses will be dissipated in the switch if the diode is snappy. The snappiness is defined as  $\frac{t_a}{t_b}$ .

Additionally, extra losses will occur in the switch because of the diode reverse recovery current. Since a current will flow in the "wrong" direction during the reverse recovery time which, because of the layout, will be conducted through the switch when it opens causing losses.

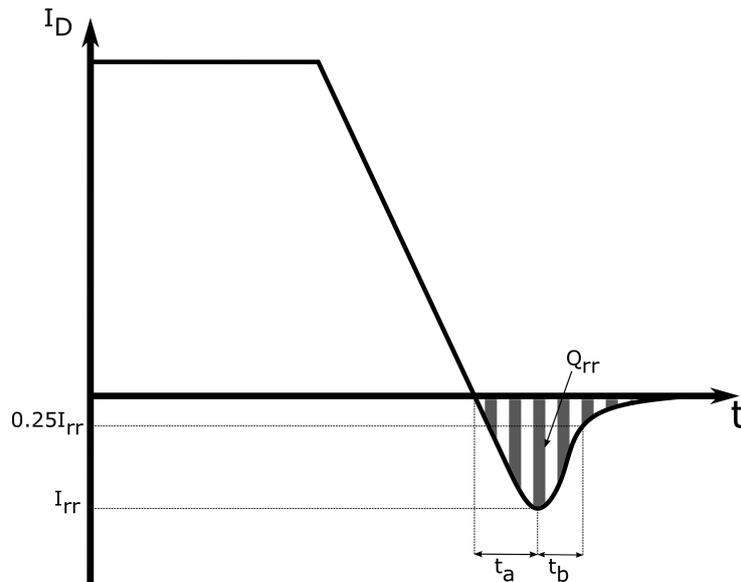


Figure 2.12: Reverse recovery current of a diode.

## 2.6 Conducted EMI filter design

A conducted EMI filter is depicted in figure 2.13 [12].

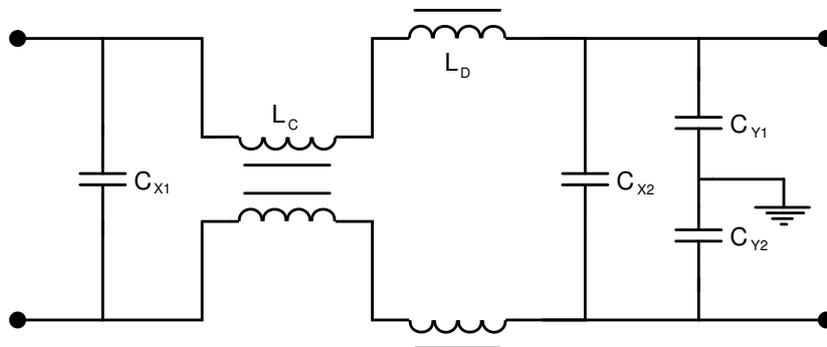


Figure 2.13: An EMI filter.

The filter will appear different for common mode (CM) noise than differential mode (DM) noise and the equivalent circuits for the different noises forms second order LC-filters with corner frequencies ( $f_{c,CM}$ ) and ( $f_{c,DM}$ ) calculated as [12]

$$f_{c,CM} = \frac{1}{2\pi\sqrt{(L_{CM} + \frac{1}{2}L_{DM})2C_{CM}}} \quad (2.44)$$

$$f_{c,DM} = \frac{1}{2\pi\sqrt{(2L_{DM} + L_{leakage})C_{DM}}} \quad (2.45)$$

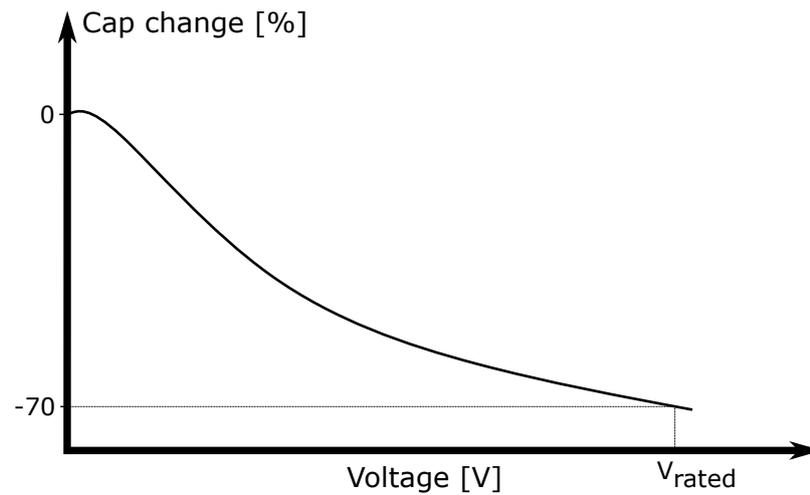
given that  $C_{DM}=C_{X1}=C_{X2}$ ,  $C_{CM}=C_{Y1}=C_{Y2}$ ,  $C_{DM} \gg C_{DM}$  and  $L_{leakage}$  is the leakage inductance of the common mode choke. The leakage inductance is practically between 0.5 % and 2 % and can therefore be utilized as DM choke [12].

Capacitor  $C_{X1}$  and  $C_{X2}$  are often referred to as X-capacitors, while  $C_{Y1}$  and  $C_{Y2}$  are called Y-capacitors. Special considerations regarding safety should be considered while choosing these capacitors. The Y-capacitors are grounded and if they fail as a short circuit the ground could assume dangerous voltages. The X-capacitors are connected across the AC line and presents a fire hazard if they fail [13]. Therefore there are capacitors especially designed for these applications, and there are different sub classes of these capacitors, namely X1, X2, X3, Y1, Y2, Y3 and Y4 where a lower index corresponds to a higher level of safety [14].

## 2.7 Ceramic capacitors

There are several different kinds of capacitors (electrolytic, tantalum, ceramic and polymeric capacitors) to choose from when designing. The properties of the capacitors used need to be understood in order to make correct design choices. Electrolytic capacitors are appropriate when large capacitance are needed, but because of their high series resistance (ESR) and series inductance (ESL) they may not be suitable for applications like de-coupling, bypass or filter capacitors where low ESR and ESL may be required. Tantalum capacitors have medium-high ESR and low ESL and has a high capacitance density but they can fail explosively and are therefore not used for this design. Polymeric capacitors may have the highest capacitance density and has low ESR and ESL but are expensive. The ceramic capacitors has the lowest cost and ESR, have low ESL and there are many manufacturers to choose from. Because of this, ceramic capacitors will be extensively used for this project. In order to make the correct design choices it is important to recognize that the capacitance is influenced by the voltage [15].

The capacitance of the ceramic capacitor will change when a DC-voltage is applied to it and the capacitance at the operating point may therefore be much lower than the nominal value. The characteristic change in capacitance as a result of applied voltage is called DC bias characteristic and may be provided in the data sheets. Figure 2.14 illustrates an example of DC bias characteristics for a ceramic capacitor.



**Figure 2.14:** Example of a DC bias characteristic for a ceramic capacitor.

The change of capacitance occurs because the dielectric relative permittivity decreases as the electric field strength increases [16].

Large ceramic package sizes may also cause audible noise because of their piezoelectric nature. Even cracking can occur as the PCB flexes because of the capacitor. One way to mitigate this is to mount metallic terminals to the capacitor so that the capacitor is lifted up from the PCB [15, 16].



# 3

## Method

### 3.1 Overview

Texas Instruments have developed a demo project for a digital active PFC around one of their Digital Signal Processors, DSP. The demo project is called ILPFC [17] and is freely available together with their developing suite. The processor family used is called Piccolo and is well suited for the fast operation that is required for a high frequency PFC. The built hardware will therefore be based on this demo project and utilize the very same processor.

The processor is the heart of the PFC's control system. It has the purpose of measuring voltages and currents in the circuit, generate the PWM signals and control the duty cycle so that the input current follow the input voltage waveform while keeping the output voltage at a fairly constant level. In order to get a good power factor of the PFC it is more important that the current has the correct shape than that the output voltage is stable. The current control loop therefore needs to be faster than the output voltage control loop. In the default software developed for the ILPFC project this is solved by sampling and running the current control loop at 100 kHz while the output voltage control loop runs at 50 kHz. The default switching frequency of the demo project is 200 kHz and some tweaking is therefore needed before the processor is able to control the PFC at a frequency as high as 1 MHz. The PWM signals that are generated by the processor drives two MOSFET transistors through a gate driver. The DSP needs a USB-interface for communication with a computer in order to upload firmware and for debugging.

Other sub circuits and components that needs to be developed/chosen includes:

- Power supply for DSP and peripherals
- The switching stages including boost inductors, transistors, diodes and filtering capacitors
- EMI filters
- Current and voltage measuring circuits
- DC bulk and bleeder circuit
- Temperature monitoring circuit
- Encapsulation and cooling

Furthermore a simple software needs to be developed in order to enable test and verification of the hardware.

As can be seen from the bullet list, the circuit will consist of several components and at the end of the circuits life time it will probably be recycled or end up in a land fill. The components and all the parts making up the device will fall under the RoHS directive. RoHS stands for: directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment certified, which limits the use of certain hazardous materials such as lead and mercury. From an ecological point of view, this is done in order to promote sustainable development as the heavy metals are dangerous to the environment and can harm living creatures. Heavy metals are also dangerous for humans as it may end up in our food in in our proximity. Arguments can therefore be made that it is unsustainable from a ethical and social point of view to not use RoHS components, as it could be deemed morally wrong to, by extension, poison our fellow man.

As a designer of new products or scientist working on new research you personally are in some way, by extension, morally tied to the outcome. And the person performing the work should think through the ethical consequences of results yielded by the work and make sure that he or she is morally comfortable with this. As in this case, where a device operating with lethal voltages is built without warning signs or operation manuals, the immediate question regarding possible human harm must be examined. Moral comfort is found in that the result of this thesis is a prototype which only will be handled by well-grounded engineers.

## 3.2 Input protection and EMI filters

The requirement of specifications does not specify allowed conducted EMI noise level, and the base line of the conducted EMI is difficult to predict in the initial design phase. Therefore the filter is designed by comparing a similar filter implemented in another two phase interleaved PFC operating at a lower switching frequency. The chosen values for the X-capacitors are  $C_{DM}=C_{X1}=C_{X2}=0.33\ \mu F$ , while the Y-capacitors are  $C_{CM}=C_{Y1}=C_{Y2}=4.7\ nF$ . The Y-capacitors contribute to a leakage current of  $I_{leak}=\omega C_{CM}V=340\ \mu A$  [18]. The common mode choke 7448040707 from Würth Electronics Inc. is chosen, which has a inductance of  $L_{CM}=7\ mH$  and in accordance with the reasoning of section [12] the differential mode inductance is approximated to  $L_{DM}=7\ mH*0.01=70\ \mu F$ . The corner frequencies of the filter can be calculated using (2.44) and (2.45) to

$$f_{c,CM} = \frac{1}{2\pi\sqrt{2L_{CM}C_{CM}}} = \frac{1}{2\pi\sqrt{2*7\ mH*4.7\ nF}} \approx 20\ kHz \quad (3.1)$$

$$f_{c,DM} = \frac{1}{2\pi\sqrt{L_{DM}C_{DM}}} = \frac{1}{2\pi\sqrt{70\ \mu H*0.33\ \mu F}} \approx 33\ kHz \quad (3.2)$$

The DC-output will also have a similar filter.

Because of the output bulk capacitance there will be a large inrush when the PFC is connected to the grid. The amplitude of the inrush current would probably blow the fuse and damage the circuitry of the PFC. In order to limit this initial current, a NTC thermistor is placed in series with the input. The chosen thermistor has part number SL2250004 from Ametherm and which, according to the data sheets, is able handle bulk capacitance up to 1300  $\mu F$  at 240 VAC. This component has 50  $\Omega$  at room temperature which will limit the inrush current to  $\frac{230 V * \sqrt{2}}{50 \Omega} = 6.5 A$ . The thermistor will initially consume large amounts of power and will therefore heat up, since it is a NTC the resistance will decrease and ideally go down to zero once the bulk capacitors are charged. This is however not the case, the resistance of this thermistor will drop to 0.44  $\Omega$  causing unacceptable losses during normal operation. A relay is therefore connected in parallel which will short the thermistor once the bulk capacitors are charged. The coil of the relay consumes 20 mA and will be driven by the 12 V rail via a NPN bipolar transistor controlled by the DSP.

### 3.3 Diode bridge rectifier

The full bridge diode rectifier will carry the full input current of the PFC. Assuming that the current is fully sinusoidal the input RMS current will be 5.03 A during low line operation and an efficiency of 96 %. The average current is therefore  $I_{F_{avg}} = 0.9 * 5.03 A = 4.53 A$ . The full bridge rectifier MP1010G-G is therefore used, it can handle a current of 10 A and a reverse voltage of 1000 V. The package of the rectifier makes the heat sink choice easy because of its shape. The voltage drop across one of the diodes at 4.53 A can be read from the data sheet to  $V_F = 0.9 V$ . The diodes in the bridge rectifier conducts in pair so the loss in the diode rectifier ( $P_{FBDR}$ ) is approximated as

$$P_{FBDR} = 2V_F I_{F_{avg}} = 2 * 0.9 V * 4.53 A \approx 8.2 W \quad (3.3)$$

### 3.4 Boost inductors

#### 3.4.1 Inductor size calculations

It is possible to dimension the inductance of the boost inductors to 35  $\mu H$  for the PFC using (2.5), (2.6), (2.7) and (2.9) given the following design criteria:  $V_{s,RMSmin} = 0.9 * 230 V$ ,  $V_o = 400 V$ ,  $f_s = 1 MHz$ ,  $P_o = 1 kW$ ,  $\eta = 0.96$  and  $\Delta i_{\%,Design} = 20 \% \implies 1.42 A$ . This results in an inductor ripple of 40 %.

### 3.4.2 Evaluation of possible cores

To be able to design a, for this application, proper inductor it is necessary to pick a suitable inductor core.

The manufacturer Magnetics have several core materials optimized for power inductors as well as a good documentation of their cores and the design steps. Using (2.10),  $I_{rms}$  equals 5.03 A. The RMS current for each inductor is thus  $I_{L,rms} = 2.52$  A.

Applying (2.11) and (2.12) concluding that  $I_{L,max} = 4.27$  A, which is the minimum current the inductor needs to be able to handle without saturating.

A first try is the Magnetics AmoFlux core material. AmoFlux is a metal powder material which is developed for PFC applications and is therefore able to handle both high fluxes and frequencies. The material is currently only available in toroid shaped cores. As Magnetics does not provide any recommendation chart for size versus energy capability for AmoFlux cores a good sizing guess is appropriate. Core 0088894A7 is picked as it is the smallest available. The properties of the chosen core are shown in table 3.1.

**Table 3.1:** Properties of AmoFlux 0088894A7

Physical properties [mm]			
Outer diameter, $\varnothing_o$	Inner diameter, $\varnothing_i$	Thickness, $H_t$	
27.69	14.1	12.0	
Magnetic properties			
Permeability, $\mu$	$A_L[nH/t^2]$	Area, $A_e$ [mm <sup>2</sup> ]	Path length, $l_e$ [mm]
60	75 ±8 %	65.4	63.5

Using (2.14)  $N$  is computed for the worst case  $A_L$ , which is the nominal value minus the margin of error of eight percent, to  $22.5 \approx 23$  turns.

By (2.15) is in this case  $H_{max} = 15.5$  At/cm. The datasheet of the core [19] indicates that the permeability will remain unaffected for this drive level. The permeability roll off due to the switching frequency can also be neglected.

### 3.4.3 Core loss

Using equations (2.16), (2.17), (2.18) and (2.19) with the datasheet [19],  $B_{pk}$  is calculated to 0.01 T.

The core loss density for the calculated flux swing and switching frequency is extracted from an extrapolated figure in the core datasheet [19] to be  $PL \approx 90$  mW/cm<sup>3</sup>,

which by (2.21) gives  $P_{core} = 374 \text{ mW}$ . These loss calculations are deemed to be to good to be true given the uncertainty of the data extrapolation. The core is therefore dismissed as a possible candidate.

### 3.4.4 Wire dimensioning

As the selected core is a toroid, (2.22) is used to calculate the winding circumference along with the data in table 3.1. This sets the required wire length to  $37.6 \text{ mm}$  per turn. Assuming that the amount of turns only requires a single layer, the total wire length,  $l_w$  will be approximately  $86.5 \text{ cm}$ . For convenience this is rounded to  $1 \text{ m}$ . (2.23) sets the cross section area of the wire to  $0.23 \text{ mm}^2$ . The actual wire should however be slightly thicker to compensate for increased resistance at high temperature.

The maximum thickness of the strands in a litz wire is calculated by (2.24) to about  $0.130 \text{ mm}$ . One litz wire that should be sufficient for this purpose is the Block CLI 200/60 which have an effective cross section area of  $0.471 \text{ mm}^2$ . The diameter for such a wire is about  $\varnothing_w = 0.78 \text{ mm}$ . The number of turns available for a single wire layer on the core can be approximated by

$$N = \frac{\pi \varnothing_i}{\varnothing_w} \quad (3.4)$$

With this wire, the core will be able to fit about 57 turns which is a lot more than the needed number of 23 turns. The calculated length of copper wire of 1 meter is therefore correct. The actual power loss in the wire can, by using (2.23), be calculated to  $P_{cu} = 236 \text{ mW}$  at  $100 \text{ }^\circ\text{C}$ .

### 3.4.5 Heating of the inductor

$S_{component}$  is by (2.26) calculated to  $2.5 \text{ cm}^2$ . The temperature rise is then calculated to  $\Delta T = 97.4 \text{ }^\circ\text{C}$  using (2.25). Adding the room temperature of about  $25 \text{ }^\circ\text{C}$  gives an inductor temperature of  $122 \text{ }^\circ\text{C}$ . This value is within both the wire's and the core's operating temperature. It is however very likely that the actual temperature will be lower than this for two reasons:

1. The calculated core loss is the maximum loss that can occur, the mean will be lower.
2. The air will not be completely still. If cooling is an issue, a fan can be added.

### 3.4.6 Considerations regarding core choice

The chosen core is shown to be a viable option for the application as long as the estimated core loss is reasonably correct. However the core might be unnecessary large as only a few turns are required to reach the defined inductance. It is therefore reasonable to iterate and redo the calculation process with a smaller core size and/or another core material.

### 3.4.7 Other cores

Due to the uncertainty of losses of the core picked in the calculation example, further investigation are made. The company Micrometals released, in late 2016, a new series of cores, High Frequency Sendust, specifically developed for applications utilizing high power and have documentation for frequencies up to about 5 MHz. The iterative method already presented is used to compare a few cores of the series. Micrometals does not specify the connection between the magnetic field strength and magnetic flux in their datasheets[20], thus the approximation from (2.20) is used. A set of working inductors is shown in table 3.2. To get a feeling of the physical inductor size, the material volumes are presented in the table. This parameter is calculated by adding the volume of the core and the volume of the copper wire together. The litz copper wire used is the Block 200/60, the very same as is used above, and has a physical cross section area of  $0.519 \text{ mm}^2$ .

**Table 3.2:** Inductor comparison based on Micrometals Sendust High Frequency core series, sorted by volume.

Core part number	Permeability	Turns	Material volume [ $\text{cm}^3$ ]	Losses [W]
SH-050026-2	26	81	1.72	2.17
SH-068060-2	60	44	1.99	2.25
SH-068026-2	26	51	2.09	1.63
SH-065026-2	26	60	2.10	1.90
SH-080026-2	26	58	2.55	1.96
SH-090060-2	60	37	3.01	2.17
SH-090026-2	26	48	3.19	1.59

The smallest one, SH-050026-2, have a bit too high losses to be a reasonable option. The large amount of turns needed can also make the inductor difficult to wind. The second smallest, SH-068060-2, have the highest losses of them all why it also is an unsuitable option. The SH-068026-2 is however the most viable core choice as it is small but have also low losses.

The core samples ordered from Micrometals are thus SH-068026-2 as well as the

SH-080026-2 and the SH-090060-2. The reason for the choice of core SH-080026-2 is that it is one step larger than the SH-068026-2 and can thus handle more turns or a thicker wire if it is deemed necessary. The SH-090060-2 is an option that only will need one layer of wire wound around the core. This can be useful to keep a minimum isolation distance between the core input and output. Care has to be taken in order not to place wires, with possibly 400 V, next to each other since this could lead to a breakdown of the insulation. Using a single layer mitigates the need of conductors with large potential difference to be near each other.

## 3.5 Boost MOSFETs and driver

### 3.5.1 Voltage and current rating

The overvoltage peak is dependent on the parasitic inductance and fall time of the current during switch off as described in section 2.4. Low fall time is preferred because it reduces the switching losses, hence the minimization of the parasitic inductance is therefore important. The needed breakdown voltage of the switch is difficult to precisely calculate at this point because of the uncertainties of the parasitic inductance introduced by the layout of the PCB, so 400 V and enough room for overvoltages caused by parasitic inductances are the requirements at this point. Snubbers can be implemented if the overvoltages are too severe. The peak current that the switches should be able to withstand during normal operation is the same as the used inductor peak current which is 4.27 A.

### 3.5.2 Parasitic source inductance mitigation

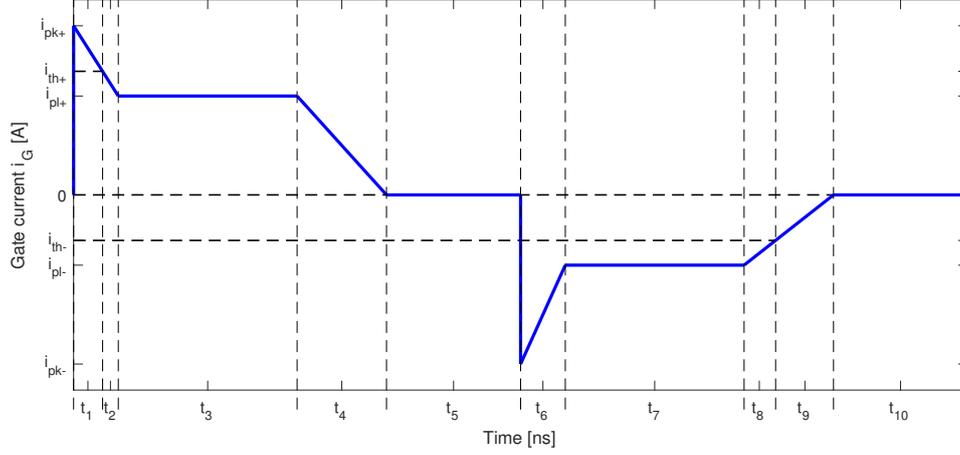
In order to mitigate problems due to parasitic source inductance, as discussed in section 2.4, a MOSFET with a so called Kelvin-source will be used. This is a fourth pin on the MOSFET which is connected directly to the source substrate of the transistor inside the casing. This separates the driving source from the power source early, thus partially avoiding the inductance of the source pin which carries fast changing high currents.

### 3.5.3 MOSFET losses

The switches finally chosen is called IPT65R195G7 and are from Infineon Technologies. The following data can be found in the data sheet: internal resistance  $R_{Gi} = 1.2 \Omega$ , Miller plateau voltage  $V_{pl} = 5.4 V$  and a threshold voltage of  $V_{th} = 3.5 V$ . Assuming no switching constrains such as maximum driver current or  $dV/dt$ -ratings and with  $V_{DD} = 13 V$  together with a gate resistance of  $R_G = 10 \Omega$

### 3. Method

(which is the test case used in the data sheets) the gate current for a turn-on and turn-off event (initialized after time  $t_5$ ) can be depicted as in figure 3.1.



**Figure 3.1:** Gate current of the G7 MOSFET for a turn-on event and turn-off event starting at time  $t_5$ .

The indicated currents in the figure are:

- $I_{pk+} = 1300 \text{ mA}$
- $I_{th+} = 950 \text{ mA}$
- $I_{pl+} = 760 \text{ mA}$
- $I_{th-} = -350 \text{ mA}$
- $I_{pl-} = -540 \text{ mA}$
- $I_{pk-} = -1300 \text{ mA}$

The current rise time ( $t_{ri}$ ) and voltage fall time ( $t_{fv}$ ) correspond to times indicated as  $t_2$  and  $t_3$  respectively. In the same way,  $t_7$  and  $t_8$  correspond to the voltage rise time  $t_{rv}$  and current fall time  $t_{fi}$ . To calculate the crossover times, the gate charge characteristic has to be investigated. Using the method presented in figure 2.11 the charge levels are extracted as  $Q_{GS2} = 1.9 \text{ nC}$  and  $Q_{GD} = 6.3 \text{ nC}$ . Calculating the average gate current for the rise and fall times and using (2.33) to (2.38) yields the crossover times  $t_{c(on)} = 10.5 \text{ ns}$  and  $t_{c(off)} = 15.9 \text{ ns}$ . The switching losses can then be calculated using (2.30) to (2.32) to

$$P_{G7,switching} = \frac{400 \text{ V} * 2.27 \text{ A}}{2} * 1 \text{ MHz} * (10.5 \text{ ns} + 15.9 \text{ ns}) = 12.0 \text{ W} \quad (3.5)$$

where 2.27 A is used as the average drain-source current, which is equal to the

average inductor current [8], which is half the average input current during low line operation. The loss in the driver can be calculated as

$$P_{G7,driver} = V_{DD}Q_{G,13V}f_s = 13 V * 25 nC * 1 MHz = 0.33 W \quad (3.6)$$

The loss because of  $C_{oss}$  discharging through the channel can be calculated as

$$P_{G7,Coss} = E_{oss}f_s = 2.3 \mu J * 1 MHz = 2.3 W \quad (3.7)$$

The maximum conduction losses can be calculated as

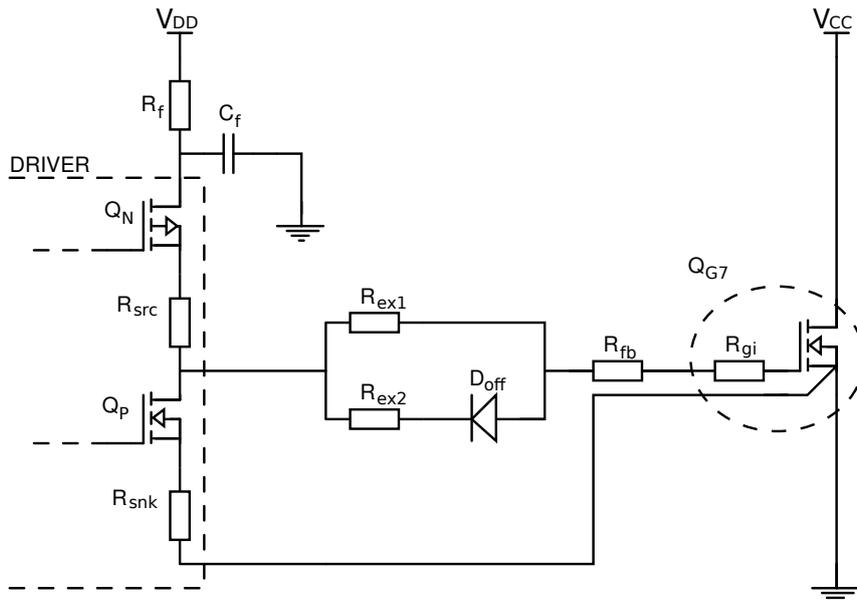
$$P_{G7,conduction} = I_{DS,RMS}^2 R_{DS,on} = (2.52 A)^2 * 0.195 \Omega = 1.24 W \quad (3.8)$$

The total losses for the IPT65R195G7 MOSFET and driver can be calculated to

$$P_{G7,loss} = P_{G7,switching} + P_{G7,driver} + P_{G7,Coss} + P_{G7,conduction} = 15.9 W \quad (3.9)$$

### 3.5.4 Driver circuitry design

A generic MOSFET drive circuit is shown in figure 3.2.



**Figure 3.2:** Generic gate driver circuitry and MOSFET.

As depicted in the figure, the driver circuitry consists of a driver with internal MOSFETs arranged in a totem pole configuration. The resistances  $R_{src}$  and  $R_{snk}$  are parasitic resistances, while  $R_{ex1}$  and  $R_{ex2}$  are actual physical resistances,  $R_{fb}$  is the DC-resistance of the ferrite bead and  $R_{gi}$  is the internal gate resistance of the MOSFET.  $R_f$  and  $C_f$  creates a filter for the input voltage. The diode  $D_{off}$  makes it possible to effectively have different values for the turn-off and turn-on.

The resulting turn-on and turn-off gate resistances can be calculated as:

$$R_{on} = R_{src} + R_{ex1} + R_{fb} + R_{gi} \quad (3.10)$$

$$R_{off} = R_{gi} + R_{fb} + \frac{R_{ex1} + R_{ex2}}{R_{ex1}R_{ex2}} + R_{snk} \quad (3.11)$$

As discussed in [10] the driver and switch layout depicted in figure 3.2 results in lower gate oscillations compared to using a PNP transistor to pull the gate low during turn-off. One of the drawbacks of using the proposed layout is that the turn-off might take a longer time since the current that flows out from the gate is limited by high resistance in the driver. In order to try to mitigate this problem a driver with low output sinking resistance is required. To avoid problems with unstable/changing ground potential an isolated driver is also preferred. The chosen driver circuit is UCC21521 from Texas Instruments. This is an isolated, dual channel gate driver with an output sinking resistance of  $R_{snk} = 0.55 \Omega$ .

The external components presented in figure 3.2 are designed by investigating MOSFET switching patterns and the data sheets of the relevant components. The circuit might be designed in such a way that the turn-on and turn-off resistances are equal. In this case the external resistor  $R_{ex2}$  and the diode  $D_{off}$  can be removed which can be beneficial since it results in lower loop inductance because of a physically shorter loop. If the turn-on and turn-off resistances of the circuitry are to be equal/similar using only one gate resistor, the internal output resistances of the driver must also be equal. Unfortunately the data sheets lists a sinking resistance of  $R_{snk} = 0.55 \Omega$  and a sourcing resistance of  $R_{src} = 5 \Omega$ . Luckily there is an internal pull-up MOSFET in parallel with the driver totem pole P-channel MOSFET which should start to conduct during the Miller-plateau. The resistance of the parallel pull-up is stated to be approximately  $1.47 \Omega$  which brings the effective sourcing and sinking resistances closer together. In order not to fall below a total gate resistance of  $10 \Omega$  the external resistor  $R_{ex1}$  should not have a higher value than  $R_{ex1} = R_{on/off} - R_{fb} + R_{gi} + R_{snk} = 10 - 0 - 1.2 - 0.55 = 8.25 \Omega$ , under the assumption that  $R_{fb} = 0 \Omega$ .

The manufacturer of the MOSFET recommends the usage of a ferrite bead close to the gate pin for fast switching applications in order to reduce any gate ringing. The ferrite bead should not saturate during operation and provide high resistance for high frequencies but not alter the PWM signal too much. The chosen bead is



$Q_C = 7.6 \text{ nC}$ . The losses of this component can be calculated using (2.42) and (2.43) to  $P_{D,conduction} = 1.56 \text{ W}$  and  $P_{D,switching} = 1.52 \text{ W}$ .

## 3.7 Smoothing and loop capacitors

### 3.7.1 Bulk capacitance value

The output capacitor, or bulk capacitors, of a PFC can be dimensioned based on the required hold up time and minimum output voltage. In this case, the output voltage does not need to be investigated since the size of the capacitor is based on the hold up time. This is often high enough to keep any output voltage ripple low enough to have insignificant effect on the power factor [21].

Assume that there is no energy storage in the PFC components and that the load will consume the rated output power during the hold up time. The losses in the capacitor is also assumed to be zero. Thus, energy in the capacitor can thus be written as  $E_C = \frac{1}{2}CV^2$  and the the needed bulk capacitance ( $C_o$ ) can therefore be written as

$$C_o = \frac{2P_o T_{hold}}{V_{initial}^2 - V_{min}^2} \quad (3.12)$$

where  $T_{hold}$  is the designing hold up time,  $V_{initial}$  is the voltage before the supply interruption and  $V_{min}$  is the voltage after the interruption has ended. To fulfill the requirements of specifications the minimum size of the capacitor is  $572\mu F$ .

### 3.7.2 Ripple RMS and $\tan \delta$

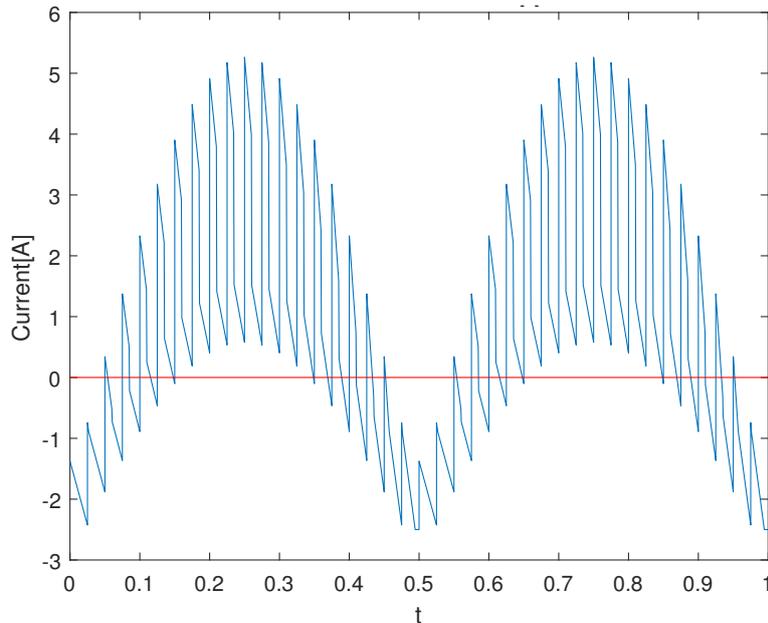
The capacitor can not handle infinite ripple amplitudes because of losses. Therefore the ripple into the bulk capacitors is investigated.

Figure 3.4 shows a simplified version of the ripple in the bulk capacitors. The simplifications made during this plot is that the amplitude of the inductor ripple is constant throughout the whole period of the 100 Hz wave. This means that the amplitude of the ripple only holds true at the two peaks at times 0.25 and 0.75 in the figure. A lower switching frequency is used for illustrative purposes. As the ripple height is the same, the figure is useful for dimensioning the required ripple capacity of the capacitors. As can be seen in the figure there are ideally two kinds of ripple: one with the twice the grid frequency and one with twice the switching frequency.

The low frequency ripple  $I_{Cio,RMS}$  can be calculated as

$$I_{C_{lo},RMS} = RMS(I_{D1,lo} + I_{D2,lo} - I_{Load}) \quad (3.13)$$

where  $I_{D1,lo}$  and  $I_{D2,lo}$  simplified as half the input current during low line operation and  $I_{Load}$  as the load current corresponding to 1 kW at 400 V results in  $I_{C_{lo},RMS} = 2.99$  A. The high frequency ripple amplitude can not exceed the maximum inductor ripple which is 1.42 A.



**Figure 3.4:** Graph depicting a simplified summation of the PFC diode currents.

The ESR of an electrolytic capacitor is frequency dependent and is defined as the sum of all the dielectric and connection resistance and can be calculated as [22]

$$R_C = \frac{\tan\delta}{2\pi fC} \quad (3.14)$$

where  $\tan\delta$  is given in the data sheets,  $f$  is the ripple frequency and  $C$  is the capacitance of the given capacitor.

Rubycon QXW series specifies  $\tan\delta = 0.24$  for their 450 V electrolytic capacitors. Four 180  $\mu F$  capacitors satisfy the minimum bulk capacitance requirement. The ripple capacity for the bulk capacitors at 60 Hz (100 Hz not specified) is 3.5 A. With a  $\tan\delta$  of 0.24 the ESR of the bulk capacitors can be found using (3.14) to be 530  $m\Omega$  resulting in a loss of  $2.99^2 A^2 * 0.530 \Omega = 4.7$  W.

As previously stated it is important to minimize the high frequency, high current loops. This can be done by placing a ceramic capacitor directly to ground after the Schottky diodes. This capacitor will act like a bypass capacitor. The PCB layout is at this stage not decided and it is possible that the Schottky diodes will be placed

far apart in order to minimize parasitic inductances for the switches and drivers. Because of this two capacitors are used, one for each channel. The voltage ripple can be calculated as  $\Delta V = \frac{\Delta Q}{C}$ , assuming that all the ripple flows through the capacitors and that the average current through the diodes are  $\frac{P_o}{2V_o}$ . The maximum change in charge  $\Delta Q$  would be if  $D = 1$  (or 0) and the high frequency voltage ripple could therefore be estimated as

$$\Delta V_{out,HF} = \frac{P_o}{2V_o C_{o,HF} f_s}, \quad (3.15)$$

where  $C_{o,HF}$  is the capacitance of the bypass capacitor used for high frequency bypass. TDK CKG57KX7T2J474M335JH7 0.47  $\mu F$ , 630 VDC can be used for the high frequency ripple. This one is selected because of its small size and its good DC-bias characteristics. At 400 VDC bias and neglecting temperature, the remaining capacitance is 0.188  $\mu F$ , leading to a voltage ripple less than 7 V. The ESR at 1 MHz can be read from the data sheet to 20  $m\Omega$  so the losses can be neglected and a low impedance path for the high frequency ripple is provided.

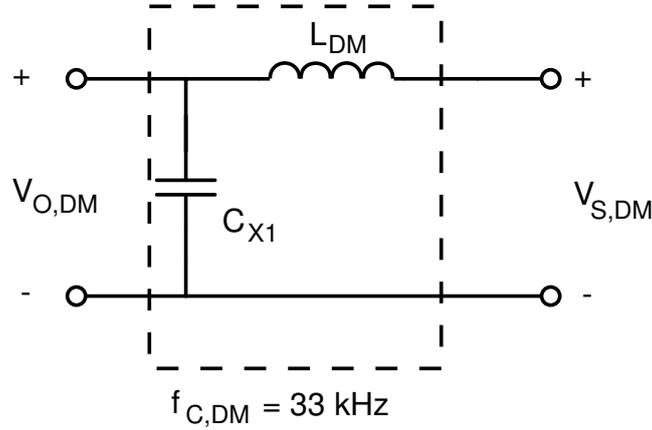
Another bypass capacitor is added after the diode bridge rectifier to provide a shorter path for the high frequency ripple. The capacitor used will be the stacked ceramic capacitor TDK CKG57NX7T2J105M500JH 1  $\mu F$ , 630 VDC. This capacitor forms a LC filter together with the boost inductors which will have a positive impact on the conducted EMI.

## 3.8 Calculated suppression of inductor ripple

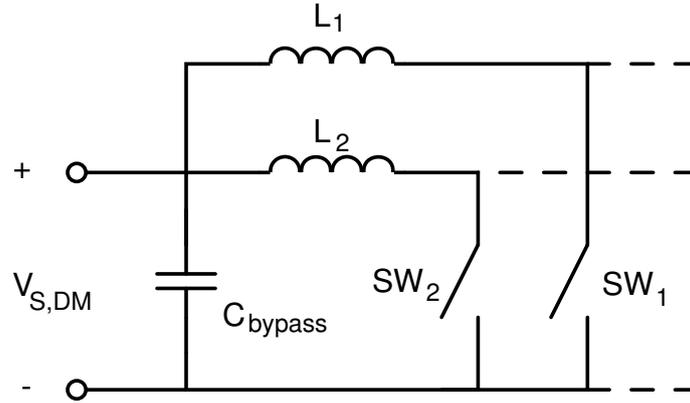
The ripple in the inductors are attenuated in several stages of the design. Firstly the bypass capacitor which forms an LC filter with the inductors. Secondly, the ripple is attenuated by the EMI filter. In addition to this, some of the ripple cancels out because of the interleaved operation.

Given that the EMI filter is designed in such a way that  $C_{X1}=C_{X1}=C_{DM}$  the equivalent circuit for attenuation of differential mode voltage noise can be drawn as depicted in figure 3.5 [12]. The differential noise voltage source  $V_{S,DM}$  caused by the inductor ripple can be represented as shown in figure 3.6.

The inductors are charged and discharged during each switching period. Assuming that all energy is provided by the 1  $\mu F$  bypass capacitor it is possible to relate the inductor ripple to a voltage ripple across the capacitor. The maximum ripple energy that is stored in the inductor occurs at the peak of the input current which during low line operation is 7.12 A. The difference in energy in the inductor because of the 1.42 A ripple can be calculated as



**Figure 3.5:** Circuit representation of DM noise attenuation of the EMI filter.



**Figure 3.6:** DM noise source circuit representation.

$$\Delta E_L = \frac{1}{2}L\hat{I}_L^2 - \frac{1}{2}L\check{I}_L^2 \quad (3.16)$$

where the currents are calculated using (2.12) and (2.19) which, using  $L = 35 \mu\text{H}$ , yields  $\Delta E_L = 177 \mu\text{J}$ .

In the same manner, if the resulting voltage change across the bypass capacitor is small, the DC-bias effect of the voltage ripple of the capacitor is also negligible. So if the voltage across the capacitor  $V_{C,bypass}$  is approximated to be constant 325 V the  $1 \mu\text{F}$  capacitor will effectively only have 450 nF. The resulting voltage change because of  $\Delta E_L$  can be found by solving

$$\frac{1}{2}C_{bypass}V_{C,bypass}^2 = \Delta E_L + \frac{1}{2}C_{bypass}(V_{C,bypass} - \Delta V_{C,bypass})^2 \quad (3.17)$$

for  $\Delta V_{C,bypass}$ . Given  $C_{bypass} = 450 \text{ nF}$ ,  $V_{C,bypass} = 325 \text{ V}$  and  $\Delta E_L = 177 \text{ } \mu\text{J}$  the equation can be solved, resulting in  $\Delta V_{C,bypass} = 1.21 \text{ V}$ .

Since there are two channels the frequency of the ripple will be 2 MHz and the differential mode noise voltage source is therefore simplified as  $V_{S,DM} = \frac{1.21}{2} \sin(2\pi t * 2 * 10^6) \text{ V}$ .

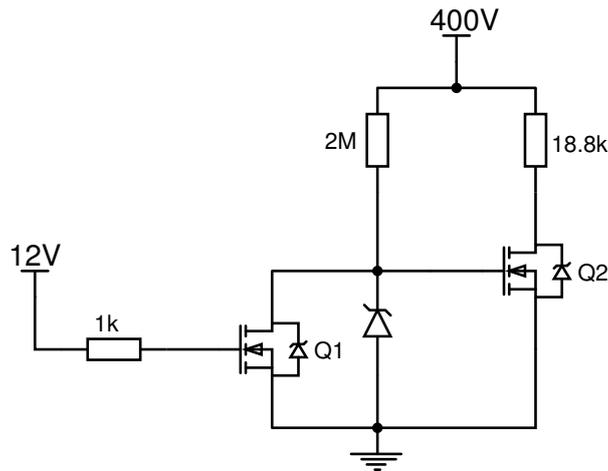
The cut-off frequency of the DM noise of the EMI filter is 33 kHz and the attenuation of  $V_{S,DM}$  is therefore equal to  $40 \log(\frac{2 * 10^6}{33 * 10^3}) = 71.3 \text{ dB}$ . The differential mode noise, caused by the inductor ripple, after the EMI filter have thus an amplitude of  $V_{O,DM} = \frac{1.21}{2} * 10^{-\frac{71.3}{20}} = 165 \text{ } \mu\text{V}$ . This is the maximum possible noise without cancellation caused by two channel operation.

## 3.9 Bleeder circuit

In order to ensure a safe handling of the device it is important to discharge the bulk capacitors when the unit is turned off. If no load is attached to the output and no discharging resistors are incorporated in the circuit the output would carry lethal voltage long after the device is disconnected from the grid. Bleeder resistors are therefore necessary to use.

A suitable choice are four  $4.7 \text{ k}\Omega$  resistors connected in series. Calculating a worst case scenario with a bulk capacitor voltage of  $450 \text{ V}$ , a bulk capacitance of  $720 \text{ } \mu\text{F} + 20 \%$  and a bleeder resistance of  $18.8 \text{ k}\Omega + 5 \%$  gives a discharging time of about 34 seconds, i.e. until a safe DC-voltage of  $60 \text{ V}$  is reached. The use of four bleeder resistors provides a spread of heat dissipation and ensures that the breakdown voltage for each of the resistors is not exceeded.

If the bleeder resistors are connected directly to the bulk capacitors an extra power loss is introduced in the circuit, generating heat and reducing the efficiency. One way around this issue is to implement a transistor circuit that only is enabled when the device is turned off. Such a circuit can look like depicted in figure 3.7. The four bleeder resistors are here lumped together as one  $18.8 \text{ k}\Omega$  resistor. When the device is powered from the grid the  $12 \text{ V}$  supply will be available and drive the gate of Q1 high, which in turn drives the gate at Q2 to ground so no current will flow through the bleeder resistor. When the  $12 \text{ V}$  supply disappears at power off the voltage over the bulk capacitors drive the gate of Q2 high and thus activate the discharging of the bulk capacitors. The zener diode ensures that the gate voltage is kept at a, for the transistor, suitable level.



**Figure 3.7:** Bleeder circuit that is disabled when the power is on.

### 3.10 Low voltage supply

In order to supply the needed 3.3 V the AC-line voltage is converted to 5 V using a 5 W PCB mounted AC/DC converter. In order to decrease the voltage further and to decrease any ripple, a linear regulator is used. A so called Low Drop Out (LDO) regulator is preferred because the voltage supplied from the AC/DC converter is 5 V, which is close required 3.3 V. Some LDOs requires an output capacitor with relatively high ESR, like electrolytic capacitors, since its control system is designed for that [23]. A parallel ceramic capacitor could effectively lower the output resistance so that the LDO control system malfunctions. Ceramic capacitors will be used as decoupling capacitors for several ICs supplied with 3.3 V which is why a LDO specifically designed for ceramic capacitors is required. A suitable regulator is LP2989 which is able to provide 500 mA at 3.3 V. According to its data sheet the input capacitor should not drop below  $1.5 \mu F$  and the output capacitor should not drop below  $2.2 \mu F$ . The output capacitor used will be ceramic so it is important to consider its DC-bias behaviour. In order to limit the effect of the DC-bias ceramic X7R capacitors rated for 25 V in 1206 SMD package is used. The chosen value for both input and output capacitor is  $4.7 \mu F$ . Another one of these regulator setups are used for the isolated USB supply voltage as well. The current requirements is presented in table 3.3 and table 3.4 and it can be concluded that the 500 mA provided by the regulator is enough.

The 12 V supply is used by the driver and a fan which consumes 2.45 W. The 12 V supply is supplied via a 5 W PCB mounted AC/DC converter. The energy provided by the low voltage supplies can be seen as losses. The specified typical efficiency of the AC/DC converters is 70 % and losses because of the 3.3 V supply is approximated as  $\frac{(153+60+30+0.006) mA \cdot 5 V}{0.7} \approx 1.74 W$ . This means that the total loss because of the low voltage supplies can be estimated as  $1.74 W + \frac{2.45}{0.7} W = 5.24 W$ .

**Table 3.3:** 3.3V board current requirements

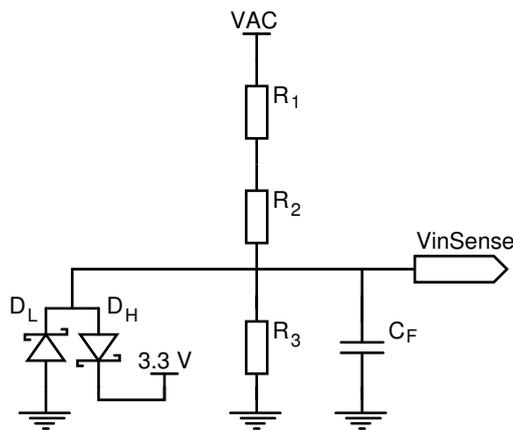
Discription	Part no.	Requirement [mA]
Digital isolator	ISO7240	25
Digital isolator	ISO7242	24
DSP	TMS320F28035PNS	153
2x OP-amps	OPA2365	~ 60
Gate driver	UCC21512	30
4x Signal LEDs	-	80
Linear active thermistor	MCP9700AT-E/LT	0.006
<b>Total</b>		~ 372

**Table 3.4:** Isolated 3.3V USB current requirements

Discription	Part no.	Requirement [mA]
Digital isolator	ISO7240	11
Digital isolator	ISO7242	24
UART/FIFO	FT2232HL	210
EEPROM	93LC56BT	2
LED	-	20
<b>Total</b>		~ 267

### 3.11 Input voltage dividers

The circuit that scales down the input voltage to a, by the DSP, measurable voltage is presented in figure 3.8.

**Figure 3.8:** Circuit for measuring the input voltage.

The circuit is essentially a resistive voltage divider where the resistors  $R_1$  and  $R_2$  values are chosen with respect for the current drawn by the sensing pin as to minimize the distortion of the signal. The reason why two resistors is used for the high side

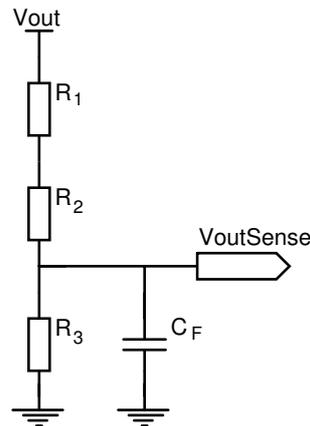
of the divider is to increase the voltage rating of the divider.  $432\text{ k}\Omega$ ,  $500\text{ V}$  SMD resistors are used for  $R_1$  and  $R_2$ . The package of these resistors are 1206 and the distance between the leads of the solder pattern will be therefore be  $1.6\text{ mm}$ . This is in accordance with the IPC-2221 standard for electrical conductor spacing which require a minimum of  $0.8\text{ mm}$  separation of the conductors in this application. The low side resistor,  $R_3$ , is chosen to be  $7.15\text{ k}\Omega$  if the signal  $V_{inSense}$  is to be kept below  $3\text{ V}$  at normal operation. The diodes are protecting the sense pin by limiting the voltage that can occur over it. If an error causes the voltage on the sense pin to go above  $3.3\text{ V}$  or below  $0\text{ V}$  the diodes will conduct and thus protect the processor from being destroyed.

$C_F$  together with the resistances of the divider forms a low pass filter in which  $-3\text{ dB}$  is reached at

$$f_c = \frac{1}{2\pi \frac{(R_1+R_2)R_3}{R_1+R_2+R_3} C_F} \approx 5.8\text{ kHz} \quad (3.18)$$

## 3.12 Output voltage divider

The circuit used to sense the output voltage is shown in figure 3.9.



**Figure 3.9:** Circuit for measuring the output voltage.

The same reasoning as applied in section 3.11 applies to this divider. The values of  $R_1$  and  $R_2$  are  $1\text{ M}\Omega$ ,  $R_3$  is  $10\text{ k}\Omega$  and capacitor  $C_F$  is  $7.8\text{ nF}$  (two  $3.9\text{ nF}$  capacitors are used). No protective Schottky diodes are needed here as the output voltage is controlled by the processor.

### 3.13 Current measuring circuits

The current through the two switches is measured as one measurement. The current is passed through a  $20\text{ m}\Omega$  current sense resistor. The peak of the current through this resistor occurs at the peak of the input current during low line operation and when the inductor ripple reaches its maximum. The current at this point is  $8.6\text{ A}$  which will result in a voltage of  $172\text{ mV}$  across the sense resistor. However it is good to be able to measure an even larger current so the PWM can be controlled even at an overcurrent state. The DSP's ADC can measure a voltage between  $3.3$  and  $0\text{ V}$ . To optimally utilize this window an operation amplifier, OP-amp, in differential configuration is used to amplify the measured voltage. With a gain of  $10$  the highest measurable voltage is  $330\text{ mV}$  and thus  $16.5\text{ A}$ . The chosen OP-amp, OPA2365, can output voltages close to the supply voltage rails but not exactly, which is why the linearity is reduced at the limits. At the upper current limit, this is not a big problem but it is important that currents close to zero also can be measured accurately. This issue is mitigated by raising the positive leg of the OP-amp by a small fixed voltage offset. The lowest output voltage of the OP-amp is now the offset voltage and the nonlinear tendencies are therefore avoided. This comes at a cost of decreased resolution due to a smaller measuring window, which is deemed to be an acceptable tradeoff.

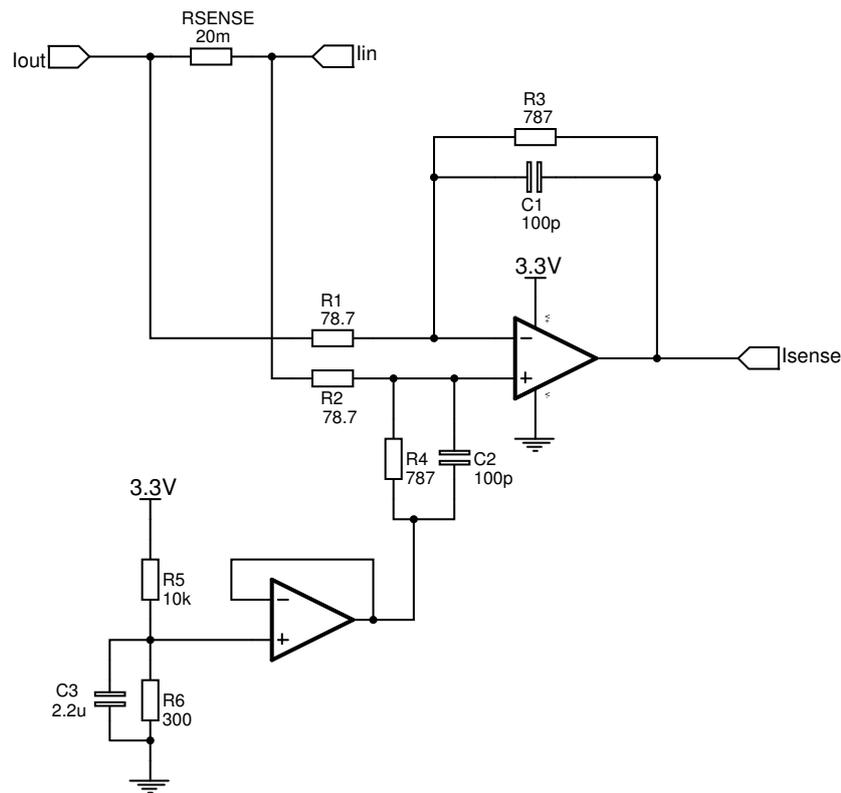
The sensor voltage amplified by the OP-amp should be low pass filtered to get rid of any unwanted noise. This is done by adding a couple of capacitors to the differential amplifier to form a Butterworth filter. The complete current measuring circuit is shown in figure 3.10. The gain is given by  $R_3/R_1 = 10$ . The cutoff frequency for the differential low pass filter is given by  $\frac{1}{2\pi R_3 C_1}$  which in this case is about  $2\text{ MHz}$ . The voltage follower provides the voltage offset via the voltage divider. The chosen values of  $R_5$  and  $R_6$  gives an offset voltage of  $96\text{ mV}$ , while the capacitor  $C_3$  only acts as a filter.

The maximum current that can be measured when voltage offset and swing are taken into consideration is given by

$$I_{sense,max} = \frac{V_{supply} - V_{offset} - V_{satmargin}}{R_{sense}G} \quad (3.19)$$

where  $V_{supply}$  is  $3.3\text{ V}$ ,  $V_{offset}$  is the offset voltage calculated above,  $V_{satmargin}$  is the difference between the high/low rail voltage and the maximum/minimum output voltage,  $R_{sense}$  is the value of the sense resistor and  $G$  is the amplifier gain. For the OPA2365,  $V_{satmargin}$  is in the range of  $10\text{ mV}$ , but say  $20\text{ mV}$  to be on the safe side. This gives a maximum sense current of  $15.9\text{ A}$  before the OP-amp saturates which is good enough.

The DSP's ADC has a resolution of  $12$  bits, which equals to  $4096$  levels. The lowest



**Figure 3.10:** Current measuring circuit.

detectable current is calculated as

$$I_{resolution} = \frac{V_{supply}}{4096R_{sense}G} \quad (3.20)$$

which in this case is 4.3 mA.

Place holders are pre-emptively added to the PCB in order to make it possible to easily add a similar current measuring circuit in order to measure the output current if that is deemed necessary.

## 3.14 Digital Signal Processor

The DSP used for measurements, signal processing and PWM generation will be a Piccolo TMS320F28035 [24].

### 3.14.1 PWM output pins

The clock frequency of the DSP is 60 MHz. As a consequence the resolution of the duty cycle is poor since the switching period only can be divided into 60 parts when

using 1 MHz switching frequency. The resulting duty cycle resolution is 1.7 %. The DSP has a functionality called High Resolution PWM, HRPWM for short, which means that the DSP is able to divide the system clock into smaller time steps for these HRPWM-pins [25]. The improved resolution of the duty cycle is 0.018 %, and therefore these pins will be used for the PWM signal to the MOSFET drivers.

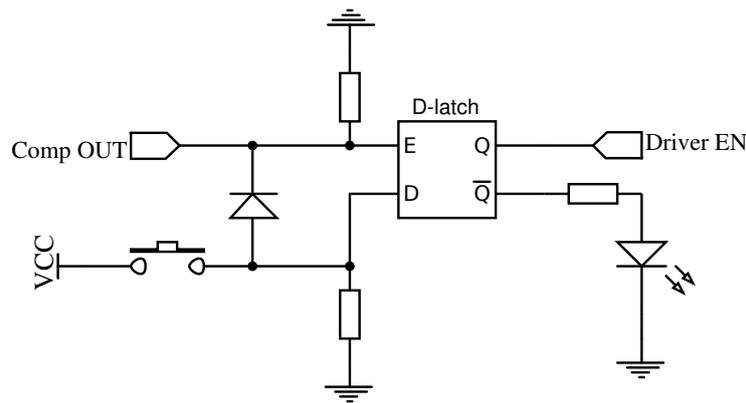
### 3.14.2 Overcurrent protection

To be able to safely operate the PFC circuit, some kind of overcurrent protection is needed. This is especially important in an early developing state where bugs can cause the transistor switching to malfunction - resulting in damaging currents. The protection needs to have a very short response time as any prolonged short circuit would immediately destroy the transistors and possible other components as well. A simple fuse is therefore not sufficient as it reacts too slow.

The most reliable way to protect the components is to rapidly turn off the PWM switching. This can be done in the DSP software as the current is measured by the DSP. The DSP can turn off the PWM output if the current is measured to be above a certain value. However, the current will most certainly not be sampled at the switching frequency but probably around one tenth of the switching frequency. This means that a lot can happen between the current samples and the transistors can have been blown into smoke before the overcurrent is detected. To get an asynchronous and quick enough disabling of the PWM, analogue circuits are needed.

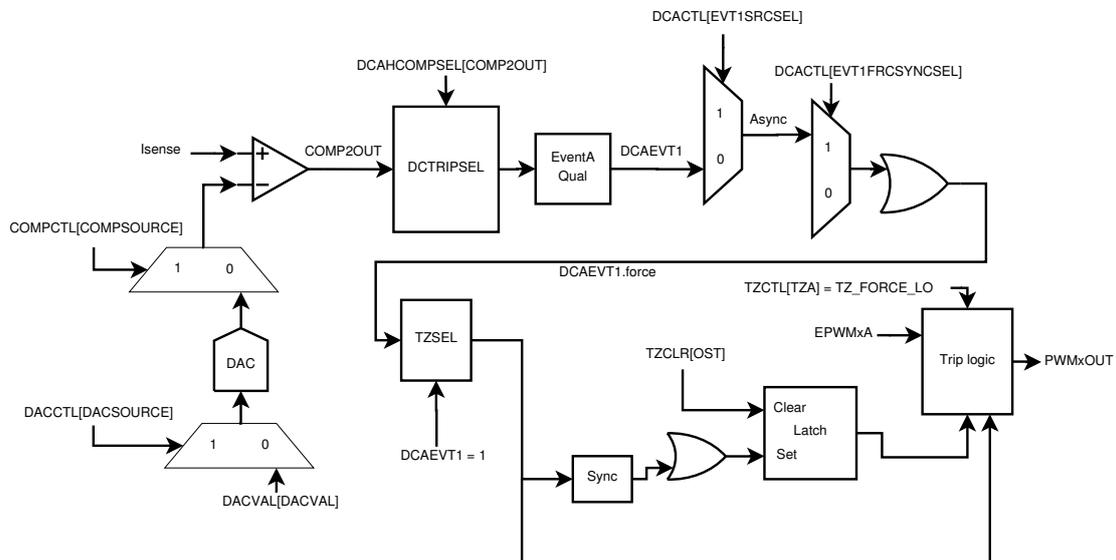
The DSP have built-in analogue comparators connected to some of the analogue inputs [26]. The comparator can compare the analogue level at the input with a reference value from an internal DAC. The reference value is set in software but the comparison is purely analogous. The output of the comparator is fed to one of the pins of the DSP. This signal can be connected to the *Enable*-inputs on the transistor drivers. The voltage over the current sense resistor can thus be fed to one comparator input and if the current is too high, the voltage will be higher than the defined reference, the comparator trips and disables the drivers and therefore the transistors. This is all done within a few nanoseconds. The drivers would however turn on again when the current once again is within nominal range. But an overcurrent is a serious issue and the drivers must be kept disabled until a manual reset is done. This can be done by setting a very quick latch between the comparator output of the DSP and the drivers' *Enable*. Figure 3.11 illustrates a D-latch with a manual reset possibility. When the reset button is pushed, Q goes high and enables the drivers. If the output from the DSP's comparator goes high due to an overcurrent, Q immediately goes low and disables the drivers. At the same time a LED lights up to show that an overcurrent event occurred and a reset is needed. The reset feature may also be implemented in software by connecting another DSP pin to the D-input of the latch.

There are however other ways to implement the overcurrent protection as well. The



**Figure 3.11:** Overcurrent protection circuit with manual reset.

output of the DSP's comparator can internally be connected to the PWM generating stage and there directly turn off the outputs. This can also be done asynchronously, leading to very short propagation times. This method is slightly more complicated and requires a bunch of registers and multiplexers to be set but does not on the other hand require any external hardware [24, 26, 27]. The internal signal path is shown in figure 3.12 where only the relevant registers and signals are included. When the signal passes the TZSEL-switch, the signal takes both an asynchronous



**Figure 3.12:** Internal processor path for overcurrent protection.

and synchronous path to the Trip logic-block. The asynchronous path makes the PWM output pin to go low immediately, but for the pin to stay low the latch needs also be set. The latch will be set if the fault is longer than at least three clock cycles, which for 60 MHz is 50 ns. If the latch is set high, a LED connected to the DSP can be turned on by software. The latch can be reset by setting the OST in the TZCLR register.

### 3.14.3 USB interface

To be able to upload firmware to the DSP and debug it, the DSP is equipped with both a serial and a JTAG interface. These interfaces are connected through isolation circuits to an USB FTDI chip, which provides a USB interface for communication with a PC. The isolation circuits ensures an electrical isolation between the USB connected computer and the DSP, provides equipment protection and user safety. These isolated interfaces, which are located in one of the corners of the PCB, are marked in the silk. The schematics can be found in the appendix A.

## 3.15 Summation of component losses

The calculated losses are summarized and presented in table 3.5.

**Table 3.5:** Calculated losses of the system, sorted by loss contribution

Discription	Loss/component [W]	Loss [W]
Boost MOSFET	15.9	31.8
Rectifier	8.2	8.2
Boost diode	3.1	6.2
LV-supply	5.2	5.2
Bulk capacitors	4.7	4.7
Boost inductor	2.2	4.4
<b>Total loss</b>		58.8 W
<b>Expected efficiency</b>		94.4 %

## 3.16 Heat mitigation

According to relevant data sheets and the result of the loss calculations, presented in table 3.5, the following components will need cooling: the MOSFETs Q2 and Q3, the boost diodes D4 and D5, and the diode bridge rectifier U4. The boost inductors may also need active cooling depending on their performance and the air flow in the encapsulating box.

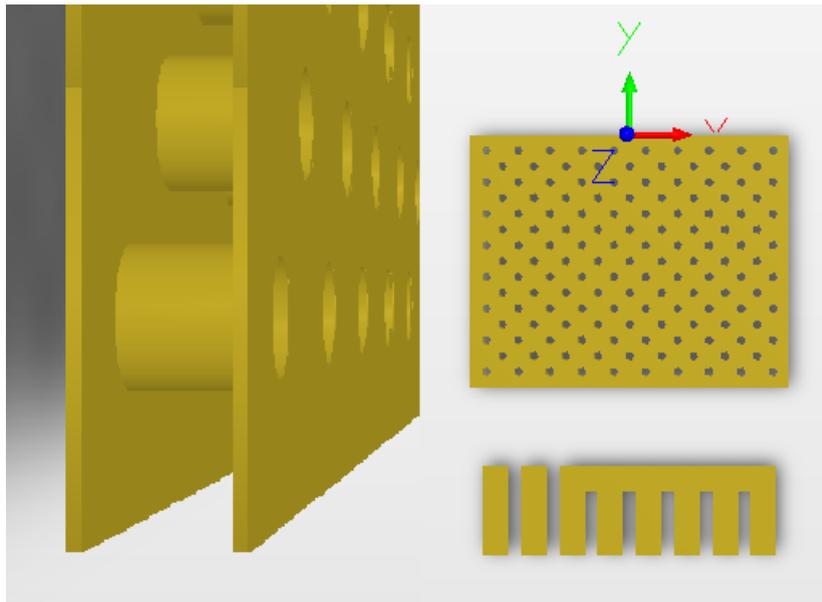
### 3.16.1 MOSFET and boost diode footprints

The MOSFETs and boost diodes are cooled through the tabs which are located on the bottom side of the components. This means that the cooling have to be done through the PCB. The thermal conductivity of the MOSFET footprint on a standard FR4 PCB is about 66 K/W [28]. 17.4 W is dissipated in each MOSFET

and the resulting temperature increase because of the PCB would theoretically be  $17.4 W * 66 K/W \approx 1150 ^\circ C$ , which of course would be impossible. The thermal resistance of the PCB needs to be decreased in order to not burn the switches. This can be done by implementing footprints with thermal vias. A thermal via is just a regular via, which essentially is a plated hole in the PCB, used for its thermal conductivity purposes. [28] recommends hole sizes of 0.3-0.5 mm with a separation distance of 0.5-1 mm. The thermal resistance of one thermal via can be calculated as [28]

$$R_{th,Via} = \frac{h_{PCB}}{\lambda \pi s (\varnothing_{via} + s)} \quad (3.21)$$

where  $h_{PCB}$  is the thickness of the PCB,  $\lambda$  is the specific thermal conductivity of copper,  $s$  is the thickness of the copper plating in the hole and  $\varnothing_{via}$  is the hole diameter. Thermal vias are implemented for the MOSFET and boost diode footprints and the footprint of the MOSFETs are depicted in figure 3.13.



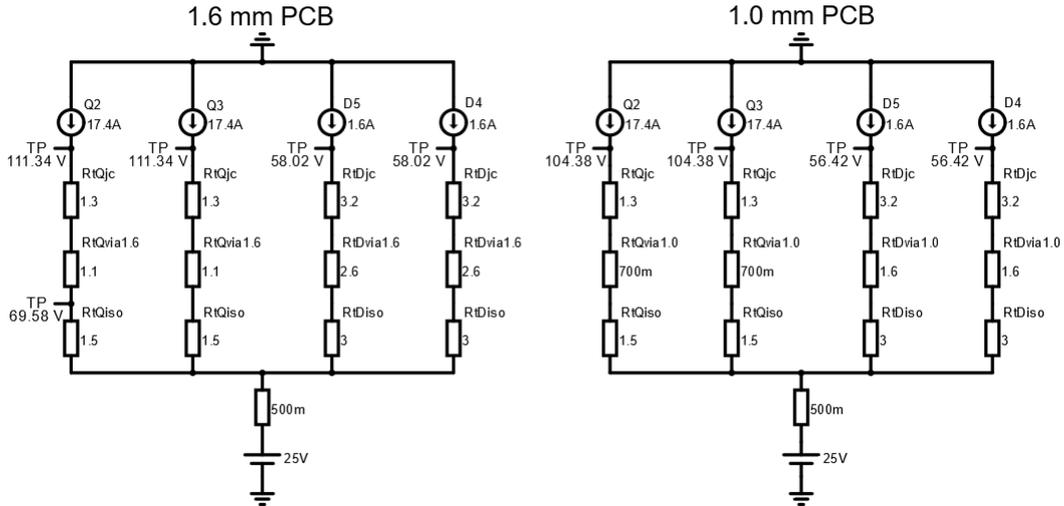
**Figure 3.13:** MOSFET footprint with thermal vias for reduced thermal resistance.

The vias are placed in two overlapping matrices shifted 0.5 mm in which the space between the centre of the holes are 1 mm. This results in a pattern in which, given that the hole diameter is 0.3 mm, the distance between the edges of the via holes are  $407 \mu m$ . This is above the specified minimum distance of  $400 \mu m$  for the considered PCB manufacturer. The thermal conductivity of one via can be calculated using (3.21) to  $\sim 155 K/W$  given a 1.6 mm thick PCB, a hole diameter of 0.3 mm and that the plating is  $25 \mu m$ . The MOSFET footprint implements 142 vias while only 60 vias fits in the boost diode footprint. This means that the thermal

### 3. Method

resistance of the footprints are  $Rt_{Qvia} = \frac{155 \text{ K/W}}{142} = 1.1 \text{ K/W}$  for the MOSFET and  $Rt_{Dvia} = 2.6 \text{ K/W}$ .

A common thickness for PCBs are 1.6 mm but thinner PCBs are possible. The observation that the thermal resistance of the via is directly proportional to the PCB thickness can easily be made given (3.21). Steady state thermal performance for the different thicknesses can quickly be made by simulating the corresponding thermal circuitry which is presented in figure 3.14.



**Figure 3.14:** Thermal circuit comparison of different PCB thicknesses.

The thermal circuit analysis assumes  $25 \text{ }^\circ\text{C}$  ambient temperature, a heat sink with a thermal resistance of  $0.5 \text{ K/W}$  like a CPU cooler or similar and specific isolation pads[29]. It can be noted, at the MOSFET TP, that there is a temperature difference of about  $7 \text{ }^\circ\text{C}$  between the different PCB thicknesses. Considering the price difference, the increased operating temperature of the 1.6 mm PCB is deemed acceptable.

A thermal sensor is added close to the two boost channels in order to add some thermal protection. The thermal sensor consists of the linear active thermistor MCP9700/9700A and is thermally connected to the heat sink through vias.

#### 3.16.2 MOSFET and boost diode heat sink

Given that the MOSFETs and boost diodes will be located close together to minimize the high frequency loops it is possible to use a heat sink with a relatively small contact area like a CPU cooler. The chosen heat sink is a low profile construction with a fan mounted on top. The total height is 37 mm. The fan will be placed in such a way that fresh air is pulled from the outside of the encapsulating box.

### 3.16.3 Thermally conductive isolation pad

Since the boost MOSFETs and diodes share the heat sink it is necessary to add an electrical insulator in between the heat sink and the PCB. This insulator needs to have a low thermal resistance in order to keep the components from being damaged. The thermal heat sink pad Hi-Flow 300P with a thermal impedance of  $0.84 \text{ cm}^2\text{K/W}$  from Bergquist is used and has a thickness of  $102 \mu\text{m}$  and a breakdown voltage of 5 kVAC. The pad is delivered in sheets which are cut to cover the contacting part of the heat sink which is  $40 \times 40 \text{ mm}$ . The PCB area that will contact the heat sink will have no solder mask in order to try to improve the interface between the component footprints and thermal pad.

### 3.16.4 Diode bridge rectifier heat sink

The full bridge rectifier will have a separate heat sink since it is cooled via the top of the component. The heat sink chosen is 6222BG by Aavid Thermalloy which has a thermal resistance of  $9.4 \text{ K/W}$  without forced cooling, resulting in a maximum temperature increase of  $77 \text{ }^\circ\text{C}$ . Worth noting is that the air inside the box will likely not be totally still because of the setup of the CPU cooler.

## 3.17 PCB design

### 3.17.1 General component placement and routing strategy

The PCB is drawn using the software Altium. Firstly, the components are placed and connected in small groups consisting of for example one linear regulator with its associated resistances and capacitances. Secondly, these small groups of routed components are placed together to form larger component clusters, i.e. the USB interface, in order to get more manageable pieces to work with in order to structure the PCB layout. Finally the clusters are connected. Digital signals are kept away from analog signals in order to try to avoid noise problems.

Components can be placed on both sides of the board in all areas except the area covered by the heat sink interface. Also, THT components placed close to the heat sink must not violate the minimum isolation distance. On this PCB almost all components are placed on the top side. The PCB is a four layer  $70 \mu\text{m}$  copper board with most of the signal routing on the top layer, while power routing and grounding is done on layer two and three. The last layer is used when signals need to cross and to connect the few bottom side mounted components.

Decoupling capacitors are placed in such a way that the routing length is minimized. The decoupling capacitors are often connected to the second and third layer and this

is done using vias. The via is placed directly to the side of the capacitor pads in order to minimize the inductance to the decoupling capacitor [30].

#### 3.17.2 Board size

There are no board size restrictions in the specification of requirement, so the clusters are placed to form a rectangular board. The size of the board directly relates to the price, which is why some effort was made in order to minimize the size. The final dimensions on the PCB is 125x220 mm.

### 3.18 Encapsulation and connectors

In order to choose a suitable box, the final height of the printed board assembly needs to be established. The limiting component on the bottom side is the heat sink which builds 37 mm and the deciding component on the top side is the electrolytic capacitors which has a height of 46 mm. Since the PCB is 1.6 mm thick the minimum inner box height is  $\sim 85$  mm. A suitable box is Hammond RM20295L, mounting holes in the PCB are made to fit the mounting inside the box. The heat sink fan rests on the bottom of the box which has a hole for the air intake. Bumpers are therefore added to elevate the box in order to not hinder the air flow. According to the requirements of specifications the finished build should have generic input/output connectors. A flush mounted IEC-60320-C14 mains socket is mounted for the input. Black and red 4 mm safety banana jacks are mounted for the output. Both input and output connectors are connected using FASTON since this is used on the PCB.

### 3.19 Functionality verification

The verification has to be done in small steps which minimizes the risk of component damage as there are no delusions regarding the initial functionality of the product. This is why a plan of verification is made, which consist of a series of preplanned hands-on tests.

1. Test of low voltage supply before soldering
  - (a) Connect the LV supplies using alligator clips to a DC power supply.
  - (b) Ramp the voltage until they start.
  - (c) Connect appropriate loads and investigate the voltage.
  - (d) Establish a minimum working voltage under which both power supplies

are able to supply a load at an appropriate voltage level. This voltage level will be called mains in this list.

## 2. Construction of boost inductors

- (a) Cut litz wire at about 1.2 times the estimated length. Dip both ends in the tin boiler. Measure the resistance in the wire which, depending on the wire length, should be under 100 m $\Omega$ . This indicates correct lead termination.
- (b) Wind two cores of the same size with appropriate number of turns. Start with the largest one as it is the easiest to wind and test the other cores when the hardware is fully working. Keep in mind voltage/turn and isolation distance between different turns.
- (c) Use a LCR meter to check that the inductance value of the wound inductors are correct. The values should correspond to the following values since there is no DC-bias.
  - i. 51  $\mu$ H for SH-090060, approximately 36 turns.
  - ii. 43  $\mu$ H for SH-080026, approximately 58 turns.
  - iii. 45  $\mu$ H for SH-068026, approximately 51 turns.
- (d) Cut excess litz wire and re-solder the leads and use hot glue to fix the ends of the wire. Check the resistance again to make sure that the new terminations are properly done.

## 3. Verification of 12 V auxiliary power supply

- (a) Ohm meter TP1 (12 V), TP2 (5 V) and TP3 (3.3 V) to GND, should not be shorted.
- (b) Connect 12 V through TP1 and GND using a current limited power supply.
- (c) Measure 0 V at the gates of the boost switches, at start up. The voltage across C12 and C13 should be 12 V. Detach 12 V.
- (d) Attach connector J1-J7, J9-J12 and J14. Also solder the diodes D8-D10.
- (e) Connect heat sink fan and connect 12 V again. The fan should spin. Test both 12 V connectors.
- (f) Attach 20 V, with an ampere meter in series, via test pins to one of the electrolytic capacitor pads. When 12 V is applied to U1 output pads, the ampere meter should show 0 mA. When 12 V is absent, the current should be 1 mA, which flows through the 18,8 k $\Omega$  bleeder resistors.

### 3. Method

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- (g) Ohm meter J4 and J5 should show OL.
- (h) Solder U1.
- (i) Connect J4 and J5 to mains and measure TP1 (12 V), should show 12V.
- (j) Remove mains.

#### 4. Verification of 3.3 V auxiliary power supply

- (a) Connect a current limited power supply at the TP2 (5 V) and GND, use 4 V. Incrementally increase the power supply output to 5 V while measuring the voltage at TP3 (3.3 V), which should remain steady at 3.3 V.
- (b) Mount U2.
- (c) Attach mains.
- (d) Measure TP3 (3.3 V), should show 3.3 V. Measure TP2 (5 V), should show 5 V.
- (e) Turn on pin 3 on S1, D6 should light up.
- (f) Remove mains.

#### 5. Verification of 3.3 V analogue

- (a) Attach mains.
- (b) Measure 3.3 V at C5.
- (c) Measure 96 mV at TP16 (Isense) and TP24 (IoutSense).
- (d) Measure around 750 mV at TP26 (Temp). This indicates room temperature.
- (e) Remove mains.

#### 6. USB interface and basic DSP operation

- (a) Solder J14, C71 and C72.
- (b) Connect USB cable, D10 should light up.
- (c) Measure U18 output voltage by measuring voltage across C57, should be 3.3 V.
- (d) Connect mains to LV supplies.

- (e) Program the FTDI chip to emulate the Texas Instruments XDS100v2 interface, using the Blackhawk Control Panel utility.
- (f) Upload test firmware to the DSP, LEDblink.c - found in appendix D.2. Ensure that all DSP connected LEDs (D6-D9) can light up.
- (g) Unplug USB cable and mains.

#### 7. Verification of mains input

- (a) Solder relay K1 and NTC R5. Connect mains to J4 and J5, relay should not short R5 and 50 Ohms should still be measured across it.
- (b) Connect USB cable, set Rel\_bypass pin high through DSP. The relay should click, 0 ohms should show over the NTC.
- (c) Disconnect mains and USB connector.
- (d) Solder F2, attach fuse cartridge. Solder R6, L2, C7 and C8.
- (e) Ohm meter at J9 and J10. No short circuit.
- (f) Use the jumpers to short J4-J6 and J5-J7. Also connect J10 to GND and a volt meter between VACS-L and GND.
- (g) Short the NTC resistor R5 using alligator clips.
- (h) Apply mains to J9 and J10. J9 should be connected to minus and J10 to plus.
- (i) Volt meter on TP7 (VACS\_L), which should show  $492.6 \pm 9.8$  mV.
- (j) Upload the BoostControl program, from appendix D.1, with the PWM configs commented out, to the DSP. Use the expressions window to read the values. Check that VacL is reasonable.
- (k) Disconnect the applied voltage.
- (l) Swap the terminals J9 and J10, set the GND testpoint to J9.
- (m) Volt meter on TP13 (VASC\_N), which should show  $492.6 \pm 9.8$  mV.
- (n) Run the boost test program again and check that VacN is reasonable.
- (o) Read the Temp value on the DSP. Should show around room temperature.
- (p) Disconnect all voltages.

#### 8. Current and voltage measurement circuitry verification

### 3. Method

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- (a) Solder L12. Ohm meter between TP5 and J12, should show slightly above 40 m $\Omega$ .
- (b) Connect J12 to plus and TP5 to minus of a current limited (2 A) Power supply. Do not turn on, turn voltage knob to minimum. Attach a volt meter to TP16.
- (c) Connect 230 V to J4 and J5, the voltage shown should be 96 mV. Ramp up the current, 1 amp should equal 200 mV increase.
- (d) Check the Isense variable on the DSP so the read value is reasonable.
- (e) Disconnect all voltages and move measuring equipment to TP24 and repeat the above steps from 8.
- (f) Disconnect all voltages.
- (g) Connect the multimeter to TP25.
- (h) Connect J11 to plus and J12 to minus of a 60 V power supply, use caution when ramping the voltage.
- (i) Check that the values are reasonable and check corresponding Vout variable on the DSP.
- (j) Disconnect all voltages.

### 9. PWM and overcurrent protection verification

- (a) Activate both PWM outputs, synchronous but phase shifted 180 degrees, at 50 % duty cycle. Read the signals at TP22 and TP23. Check that the signals behaves as expected. Measure also on the gates to verify that the PWM signals are propagating to the transistors.
- (b) The overcurrent protection is tested by applying a low voltage to TP16. However, the circuit has a low resistive path to ground when doing so and therefore the protection must be set to a much lower voltage than usual. Set the DAC value to 155, which corresponds to 0.5 V on the pin or 2.5 A through the sense resistor. Slowly ramp up the voltage to 0.5 V. The PWMs should turn off and remain off when the voltage is decreased. LED D9 should be illuminated.
- (c) Reset the device and set the DAC value back to 639.
- (d) Apply a voltage at TP25. Slowly ramp up the voltage to 2.11 V, which correspond to a voltage of 425 V over the bulk capacitors. The overvoltage protection should trip the PWM outputs and remain off when the voltage is decreased. LED D9 should be illuminated.

- 
10. Power (overcurrent and overvoltage protection must be implemented and controlled, inspect using thermal camera)
    - (a) Disconnect all cables.
    - (b) Solder bulk capacitors and boost inductors as well as any remaining components. Allow for probe connection on pin 2 of the inductor.
    - (c) Program DSP to output 50 kHz with  $D = 0.20$  for one channel. The other channel should be off.
    - (d) Connect an oscilloscope to TP16 and GND using a voltage probe and a multimeter from TP25 to GND.
    - (e) Connect a electric load to J11 and J12 and set the resistance to  $20 \Omega$ , attach a power supply to J9 and J10.
    - (f) Connect LV-supplies.
    - (g) Ramp up the voltage to 32.5 V while watching the output voltage. There should now be 40 V at the output, CCM. The peak value of the input current should be around 5 A.
    - (h) Inspect the drain-source voltage of the switch by connecting a probe to pin 2 of the inductor and PGND at TP19.
    - (i) Inspect the gate voltage after the ferrite bead.
    - (j) Redo 10a-10i for the second channel.
    - (k) Incrementally increase the switching frequency and voltage in accordance with the following approach:
      - i. Voltage and switching frequency should be increased using  $V_{in} = K_v * 32.5 \text{ V}$ ,  $D = 0.2 \Rightarrow V_{out} = K_v * 40.6 \text{ V}$  and  $f_{sw} = K_f * 100 \text{ kHz}$ .  $K_f$  and  $K_v$  are just constants to track progress and are between 1 and 10.
      - ii. Keep  $K_v = 1$ ,  $R_{load} = 40 \Omega$  and incrementally increase  $K_f$  until  $K_f = 10$  while measuring and saving  $V_{ds}$ ,  $I_{ds}$  and  $V_{gs}$ . Redo for second channel.
      - iii. Set  $K_f = K_v$  and incrementally step their value until  $K_f = K_v = 10$  while inspecting and saving the waveform data. Keeping  $K_f = K_v$  BCM will be reached at a load current of  $750 \text{ mA} * 2 = 1.5 \text{ A}$ .
      - iv. Increase the load to 1 kW. Document the input power indicated by the voltage and input current.

### 3. Method

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- (l) When 1 MHz operation with full load, duty cycle 0.2, is verified, decrease the voltage and increase the duty cycle to about 0.425. Increase the voltage and fine tune the duty cycle until an input current of 4.54 A, as used in calculation (3.5), is measured while maintaining the output voltage of 400 V and 1 kW load. The losses in the circuit should now be close to what is expected during low line AC operation and the efficiency can therefore be estimated. Measure the efficiency.
  - (m) Now it is possible to do other hardware measurements like current ripples and brown out withstanding.
11. To test and evaluate the Texas Instruments ILPFC software, refer to the ILPFC documentation [17].

# 4

## Results

### 4.1 Verification and assembly

The verification process began with testing the low voltage power supplies in accordance with verification specification task 1 in order to determine their lowest working voltage. The five volt supply was found to be able to fully function at an input voltage of 60 VDC. At a load of 3.93 W the output voltage is 4.69 V. As the calculated maximum power requirement at the five volt rail is 1.74 W the given 60 V input will be sufficient for use under testing.

At 60 V input the 12 V power supply works to satisfaction, where it can supply 4.2 W at 12.16 V. The 12 V supply does actually start to function earlier than the five volt supply, but since the 5 V supply sets the worst case input level, a supply voltage of 60 VDC is used.

The linear regulators did not initially perform as intended as they were oscillating heavily. The problem was solved by removing the bypass capacitors C2 and C45. The capacitors are not required for the LDOs to operate but should decrease any voltage ripple further. However, the requirements on the capacitors are very narrow and the malfunctioning behaviour was probably caused by too poor capacitors. Once the 3.3 V supply was operational, 95 mV was measured at IOUtsense and Isense while 760 mV was read at Temp. The measured values are close to the expected values and the part of the verification is therefore deemed passed.

The measured voltage at VACS\_L is 492.6 mV when 60 V is applied as described in point 7 in the verification list. The measured voltage is within the accepted range and the input voltage circuits are therefore deemed to be working as intended.

### 4.2 PCB

The top side of the PCB is presented in figure 4.1 and a close up of the footprints for the boost stages is presented in figure 4.2. They are of special importance and the thermal vias are clearly shown. Images depicting the Gerber files of the copper

## 4. Results

layers are found in appendix B.

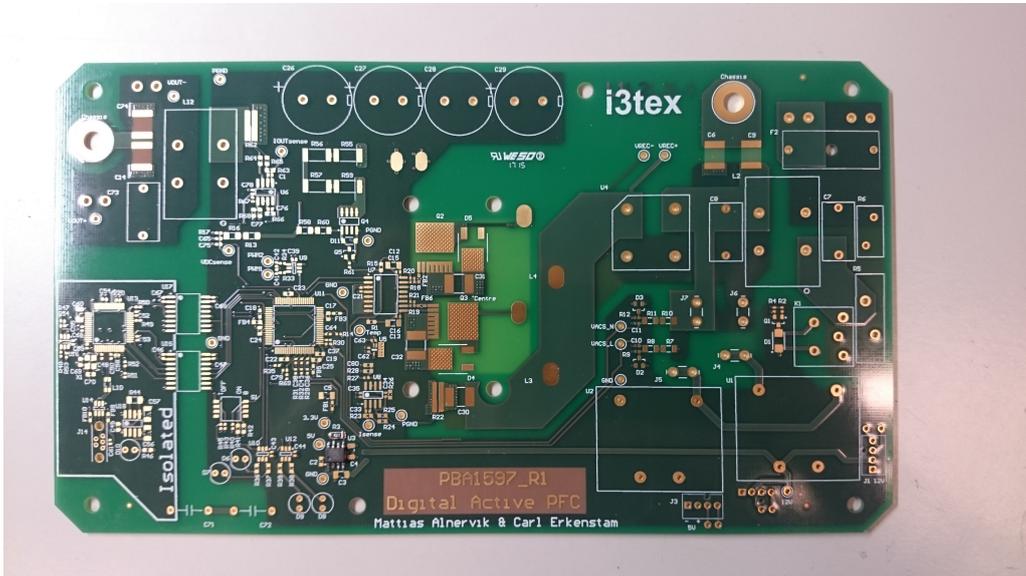


Figure 4.1: Top side of the PCB.

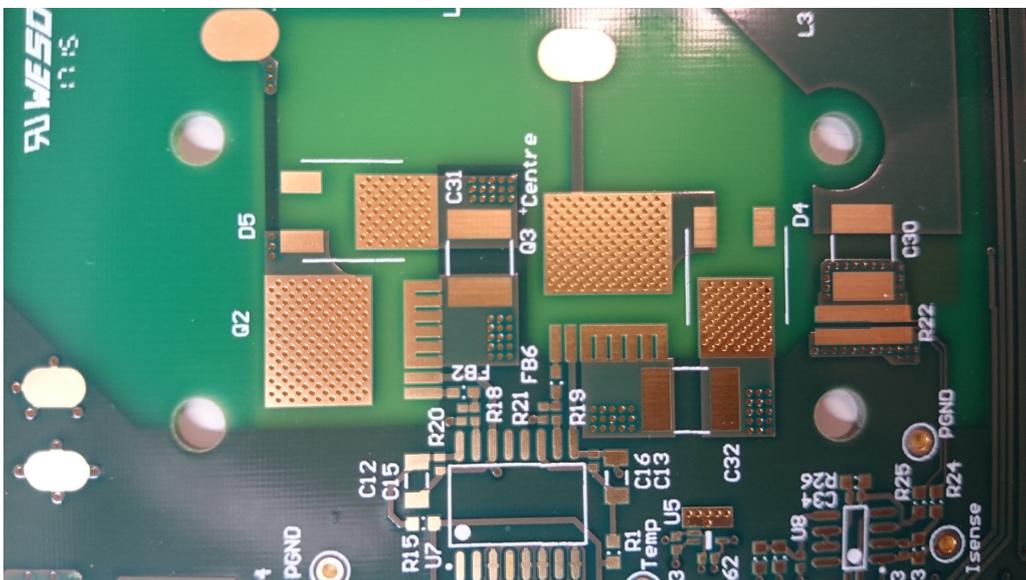


Figure 4.2: Close up of crucial footprints.

The bottom side of the PCB, which is shown in figure 4.3, does not have a lot of footprints. Notice that the solder mask is removed where the heat sink will meet the PCB.

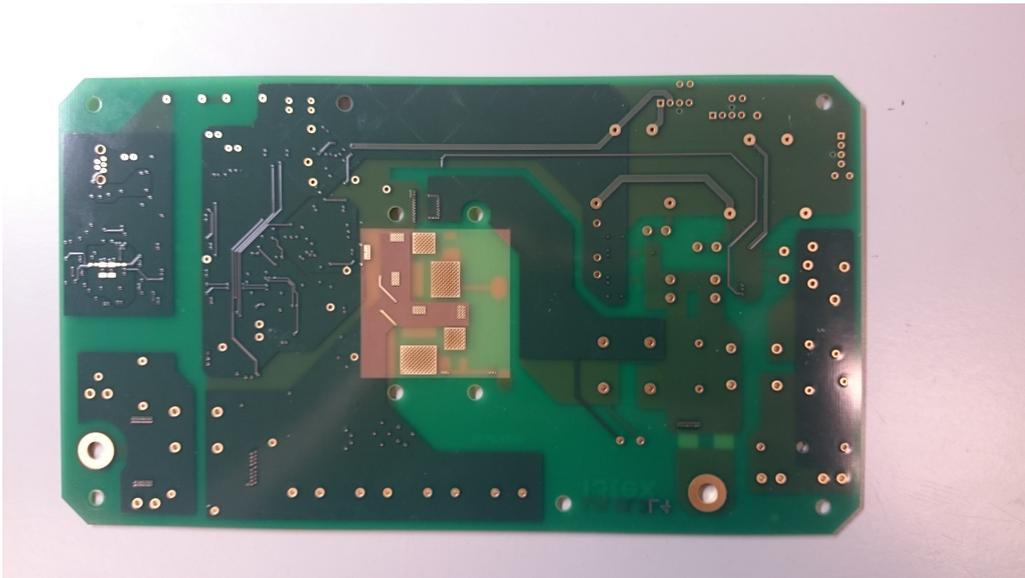


Figure 4.3: The bottom side of the PCB.

### 4.3 Final Assembly

The final PBA is presented in figure 4.4 and in figure 4.5 where the top and the bottom side of the PBA are shown respectively. All the used components and the schematics are found in appendix A and C.

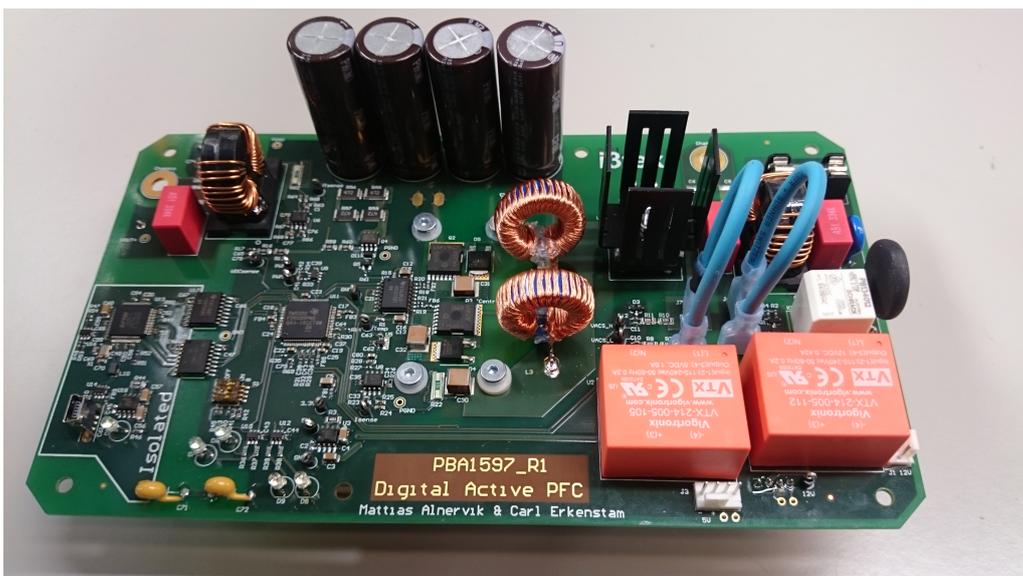


Figure 4.4: Top side of the PBA.

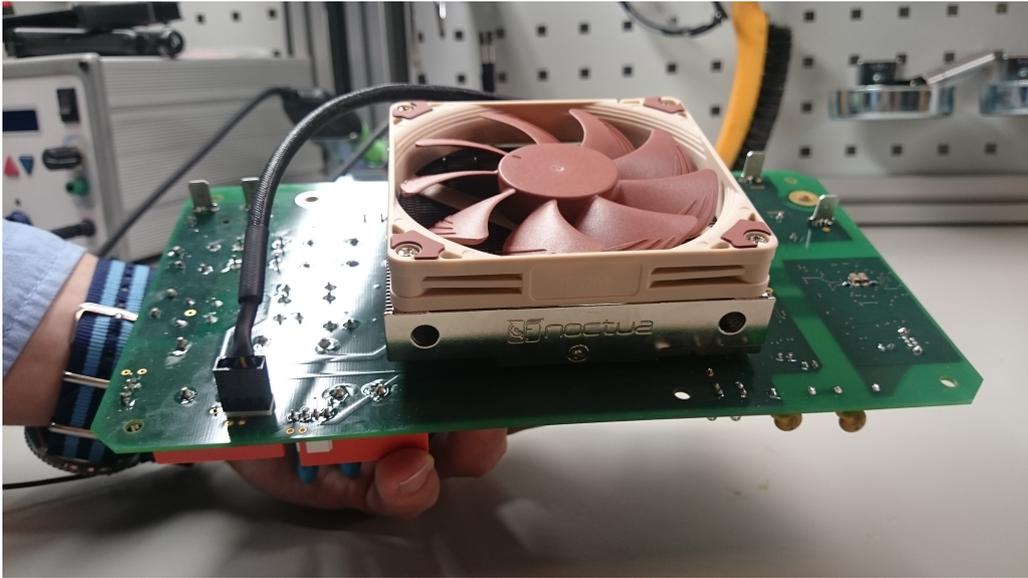


Figure 4.5: Bottom side of the PBA.

## 4.4 Measurements and gathered data

### 4.4.1 Efficiency

The verification process of the switching capabilities is described in section 3.19 and the switching frequency and input voltage are increased accordingly. The final test utilizing a frequency of 1 MHz, 400 V and 1 kW output with an input current of 4.54 A is the most interesting test and the measurement acquired is presented in this section.

The PBA is connected to two power supplies, an electronic load and a desktop computer. The input and output voltages and current can be read directly from the apparatus and the data are presented in table 4.1.

Table 4.1: Testing conditions during the final test

$V_{in}$	229.0 V
$V_{inLV}$	61.0 V
$V_{out}$	400.3 V
$I_{in}$	4.61 A
$I_{inLV}$	0.075 A
$I_{out}$	2.50 A
$D$	0.375

The efficiency can be calculated to 94.5 % given the data presented in the table. Since a DC power supply is used as input instead of the main grid, the efficiency presented is expected to go down by a small amount as there are no losses in the

bulk capacitors due to the absence of the 100 Hz ripple. The losses in the bulk capacitors are calculated to be another 4.7 W. Adding these extra losses to the efficiency calculation gives the final efficiency to drop to 94.1 %. This value is close to the expected 94.4 % efficiency presented in table 3.5.

#### 4.4.2 Switching speeds

A large portion of the total losses are switching losses and some effort has been made in order to investigate and predict these losses in order to design the PCB. The current fall and rise times are difficult to measure because of the design, but the voltage fall and rise times can be measured and compared to what the calculations yields. The times should be  $t_{fv} = 9.5 \text{ ns}$  and  $t_{rv} = 11.7 \text{ ns}$  using (2.36),(2.37), the method used in section 3.5.3 and given the driver configuration. The measured voltage waveforms are presented in figure 4.6 which shows  $V_{VDS}$  for a couple of cycles. A zoom for the edges are shown as well in order to clearly depict the 10 % and 90 % times, which of course are used to find the rise and fall times of the voltage.

Inspection of the figure yields measured rise and fall times of  $t_{fvMeasured} = 49.5 \text{ ns} - 43.2 \text{ ns} = 6.3 \text{ ns}$  and  $t_{rvMeasured} = 59.1 \text{ ns} - 42.4 \text{ ns} = 16.7 \text{ ns}$ . To compare them with the calculated values, the theoretical times are multiplied with 0.8 since the 10% – 90% method was used in the measurements, while the calculations are based on figure 2.10 and the corresponding mathematics.

**Table 4.2:** Measured and expected rise and fall times during switching

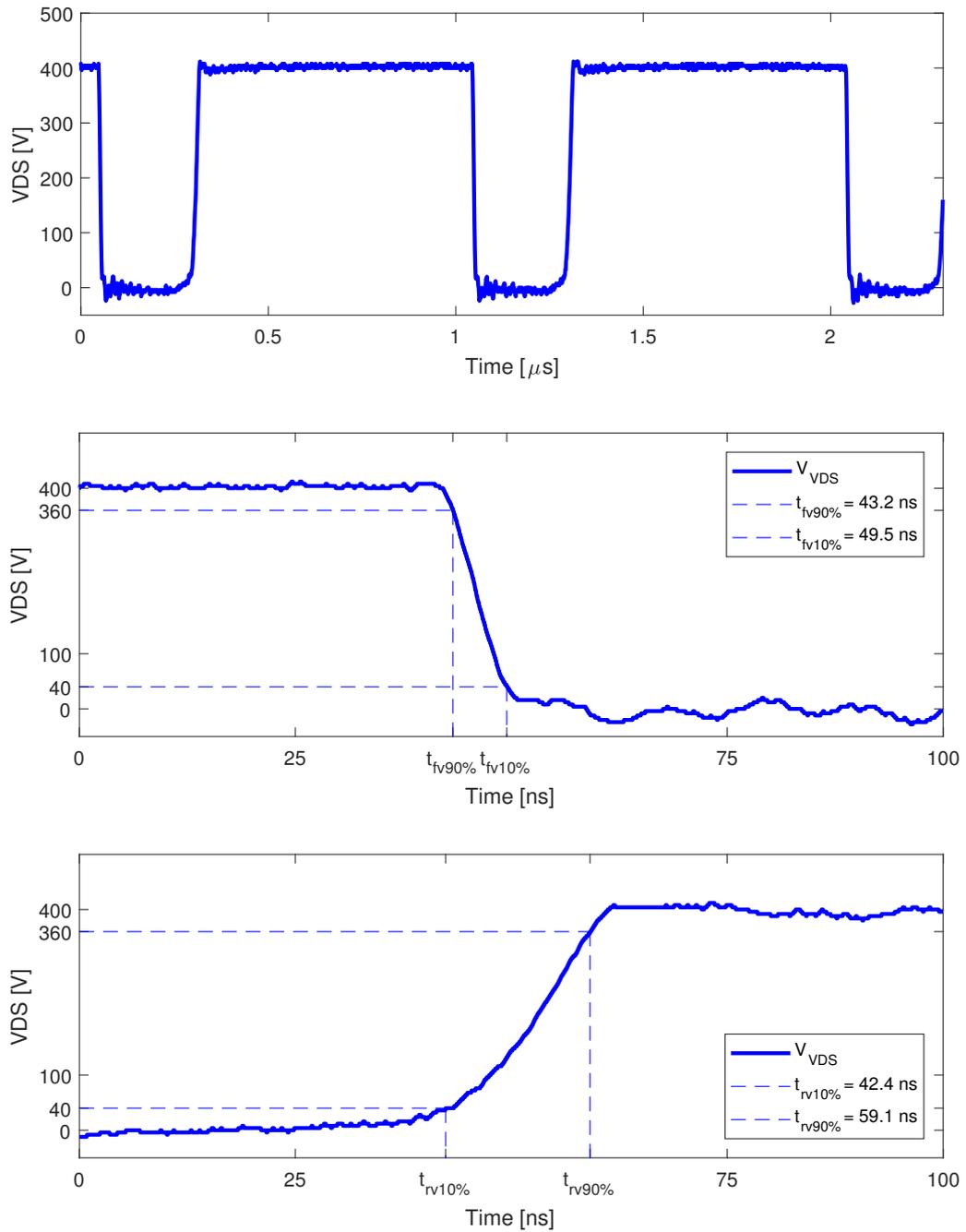
Unit	Measured	Expected (compensated)
$V_{fv}$	6.3 ns	7.6 ns
$V_{rv}$	16.7 ns	9.3 ns

The measured fall time is close to the expected value and deviates by 21 %. The expected result was that the real fall time would, if anything, be larger than calculated values because of the driver output resistances. Data regarding these resistances was given for a low output current, and the real values were therefore suspected to be higher.

The rise time on the other hand deviates by 80 % and is longer than the expected value. Possible explanations are, again, uncertainties regarding the output resistances of the driver.

The switching behaviour is strongly dependent on the voltage across the gate. One more possible explanation for the deviating rise and fall times might be found by investigating the gate voltage waveforms. The waveforms are also interesting in order to investigate gate ringing.

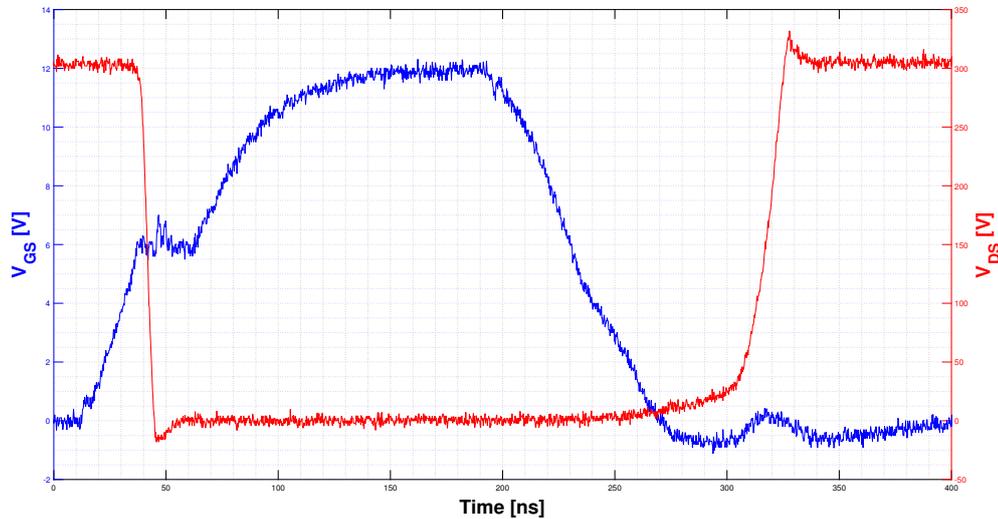
The change in voltage across the gate of one of the MOSFET during one turn-on and turn-off cycle is shown in figure 4.7 together with  $V_{DS}$ . The measurement is



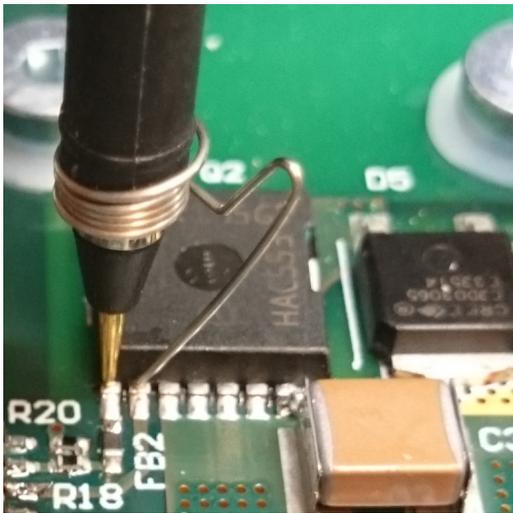
**Figure 4.6:** Boost MOSFET  $V_{DS}$  with zoom on the edges.

done at an output voltage of 300 V because of probe limitations. The measurement was done as close as possible to the MOSFET, with the probe hat off and very short GND-loops using ground springs in order to minimize distortion because of

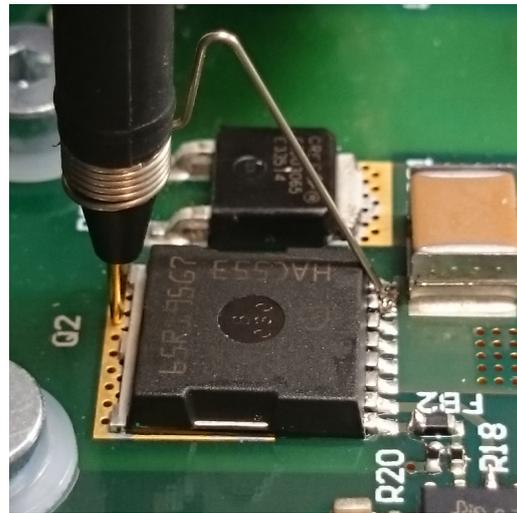
inductance to ground. The probing setup used is shown in figure 4.8 and 4.9 where the probing for measuring  $V_{GS}$  and  $V_{DS}$  are shown respectively.



**Figure 4.7:**  $V_{GS}$  for one turn-on and turn-off event. The PWM is set high at time 12 ns and is then switched off after about 180 ns.



**Figure 4.8:** Probe setup for the  $V_{GS}$  measurements depicted in figure 4.7.



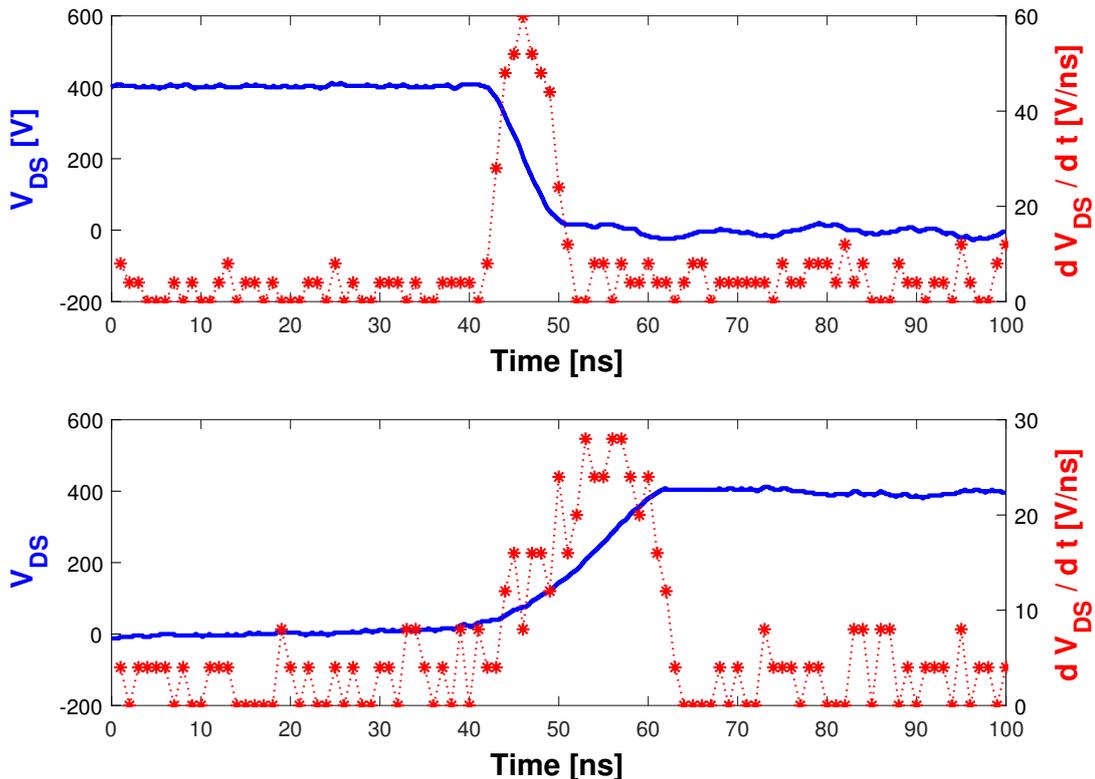
**Figure 4.9:** Probe setup for the  $V_{DS}$  measurements depicted in figure 4.7.

During turn-on, the gate voltage waveform looks like the used model, as figure 2.10. The Miller plateau is clearly visible. The fall time of  $V_{DS}$  does however not correspond to the whole Miller plateau time, this is not a surprise as the  $V_{DS}$  fall time can be divided into distinct times with different fall speeds as described in [1].

The gate voltage during the turn-off does not look like the model and can be the reason why the predictions regarding the rise time of  $V_{DS}$  is off by 80 %. Why reality

deviates from the model is unclear and deemed to be outside the scope of the thesis but can be an interesting topic for another work.

Yet another important aspect of the switching is that the  $dV/dt$  rating is not exceeded. The data points of the slopes presented in figure 4.6 can be analyzed for the purpose of investigating the  $dV/dt$ . The data set consists of 2500 data points which is divided into 100 sections. In each section, the  $dV/dt$  is estimated as the difference between the starting and end voltage of the section, divided by the time step. The acquired data are plotted against the slopes as orange stars in figure 4.10.



**Figure 4.10:** Visualization of  $dV_{DS}/dt$  during both on and off switching.

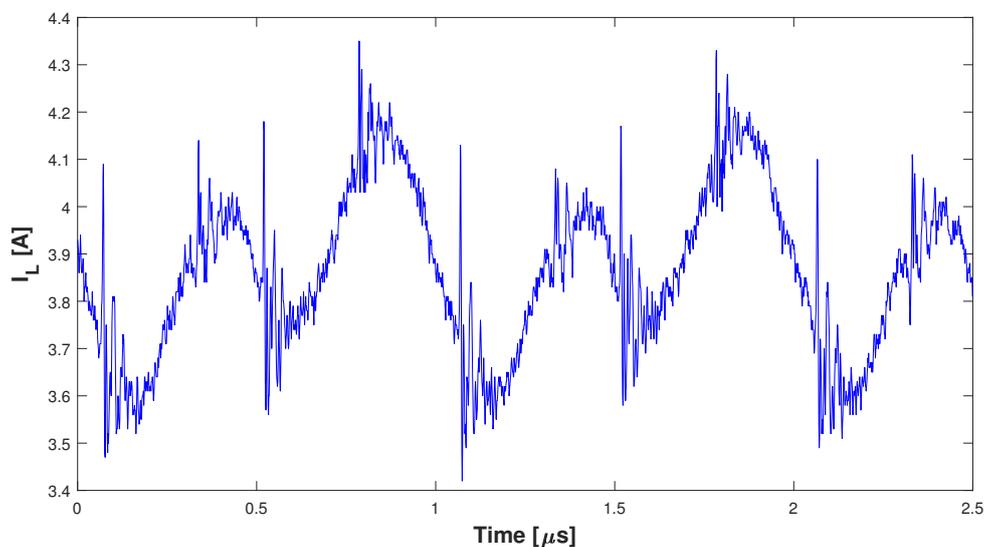
Because of the low resolution of the measured drain source voltage along with too few data points of the set, the results are quite noisy but are still deemed useful for the  $dV/dt$  inspection. Upon studying the figure one quickly realizes that there is room for improving the cross over times and therefore the efficiency since the maximum measured  $dV/dt$  is below 30 V/ns at turn-off while the maximum allowed is 100 V/ns. This can be done by modifying the gate driver circuitry by changing the gate resistance or the gate ferrite. One might also increase the gate driver voltage but this would only shorten the fall time, which already is quick.

Another observation that can be made by inspecting figure 4.6 and figure 4.10 is that there is little to no overvoltage at turn-off. This is not true. Overvoltages, some 30 V at 300 V out, shows up in measurement 4.7 as the slow differential probe

was not used for this measurement. As the faster probe cannot measure 400 V the same measurements cannot be made for the 400 V case.

### 4.4.3 Current measurements to find inductance value

The boost inductors are shown mounted on the PCB in figure 4.4. They are the toroidal inductors in the middle of the PCB, not be be mistaken for the common mode chokes located at the edges of the PCB. Their common current are measured as a voltage at the test point named ISense and is depicted in figure 4.7.

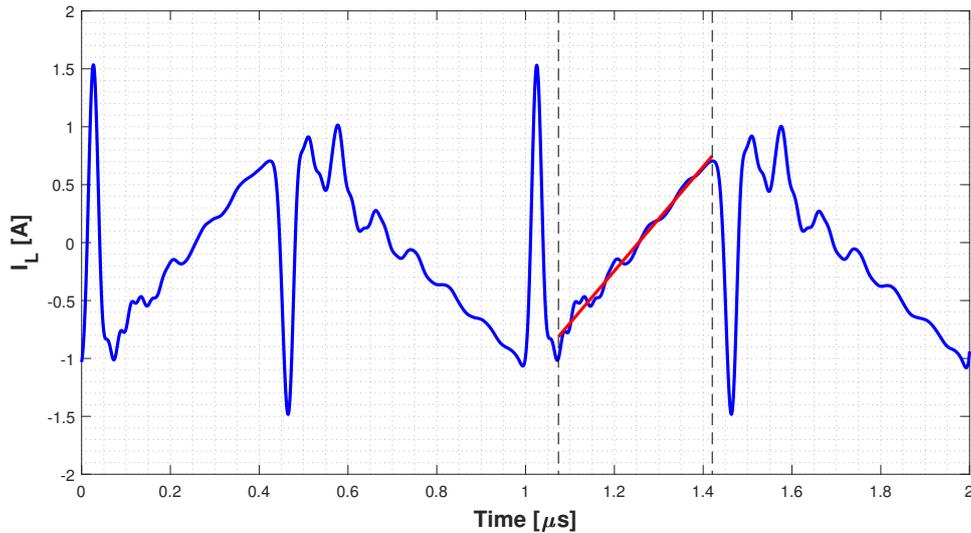


**Figure 4.11:** Current through both boost inductors during 1 MHz switching frequency, measured at ISense test point.

The signal is noisy even though measures to minimize the GND loop of the probe using ground springs are made. The data are intended to be used for boost inductance verification. Processing of this data yields unexpectedly large inductance values of  $\sim 100 \mu\text{H}$ . The measurement is therefore deemed invalid and the probable cause is that the signal from ISense is a filtered signal with a cut off frequency of 2 MHz which is the same as the fundamental frequency of the ripple. The peaks of the inductor current is therefore not truthfully shown.

Since the measurement of the inductor current via the ISense test point does not yield good data, another measurement needs to be conducted. The current can be measured using a Rogowski coil clamped around one leg of an inductor. The coil was positioned as far away from the switches as possible as they generate high  $dV/dt$  which interferes with the measurement [31]. The sensitivity of the Rogowski coils is 20 mV/A and the resulting current in the inductor is depicted in blue in figure 4.12.

The parameters during the test is: Input voltage 232 V, input current 4.5 A, output voltage 412 V. The Rogowski coil does not measure DC, which is why the current is



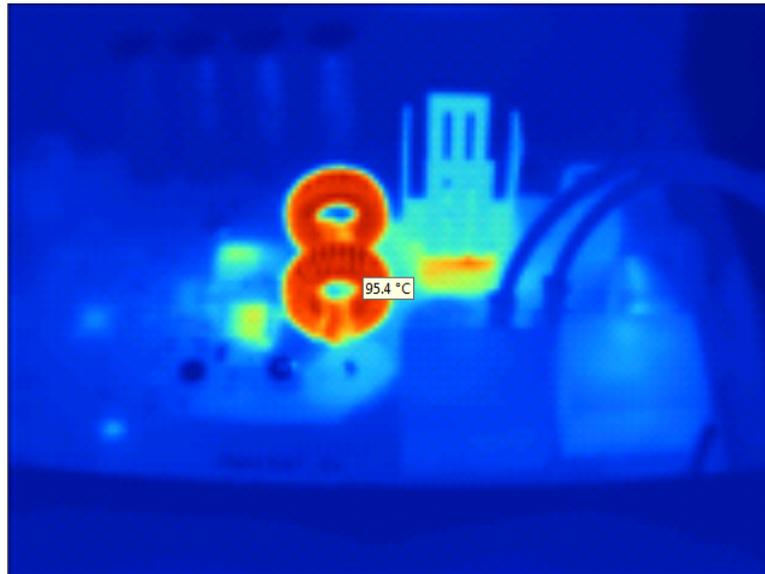
**Figure 4.12:** Current through one inductor during 1 MHz switching frequency, measured using a Rogowski coil.

centered around zero. As shown by the figure the measurement is quite noisy and there are four large spikes at times  $\sim 0, 0.45, 1$  and  $1.45 \mu s$ . These spikes occur at the peak of the expected triangle wave, which is at the same time as the MOSFET switches. The spikes are therefore deemed to be measurement errors. In order to find the slope, which will yield the inductance, a first order approximation using the least square method of the data points between the dashed black lines is made. The resulting slope is shown in red. The slope is  $4.5 \text{ A}/\mu s$  which gives an inductance of  $\frac{232 \text{ V}}{4.5 \text{ A}/\mu s} \approx 52 \mu H$  which deviates from the intended  $35 \mu H$ . The inductance is about 50 % higher than designed value. This was not unexpected given the relatively simple hand calculations based on worst case scenarios, measurement errors and that "off the shelf" industrial manufactured inductors often specifies inductance deviations of 20 %.

#### 4.4.4 Device temperatures under load

The temperatures of the PBA was inspected using a thermal camera. The temperatures settles after about 15 minutes and a thermal image focusing on the inductors are shown in figure 4.13 which was captured after 15 minutes of supplying a 1 kW load.

It was difficult to get a good picture of both the inductors and the switches so a thermal close up of the switches are shown in figure 4.14. This image is also captured after about 15 minutes.



**Figure 4.13:** Thermal image of the PBA during  $K_f = K_v = 10$  with focus on the boost inductors, maximum inductor temperature indicated.

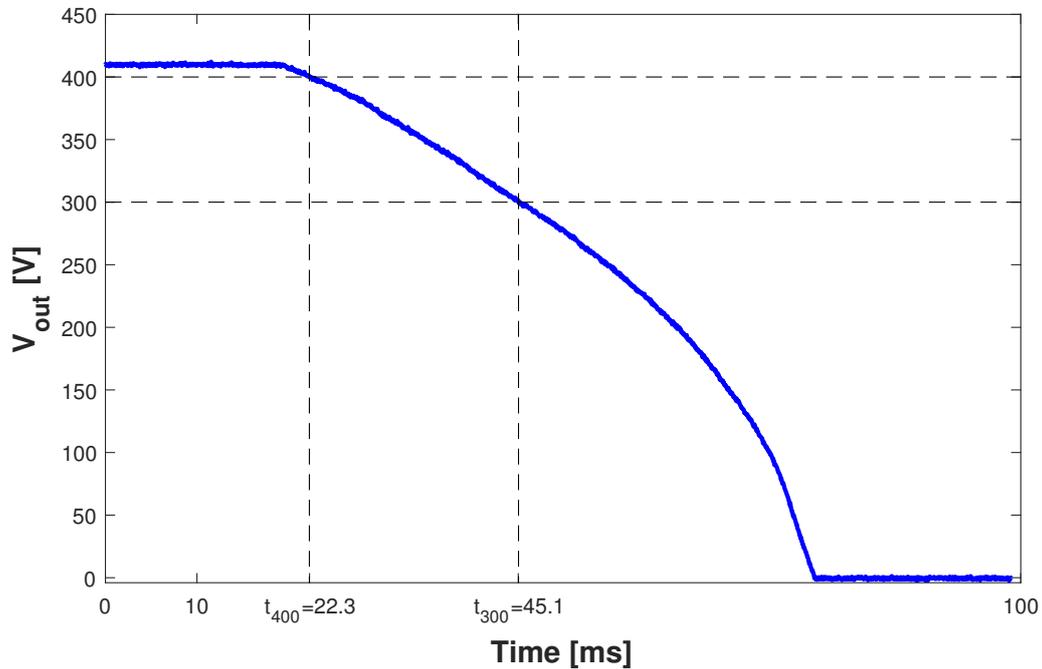


**Figure 4.14:** Thermal close up image of the switches during  $K_f = K_v = 10$ , with maximum transistor casing temperature indicated.

#### 4.4.5 Hold up time

The hold up time is measured by investigating the output voltage of the step-up converter using an oscilloscope. The electronic load connected to the output is set to consume a constant power. To simulate a voltage interruption, the power supply is simply turned off. The fall in output voltage is presented in figure 4.15 where the times corresponding to 400 V and 300 V are indicated. The hold up time is the difference between  $t_{400}$  and  $t_{300}$  and is equal to 22.8 ms, thus greater than the

requirement of 20 ms.



**Figure 4.15:** Measurement of the output voltage at disconnection of the power supply.

## 4.5 Outcomes versus requirements

The final comparison between the specifications of requirements and final results is presented in table 4.3.

**Table 4.3:** Presentation of the specifications and the results of the design process

Requirement	Result	Pass/Fail	Verification method
$f_{sw} = 1$ MHz	1MHz	Pass	Measured
1 kW output power	1 kW	Pass	Measured
96 % efficiency	94.1 %	Fail	Measured calculated
400 VDC output	400 VDC	Pass	Measured
230 VAC input	-	-	Not tested
Generic connectors	Safety banana plugs C14 plug USB mini-B	Pass	Design
Air cooled design	Air cooled	Pass	Design
20 ms hold up time	22.8 ms	Pass	Measured

# 5

## Discussion

This thesis was performed in order to investigate if it was possible to design a high frequency two channel interleaved step-up converter intended for PFC applications. The method used to answer this research question was to make calculations on relevant power components, and to design and build a PCB for physical testing and verification.

The key results of the study is that it is possible to design a device intended for PFC that utilizes a very high switching frequency using commercially available components whilst maintaining a sensible efficiency, even though it was lower than the initial goal.

This was made possible partly because the MOSFETs used were the best found at the time and also because the boost inductors were custom designed. As discussed before, the boost inductors can be made smaller with a higher switching frequency. A volume comparison can be made with a design example from Infineon [8] where they design an inductor for a single channel 1.2 kW PFC with generic input operating at a switching frequency of 100 kHz. The cores chosen for the design example are two toroids stacked together with 61 turns of copper wire. The total iron volume of their inductor can be calculated to 27 cm<sup>3</sup>. Given the data regarding the diameter of copper wire used and the DC resistance, the volume of the copper wire can be calculated to 4.5 cm<sup>3</sup> which means that their total inductor material volume is 31.5 cm<sup>3</sup>. The total material volume for the inductors used in this design is 3 cm<sup>3</sup> which brings the total inductor volume to 6 cm<sup>3</sup>.

The step-up converter with all its peripherals has only been investigated using a DC-power supply as input while driving a resistive load. This puts limitations on the study as the PFC capabilities has not been tested. The behavior of the device whilst supplying different inductive and capacitive loads is also unknown as these measurements has not been made.

The step-up converter did not meet the efficiency specified, however this was expected based on the calculations. It might be possible to reduce the losses in the MOSFETs, which in this device is the main source of the losses, by tinkering with the gate driver resistor, ferrite and voltage in order to decrease the cross over times. This should be possible based on the measured  $dV_{DS}/dt$ .

It should also be possible to decrease the losses in the inductors by constructing and testing the smaller inductors that have been designed but not yet constructed. The inductor size was determined by a designing ripple amplitude of 20 %. The ripple allowed could be higher and inductors corresponding to for example 40 % ripple could be made in order to make them even smaller.

In order to investigate the performance of the circuit as a PFC, the software must be implemented. This is an important aspect that has to be done in order to investigate the circuit when it uses 230 VAC as input. Future relevant implementations also includes making the device able to run on a generic input i.e 110 VAC 60 Hz / 230 VAC 50 Hz.

No EMI measurements has been conducted. The assumption, because of the nature of the circuit operation, is that the circuit will not conform to limiting standards and it is very possible that EMI suppression has to be improved.

Future research regarding the switching wave forms of the MOSFET needs to be pursued in order to understand why the gate voltage and corresponding cross over time at turn-off deviates from the models used.

# 6

## Conclusion

The purpose of this thesis was to build a high frequency dual channel step-up converter intended for PFC applications. The aim was to reach a switching frequency of 1 MHz while maintaining 96 % efficiency supplying a output power of 1 kW at a voltage of 400 V using single phase 230 VAC input. The developed prototype is able to supply 1 kW at a voltage of above 400 V using 1 MHz switching frequency, but the efficiency drops to 94.5 %. The input used during the tests was 230 VDC as the control needs to be implemented before grid operation. During grid operation the efficiency is calculated to drop to 94.1 %. As the  $dV/dt$  measurements indicates that faster switching may be possible, the losses can probably therefore be reduced to try to bring the efficiency closer to the goal. Winding and implementation of the smallest designed inductor saves another calculated 1 W. Implications, given the possibility of higher switching frequency, is that future designs may be built using smaller boost inductors and smaller filters. The consequence of this is probably cheaper filters and boost inductors, and maybe also that the PFC weighs less and takes up less space. Given that PFC are used in conjunction with loads, smaller PFC circuits might by extension lead to less bulky power tools using DC, smaller power supplies etc.

### 6.1 Future work

The device developed is a prototype and some further work is needed before it can be used as a PFC. There are also work to be done tweaking the circuit for higher efficiency and some tests, such as EMI measurements, that are of interest. A small bullet list of future steps regarding future work is therefore presented.

- Tweak the gate resistance and ferrite in order to fully utilize the high  $dv/dt$  rating of the switches and implement the smaller inductors to reduce losses.
- Perform EMI measurements and verify against regulations.
- Design equipment to control the air flow from existing fan in order to cool warm components.
- Finish the software and investigate the PFC performance.



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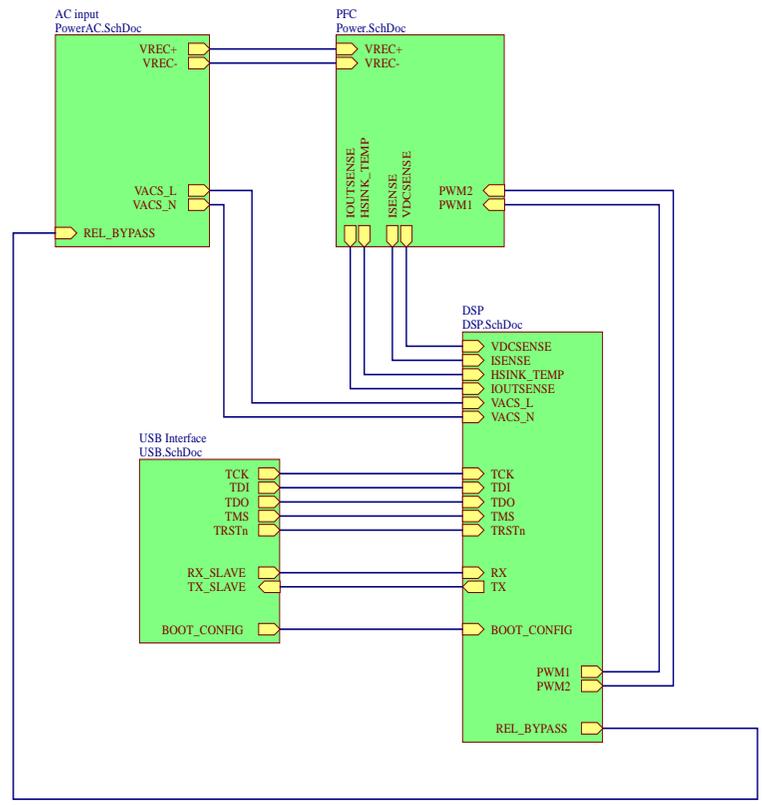
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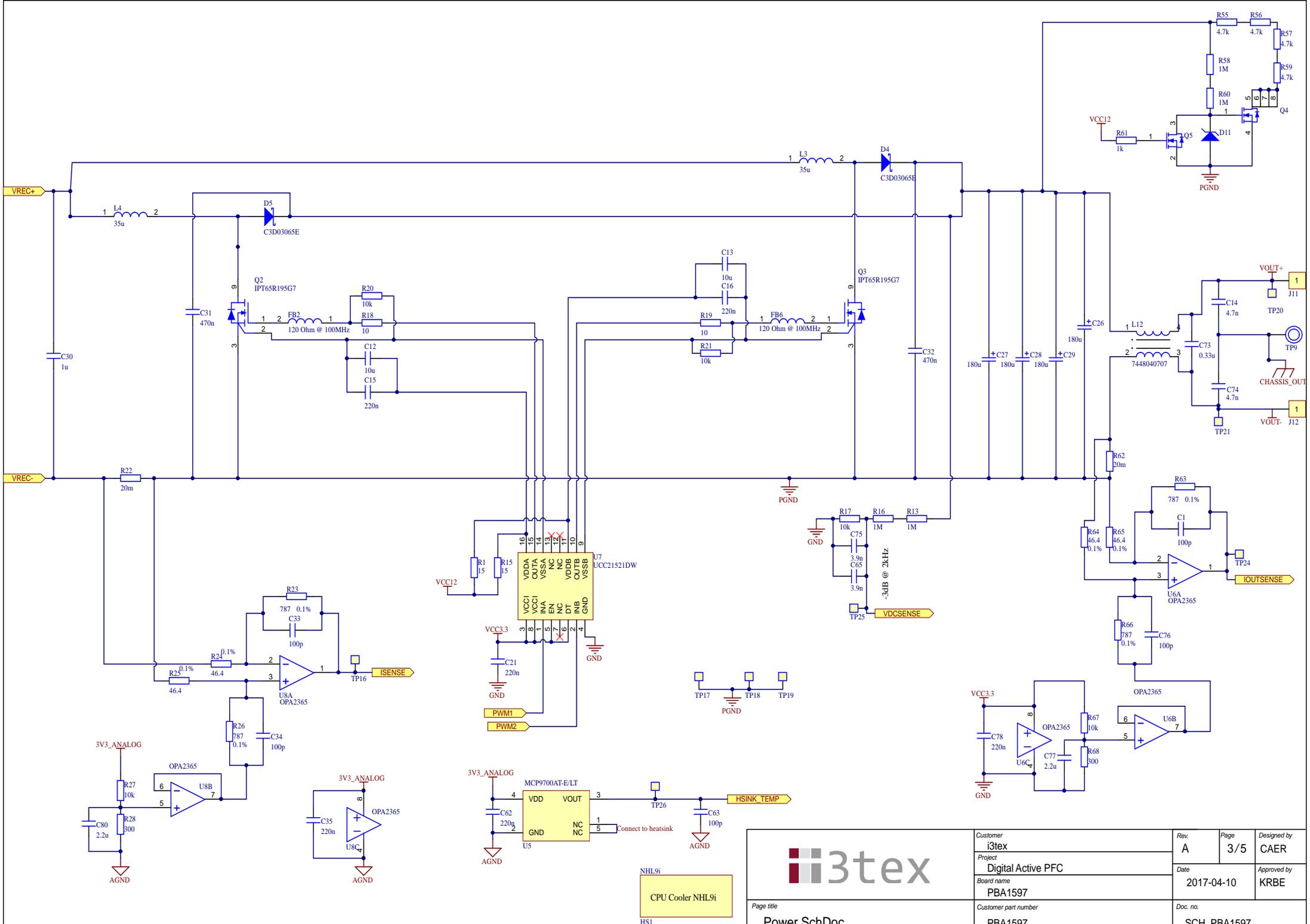
A

# Circuit schematic



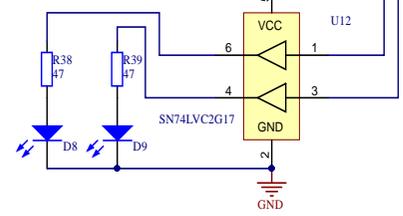
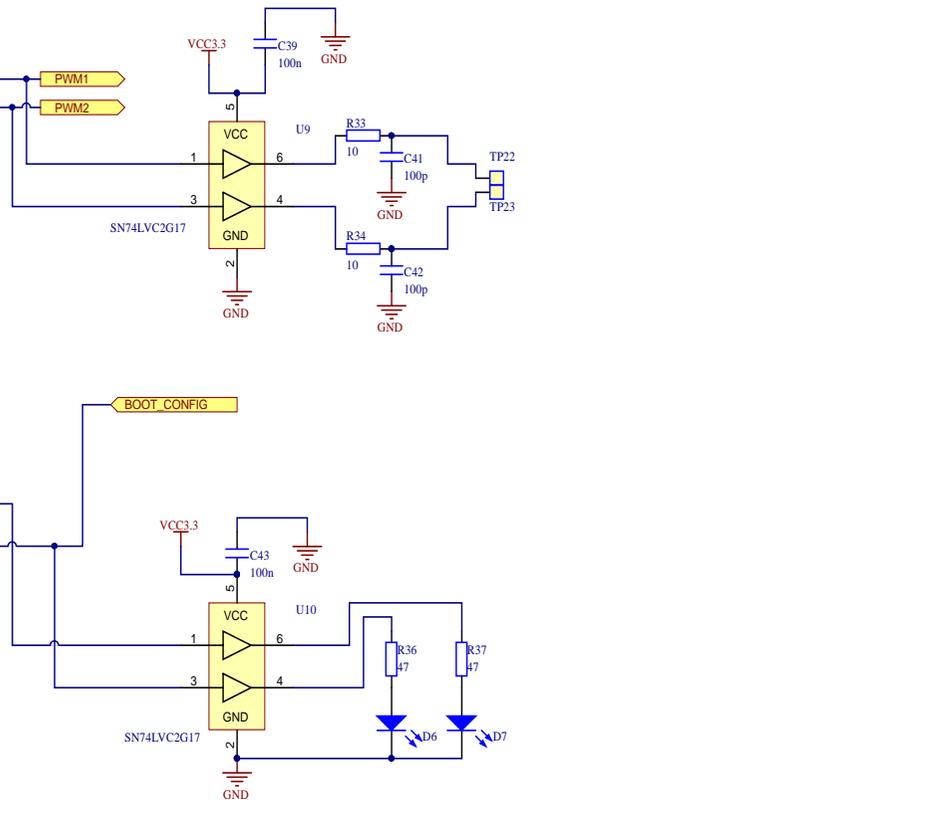
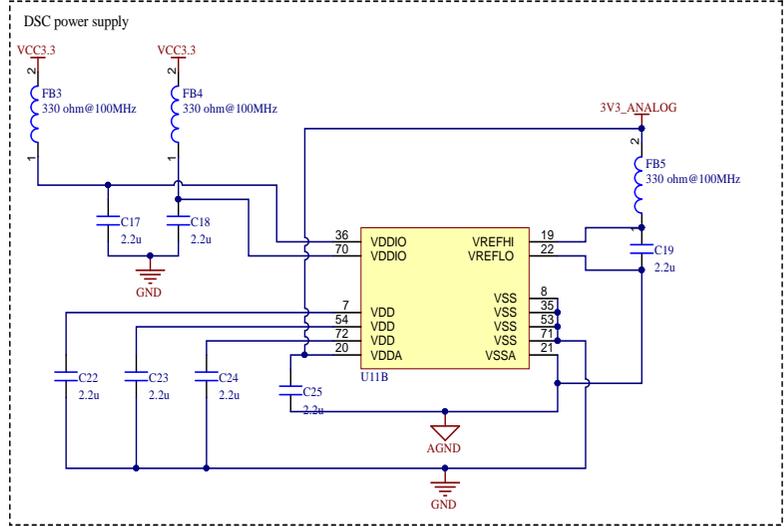
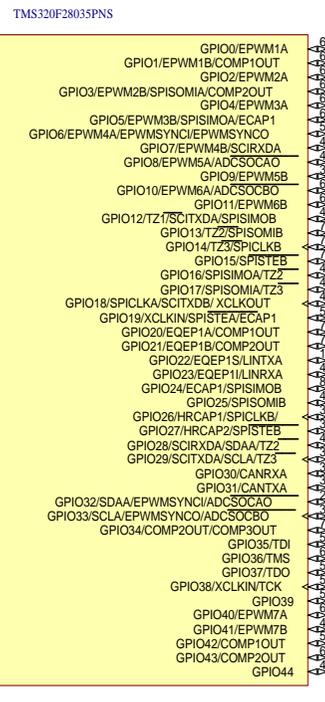
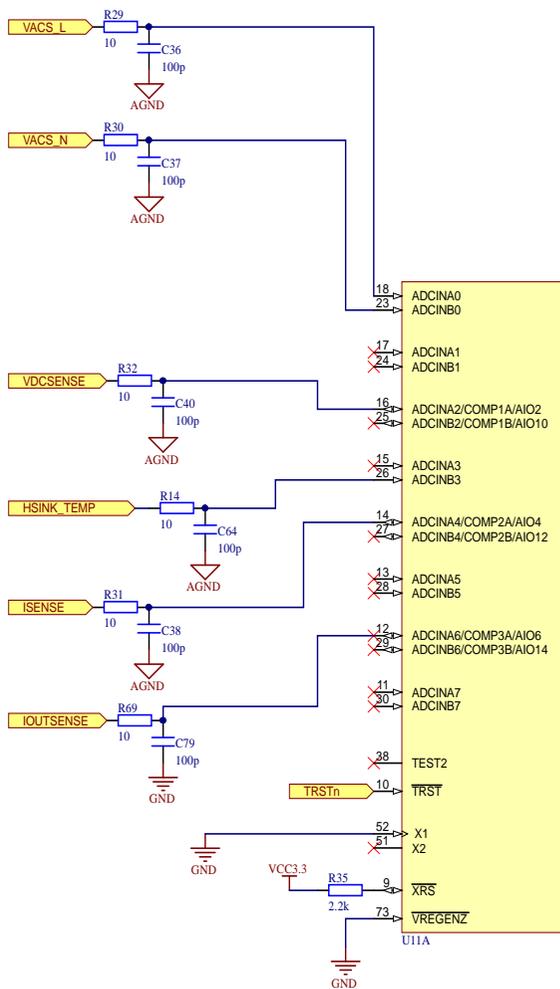
	Customer i3tex	Rev. A	Page 1/5	Designed by CAER
	Project Digital Active PFC	Date 2017-04-10	Approved by KRBE	
	Board name PBA1597	Customer part number PBA1597	Doc. no. SCH_PBA1597	
Page title MainOverview.SchDoc				



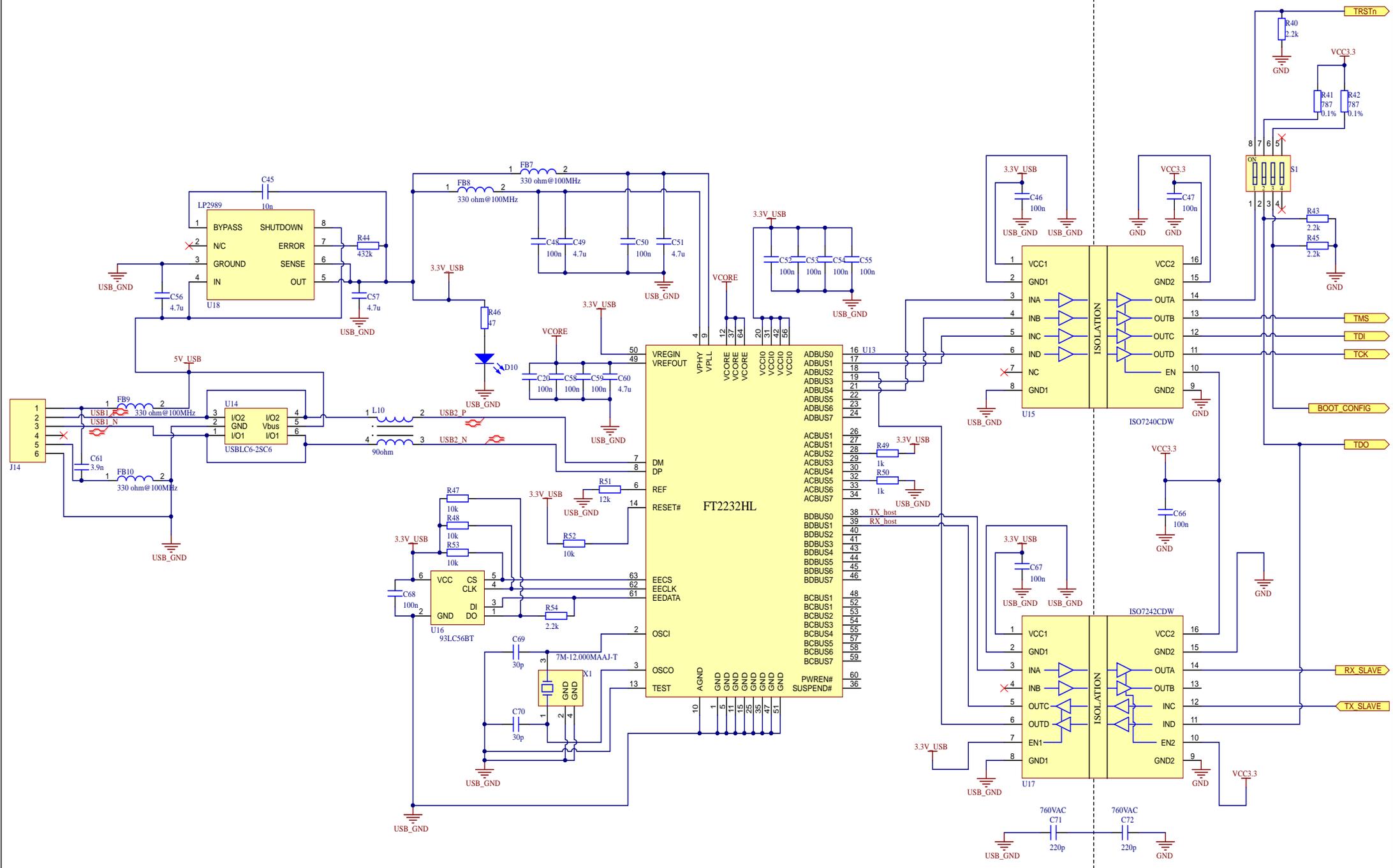


	Customer	i3tex	Rev.	A	Page	3/5	Designed by	CAER
	Project	Digital Active PFC	Date	2017-04-10	Approved by	KRBE		
Board name	PBA1597	Customer part number	PBA1597	Doc. no.	SCH_PBA1597			
Page title	Power.SchDoc							

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	Customer i3tex	Rev. A	Page 4/5	Designed by CAER
	Project Digital Active PFC	Date 2017-04-10	Approved by KRBE	
Board name PBA1597	Customer part number PBA1597	Doc. no. SCH_PBA1597		
Page title DSP.SchDoc				

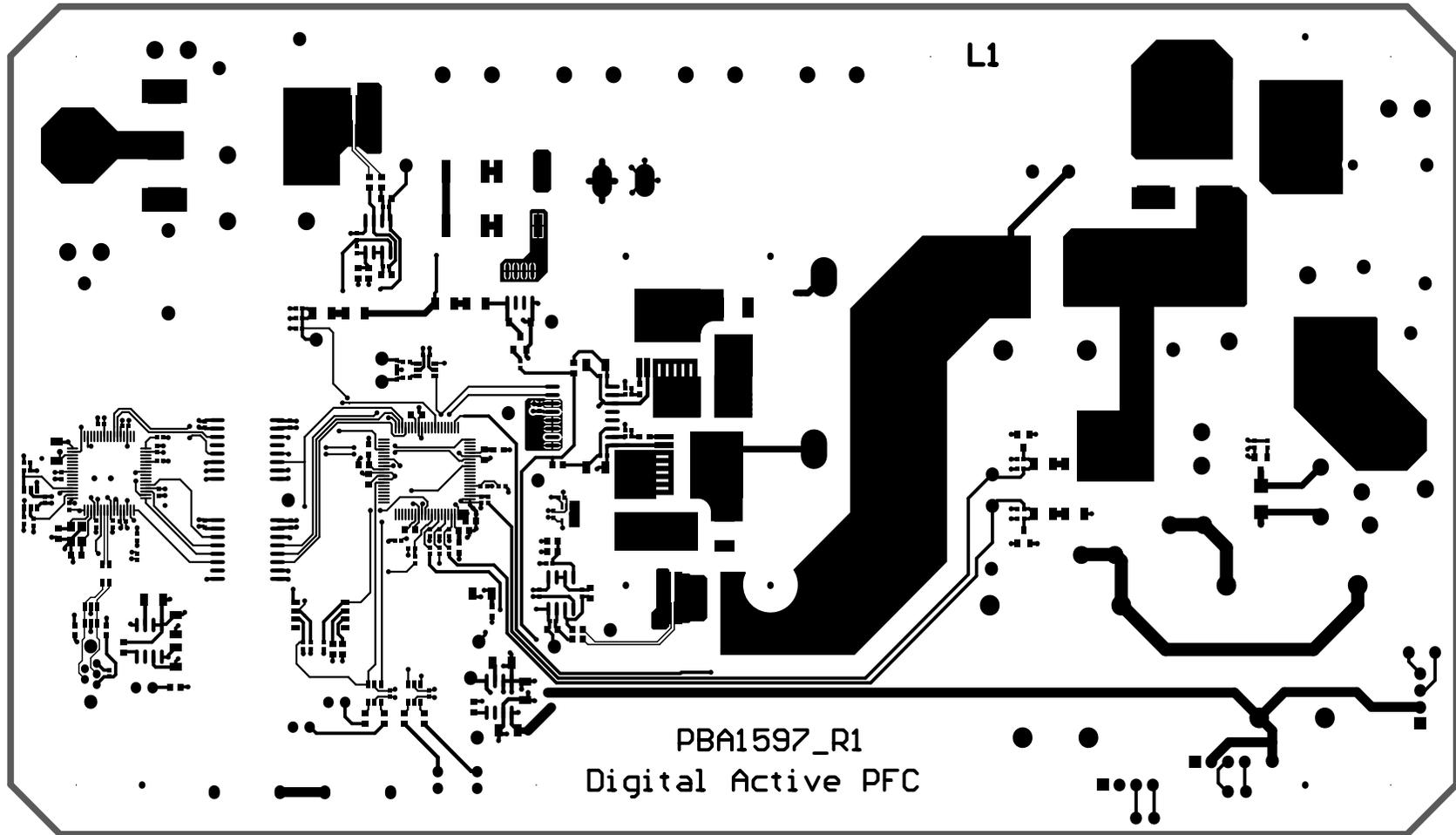


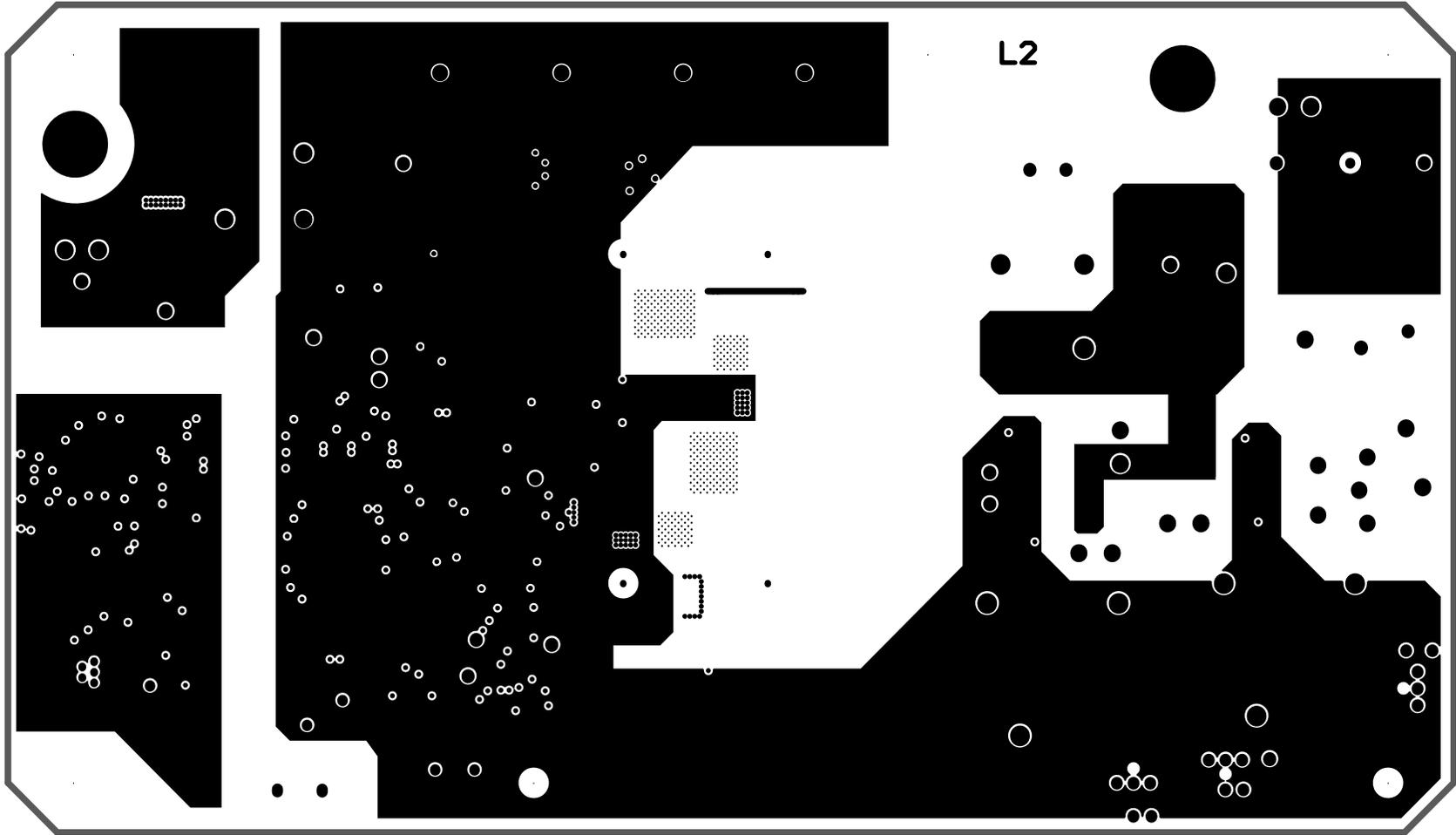
	Customer <b>i3tex</b>	Rev. <b>A</b>	Page <b>5/5</b>	Designed by <b>CAER</b>
	Project <b>Digital Active PFC</b>	Date <b>2017-04-10</b>	Approved by <b>KRBE</b>	
Board name <b>PBA1597</b>	Customer part number <b>PBA1597</b>	Doc. no. <b>SCH_PBA1597</b>		
Page title <b>USB.SchDoc</b>				

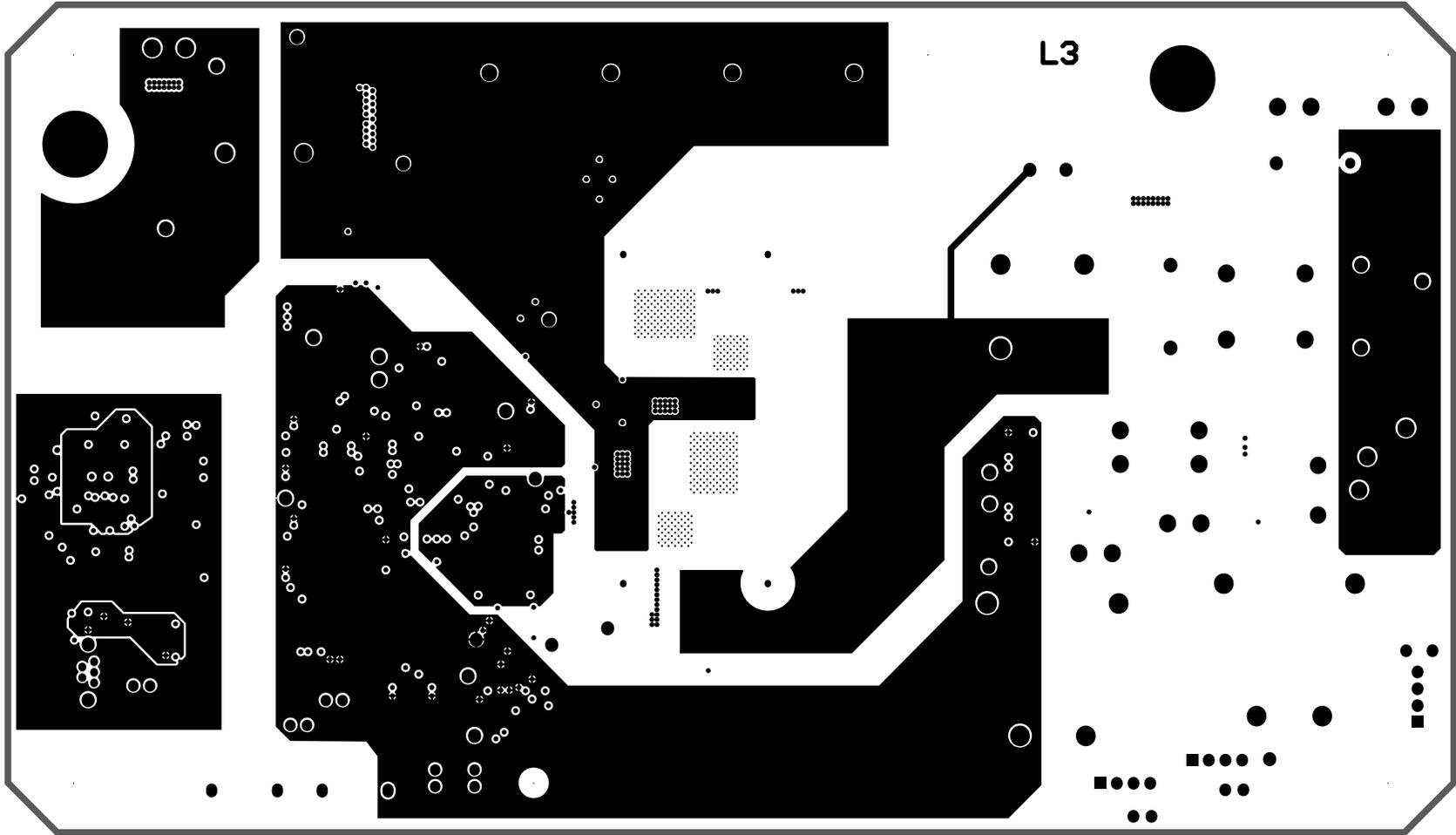
# B

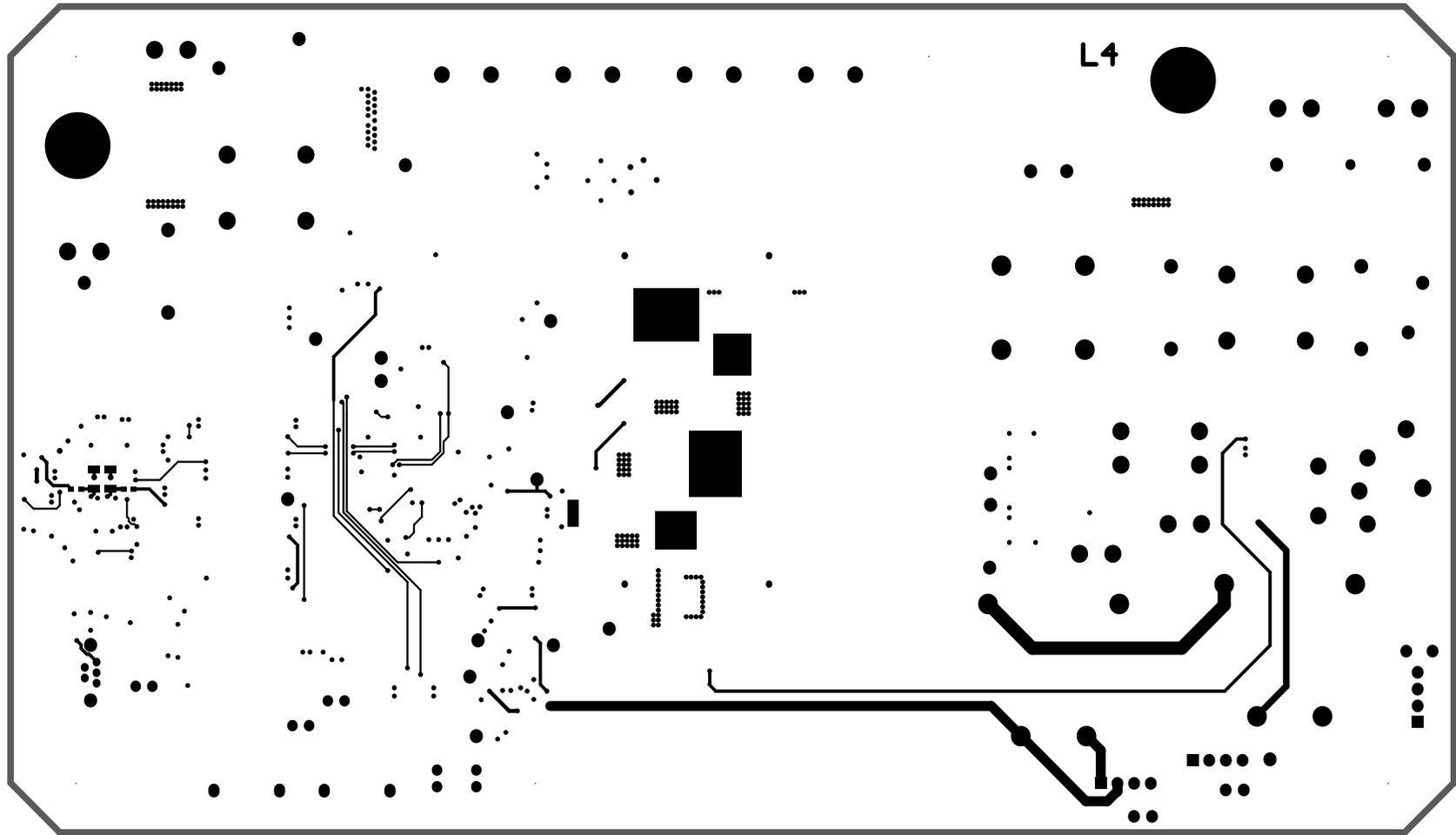
## PCB layout

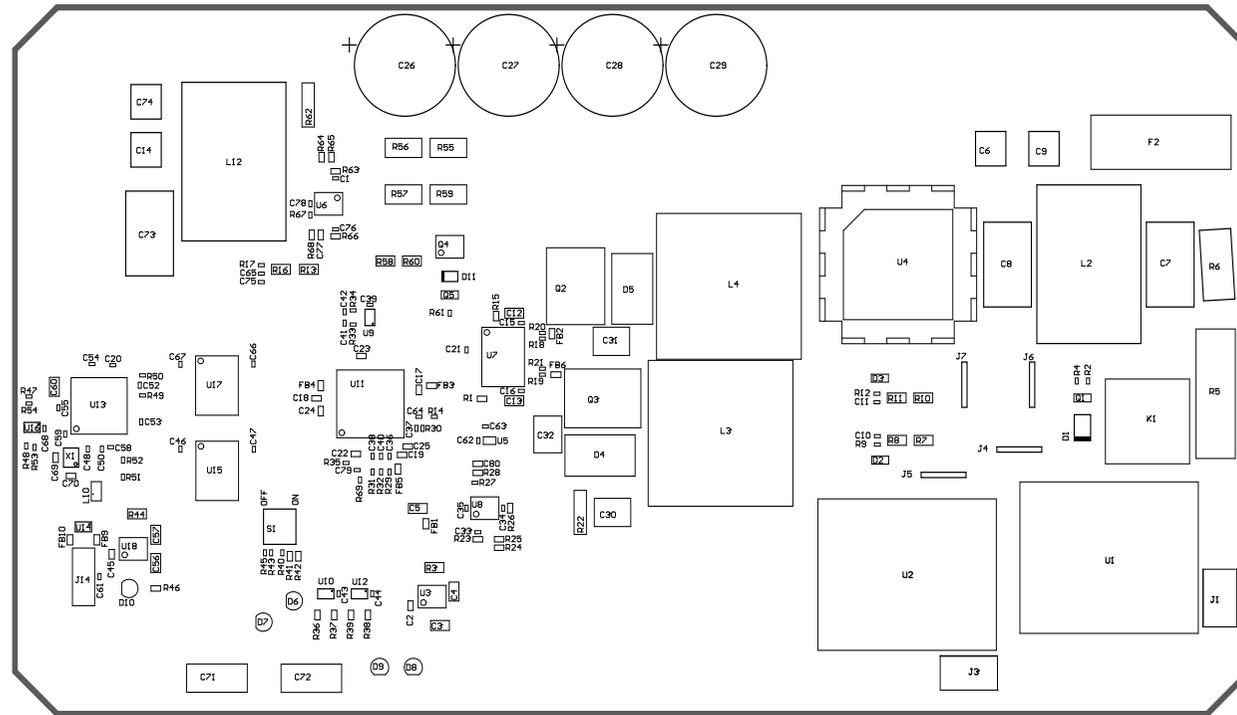
The four PCB layers are shown from top to bottom along with the assembly drawings.











<h1>i3tex</h1>	Customer i3tex	Rev. A	Designed by CAER
	Project Digital Active PFC	Date 2017-04-10	Approved by KRBE
Printed 2017-05-11 08:51:04	Board name PBA1597	Customer part number PBA1597	Doc. no. AD_PBA1597
Title Top Assembly Drawing	SCALE: 1,00		



<h1>i3tex</h1>	<i>Customer</i> i3tex	<i>Rev.</i> A	<i>Designed by</i> CAER
	<i>Project</i> Digital Active PFC	<i>Date</i> 2017-04-10	<i>Approved by</i> KRBE
	<i>Board name</i> PBA1597	<i>Customer part number</i> PBA1597	<i>Doc. no.</i> AD_PBA1597
<i>Printed</i> 2017-05-11 08:51:05	<i>SCALE:</i> 1,00		
<i>Title</i> Bottom Assembly Drawing			



# C

## Bill of Materials

# Bill of materials



Project: Digital Active PFC  
 PBA: PBA1597  
 Doc. Number: BOM\_PBA1597  
 Revision: A  
 Date: 2017-04-24

#	Change	Designator	Quantity	Description	Value	Ratings				PackageReference	Manufacturer	Part Number	Mounting	Supplier 1	Supplier Part Number 1	Note	
						Tolerance	Voltage	Dielectric	Temperature range								
1	Y	C1, C33, C34, C36, C37, C38, C40, C41,	13		100p	5%	16V	COG, NP0		0402			SMD				
2	Y	C2, C45	2		10n	5%	16V	COG, NP0		0603			SMD				
3	Y	C3, C4, C5, C49, C51, C56, C57, C60	8		4.7u	10%	25V	X7R		1206			SMD				
4	Y	C6, C9, C14, C74	4	Cap, safety, Y2, ceramic, SMD, 2220(5/750)	4.7n	10%	250VAC	X7R	2220(5/750)		Murata	GA355DR7GF42KW0	SMD	Digi-key	490-3482-1-ND		
5	Y	C7, C8, C73	3	Film capacitor, metallized polypropylene, X2,	0.33u	10%	310VAC	Metallized			Würth	890334024003	THT	Digi-key	732-5839-ND		
6	Y	C10, C11, C61, C65, C75	5	CAP CER 3900PF 50V X7R 0402	3.9n	10%	25V	X7R	0402				SMD				
7	Y	C12, C13	2		10u	10%	25V	X7R	1206				SMD				
8	Y	C15, C16, C21, C35, C62, C78	6		220n	10%	16V	X7R	0402				SMD				
9	Y	C17, C18, C19, C22, C23, C24, C25, C77,	9		2.2u	10%	10V	X7R	0603				SMD				
10	Y	C20, C39, C43, C44, C46, C47, C48, C50,	17		100n	10%	16V	X7R	0402				SMD				
11	Y	C26, C27, C28, C29	4	Electrolytic cap, 180uF, 450V, diam 18mm,	180u	20%	450V	Aluminium			Radial, 7.5mm	Nichicon	UCP2W181MHD	THT	Digi-key	493-13663-ND	
12	Y	C30	1	Cap, ceramic, high voltage, X7T, 630V, stacked	1u	20%	630V	X7T	2220(5/650)		TDK	CKG57NX7T2J105M50	SMD	Digi-Key	445-7110-1-ND		
13	Y	C31, C32	2	Cap, ceramic, high voltage, X7T, 630V	470n	20%	630V	X7T	2220(5/650)		TDK	CKG57KX7T2J474M33	SMD	Digi-Key	445-7104-1-ND		
14	Y	C68, C70	2	CAP CER 30PF 50V NP0 0603	30p	5%	25V	COG, NP0	0603				SMD				
15	Y	C71, C72	2	Ceramic disc capacitor, 220pF, X760	220p	10%	760VAC	Y5S			Radial, Disc	Vishay	VY1221K31YSS063V0	THT	Digi-key	8C2370-ND	
16	Y	D1	1	Schottky Diode, 40V, 3A, SMA, SMD					SMA		On Semiconductor	MBRA340T3G	SMD	Digi-Key	MBRA340T3GOSTR-ND		
17	Y	D2, D3	2	Schottky Diode, dual-in-line , 200mA, 30V,	BAT54S				SOT-23		Fairchild	BAT54S	SMD	Digi-key	BAT54SFCST-ND		
18	Y	D4, D5	2	DIODE SCHOTTKY 650V 3A TO252-2	C3D03065E				TO-252-2_VIAS		CREE	C3D03065E	SMD	Digi-Key	C3D03065E-ND		
19	Y	D6, D7, D8, D9, D10	5	LED 3mm	3mm				3mm			3mm	THT				
20	Y	D11	1	Zener diode, 10V, 0.5W	MMSZ5240B				SOD-123		Fairchild	MMSZ5240B	SMD	Digi-key	MMSZ5240BFCST-ND		
21	Y	F2	1	FUSE BLOK CARTRIDGE 250V 10A PCB							Littelfuse Inc.	65600001009	THT	Digi-Key	WK6245-ND		
22	Y	FB1, FB3, FB4, FB5, FB7, FB8, FB9, FB10	8	Ferrite bead, 330 ohm@100MHz, 500mA,	330				0603		Murata	BLM18EG3311N1D	SMD	Digi-key	490-5913-1-ND		
23	Y	FB2, FB6	2	Ferrite bead inductor	120 Ohm @				0603		Murata	BLM18KG121TH1D	SMD	Digi-Key	490-13261-1-ND		
24	Y	HS1	1	CPU cooler NHL9I							NOCTUA	NHL9I					
25	Y	J1, J2, J3	3	Standard 4-pin processor fan connector							Molex	47053-1000	THT	Digi-Key	WM4330-ND		
26	Y	J4, J5, J6, J7, J9, J10, J11, J12	8	Tab, FASTON, 6.35x0.81mm, with solder	1217861-1				Custom		TE	1217861-1	THT	Digi-key	A100452CT-ND		
27	Y	J14	1	USB mini type B, through-hole, vertical	651005136421				Custom			651005136421	THT	Farnell	1841175		
28	Y	K1	1	RELAY GEN PURPOSE SPST 10A 12V	PB134012						TE Connectivity Potter	PB134012	THT	Digi-Key	PB768-ND		
29	Y	L2, L12	2	n 7mH @ 10kHz 2 Line Common Mode Choke	7448040707				Custom		Würth	7448040707	THT	Digi-key	732-5589-ND		
30	Y	L3, L4	2	2PHILPFC Inductor 1, Master thesis Digital	35u							2PHILPFC_INDUCTO					
31	Y	L10	1	SMD common mode choke	90ohm				Dual 1206		Würth	744232090	SMD	Digi-Key	732-1469-1-ND		
32	Y	Q1	1	BJT NPN 80V 0.5A SOT-23				-55 to +150C	SOT23		Fairchild	MMBTA06	SMD	Digi-key	MMBTA06FCST-ND		
33	Y	Q2, Q3	2	MOSFET N-channel, 650V, 14 A 195mOhm	IP1T65R195G7			-55 - +150	TOLL		Infineon	IP1T65R195G7	SMD	Mouser	726-IP1T65R195G7XTMA1	C7 CoolMos Gold edition	
34	Y	Q4	1	MOSFET N-channel, 600V, 250mA	STS1NK60Z			-55 to 150	SOIC-8		ST	STS1NK60Z	SMD	Digi-key	497-12798-1-ND		
35	Y	Q5	1	MOSFET N-channel, 60V, 115mA, 1.7ohm	2N7002			-55 to 150 °C	SOT-23		Fairchild	2N7002	SMD	Digi-Key	2N7002NTR-ND		
36	Y	R1, R15	2	Resistor	15	1%	50V		0603				SMD				
37	Y	R2, R49, R50, R61	4	Thick film, 1 kohm, 50 V, 0402, 62.5 mW, ± 1%	1k	1%	50V		0402				SMD				
38	Y	R3, R7, R8, R10, R11, R44	6	Resistor	432k	1%	500V		1206				SMD				
39	Y	R4, R17, R20, R21, R27, R47, R48, R52,	10	Resistor	10k	1%	50V		0402				SMD				
40	Y	R5	1		SL22 50004	±20%			Disc 23x7mm		Ametherm		THT	Digi-key	570-1051-ND		
41	Y	R6	1	Metal Oxide Varistor (MOV), disc type, 12mm	B72210S0271K10						TDK	B72210S0271K101	THT	Digi-Key	495-3786-ND		
42	Y	R9, R12	2	Resistor	7.15k	1%	50V		0402				SMD				
43	Y	R13, R16, R58, R60	4	Resistor	1M	1%	500V		1206				SMD				
44	Y	R14, R18, R19, R29, R30, R31, R32, R33,	10	Resistor	10	1%	50V		0402				SMD				
45	Y	R22, R62	2	Current sense resistor, 2pin, 0830 (2075), 2W,	20m	1%			0830 (2075)		Susumu	RL750WT-R020-F	SMD	Digi-key	RL75WT.02FCST-ND		
46	Y	R23, R26, R41, R42, R63, R66	6	Resistor	787	0.1%	25V		0603				SMD				
47	Y	R24, R25, R64, R65	4	Resistor	46.4	0.1%	25V		0603				SMD				
48	Y	R28, R68	2	Resistor	300	1%	25V		0603				SMD				
49	Y	R35, R40, R43, R45, R54	5	Resistor	2.2k	1%	50V		0402				SMD				
50	Y	R36, R37, R38, R39, R46	5	Resistor	47	1%	25V		0603				SMD				
51	Y	R51	1	Resistor	12k	0.1%	25V		0402				SMD				
52	Y	R55, R56, R57, R59	4	Resistor	4.7k	5%	250V		2512				SMD				
53	Y	S1	1	Switch, DIP, 4 positions, 1.27mm pitch, top	218-4LPST						CTS	218-4LPST	SMD	Digi-Key	CT2184LPST-ND		
54	Y	TP1, TP2, TP3, TP4, TP5, TP7, TP8, TP10,	22	Test pin, 1.2mm THT, 2mm pad	TP							TP	THT				
55	Y	TP6, TP9	2	5mm, Test Point	5mmTPRing							5mmTPRing	THT				
56	Y	U1	1	AC/DC converter, 12V, 5W	VTX-214-005-112					VTX-214-4PIN		Vigortronix	VTX-214-005-112	THT	Farnell	2401044	Alternative part: Myrra 47154

57	Y	U2	1	AC/DC converter, 5V, 5W	VTX-214-005-105				VTX-214-4PIN	Vigortronix	VTX-214-005-105	THT	Farnell	2401040	
58	Y	U3, U18	2	Lin reg. for ceramic, 3.3V, 500mA	LP2989				SOIC-8N	Texas Instruments	LP2989	SMD	Digi-Key	LP2989IMX-3.3/NOPBCT-ND	
59	Y	U4	1	RECT BRIDGE GPP 1000V 10A MP8	1000V, 10A				MP-8	COMCHIP	MP1010G-G	THT	Digi-Key	841-1377-ND	
60	Y	U5	1	Linear active thermistor	MCP9700AT-E/LT			-40°C to 125°C	SC70-5	Microchip	MCP9700AT-E/LT	SMD	Digi-Key	MCP9700AT-E/LTCT-ND	
61	Y	U6, U8	2	50MHz, Low-Noise Single-Supply Rail-to-Rail	OPA2365				SOIC-8	Texas Instruments	OPA2365	SMD	Digi-Key	296-20801-ND	
62	Y	U7	1	OPTOISO 5.7KV GATE DRVR 16SOIC	UCC21521DW			-40°C ~ 125°C	SIOC16W	Texas Instruments	UCC21521DW	SMD	Mouser	595-UCC21521DW	
63	Y	U9, U10, U12	3	SN74LVC2G17 Dual Schmitt-Triggeer Buffer,	SN74LVC2G17			40°C ~ 125°C (TA)	SN74LVC2G17	Texas Instruments	SN74LVC2G17	SMD	Digi-Key	296-13012-1-ND	
64	Y	U11	1	MCU, C2000 Piccolo, 60MHz, 3V3, with CLA	TMS320F28035P				LQFP-80	TI	TMS320F28035PNS	SMD	Digi-Key	296-32763-ND	
65	Y	U13	1	IC USB HS DUAL UART/FIFO 64-LQFP	FT232HL			-40°C ~ 85°C	LQFP64	FTDI	FT232HL	SMD	Digi-Key	768-1024-1-ND	
66	Y	U14	1	ESD protection, USB 2.0 compatible, 2 data-	USBLC6-2SC6			-40°C to 125°C	SOT-23-6	STMicroelectronics	USBLC6-2SC6	SMD	Digi-Key	497-5235-1-ND	
67	Y	U15	1	DGTL ISO 2.5KV GEN PURP 16SOIC	ISO7240CDW			-40°C ~ 125°C	SOIC-16-W	Texas Instruments	ISO7240CDW	SMD	Digi-Key	296-22628-5-ND	
68	Y	U16	1	2K Microwire Compatible Serial EEPROM	93LC56BT			-40°C ~ 85°C	SOT23-6	Microchip	93LC56BT	SMD	Digi-Key	93LC56BT-I/OTCT-ND	
69	Y	U17	1	DGTL ISO 2.5KV GEN PURP 16SOIC	ISO7242CDW			-40°C ~ 125°C	SIOC-16-W	Texas Instruments	ISO7242CDW	SMD	Digi-Key	296-22966-5-ND	
70	Y	X1	1	CRYSTAL 12.0000MHZ 18PF SMD	7M-12.000MAAJ-					TXC Corporation	7M-12.000MAAJ-T	SMD	Digi-Key	887-1121-1-ND	
			<b>Total quantity</b>	239											

Change	
X	Changed in this revision
Y	Added in this revision
Z	Deleted in this revision

Revision History		
Rev	Date/Sign	Changes
A	2017-04-24/MAAL	First release of PBA1597 R1A



**Bill of Material**

Project Name: Digital Active PFC  
 Document Name: BOM-DEV1406  
 Date: 2017-04-20  
 Rev: PA1

Changes	POS	Amount	Article no.	Description	Manufacturing no	Manufacturer	Distributor	Distributor no	Note
Y	1	1	PBA1597_R1A	Main board		3texas			
Y	2	1		Enclosure	RM2095L	Hammond	Digi-Key	HM1101-ND	
Y	3	1		Flush mounted C14	6162.0058	Schurter	Elfa	143-49-923	
Y	4	1		Thermal pad	HF300P-0.0015-00-4/4	Bergquist	Farnell	8783683	
Y	5	1		4 mm banana safety jack, black	CT2238-0	Cal Test Electronics	Digi-Key	BKCT2238-0-ND	
Y	6	1		4 mm banana safety jack, red	CT2238-2	Cal Test Electronics	Digi-Key	BKCT2238-2-ND	
Y	7	12		FASTON female crimp connector	3-350819-2	TE Connectivity AMP	Digi-Key	A27824CT-ND	Order a few more for spare and verification
Y	8	1		Mains cable, Schuko - C13	SP-230-06-S	Maxxtro	Elfa	143-52-591	Order one extra for verification
Y	9	4		Bumper	SJ-5514 (BLACK)	3M	Digi-Key	SJ5514-0-ND	
Y	10	1		Litz wire	CLI 200/60	Block	Elfa	155-16-547	For inductor manufacturing
Y	11	2		Inductor core, Sendust HF	-	Micrometals	Micrometals		Part number TBD
Y	12	6		Slot screw, M3, 60 mm	BN 330SLOT 4,8 M3X60MM	Bossard	Elfa	110-76-331	PCB fastening and support
Y	13	15		Nut, M3	M6MS M3 / CLL629 MUTTER A4	Bossard	Elfa	148-00-081	
Y	14	32		Plain washer, plastic, 3,2 mm	003030500001	Richco	Elfa	148-49-246	
Y	15	4		Torx screw, M3, 8 mm	BN 15857 M3X8MM	Bossard	Elfa	148-42-391	Heat sink fastening
Y	16	1		Fuse, glass 5x20 mm, 6,3 A, 250 V	0034.1524	Schurter	Digi-Key	486-1241-ND	
Y	17	3		Torx screw, M3, 16 mm	BN 4851 M3X16MM	Bossard	Elfa	148-87-224	Rectifier heat sink and C14 connector fastening
Y	18	1		Bridge rectifier heat sink	6222BG	Aavid Thermalloy	Digi-Key	6222BG-ND	
Y	19	1		Screw, M2.5, 10 mm					Fuse holder fastening
Y	20	1		Nut, M2.5					Fuse holder fastening

NA	Not Available	Rev	Date/Signature	Change
NM	Not Mounted	PA1	2017-04-11/MAAL	First release
X	Changed in this revision			
Y	Added in this revision			
Z	Deleted in this revision			

# D

## Code for microprocessor

### D.1 BoostControl.c

```
1 //To watch the ADC variables in realtime, add the following to
2 //Expressions in Watch window:
3 //
4 //Temp
5 //Isense
6 //IoutSense
7 //VacL
8 //VacN
9 //Vout
10 //DutyCycle
11 //
12 //The duty cycle can be edited in realtime. The data type for
13 //all variables are fixed point, Q 18.
14
15 #include "DSP2803x_Device.h" // DSP2803x Headerfile
16 #include "DSP2803x_Examples.h" // DSP2803x Examples Headerfile
17 #include "DSP2803x_EPwm_defines.h" // useful defines for initialization
18 #define GLOBAL_Q 18 //Sets standard Q value
19 #include "IQmathLib.h" //Library for fixed point math
20
21 void PWM1_Config(Uint16, _iq);
22 void PWM2_Config(Uint16, _iq);
```

```
23 __interrupt void adc_isr(void);
24
25 Uint16 readIsense;
26 Uint16 readIoutSense;
27 Uint16 readTemp;
28 Uint16 readVout;
29 Uint16 readVacL;
30 Uint16 readVacN;
31 Uint16 pwmPeriod;
32 __iq Isense;
33 __iq IoutSense;
34 __iq Temp;
35 __iq Vout;
36 __iq VacL;
37 __iq VacN;
38 __iq DutyCycle;
39
40 void main(void)
41 {
42 // Initialize System Control:
43 // PLL, WatchDog, enable Peripheral Clocks
44 // This example function is found in the DSP2803x_SysCtrl.c file.
45 InitSysCtrl();
46
47 // Enable Gpio for EPWM1 and EPWM2
48 // These functions are in the DSP2803x_EPwm.c file
49 InitEPwm1Gpio();
50 InitEPwm2Gpio();
51
52 // Clear all interrupts and initialize PIE vector table:
53 // Disable CPU interrupts
54 DINT;
55
56 // Initialize the PIE control registers to their default state.
57 // The default state is all PIE interrupts disabled and flags
58 // are cleared.
59 // This function is found in the DSP2803x_PieCtrl.c file.
60 InitPieCtrl();
61
62 // Disable CPU interrupts and clear all CPU interrupt flags:
63 IER = 0x0000;
64 IFR = 0x0000;
65
66 // Initialize the PIE vector table with pointers to the shell Interrupt Service Routines (ISR).
```

```

67 // This function is found in DSP2803x_PieVect.c.
68 InitPieVectTable();
69
70 // Initialize all the Device Peripherals:
71 EALLOW;
72 SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
73 PieVectTable.ADCINT1 = &adc_isr; //Enable ADC interrupt
74 EDIS;
75 InitAdc();
76 AdcOffsetSelfCal();
77
78 // Enable ADCINT1 in PIE
79 PieCtrlRegs.PIEIER1.bit.INTx1 = 1; // Enable INT 1.1 in the PIE
80 IER |= M_INT1; // Enable CPU Interrupt 1
81 EINT; // Enable Global interrupt INTM
82 ERTM; // Enable Global realtime interrupt DBGM
83
84 EALLOW;
85 AdcRegs.ADCCTL1.bit.INTPULSEPOS = 1; //ADCINT1 trips after AdcResults latch
86 AdcRegs.INTSEL1N2.bit.INT1E = 1; //Enabled ADCINT1
87 AdcRegs.INTSEL1N2.bit.INT1CONT = 0; //Disable ADCINT1 Continuous mode
88 AdcRegs.INTSEL1N2.bit.INT1SEL = 2; //setup EOC2 to trigger ADCINT1 to fire
89 AdcRegs.ADCSOC0CTL.bit.CHSEL = 4; //set SOC0 channel select to ADCINA4(dummy sample for rev0 errata workaround)
90 AdcRegs.ADCSOC1CTL.bit.CHSEL = 4; //set SOC1 channel to Isense input (ADCINA4)
91 AdcRegs.ADCSOC2CTL.bit.CHSEL = 0xB; //Temperature
92 AdcRegs.ADCSOC3CTL.bit.CHSEL = 6; //Ioutsense
93 AdcRegs.ADCSOC4CTL.bit.CHSEL = 0; //VacL
94 AdcRegs.ADCSOC5CTL.bit.CHSEL = 8; //VacN
95 AdcRegs.ADCSOC6CTL.bit.CHSEL = 2; //Vout
96
97 //set SOCx start trigger on EPWM4A
98 AdcRegs.ADCSOC0CTL.bit.TRIGSEL = 0xB;
99 AdcRegs.ADCSOC1CTL.bit.TRIGSEL = 0xB;
100 AdcRegs.ADCSOC2CTL.bit.TRIGSEL = 0xB;
101 AdcRegs.ADCSOC3CTL.bit.TRIGSEL = 0xB;
102 AdcRegs.ADCSOC4CTL.bit.TRIGSEL = 0xB;
103 AdcRegs.ADCSOC5CTL.bit.TRIGSEL = 0xB;
104 AdcRegs.ADCSOC6CTL.bit.TRIGSEL = 0xB;
105
106 //set SOCx S/H Window to 7 ADC Clock Cycles, (6 ACQPS plus 1)
107 AdcRegs.ADCSOC0CTL.bit.ACQPS = 6;
108 AdcRegs.ADCSOC1CTL.bit.ACQPS = 6;
109 AdcRegs.ADCSOC2CTL.bit.ACQPS = 6;
110 AdcRegs.ADCSOC3CTL.bit.ACQPS = 6;

```

```

111 AdcRegs.ADCSOC4CTL.bit.ACQPS = 6;
112 AdcRegs.ADCSOC5CTL.bit.ACQPS = 6;
113 AdcRegs.ADCSOC6CTL.bit.ACQPS = 6;
114
115 EDIS;
116
117 //ePWM initialization
118 // Assumes ePWM4 clock is already enabled in InitSysCtrl();
119 EPwm4Regs.ETSEL.bit.SOCAEN = 1; // Enable SOC on A group
120 EPwm4Regs.ETSEL.bit.SOCASEL = 4; // Select SOC from from CPMA on upcount
121 EPwm4Regs.ETPS.bit.SOCAPRD = 1; // Generate pulse on 1st event
122 EPwm4Regs.CMPA.half.CMPA = 0x0080; // Set compare A value
123 EPwm4Regs.TBPRD = 0xFFFF; // Set period for ePWM4, 916 Hz
124 EPwm4Regs.TBCTL.bit.CTRMODE = 0; // count up and start
125
126 //Activate PWM outputs (Period, Duty cycle)
127 //pwmPeriod = Sysclock freq / PWM output freq, 60 => 1 MHz
128 //Duty cycle as fixed point value
129 DutyCycle = _IQ(0.18);
130 pwmPeriod = 60;
131 PWM1_Config(pwmPeriod, DutyCycle); //Ch 1
132 PWM2_Config(pwmPeriod, DutyCycle); //Ch 2
133
134
135 EALLOW;
136 SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
137
138 //Overvoltage protection. Enables software to trip PWMs
139 EPwm1Regs.TZSEL.bit.OSHT1 = 1;
140 EPwm2Regs.TZSEL.bit.OSHT1 = 1;
141 EPwm1Regs.TZCTL.bit.TZA = TZ_FORCE_LO; // EPWM1A will go low
142 EPwm2Regs.TZCTL.bit.TZA = TZ_FORCE_LO; // EPWM2A will go low
143
144
145 //Overcurrent protection. Trips PWMs asynchronously when an overcurrent is detected.
146 EPwm1Regs.DCTRIPSEL.bit.DCAHCOMPSEL = DC_COMP2OUT; //Set Digital Comparator to use Comparator 2
147 EPwm1Regs.DCACTL.bit.EVT1SRCSEL = DC_EVT1; //Use DCAEVT1
148 EPwm1Regs.DCACTL.bit.EVT1FRCSYNCSEL = DC_EVT_ASYNC; //Asynchronous propagation to DCAEVT1.force
149 EPwm1Regs.TZDCSEL.bit.DCAEVT1 = TZ_DCAH_HI; //Activate when Comp 2 is HIGH
150 EPwm1Regs.TZSEL.bit.DCAEVT1 = 1; //Let DCEVT1 trigger One Shot (OSHT)
151 EPwm1Regs.TZCTL.bit.TZA = TZ_FORCE_LO; //Set EPWMxA low when tripped
152
153
154 EPwm2Regs.DCTRIPSEL.bit.DCAHCOMPSEL = DC_COMP2OUT; //Set Digital Comparator to use Comparator 2

```

```

155 EPwm2Regs.DCACCTL.bit.EVT1SRCSEL = DC_EVT1; //Use DCAEVT1
156 EPwm2Regs.DCACCTL.bit.EVT1FRCSYNCSEL = DC_EVT_ASYNC; //Asynchronous propagation to DCAEVT1.force
157 EPwm2Regs.TZDCSEL.bit.DCAEVT1 = TZ_DCAH_HI; //Activate when Comp 2 is HIGH
158 EPwm2Regs.TZSEL.bit.DCAEVT1 = 1; //Let DCEVT1 trigger One Shot (OSHT)
159 EPwm2Regs.TZCTL.bit.TZA = TZ_FORCE_LO; //Set EPWMxA low when tripped
160
161 AdcRegs.ADCCTL1.bit.ADCBFPWD = 1; //Turns ADC block on. Already done if InitAdc() have been called.
162 Comp2Regs.COMPCIL.bit.COMPDACEN = 1; //Enables Comparator 2
163
164 Comp2Regs.COMPCIL.bit.COMPSOURCE = 0x0; //Set comparator 2 to use DAC as input
165 Comp2Regs.DACCTL.bit.DACSOURCE = 0x0; //Set DAC to use defined value
166
167 Comp2Regs.DACVAL.bit.DACVAL = 639; //Tripping current. 10 A => 639
168
169 //Initialize red LED D9
170 GpioCtrlRegs.GPBMUX1.bit.GPIO40 = 0;
171 GpioCtrlRegs.GPBDIR.bit.GPIO40 = 1;
172
173 //Activate relay bypass
174 GpioCtrlRegs.GPAMUX2.bit.GPIO17 = 0;
175 GpioCtrlRegs.GPADIR.bit.GPIO17 = 1;
176 GpioDataRegs.GPASET.bit.GPIO17 = 1;
177
178 EDIS;
179
180 while (1) //Infinite loop
181 {
182
183     GpioDataRegs.GPBSET.bit.GPIO40 = EPwm1Regs.TZFLG.bit.OST; //Red light if tripped
184
185     //Conversion of ADC values into something human friendly.
186     Temp = _IQmpy(_IQdiv(_IQ(readTemp),_IQ(4096.0)),_IQ(330.0)) - _IQ(50.0);
187     Isense = _IQmpy(_IQdiv(_IQ(readIsense),_IQ(8190)),_IQ(33)) - _IQdiv(_IQ(11),_IQ(21));
188     IoutSense = _IQmpy(_IQdiv(_IQ(readIoutSense),_IQ(8190)),_IQ(33)) - _IQdiv(_IQ(11),_IQ(21));
189     VacL = _IQmpy(_IQ(readVacL),_IQ(0.09816));
190     VacN = _IQmpy(_IQ(readVacN),_IQ(0.09816));
191     Vout = _IQmpy(_IQ(readVout),_IQ(0.16194));
192
193     if(readVout >= 2624){//Turn off PWM if voltage is too high. 425 V => 2624
194         EALLOW;
195         EPwm1Regs.TZFRM.bit.OST = 1;
196         EPwm2Regs.TZFRM.bit.OST = 1;
197         EDIS;
198     }

```

```

199 //Update duty cycle if changed through Watch window
200 EPwm1Regs.CMPA.half.CMPA = _IQint(_IQmpy(_IQ(pwmPeriod), (_IQ(1.0) - DutyCycle)));
201 EPwm2Regs.CMPA.half.CMPA = _IQint(_IQmpy(_IQ(pwmPeriod), (_IQ(1.0) - DutyCycle)));
202 }
203 }
204
205 void PWM1_Config(Uint16 period, _iq duty)
206 {
207     EPwm1Regs.TBCTL.bit.PRDL = TB_IMMEDIATE;           // set Immediate load
208     EPwm1Regs.TBPRD = period - 1;
209     EPwm1Regs.CMPA.half.CMPA = _IQint(_IQmpy(_IQ(period), (_IQ(1.0) - duty))); //Sets duty cycle
210     EPwm1Regs.TBPHS.all = 0;                          //Phase zero
211     EPwm1Regs.TBCTR = 0;
212
213     EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;        //PWM counts only up
214     EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;           //EPwm1 is the Master
215     EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;       //Reference zero
216     EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
217     EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;             //PWM runs at Sysclock freq, = 60 MHz
218
219     EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
220     EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;       //Use shadow registers
221
222     EPwm1Regs.AQCTLA.bit.ZRO = AQ_CLEAR;              // PWM toggle low/high
223     EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;
224 }
225
226 void PWM2_Config(Uint16 period, _iq duty)
227 {
228     EPwm2Regs.TBCTL.bit.PRDL = TB_IMMEDIATE;           // set Immediate load
229     EPwm2Regs.TBPRD = period - 1;                      // PWM frequency = 1 / period
230     EPwm2Regs.CMPA.half.CMPA = _IQint(_IQmpy(_IQ(period), (_IQ(1.0) - duty)));
231     EPwm2Regs.TBPHS.half.TBPHS = (period - 1) / 2;    //Phase shift 180 degrees
232     EPwm2Regs.TBCTR = 0;
233
234     EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
235     EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;            //EPwm1 is the Master
236     EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;        //Synchronize with EPwm1
237     EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
238     EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
239 }
240
241
242

```

```
243 EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
244 EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
245
246 EPwm2Regs.AQCTLA.bit.ZRO = AQ_CLEAR;           // PWM toggle low/high
247 EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;
248 }
249
250 __interrupt void adc_isr(void)
251 {
252     //Save all ADC data to variables
253     readIsense = AdcResult.ADCRESULT1;
254     readTemp = AdcResult.ADCRESULT2;
255     readIoutSense = AdcResult.ADCRESULT3;
256     readVacL = AdcResult.ADCRESULT4;
257     readVacN = AdcResult.ADCRESULT5;
258     readVout = AdcResult.ADCRESULT6;
259     AdcRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //Clear ADCINT1 flag reinitialize for next SOC
260     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1; // Acknowledge interrupt to PIE
261     return;
262 }
```

## D.2 LEDblink.c

```

1 #include "DSP28x_Project.h" // Device Headerfile and Examples Include File
2
3 __interrupt void cpu_timer0_isr(void);
4
5 Uint32 lastTime = 0;
6 Uint32 currentTime = 0;
7 Uint32 lastTimeRelay = 0;
8 Uint32 currentTimeRelay = 0;
9
10 Uint32 millis(){
11     return CpuTimer0.InterruptCount;
12 }
13
14 void setup(){
15     // This example function is found in the DSP2803x_SysCtrl.c file.
16     InitSysCtrl();
17
18
19     // Clear all interrupts and initialize PIE vector table:
20     // Disable CPU interrupts
21     DINT;
22
23     // This function is found in the DSP2803x_PieCtrl.c file.
24     InitPieCtrl();
25
26     // Disable CPU interrupts and clear all CPU interrupt flags:
27     IER = 0x0000;
28     IFR = 0x0000;
29
30     // This function is found in DSP2803x_PieVect.c.
31     InitPieVectTable();
32
33     // Interrupts that are used in this example are re-mapped to
34     // ISR functions found within this file.
35     EALLOW;
36     PieVectTable.TINT0 = &cpu_timer0_isr;
37     EDIS;
38
39     // This function can be found in DSP2803x_CpuTimers.c
40     InitCpuTimers(); //Only initialize the Cpu Timers
41     // Configure CPU-Timer 0 to interrupt every millisecond:

```

```

42 // 60 MHz CPU Freq, 1 ms period in us
43 ConfigCpuTimer(&CpuTimer0, 60, 1000);
44
45 CpuTimer0Regs.TCR.all = 0x4001; // Use write-only instruction
46                               // to set TSS bit = 0
47
48 EALLOW;
49 //Configure the LED pins to outputs
50 GpioCtrlRegs.GPBMUX1.bit.GPIO34 = 0;
51 GpioCtrlRegs.GPBDIR.bit.GPIO34 = 1;
52 GpioCtrlRegs.GPAMUX2.bit.GPIO31 = 0;
53 GpioCtrlRegs.GPADIR.bit.GPIO31 = 1;
54 GpioCtrlRegs.GPBMUX1.bit.GPIO40 = 0;
55 GpioCtrlRegs.GPBDIR.bit.GPIO40 = 1;
56 GpioCtrlRegs.GPBMUX1.bit.GPIO41 = 0;
57 GpioCtrlRegs.GPBDIR.bit.GPIO41 = 1;
58
59 EDIS;
60
61 // Enable CPU INT1 which is connected to CPU-Timer 0:
62 IER |= M_INT1;
63
64 // Enable TINT0 in the PIE: Group 1 interrupt 7
65 PieCtrlRegs.PIEIER1.bit.INTx7 = 1;
66
67 // Enable global Interrupts and higher priority real-time debug events:
68 EINT; // Enable Global interrupt INTM
69 ERIM; // Enable Global realtime interrupt DBGM
70
71 }
72
73 void continous(){ //Toggle between the LEDs that are on
74     currentTime = millis();
75     currentTimeRelay = millis();
76     if(!GpioDataRegs.GPBDAT.bit.GPIO34){
77         if (currentTime - lastTime >= 2000){
78             lastTime = currentTime;
79             GpioDataRegs.GPASET.bit.GPIO34 = 1;
80             GpioDataRegs.GPACLEAR.bit.GPIO31 = 1;
81             GpioDataRegs.GPASET.bit.GPIO40 = 1;
82             GpioDataRegs.GPBCLEAR.bit.GPIO41 = 1;
83         }
84     }else{
85         if(currentTime - lastTime >= 500){

```

```
86     lastTime = currentTime;
87     GpioDataRegs.GPBCLEAR.bit.GPIO34 = 1;
88     GpioDataRegs.GPASET.bit.GPIO31 = 1;
89     GpioDataRegs.GPBSET.bit.GPIO41 = 1;
90     GpioDataRegs.GPBCLEAR.bit.GPIO40 = 1;
91     }
92   }
93 }
94
95 void main(void)
96 {
97     setup(); //Run once
98     for(;;){
99         continous(); //Run forever
100    }
101 }
102
103 __interrupt void cpu_timer0_isr(void)
104 {
105     CpuTimer0.InterruptCount++;
106     // Acknowledge this interrupt to receive more interrupts from group 1
107     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
108 }
```