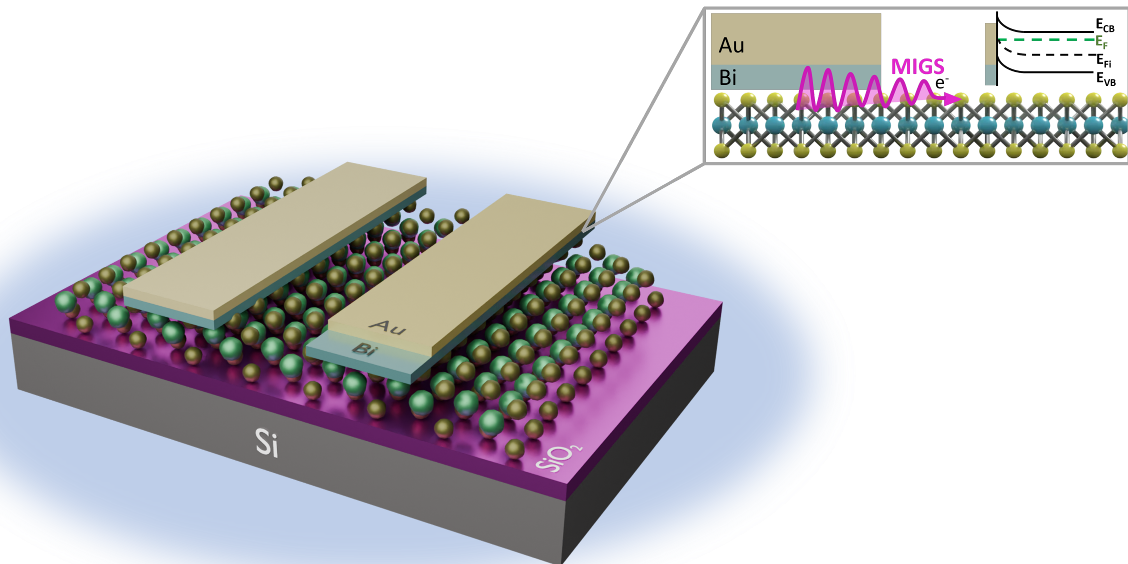

Engineering of electrical contacts on 2D-semiconductor field-effect transistors

A report on two-dimensional transistor performance evaluation

Master's thesis in Physics

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DEPARTMENT OF PHYSICS
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2024
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Emerging materials for contact engineering of two-dimensional semiconductor field-effect transistors

A report on two-dimensional transistor performance evaluation

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Division of Quantum device Physics, Nanoelectronics and Spintronics
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Cover: An MoS_2 field-effect transistor with bismuth contacts.

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Abstract

Two-dimensional (2D) semiconductor materials, such as the transition metal dichalcogenides (TMDC), have attracted great attention in the last decade due to their excellent electronic properties, thin nature, free of surface dangling bonds, and ability to retain high carrier mobility down to atomic thickness. TMDCs such as Molybdenum disulfide (MoS_2) have the potential to be integrated into and augment conventional silicon complementary metal-oxide semiconductor (Si-CMOS) technology for post-Moore's law technology. However, the performance of 2D field-effect transistors (FETs) are largely limited by poor charge carrier injection at the metal-semiconductor (M-S) interface, owing to a large Schottky barrier due to metal-induced gap states (MIGS) and fermi-level pinning (FLP). In this work, exfoliated MoS_2-FETs were fabricated and various contact engineering approaches were proposed to mitigate MIGS, to achieve efficient carrier injection. The M-S junction of gadolinium and bismuth has been investigated using state-of-the-art fabrication methods and electrical measurement techniques. Semi-metal Bi has the ability to suppress MIGS due to its near-zero density of states (DOS) near the charge-neutrality point (CNP), while gadolinium is in theory able to lower the Schottky barrier by work function tuning. Key parameters were extracted by performing temperature-dependent I-V measurements, as well as height profile analysis by AFM. It was found that both bismuth and gadolinium have the potential to be considered as good ohmic contacts to MoS_2, owing to their low SBH of $\phi \approx 43$ meV and $\phi \approx 56$ meV, respectively. This thesis work sheds light on the challenges of contact engineering and fabrication methods for 2D-FETs.

Keywords: FET, contacts, 2DMs, TMDC, MIGS, MoS_2, FLP, SBH

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Patrik Ullman, Gothenburg, June 2024

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

MOSFET	Metal-oxide semiconductor field-effect transistor
CMOS	Complementary metal-oxide semiconductor
TMDC	Transition metal dichalcogenide
FET	Field-effect transistor
SS	Subthreshold-swing
CVD	Chemical vapor deposition
PVD	Physical vapor deposition
EBL	Electron beam lithography
2DM	two-dimensional material
TLM	Transfer length method
SBH	Schottky barrier height
CMOS	Complementary metal-oxide semiconductor
SB	Schottky barrier
AFM	Atomic force microscopy
TLM	Transfer length method
I-V	Current-voltage
VLSI	Very large scale integration
FLP	Fermi-level pinning
TE	Thermionic emission
TFE	Thermionic field emission
FE	Field emission
MIT	Metal-insulator transition

Contents

List of Acronyms **ix**

List of Figures **xiii**

List of Tables **1**

1 Introduction **1**
1.1 Recent advancements 3
1.2 Aim and objective 7
1.3 Disposition 7

2 Theory and Concepts **9**
2.1 The field-effect transistor 9
2.2 Rectifying- and ohmic contact formation 10
2.2.1 Metal-induced gap states and Fermi level pinning 12
2.3 Electrical characterisation and benchmarking of key transistor parameters 14
2.4 Two-dimensional semiconducting materials 18
2.4.1 Molybdenum disulfide (MoS_2) 18
2.5 Theory regarding experimental procedure 20
2.5.1 Electron-beam lithography 20
2.5.2 Chemical vapor deposition 20
2.5.3 Exfoliation 20
2.5.4 Electron-beam physical vapour deposition 21
2.5.5 Atomic force microscopy (AFM) 21
2.5.6 AutoCAD 21

3 Device fabrication **23**
3.1 Exfoliated few-layer MoS_2-FET with Gd & Bi contacts 23
3.2 Measurement method of 2D-FET devices 26

4 Results **27**
4.1 *I*-*V* characteristics of Exfoliated few-layered MoS_2-FET with Gd contacts 27
4.2 *I*-*V* characteristics of exfoliated few-layered MoS_2-FET with Bi contacts 31

5 Conclusion **37**

List of Figures

1.1 **Timeline of transistor evolution since early 1900's.** This timeline highlights the most significant events in the history of the transistor, starting from the invention of the vacuum tube in the early 1900's [1]. 1920's brought the first transistor which was a single-point transistor with gold foil contacts. The transistor density count on integrated circuits saw exponential growth according to Moore's law when the MOSFET and related CMOS technology was invented in the 1960's. 2000's and onwards brought MOSFET's successor, the FinFET and GAAFET, allowing even greater performance. Future advancements in transistor technology may involve the integration of 2D materials into existing Si-CMOS technology and neuromorphic computation. Images are adapted from [2, 3, 4]. 2

1.2 **Recent advancements in MoS_2-FET channel engineering.** **a)** First demonstration of MoS_2 as conductive channel in a FET [5]. **b)** Single-walled carbon nanotube (SWCNT) as 1 nm gate electrode [6]. **c)** Self-aligned vertical contacts for ultra-short channel length [7]. **d)** Side-wall MoS_2 transistor with atomically thin channel [8]. **e)** Ultrashort Vertical-channel by an ultrathin insulating spacer between source and drain electrodes [9]. 4

1.3 **Recent advancements in MoS_2-FET contact engineering.** **(a)** MoS_2-FET with Al_2O_3 as interspacer between Ti contacts and MoS_2 channel [10]. **b)** Phase-engineering from 2H semiconducting to 1T metallic phase of MoS_2, thereby using 2DM for both channel and contacts [11]. **c)** Top contact and edge contact geometries of a FET. **d)** Semimetal-semiconductor junction FET using Bi as contact [12]. **e)** MoS_2-FET with graphene as interlayer between Ti and channel [13]. **f)** MoS_2-FET with gadolinium top contacts [14]. 6

2.1 **Schematic of a typical n-type MOSFET.** In this configuration, the gate terminal (G) is electrostatically coupled with the channel material through the gate oxide. The flow of charge carriers in the channel is modulated by a voltage bias. 9

2.2 **Ohmic contact interface before and after the formation of a junction.** **(a)** Prior to contact formation. **(b)** Post contact formation. Here, band bending is occurring due to the difference between metal work function ϕ_m and semiconductor electron affinity χ_s. . . . 11

2.3 **Rectifying contact interface before and after the formation of a junction.** **(a)** Prior to contact formation. **(b)** Post contact formation. here, a rectifying behaviour is observed and a Schottky barrier is formed due to the difference between ϕ_m and χ_s. 12

2.4 **Fermi level pinning and metal-induced gap states.** **a)** Energy diagram showing various Fermi levels pinned to a fixed location within the band gap of MoS_2. **b)** Schematic of metal-induced gap states in an M-S junction. Here, the metal electronic wave functions perturb the potential of the semiconductor, inducing gap states at the interface, shown as pink horizontal lines. 13

2.5 **Key parameters**. **a)** Typical logarithmic transfer curve to extract subthreshold swing. **b)** Linear transfer curve at a certain V_{GS} and linear extrapolation to extract V_{th}. **c)** Extraction of transconductance which corresponds to the slope of the linear region. 15

2.6 **Charge carrier mechanisms and extraction of Schottky-barrier height at flat-band voltage.** **a)** Charge carrier injection mechanisms at various voltage regimes, (Thermionic emission (TE), Thermionic field emission (FTE), Field emission (FE)). **b)** Typical Arrhenius plot for various voltages. **c)** Effective potential barrier expressed in meV as a function of applied gate voltage. The actual SBH is extracted at the flat-band voltage, where the curve deviates from its linear dependence on gate voltage. The figure is adapted from [15]. 17

2.7 **Geometrical structure for TLM measurement.** **a)** Contacts with varying spacing are patterned on the channel material on the substrate. **b)** A typical graph of TLM measurement. The y-axis intercept of the linear fit gives $2R_C$ and the slope gives the R_{sheet}. . . 18

2.8 **Crystal structure and band gap of MoS_2.** **a)** Crystal structure of MoS_2. **b)** Semiconducting 2H-phase (stable) and metallic 1T-phase (metastable). **c)** Optical band gap of mono-layer, few-layer, and bulk MoS_2. Images are partly adopted from [11, 16, 17]. 19

3.1 **Exfoliation and transfer of MoS_2.** A Polydimethylsiloxane (PDMS) is placed with the sticky side onto bulk MoS_2 and gently rubbed to allow MoS_2 to adhere to the surface. This process is done repeatedly to obtain few-layer sheets. The PDMS with MoS_2 attached is placed onto the SiO_2 substrate and gently rubbed. Lastly, PDMS is carefully and slowly removed and few-layer MoS_2 is transferred to the SiO_2 substrate. 24

3.2 **Workflow of fabrication method.** The substrates are first spin-coated to create a uniform positive resist layer. The soft baking ensures hardening of the resist. AutoCAD were used to design the contact blueprints which were communicated with JEOL EBL for exposure. Development is done to reveal the EBL patterning. PVD is used to deposit Ti, Au, Gd, and Bi. Lift-off is performed in Acetone to remove unwanted metals. The device is then taken out of the cleanroom for transistor measurements. 24

3.3 **Complete device structures.** **a)** Complete structure of MoS_2-FET with gadolinium contacts. The device has a back-gate, top contact configuration with channel length and width of 0.4 μm and 6.0 μm, respectively. **b)** Complete structure of MoS_2-FET with bismuth contact. The device has a back-gate, top contact configuration with channel length and width of 0.4 μm and 0.4 μm, respectively. 25

3.4 **Measurement setup and circuit diagram**. **a)** Device on SiO_2-substrate mounted on chuck holder. The substrate is attached to the holder by Ag-paste, and each contact is then bonded by 25 μm gold wire to each bonding pad. **b)** Circuit diagram for electrical measurements. 26

4.1 **Height profile analysis by AFM.** **a)** MX50 Optical image of the device. The source and drain are marked with red dots. **b)** AFM height profile image. The white line indicates where the height profile has been assessed. **c)** AFM height analysis shows a channel thickness of $\approx$ 20 nm. 28

4.2 **Electrical measurements of exfoliated MoS_2-FET with Gd contacts.** **a)** MX50 optical image of the device. Transistor properties are measured between the source and drain marked 's' and 'd'. **b)** Transfer characteristics in linear scale measured between $V_{GS} = [-60, 60]$ V for $V_{DS} = [0.1, 1]$ V in steps of 100 mV. The maximum current is around 60 μA. **c)** Output characteristic curve for various V_{GS} in linear scale. **d)** Summary of extracted parameters. L_c is channel length, W_c is channel width, and t is flake thickness. **e)** Transfer curve in logarithmic scale for V_{DS} between 0.1 V and 1 V and **f)**, output curve in logarithmic scale. 28

4.3 **Extraction of Schottky barrier height (Φ_{SBH}) at flat-band condition and μ-T dependence.** **a)** MX50 optical image of the device. **b)** Temperature-dependent tranfer characteristics measured at $V_{DS} = 1$ V for T= [100,300] K in linear scale and, **c)** logarithmic scale. **d)** Mobility μ_{FE} as a function of temperature. The positive mobility dependence on temperature between 100K to 250K is attributed to transport dominated by ionized impurity scattering. Above 250 K, mobility decreases due to phonon scattering. **e)** Arrhenius plot constructed according to the Arrhenius technique. **f)** Effective potential barrier as a function of gate voltage. $\Phi_{SBH} \approx 56$ meV is extracted at flat-band condition, where the curve deviates from linearity. 30

4.4 **Height profile analysis by AFM.** **a)** MX50 Optical image of the device. The source and drain are marked with red dots. **b)** AFM height profile image. White lines indicate where the height profile has been assessed. **c)** AFM height analysis showing a channel thickness of around 10 nm, i.e. ca 14 layers. 31

4.5 **Electrical measurements at 300K of exfoliated MoS_2-FET with bismuth contacts.** **a)** MX50 optical image of the device. The source and drain are marked with red dots. **b)** Transfer characteristics in linear scale measured between $V_{GS} = [-60, 60]V$ for $V_{DS} = [0.1, 1]$ V in steps of 100 mV. **c)** Transfer curve in logarithmic scale for V_{DS} between $[0.1, 1]$ V. **d)** Summary of extracted parameters. L_c is channel length, W_c is channel width, and t is flake thickness. **e)** Output characteristic curve for various V_{GS} in linear scale and **f)** logarithmic scale. 32

4.6 **Extraction of Schottky barrier height (Φ_{SBH}) at flat-band condition and μ-T dependence.** **a)** MX50 optical image of the device. Here, the source and drain are marked by 'S' and 'D'. **b)** Temperature-dependent tranfer characteristics measured at V_{DS} = 1 V for T=[100,300] K in linear scale and logarithmic scale. **c)** Contour plot of temperature, drain current, and gate bias. **d)** Mobility μ as a function of temperature T above, at, and below phase transition. Transconductance was extracted at [-35,-30] V below transition, [-30,-15] V at the transition, and [20,40] V above transition. **e)** Arrhenius plot constructed according to the Arrhenius technique. **f)** Effective potential barrier as a function of gate voltage. $\Phi_{SBH} \approx 43$ meV is extracted at flat-band condition. 33

4.7 **Schottky barrier height for multilayer MoS_2 devices.** Previously reported values of SBH as dependent on work function. The red stars represent this work calculated SBH by thermionic emission model. Previously reported SBH are obtained from [18], [19], [20], [14]. 34

4.8 **Metal-insulator transition.** **a)** Temperature-dependent transfer curve, highlighting the insulator and metallic regions. The threshold for phase transition occurs at around -15 V, corresponding to $n_{crit} \approx 2.62{\cdot}10^{13}\ cm^{-3}$. **b)** Percolation exponent as a function of temperature. The red line is a mean value of $\delta \approx 1$. **c)** Schematic of variable-range hopping and percolative transport. At the insulating phase, VRH occurs due to strong localization and at metallic phase weak localization dominates, resulting in percolative transport. 35

.1 **Contact design in AutoCAD.** II

.2 **Temperature dependent measurements and extraction of Φ_{SBH} at flat-band condition.** **a)** MX50 optical image of the device. **b)** Temperature-dependent tranfer characteristics measured at V_{DS} = 1 V for T=100 K to 300 K in linear scale and, **c)** logarithmic scale. **d)** Mobility μ as a function of temperature. The positive mobility dependence on temperature between 100K to 250K is attributed to transport dominated by ionized impurity scattering. Above 250 K, mobility decreases due to phonon scattering. **e)** Arrhenius plot **f)** Effective barrier as a function of gate voltage and Schottky barrier extraction. III

.3 **Electrical measurements at 100K of exfoliated MoS_2-FET with bismuth contacts electrodes.** **a)** MX50 optical image of the device. **b)** Transfer characteristics in logarithmic scale measured between $V_{GS} = [-60, 60]V$ for $V_{DS} = [0.1, 1]$ V in steps of 100 mV. **c)** Transfer curve in linear scale for V_{DS} between $[0.1, 1]$ V. **d)** Output characteristic curve for various V_{GS} in linear scale and, **e)** logarithmic scale. **f)** Summary of key parameters extracted for I-V measurements. IV
.4 **Contact resistance extraction by TLM.** **a)** Optical image of the device. **b)** The contact resistance was estimated by the TLM method to be $R_c \approx 4.2 \cdot 10^5\ \Omega$, and sheet resistance $R_{sheet} \approx 1.67 \cdot 10^6\ \Omega$. **c)** Geometrical structure of a TLM measurement setup. IV
.5 **Contour plot and hysteresis.** **a)** Optical image of the device. **b)** Contour plot of temperature-gate dependence and current. **c)** Hysteresis at high and low temperature. Hysteresis disappears at low temperature due to inert interface trap sites. V

1
Introduction

Modern civilization is founded on a nanoscale switch named "transistor". The transistor was theorised in 1926 [21], and invented in 1947 at Bell Laboratories, influenced by the discovery of the electron and the vacuum tube. The first transistor was a single-point transistor made of two gold foil contacts resting on a germanium crystal [22]. In 1948, the same group at Bell Labs invented the bipolar junction transistor (BJT) which utilises both electrons and holes as charge carriers. Ten years later, the planar structure metal–oxide semiconductor field-effect transistor (MOSFET) was also invented at Bell Labs, marking one of the most important inventions in human history [23]. The MOSFET was able to overcome challenges that other uni-polar field-effect devices faced with electronic surface states, making it a critical step for realising large-scale semiconductor-device manufacturing. In the same year, the first Si-MOSFET compatible integrated circuit (IC) was invented [24]. The IC became and still is the central driving force for the evolution of the transistor. Its invention led to the miniaturization of electronic components, enabling the development of smaller, faster, and more efficient electronic devices. In 1963, the IC was further improved with complementary metal-oxide-semiconductor (CMOS) technology which complements p-type and n-type MOSFETs, allowing an even higher transistor on chip density and introducing very large scale integration (VLSI) [1]. Fig.1.1 presents a timeline of the major innovation steps in the history of the transistor since the early 1900's.

The density count of transistors on an ICs has seen exponential growth since the 1960's, in an observation known as Moore's law guided by Dennard's scaling principle [25, 26]. Today, the state-of-the-art IC chip has a transistor density of over 100 million transistors per square millimetre. For example, Apple iPhone's A17 processor chip contains 19 billion transistors and Intel's Core i9 contains around 25 billion units. Being the most fundamental building block in modern electronics, it could be argued that the invention of the transistor is what has impelled our society into the information age of exponential growth, which undoubtedly candidates the device as the most important invention of the 20th century.

The silicon-MOSFET was the dominating technology for almost five decades, until the invention of the Si-finFET in the early 2000's. The improved design allows significantly faster switching times and higher current density due to enhanced electrostatic control of the fin-shaped channel by the gate that encapsulates it. The device operates at a lower voltage than the planar structure and still has less current leakage while maintaining the same performance at half the power consumption. The

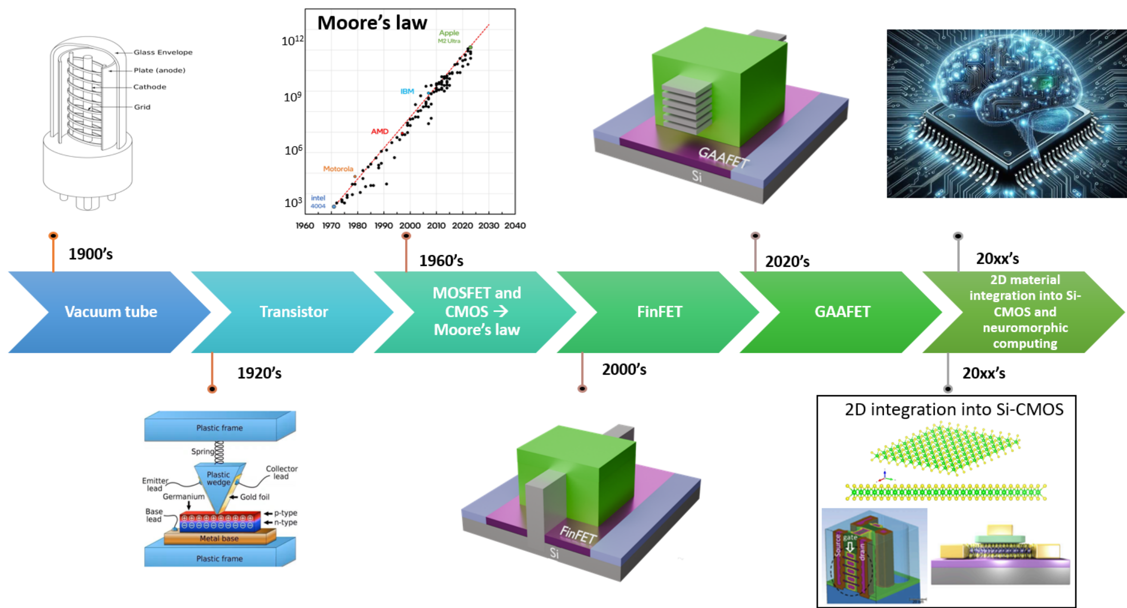


Figure 1.1: Timeline of transistor evolution since early 1900's. This timeline highlights the most significant events in the history of the transistor, starting from the invention of the vacuum tube in the early 1900's [1]. 1920's brought the first transistor which was a single-point transistor with gold foil contacts. The transistor density count on integrated circuits saw exponential growth according to Moore's law when the MOSFET and related CMOS technology was invented in the 1960's. 2000's and onwards brought MOSFET's successor, the FinFET and GAAFET, allowing even greater performance. Future advancements in transistor technology may involve the integration of 2D materials into existing Si-CMOS technology and neuromorphic computation. Images are adapted from [2, 3, 4].

successor to FinFET technology is expected to be the emergence of the nanosheet Gate-All-Around-Field-Effect-Transistor (GAAFET). In this architecture, the gate fully encapsulates multiple ultrathin channels, providing even better electrostatic control, lower current leakage, and allowing even lower voltage than its predecessors, Fig.1.1.

Although the planar-FET, FinFET, and GAAFET technologies are highly advanced, Silicon-based transistors are reaching the scaling limit as gate- and channel lengths are reaching nano-scale. Below a certain threshold, short channel effects such as drain-induced barrier lowering, low mobility due to strong scattering, and tunnel currents, will significantly degrade the performance of the device. For example, mobility μ decreases with the body thickness to the sixth power $\mu - t^6$ while the band gap increases by the square of the thickness [27]. It is thus important to explore novel materials and find ways of designing next-generation transistors to mitigate degradation and heat dissipation, to extend Moore's law.

In the past decade, *two-dimensional transition metal dichalcogenides* (2D TMDCs) has attracted considerable attention for potentially being suited as channel material

for next-generation nanoelectronics and field-effect devices. Their naturally atomically thin nature, free of surface dangling bonds, coupled with excellent electrostatic control, tunable band gap, and ability to retain high carrier mobility down to atomic thickness make them promising candidates [28, 29, 30]. The excellent properties of 2D materials (2DMs) greatly mitigate short-channel effects that naturally arise in the scaling of silicon-based electronic devices, which collectively makes them promising candidates for extending Moore's law. Even though it is a relatively young family of materials, 2D semiconductors are seeing a wide range of applications in areas such as VLSI, RF electronics, neuromorphic computing, sensing, memory logic, logic gates, optoelectronics, photovoltaics, and even spintronics [31] [32] [33], [34]. What's more, 2D semiconductors carry great potential to be integrated into and augment existing Si-CMOS technology owing to their ability to retain high carrier mobility at atomic thickness [35, 36].

Given the potential and broad applicability of these 2DMs, it is evident that there is a great incentive to further explore the realm of 2D semiconductors in field-effect transistors. However, the performance of 2D-FETs are largely limited by poor charge carrier injection at the metal-semiconductor (M-S) junction, where metal-induced gap states (MIGS), Fermi-level pinning (FLP), and Schottky barrier height (SBH) play vital roles. Therefore, the focus of this work lies in the aspect of contact engineering of 2D-FETs and the role 2D semiconductors play as ultra-thin nanosheets as channel materials for next-generation field-effect transistors.

1.1 Recent advancements

This section outlines the recent advancements in the field of 2D-FETs and serves to give the proper context and motivation for this project. The first part mainly covers advancements and current research regarding channel length and scaling of 2D-FETs. The second part highlights the relevant research and challenges in minimizing contact resistance and achieving ohmic contacts through contact engineering of 2D-FETs.

In the last decades, efforts have been made to scale down the transistor and at the same time enhance performance and switching characteristics. Due to Silicon-based technology suffering from short-channel effects, much effort has been devoted to finding new materials in which the main focus has been on two-dimensional materials such as TMDs (MoS_2, Wse_2, WS_2). 2DMs naturally introduce atomically thin channel lengths that are much more resilient to short-channel effects than Silicon-based transistors in terms of mobility degradation.

One of the pioneering papers of 2D-FETs showed, for the first time, the possibility of fabricating a FET using monolayer Molybdenum disulfide (MoS_2) as a single layer conductive channel, insulated from the gate by Hafnium dioxide HfO_2, Fig.1.2a. Their results paved the way for realising applications of electronics and integrated circuits based on 2DMs and sparked further interest in this novel field of research [37].

B. Desai et al. showed that a single-walled carbon nanotube (SWCNT) can be used as gate to reach a gate length of 1 nm and sub-50 nm channel length, Fig.1.2b. The device measured excellent performance, although difficult to realise in large-scale production [6]. Jinbao et al. fabricated a nanometer-scaled transistor with a channel length of 10 nm via a vertical channel using MoS_2 Fig.1.2e, demonstrating feasibility for high density and large scale integration [9].

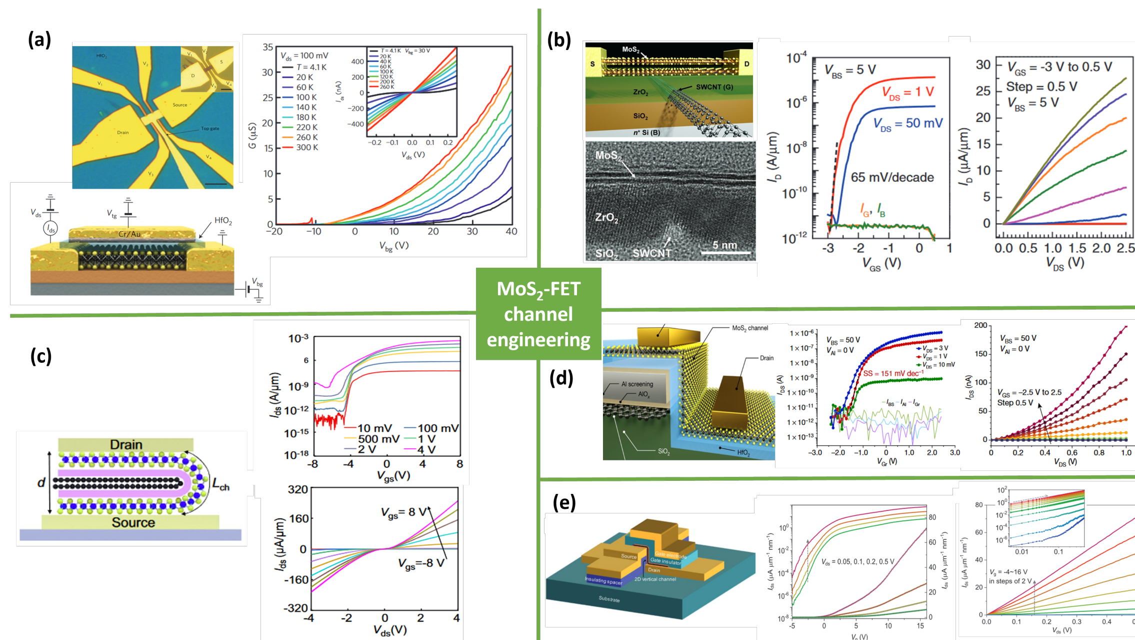


Figure 1.2: Recent advancements in MoS_2-FET channel engineering. a) First demonstration of MoS_2 as conductive channel in a FET [5]. **b)** Single-walled carbon nanotube (SWCNT) as 1 nm gate electrode [6]. **c)** Self-aligned vertical contacts for ultra-short channel length [7]. **d)** Side-wall MoS_2 transistor with atomically thin channel [8]. **e)** Ultrashort Vertical-channel by an ultrathin insulating spacer between source and drain electrodes [9].

Another vertical configuration was demonstrated as a side-wall MoS_2 transistor with an atomically thin channel and a physical gate length below 1 nm by utilizing the natural thickness of graphene as a gate electrode Fig.1.2d, showing promising current-voltage characteristics [8].

Liting liu et al. demonstrated a method to simultaneously scale gate and channel length by mechanically folding a stacked graphene/boron nitride/MoS_2-heterostructure, thus achieving precise alignment of source-drain contacts around the folded edge Fig.1.2c. The device realized sub-1 nm gate determined by the thickness of graphene, and sub-50 nm channel length determined by the thickness of the heterostructure [7].

Furthermore, the performance of 2D-FETs are largely limited by poor charge carrier injection at the M-S contact junction, since this parameter determines the contact resistance R_C. A key challenge and bottleneck of realising high-performance 2D-FETs is obtaining low contact resistance for efficient carrier injection. 2D-FETs

are currently limited by the presence of a Schottky barrier (SB) in which Fermi-level pinning (FLP) and metal-induced gap states (MIGS) play vital roles. Much effort has been devoted to understanding the nature of the contact interface in these devices, with the aim of decreasing the rectifying Schottky barrier and achieving low-resistance ohmic contacts. Ohmic contacts in conventional bulk silicon transistor technology are usually realised by heavily doping the source and drain regions by methods such as ion implantation or diffusion. However, doping of 2DMs such as MoS_2 and WSe_2 has proven challenging because the incorporation of dopants into atomically thin layers will introduce defects and degrade performance.

There are a few creative contact engineering approaches that are employed to achieve low contact resistance. Methods that have seen proof-of-concept include metal work function engineering, choosing appropriate electrode material according to physical properties, contact geometry design engineering, incorporation of interlayer spacer between M-S junction, Van der Waals contacts, semimetal-semiconductor contacts junction, among others [10, 28].

It has been shown that inserting an ultra-thin Al_2O_3 layer of a certain thickness between metal-MoS_2 contacts, Fig.1.3a, yields a lower contact resistance, low Schottky barrier (SB), improved on/off-ratio, and higher mobility μ compared to the absence of an interlayer spacer. The idea is that the interlayer acts as a physical barrier between the two materials so that the wave function from the metal cannot extend to penetrate the semiconductor, reducing the density of MIGS and thus mitigating the effects of FLP [10]. Unpinning the Fermi-level in this way allows for lower SBH which is associated with lower contact resistance [38]. Another research group utilised a similar concept to alleviate FLP and mitigate MIGS, using TiO_2 as an interlayer [39].

Moreover, several studies have explored graphene as a contact material because its properties may prevent or mitigate FLP. It has been shown that graphene can be introduced as an interlayer spacer for 2D-FETs due to its tunable Fermi level and semi-metal nature [40]. Chee et al. used CVD-grown graphene film to realise a MoS_2-FET with gr/Ag contacts, Fig.1.3e, showing an improvement in output and transfer characteristics as well as lower SBH compared to conventional Au/Ti contacts [41]. Another research group introduced a graphene interlayer between Ti contacts and large area MoS_2 using a wet transfer method. They were able to achieve a low Schottky barrier, due to the clean interface between the two 2D materials, thus lowering contact resistance [13].

Ohmic contacts between semi-metallic bismuth and MoS_2 have been reported, Fig.1.3d, where MIGS are suppressed to the point where a zero Schottky barrier height was achieved. A contact resistance of 123 Ω µm marks one of the lowest measured resistances in this context to date [12]. Recently, another group of researchers fabricated a MoS_2-FET that approaches the contact resistance quantum limit by utilizing hybridization of energy bands at the fermi level with semi-metal antimony as contacts [42].

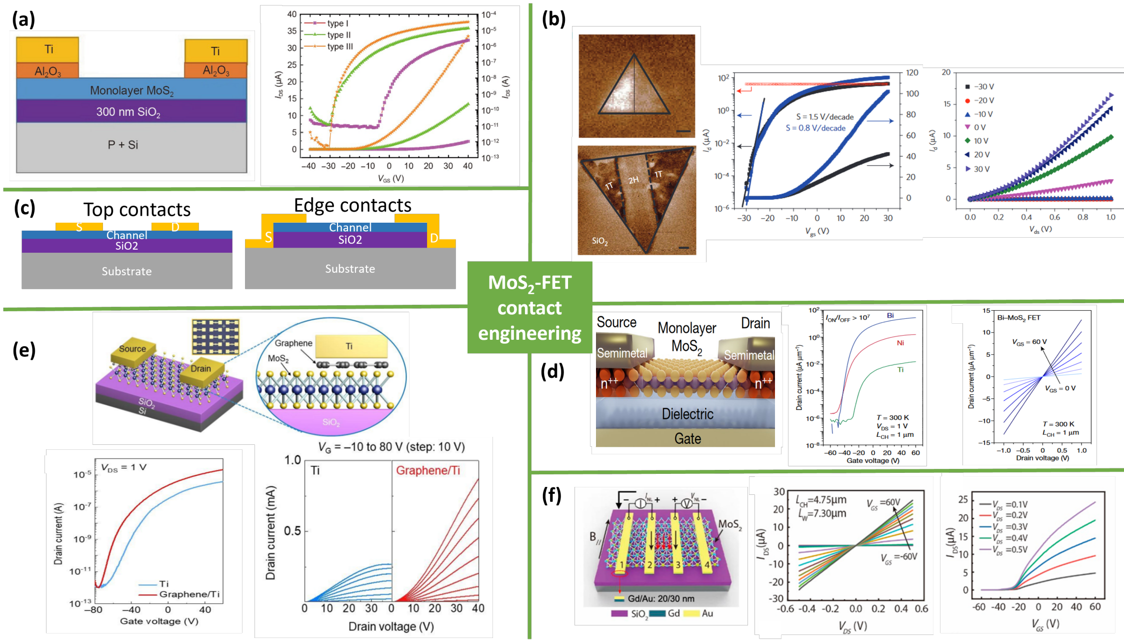


Figure 1.3: Recent advancements in MoS_2-FET contact engineering. (a) MoS_2-FET with Al_2O_3 as interspacer between Ti contacts and MoS_2 channel [10]. **b)** Phase-engineering from 2H semiconducting to 1T metallic phase of MoS_2, thereby using 2DM for both channel and contacts [11]. **c)** Top contact and edge contact geometries of a FET. **d)** Semimetal-semiconductor junction FET using Bi as contact [12]. **e)** MoS_2-FET with graphene as interlayer between Ti and channel [13]. **f)** MoS_2-FET with gadolinium top contacts [14].

As for metal work function engineering, a group has shown that low work function metals such as Ytterbium (Yb) can be used for good electrical contacts to few-layer WS_2 [20]. Moreover, a CVD-grown MoS_2 device was very recently fabricated using lanthanide materials Gadolinium (Gd) and Samarium (Sm) as contact electrodes. They were able to realise an almost negligible SBH and ohmic behaviour [14].

The most common contact geometry designs are surface contacts (top and bottom) and edge contacts, Fig.1.3b. The top-contact configuration is relatively simple to fabricate by for example physical vapor deposition (PVD) and is used throughout this project. The ease of fabrication comes with the trade-off that carrier injection occurs out-of-plane in this configuration, which is suboptimal.

Edge contact has proven advantageous in several ways, however, higher complexity of fabrication steps are needed due to the ultra-small contact area of the edge of a 2D material. The contacts are formed at the edge of the 2D material, which means that the charge carrier injection happens in-plane which is more efficient than that of top contact configuration [38]. Furthermore, the space separation between metal-2DM edge contacts is smaller than for top contacts. The reduced separation results in a stronger orbital overlap and thinner tunnel barrier, making charge

carrier injection more efficient for edge configurations. Although the edge contact configuration on metal-TMDs has proven difficult, a group recently succeeded in making a one-dimensional edge contact by applying SF_6/O_2 plasma etching on a hBN-MoS_2 heterostructure [43].

Phase engineering of 2DMs has been investigated for contact improvement. MoS_2 can for example be utilized as both channel and contact electrodes by locally inducing a phase change from its semiconducting 2H-phase to metallic 1T-phase at the junction. The phase change creates an atomically sharp boundary at the contact interface and reduces the contact resistance by a great amount [11].

It is evident that great efforts have been made and considerable progress has been proven in the field of improving overall transistor technology, however, all aspects are still not well understood and require more research. The field still faces challenges with scaling, choice of materials, improving contact interface and charge carrier injection, as well as realizing large-scale CMOS-compatible integration.

1.2 Aim and objective

Given the recent advancements and current challenges that 2D-FETs face regarding contact interface, this thesis project aims to explore various contact engineering approaches with the goal of expanding the knowledge base of contact formation between 2DMs and unconventional three-dimensional electrodes. The two contact engineering approaches in this thesis include work function metal tuning using gadolinium, and semimetal-semiconductor junction using bismuth as electrode. This will be realised through state-of-the-art fabrication techniques such as electron-beam lithography (EBL), physical vapour deposition (PVD), atomic force microscopy (AFM), and exfoliation. Furthermore, as the research of 2D-FETs has grown to such a vast field, all aspects cannot be considered. This thesis is therefore limited to analysing contact interfaces between gadolinium, bismuth and few-layer MoS_2 as conductive channel.

1.3 Disposition

The first chapter of this thesis gives a general introduction and historical context to the transistor and the role of 2D semiconductors, as well as recent advancements in the field of channel scaling and contact engineering. Chapter two outlines the necessary theory, concepts, methodology, and fabrication methods on which this work stands on. Chapter three presents the resulting measurement and performance evaluation. Lastly, a conclusion is presented along with an outlook on what lies ahead as well as various pathways for continuing research.

2

Theory and Concepts

This section is initiated by introducing the concept and working principle of the main subject in this thesis, the *field-effect transistor*. Next, concepts and theory regarding metal-semiconductor contact interface and characterisation techniques of FETs will be introduced to provide the proper context for the measurement results and performance evaluation. The last section reviews the theory behind the experimental procedures and instruments used in this work which are mainly EBL, Exfoliation, and EBPVD.

2.1 The field-effect transistor

The field-effect transistor (FET) is an electrical device that is capable of current gain, voltage gain, and signal power gain. It has the ability to turn on and off a current flow at high switching times, making the device essential for almost any modern electric device.

The FET typically consists of four terminals called the source, drain, gate, and body or substrate. The basic structure is shown in Fig.2.1 and the working princi-

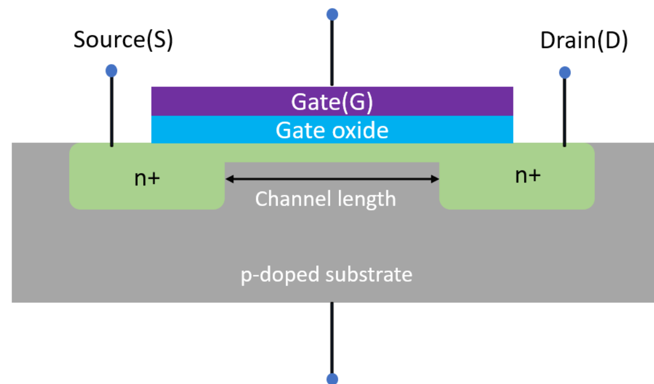


Figure 2.1: Schematic of a typical n-type MOSFET. In this configuration, the gate terminal (G) is electrostatically coupled with the channel material through the gate oxide. The flow of charge carriers in the channel is modulated by a voltage bias.

ple is as follows. The conductance in the semiconductor channel between the source and drain can be controlled by the gate terminal, which is electrostatically coupled

through the dielectric gate oxide. It is essentially the electric field effect induced by applying a gate voltage that allows the device to vary the carrier concentration in the semiconductor channel and, consequently, change an electric current flowing through the source and drain terminals. Essentially the device works as a very quick switch. The working principle can be illustrated by a simple analogy. Imagine a water faucet where the knob (gate) controls the flow of water (charge carriers) from the source (pipe) to the drain (sink). Turning the knob adjusts the flow rate, just as how voltage applied to the gate controls the current flow in a FET.

The electrostatics in the device is governed by the one-dimensional Poisson's equation,

$$\frac{d^2\phi(x)}{dx^2}\frac{\phi(x)}{\lambda^2} = 0 \tag{2.1}$$

where $\lambda = \sqrt{\frac{t_b t_{ox} \epsilon_b}{\epsilon_{ox}}}$, $\phi(x)$ is the potential in the source-drain direction, λ is the transistor characteristic length, t_b and t_{ox} are the body and oxide thicknesses respectively, and $\epsilon_{t,ox}$ are body and oxide permeability, respectively [27].

The most widely used transistor is the MOSFET, and the basic operation is as follows. The MOSFET utilises the concept of doped regions and the PN-junction, and can essentially be operated in four modes; n-type depletion mode, n-type enhancement mode, p-type depletion mode, and p-type enhancement mode. In n-type semiconductors, electrons are the majority charge carriers, and in p-type, holes act as the majority charge carriers. Whether the device uses electrons or holes as charge carriers is determined by the doping procedure.

In an n-type channel depletion mode setting, a negative gate-to-source voltage induces a charge depletion region at the semiconductor-oxide interface which effectively removes the ability for the charge carriers to flow, thus switching off the device. In this mode of operation, the channel region is present even at zero gate voltage. The channel is present until a negative voltage reduces or removes it.

For the n-type enhancement mode, the opposite is true. A positive source-to-gate voltage induces an electron inversion layer connecting the source and drain, thus creating a channel for charge carriers to flow. The p-channel device operates similarly to its n-channel counterpart, with the difference being that the charge carriers are holes, and both the conventional current direction and voltage polarities are reversed.

2.2 Rectifying- and ohmic contact formation

The contacts are the components that connect the field-effect device to the outside world. It is the link between the transistor and all external circuitry.
When a metal and a p- or n-type semiconductor come in close proximity, a junction of either non-rectifying ohmic behaviour, or rectifying electrical behaviour will be formed. The contact resistance in a 2D-FET is given by

$$R_C = \frac{h^3}{4\pi e^2 m^* t k_b T}(\frac{e\phi_B}{k_B T}) \tag{2.2}$$

where ϕ_B is the Schottky barrier height, m* is the effective mass, t is the thickness, and h is Planck's constant [28].

An *Ohmic contact* is a non-rectifying electrical junction that exhibits a linear current-voltage relationship according to Ohm's law $V = IR$. This type of contact is the most desired one given the context, as it achieves low contact resistance at the interface, allowing efficient carrier injection. It is the usual behaviour that a silicon-based MOSFET exhibits and achieves through doping of source and drain terminals. Fig.2.2a, b shows an M-S junction before and after ohmic contact formation. After formation, band bending occurs due to differences in the material properties. In this case, a negative Schottky barrier is realised which is associated with efficient carrier injection and low resistance.

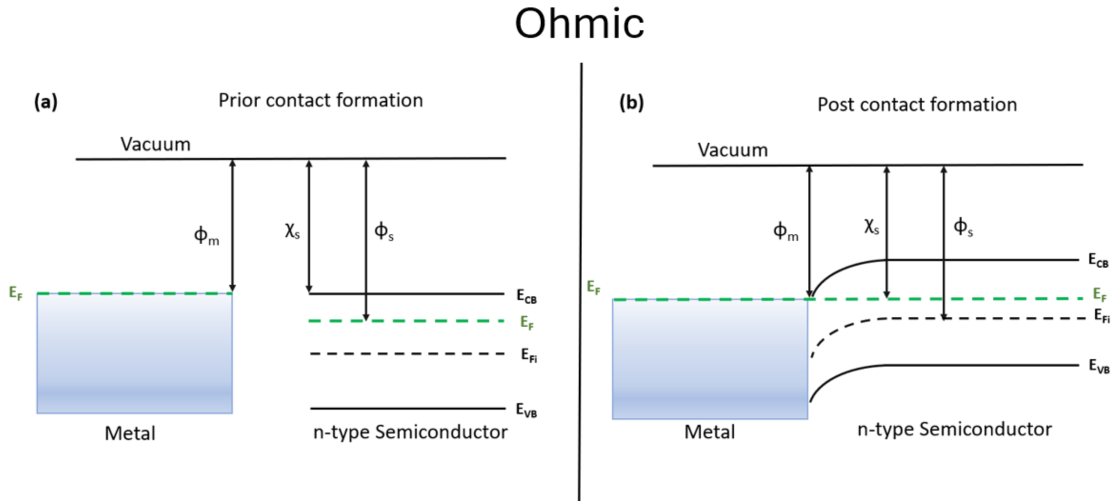


Figure 2.2: Ohmic contact interface before and after the formation of a junction. **(a)** Prior to contact formation. **(b)** Post contact formation. Here, band bending is occurring due to the difference between metal work function ϕ_m and semiconductor electron affinity χ_s.

Certain contact junctions will not show an ohmic behaviour but instead form a rectifying electrical junction that almost only conducts current in one direction according to a diodic behaviour. In Fig.2.3a, the Fermi-level of the semiconductor is below that of the metal.
In this context, a system is considered to be in thermal equilibrium when the Fermi level aligns throughout the system. It then follows that for the system to equilibrate, charge carriers occupying quantum states in the semiconductor have to migrate to the lower quantum states of the metal according to the Fermi-Dirac distribution. This scenario happens immediately after contact formation and is shown in Fig.2.3b. Here, band bending occurs and a rectifying contact and hence a potential barrier named *Schottky barrier* (SB) is formed due to the difference between metal work

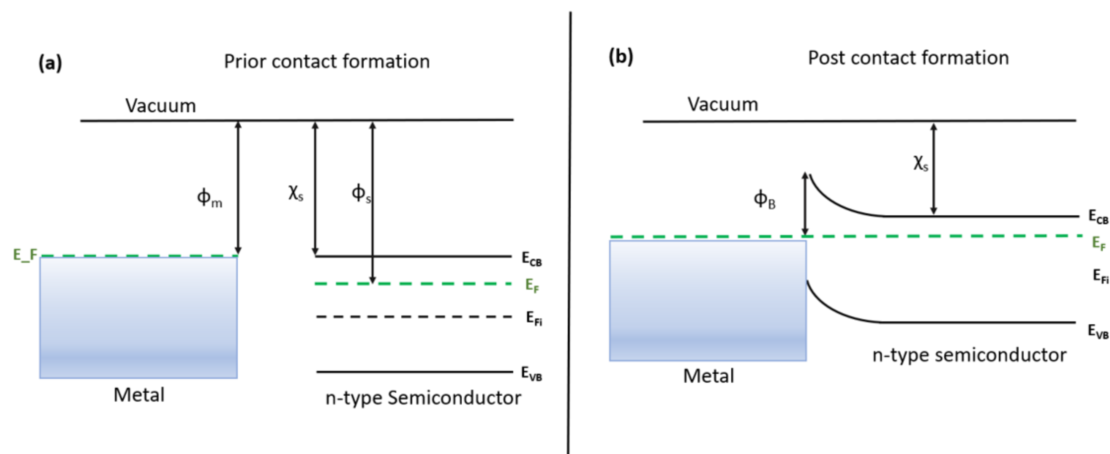


Figure 2.3: Rectifying contact interface before and after the formation of a junction. **(a)** Prior to contact formation. **(b)** Post contact formation. here, a rectifying behaviour is observed and a Schottky barrier is formed due to the difference between ϕ_m and χ_s.

function ϕ_m and electron affinity χ_s.

If the semiconductor is n-type and the metal work function is larger than the electron affinity of the semiconductor a barrier will be formed. The likewise but opposite relation holds for p-type semiconductors. As a result, the Schottky barrier hinders charge carriers from flowing from the semiconductor to the metal, thus per definition increasing resistance.

2.2.1 Metal-induced gap states and Fermi level pinning

The Schottky barrier height can be theoretically determined by the Schottky-Mott rule [43]. The rule states that the potential barrier seen by the charge carriers is proportional to the difference between the metal vacuum work function and the semiconductor electron affinity, as in equation 2.3.

$$\Phi_{Schottky} = \phi_m - \chi_s \tag{2.3}$$

where the vacuum metal work function ϕ_m is the minimum thermodynamic work needed to remove an electron from the metal to a point outside of the surface, and electron affinity χ_s quantifies the tendency of an atom to form a negative ion.

The Schottky-Mott rule is an ideal case and does not reflect all the real physics behind contact formation. The rule often predicts incorrect barrier height, partly due to a phenomenon called *Fermi-level pinning* (FLP). The pinning effect can arise naturally in the M-S interface if there exist chargeable states in the semiconductor. These surface states can be induced when the junction is formed, or already be

present prior to formation. The effect happens due to surface states absorbing charge from the metal, thus shielding the semiconductor. This will result in the alignment of the semiconductor's electronic band structure which will pin to the Fermi level. The concept of Fermi level pinning effect for various metal-semiconductor pairs is shown in Fig.2.4a. Due to pinning, the Schottky barrier height seems to show very little dependency on metal work function and electron affinity as stated by the Schottky-Mott rule [43].

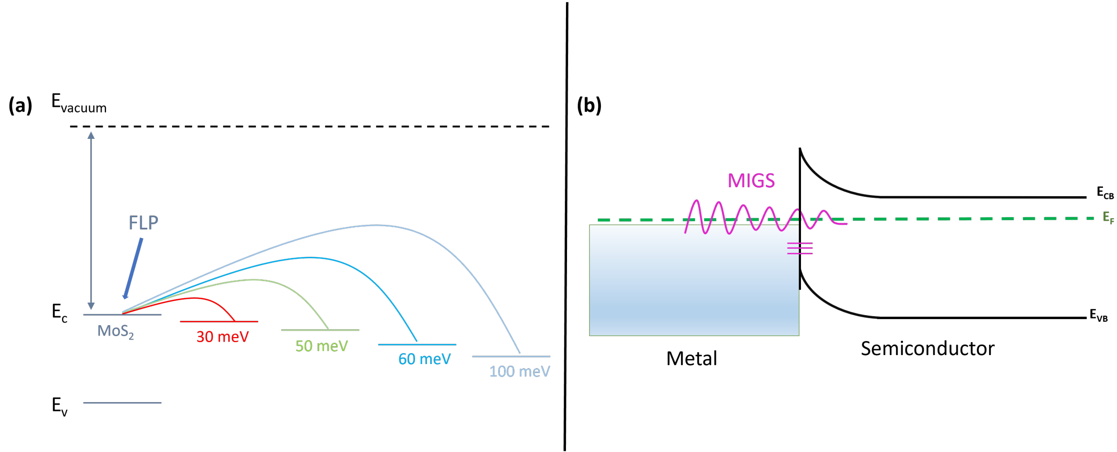


Figure 2.4: Fermi level pinning and metal-induced gap states. a) Energy diagram showing various Fermi levels pinned to a fixed location within the band gap of MoS_2. **b)** Schematic of metal-induced gap states in an M-S junction. Here, the metal electronic wave functions perturb the potential of the semiconductor, inducing gap states at the interface, shown as pink horizontal lines.

To account for FLP, the Schottky barrier height is instead estimated by introducing a pinning factor (S) and charge neutrality level (CNL) to expand the Schottky-Mott rule. The equation is modified as

$$\phi_B = S(\phi_M - \phi_{CNL}) + (\phi_{CNL} - \chi) \tag{2.4}$$

where $S = \frac{d\phi_B}{d\phi_M}$ is the pinning factor, χ is the electron affinity, and $\phi_{CNL} = \frac{\chi+b}{1-S}$ is the charge neutrality level [44]. A strong Fermi level pinning is associated with $S = 0$ and a weak or no pinning effect when $S = 1$.

It is proposed that the main cause of FLP originates from metal-induced gap states (MIGS). When a metal and a semiconductor come into close proximity, the potential of the semiconductor is perturbed by the metal, Fig.2.4b. The wavefunction mismatch from the penetration into the semiconductor alters the electronic states at the interface and induces these gap states. The metal wave function penetration decays exponentially in the semiconductor, resulting in localized gap states near the interface [45] [46].

It is evident that a rectifying behaviour and Schottky barrier are not desired in the context of fabrication of low-resistance contacts for 2D-FETs. As stated in the

introduction, much research has been devoted to mitigating the MIGS, Fermi-level unpinning and lowering of the SBH to break the performance bottleneck of 2D-FETs.

What's more, the laws of physics set a limit at which the contact resistance cannot go below. Quantum physics constrains the contact resistance of reaching below this limit. The quantum limitation of contact resistance in a junction can be expressed as

$$R_{c,min} = \frac{h}{2q^2} e^{2k_0 d} \sqrt{\frac{\pi}{2n_{2D}}} \tag{2.5}$$

where q is the charge, n_{2D} is carrier concentration, and h is Planck's constant, k_0 is a decay constant, and d is the size of the gap [42]. It is evident in the equation that the quantum limit is dependent on the charge carrier concentration in the channel.

2.3 Electrical characterisation and benchmarking of key transistor parameters

This section outlines the theory of electrical characterisation and key parameter extraction techniques used in this work and commonly used for transistor performance evaluation and comparison. In the context of this thesis, the most relevant performance evaluation is the systematic electrical characterisation, i.e. *transfer*- and *output* measurements of the FET. They are collectively known as current-voltage (I-V) characteristics and are essential for quantitative and qualitative analysis of intrinsic and external semiconductor properties [47] .

The output characteristic curve is a measure of source-drain current (I_{DS}) as a function of source-drain voltage (V_{DS}), for various discrete values of gate voltage (V_{GS}). For small V_{DS}, the transistor acts as a linear resistor. The transfer characteristics entail measuring the I_{DS} as a function of applied V_{GS} at various discrete values of V_{DS}. When measuring I-V characteristics, it is common practice to sweep the voltages over both positive and negative values over an interval sufficiently large to capture the behaviour and reveal hysteresis. For low power analysis, the V_{DS} sweeps are typically carried out between -1 and 1 V, and V_{GS} between -60 to 60 V.

Field-effect mobility reflects the sensitivity of the source-drain current response to gate voltage and is a measure of a charged particle's ease to move in a semiconductor in response to an applied electric field. Mathematically, it is derived from the transconductance in the linear regime of the transfer curve and is given by

$$\mu_{FE} = \frac{L_{ch} g_m}{W_{ch} C_{ox} V_{DS}} \tag{2.6}$$

where L_{ch} is the channel length, W_{ch} is the channel width, both of which are measured from the device structure [48]. g_m is the transconductance defined as $g_m \equiv \frac{\delta I_{DS}}{\delta V_{GS}}$, V_{DS} is the particular drain-source voltage at which the device is measured at, and $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the oxide capacitance.

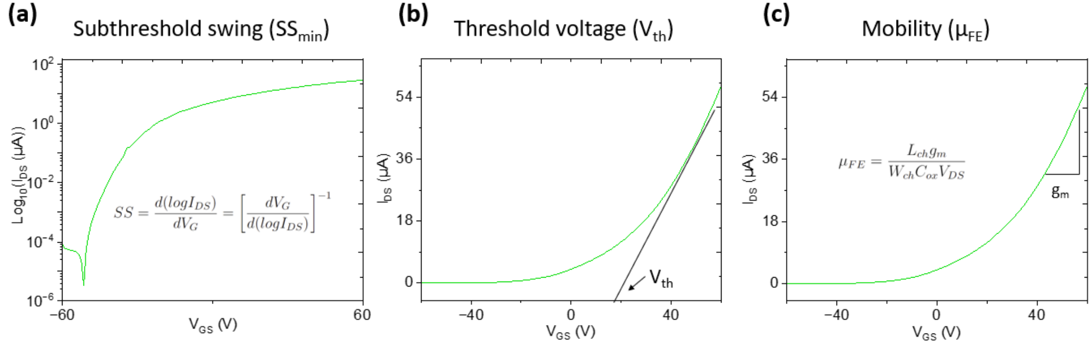


Figure 2.5: Key parameters. **a)** Typical logarithmic transfer curve to extract subthreshold swing. **b)** Linear transfer curve at a certain V_{GS} and linear extrapolation to extract V_{th}. **c)** Extraction of transconductance which corresponds to the slope of the linear region.

on/off-ratio (I_{max}/I_{min}) gives the ratio of the maximum on-state current and the minimum off-state current. I_{max} is obtained by recording the highest value of the logarithmic transfer characteristics curve at a constant source-drain voltage. I_{min} is defined as the minimum current and is obtained from the lowest value of the logarithmic transfer curve [47, 34]. It is desired to have a low OFF current to keep low standby power consumption, and a high ON current to ensure the right amount of power supply.

Sub-threshold swing (SS) is a measure of the switching performance of the device and is defined as the V$_{GS}$ required to increase the current by a factor of 10. It essentially gives information on the sharpness of the device switching between on- and off states. SS can be extracted from the slope of the log-linear portion of the transfer curve [49].
In theory, SS is governed by

$$SS = (1 + \frac{C_s}{Cb}\frac{kT}{q}ln10) \tag{2.7}$$

where C$_s$ is the capacitance of the semiconductor channel and C$_b$ is the body capacitance. Taking the limit of this equation results in

$$SS_{min} = ln(10)\frac{kT}{q} \tag{2.8}$$

which yields the fundamental thermionic limit of 60 mV/DEC at 300K for conventional MOSFETs. The limit arises due to the nature of the electron density of states (DOS) and the Fermi-Dirac distribution when applying a gate voltage [50].
In practice, however, SS is calculated by

$$SS = \frac{d(logI_{DS})}{dV_G} = \left[\frac{dV_G}{d(logI_{DS})}\right]^{-1} \tag{2.9}$$

where I_{DS} is expressed as $I_{DS} \sim e^{\frac{q(V_{GS}-V_{th})}{k_B T}}$ in the subthreshold regime ($V_{GS} < V_{th}$) [15].

Threshold voltage (V_{th}) is a key metric for performance evaluation, defined as the minimum applied gate voltage needed to induce a significant current flow from the source to the drain electrode. In the case of an n-type enhancement mode MOSFET, this occurs when applying a positive gate voltage until an inversion layer is fully connected between the source and drain. Threshold voltage is an important parameter as it quantifies at which voltage the device turns on and allows current to flow. Various extraction methods exist but the most common one is to use the value at the X-axis intercept from a linear extrapolation of the transfer characteristics curve in the linear region as shown in Fig.2.5b [34].

A common method to analyze the nature of the contact junction is to obtain the *Schottky Barrier height* (SBH). The most prevalent method for SBH extraction is the Arrhenius technique which entails temperature-dependent output or transfer characteristic measurements. In a 2D-FET contact junction, the charge carrier injection is mainly due to thermionic emission (TE) and tunnel transport. In thermionic emission, injection occurs due to electrons gaining sufficient thermal energy to overcome the potential barrier while tunnel transport instead occurs due to quantum tunnelling through the potential barrier, depicted in Fig.2.6a. Tunnelling transport is further split into thermionic field emission (TFE) and field emission (FE). In the off-state of a 2D-FET, thermionic emission dominates and the current is expressed according to

$$I_{DS}(V_{GS}) = A^* T^{3/2} e^{\frac{-q\phi_{B,eff}(V_{gs})}{k_b T}} [1 - e^{\frac{qV_{DS}}{k_b T}}] \tag{2.10}$$

where $A^* = q(8\pi k_b^3 m^*)^{0.5}/h^2$ is the Richardson's constant, q is elementary charge of an electron, T is temperature, and $\phi_{B,eff}$ is the effective potential barrier, and h is Planck's constant [7, 15]. I_{DS} is then plotted as a function of temperature in an Ahrrenius plot ($\ln(I_{DS}/T^{3/2}) \sim 1000/T$) for various V_{DS} [7, 12] such as shown in Fig.2.6b.

The effective potential barrier is extracted by linear fit of the Arrhenius curves and expressed as

$$\phi_{eff}(V_{GS}) = \frac{k_B}{q} \left[\frac{\Delta ln(I_D(V_{GS}/T^{3/2}))}{\Delta T^{-1}} \right]. \tag{2.11}$$

where the potential barrier is obtained by the slope of the Arrhenius plots. Lastly, the effective barrier ϕ_{eff} is plotted as a function of V_{GS} as shown in Fig.2.6c. The curve is linear in the thermionic emission region until the flat-band condition ($V_{GS} > V_{FB}$) is met. At gate bias exceeding flat-band voltages ($V_{GS} > V_{FB}$), TFE is the dominating current transport which emerges as a deviation from the linear gate dependence. The effective potential barrier ϕ_{eff} is equal to the Schottky barrier ϕ_{SB} at the kink at which this deviation occurs and so the value for the SBH is obtained [51].

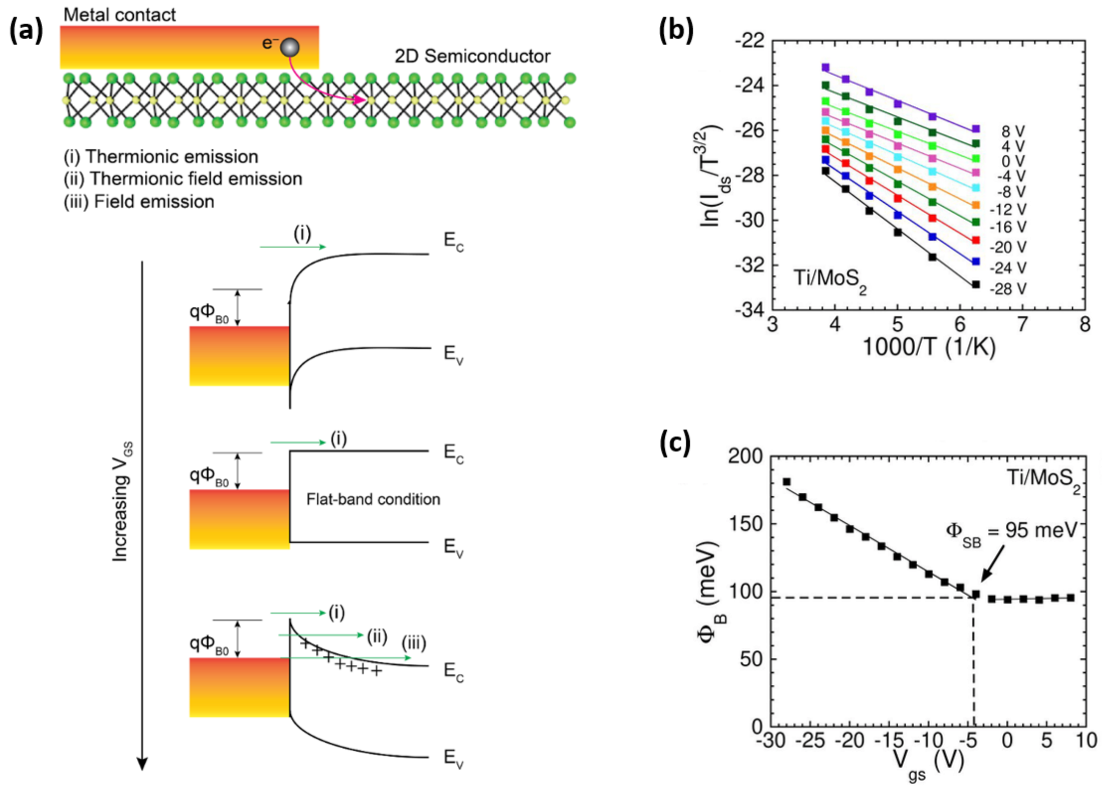


Figure 2.6: Charge carrier mechanisms and extraction of Schottky-barrier height at flat-band voltage. a) Charge carrier injection mechanisms at various voltage regimes, (Thermionic emission (TE), Thermionic field emission (FTE), Field emission (FE)). **b)** Typical Arrhenius plot for various voltages. **c)** Effective potential barrier expressed in meV as a function of applied gate voltage. The actual SBH is extracted at the flat-band voltage, where the curve deviates from its linear dependence on gate voltage. The figure is adapted from [15].

The V_{GS}-dependent contact resistance R_C between a metal and 2D semiconductor can be assessed by various methods, one being the *Transfer length method (TLM)*. A schematic of the measurement setup is shown in Fig.2.7a and the process is as follows. Contacts of varying interspacing are patterned for example by lithography. The total resistance R_{tot} between a pair on contacts spanning one channel is then given by

$$R_{tot} = \frac{R_{sheet}}{L} d + 2R_C \tag{2.12}$$

where R_{sheet} is the channel sheet resistance, L is the width of the contacts, d is the spacing between the contacts, and R_C is the contact resistance. R_{tot} is plotted against varying and equidistant increasing of contact spacing d. As d increases, so does R_C and R_{tot}, resulting in a linear relation such as shown in Fig.2.7b. From this graph, three parameters can be extracted; transfer length L_t, contact resistance R_C, and sheet resistance R_{sheet} [52].

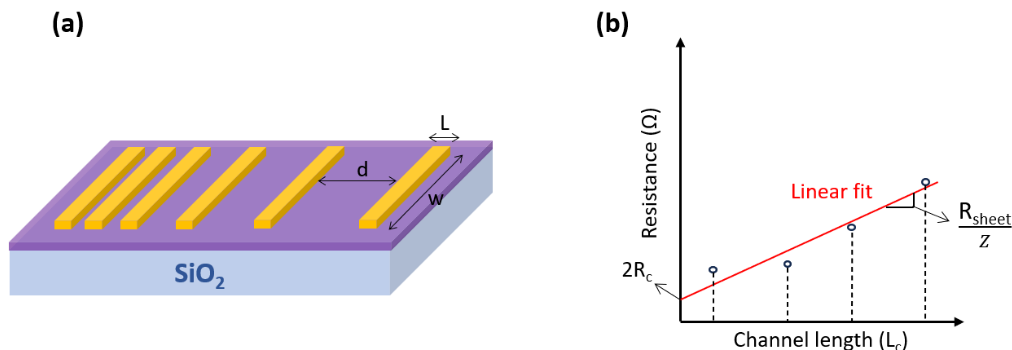


Figure 2.7: Geometrical structure for TLM measurement. a) Contacts with varying spacing are patterned on the channel material on the substrate. **b)** A typical graph of TLM measurement. The y-axis intercept of the linear fit gives $2R_C$ and the slope gives the R_{sheet}.

The device performance is heavily dependent on the number of channel material layers. Channel thickness is therefore a critical parameter for device evaluation and comparison. The atomic scale height profile of a 2DM channel can be assessed by *Atomic force microscopy* (AFM). In this work, AFM tapping mode was used for all height profile analyses.

2.4 Two-dimensional semiconducting materials

2.4.1 Molybdenum disulfide (MoS_2)

Molybdenum disulfide (MoS_2) is a two-dimensional semiconductor material that falls under the category of transition metal dichalcogenides (TMDs). It primarily exists in two crystalline phases, namely trigonal prismatic (2H) and octahedral (1T) Fig.2.8a-c. H and T correspond to hexagonal, and tetragonal symmetries, respectively, with the numbers indicating layers in a unit cell. The properties of MoS_2 are significantly influenced by its phase; for instance, trigonal prismatic MoS_2 exhibits semiconductor characteristics, while tetragonal MoS_2 displays metallic behavior [11].

2H-MoS_2 are structurally intralayer covalently hybridized orbitals of p_z and d orbitals coming from Sulfur and Molybdenum atoms respectively. Covalently bonded S-Mo-S atoms are stacked in lattice planes with lattice constant a = 3.16 Å and c = 12.8 Å. 2H-phase means that each Mo atom is bonded to six Sulfur atoms, forming a hexagonal lattice structure. Each adjacent layer which is approximately 0.7 nm thick, is held together vertically by van der Waals interactions. Van der Waals force is a weak interaction and much like graphene, mono-layer MoS_2 can be isolated by for example mechanical or chemical exfoliation from bulk crystals. In bulk form, MoS_2 has an indirect energy band bap E_g of 1.23 eV, while mono-layer MoS_2 has a direct energy band gap of 1.8 eV. In contrast, other 2D semiconducting materials such as WS_2 and WSe_2 have mono-layer band gaps of 2.03 eV and 1.67 eV, respectively

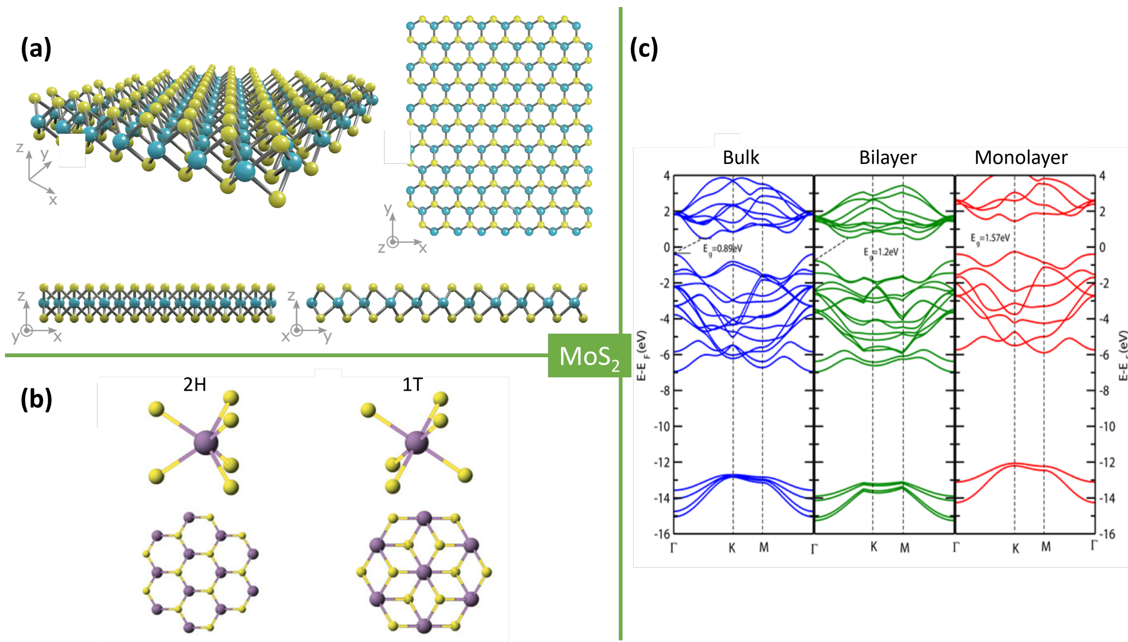


Figure 2.8: Crystal structure and band gap of MoS_2. a) Crystal structure of MoS_2. **b)** Semiconducting 2H-phase (stable) and metallic 1T-phase (metastable). **c)** Optical band gap of mono-layer, few-layer, and bulk MoS_2. Images are partly adopted from [11, 16, 17].

[53, 54]. The change in band structure is due to quantum confinement as a result of reduced dimensionality when layer thickness reaches mono-layer. Specifically, as MoS_2 bulk reduces towards mono-layer, the charge carriers are confined within a two-dimensional space and the conduction band minimum at a certain point in the Brillouin zone increases due to a decrease in interaction between electronic orbitals between Mo and S [38].

2.5 Theory regarding experimental procedure

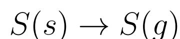
The purpose of this section is to explain the theory behind the fabrication steps and working principle of each instrument used throughout this work. Electron-beam lithography (EBL), electron beam physical vapour deposition (EBPVD), atomic force microscopy (AFM), AutoCAD, and exfoliation will be reviewed in the context of 2D-FETs.

2.5.1 Electron-beam lithography

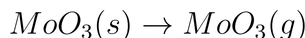
Electron Beam Lithography (EBL) is a key instrument in nano-device fabrication. EBL uses a stream of electrons to draw predefined patterns on a substrate with extremely high precision and resolution in the nm scale [55]. The substrate to be patterned is coated with an electron-sensitive polymer resist prior to exposure to the electron beam. When incident 50-100 kV electrons interact with the polymer they either strengthen or break the molecular bonds which result in an increased or decreased solubility, depending on the polymer type. The electron beam is typically generated by thermionic emission or field emission and is then directed with magnetic lenses, allowing very precise control. The minimum time to expose a given area on a substrate is governed by $D \times A = T \times I$, where A is the area, D is the dose, I is current, and T is the time of exposure. The particular EBL instrument used in this project is the JEOL JBX-9300FS [56].

2.5.2 Chemical vapor deposition

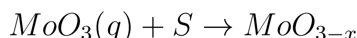
There are several state-of-the-art methods for material nucleation and growth on substrates, in which chemical vapour deposition is one of the most common in nanofabrication [57]. It is a vacuum deposition method where two precursors are vaporized by heating, and are then injected into a vacuum chamber where they chemically react and coat the target substrate.
The CVD process of growing few-layer MoS_2 on a substrate is essentially a chemical reaction between Molybdenum trioxide (MoO_3) and sublimed Sulfur (S) and follows the following chemical reaction formula



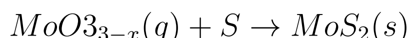
$$S(s) \rightarrow S(g)$$



$$MoO_3(s) \rightarrow MoO_3(g)$$



$$MoO_3(g) + S \rightarrow MoO_{3-x}$$



$$MoO3_{3-x}(g) + S \rightarrow MoS_2(s)$$

[58] [59] [49].

2.5.3 Exfoliation

The first exfoliation in a scientific setting was as early as the 1800's. However, the real turning point came in 2004 when Geim and Novoselov isolated graphene using mechanical exfoliation [60]. It is a surprisingly simple method where the fact that

layers held together by a weak van der Waals force is utilized to obtain thin layers of graphene or any van der Waals material by repeated peeling with adhesive tape. Even though it is the go-to method in fundamental research for growing pristine, high crystalline, clean mono, bi, and few-layer MoS_2 it is not suitable for industrial use, due to the small flake size, uncontrollable thickness, and incompatible with large scale production [61].

2.5.4 Electron-beam physical vapour deposition

Electron-beam physical vapour deposition (EBPVD) is a thin-film deposition process that uses a high kV electron-beam in vacuum to deposit an ultra-thin coating of metals on substrates. The EBPVD system requires a low vacuum and an applied B-field to guide the electrons to the metal target anode. The e-beam is generated by thermionic emission or field emission and upon striking the target anode, high-energy collimated electrons collide and kinetic energy is converted mostly to heat, causing the metal to sublimate. The gaseous phase then cools down and precipitates, coating the whole chamber and the substrate with a uniformly thick layer of the metal [62].

2.5.5 Atomic force microscopy (AFM)

The height profile of an ultrathin channel can be assessed by *Atomic force microscopy (AFM)*. A cantilever is employed to record forces and produce detailed topological images. The cantilever has a sharp tip that oscillates at a specific frequency, tapping the surface of the sample as it scans, allowing high-resolution imaging of the surface topography.

2.5.6 AutoCAD

Computer-aided design (AutoCAD) is a software used to prepare technical drawings. In the context of this thesis, AutoCAD is used to design the device contact patterns that are converted and communicated to the electron beam lithography instrument as a blueprint. The template for the substrate reference points used throughout this project was created in 2018 by Andre Dankert at Chalmers.

3
Device fabrication

Ultraclean conditions must be maintained while fabricating nano-devices. Even the tiniest dust particle can damage or degrade the performance of the device. Therefore, it is essential that nano-devices are fabricated inside cleanroom facilities. The cleanroom minimizes the presence of airborne particles and regulates factors like air purity, humidity, and temperature. This thesis project was largely carried out in the MC2 cleanroom at Chalmers, which has the classification Fed. Std.209 E Class (10-100) and ISO 14644-1 Class (4-5).

This section contains the chronological workflow of the fabrication steps as well as the measurement process. An exhaustive and detailed step-by-step explanation of the fabrication process can be found in the appendix.

3.1 Exfoliated few-layer MoS_2-FET with Gd & Bi contacts

Thin layers of MoS_2 are peeled from a bulk crystal by using Kapton tape. The thin layer is repeatedly exfoliated until mono, bi, few layers are obtained. MoS_2 is then transferred from Kapton tape to Si/SiO_2 substrate by using Polydimethylsiloxane (PDMS) tape according to Fig.3.1. The chips were then manually raster scanned in an MX50 microscope to select the most pristine few-layer flakes.

Contacts were designed in AutoCAD for the best quality MoS_2 flakes. The chips were then spin-coated with positive resist twice and soft-baked twice. The thickness of the resist is inversely proportional to the square root of the spinning speed which means that the parameters can be adjusted to yield an arbitrary thickness. Subsequently, EBL was performed to pattern the contacts. The exposed substrate had a positive resist coating which means that the EBL effectively increases the solubility of the polymer resist upon exposure. EBL was followed by development in n-Amyl Acetate and MIBK IPA 1:1 to remove any unwanted resist layer.

For the gadolinium device 35 nm Gd, 20 nm Ti, and 35 nm Au were deposited by EBPVD, and 80 nm Bi, 20 nm Au for the bismuth device. Titanium is deposited between gold and gadolinium to assist the poor adherence of gold. PVD was followed by lift-off in Acetone and cleaning in IPA. At this stage, the sample is ready to be taken out of the cleanroom for wire bonding and electrical characterisation. The complete fabrication workflow is shown in Fig.3.2 and detailed in the appendix.

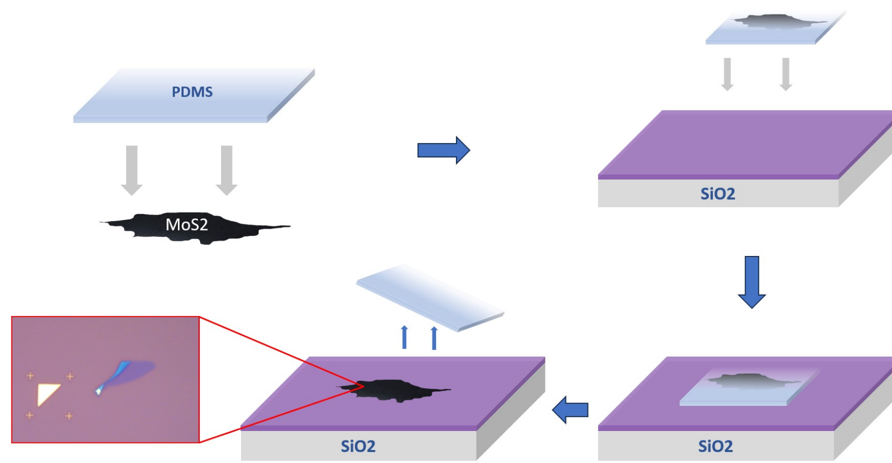


Figure 3.1: Exfoliation and transfer of MoS_2. A Polydimethylsiloxane (PDMS) is placed with the sticky side onto bulk MoS_2 and gently rubbed to allow MoS_2 to adhere to the surface. This process is done repeatedly to obtain few-layer sheets. The PDMS with MoS_2 attached is placed onto the SiO_2 substrate and gently rubbed. Lastly, PDMS is carefully and slowly removed and few-layer MoS_2 is transferred to the SiO_2 substrate.

A summary of the two device structures is shown in Fig.3.3a,b.

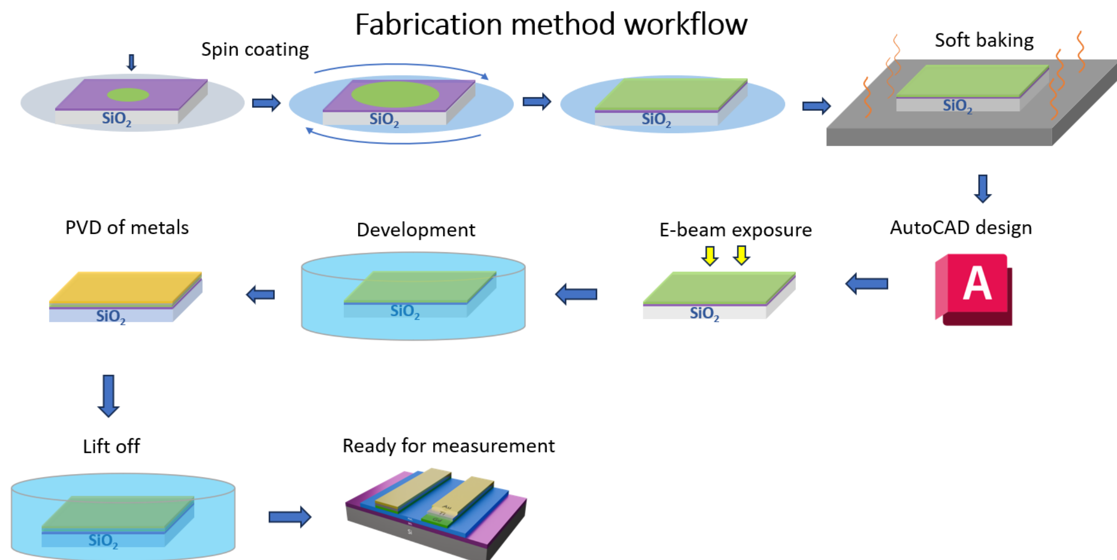


Figure 3.2: Workflow of fabrication method. The substrates are first spin-coated to create a uniform positive resist layer. The soft baking ensures hardening of the resist. AutoCAD were used to design the contact blueprints which were communicated with JEOL EBL for exposure. Development is done to reveal the EBL patterning. PVD is used to deposit Ti, Au, Gd, and Bi. Lift-off is performed in Acetone to remove unwanted metals. The device is then taken out of the cleanroom for transistor measurements.

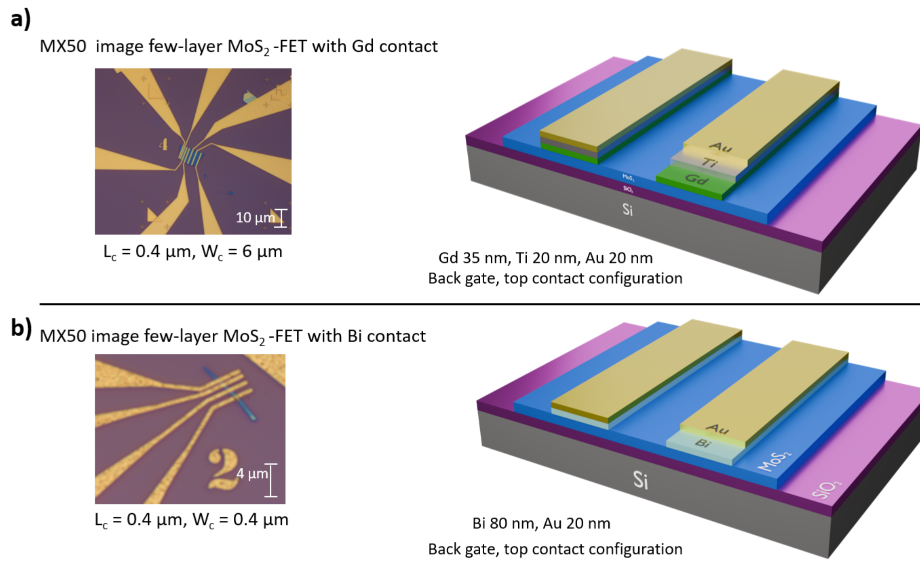


Figure 3.3: Complete device structures. a) Complete structure of MoS_2-FET with gadolinium contacts. The device has a back-gate, top contact configuration with channel length and width of 0.4 μm and 6.0 μm, respectively. **b)** Complete structure of MoS_2-FET with bismuth contact. The device has a back-gate, top contact configuration with channel length and width of 0.4 μm and 0.4 μm, respectively.

3.2 Measurement method of 2D-FET devices

Once a device is fabricated, it has to be bonded prior to any measurement to create conductive connections from the device to the chip carrier that is compatible with the measurement system. Each contact is bonded to an individual pad using a 25 μm Au wire on the chip carrier manually using a wire bonding machine. A schematic of the device mounted on the chip carrier is shown in Fig.3.4a. The chip carrier containing the chip is then mounted for measurement. The device's transistor properties were measured under vacuum and room temperature using a Keithley probe station controlled with Labview. A measurement is performed as follows; The contacts are first run through a preliminary check to verify which ones show switching behavior and which do not. This is typically done by applying a gate-dependent voltage V_{GS} for some source-drain voltage V_{DS} value over all contacts of the device sequentially while measuring source-drain current I_{DS}. The devices that show transistor behaviour are then measured by sweeping V_{GS}, holding V_{DS} constant for various discrete and increasing values while measuring I_{DS}. Then, a V_{DS} is applied, holding V_{GS} constant for various and increasing discrete values while measuring I_{DS}. Each sweep is carried out in a negative and positive voltage direction to reveal any hysteresis caused by trapped sites at the SiO_2/MoS_2 interface. All devices in this work has a back-gate structure, with the substrate serving as ground. A circuit diagram of the measurements is shown in Fig3.4b.

The temperature dependence measurement is carried out in the same manner as the systematic measurements described above while adjusting temperatures between 100K and 300K. To assess the height profile, i.e. thickness of the channel, AFM is used.

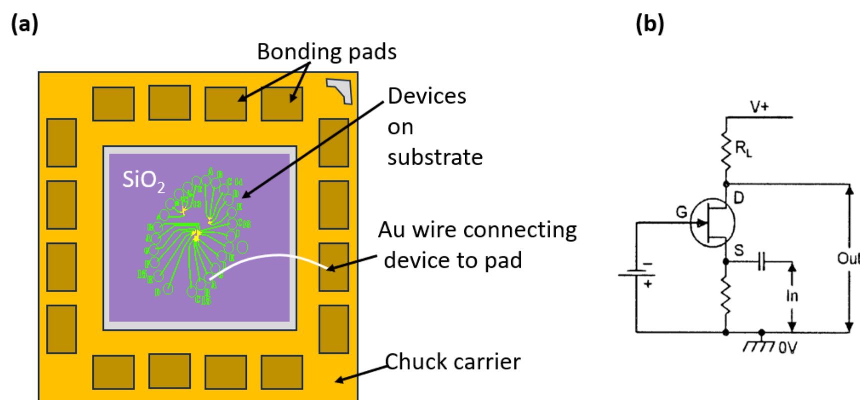


Figure 3.4: Measurement setup and circuit diagram. **a)** Device on SiO_2-substrate mounted on chuck holder. The substrate is attached to the holder by Ag-paste, and each contact is then bonded by 25 μm gold wire to each bonding pad. **b)** Circuit diagram for electrical measurements.

4

Results

Herein, field-effect transistors were fabricated utilizing exfoliated few-layer TMDCs as ultrathin channels on Si/SiO_2 substrates. Combined with this configuration, various contact engineering approaches have been investigated. Transistor performance was evaluated by basic transport measurements at different temperatures, and height profile was assessed by AFM. In this section, the measurement results and calculation of key parameters are presented separately for each device. All data were processed with Labview and analysed in OriginLab Pro 2024.

4.1 *I-V* characteristics of Exfoliated few-layered MoS_2-FET with Gd contacts

Contact engineering by low work function metals has been well-studied due to their ability to lower the SBH. Very recently, gadolinium was reported to show good contact behaviour on exfoliated MoS_2-channels. This section presents results from a few-layer MoS_2 device with gadolinium as contact material.

Exfoliated few-layer MoS_2 with Gd/Ti/Au contacts were fabricated on a 290 nm Si/SiO_2-substrate as described in the fabrication section and detailed in the appendix. An optical image of the device is shown in Fig.4.1a. In this top-contact configuration, the exfoliated few-layer MoS_2 flake acts as the ultra-thin channel material and is $\approx$ 20 nm thick measured by AFM, Fig.4.1b,c.

The fabricated FET effectively operates in depletion mode. Gd/Ti/Au acts as contact materials and are approximately 35, 20, and 20 nm thick, respectively. The channel length and width are 0.4 μm and 6.0 μm. Measurements were carried out at 300 K under vacuum conditions, using Si-substrate as back-gate and ground. Device performance evaluation was done by electrical characteristic measurements using a Keithley 2612b channel source meter as described in the previous chapter. The current-voltage characteristics at 300 K are shown in Fig.4.2. The transfer curve (I_{DS}-V_{GS}) were obtained by a gate voltage sweep between [-60,60] V in increments of 1 V, for a total of ten equidistant source-drain voltage sweeps between 0.1 and 1 V. The voltage sweeps were carried out in both negative and positive directions to reveal any hysteresis. At room temperature, there was an asymmetrical shift in current from negative to positive sweep, which is attributable to the effects of hysteresis. The origin is likely due to charged trap sites at the SiO_2/MoS_2-interface that delays gate-capacitance [63]. The resulting transfer curves are shown in linear

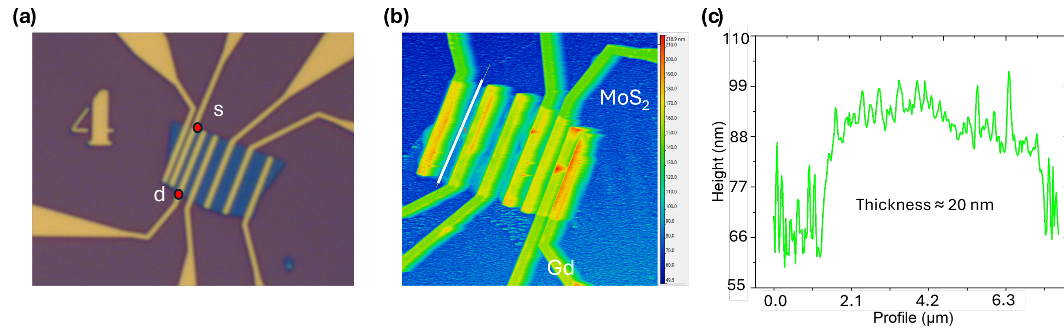


Figure 4.1: Height profile analysis by AFM. a) MX50 Optical image of the device. The source and drain are marked with red dots. **b)** AFM height profile image. The white line indicates where the height profile has been assessed. **c)** AFM height analysis shows a channel thickness of ≈ 20 nm.

and logarithmic scales in Fig.4.2b and Fig.4.2e.

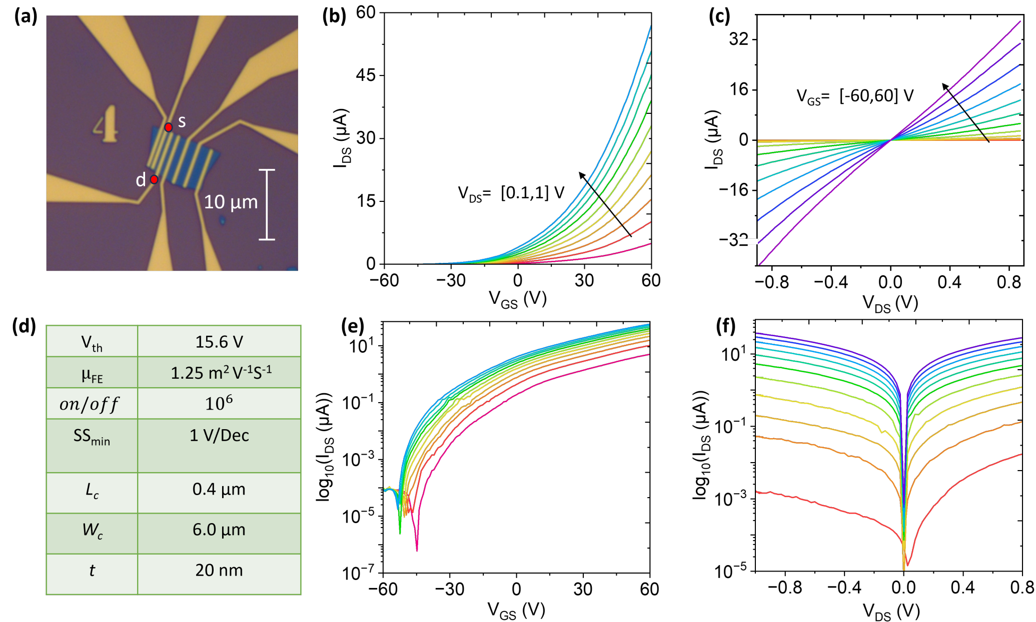


Figure 4.2: Electrical measurements of exfoliated MoS_2-FET with Gd contacts. a) MX50 optical image of the device. Transistor properties are measured between the source and drain marked 's' and 'd'. **b)** Transfer characteristics in linear scale measured between $V_{GS} = [-60, 60]$ V for $V_{DS} = [0.1, 1]$ V in steps of 100 mV. The maximum current is around 60 μA. **c)** Output characteristic curve for various V_{GS} in linear scale. **d)** Summary of extracted parameters. L_c is channel length, W_c is channel width, and t is flake thickness. **e)** Transfer curve in logarithmic scale for V_{DS} between 0.1 V and 1 V and **f)**, output curve in logarithmic scale.

The logarithmic transfer plot emphasizes the subthreshold region, i.e. the off state of the device. In contrast, the linear transfer plot highlights the device behaviour

above the threshold voltage. Regarding Fig.4.2b, at $V_{GS} < V_{th}$, the current is low and the device is in its off-state, referred to as the subthreshold region. In this region, thermionic emission is the dominating charge carrier injection mechanism for overcoming the potential energy barrier at the source-channel interface. As V_{GS} approaches V_{th}, current is observed to increase exponentially. This behaviour can be attributed to the Boltzmann distribution of the charge carriers. The electron density in the MoS_2-channel is proportional to gate voltage according to $n \propto e^{q\frac{(V_{GS}-V_{th})}{kT}}$, where k is Boltzmann's constant and q is the elementary charge. The relation between n and V_{GS} shows exponential dependence in the subthreshold region. Since the I_{DS} is proportional to n, the current is also increasing exponentially. Above V_{th}, I_{DS} exhibits a linear V_{GS}-dependence. If V_{GS} is increased even further, current would reach a saturation region, showing less response to gate voltages.

As is evident from the transfer curves, the device exhibits n-type characteristics meaning that the Fermi-level lines up close to the conduction band of the MoS_2 and thus electrons are the majority charge carriers. The n-type behaviour can likely be attributed to S orbital vacancies. Here, a clear on an off state is observed, with on/off-ratio $\approx 10^6$, obtained by $I_{max} = 10^2$ μA and $I_{min} = 10^{-4}$ μA at $V_{DS} = 1$ V from the logarithmic transfer curve. The threshold voltage $V_{th} \approx 22$ V at $V_{DS} = 1$ V was extracted by linear extrapolation method of the transfer curve with corresponding carrier density $n = C_{ox}\frac{V_{GS}-V_{th}}{q}$ of $\approx 1.57 \cdot 10^{12}$ cm^{-3}. $V_{th} > 0$ further proves n-type characteristics. Field-effect mobility at $V_{DS} = 1$ V is 1.25 $m^2/V \cdot s$ using equation 2.6, where transconductance is $g_m \approx 2.26 \times 10^{-7}$ A/V at $V_{DS} = 1$ V. The sharpness of the switching characteristics, measured as SS_{min}, was obtained by the slope of the logarithmic transfer curve and equation 2.9 and is ≈ 1 V/Dec. In this context, a low SS is desirable to achieve high efficiency.

The output characteristics were obtained by sweeping source-drain voltage between $V_{DS} = [-1, 1]$ V, holding gate voltage constant for values between $V_{GS} = [-60, 60]$ V in discrete increments of 10 V, shown in linear and logarithmic scale in Fig.4.2c, f. The nature of the $I_{DS} - V_{DS}$ curves are used to evaluate the quality of the contact between MoS_2 and gadolinium electrodes. In an ideal case, the junction is of ohmic behaviour and can facilitate efficient charge transfer. In Fig.4.2c, I_{DS} increases linearly at low drain voltage bias for $V_{GS} = [-60, 60]$V, indicating ohmic contact behaviour. At sufficiently high drain bias, the device would likely saturate. The symmetrical nature of the curves for negative and positive voltages indicates uniform charge transfer.

Temperature-dependent I-V measurements were carried out for the device ranging from 100 K to 300 K. $I_{DS}-V_{GS}$ curves at $V_{DS} = 1$ V are shown in linear and logarithmic scale in Fig.4.3b, c. As temperature increases from 100K to 300K, max current increases from 20 μA to 45 μA, showcasing typical semiconducting conductance-temperature dependence. The underlying physics behind the dependence can be understood by considering electronic bandstructure, DOS, and the Fermi-Dirac distribution. At low temperatures, fewer electrons have sufficient energy to break covalent bonds to jump from the valence band to the conduction band and therefore the current should decrease, as observed. What's more, V_{th} is shifted from 18 V to

35 V when decreasing temperature, owing to more carriers due to thermal activation.

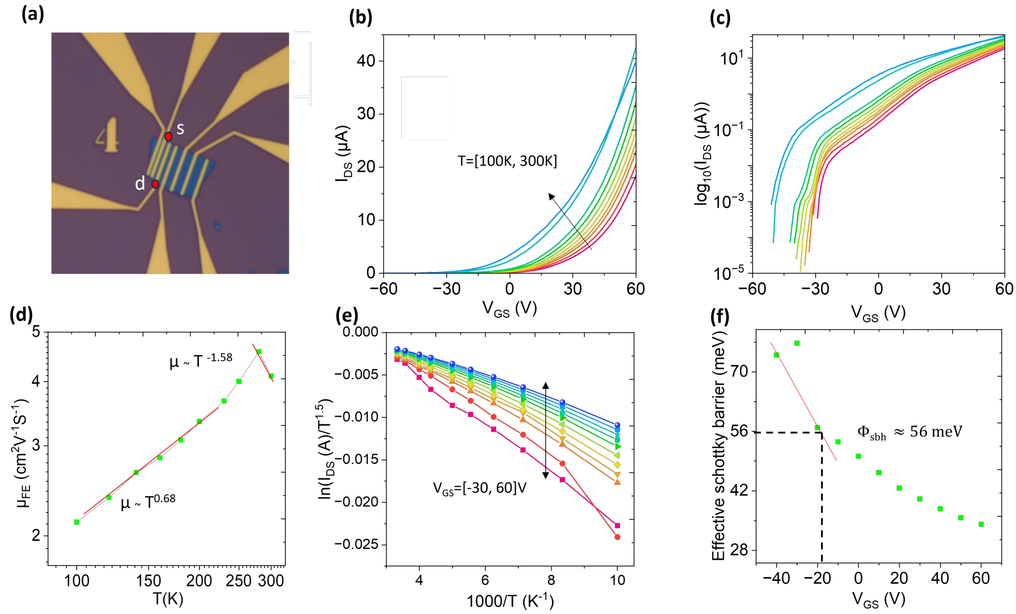


Figure 4.3: Extraction of Schottky barrier height (Φ_{SBH}) at flat-band condition and μ-T dependence. **a)** MX50 optical image of the device. **b)** Temperature-dependent tranfer characteristics measured at V_{DS} = 1 V for T= [100,300] K in linear scale and, **c)** logarithmic scale. **d)** Mobility μ_{FE} as a function of temperature. The positive mobility dependence on temperature between 100K to 250K is attributed to transport dominated by ionized impurity scattering. Above 250 K, mobility decreases due to phonon scattering. **e)** Arrhenius plot constructed according to the Arrhenius technique. **f)** Effective potential barrier as a function of gate voltage. $\Phi_{SBH} \approx 56$ meV is extracted at flat-band condition, where the curve deviates from linearity.

In Fig.4.3d, field-effect mobility μ_{FE} is observed to increase until a certain temperature, thereafter decreasing. The mobility at low temperatures is slightly larger than 2 $cm^2V^{-1}S^{-1}$, and peaks at 270 K around 4.5 $cm^2V^{-1}S^{-1}$. The dependence can be understood by considering scattering mechanisms in the semiconductor lattice. The positive $\mu-$T dependence from 100 K - 250 K observed is due to ionized impurity scattering. In this model, the thermal velocity of the charge carriers increases with temperature, which means that the duration at which an electron spends in close proximity to an ionized impurity decreases. The less time spent around an unbalanced local charge, the smaller the scattering time, and therefore should mobility increase with increasing temperature, if solely considering ionized impurity scattering. However, one cannot only consider this effect, for at T > 0K, atoms also vibrate about their relatively fixed position in the lattice due to thermal energy. Charge carriers interact with these vibrations in what is called phonon scattering. At increasing temperature, phonons naturally increase and thus also the probability for a scattering event, effectively decreasing mobility. The effect of phonon scattering comes into play at 270 K in Fig.4.3d, [5].

The thermionic emission model was used to extract Φ_{SBH} as described in the theory section [15]. The Arrhenius plot shown in Fig.4.3e is obtained for V_{GS} ranging from -30 V to +60 V in steps of 10 V. The slopes of each fitted curve in the Arrhenius plot are used to obtain the effective potential barrier dependence on gate voltage and are shown in Fig.4.3f. For gate voltages below the flat-band voltage ($V_{GS} < V_{FB}$), calculations show a negative and linear SB with V_{GS}, as expected for n-type FETs. As the gate voltage increases and exceeds the flat-band voltage ($V_{GS} > V_{FB}$) (i.e the situation at which the conduction band is exactly aligned with the SBH) then the effective barrier $\Phi_{eff} = \Phi_{SBH}$ and the deviation from linearity occurs, just as explained in the theory section. For this device, Φ_{SBH} is $\approx$ 56 meV at flat-band condition of $V_{FB} \approx 2$ V. The low Schottky barrier is similar to previously reported results and is attributed to the low work function of gadolinium [14].

4.2 *I-V* characteristics of exfoliated few-layered MoS_2-FET with Bi contacts

Recently, Semi-metals have attracted attention as contact material due to their ability to suppress metal-induced gap states. Previous studies have reported a variation of results, such as bismuth contacts on mono-layer MoS_2, WS_2, and WSe_2 with SBHs as low as 0 meV [64, 65, 66, 67]. However, investigation of Bi contacts with few-layer MoS_2 as well as detailed temperature-dependent studies is still missing. Therefore, few-layer MoS_2 with bismuth contacts has been explored and is presented in this section.

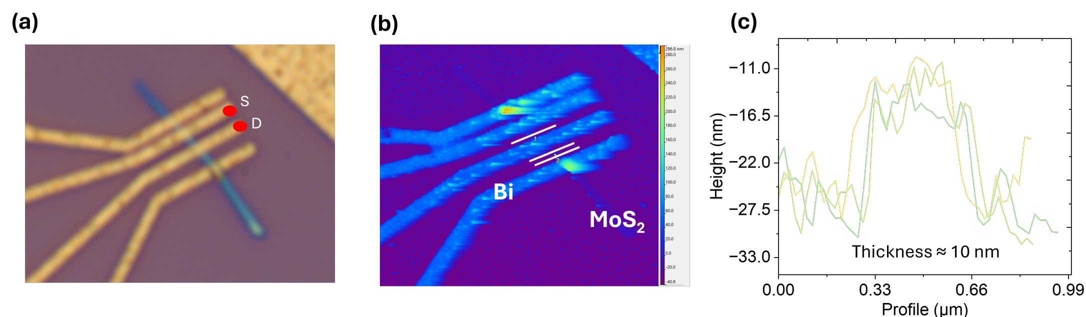
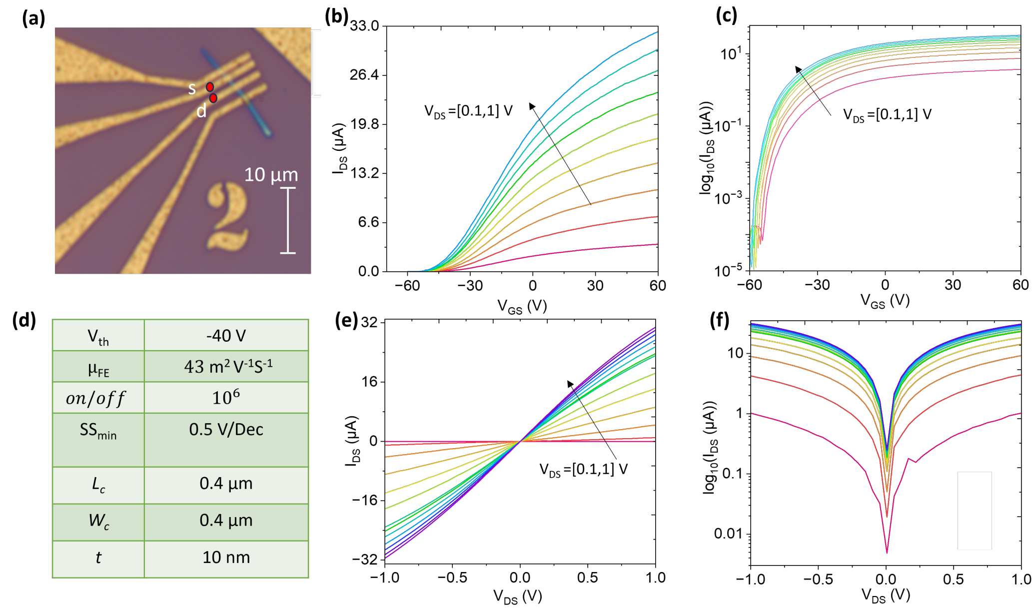


Figure 4.4: Height profile analysis by AFM. a) MX50 Optical image of the device. The source and drain are marked with red dots. **b)** AFM height profile image. White lines indicate where the height profile has been assessed. **c)** AFM height analysis showing a channel thickness of around 10 nm, i.e. ca 14 layers.

Exfoliated few-layer MoS_2-FET with Bi contacts on a 290 nm Si/SiO_2-substrate were fabricated and systematically evaluated in the same manner as the gadolinium device. The height profile was assessed by AFM and is $\approx$ 10 nm, Fig.4.4a-c. The channel length and width of the MoS_2 are both 0.4 μm, measured by alignment in

AutoCAD. The I-V characteristics of this device at 300 K are shown in Fig.4.5. The device exhibits excellent n-type transistor behaviour for both gate and drain bias. The exponential behaviour at negative gate voltages between [-50,-30] V can be attributed to Boltzmann distribution just like for the gadolinium transistor. At higher gate bias, the slope levels out and the current becomes relatively independent of gate bias, reaching a saturation point. At 300 K, this device has an on/off-ratio of 10^6, $V_{th} \approx -40$ V at $V_{DS} = 1$ V. Field-effect mobility μ_{FE} at $V_{DS} = 1$ V is $\approx$ 43 $cm^2/V \cdot s$ using eq 2.6. SS_{min} is $\approx$ 0.5 V/Dec, obtained by eq 2.9.



V_{th}	-40 V
μ_{FE}	43 $m^2 V^{-1} S^{-1}$
on/off	10^6
SS_{min}	0.5 V/Dec
L_c	0.4 µm
W_c	0.4 µm
t	10 nm

Figure 4.5: Electrical measurements at 300K of exfoliated MoS_2-FET with bismuth contacts. **a)** MX50 optical image of the device. The source and drain are marked with red dots. **b)** Transfer characteristics in linear scale measured between $V_{GS} = [-60, 60]V$ for $V_{DS} = [0.1, 1]$ V in steps of 100 mV. **c)** Transfer curve in logarithmic scale for V_{DS} between $[0.1, 1]$ V. **d)** Summary of extracted parameters. L_c is channel length, W_c is channel width, and t is flake thickness. **e)** Output characteristic curve for various V_{GS} in linear scale and **f)** logarithmic scale.

The output characteristics at room temperature, Fig.4.5e, show a linear increase of I_{DS} at low drain bias, indicating ohmic behaviour. In addition, low-temperature I-V measurements at 100 K were carried out and are shown in Appendix Fig.3, showing slightly less linear behaviour. Previous studies have reported similar transistor behaviour, however, for mono-layer channels.

Temperature-dependent I-V measurements were carried out at temperatures ranging from 100 K to 300 K. The Arrhenius plot in Fig.4.6e and the effective potential barrier gate voltage dependence in Fig.4.6f are obtained in the same manner as for the gadolinium device, i.e via the Arrhenius technique according to the thermionic emission model explained in the previous section. For this device, $\Phi_{SBH} \approx$ 43meV at

$V_{FB} \approx -20$ V, where the potential barrier-gate dependence deviates from linearity. Firstly, the low Schottky barrier of 43 meV for this few-layer MoS_2-configuration can be attributed to the fact that Bi has almost zero DOS at the CNP, so that gap states are greatly suppressed and no Fermi-level pinning can occur. Secondly, the fact that the output characteristics ($I_{DS}-V_{DS}$) in Fig.4.5e exhibit close to linear behaviour indicates a low or negligible Schottky barrier. Previous studies have reported zero or negligible SB and ultra-low contact resistance, however their work is focused on mono-layer flakes.

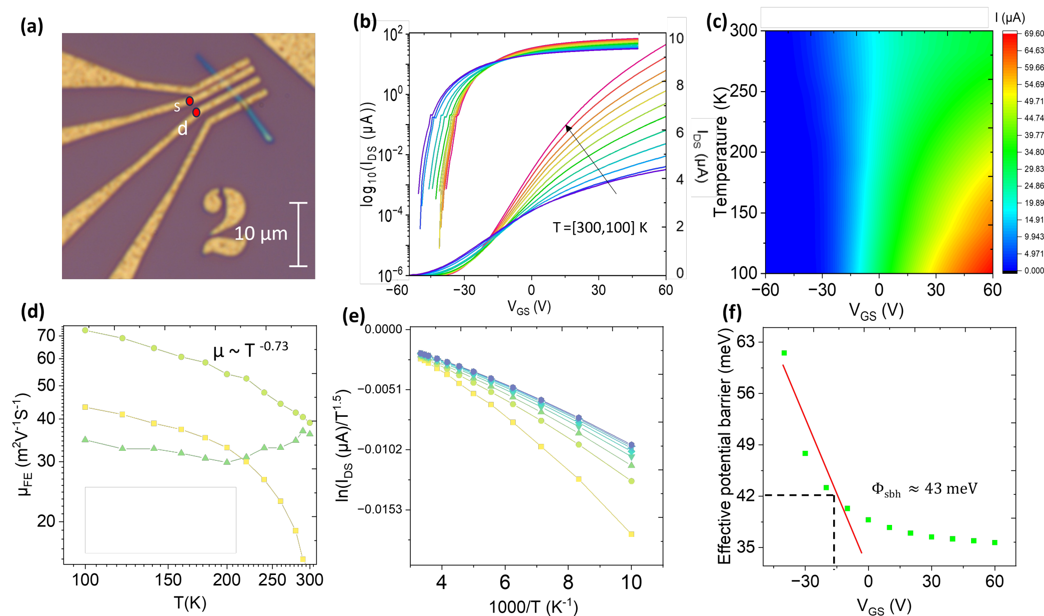


Figure 4.6: Extraction of Schottky barrier height (Φ_{SBH}) at flat-band condition and μ-T dependence. **a)** MX50 optical image of the device. Here, the source and drain are marked by 'S' and 'D'. **b)** Temperature-dependent tranfer characteristics measured at $V_{DS} = 1$ V for T=[100,300] K in linear scale and logarithmic scale. **c)** Contour plot of temperature, drain current, and gate bias. **d)** Mobility μ as a function of temperature T above, at, and below phase transition. Transconductance was extracted at [-35,-30] V below transition, [-30,-15] V at the transition, and [20,40] V above transition. **e)** Arrhenius plot constructed according to the Arrhenius technique. **f)** Effective potential barrier as a function of gate voltage. $\Phi_{SBH} \approx 43$ meV is extracted at flat-band condition.

To compare our estimated SBHs for Bi and Gd onto multi-layer MoS_2 with recently reported results, we have summarised previously estimated SBHs for various contact materials in Fig.4.7, where the red stars indicate our results. Our findings show that the SBH for Bi (43 meV) and Gd (56 meV) are relatively low compared to other contact materials such as W, Co, Ni, and Pt, which exhibit much higher SBHs. Notably, our estimated value for Gd is in a similar range to that reported by D. Wang et al.[14]. Interestingly, we found an SBH of about 43 meV for Bi with multilayer MoS_2, whereas Shen et al. [12] reported almost zero SBH for Bi. This discrepancy could be attributed to the FLP effect in our device.

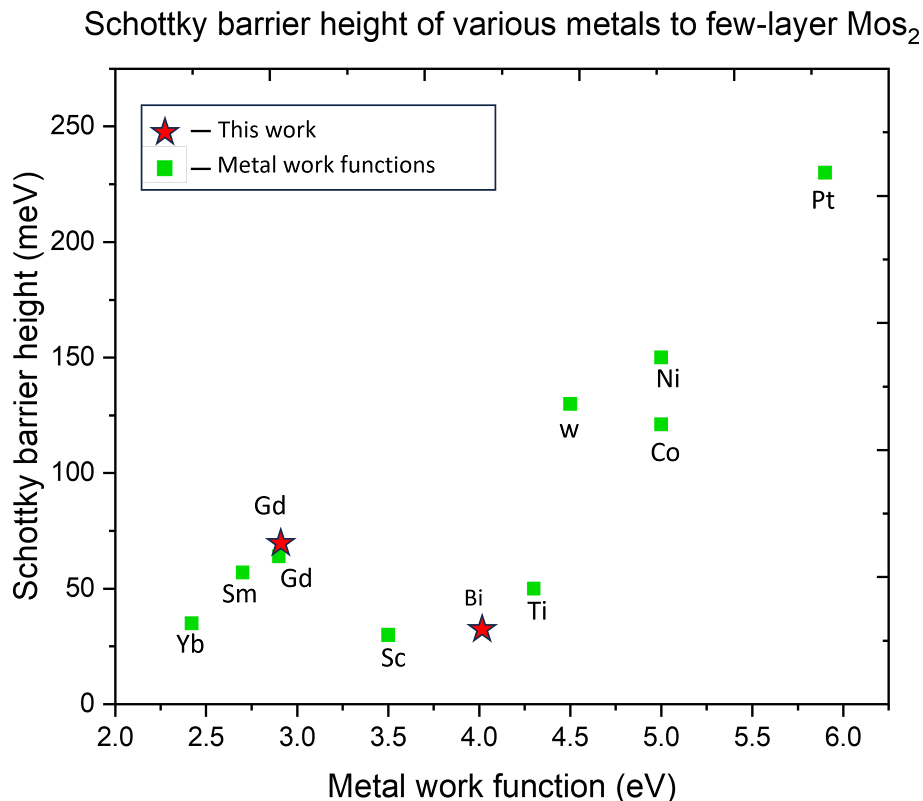


Figure 4.7: Schottky barrier height for multilayer MoS_2 devices. Previously reported values of SBH as dependent on work function. The red stars represent this work calculated SBH by thermionic emission model. Previously reported SBH are obtained from [18], [19], [20], [14].

$I_{DS} - V_{GS}$ curves at $V_{DS} = 1$ V ranging from 100K to 300K are shown in linear and logarithmic scale in Fig.4.6b. The maximum current is around 70 μA at low temperatures. Mobility as a function of temperature at, below, and above transition are shown in Fig.4.6d. Below transition at 100 K, $\mu_{FE} \approx 35$ $cm^2V^{-1}S^{-1}$, increasing to 40 $cm^2V^{-1}S^{-1}$ at 270 K, showcasing typical semiconducting behaviour. At and above transition, mobility is initially greater but seen to decrease with temperature. This behaviour is due to increased phonon scattering.

An interesting physical phenomenon can be observed at $V_{GS} \approx -15$ V. At charge carrier densities below the inflexion point in Fig.4.6b corresponding to $n_{crit} \approx 2.62 \cdot 10^{13}$ cm^{-3} for T = 100 K, MoS_2 exhibits expected semiconductor behaviour, i.e a positive conductance-temperature dependence. As carrier densities increase beyond n_{crit}, MoS_2 instead show negative conductance-temperature dependence. This is an indication that MoS_2 undergoes a gate-induced (electrostatic doping via gate) thermodynamic phase transition from semiconducting to metallic behaviour with regard to its electron transport mechanism. It can also be observed that n_{crit} and

thus the phase change depends on temperature. It is evident in the shift of the inflexion points towards lower gate voltages as temperature decreases. The transition is a well-studied phenomenon and is referred to as metal-insulator transition (MIT). In the insulating phase at $n < n_{crit}$, electron transport in MoS_2 might be explained by Mott 2D variable-range hopping (2D-VRH) model. In this model, electrons are subjected to strong localization potentials due to a disordered lattice as a result of impurities. Electrons are therefore hopping between strong localized potential puddles, unable to overcome the Coulomb interaction due to weak electron-electron screening, and MoS_2 behaves like an insulator. Above the phase transition, sufficient screening enables electrons to overcome the Coulomb interaction and weak localization dominates, allowing a percolation-driven electron transport which results in metallic behaviour. Note that this phase transition is not permanent because MoS_2 is not in equilibrium in its metallic state, and transitions back to semiconducting behaviour for gate bias below n_{crit}. A schematic of the electron transport is shown in figure Fig.4.8c.

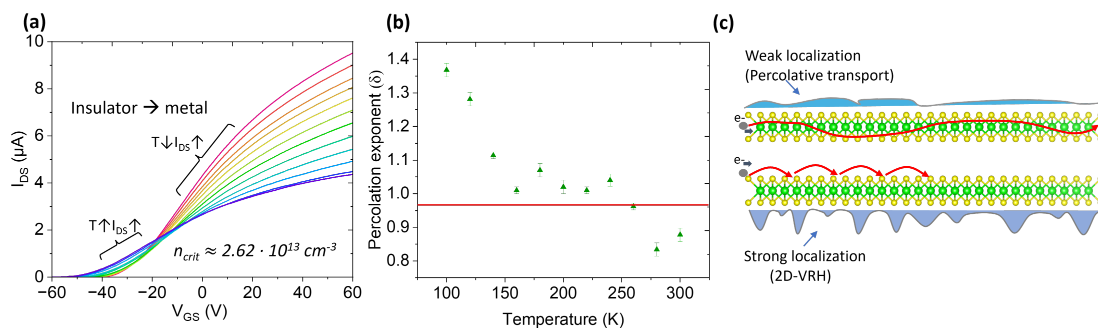


Figure 4.8: Metal-insulator transition. a) Temperature-dependent transfer curve, highlighting the insulator and metallic regions. The threshold for phase transition occurs at around -15 V, corresponding to $n_{crit} \approx 2.62 \cdot 10^{13}\ cm^{-3}$. **b)** Percolation exponent as a function of temperature. The red line is a mean value of $\delta \approx 1$. **c)** Schematic of variable-range hopping and percolative transport. At the insulating phase, VRH occurs due to strong localization and at metallic phase weak localization dominates, resulting in percolative transport.

To strengthen the hypothesis of a percolation-driven transport, a percolation exponent δ according to $\sigma(n) = (n - n_c)^{\delta}$ can be calculated for a given system. In theory, a 2D-system exhibits a transition if $\delta \approx 1.33$ [68]. The percolation exponent δ was calculated in this work and plotted against temperature in Fig.4.8b. The value is close to 1.33 which further confirms the hypothesis. MIT was observed in MoS_2 for bismuth but not for the gadolinium device. Since MIT is a characteristic of the MoS_2 channel, the number of layers, channel thickness and channel width might play a role in whether a transition happens. For the bismuth device, the channel was much narrower (0.4 μm compared to 6 μm) and the thickness was half that of the gadolinium device. The greater mobility coming from a thinner width might play a role in this transition. It should also be mentioned that this transition is not well understood yet, and there are other frameworks for explaining electron transport in

2D systems exhibiting MIT.

5 Conclusion

Over the past six decades, semiconductor technology has experienced an exponential boom, driven by the emergence of MOSFET and CMOS technology. The last decade, in particular, has seen significant advancements in the development of 2D field-effect transistors for next-generation nano-devices, aimed at extending Moore's law. Despite exciting advancements, the integration of two-dimensional materials in FETs has encountered numerous challenges that ultimately constrain the performance. These include difficulties associated with downscaling, poor carrier injection due to large Schottky barrier height (SBH) from the formation of MIGS and the effect of FLP at the contact interface, and obstacles in achieving large-scale integration, among others.

Therefore, the main aim of this thesis was to address one of these challenges by investigating the contact properties of gadolinium and bismuth on exfoliated MoS_2 as the ultrathin conductive channel. In achieving this goal, two contact engineering approaches have been explored; Firstly, work function engineering was implemented using the low work function metal gadolinium, realised by state-of-the-art fabrication and characterisation methods such as EBL, EBPVD, exfoliation, AFM, and systematic temperature-dependent measurements using vacuum probe stations. The device exhibited excellent transistor properties, linear I-V characteristics, and a low Schottky barrier, indicating promising contact behaviour. Secondly, a semimetal-semiconductor junction with bismuth as contact material was explored due to its near-zero density of states at the Fermi level. The fabrication and measurement techniques were otherwise identical to the gadolinium device. It was found that bismuth exhibits promising contact properties, I-V characteristics indicative of ohmic behaviour and a low Schottky barrier height consistent and comparable with previous reports. The information gathered from this project provides valuable insights into the challenges associated with contact formation and fabrication of nano-devices and might contribute to the existing body of research for next-generation semiconductor FETs.

Future work could focus on exploring device-to-device variability and investigating more scalable approaches to facilitate large-scale production and integration. One pathway could be to investigate large-scale growth models such as MOCVD, and device-to-device variability by fabricating a large number of devices to perform statistical analyses. What's more, recent reports have shown that 2DMs are able to achieve some functionalities required for neuromorphic computing, which would be an interesting topic to further explore [69]. Given the potential of 2D materials

to augment existing Si-CMOS technology, future research could also explore these aspects for CMOS integration. For example, since both n-type and p-type semiconductors are needed for CMOS technology, investigating p-type channels with gadolinium and bismuth could be an interesting study that has yet to be shown.

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Appendix

Fabrication of exfoliated MoS_2-devices

I. **Mechanical exfoliation of MoS_2.** The process of obtaining mono- to few-layer MoS_2 by mechanical exfoliation is as follows. One starts with bulk form of a MoS_2 crystal. A substrate is prepared on which the exfoliated flakes can be transferred. For this device, 290 *nm* Si/SiO_2 is used. A piece of adhesive tape is placed on the bulk MoS_2 crystal. As the tape is peeled off, thin layers of MoS_2 will adhere to the tape. The tape containing thin layers of MoS_2 is then repeatedly attached and peeled to several other tapes, with each exfoliation yielding thinner layers. This procedure was repeated 4-5 times. It is important to note here that obtaining high-quality mono-layer MoS_2 is a completely random process, it is not possible to know beforehand which peeling will be successful. It is therefore repeated several times to collect many samples. The MoS_2 layers are then transferred to a substrate by first transferring it to a PDMS tape, and then pressing the PDMS tape directly to the Si/SiO_2-substrate. This procedure was repeated around 20 times before just a few quality flakes were obtained.

II. **Spin coating and soft baking.** Spin coating and soft baking were done twice and subsequently as follows; The chip was transferred to the spin coating machine and carefully placed on the vacuum chuck, with a vacuum suction below 0,5 bar to make it stick. A pipette was used to distribute around 5 droplets of PMMA 8.5 EL8, followed by spin coating at 6000 rpm, acceleration of 3000 $rpms^{-1}$ for a duration of 60 seconds to create a 200 nm uniformly thick resist layer on the chip. The thickness of the resist is inversely proportional to the square root of the rotation speed and one can therefore select an arbitrary thickness by controlling rotation and acceleration. The chip was then softbaked at 150°C for 7 minutes. The procedure of spin coating and soft baking was repeated with the same parameters, using APR 6200 1:3 as the second resist layer.

III. **AutoCAD design of contacts.** AutoCAD was used to design the top contacts by drawing Polygons according to (Fig..1). The contacts are about 500 nm thick and are designed according to TLM geometry.

Next, the AutoCAD design was patterned onto the substrate by EBL exposure. First, the chip is loaded and the instrument is calibrated according to reference markers on the substrate. A beam of 50 keV electrons exposed the resist for a

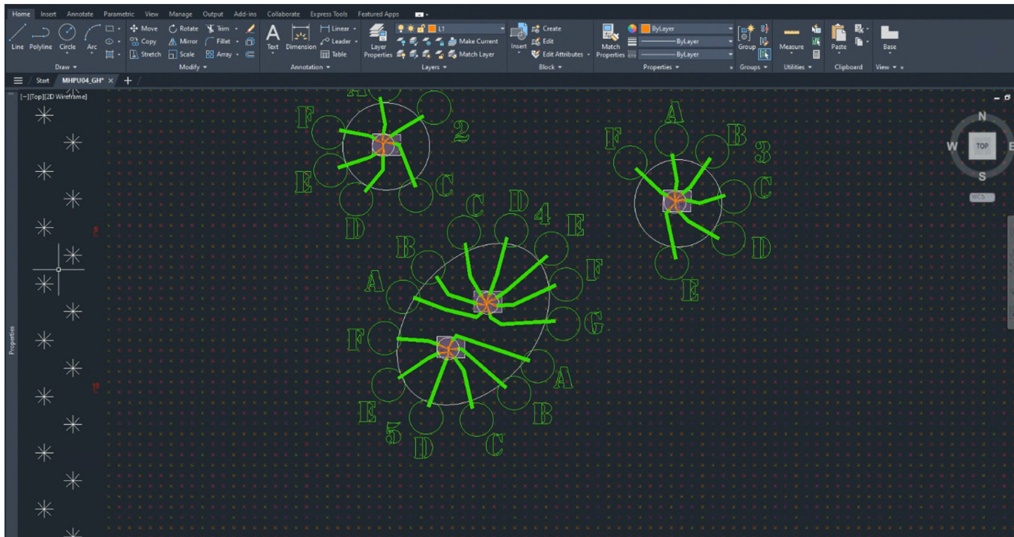

Figure .1: Contact design in AutoCAD.

duration of a few minutes. The exposed substrate had a positive resist coating which means that the EBL effectively increases the solubility of the polymer upon exposure.

IV. Development. The EBL-exposed substrates were developed by submergence in n-Amyl acetate and MBK-IPA 1:1. The chip was first placed in n-Amyl acetate for 45 seconds, followed by MBK-IPA 1:1 for 1 min 15 seconds. The samples were then blow-dried using nitrogen. The development step effectively removes the exposed photoresist, leaving only unexposed regions. In between each fabrication step, an ocular inspection was done using MX50 microscope.

IX. Physical vapour deposition and lift-off of gadolinium, bismuth, gold, and titanium. Physical vapour deposition was used to deposit 35 nm gadolinium, 80 nm bismuth, 40 nm gold, and 20 nm titanium. The deposition rate was 1-2 Å/s. Deposition of metals was followed by lift-off in 60°C Acetone for approximately 5 minutes to remove regions of unwanted metals. A pipette was used to increase the speed of the lift-off process. The sample was then cleaned with Isopropanol and an ocular inspection was done in MX50 to verify the result. The chip was then taken out of the clean room for wire-bonding and electrical measurements.

Temperature dependent measurements and TLM

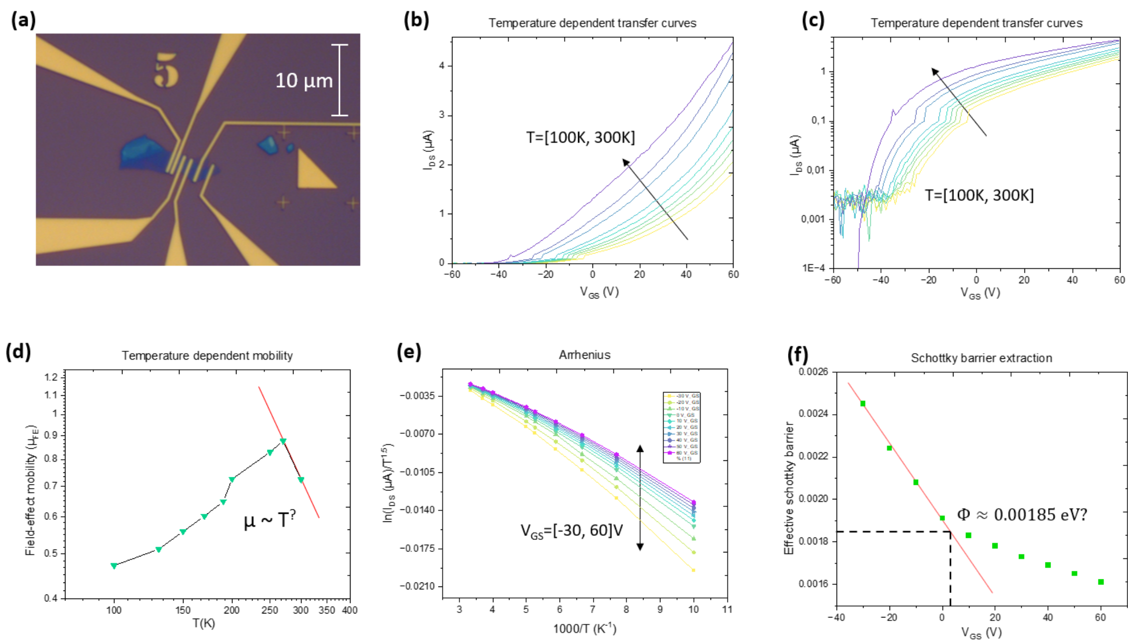

Figure .2: Temperature dependent measurements and extraction of Φ_{SBH} at flat-band condition. a) MX50 optical image of the device. **b)** Temperature-dependent tranfer characteristics measured at $V_{DS} = 1\ V$ for T=100 K to 300 K in linear scale and, **c)** logarithmic scale. **d)** Mobility μ as a function of temperature. The positive mobility dependence on temperature between 100K to 250K is attributed to transport dominated by ionized impurity scattering. Above 250 K, mobility decreases due to phonon scattering. **e)** Arrhenius plot **f)** Effective barrier as a function of gate voltage and Schottky barrier extraction.

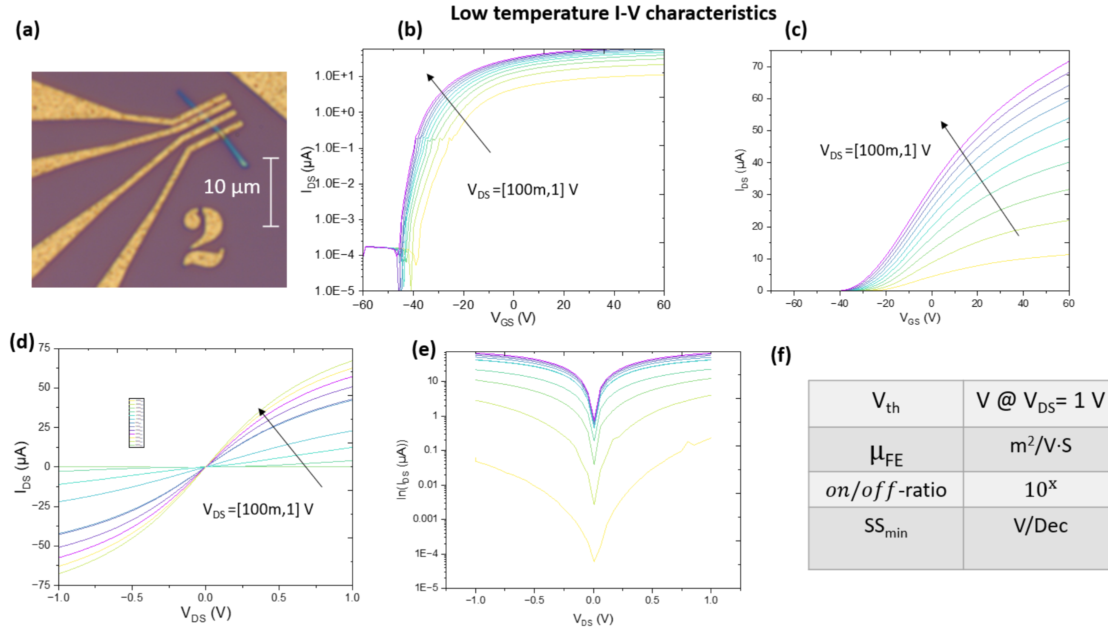

Figure .3: Electrical measurements at 100K of exfoliated MoS_2-FET with bismuth contacts electrodes. a) MX50 optical image of the device. **b)** Transfer characteristics in logarithmic scale measured between $V_{GS} = [-60, 60]V$ for $V_{DS} = [0.1, 1]$ V in steps of 100 mV. **c)** Transfer curve in linear scale for V_{DS} between $[0.1, 1]$ V. **d)** Output characteristic curve for various V_{GS} in linear scale and, **e)** logarithmic scale. **f)** Summary of key parameters extracted for I-V measurements.

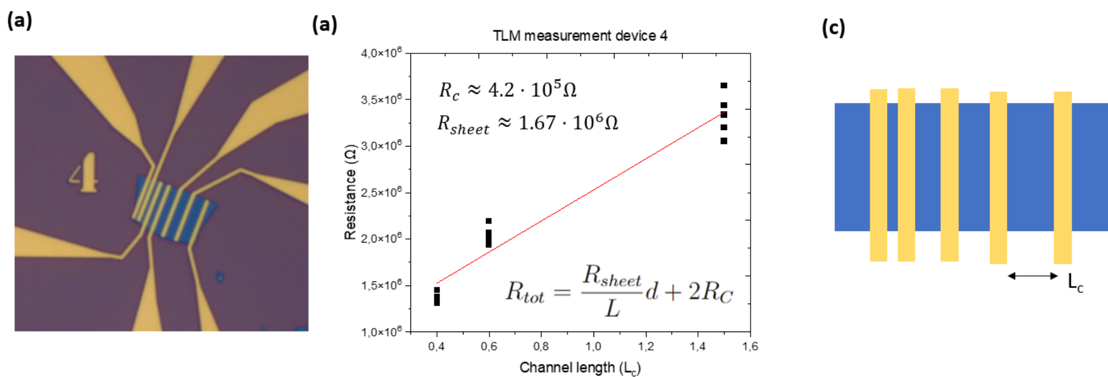

Figure .4: Contact resistance extraction by TLM. a) Optical image of the device. **b)** The contact resistance was estimated by the TLM method to be $R_c \approx 4.2 \cdot 10^5$ Ω, and sheet resistance $R_{sheet} \approx 1.67 \cdot 10^6$ Ω. **c)** Geometrical structure of a TLM measurement setup.

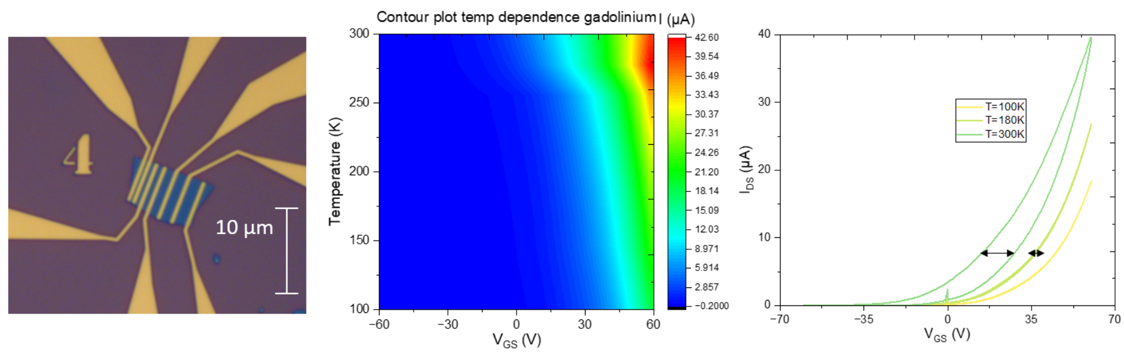

Figure .5: Contour plot and hysteresis. a) Optical image of the device. **b)** Contour plot of temperature-gate dependence and current. **c)** Hysteresis at high and low temperature. Hysteresis disappears at low temperature due to inert interface trap sites.

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