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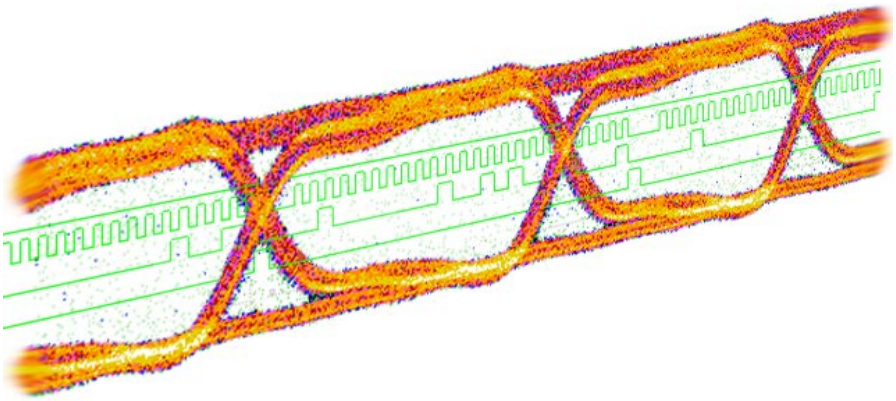

System design of an FPGA and analog based point-to-point wireless link

Master's thesis in Electrical Engineering

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Department of Microtechnology and Nanoscience
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Printed by Reproservice, Chalmers
Gothenburg, Sweden 2014

Abstract

In today's event and media industry big screens and projectors are used to an increasing extent. The video resolution increases with time and so does the bandwidth that is required to transfer the signals. Electrical coaxial or optical cables provide the required bandwidth with a low latency and high reliability but also comes with high costs and requires much work for mounting and demounting. However, cables require more planning and work regarding the installation and therefore a wireless solution may be preferable, as long as the reliability and performance can be guaranteed.

The purpose of this thesis was to explore the possibility to implement a one-way wireless link for streaming of high-definition video with similar performance to commonly used wired solutions. This was done using existing and relatively low cost materials. The system was designed for use in the 60 GHz spectrum. Based on the project prerequisites and theoretical studies D-BPSK was chosen as modulation technique. The system was also designed for a data bandwidth of 1.485 Gbit/s, which is compliant with the HD-SDI standard.

The system was implemented using both VHDL design together with FPGAs and self-designed PCBs. The FPGA parts consist of video processing and encoding functions while the PCBs contain components for modulation and demodulation of the signal. To make a complete link two radio front ends and antennas are needed, which were not developed in the scope of this thesis. The most comprehensive tests were conducted using all the parts implemented during the project and a video signal as input. Instead of front ends and antennas the system was connected using waveguide attenuators.

The results from the tests show that it is possible to achieve a high data rate in the 60 GHz region using relatively simple methods. The components used and developed in this project did however prove to be susceptible to interference, largely due to how the signal ground was handled. By improving the overall build quality of the system as well as some minor design flaws, a highly reliable system should be in reach. In the future the system should be tested in real-world applications together with front ends and antennas. If desired the concept should also allow for higher data rates using more capable components and higher order modulation techniques.

Acknowledgements

First of all we want to thank Simon, Jens and Dzana who always offered us their help with everything from technical issues to proofreading of our texts. We do also want to thank Christian Fager for being our examiner. In addition we would like to thank everyone who has given us feedback during the project and especially Sebastian Gustafsson who helped us with everything from opening the locked premises to troubleshooting the PCBs. We are also grateful for all the free coffee we drank and all the equipment we borrowed from the Microwave Electronics Laboratory.

Finally, we would like to thank Adrian, Frank and the rest of our friends and families.

Aron Svensson, Jonathan Flod, Gothenburg 2014-01-16

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Acronyms & Abbreviations

ADS - Advanced Design System
ASIC - Application-Specific Integrated Circuit
BER - Bit Error Rate
BPSK - Binary Phase Shift Keying
D-BPSK - Differential Binary Phase Shift Keying
DUT - Device Under Test
DVI - Digital Visual Interface
EC - Error Count
FPGA - Field-Programmable Gate Array
HDL - Hardware Description Language
HDMI - High-Definition Multimedia Interface
I/O - Input/Output
IF - Intermediate Frequency
LO - Local Oscillator
Modem - Modulator-demodulator
PCB - Printed Circuit Board
PLL - Phase-Locking Loop
RF - Radio Frequency
PRBS - Pseudorandom Binary Sequence
RF - Radio Frequency
SDI - Serial Digital Interface
SNR - Signal-to-Noise Ratio
Transceiver - Transmitter-receiver
VHDL - VHSIC (Very High Speed Integrated Circuit) Hardware Description Language

1. Introduction

This chapter accounts for the background of the thesis and describes the scope in terms of purpose, limitations and problem description. The thesis outline will also be explained.

1.1. Background

In today's event and media industry big screens and projectors are used to an increasing extent. This combined with higher video resolutions requires a very high bandwidth. The signals are usually transferred using electrical coaxial or optical cables that provide a high bandwidth and reliability. However, cables require more planning and work regarding the installation and therefore a wireless solution may be preferable, as long as the reliability and performance can be guaranteed. Digital Visual Interface (DVI) and High-Definition Multimedia Interface (HDMI) are common interfaces for transferring video signals. Since these standards use multiple signals in parallel they are not suitable for wireless transmissions. A pure serial standard widely used in the industry is Serial Digital Interface (SDI), which would require less work to transfer wireless.

One of the main advantages with a wired solution is the fact that you have your own ether in which the signal can propagate without interference from unwanted signals. With wireless solutions the ether is usually shared with other wireless applications such as cell phones, wireless networks, bluetooth units, radio links etc. Usually a high data bandwidth also requires a high radio bandwidth. Since a bandwidth that is relatively high in relation to the radio frequency (RF) may be hard to cope with, utilisation of the higher frequency regions is preferable.

This thesis is focused on the region close to 60 GHz. The oxygen molecules in the atmosphere tend to resonate close to that frequency, which leads to large attenuation of the signal. Because of this the region is license free in most parts of the world. Another phenomenon that needs to be accounted for is the fact that all radio links operating above the frequency 10 GHz are significantly limited by heavy rainfall. These phenomena create a need for highly directional antennas with high gain and also forces such systems to be line of sight. This also causes the signals not to interfere with other systems in its close surrounding, which makes a 60 GHz system suitable for short to mid-range distances with line of sight communication. The atmospherical attenuation is shown in figure 1.1.

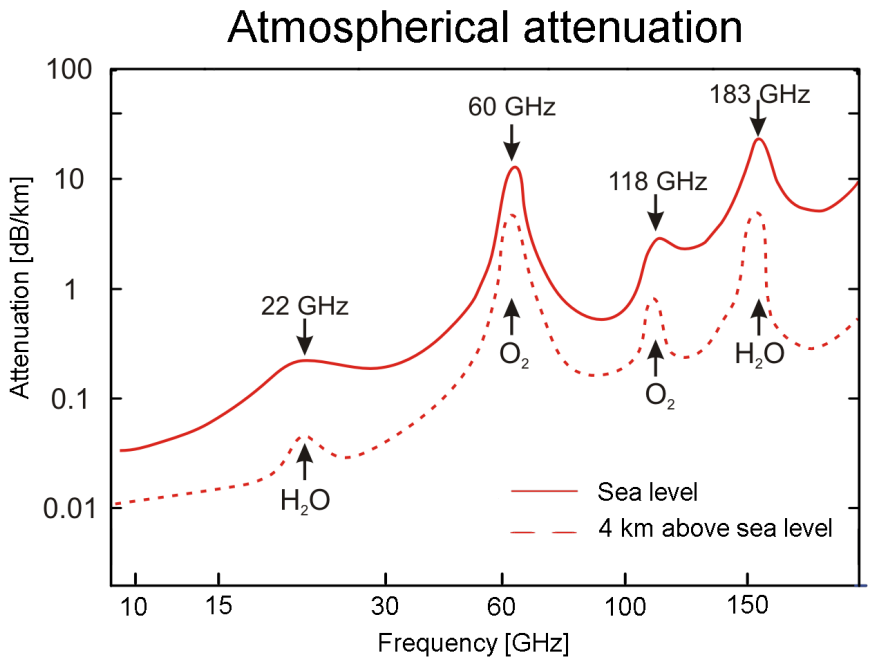


Figure 1.1.: The atmospherical attenuation of radio signals for different frequencies.

The use of the 60 GHz spectrum is becoming more common, both as near-range radars and in telecommunications. One large organisation that developed and promoted a technique for data transfer in the 60 GHz spectrum is the Wireless Gigabit Alliance. The protocol for the technique is called IEEE 802.11ad and delivers data at transfer rates up to 7 Gbit/s. The protocol supports two different modulation schemes, one for stationary units, which also supports the highest data rate, and one for handheld mobile devices which uses less power and thus supports lower data rates.[1]

Another system that uses 60 GHz for video transfer is Boxx Cerulean. It is designed for transmitting two uncompressed HD video streams without error correction. The system is designed to replace a fiber link with a low latency wireless transmission. The system offers a range between 20 and 500 meters with full data capacity.[2]

1.2. Purpose & goals

The purpose of the project is to design, implement and verify a one way point-to-point radio link for wireless transmission of video signals that meets certain specifications. This should be done as a proof of concept using relatively simple and cost-effective methods. The system should consist of video processing functions for converting parallel signals to serial, a radio baseband, 60 GHz radio front ends and antennas.

The system should be able to:

- Handle DVI or HDMI as input and output for video signals.
- Have an effective data bandwidth of 1.485 Gbit/s as required by HD-SDI signals.
- Use an antenna for the wireless transmission at a radio frequency of 60 GHz.
- Have a wireless transmission range of at least 300 m.

1.3. Limitations

The following limitations apply to the project:

- In order to minimize the design workload existing designs and open-source solutions will be used and further developed where it is deemed necessary or resource effective.
- The radio front ends and the FPGA platforms are given from start and can therefore not be chosen based on requirements and evaluations.
- No efforts will be made to ensure that the system can withstand any weather conditions or mechanical stress outside of the lab.

1.4. Detailed problem description

The main focus of the project is to design and implement the video processing functions and the radio baseband. In this thesis the baseband is defined as a modulator together with potential encoding functions on the transmitter side and a demodulator on the receiver side. Implementation of the front ends and antennas are secondary objectives and will be done if time permits.

There are three FPGA platforms available in this project, which are further discussed in section 4.2.2. The radio front ends are given from start, which means that the whole system needs to be compatible with their specifications. They require an input intermediate frequency (IF) between 1-5 GHz. The radio front ends also have a radio frequency (RF) bandwidth of 58-63 GHz. More specification regarding the front ends can be seen in appendix A. Figure 1.2 shows a block diagram of the envisaged system.

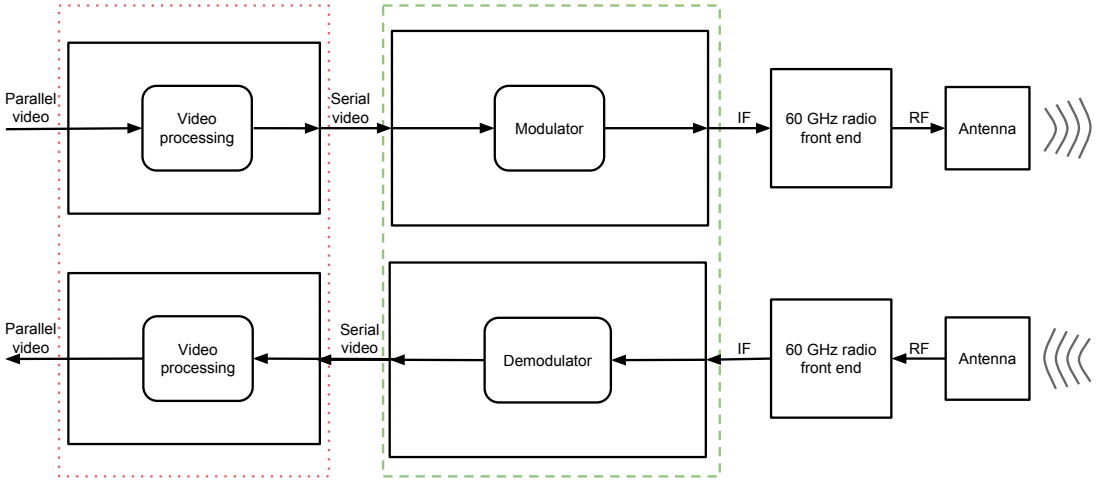


Figure 1.2.: An overview of the envisaged system. The red dotted box contains the video processing part and the green dashed box contains the radio baseband.

1.5. Thesis outline

Chapter 2 describes the method that has been used to accomplish the project. Chapter 3 accounts for the theoretical studies that were conducted in order to successfully design the system. Based on the theory the system is then further specified in chapter 4. How the different parts were actually implemented are also described here. The results from simulations and measurements are then presented in chapter 5 together with a discussion regarding the individual results as well as the complete system. Finally, chapter 6 and chapter 7 contain the thesis conclusion and proposals for future work.

2. Method

In this chapter the methods that have been used in the project to design, implement and verify the system will be presented and explained.

2.1. System level workflow

The first step in this project will be to get a good overview of the problem. This will be done using theoretical studies and discussions with the technical supervisor of the project. The theoretical studies will also be the basis for a link budget, which will be used to design the system.

A link budget is a tool for calculating all of the gains and losses from the transmitter to the receiver in a communication system. The more precise the link budget is the better the final result, and ultimately the choice of components will be. The link budget will be an important tool when deciding which antenna type and modulation technique that is preferred. Since the project will include both digital and analog designs the work will be divided into two design paths.

2.2. Digital sub-systems design flow

The digital parts of the system will be implemented using the FPGA platforms that are available in the project. When the major components that are needed in the system are identified they will be implemented component by component, verified individually and later combined into a system of subsystems.

The design work will be carried out using Alteras Quartus II 13.0 software and the hardware description language VHDL. The software tools that will be used for verification of the FPGA design are Mentor Graphics ModelSim for simulation and Alteras Signaltap II logic analyzer for reading of actual signals.

2.3. Analog sub-systems design flow

The analog work will be based on self-designed Printed Circuit Boards (PCBs). The first objective when designing PCBs is to decide which functions are desired. Based on the desired functions components will then be chosen and compared with focus on relevant properties. Before the design process can begin, information regarding how the components should be biased and connected are gathered and consolidated into a

circuit schematic. The remaining design parameters are determined by the PCB substrate properties. The design process will be carried out using Advanced Design System (ADS) from Agilent, which also enables the possibility to run simulations and relevant calculations. The design file will then be sent to a PCB manufacturer for production of the PCBs. When the ordered PCBs are delivered the components will be mounted. Component that need to be accurately assembled are mounted using a reflow oven and the rest of the components are mounted using a soldering iron.

2.4. System verification

Verification on system level will be conducted step by step in a number of different setups. Most of the digital FPGA-based design can be verified independently of the analog modulator and demodulator, and vice versa. When this has been done all the functions that will be designed in this project can be tested and verified together. The modulator and demodulator will first be connected together directly and later with attenuated waveguides to simulate path loss. If possible, the system will also be tested with the radio front ends and the antennas. During the tests both test signals and real video signals will be used.

In the tests, of both the digital and analog parts as well as the complete system, a number of tools will be used. The most important are a pattern generator with a Bit Error Rate Tester (BERT), together with oscilloscopes for measurements and analysis of the signal waveforms.

3. Theoretical studies

The design choices that will be made regarding the system and its specifications will mainly be based on the theory presented in this chapter. In the last paragraph of each section a small conclusion regarding how it affects the system will be made. Some theory relevant for the verification of the system will also be presented at the end of this chapter.

3.1. Link budget

As explained in section 2.1 the link budget is a tool to get a good overview of losses, gains and signal-to-noise ratio in the system. The most important parameters are the link distance, front-end gain, antenna gain, path loss, back-end gain and noise level. A brief link budget for the envisaged system can be seen in figure 3.1.

What	Value	Unit	Comment
Wavelength	0,005	m	Because of the frequency
Link distance	300	m	As specified in the purpose
Tx power from modem	-20	dBm	Approximated value
Front-end gain	25	dB	Specified in data sheet
Tx antenna gain	0	dB	To be decided
Path loss	-117,547	dB	Calculated with 20*log(4*pi*L/lambda)
Rx antenna gain	0	dB	To be decided
Back-end gain	8	dB	Specified in data sheet
Total Rx gain	**8**	**dB**	Total gain in the receiver
Recieved signal level	**-104,547**	**dBm**	The signal level after the receiver
Total noise power	-71	dBm	Total amount of noise
Signal-to-noise ratio	**-33,5**	**dB**	The signal level related to the noise level

Figure 3.1.: Simplified link budget.

Many of the values in the simplified link budget comes from either the project specification or data sheets from equipment that were specified in the project. The antenna gains are currently zero, which gives us the possibility to affect the received signal level to a large extent. The most relevant value is the signal-to-noise ratio (SNR), which is very low in the simplified link budget. Note that the antennas' gain will improve the value very much. SNR will be further explained in section 3.1.2.

3.1.1. Losses and noise

In order to make the link budget more accurate all the losses need to be taken into consideration. Since the signal is quite sensitive there are losses introduced every time the signal changes medium. The signal is also attenuated as it travels in the same medium. Noticeable losses are coupling losses between cables and components, path loss as the signal travels, pointing error losses and rain losses if it is a wireless system with antennas.

Rain losses are calculated using the regional rainfall rates from the 'Crane Model'. The specific attenuation from the rain is calculated from the amount of rain per hour in a specific region, which frequency spectrum the system is operating in and the probability of the amount of rain in the region. From the calculation, the user can calculate the probability of rain fall and thus account for the downtime of the system due to heavy rain.[3]

The noise in the system originates from various sources, and the antenna noise comes from both sky noise and antenna losses. The sky loss itself originates from the cosmic microwave background, which is believed to come from the big bang. In addition to this there is thermal noise. Thermal noise is introduced both as a function of the bandwidth of the system, but also in all non-zero temperature equipment. Each time the signal is amplified, filtered, mixed or anything similar, there is noise introduced by moving electrons due to the non-zero temperature.[4]

3.1.2. Signal-to-noise ratio

SNR is a comparison between the signal level and the noise level. If the ratio is larger than 1:1 it indicates that the signal level is higher than the noise level. It is a tool to describe the performance of a communication link. There is also a relation between the signal-to-noise ratio and the Bit Error Rate (BER). A specific modulation technique requires a specific SNR ratio to maintain a specified BER. For a higher degree of modulation there are higher requirements on the SNR to maintain the same bit-error rate. At the same time the higher degree of modulation will lower the bandwidth requirement and therefore also the noise, which gives a trade-off that needs to be considered for every independent system. This will be further explained in section 3.5.2.

Based on the contents of this section it is clear that there is primarily one important parameter in the link budget that can be affected by the system-level design, the antenna gain. Since the SNR in the end of the complete system affects the choice of modulation techniques, which will be further explained in section 3.3, an antenna with relatively high gain is preferable.

3.2. Antennas

Antennas are used to convert electric power into electromagnetic waves or vice versa. They play an essential role in all kinds of communicating equipment and can consist of anything from a simple wire to a complex array of dish antennas. What type of antenna that is needed is highly dependent on the application. Important properties will be discussed in the following paragraph.

The antenna gain is a value, often specified in decibels, which combines the antenna's electrical efficiency and directivity. In other words it tells you how good the antenna converts input power into radio waves in a specific direction. An attribute often closely connected to the gain is the half-power beamwidth. The half-power beamwidth is the angle of the cone when the power has dropped 3 dB, or half of the maximum power. In other words, if the half-power beamwidth is a small value and thus a small cone, the maximum gain at the head of the cone is larger than it would have been for a larger cone. To a wide band application it is important that the antenna has approximately the same properties for the whole frequency band. As have been stated in section 1.1 the 60 GHz spectrum requires highly directional antennas to transmit the signal. There are many types of antennas, but there are mainly two types that have been addressed in the scope for this thesis, horn antennas and reflector antennas.

3.2.1. Horn antennas

A horn antenna is shaped as a horn and direct radio waves in a beam out of the horn. They are widely used in microwave applications, both stand alone and as feeders for larger reflector-antenna structures. The antenna works by providing a gradual transition between the impedance of the waveguide and the free space, which enables an efficient radiation. Without the gradual transition the wave would experience a sudden change of impedance, which would give a large reflection and a much lower efficiency. The advantages with a horn antenna are simple construction, broad bandwidth, low standing-wave ratio and moderate gain. A disadvantage is the moderate beamwidth.

3.2.2. Reflector antennas

A reflector antenna is what people usually call a parabolic dish. There are many types of reflector antennas but the common characteristic is the reflector which focus the beam of electromagnetic energy. The main advantages with reflector antennas are the high gain and low side lobes. The disadvantages are low beamwidth and moderate bandwidth. The gain is proportional to the size of the reflector causing a trade-off between high gain and a large antenna.

Considering the low SNR in the simplified link budget in figure 3.1 and the properties of the 60 GHz spectrum, a reflector antenna is probably the best choice, as long as

the bandwidth is high enough for the final system. As high gain as possible also gives more freedom in the choice of modulation technique.

3.3. Modulation techniques

Modulation is the process when one or more properties of a periodic waveform are varied with the signal. The properties that can be varied are; amplitude, frequency, phase or a combination of these. Analog modulation is the generic name of these modulation techniques. The modulation is done in order to make the transmitted information distinguishable by the receiver.

As figure 3.2 shows the modulation techniques can be distinguished by how they modulate the carrier signal. With amplitude modulation the carrier varies in amplitude as a function of the message signal, while in frequency modulation it is the frequency that varies and in phase modulation the phase of the carrier varies as a function of the message signal.[5]

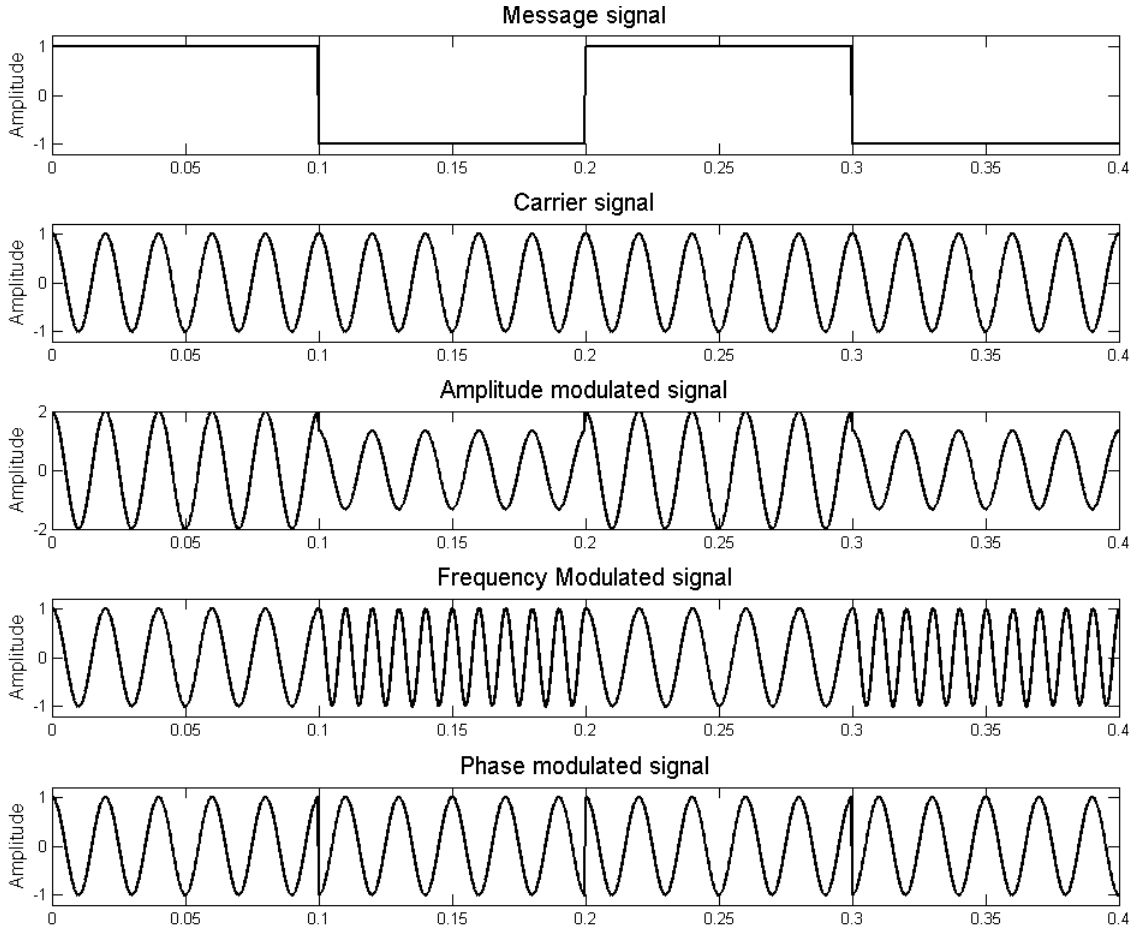
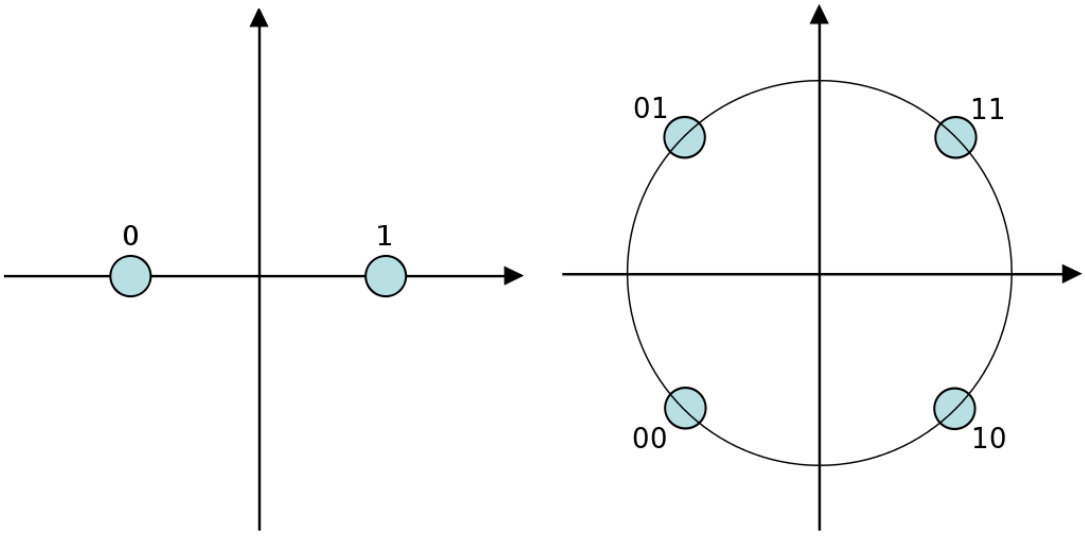


Figure 3.2.: Basic analog modulation techniques.

A widely used modulation scheme is Phase Shift Keying (PSK), which is based on phase modulation. Because of its simplicity it is often used in different kinds of low-cost technologies, such as different versions of the IEE.802.11 and Radio-Frequency Identification (RFID) standards.[7]

3.3.1. Phase Shift Keying

There are different kinds of PSK schemes. The most simple one is Binary Phase Shift Keying (BPSK) followed by Quadrature Phase Shift Keying (QPSK) and higher order variants. BPSK modulates one bit per symbol, which makes it robust and less sensitive to noise and other types of distortion. Due to the one bit per symbol modulation the bandwidth needed for the signal become very large when high data rates are needed. With higher orders of modulation one symbol contains several bits, therefore the data rate may be increased while maintaining a lower bandwidth, or the bandwidth lowered with the same data rate, compared to BPSK. Figure 3.3 shows how digital data is coded for different orders of modulation, here BPSK and QPSK.



(a) BPSK (b) QPSK

Figure 3.3.: Constellation diagram for BPSK and QPSK.

When receiving the signal it can be done either coherently or non-coherently, the difference being whether the system does it with respect to the phase or not. In a coherent system the phase is the same in the transmitter and the receiver. In a wireless system this is usually done with a phase recovering function that recovers the phase from the incoming signal. In a non-coherent system the phase is not recovered, which forces the system to detect the relative difference between each symbol instead of an absolute difference.

For example, if the phase is 180° the output is '0' and if the phase is 0° the output is '1'. But if the receiver is out of phase in comparison to the transmitter there will be an

ambiguity in the decoding process. Instead of 180° and 0° the phase difference could be for example 225° and 45°, then the receiver would be unsure if it is a '0' or a '1'. This problem is solved by using the relative difference in phase between each symbol instead of the absolute phase.

In the simple form of PSK the coherent modulation technique is called BPSK and the non-coherent modulation technique is called Differential Binary Phase Shift Keying (D-BPSK). To implement D-BPSK in a system the information needs to be encoded in the transmitter in order for the receiver to decode it correctly. The difference is illustrated in figure 3.4.[7]

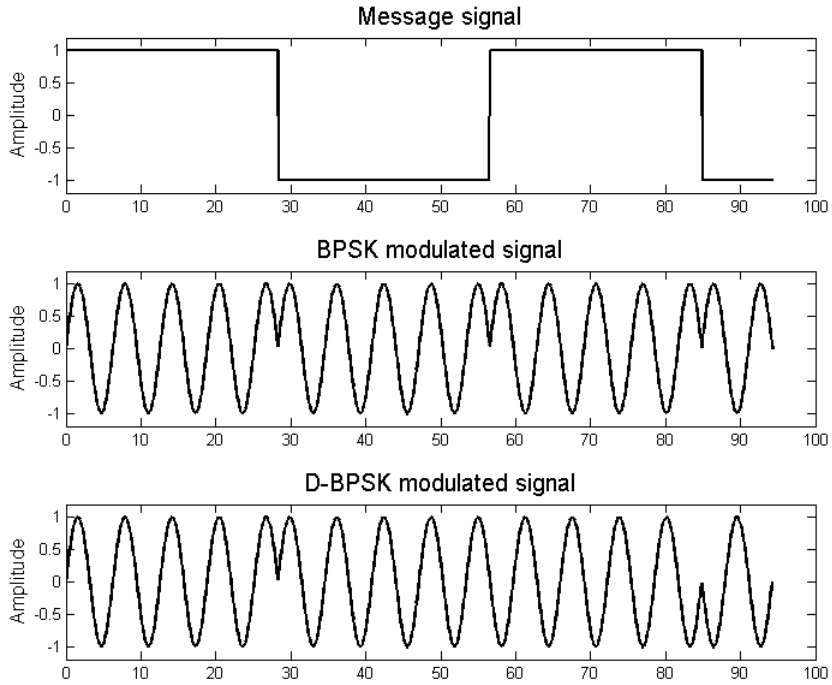


Figure 3.4.: The difference between BPSK and D-BPSK.

3.3.2. Differential encoding

The encoding used in D-PSK techniques is what ensures that the original data can be retrieved from a symbol, based on the relative phase difference. For a N-bit data input $[a_0, a_1, ..., a_N]$, which represents k symbols $[\theta_0, \theta_1, ..., \theta_k]$, depending on the actual coding rule, the signal phase of the output θ_k can be expressed as the following sum. [8]

$$\theta_k = \theta_{ref} + \sum_{i=0}^{k} \Delta\theta_i \tag{3.1}$$

Where θ_{ref} is the initial reference value and $\Delta\theta_i$ is the addition to the phase from every symbol based on the coding rules.

In the case with D-BPSK the number of data bits and symbols are equal. Because of this the encoding process can be carried out using the following relation, where d_k is the encoded data that can be directly applied to the output-signals phase.

$$d_k = \overline{a_k \oplus d_{k-1}} \tag{3.2}$$

While the use of differential encoding eliminates the need of coherent detection it also has one significant drawback, error multiplication. This means that if the demodulator receives one erroneous symbol, the output of the demodulator will have two erroneous symbols. This phenomenon renders a BER that is approximately twice as high as the rate for a coherent system at a SNR where errors seldom appear in consecutive symbols.

3.3.3. Decoding

As explained in section 3.3.1 detectors can either be coherent or non-coherent depending on the detection process. Coherent detectors must synchronise its local clock to the phase of the incoming signal in some way. This is usually solved with a phase-recovering circuit and must be done for the system in order to interpret the incoming signal in the right way. In a non-coherent system this is not needed because the system can translate the incoming signal independent of the absolute phase.

An example of a D-BPSK demodulation technique is quadrature detection. To demodulate the signal the previous symbol is used as reference when the current symbol is demodulated. The modulation scheme is explained in table 3.1.[9]

Table 3.1.: Modulation scheme explaining the modulation and demodulation process.

Modulation	**ref.**									
Message a_k		1	0	1	1	0	0	0	1	1
Encoding $d_k = \overline{a_k \oplus d_{k-1}}$	1	1	0	0	0	1	0	1	1	1
Signal phase θ	0	0	π	π	π	0	π	0	0	0
Demodulation										
Demodulation ($\cos\theta$)		1	-1	1	1	-1	-1	-1	1	1
Demodulator output		1	0	1	1	0	0	0	1	1

To accomplish the demodulation process the previous and the current symbol have to be multiplied. This can be derived mathematically with two sinusoids with amplitude A and an arbitrary time difference of d, which in this case corresponds to a one symbol delay.

$$Asin(2\pi ft) \tag{3.3}$$

$$Asin(2\pi f(t-d)) \tag{3.4}$$

By mixing these signals together we receive the following.

$$Asin(2\pi ft) * Asin(2\pi f(t-d)) = \tag{3.5}$$

$$= \frac{A^2}{2}cos(2\pi fd) - \frac{A^2}{2}cos(2\pi fd)cos(2*2\pi ft) + \frac{A^2}{2}sin(-2\pi fd)sin(2*2\pi ft)$$

From 3.5 it can be seen that the second and third term has twice the frequency, which are not of interest and thus may be filtered away using a low-pass filter. The first term, the one of value, varies in sign and amplitude depending on the phase difference between the previous and current symbol. If the current and previous symbol are in phase the difference is zero and thus the output is $\frac{A^2}{2}$. If the current and previous symbol are π radians out of phase, the output will be $-\frac{A^2}{2}$. This is only valid if the phase is 0° and 180°, if it would be 90° and 270° the output would be 0 all the time.

With this as background the demodulator recovers the signal phase modulation as a varying baseband signal.[9]

From an implementation perspective BPSK, or more specific D-BPSK, is the modulation technique that is easiest to implement, mostly because of the simple BPSK constellation diagram and the differential encoding, which eliminates the need of synchronisation between the transmitter and the receiver.

As earlier mentioned two major drawbacks with D-BPSK are the large radio bandwidth needed for the signal and the BER, which is approximately twice as high at the same SNR compared to the non differential counterpart. Thanks to the properties of the 60 GHz spectrum the available bandwidth is quite large though, and the rest of the system should be able to provide a SNR that is good enough for a BER suitable for video signals.

3.4. Digital video signals

There are some different standards and interfaces that are widely used by consumers and the industry in order to transfer video. On longer distances it may be practical to send the data serially to minimize the number of wires in a cable. This field includes a lot of different open and closed standards for different video formats and encoding standards.

3.4.1. Parallel interfaces

Two common interfaces for transferring digital video are DVI and HDMI. DVI was created as an industry standard for digital video, but the interface also includes analog

signals for backward compatibility. The digital signals are encoded using transition minimized differential encoding, which is a variant of 8-bit/10-bit encoding. This is to allow a high data rate over as long cables as possible. The encoding is done separately for each color in the signal which leads to an output based on three channels that send color data rate at ten times the pixel clock. The pixel clock and some other signals are also sent over the DVI cable. [12]

On older cathode-ray-tube based monitors the analog signal included blanking periods where the electron gun could go back to start a new line. Because of the backwards compatibility the digital signals also contain these periods, but instead of doing nothing the empty space may be used to send additional data.

HDMI is compatible with the digital part of DVI which makes the conversion between the two very easy. This newer standard do however include additional features such as transmission of audio signals and support for different color spaces. HDMI do not provide any support for analog video signals. Figure 3.5 shows the principle of parallel video transfer using HDMI. [13]

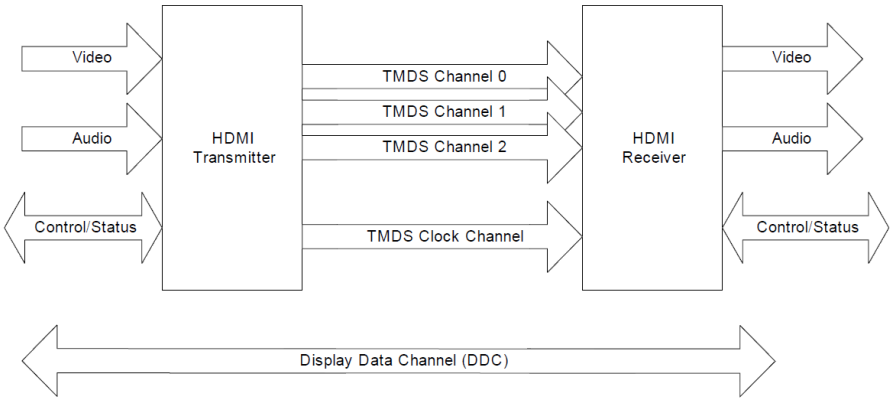


Figure 3.5.: A flow diagram describing the principle of parallel HDMI video signals.

3.4.2. Serial interfaces

If a video signal is to be sent as a serial bit stream it needs to be packaged properly in order for the receiver to be able to retrieve the parallel signal from it. A very common interface used throughout the media industry for this purpose is Serial Digital Interface (SDI). The standard exists in various versions for different video resolutions, but the one relevant for this thesis is HD-SDI.

The HD-SDI standard is standardized in SMPTE292 by The Society of Motion Picture and Television Engineers (SMPTE) and specifies both the technical details and the data format of the signal. It uses a bit rate of 1.485 Gbit/s to transfer HD-video signals using electrical coaxial cables with an impedance of 75 Ω. Figure 3.6 shows the underlying standards that the interface is built around.

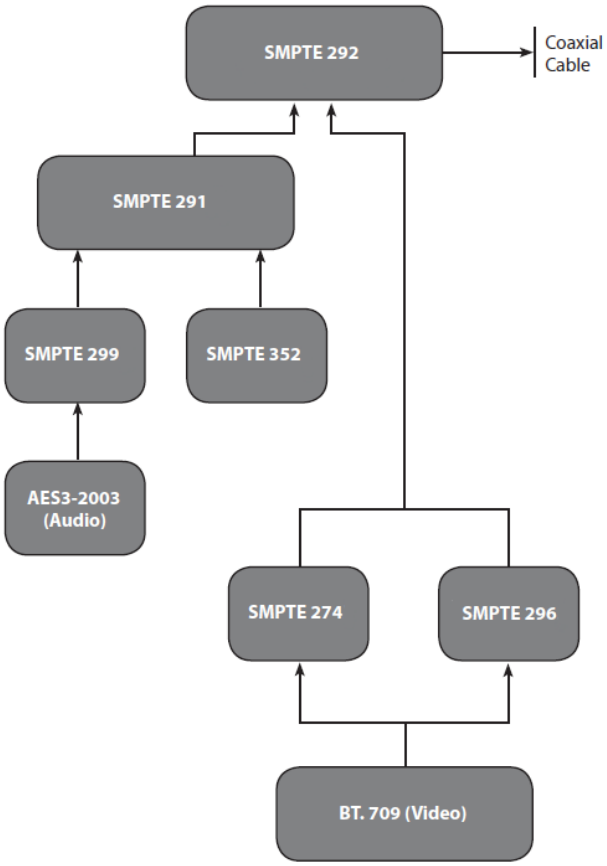


Figure 3.6.: A flow diagram describing the standards that are included in the SDI interface.

SMPTE 292 is the actual HD-SDI-interface standard that encodes the signals as a serial bit stream that consists of 10-bit words. It divides every line of a video signal into four areas; start of active video, end of active video, digital line blanking and digital active line. As input video it requires 10-bit words that are encoded according to SMPTE 274 or 296, which are standards for encoding digital video into parallel 10-bit words. The digital line blanking area is used to embed ancillary data such as audio into the signal. SMPTE 291 is a standard for organizing this ancillary data into 10-bit words compatible with the interface standard.[14]

The parallel digital video standards SMPTE 274 and 296 are based on an older high-definition television standard recommended by the International Telecommunication Union (ITU). This recommendation is called BT.709 and specifies pixel count, refresh rates and color spaces. Worth mentioning is that these standards use both the well known color space RGB but also YCbCr. YCbCr is not an absolute color space but a way of encoding RGB color data. Figure 3.7 shows an example image encoded in YCbCr.

Figure 3.7.: An YCbCr-encoded image divided into luma, blue-difference and red-difference chroma components.

In RGB the image is encoded with different levels of red, green and blue where the highest values represent white, and the lowest black. In YCbCr the color data is instead encoded as luminance, which is basically a grayscale version of the image, and the other two channels are defined as color differences. One big advantage with YCbCr is that the human eye is more sensitive to the luma information. Therefore the colour information may be compressed or downscaled without affecting the visual experience as much as with RGB.

There are a lot of standards that are strongly specified and this can be confusing when trying to implement them. However, by using them the signals are guaranteed to be compatible with other devices. The standards are also optimized for withstanding attenuation and interference when transmitted over large distances.

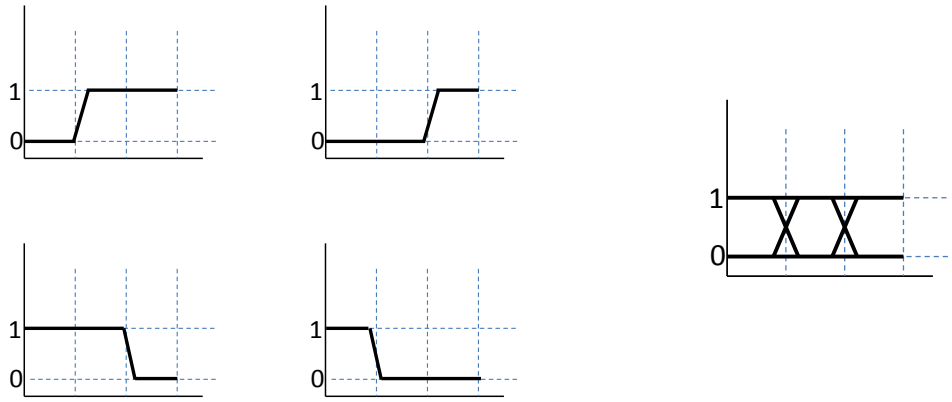
3.5. System verification

This section explains some concepts that are essential for understanding of the verification part of the project.

3.5.1. Eye diagram

An eye diagram is a diagram that shows different signal segments in the same diagram. By superimposing a series of bits, the generated output looks like the opening of an eye. If the communication system would be ideal the eye would look like a rectangular box, but since every electrical transition from '0' to '1' or '1' to '0' takes some time the vertical lines will have some inclination. This can best be understood by watching figure 3.8 where four different series of three bits are superimposed into the resulting eye diagram.[10]

The eye diagram is an advantageous tool when analyzing the non-logical signal integrity. It is also useful when deciding the best sampling point, determining the SNR at the sampling point and can indicate the amount of distortion in the signal.



(a) Different transitions for a series of 3 bits.

(b) The resulting eye diagram.

Figure 3.8.: The principle of an eye diagram.

3.5.2. Bit error rate

The BER of a system is calculated by dividing the number of erroneous bits with the total number of sent bits. This is a good way to measure how much of the originally transmitted data that passes through a system correctly, which is closely related to the expected performance. To measure the BER, a Bit Error Rate Tester (BERT) can be used. The basic idea is to use a known output and compare it with the input when the signal has passed through the Device Under Test (DUT). The number of non-matching bits adds to the error count. The actual BER can only be calculated when the number of tested bits approaches infinity and therefore the problem is of a statistical character. The confidence level CL for a certain test can be calculated as follows.[11]

$$CL = 1 - e^{-N_{bits} \times BER} \tag{3.6}$$

Where the BER is specified in the form 10^{-n} and N_{bits} is the number of tested bits. This method for calculating the relation between BER and confidence level is only valid as long as the EC is zero during the test. When errors occur there are no closed solution, hence the calculations must be solved numerically. For a certain confidence level and BER the equation 3.6 can be used to calculate the number of bits that are needed for a successful test, as shown below.[11]

$$N_{bits} = \frac{-ln(1 - CL)}{BER} \tag{3.7}$$

Various signals can be used when performing a BERT. A common and useful type is a Pseudo Random Binary Sequence (PRBS) signal. The generation of PRBS signals is easy to implement in hardware and the signal is a repeating sequence of a specific

length, depending on the degree and type. A PRBS-n sequence is generated based on n bits and has a maximum length of $(2^n - 1)$ bits, which if it is the maximum length sequence contains every possible n-bit binary number except all zeros. Even though a PRBS signal is deterministic hence not truly random, it stresses a system in a similar way that random signals would. As the degree of the PRBS-n signal increases so does the stress on the system with longer continuous sequences of ones and zeros.

3.5.3. BER vs. SNR

In section 3.1.2 the relation between BER and SNR is mentioned. Since the noise varies with the bandwidth, the SNR also varies with the bandwidth. Therefore another measure is used, normalized SNR. The normalized SNR is called E_b/N_0 and is also known as "SNR per bit". E_b is referred to as the energy per bit and N_0 is referred to as the noise spectral density. For a specific BER a certain ratio between E_b and N_0 is required and the ratio can be used to compare different modulation techniques. The ratio can thereafter be converted into a specific number of required SNR for the system. A graph showing BER vs E_B/N_0 is shown in figure 3.9.

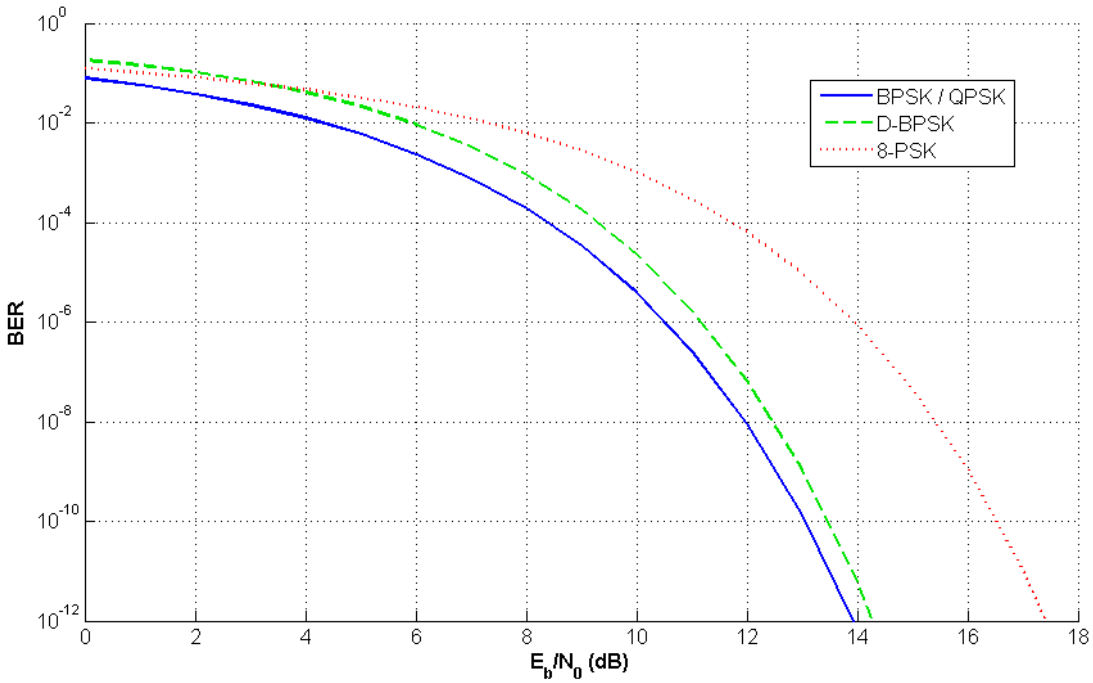


Figure 3.9.: BER vs E_b/N_0 for different modulation schemes.

4. Design & implementation

This chapter accounts for the design and implementation work that has been carried out during the project. The first section presents a more detailed system with design choices that have been made based on the theoretical studies. Since the system contains both digital and analog components, which have been implemented separately the following sections are broken down to describe the implementation from a digital and analog perspective.

4.1. System level design

A more detailed link budget was finalized based on the theoretical studies and specifications of components used in the system. The calculations are based on D-BPSK, which was chosen as the modulation technique, and reflector antennas. The detailed link budget can be seen in appendix B.

The system was designed to have parallel video, such as DVI or HDMI, as input on the transmitter side and then convert it into HD-SDI signals. Because of the modulation technique the baseband has to contain functions to apply differential encoding to the signal. The IF is then modulated by the encoded signal and connected to the input of the front end. The IF has been chosen to 3 GHz based on the front end specifications. In the front end the signal gets upconverted to the RF of 60 GHz and then transmitted by the antenna.

On the receiver side the radio front end will down-convert the RF which results in the IF. When the signal is demodulated the original HD-SDI signal will be its output. This signal can then be converted back to parallel video. An overview of the complete system can be seen in figure 4.1. As mentioned, the work was divided into two separate design paths. Which component that was implemented using digital or analog design is also shown in the figure.

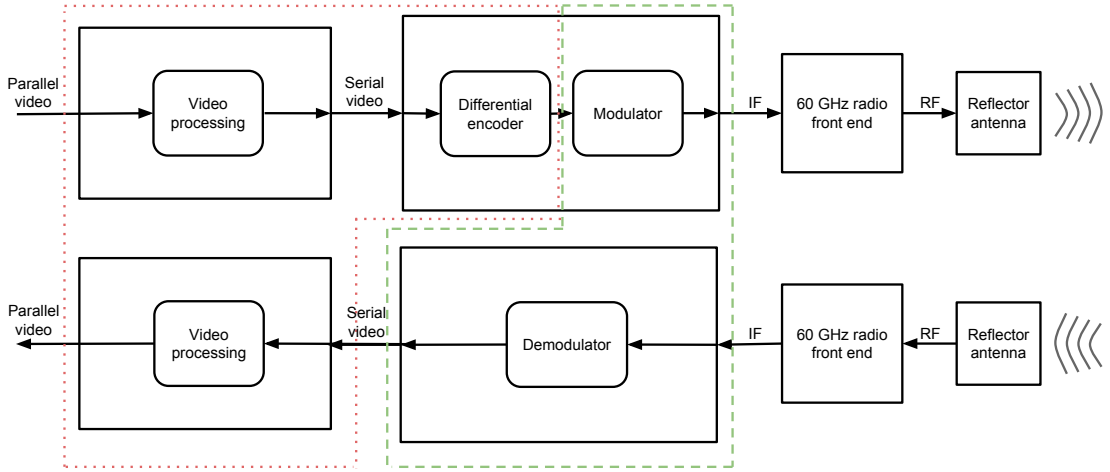


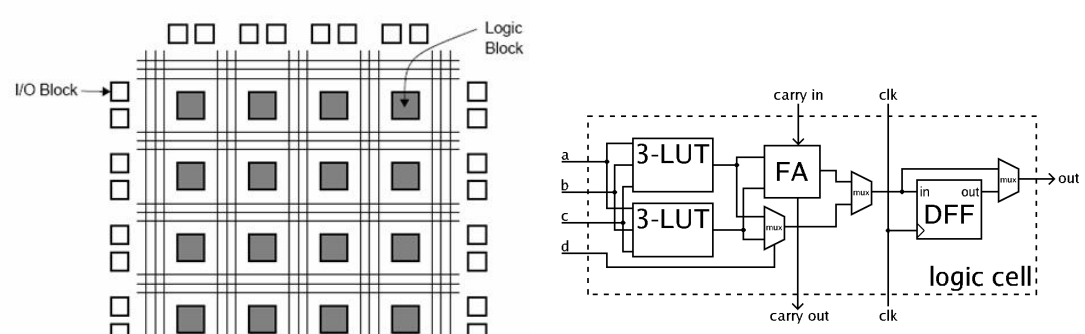
Figure 4.1.: Overview of the complete system. The red dotted box contains the digital parts and the green dashed box contains the analog parts.

4.2. Digital implementation

The digital parts of the system have been implemented using different FPGA-based platforms. The parts of the design that were implemented in FPGAs are the video processing and the differential encoder. The first subsection below explains what FPGAs and hardware description languages implies and may be skipped by initiated readers. After this the implementation of the different parts of the design are explained.

4.2.1. FPGA design and hardware description languages

A Field-Programmable Gate Array (FPGA) is a reconfigurable integrated circuit that usually contains an array of logic blocks, routing interconnects and I/O blocks. A logic block consists of a number of logic cells, by configuring these blocks and the routing between them, different functions can be adopted. The principal function of a logic cell can be described with configurable lookup tables, a full adder and a D-type flip-flop. Figure 4.2 shows the basic structure of an FPGA and a logic cell. In addition to these fundamental components a modern FPGA may also contain multipliers dedicated for digital signal processing, embedded memory, processors and other embedded components to form a complete system on a chip.[15]



(a) An FPGA with its main components.

(b) Example illustration of a logic cell.

Figure 4.2.: Basic description of an FPGA and a logic cell.

The typical applications for FPGAs are prototyping and smaller production series where low latency and a high level of parallelism are needed. Compared to micro controllers and ordinary computers an FPGA offers a lot more parallel computing power and higher power and space efficiency. On the other hand an Application Specific Integrated Circuit (ASIC) offers even better performance in these aspects, but comes with the drawbacks that it has a very high initial cost to start manufacturing of the circuits, more expensive developing costs and is more complex to test. According to Xilinx, the largest FPGA manufacturer in the world, FPGAs are a better choice than ASICs for an increasing number of higher-volume applications. This statement is based on the facts that FPGAs have higher performance, reduced power consumption and lower material costs than before at the same time as ASICs are affected negatively by a number of factors. These factors include rising initial production costs, higher complexity and therefore development time which leads to costs and increasing revenue losses for time to market.[19]

In order to configure an FPGA a Hardware Descriptive Language (HDL) must be used. The two most common languages are VHDL and Verilog where the major difference lies in the syntax. These two languages are also endorsed as standards at the Institute of Electrical and Electronics Engineers (IEEE). Compared to common computer programming languages the HDLs are not executed as sequential programs but are said to describe the hardware, and can do so for both sequential and concurrent functions. The concurrent functions are executed in parallel, while this enables very effective solutions for a number of problems it also introduces potential problems such as race conditions.

A HDL designer often writes the code at the registry transfer level (RTL). This means that the code describes the design as a flow of data signals between registers and logic operations applied to these signals. Since an FPGA does not execute the HDL code as a regular processor that processes instructions, the code is rather far from how it

is physically implemented in the FPGA. To successfully configure the device based on a design, synthesis tools are used. These tools often come from the respective FPGA manufacturer and analyzes the code, breaks it down to basic logic-gate functions and then translates it into actual connections and configurations of the circuit. Not all HDL code is possible to synthesize though and is used purely for simulations and test benches. There are also tools that can carry out synthesis of the HDL code targeting ASIC production.[15]

A state machine is often used in order to implement more advanced sequential functions in VHDL. In this project the state machines have been based on Gaislers two-process method. It is a method that can be used for any single-clock design, some of its most important goals are to increase the abstraction level, improve readability and simplify debugging. By using one sequential process that only performs latching of the state vector and a combinatorial process, where the outputs are functions of the sequential output r and other signals, these goals can be acheived. Figure 4.3 shows a generic two-process circuit.[16]

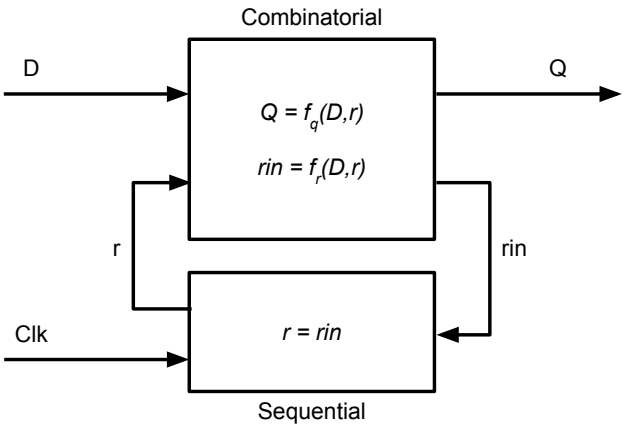


Figure 4.3.: Generic two-process circuit.

4.2.2. Available FPGA-platforms

There were three different hardware platforms available for the development in this project. The first one (A) is a Cyclone III based FPGA and it exists in two variants, one for transmitting and one for receiving. The board has separate circuits for DVI I/O and SDI video I/O via an optical interface. This platform is relatively cheap, but also not very adaptable. The second platform (B) is a Cyclone IV GX starter kit from Altera. The FPGA in this platform has embedded transceivers with corresponding connectors on the board as well as a number of general I/O pins. The third platform (C) is based on an Arria V GX FPGA, which contains a lot of logic and arithmetic resources and some

I/O, including one HDMI output. Photos of the three different platforms can be seen in appendix C. Table 4.1 shows a selection of specifications of the different platforms.

Table 4.1.: Comparison of the FPGA platforms.

FPGA	**Logic Elements**	**Memory [kbits]**	**Multipliers**	**Cost [$]**
A - Altera Cyclone III	15,408	504	56	200
B - Altera Cyclone IV GX	14,400	540	0	395
C - Altera Arria V GX	190,000	1,180	1200	850

From the table it is clear that the Arria V FPGA has a lot more resources for both logic and arithmetic operations compared to the other two. Another interesting feature in this project is the performance of the embedded transceivers. The Cyclone IV GX transceivers can operate at up to 2.5 Gbit/s while the Arria V GX can reach 5.6 Gbit/s. The FPGA on platform A has no embedded transceivers and has to rely on other circuits for high speed serial data transfer.

At the start of the project the possibility to implement all the desired functions on the Arria V GX platform was explored. One problem that was discovered is that the single HDMI connector can only be used as an output. This means that some modifications and additional hardware would have been needed. Another difficulty with this platform was that the FPGA at the time was a very new design with new features that were hard to find documentation and support for. Based on this and the fact that the other platforms seemed to be good enough and also less costly platform C was abandoned.

4.2.3. Video processing

The processing functions were implemented on the Cyclone III based platform A. The design was carried out in three major steps. The first was to output a test image generated in the FPGA to a monitor from the board that would be used to receive serial video data, called the receiver side. The test image was designed to contain a number of geometric figures, some outer borders and a moving square. These figures could then be used to verify proportions, refresh rate as well as horizontal and vertical synchronisation visually on a monitor. The test image generator was also designed using generic values in order to easily test different resolutions and refresh rates.

The next step was to generate the test image in the FPGA on the transmitter side, serially transfer it to the receiver side and then output it to a monitor. To send data as serial SDI signals using the on-board circuit, the RGB color data had to be converted to YCrCb data according to the circuits input specifications. This conversion is carried out by multiplying the RGB data with certain constants and mapping the results onto the three YCrCb channels. The constants used in this conversion are based on the standard described in the ITU-R recommendation bt.601.[17] Computer graphics use the full 0-255 range for each RGB channel, but the standard is created for signals that only use the

range 16-255, therefore the constants have been slightly modified to get the correct black levels. Since the conversion only applies to the color data and takes a couple of clock cycles to perform, the synchronization signals have to be delayed by the same amount of cycles.[18]

On the receiver side the conversion back to RGB needs to be made. Except for the inverse conversion the FPGA design on this side is very similar to the one on the transmitter side. Both sides also use a built-in Phase Locking Loop (PLL) in order to distribute the needed clock signals. When the serial video transfer was verified the test image generator could be replaced with an actual input of video data from an ordinary personal computer. A dataflow diagram that describes the final design of the transmitter and the receiver can be seen in figure 4.4 and 4.5. The SDI circuit uses optical I/O and therefore converters will be needed in order to connect with the baseband, which uses coaxial SMA connectors.

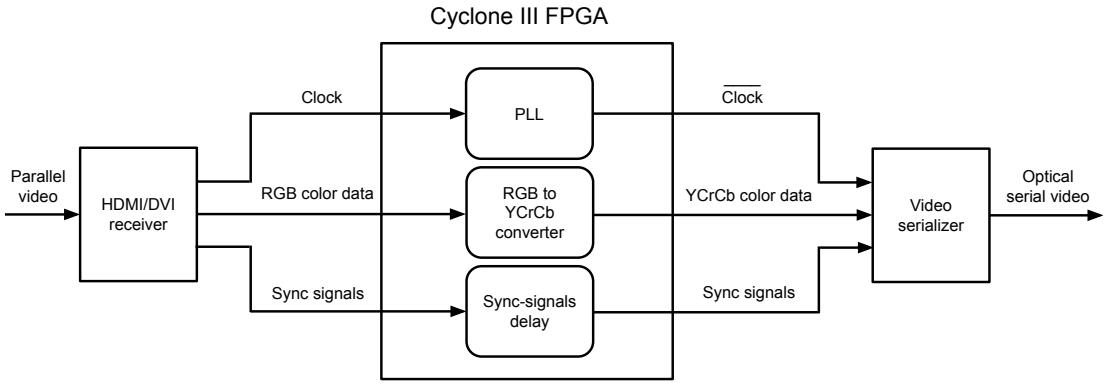


Figure 4.4.: Overview of the FPGA design for video processing on the transmitter side.

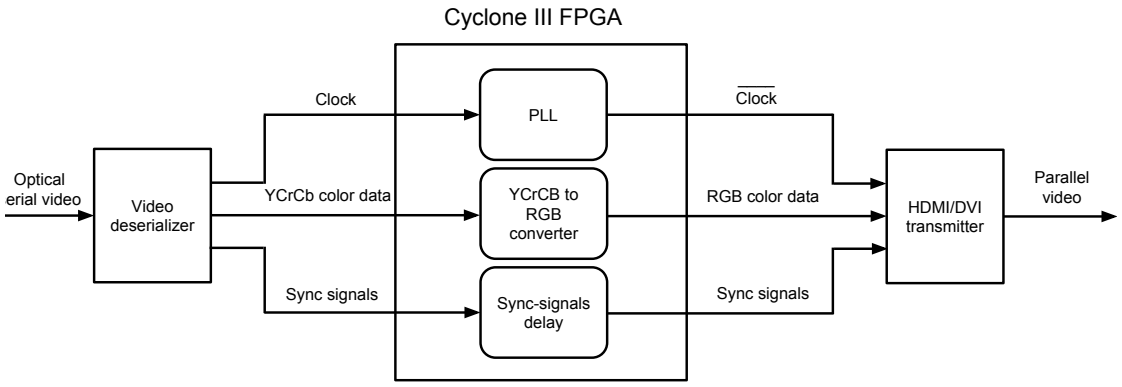


Figure 4.5.: Overview of the FPGA design for video processing on the receiver side.

The video transmitter and receiver may also be used as a pure serializer or deserializer and bypass all the video coding features. By using them in this mode D-BPSK encoded

data could be sent instead, which is required for the recovery of the original signal in the demodulator. Since the receiver was unable to lock to the differential encoded data the implementation of this solution was unsuccessful and the differential encoding had to be implemented on a separate platform.

4.2.4. Differential encoder

The baseband differential encoder was implemented on platform B with the Cyclone IV GX FPGA. The first step was to implement and verify the transceiver in the FPGA, followed by the addition of differential encoding and some supporting functions.

Since the FPGA cannot work in such high speed as the HD-SDI standard uses, 1.485 GHz, the serial data has to be deserialized. To do this, and also to serialize the data again after processing, the built in transceiver on the FPGA was used. The transceiver was configured to output the data to the FPGA fabric at a speed 20 times lower than the actual data rate. The receiver also outputs a clock that is recovered from the serial data signal. The transceiver also has a reference-clock input, which is used to help the receiver to recover the data and also to clock the transmitter. The ideal frequency for this clock is the exact frequency of the incoming data. However, the reference clock must be driven from an external input and therefore the recovered clock cannot be used and routed internally which might have been preferable.

In order to solve this problem an external clock conditioner from Texas Instruments, LMK03000C, was used. The clock conditioner contains a PLL and locks to an incoming clock and outputs a stable and clean clock signal. After a lot of testing and debugging it was determined that the best way to make the system run was to start the clock conditioner with a clock signal from an on-board oscillator and then switch to the recovered clock from the transceiver. In this way the transceiver is driven by a stable clock that is matched with the incoming data and actually originates form its own recovered clock signal. The programming of the clock conditioner was done based on the specifications of the circuit described in [20].

The main purpose of deserializing the signal was to apply differential encoding which is needed for the demodulator to successfully recover the original signal. The encoding was implemented using the parallel prefix layer structure proposed in [8]. This encoder is a pipelined design that applies the encoding to 20 bits in parallel and over several clock cycles. The details of the encoding process is better described in 3.3.2.

When the transceiver and the differential encoding had been implemented a number of additional functions were added to the design. To start with some control logic was designed. This logic enables the system to perform a reset, either manually using a push button or automatically on loss of synchronization or after a period without an input signal. The status of the signal and synchronization is also shown on two of the boards LEDs.

A component was also added that handles the configuration of a frequency synthesizer, which is described in 4.3.4. As mentioned in section 4.3.4 this component needs to be

configured and this is done in a similar way to the configuration of the clock conditioner. Therefore, most of the code could be reused. Figure 4.6 shows a dataflow diagram of the Cyclone IV GX design with the differential encoder.

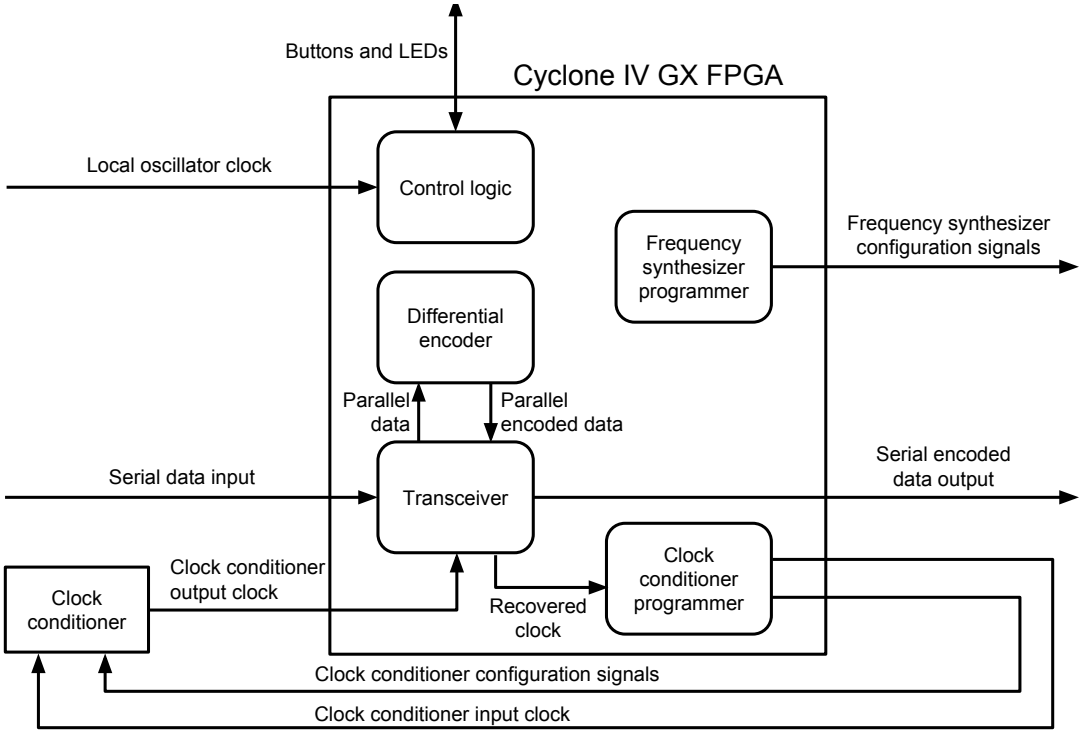


Figure 4.6.: A dataflow diagram of the most important signals of the FPGA design for the Cyclone IV FPGA together with the clock conditioner.

4.3. Analog implementation

The first part of this section describes some theory related to the design process and thereafter the analog implementation process will be described.

The first part of the design process was to choose how the transmission lines should be built and what PCB material to use. The next part was to decide which features that were desired. In order to minimize troubleshooting each feature were to be designed on different circuit boards, as each circuit can be measured without being connected to the other boards. In total there were three boards that were to be designed: (1) modulator, (2) demodulator and (3) frequency synthesizer. The final PCBs with components are shown in appendix D.

4.3.1. High-frequency circuit design

The first part of the design is to decide which circuit design that is desired and achieves the best results. There are mainly three types of circuit designs that are presented together with its advantages and disadvantages below.

In the early years of microwave development the waveguide, in particular the rectangular, were the dominant conductor due to the possibility to combine it with high quality discrete components. Even though this enabled the use of better components the waveguide itself suffered from its narrow bandwidth due to the cut-off frequency. To overcome the problems with narrow bandwidth the waveguide was replaced by the coaxial line, which instead raised problems with expensive components. To solve these problems the coaxial cable was modified to what is called a strip transmission line or stripline, which can be seen in figure 4.7.

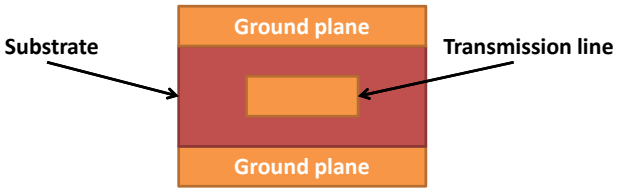


Figure 4.7.: Cross-section of a stripline.

The stripline is similar to the coaxial cable in several ways, it has no cut-off frequency and it is non dispersive. Since the area between the outer plates consists of only one medium the phase velocity and characteristic impedance of the dominant mode does not vary with frequency. Stripline is often used in multilayer boards since it can be routed in the substrate between the other layers. The return path for a high frequency is located just above and below the transmission line thus the signal is contained inside the PCB, which minimizes radiation.

Directly after the stripline was introduced it was modified by removing the ground

plane above the transmission line, leaving the transmission line and bottom ground plane only separated by the substrate. This is illustrated in figure 4.8.

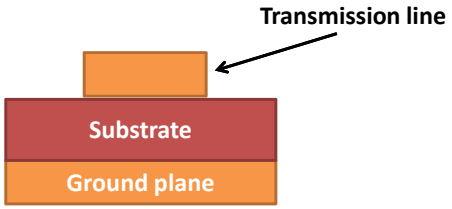


Figure 4.8.: Cross-section of a microstrip.

The modified stripline is called microstrip and is the most used and best known planar transmission line for microwave and RF circuits. It is very popular due to the easy manufacturing process, good integration with solid-state devices, good mechanical support and good heat dissipation. Due to the asymmetries in the microstrip line all discontinuities make the pattern radiate to a certain extent and therefore cause higher losses. The primary advantages of the mirostrip is low cost, compact size and simple manufacturing process, while the disadvantages mainly are higher losses and slightly altered properties with changing frequency.

More recently a new type of waveguide was developed with both the transmission line and the ground plane in the same layer. It is called grounded coplanar waveguide and can be seen in figure 4.9.

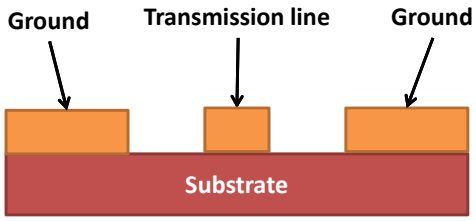


Figure 4.9.: Cross-section of a grounded coplanar waveguide.

The grounded coplanar waveguide has a zero cut-off frequency, which makes it suitable for wideband applications. Much like the stripline the grounded coplanar waveguide has two ground planes, which require the same potential in order to prevent unwanted modes from propagating. If both ground planes are connected through vias the grounded coplanar waveguide has less tendency of radiating than the microstrip.

Mainly based on the low cost, the microstrip was chosen as design structure for the circuit design.

4.3.2. PCB substrate

With a design structure in mind the next step was to find a suitable PCB substrate. The choice of PCB substrate is essential since the electrical properties may vary with the frequency. The highest priority was to find a substrate that was suitable for high frequency applications, which correspond to a material with stable electrical properties. This is important since the impedance matching needs to be controlled throughout the frequency spectrum. The most common material is FR4 which has good dimensional stability, is good for multilayer buildups but has poor electrical properties. Based on the desired properties a material called UltraLam 3850 was chosen and its properties can be seen in table 4.2. It has a very stable dielectric constant and low stable dissipation factor, which makes it very suitable for the application.[21]

Table 4.2.: Ultralam 3850 substrate parameters.

Property	**Typical value**	**Unit**
Dielectric Constant, 3 GHz	2.9	-
Dissipation Factor	0.0025	-
Surface Resistivity	1×10^{10}	MΩ
Volume Resistivity	1×10^{12}	MΩcm

Table 4.3.: Standard thickness of the Ultralam 3850 substrate and copper cladding.

Standard thickness
0.001" (25 μm)
0.002" (50 μm)
0.004" (100 μm)

Standard copper cladding
½ oz. (18 μm)

The final layer buildup for the PCB with Ultralam 3850 as substrate and FR4 as laminate material can be seen in figure 4.10 and table 4.5. Note that it was designed as a three layer card with the ground plane in the middle.

4.3.3. Baseband modulator

The desired function of the modulator is to modulate the local oscillator (LO) signal, which is generated by the frequency synthesizer, using the modulation scheme D-BPSK. This can be done by mixing the encoded data stream with the LO signal using a XOR-gate, which works as a mixer. To achieve the functionality a XOR-gate that has fast rise time, low power consumption and is suitable for broadband applications was required. A circuit called HMC745LC3 was chosen and its properties are presented in table 4.4.[22]

The design of the modulator was based on the mixer and the demands it places on the circuit. Elements that are essential for the functionality are power supply voltage (V_{CC}), ground (GND), output voltage control (VR) and inputs and outputs to the mixer. To

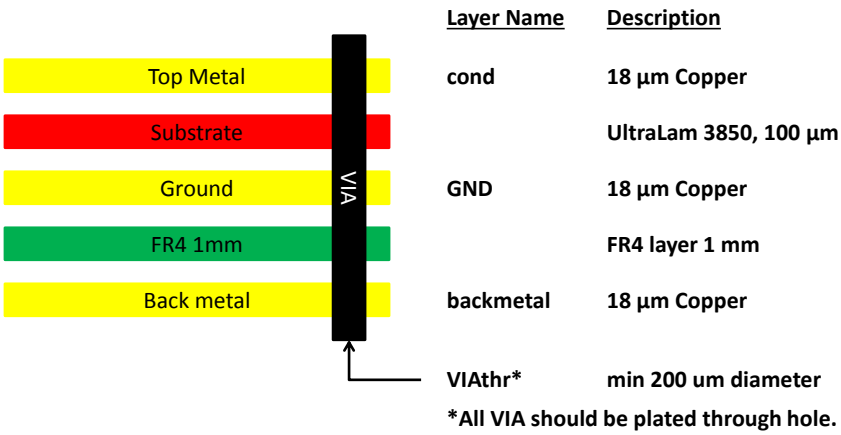


Figure 4.10.: The design stack for the PCBs.

Table 4.4.: HMC745LC3 parameters.

Parameter	**Min**	**Typical**	**Max**	**Unit**
Power Supply Voltage	3.0	3.3	3.6	V
Power Supply Current	-	72	-	mA
Maximum Data Rate	-	13	-	Gbps
Maximum Clock Rate	-	13	-	GHz
Input High Voltage	3.8	-	3.8	V
Input Low Voltage	2.1	-	3.3	V
Output Amplitude (Single-Ended)	-	550	-	mVp-p
Output Amplitude (Differential)	-	1100	-	mVp-p
Output Rise / Fall Time (20%-80%)	-	21 / 19	-	ps

visualise the elements essential for the mixer a simplified circuit diagram is visible in figure 4.11. AP and BP are positive inputs, AN and BN are negative inputs and DP and DN are positive and negative outputs respectively.

The physical dimensions of the conductors on the PCB affect the characteristic impedance, which in turn affects how well the wave can propagate. It can be shown that conductors with a characteristic impedance of 30 Ω gives the best power handling and conductors with a characteristic impedance of 77 Ω gives the lowest losses. The best compromise between them are approximately 50 Ω, which have been chosen as a standard for RF circuits. Therefore the width of the conductor lines have been calculated to ensure that the characteristic impedance is 50 Ω. The calculations have been done using a tool called LineCalc in ADS. LineCalc uses information about different parameters, including the substrate relative dielectric constant, thickness, dissipation factor and frequency, to calculate the width of the line to achieve a specified characteristic impedance.

To connect the front metal with the ground plane and back metal vias were used. In both cases the VIA was a plated through hole with a minimum diameter of 200 μm. If

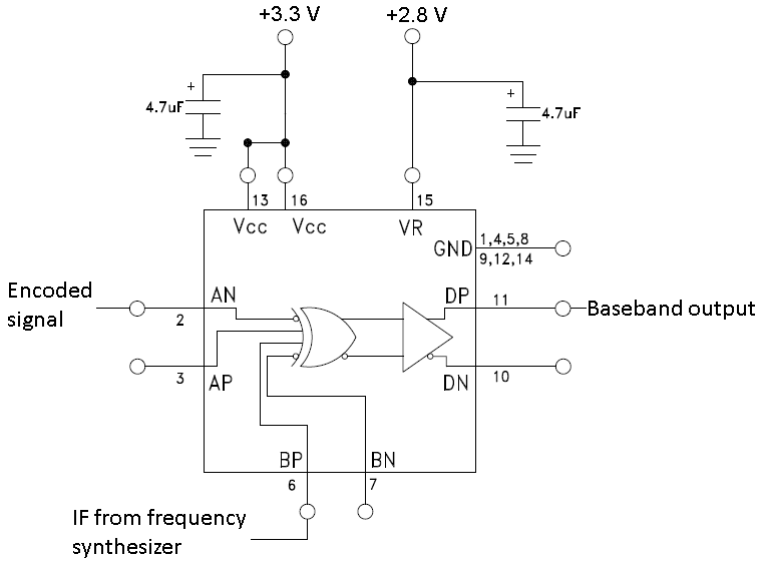
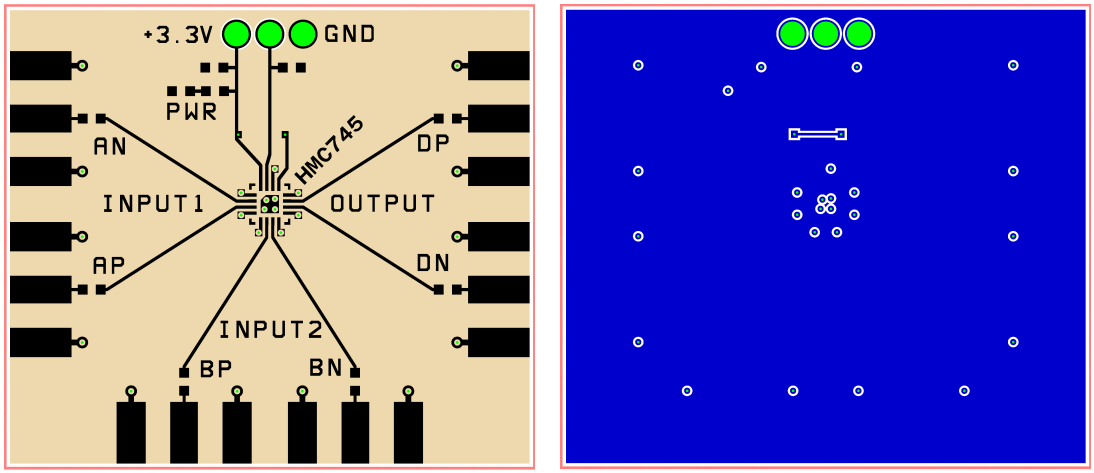


Figure 4.11.: Simplified circuit diagram of the baseband modulator.

the front and back metal are to be connected it is undesirable to connect the ground plane to. To avoid it from being connected, an opening in the ground plane is done that is slightly larger than the plated through hole, then the ground plane will remain unconnected as the plating is done.

To avoid DC signals from traveling through the system each input and output have a capacitor that acts as a high pass filter in series. To ensure good connectivity all inputs and outputs are connected with a SMA connector. The circuit is biased with +3.3V power supply and +2.8V output voltage control.

The final result of the baseband modulator can be seen in figure 4.12, which shows the front and the back of the PCB.



(a) The front of the baseband modulator.

(b) The back of the baseband modulator.

Figure 4.12.: The front and back of the baseband modulator.

4.3.4. Frequency synthesizer

As stated in section 4.3.3 the modulator is supposed to modulate an IF signal with the encoded data stream. To obtain the desired frequency, a PCB for a frequency synthesizer was designed. A frequency synthesizer is an electric circuit, which can generate a range of frequencies from a single frequency. The frequency synthesizer combines frequency multiplication, frequency division and frequency mixing to generate the desired frequency. To obtain a single frequency from which the synthesizer can generate the output frequency there is a PLL integrated inside. The PLL is a phase detector that locks on the phase of the incoming signal and then adjusts the phase of the frequency synthesizer to make sure that it does not drift. The input signal, from which the PLL detects the phase, comes from an oscillating crystal connected to the circuit.[23]

The PLL works on the principle of comparing a reference signal with a feedback signal generated inside the PLL. If the reference signal has higher frequency than the feedback frequency, the frequency detector signals "higher frequency" to the charge pump which generates a current. The current is sent into the loop filter, which converts the current to a control voltage, that bias the voltage controlled oscillator. The oscillator then oscillates faster and send a feedback signal to the phase frequency detector once again. When the reference and feedback signal has the same phase and frequency the process stabilizes.[24]

The frequency synthesizer that was chosen has a wide bandwidth, which is good if the IF has to be changed, it has a integrated PLL and high reliability over temperature changes. The frequency synthesizer is called WSN-4G+ and a simplified circuit diagram is available in figure 4.13.[25]

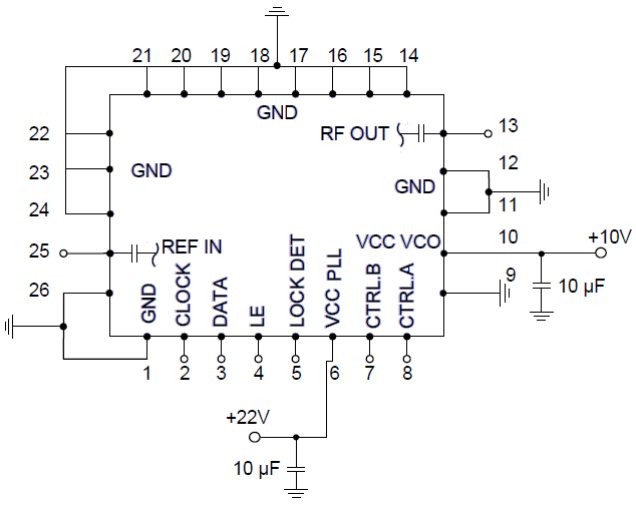
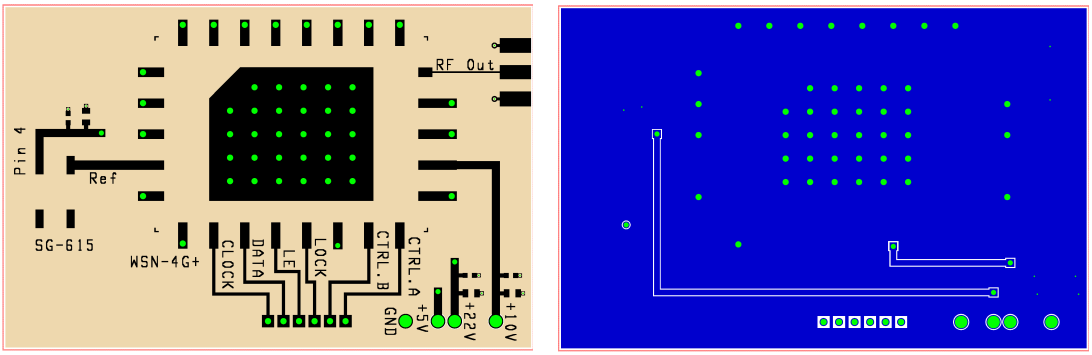


Figure 4.13.: The phase-locking loop circuit diagram.

In this process the high frequency conductors have been dimensioned for 50 Ω to avoid reflections. The rest of the design has been done with the same methodology as before. All RF and IF connections are connected with SMA connectors, all data pins

are connected with signal cables, all ground connections are connected to the ground plane and all VIAs are made as described in section 4.3.3. Unluckily the circuit requires three different voltage levels, +5V to the crystal, +10V to the frequency synthesizer and +22V to the PLL. The front and back of the frequency synthesizer can be seen in figure 4.14.



(a) The front of the frequency synthesizer. (b) The back of the frequency synthesizer.

Figure 4.14.: The front and back of the frequency synthesizer.

In order to generate the desired frequency the synthesizer has to be programmed at startup. The programming is done by a programmer implemented in the Cyclone IV GX FPGA, as described in 4.2.4.

4.3.5. Baseband demodulator

The function of the demodulator is to decode the incoming signal and recover the original data. The complete demodulation process is described in figure 4.15.

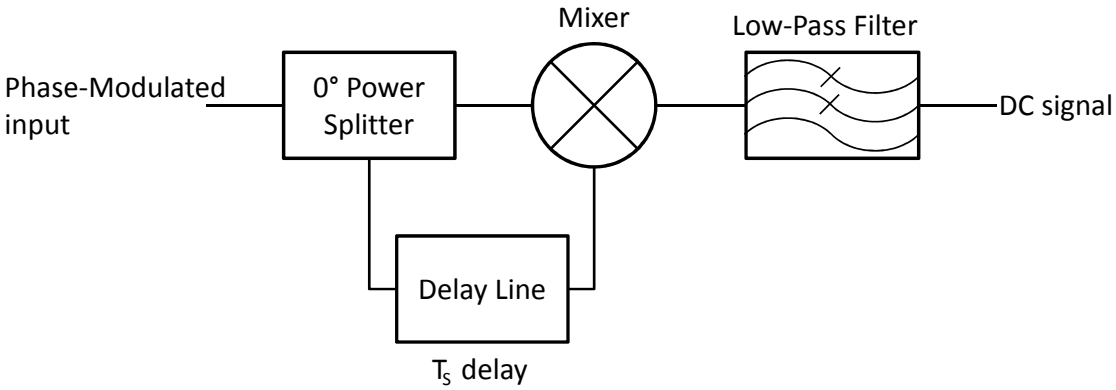


Figure 4.15.: A block diagram that shows the principle of the demodulator.

The theory behind the recovering process is described in section 3.3.3. The theory states that the signal has to be multiplied with a time delayed copy of itself, this is done by splitting the incoming signal into two using a power splitter. Since the incoming signal will be weak it is important that the power splitter only reduce the signal level by

3 dB, which corresponds to half power. It is also important that the power splitter does not introduce any phase shift to one of the signals since the signals will be compared in a later stage. Based on these specifications a suitable power splitter called RPS-2-30+ was found and used in the design.[26]

The time delayed copy should be delayed exactly one symbol in order to achieve the best possible output. To delay the signal one symbol a delay line was designed to be precisely one wavelength longer than the other line. The length is stated as an electrical length because waves travel with different speed in different materials, therefore the electrical length was converted to a physical length using the LineCalc tool described in section 4.3.3.

To verify the conversion from electrical length to physical length a transient analysis was carried out also using ADS, this analysis show that the symbol is delayed close to one symbol. In the simulation a bit sequence is simulated together with a 50 Ω line that is terminated with a 50 Ω load. To see if the delay is one symbol, the bit sequence is studied before and after the 50 Ω delay line. The simulation setup is visible in figure 4.16 and results can be seen in figure 4.17.

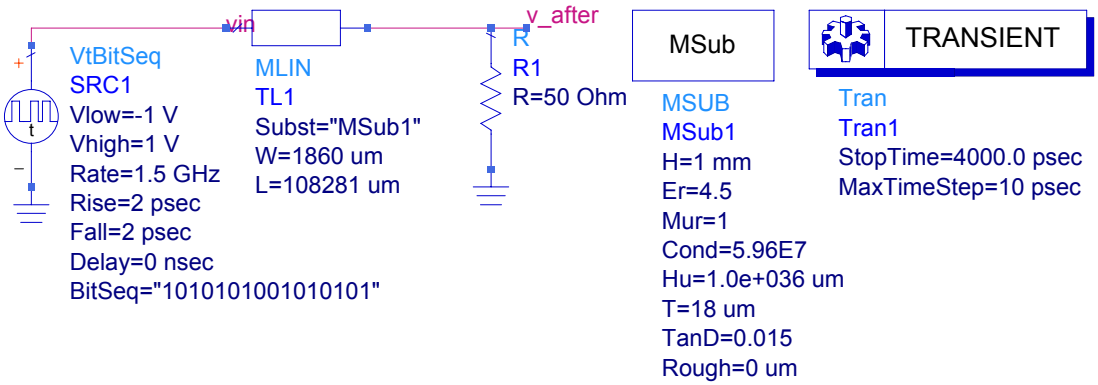


Figure 4.16.: The simulation setup in ADS for the transient analysis.

The multiplication of the current and previous symbol is done in the same type of mixer as in the baseband modulator. Since the mixer is the only active component in the circuit the biasing will be done in the same way as in the modulator with +3.3V to V_{CC} and +2.8V to VR. From the theory in section 3.3.3 it is known that the output from the mixer will consist of a varying DC signal and a signal with twice the IF. The desired signal is the DC signal and therefore the output will be low-pass filtered with a discrete component connected to the output SMA connector.

The delay line was also made with the possibility to be extended or shortened since there may be some delay introduced that was not accounted for. Besides the power splitter and delay line the baseband demodulator is quite similar to the baseband modulator and the first design can be seen in figure 4.18.

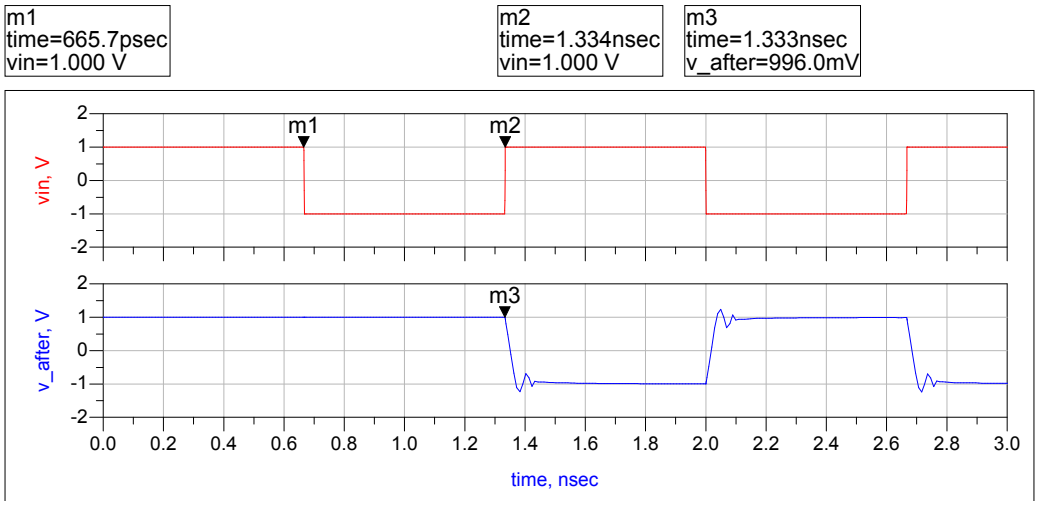
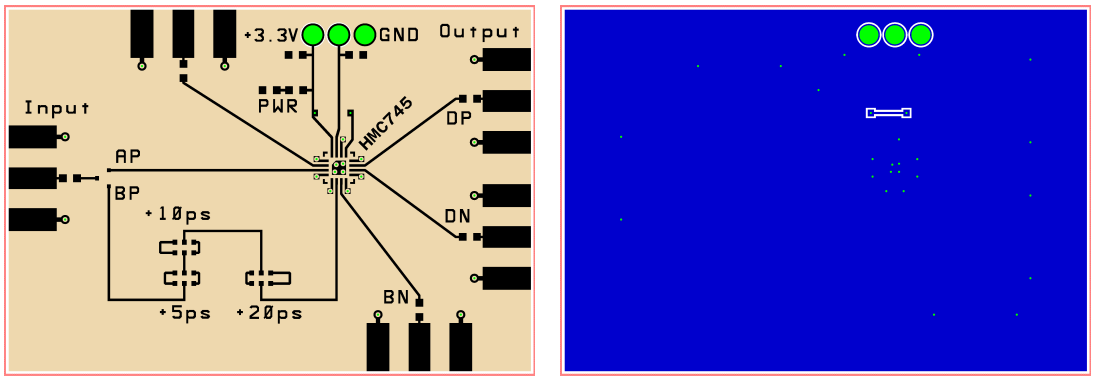


Figure 4.17.: The simulation results in ADS for the transient analysis.



(a) The front of the first baseband demodulator. (b) The back of the first baseband demodulator.

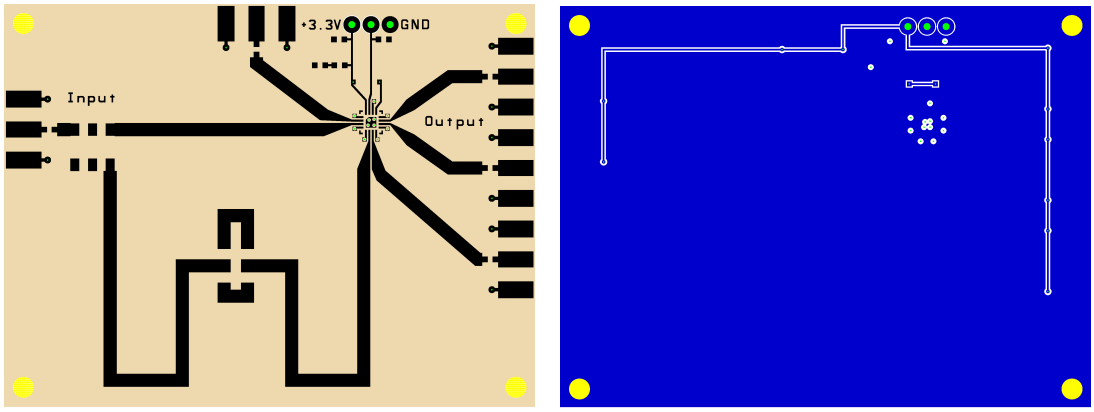
Figure 4.18.: The front and back of the baseband demodulator.

After the PCBs were ordered and initially tested it was found that the baseband demodulator was incorrectly designed. Due to a mistake in the previous planning the delay line was designed for 4 GHz instead of the symbol rate of 1.485 GHz. The baseband was redesigned with a new delay line and manufactured with a different PCB substrate, Shengyi S1141. The change of PCB substrate was based on availability, price and time to delivery. The properties of the new PCB substrate can be be seen in table 4.5.

Table 4.5.: Shengyi S1141 substrate parameters.

Property	**Typical value**	**Unit**
Dielectric Constant, 3 GHz	4.5	-
Dissipation Factor	0.015	-
Surface Resistivity	5.2×10^8	MΩ
Volume Resistivity	5.4×10^7	MΩcm

The new baseband demodulator also has the possibility to extend or shorten the delay line to ensure the correct electrical length. This is visualised in figure 4.19 which shows the front and back of the redesigned baseband demodulator.



(a) The front of the redesigned baseband demodulator.

(b) The back of the redesigned baseband demodulator.

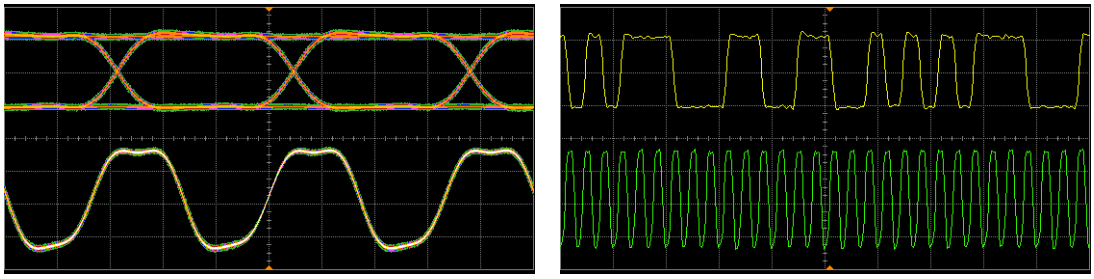
Figure 4.19.: The front and back of the redesigned baseband demodulator.

5. Results & discussion

This chapter starts with describing some general details of how the verification and measurements were conducted. The results from the tests are then presented for both the individual components and larger parts connected together. Due to insufficient time the radio front ends and antennas were never implemented in the system, hence all measurements have been done without these components. Discussions regarding the results are present throughout the chapter and at the end there is a final discussion.

5.1. Verification

The two sections below describe the methods used for the digital and analog parts respectively. For both the digital and analog parts, as well as the system tests, a pattern generator was used to generate a data output, which is known. Together with frequency synthesizers and oscilloscopes, different test setups were analyzed and verified. The output from the pattern generator can be either a predefined data sequence or a PRBS signal. More information about the PRBS signal is available in section 3.5.2. The predefined data sequence that has been used in the measurements is *"11100011001100101010"*, which is fairly easy to recognize in the output. The eye diagram and data pattern can be seen in figure 5.1.



(a) Eye diagram of the output.

(b) The data pattern.

Figure 5.1.: Output from the pattern generator.

Since the output from the pattern generator is practically noise free and well defined it is easy to see whether the cards introduce any noise or distortion to the signal.

5.1.1. Digital parts

The FPGA designs are mostly built up by smaller components whose functions are purely digital. In order to test every component the following work flow is used. After the code

is written the device under test (DUT) is simulated using a tool called Modelsim. After a successful simulation the signals in the DUT can be analyzed using an internal logic analyzer tool called Signaltap II. Finally, if possible, the outputs from the DUT can be measured using an oscilloscope, and in some cases the actual function can be verified. Figure 5.2 shows an example of a simulation of the frequency-synthesizer programmer using Modelsim.

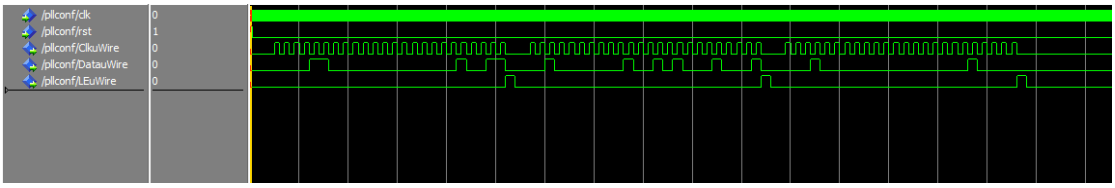


Figure 5.2.: Simulation of the frequency-synthesizer programmer in Modelsim using RTL code.

From figure 5.2 it can be verified that the behavior of the code is as expected, according to the data sheet of the component that is being programmed. This simulation is performed using RTL code, which is fast and usually enough. However, errors might occur in a later stage of the synthesis process, and if so, simulations can be ran again using gate-level simulation. This is based on a later stage in the synthesis and is more accurate regarding timings and code that may have been optimized away, but it is also much slower and therefore not used if not needed. Figure 5.3 shows measurement data from Signaltap II acquired from the component used in the simulation above but actually running on the FPGA.

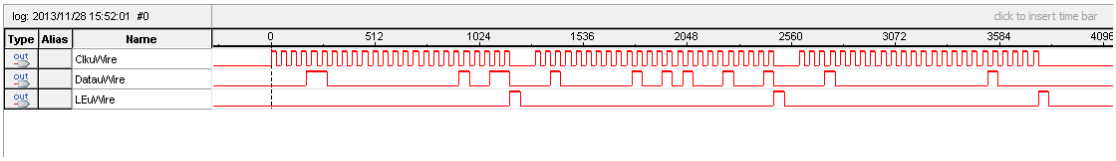


Figure 5.3.: Capture of the signals from the frequency-synthesizer programmer using Signaltap II.

In figure 5.3 it can be seen that the measurements from Signaltap II correspond to the waveforms in the Modelsim simulations. Figure 5.4 shows the same signals after they have been put out on actual wires and measured using an oscilloscope. Even though the signals in the figure contain some ripple they are considered to be very good, the most important parts of the waveform are the rising and falling edges. If all these steps are successful, and in this case when the frequency synthesizer behaves as expected when programmed, the DUT can be regarded as functional.

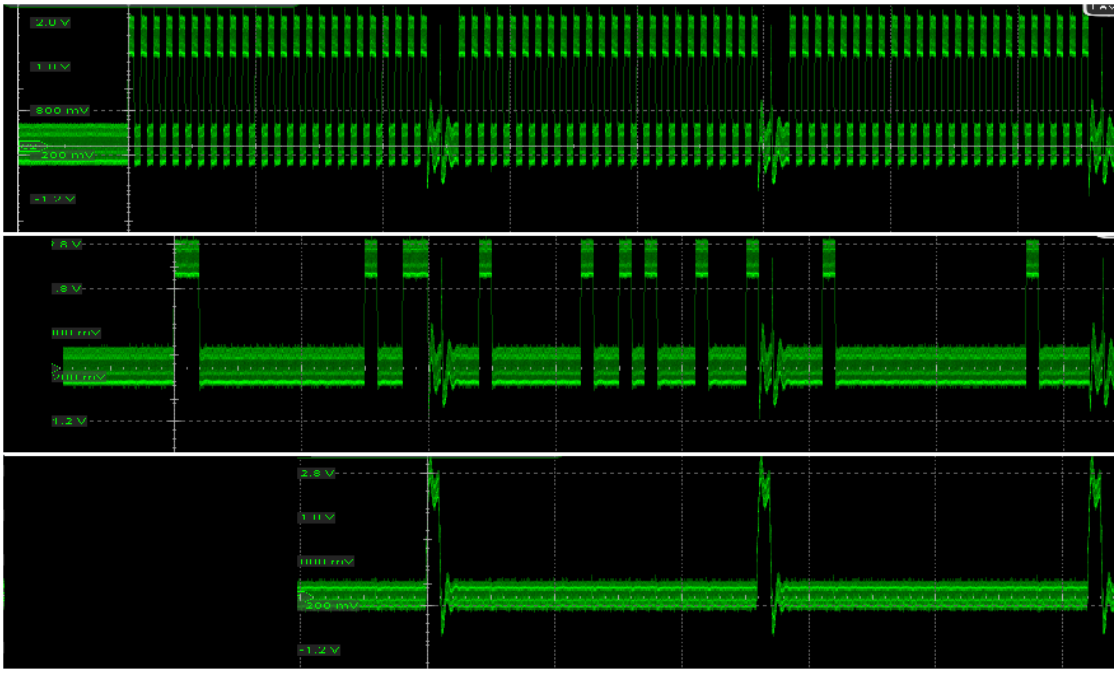


Figure 5.4.: Captures from the oscilloscope measurements of the frequency-synthesizer programmer output.

5.1.2. Analog parts

The baseband modulator PCBs were verified both individually and together in order to see how the signal gets distorted by the components. The performance of the system is mainly characterized by SNR and BER. For the measurements that require an IF signal it will be generated using a variable frequency synthesizer to analyse how the results vary with the frequency.

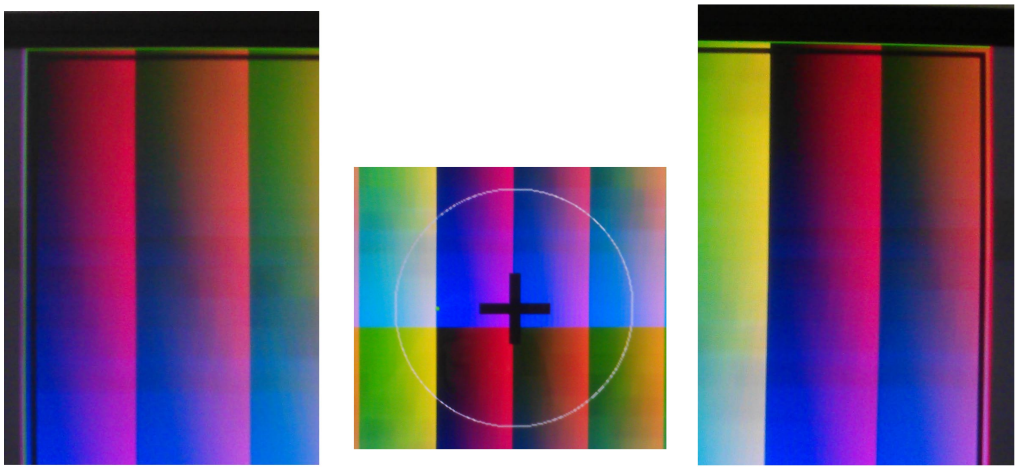
5.2. Video processing

This section accounts for the results of the tests performed with the Cyclone III based platforms alone. The components in the design have been verified using the method described in 5.1.1. The designs are relatively small and use only a limited part of the FPGAs available resources, two and five percent of the transmitter and receiver FPGAs logic elements. This is no surprise since these platforms do much of the video processing on separate circuits. Because of the low usage an even more basic FPGA could be used. Another option would be to integrate more of the functions into the FPGA and thereby increase the utilization.

5.2.1. Video transfer without encoding

During the three stages of the implementation described in section 4.2.3 all the parts were verified as working. The test image from the final design can be used to verify the

video output in a number of ways. Figure 5.5 shows parts of a photo of the test image output on a monitor.



(a) Signals out of sync. (b) Centre of test image. (c) Borders look correct.

Figure 5.5.: Three test image outputs from the video system.

From the test image a number of properties can be verified such as proportions, refresh rate and vertical and horizontal alignment. In picture (a) a thin pink line can be seen at the leftmost pixels. This occurred when the sync signals and the color data were out of sync. Picture (b) shows another part of the test image. Since the circle is completely round and the cross is equally long in all directions, the proportions of the image are correct. The small green square in the middle moves back and forth at a constant speed and since this is done without any glitches the refresh rate can be considered being correct. Picture (c) shows a border that is red as intended and therefore correctly aligned.

At a later stage the video transmitter and receiver was used to transfer a real video stream from a computer to a monitor. The test setup can be seen in figure 5.6.

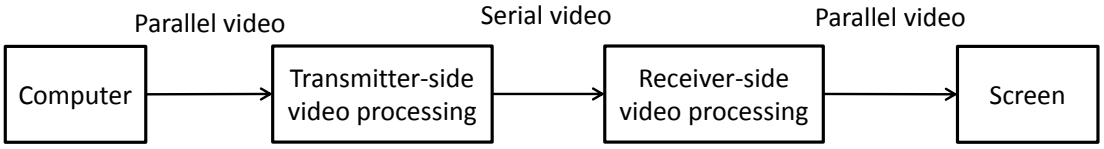


Figure 5.6.: Video test setup with the Cyclone III platforms.

This setup transferred the video signals without any visual problems. Since all components have been tested and the system actually transfers parallel HD-video data over a serial link it could be considered as working. Many of the components involved in the converting process are located outside of the FPGA and have not been designed in this project. Since these components are commercially available products and are widely

used and documented they can also be considered as problem free.

5.3. Baseband components

The baseband was first tested and evaluated componentwise to ensure that each component works and to examine how it affects the system. Secondly the components were tested together to see the combined results. The baseband consists of the differential encoder, modulator, frequency synthesizer and the demodulator.

5.3.1. Transceiver and differential encoding

The transceiver and the differential encoding was implemented on a Cyclone IV GX based platform. When all the individual components required for the transceiver to operate, such as the clock conditioner, were tested and implemented some measurements were made to verify the transceiver function with the encoding bypassed. By using a pattern generator and its built in BERT the BER can be calculated. When repeating the predefined data pattern *"11100011001100101010"* the function of the transceiver showed no errors. However, when using different lengths of PRBS signals instead the transceiver starts to output erroneous bits as the length of the sequence increases. Figure 5.7 shows the test setup and table 5.1 shows the results from the BERT.

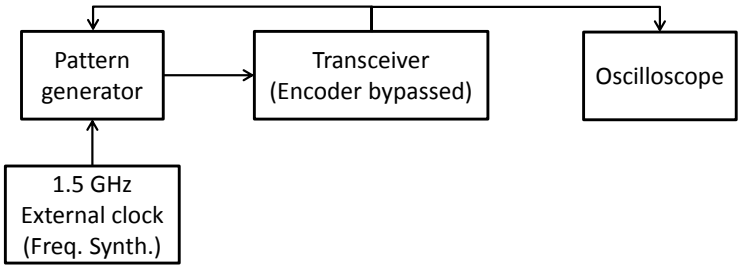


Figure 5.7.: Block diagram of the cyclone IV GX transceiver test setup.

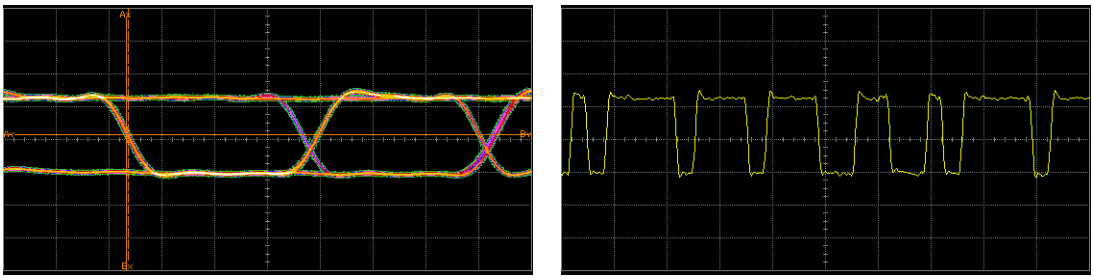
Table 5.1.: Measured bit error rate of the transceiver using different lengths of PRBS.

Length [bits]	**EC**	**BER**
$2^7 - 1$	0	0.0000×10^{-12}
$2^9 - 1$	0	0.0000×10^{-12}
$2^{10} - 1$	90011	3.0337×10^{-8}
$2^{11} - 1$	0	0.0000×10^{-12}
$2^{15} - 1$	175040	5.8995×10^{-8}
$2^{20} - 1$	447754	1.5091×10^{-7}
$2^{23} - 1$	358180	1.2072×10^{-7}
$2^{31} - 1$	419835	1.4150×10^{-7}

All the tests in the table ran for 33 minutes and 18 seconds, which is the time that gives a confidence level of 0.95 as long as no errors occur according to the formulas in section 3.5.2. The BER increases almost linearly with the grade of the PRBS except for two local maximas for $2^{10} - 1$ and $2^{20} - 1$. The absolute results vary quite a bit depending on the position of the placement of the cards and cables, both better and worse results have been acquired. The relative difference between the PRBS sequences stay the same though and the BER maximas at PRBS 10 and 20 exist in all cases. There are also some problems with occasional loss of synchronisation which makes the system reset automatically.

These results show that the transceiver works, but not without errors in all cases. Since the PRBS is designed to stress the system, as a random signal, it is pretty hard to handle. When using higher grades of PRBS the number of consecutive ones and zeros increases and therefore it gets harder for the transceiver to properly lock on the signal. The BER maximas at PRBS 10 and 20 are strange but observed in multiple tests. The reason for this remains unknown but something that can easily be seen is that the length coincides with the data bus width, which is 20 bits.

A continuous BERT with PRBS could not be performed for the transceiver with the differential encoding included, since the encoding modifies the information. However a test with the predefined data pattern as output from the pattern generator and the encoded counterpart as an expected input was run successfully. Figure 5.8 shows the encoded output from the transceiver.



(a) Eye diagram (b) Bit pattern waveform

Figure 5.8.: The encoded data output from the transceiver.

The signal quality is similar to the output directly from the pattern generator which can be seen in figure 5.1. This means that any noise introduced in the transceiver is negligible.

5.3.2. Modulator

The modulator was tested to see if it introduced any noise to the signal. To measure the performance of the modulator the input signal was compared with the output signal to see the amount of distortion introduced. The input signal was generated by the pattern generator and thus known from the beginning. The IF was varied using a frequency

synthesizer and the output was monitored using an oscilloscope. The complete test setup can be viewed in figure 5.9 and the results can be seen in figure 5.10.

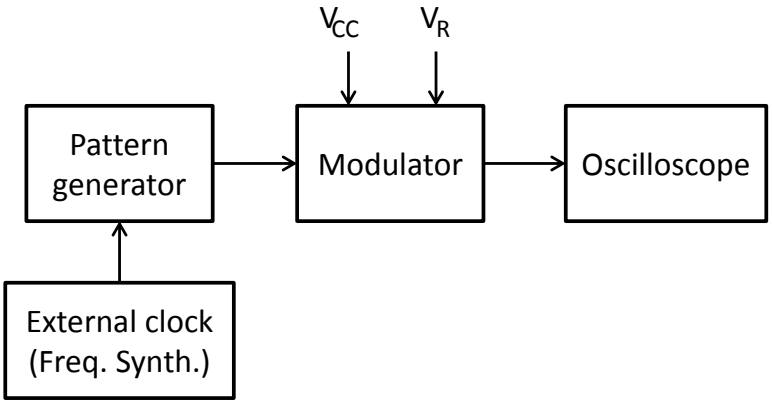
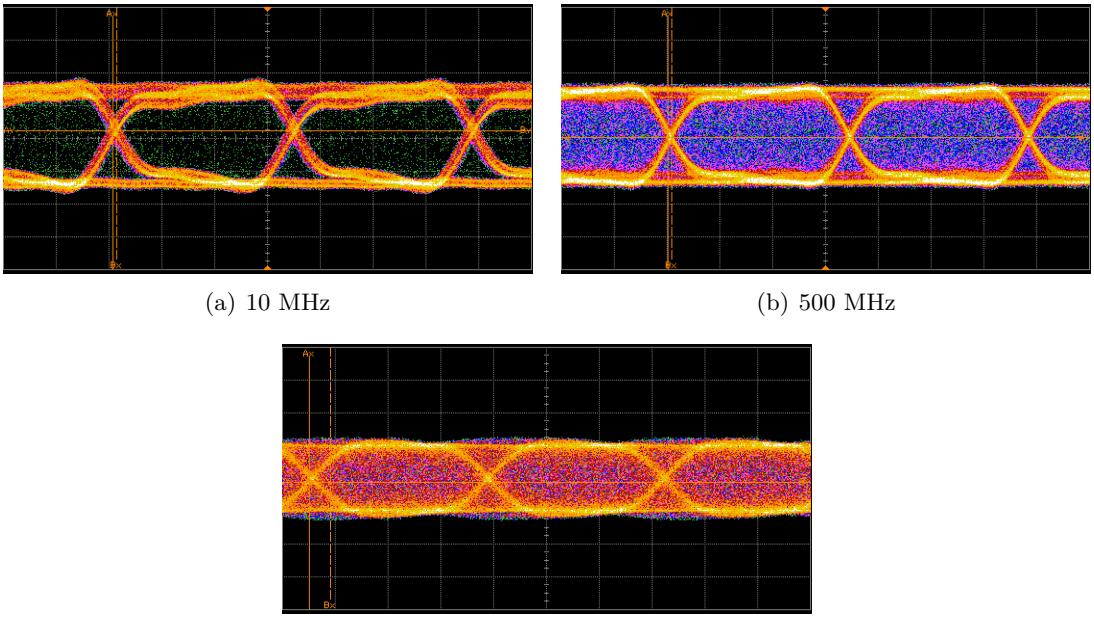


Figure 5.9.: Block diagram of modulator test setup.



(a) 10 MHz

(b) 500 MHz

(c) 1000 MHz

Figure 5.10.: Output from the baseband modulator for different intermediate frequencies.

The test results in figure 5.10 shows the output for different LO signals. A quite clear data signal is visible but there are another signal superimposed. Since the output shows an eye diagram together with another signal the functionality of the mixer is verified. The superimposed signal is most likely the LO signal, which becomes more intense as the frequency is getting higher. The circuit was tested with a LO signal at 3 GHz but it was impossible to distinguish any pattern in the output. It might be valuable to compare the frequency spectrum from the encoded signal with the spectrum from the mixed signal to see how the LO signal affects the output.

5.3.3. Frequency synthesizer

To test the frequency synthesizer it was programmed using the Cyclone IV GX FPGA. The FPGA sent a data pattern that specified the desired frequency at startup. The reference signal that is generated by the crystal was measured and confirmed before the output from the frequency synthesizer was verified. The test setup and measurements results can be seen in figure 5.11 and figure 5.12.

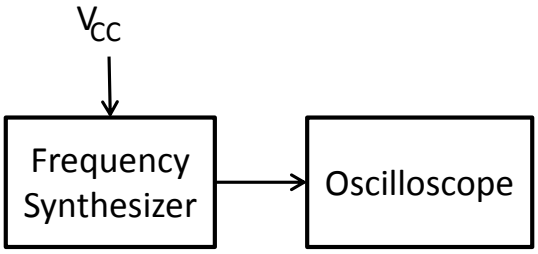


Figure 5.11.: Block diagram of frequency synthesizer test setup.

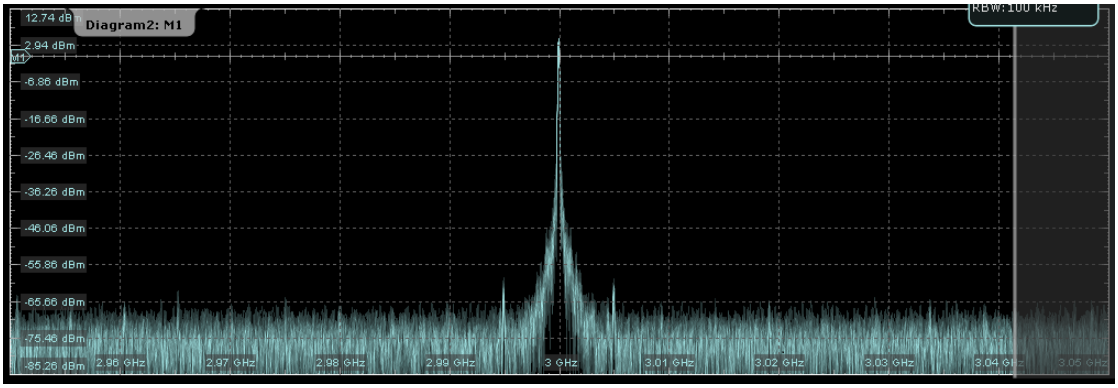
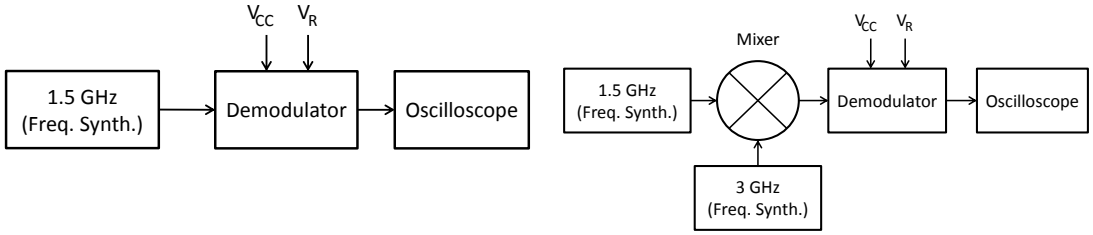


Figure 5.12.: The output signal generated by the frequency synthesizer.

In figure 5.12 the frequency spectrum from 2.95 GHz to 3.05 GHz is visible. The desired frequency at 3 GHz is clearly visible and very narrow. The output power peaks at approximately +3 dBm.

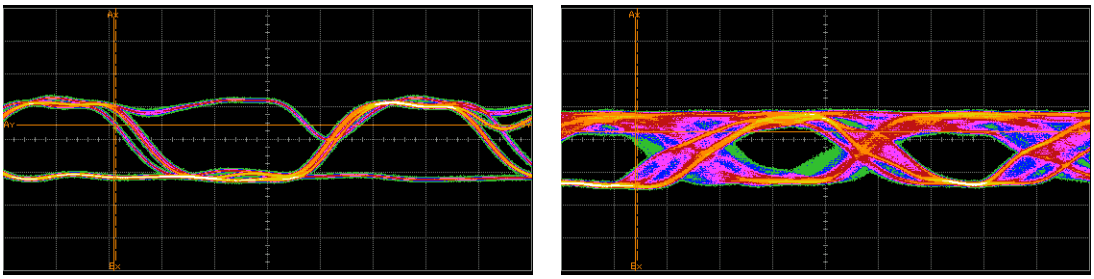
5.3.4. Demodulator

The first test of the demodulator was done in order to see if the demodulator introduces any noise. The demodulator was tested with an input signal consisting of a pure sine wave with frequency 1.5 GHz and amplitude +2 dBm, which was generated with a signal generator. Furthermore the demodulator was tested with an input signal consisting of two mixed sine waves, the first with a frequency of 1.5 GHz, representing the symbol frequency, the second with a frequency of 3 GHz to represent the intermediate frequency. The test setups and the test results are shown in figure 5.13 and figure 5.14.



(a) Pure sinusoidal wave input (b) Two mixed sinusoidal waves input

Figure 5.13.: Output from the demodulator for one and two sine waves.



(a) Pure sinusoidal wave input (b) Two mixed sinusoidal waves input

Figure 5.14.: Output from the demodulator for one and two sine waves.

The results in figure 5.14 show that a pure sine wave can pass through the demodulator without getting distorted. These tests were mainly conducted in order to verify the functionality of the mixer in the demodulator. The results also show that two mixed signals with a symbol rate of 1.5 GHz and intermediate frequency of 3 GHz gives the desired output, a data signal that varies between -1 and 1. Even though the signals are ideal the output contains alot of noise. This is most likely due to bad grounding and self-induced signals from the surroundings.

The results from the individual baseband components were taken into consideration in the following tests where the components were tested together to see their combined performance.

5.4. System results

The tests of the system were initially performed using the pattern generator as input to the complete baseband. The final test used a real video signal as input. Since the planned equipment for converting the optical video signals to electrical signals were unavailable during the tests the video processing functions could not be included in these tests.

5.4.1. Complete baseband tests

The baseband was tested at the intermediate frequencies that turned out to give the best outputs, which are multiples of 800 MHz. The reason why some frequencies give

a better result is that the constellation diagram rotates as the frequency changes. At multiples of 800 MHz the phase varies between approximately 0° and 180°. These tests were conducted with a pre-defined bit pattern. The test setup and the results can be seen in figure 5.15 and figure 5.16. Worth mentioning is that the results with an IF of 3200 MHz resulted in a very blurry output and is therefore not shown here.

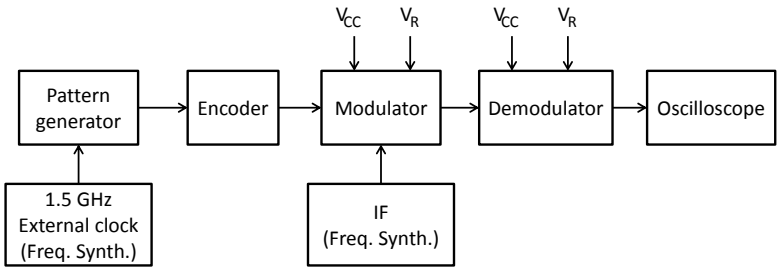
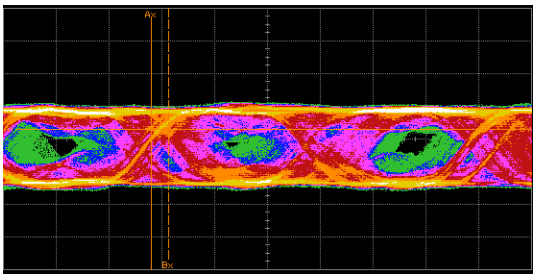
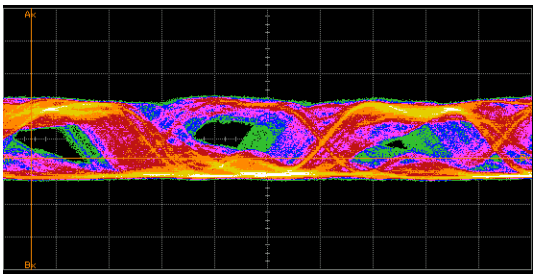


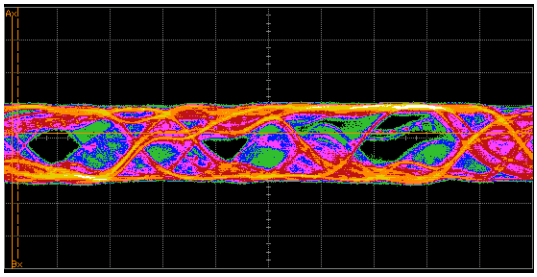
Figure 5.15.: Block diagram of baseband test setup.



(a) 800 MHz



(b) 1600 MHz

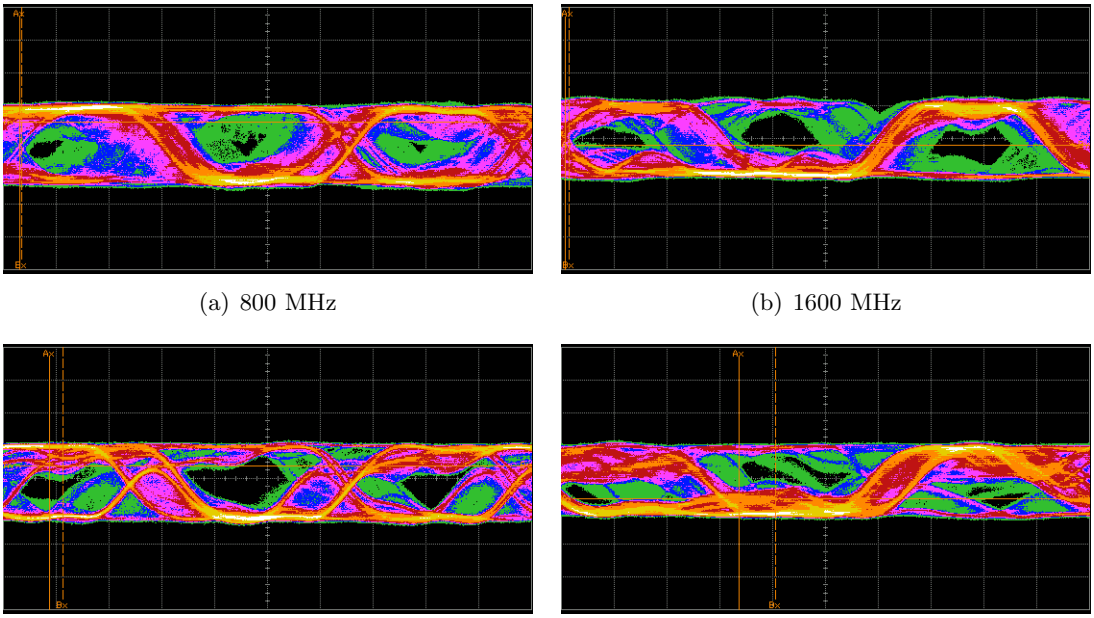


(c) 2400 MHz

Figure 5.16.: Output from the baseband for different intermediate frequencies.

From the results visible in figure 5.16 some kind of interference or reflection was suspected. The first action was to terminate all open inputs and outputs on the modulator and demodulator. In the subsequent test the open inputs on the modulator and demodulator were terminated using 50 Ω terminations. With terminations the output at an IF of 3200 MHz was improved enough to distinguish an eye diagram. The output eye diagrams can be seen in figure 5.17.

From these results it is clear that the suspected interference or reflection depend partly on lack of termination. Since the eye diagrams were not good enough, it was also

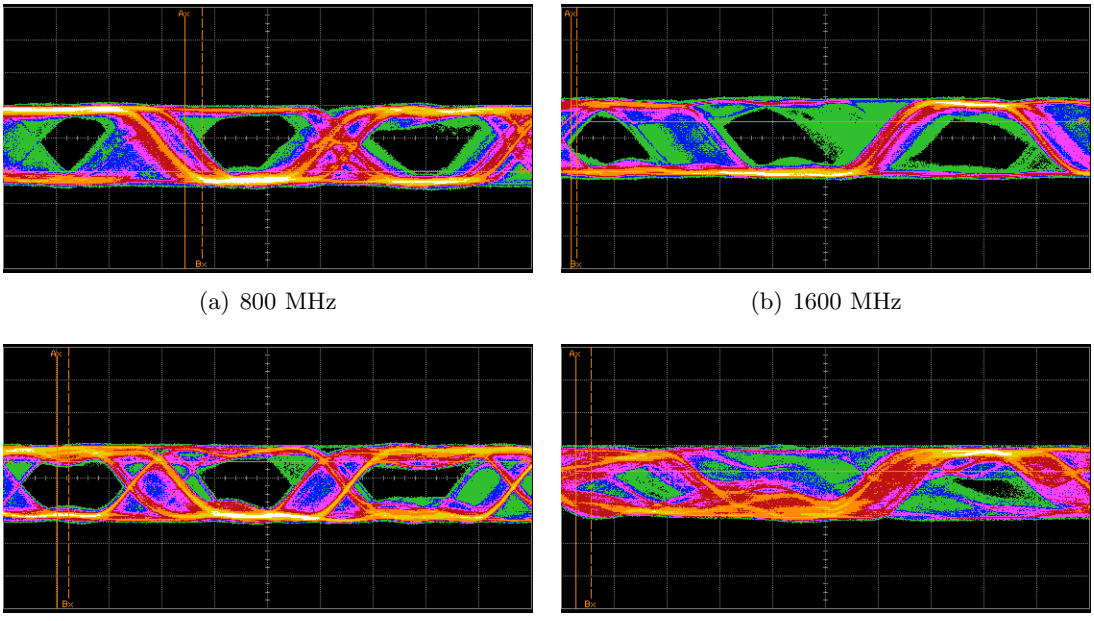


(a) 800 MHz (b) 1600 MHz

(c) 2400 MHz (d) 3200 MHz

Figure 5.17.: Output from the baseband with terminated inputs for different intermediate frequencies.

suspected that the mixer in the demodulator was compressed due to the power level of the incoming signal. Therefore the final tests performed on the baseband were done with a 3 dB attenuator between the modulator and demodulator. The results from these measurements are shown in figure 5.18.



(a) 800 MHz (b) 1600 MHz

(c) 2400 MHz (d) 3200 MHz

Figure 5.18.: Output from the baseband with terminated inputs and 3 dB attenuator for different intermediate frequencies.

In general the results became better with an attenuator between the modulator and demodulator. To see if the performance was affected by even more attenuation a BERT was used with different attenuations. Each test lasted 5 minutes and the attenuation varied from 0 to 9 dB. The measured performance is shown in table 5.2.

Table 5.2.: Measured bit error rate of the baseband using a pre-defined data sequence.

Number of bits	**Attenuation [dB]**	**EC**	**BER**
4.5×10^{11}	0	0	0.0000×10^{-12}
4.5×10^{11}	3	0	0.0000×10^{-12}
4.5×10^{11}	6	812990	1.8249×10^{-6}
4.5×10^{11}	9	-	-

From the BERT it is clear that more than 3 dB attenuation is undesired. This is most likely due to the power level of the signal that then becomes too low.

When using PRBS as input to the baseband no results were acquired, even though the signals actually looked relatively good when using an oscilloscope. One reason for this was that the data bus was flipped internally in the FPGA when using the differential encoder, but not when bypassing it. Unfortunately this was discovered when all measurements were already done.

5.4.2. Video transfer tests

To see if the system meets the desired specifications of video transfer a baseband test with video input were conducted. Instead of the video processing functions that were verified in section 5.2 another pair of HDMI to SDI converters were used. This was done because the project did not have the optical to electrical converters that were needed to connect the video-processing boards with the baseband. To perform the test a computer was connected to a converter, which in turn was connected to the baseband, which on the other side was connected to another converter. The test was mainly done to see if the performance of the system could handle the HD-SDI standard. Unfortunately the baseband did not perform good enough for the signal to be recovered. The test setup and the measured output from the baseband is shown in figure 5.19 and figure 5.20.

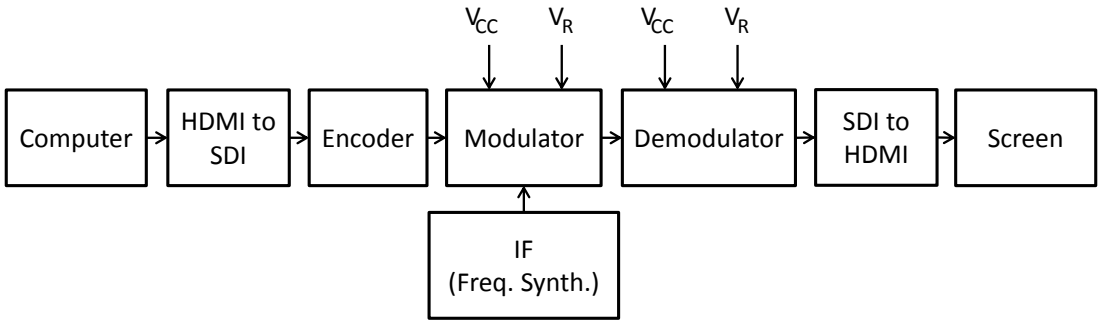


Figure 5.19.: Block diagram of video test setup.

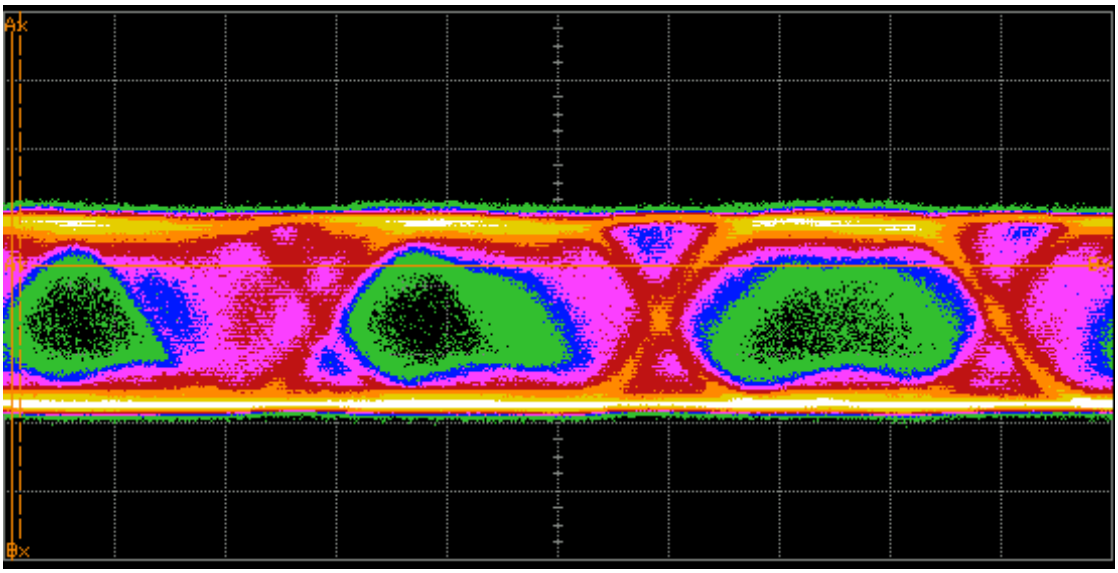


Figure 5.20.: The output from the baseband with HD-video as input signal.

In the figure it is clearly visible that the baseband do introduce a lot of noise. Again, the main reason that it does not work is probably the flipped data bus. That the video processing functions implemented in this project was not used together with the baseband in these tests is not of particularly big importance. Since that part was verified by itself it would most probably have worked together with a fully functional baseband too, as long as the right optical to electrical converters are used.

5.5. Further discussion

The hardware used in this project has both advantages and disadvantages. The platform used for the video processing is relatively cheap and easy to use. It does not offer much freedom in terms of I/O though, which can limit a developer who wants to implement additional functions. The optical receiver and transmitter do not really add anything but cost and complexity in this projects application. Because of this another platform

would be preferable for the video processing.

The Cyclone IV GX based platform used for the differential encoding offers sufficient performance at the data rates that this project aimed for. It also offers some I/O pins that can be used for additional functionality and interfaces. A dedicated clock output to the clock conditioner would have been good to have, which probably would have reduced the problems with grounding and interference, and contributed to a more consistent performance. The problem with the flipped data was due to a design flaw, and with this corrected the system should work without problems.

The designed PCBs proved to have the correct functionality but lack in performance due to the fact that neither one of the designers had any previous experience in designing PCBs. However, one of the goals was to use simple and cost effective methods, which led to the decision of designing the PCBs by ourselves. Since the PCBs were designed by ourselves the functionality was custom made for the application intended, which is crucial if the system should be cheap and simple. Also the choice of dividing the design into different PCBs turned out to be successful since the demodulator was improperly designed in the first draft.

Since the performance of the system was quite poor it is hard to say whether the link budget is accurate or not in relation to our system. All inputs to the link budget are either calculated or extracted from data sheets, and in our opinion therefore reliable.

Some quick tests have been carried out with the late discovered design flaws corrected and they show that all the digital parts of the system seem to work well enough. Problems with noise and the bad quality of the ground signal throughout the system still deteriorate the performance though. Maybe it would have been a good choice to limit this thesis to parts of the project, and instead spend more resources on details. On the other hand, if this had been done the system aspect of the project would not have been as clear.

6. Conclusion

The main purpose of the project was to design and implement a radio link as a proof of concept given certain prerequisites and specifications. The desired video processing functions have been implemented, as well as the baseband components. Based on theoretical studies D-BPSK was chosen as modulation technique. The tests that have been carried out also show that it has a data capacity high enough for HD-SDI signals.

Due to lack of time and problems that were solved too late no tests of a complete system including 60 GHz front ends and antennas were performed. Some problems also remain with the quality of the signal which suffers from bad ground and interference from unwanted signals. The low signal-to-noise ratio is good enough for test benches in the lab, but probably not sufficient for wireless transmission over the desired distances.

The fact that data has been transferred through the system without errors show that the system is indeed a proof of concept. But since the performance in terms of signal quality is quite bad, future work should focus on improving the signal-to-noise ratio. Together with radio front ends and antennas the system designed in this project could then form a fully functional wireless point-to-point link for transmission of high definition video.

7. Future work

This chapter presents some suggestions for future work in order to improve the stability and functionality of the system.

7.1. Improved stability

In order to go from proof of concept to a robust product that works out on the field the system needs to become more stable and have a better SNR. Possible solutions to this problem would be to resolder all components that have been mounted and use more rigid cables and connectors. Another FPGA on the receiver side could also increase the performance and consistency of the system. Some kind of shielding to reduce the influence of outer unwanted signals should also improve the SNR.

7.2. Implement radio front ends

In order to create a complete system, front ends and antennas need to be integrated. Since the system is designed with this in mind it should already be compatible, so the most crucial thing is SNR. When the system is completed tests and measurements can be conducted in various environments and at different distances.

7.3. Increased data bandwidth

A higher data bandwidth should be achievable but would require some modifications to the design.

7.3.1. More capable FPGA platforms

The actual differential-encoder design is supposed to be functional for up to 10 Gbit/s according to the cited reference [8]. The FPGAs and their on-chip transceivers however need to be upgraded since the maximum speed that can be handled by the Cyclone IV GX, that has been used in this project, is 2.5 Gbit/s.

7.3.2. Higher-order modulation

If the data rate would be doubled using D-BPSK the radio bandwidth would also be doubled. This would lead to problems, therefore a higher-order modulation scheme can be used to pack more data into the same radio bandwidth. A first step would

be to use D-QPSK, which is similar to D-BPSK but contains two bits per symbol. It should be possible to implement this using the same hardware with not too much development. D-QPSK also requires a bit higher SNR compared to D-BPSK, which needs to be considered.

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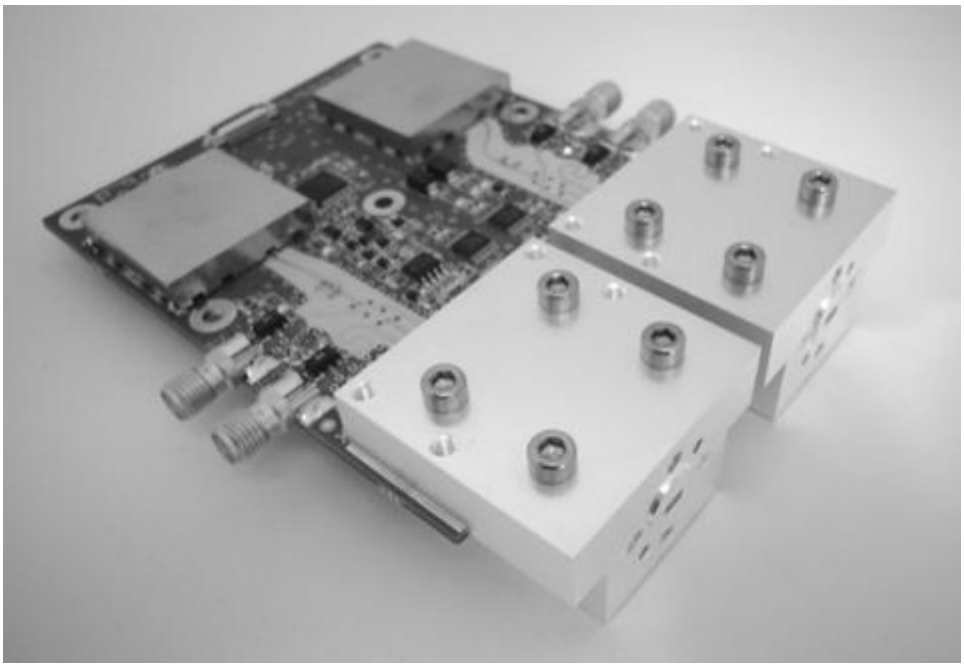
A. Front end

The following pages contain the data sheet for the front end given in the project.

FC1005V/00
58-63 GHz V-band Converter with LO



General

This converter platform is a broadband and versatile building block for V-band (58-63 GHz) applications. The platform is easily modified to customer requirements. It consists of one up- and one down-converter in a single unit. The up- and down-converter operate independently, and can thus be used in both frequency multiplexed and time multiplexed applications. The FC1005V/00 utilizes on-board LO synthesizers. Waveguide filters and diplexers are available as options.

Features

- 58-63 GHz RF bandwidths (usable from 57-66 GHz)
- Platform concept, easy to customize
- 1.0-5.0 GHz IF bandwidth
- Small size and weight
- Standard waveguide and SMA interfaces

The basic V-band platform possesses a very broad IF bandwidth, from 1.0 to 5.0 GHz. A set of two identical V-band modules can be used in a full duplex configuration by appropriate choice of LO signals for the up- and down-converter respectively. The converter is controlled through a standard I2C interface.

Applications

- Point-to-point or multi-point radio
- Multi-Gbps wireless transfer
- Measurement systems
- Any application requiring a high-quality mm-wave signal source

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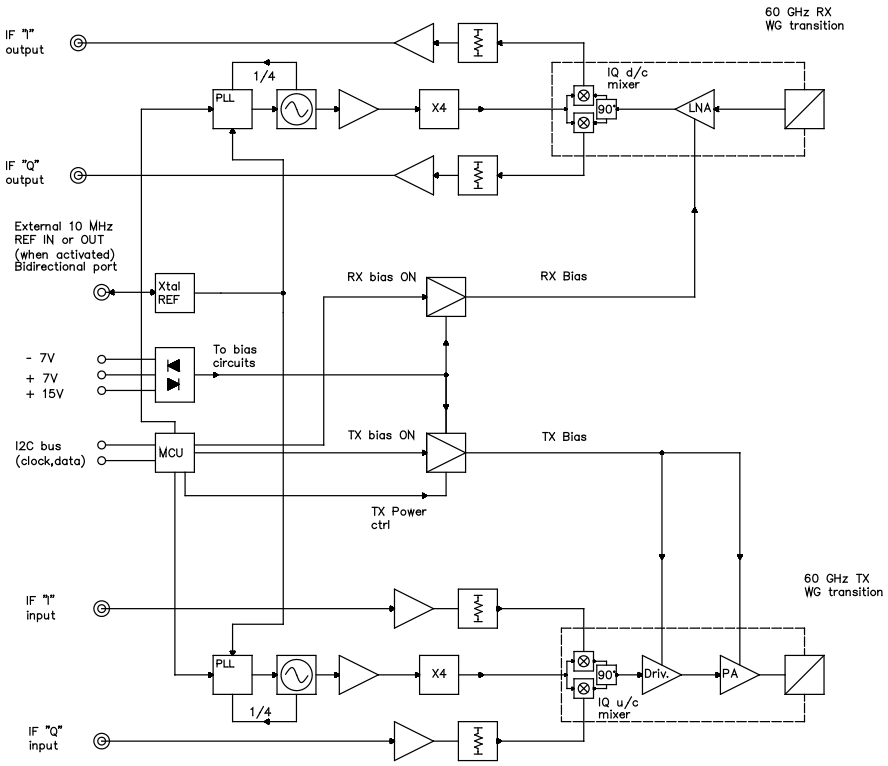
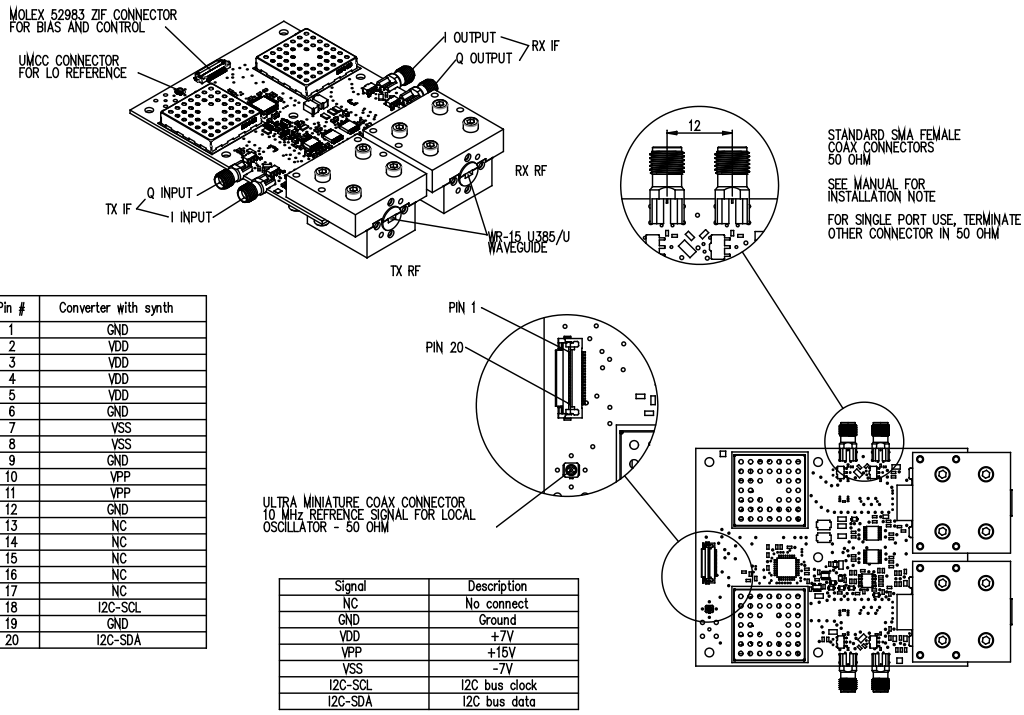
FC1005V/00
58-63 GHz V-band Converter with LO

Block Diagram



Interfaces



Pin #	Converter with synth
1	GND
2	VDD
3	VDD
4	VDD
5	VDD
6	GND
7	VSS
8	VSS
9	GND
10	VPP
11	VPP
12	GND
13	NC
14	NC
15	NC
16	NC
17	NC
18	I2C-SCL
19	GND
20	I2C-SDA

Signal	Description
NC	No connect
GND	Ground
VDD	+7V
VPP	+15V
VSS	-7V
I2C-SCL	I2C bus clock
I2C-SDA	I2C bus data

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FC1005V/00
58-63 GHz V-band Converter with LO

SIVERSIMA

Transmit Up-Converter				
Parameter	**Min**	**Typical**	**Max**	**Units**
RF output frequency range design/measured*	58-63			GHz
RF output frequency range operational, not guaranteed	57-66			GHz
IF input frequency range*	1		5	GHz
Nominal gain IF to RF*	25		40	dB
1-dB output compression point*	10			dBm
Saturated output power*	16			dBm
OIP3	20	25		dBm
LO phase noise @ 100 kHz offset @ V-band			-80	dBc/Hz
LO synthesizer frequency range	56.8		59.6	GHz
LO synthesizer step size @ V-band		0.25		MHz
Noise power density at waveguide output		-125		dBm/Hz
LO leakage (at port)		10	15	dBm
Gain flatness over frequency*			10	dB/GHz
Group delay variation		1		ns/GHz
RF Return loss		TBD		dB
IF Return loss	10			dB
I/Q balance phase		TBD		degrees
I/Q balance amplitude		2	4	dB
Image rejection	10	20		dB

*** Value 100% production tested; all other values indicative.**

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FC1005V/00
58-63 GHz V-band Converter with LO

SIVERSIMA

Receive Down-Converter				
Parameter	**Min**	**Typical**	**Max**	**Units**
RF output frequency range design/measured*	58-63			GHz
RF output frequency range operational, not guaranteed	57-66			GHz
IF output frequency range*	1		5	GHz
Nominal gain RF to IF*	8		20	dB
Noise figure *		8	10	dB
1-dB input compression point	TBD	TBD		dBm
LO phase noise @ 100 kHz offset @ V-band			-80	dBc/Hz
LO synthesizer frequency range	56.8		59.6	GHz
LO synthesizer step size @ V-band		0.25		MHz
Gain flatness over frequency		1	2	dB/GHz
Group delay variation		1		ns/GHz
Image rejection	10	14		dB
RF Return loss		TBD		dB
IF Return loss	10			dB
I/Q Balance Phase		TBD		deg
I/Q Balance Amplitude		2	3	dB

*** Value 100% production tested; all other values indicative.**

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Physical, Electrical and Environmental				
Parameter	**Min**	**Typical**	**Max**	**Units**
Operating temperature	-30		70	°C
Storage temperature	-50		80	°C
Humidity			90	% relative @25°C
Shock		Meets EN 300 019-2-4		
Vibration		Meets EN 300 019-1-4 Class 4.1		
VSS voltage*	-6.75		-7.25	V
VSS current consumption*		50	60	mA
VDD voltage *	6.75		7.25	V
VDD current consumption*		1260	1300	mA
VPP voltage *	14.75		15.25	V
VPP current consumption*		20	30	mA
Total power consumption*		9.5		W
External reference level	0.5	1	3	V (peak-to-peak)
External reference input frequency		10		MHz
Internal reference output frequency		10		MHz
Internal reference output frequency accuracy	-5		5	ppm
Internal reference output level		3		V (peak-to-peak)
Overall dimensions			117x80 x26	mm
Weight		≈ 200		g

*** Value 100% production tested; all other values indicative.**

Interfaces	
Waveguide input/output WR 15	UG-385/U
Control and bias connector	Molex 52893-2095
SMA connectors	SMA female
External/internal reference connector	UMCC

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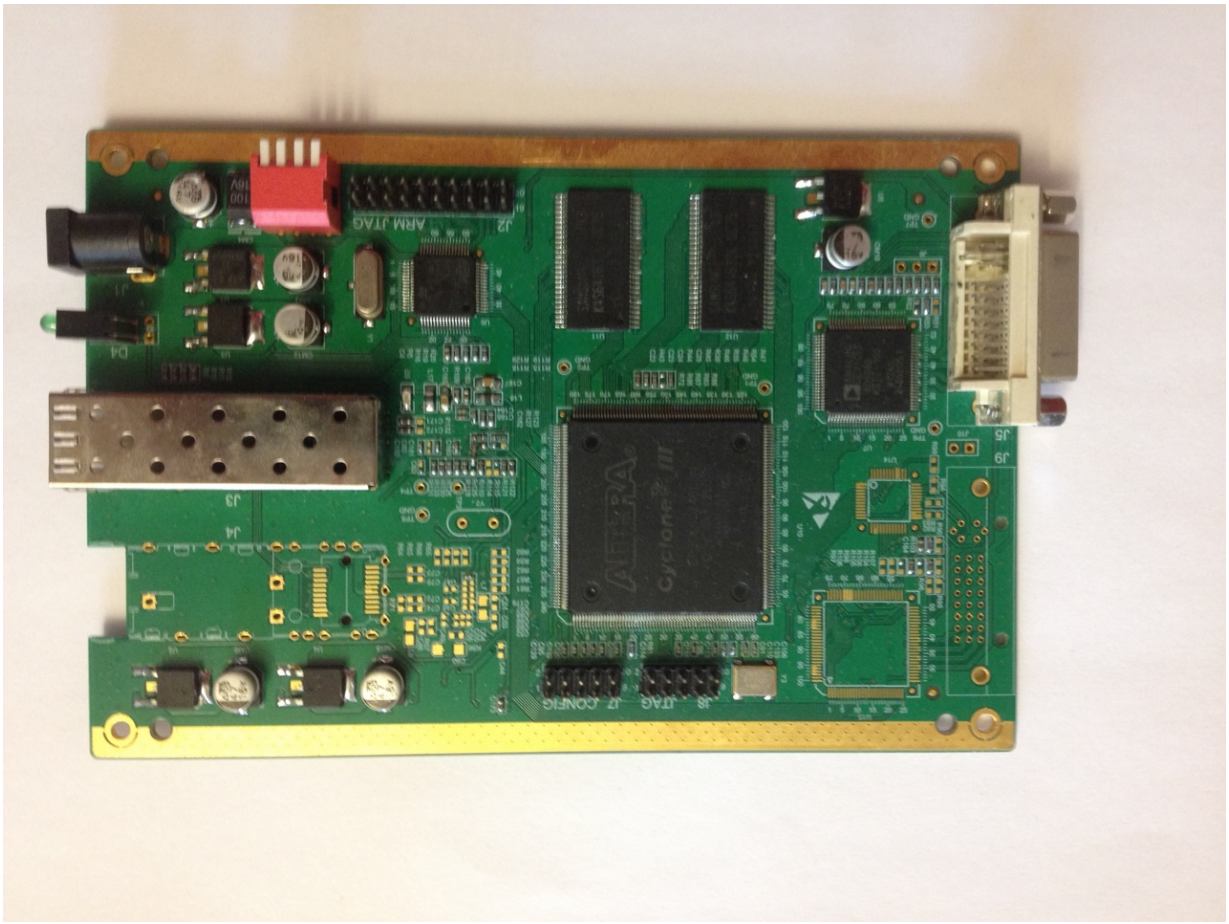
B. Link budget

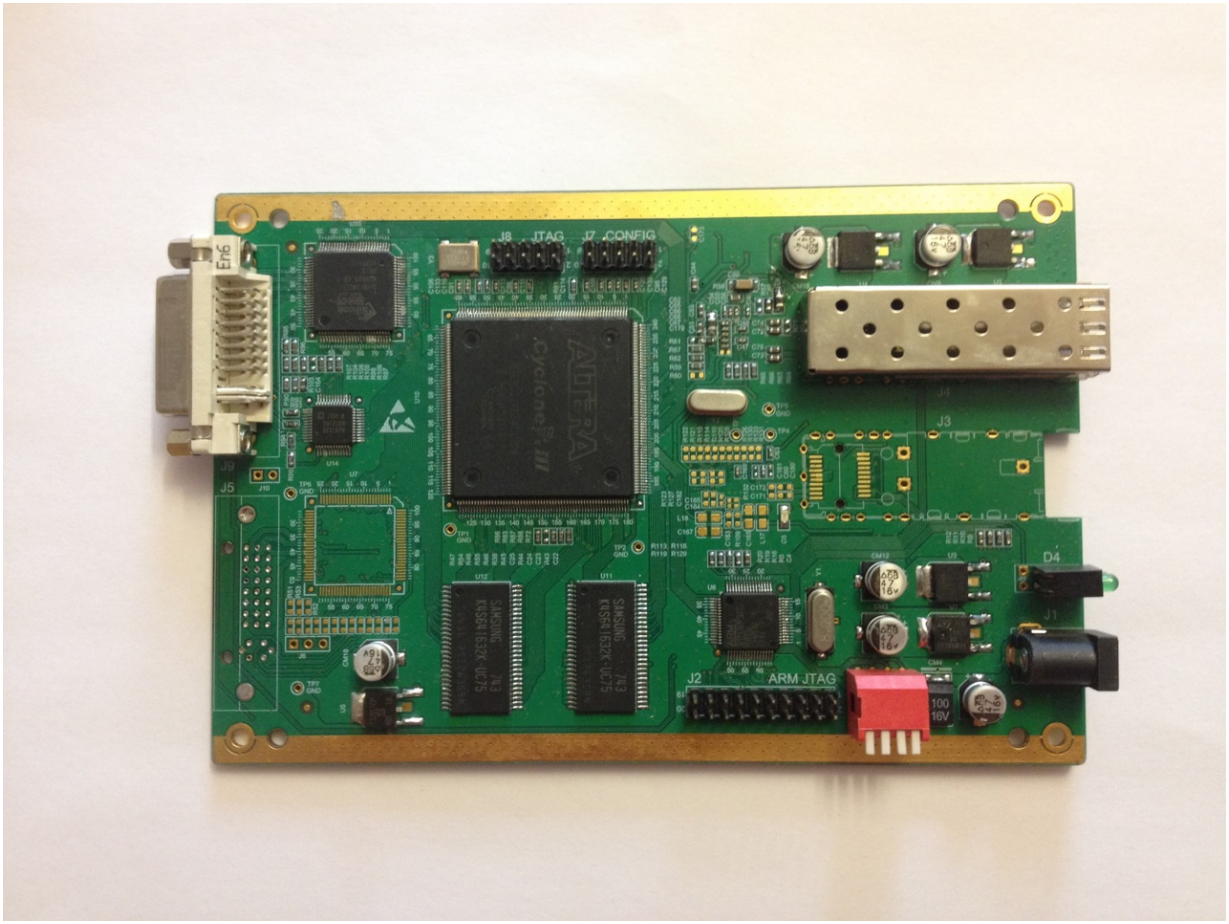
What	Value	Unit	Comment
Frequency	6,00E+10	Hz	
Wavelength	0,005	m	
Polarization	Hor/Ver		Vert. is better for rain
Link distance	300	m	
Tx power from modem	-17	dBm	
Tx loss	-1,5	dB	Coupling losses
Radome loss	-0,7	dB	
Front-end gain	25		(Min 25, Max 40), 1-dB comp. = 10 dBm
Tx antenna gain	34,4	dB	Using reflector antenna
EIRP	**40,2**	**dBm**	Max. 40 dBm (according to PTS)
Path loss	-117,547	dB	20*log(4*pi*L/lambda)
Tx pointing error	-1	dB	
Rain loss	-2,429086	dB	0,01% -> 22 mm/hr (Vert. Pol.)
Multipath	0	dB	Due to high attenuation of 60 GHz
Atmospheric loss	-4,5	dB	Approx. -15 dB/km
Total path loss	**-125,4761**	**dB**	
Radome loss	-0,7	dB	
Rx antenna gain	34,4	dB	Using reflector antenna
Polarization loss	0	dB	
Rx loss	-1,5	dB	Coupling losses
Rx pointing error	-1	dB	
Back-end gain	8		(Min 8, Max 20)
Total Rx gain	**39,2**	**dB**	
Recieved signal level	**-46,07605**	**dBm**	
Power splitter	-3	dB	For signal determination in demodulator
Rx noise figure	8	dB	Using FC1005V/00 Front end
Noise bandwidth	3,00E+09	Hz	
Bandwidth noise	-79	dBm	10*log(k*T0*B*1000)
Total noise power	-71	dBm	
MDS	**-49**	**dBm**	Minimum Detectable Signal
Signal-to-noise ratio	**22,1**	**dB**	Have to be 12,6 dB (for D-BPSK)
Availability	99,99	%	Downtime each year due to heavy rainfall
Downtime	0,876	hours / year	
Downtime	53	min/year	

C. Photos of FPGA platforms

C.1. Cyclone III based platforms

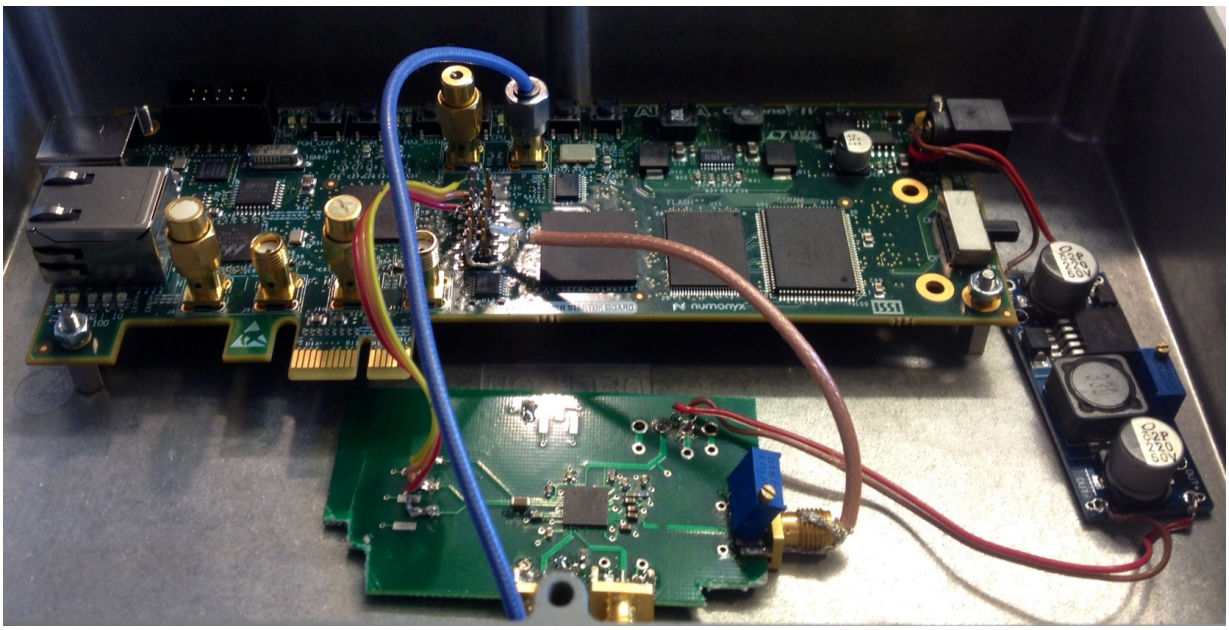


The Cyclone III board used on the transmitter side.



The Cyclone III board used on the receiver side.

C.2. Cyclone IV GX based platform

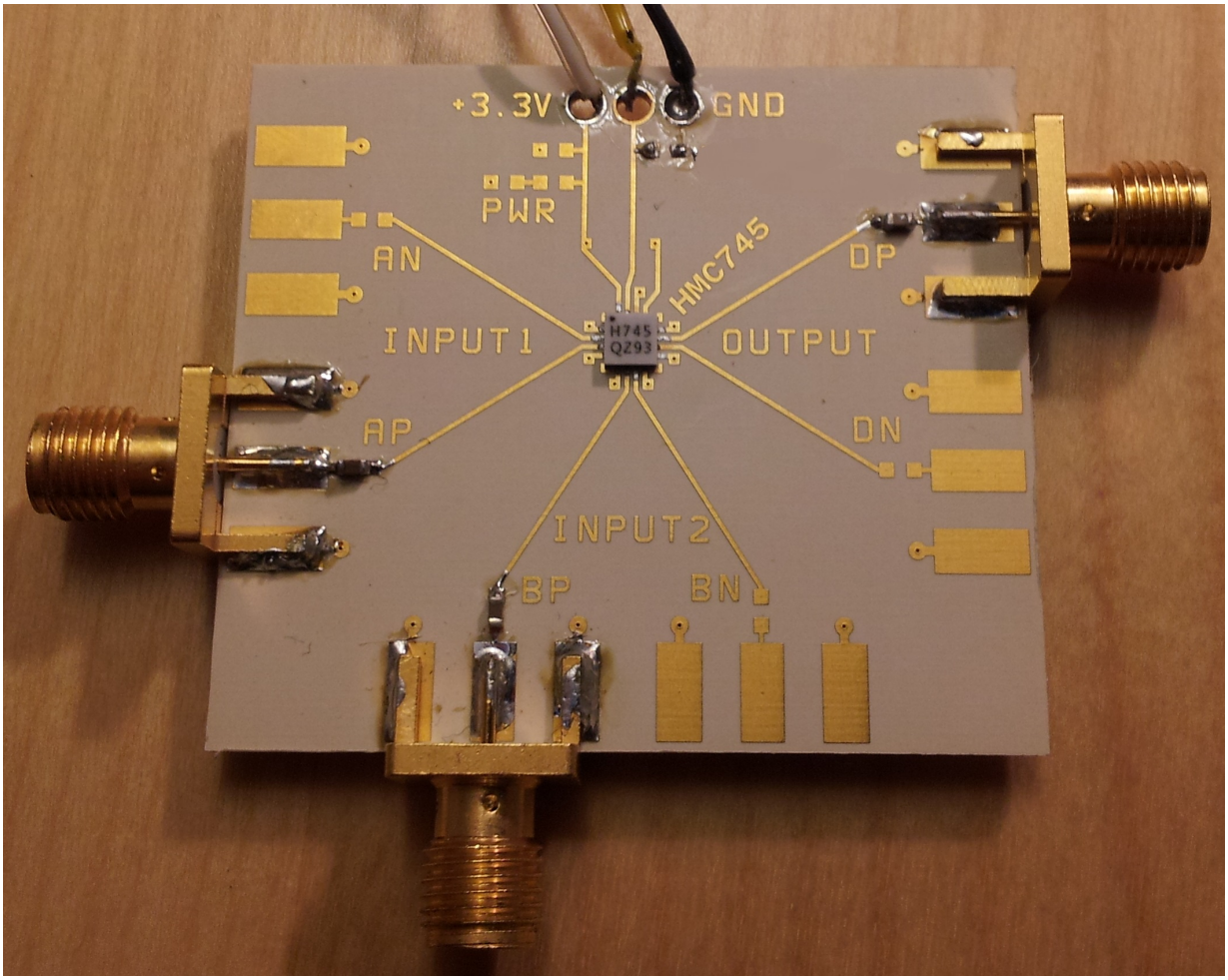


The Cyclone IV GX board with the clock conditioner and a power supply.

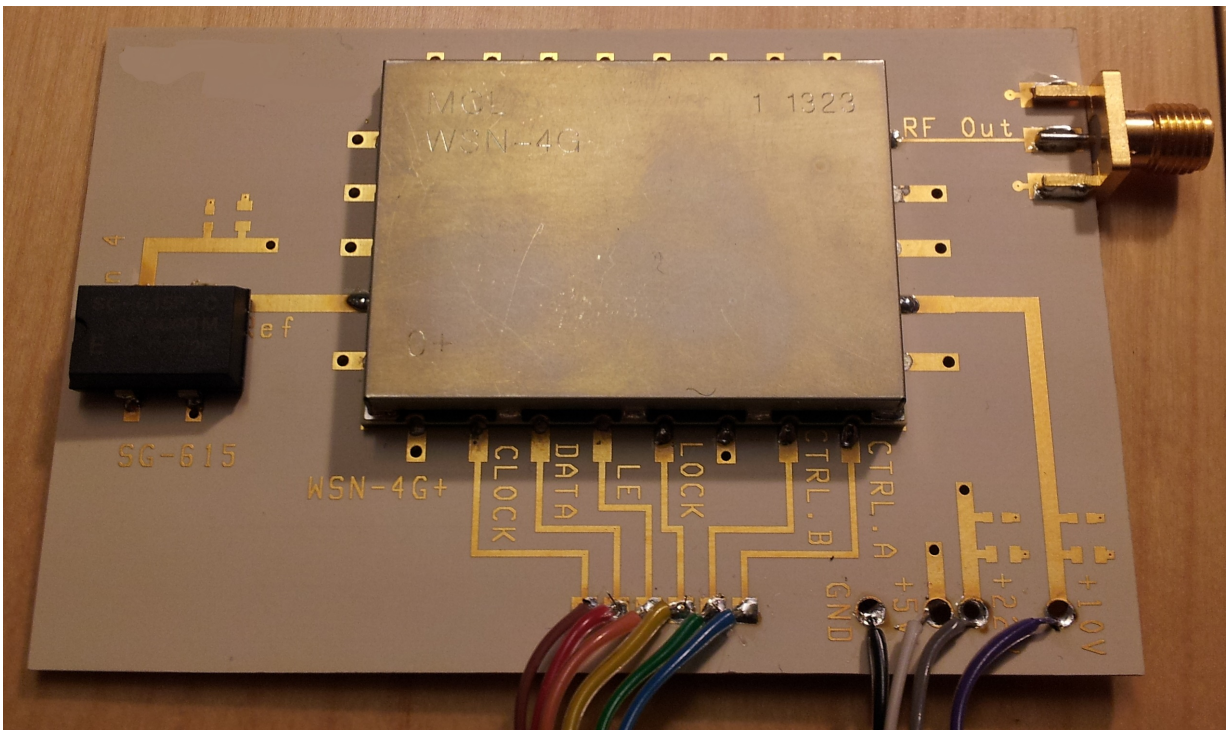
C.3. Arria V GX based platform

D. Photos of PCBs

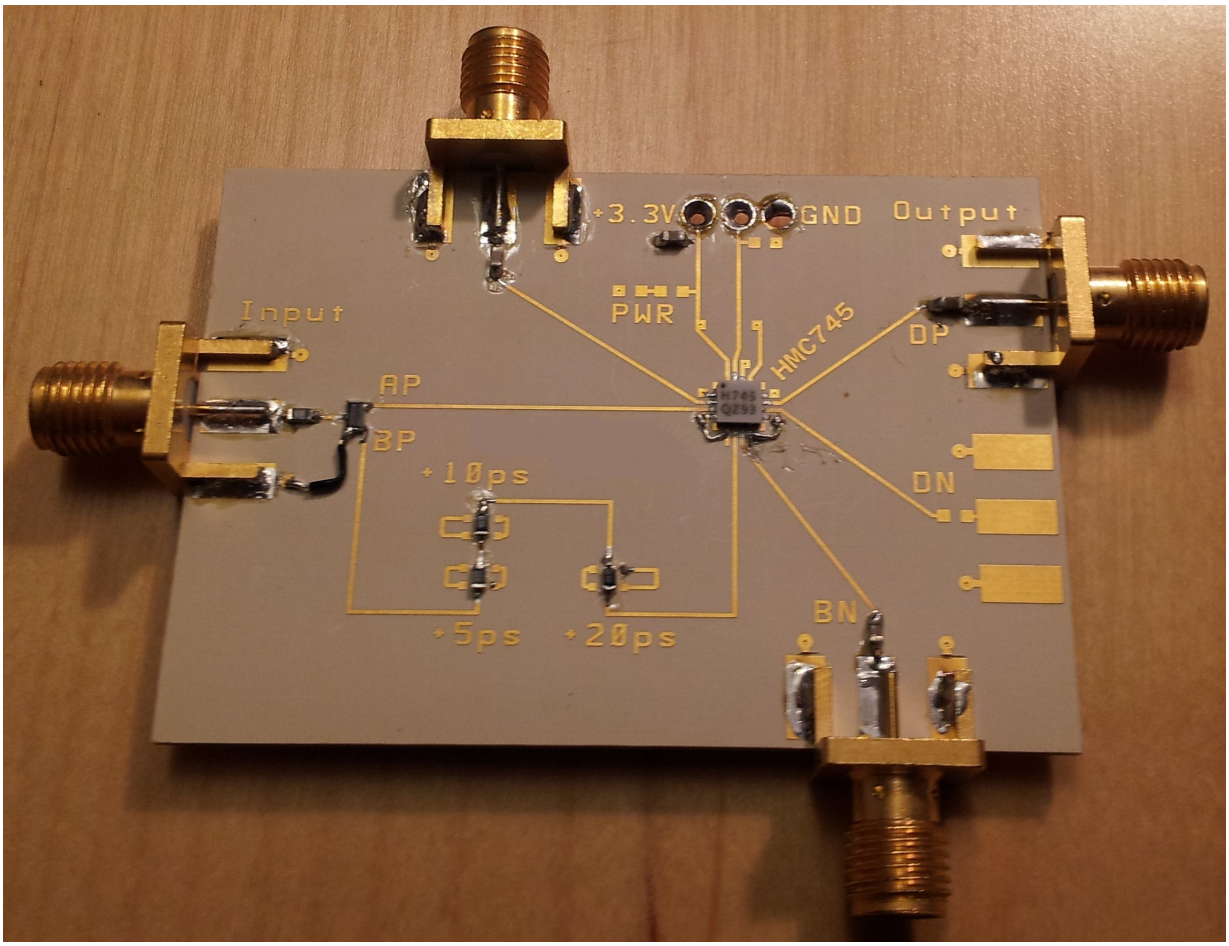
D.1. Modulator



D.2. Frequency synthesizer



D.3. First demodulator



D.4. Second demodulator