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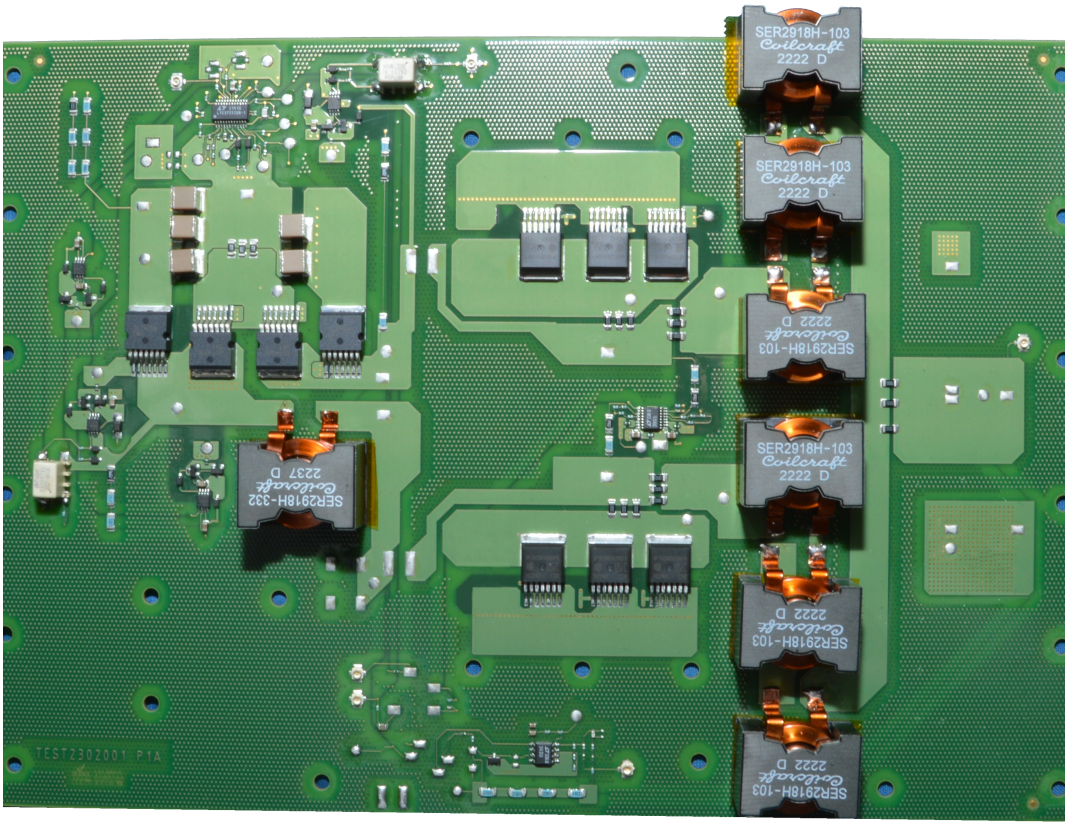

Design and Analysis of a Phase Shifted Full Bridge Converter for High Efficiency Operation

Master's Thesis in Electric Power Engineering

Johannes Karlsson & Simon Larsson

DEPARTMENT OF ELECTRICAL ENGINEERING

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Cover: Circuit board of the DC/DC full bridge converter designed in this project.

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Abstract

Saab investigates if there is a possibility to replace an existing DC/DC converter with an alternative converter design. Saab therefore wanted a phase shifted full bridge designed and constructed, capable of delivering 1.2 kW for an output voltage of 56 V, with a maximum output voltage ripple of 1%. The input voltage range is set to 350-400 V. The final design was then compared with an alternative solution, an LLC converter, in order to compare possible advantages with each solution.
The phase shifted full bridge converter was successfully designed and implemented in simulations. A list of components and a circuit schematic to realise the design in a physical implementation was then presented and the converter was constructed. Due to oscillations and a faulty snubber design, the phase shifted full bridge converter could not reach the aspirations and the maximum output power was limited to 400 W. The voltage ripple was not within the goal of 1% and the efficiency of the LLC was higher. However, the advantages of using a phase shifted full bridge compared to a LLC was also presented where a fully operational converter was considered.

Keywords: PSFB Converter, DC/DC converter, Current doubler, Transformer design, Feedback control, LLC converter.

Acknowledgements

We are grateful for the possibility we were given from Saab to do our Master's thesis at one of their departments of electrical power engineering. The opportunity to do the Master's thesis at Saab have granted us insight in the engineering work-life and how life at Saab is.
The team in which we've been employed have received us with open arms. Both the guidance and recommendations they've provided have been very insightful and their inclusion of us to the team has been outstanding. Some extra appreciation is in order towards our supervisors, Jacob Viktorsson and Daniel Samuel. Their guidance throughout the project has been very helpful and we are gratefully for all the time they spent guiding and discussing with us.
Further we want to offer our thanks to our examiner Torbjörn Thiringer for all the assistance he's given. Providing clear guidelines and helping us with the planning of a way forward when we at an early state of the project ran into certain holdups.
Simon Larsson & Johannes Karlsson, Gothenburg, June 2023

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

BJT	Bipolar junction transistor
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
MOSFET	Metal-oxide-semiconductor field-effect transistor
PCB	Printed circuit board
PSFB	Phase shifted full bridge
PSU	Power supply unit
PWM	Pulse width modulation
RMS	Root mean square
ZCS	Zero current switching
ZVS	Zero voltage switching

Contents

1

Introduction

In recent years there has been a large focus on developing sustainable, reliant power systems [1]. A driving factor has been the transition towards renewable electricity generation for the power grid. The transition towards renewable power production has led to a focus on developing high power, high efficiency power electronic devices for the electric grid [1]. On the other hand, the same development has also enabled power electronics to efficiently power different loads for different applications.

This advancement in technology has been a driving force for the project since some of Saabs technical solutions could benefit from an upgrade, considering the technological advancements. Saab has requested an evaluation of a new converter solution for an existing application. The objective is to investigate if a new design could offer higher efficiency compared to the existing solution while at the same time providing a more customised design. The present solution consists of purchasing modules from an external producer which is not ideal considering cost and the dependency on the manufacturer. By producing the converter themselves, Saab could decrease the cost while simultaneously decreasing the dependency of external manufacturers for their products.

1.1 Purpose

The purpose of this thesis is to investigate the possibility to replace the current power converter with a better converter. A phase shifted full bridge (PSFB) converter will be constructed and compared with an alternative solution consisting of an LLC converter. When comparing the converter designs the areas of interest are, but not limited to power capabilities and efficiency. The goal with the new design is a significant performance improvement compared to the already provided LLC converter, thus finding a reason for using a PSFB.

1.1.1 Technical aspirations

The prototype will be designed according to the following technical specifications set by Saab:

- Input voltage range from 350-400 V DC.

- Output voltage at 56 V DC.
- Maximum power of 1200 W.
- Maximum output voltage ripple limited to 1%.
- Peak efficiency above 95%.

1.2 Goals

Quantify potential advantages of using a phase shifted full bridge converter compared to the LLC converter. By studying and comparing the LLC converter module with a phase shifted full bridge converter, the aim is to determine if a new converter topology is overall advantageous and to which extent it might be more useful than the LLC solution. Thus, also determining shortcomings and limitations of using different converters. Aspects that need to be studied and quantified are power ratings and expected efficiency for different input voltages. Other important aspects to quantify includes voltage ripple, transient performance and number of modules needed.

Design a realistic simulation model of the phase shifted full bridge converter. By constructing the circuit in a simulation software, it will be possible to get an indication for how the converter will perform and get a baseline for the performance compared to the specifications in section 1.1.1.

Selection of Components. After studying the underlying functionality and determining the component requirements, all components will be selected accordingly with the goal to construct a functional PSFB.

Construction of a working prototype of the converter. Using the simulation model as a guide, a physical prototype can be constructed with the selected components. The prototype will be tested and verified by comparing results to the simulated behaviour. The prototype should be stable and be able to be used for performance tests.

Validate performance and compare to existing solutions. Ultimately a comparison between the developed prototype and already existing solution will determine if the PSFB converter has the potential to replace the existing technology. This would be verified by comparing the prototypes performance compared to the specifications in section 1.1.1.

1.3 Scope

In order to make this project possible, some limitations must be set.

The exclusion of electromagnetic interference (EMI) calculations and tests. EMI will be present since the circuit involves switching transistors. Since it

is a prototype board and there is time limitation for this project the circuit will not be designed to limit EMI.

External disturbances on the primary side of the converter will not be considered. A general approach of designing the primary side will be used where the specifications required are in focus. The off chance that the power to the converter is disturbed will not be considered due to time restraints.

Only the driver circuit LTC3722-1 will be used. Only the driver circuit LTC3722-1 will be investigated as a driver circuit for the converter since the report aims to investigate if a PSFB can be of interest. This driver circuit is specifically built for that application and will therefore be sufficient for the task at hand.

Only two converters will be tested. The two converters to be tested consist of one LLC converter and one PSFB that will be designed and constructed for this project. The converters operates at different power levels and will therefore be studied at their rated levels to achieve a realistic performance comparison.

There will only be tests conducted that are within the operation window of the converter during rated operation. A more comprehensive approach would include certain levels of power spikes outside of the rated power levels to ensure safe operations in case of some kind of disturbance. This will not be included in the report due to time limitations.

Total cost of the converters will not be studied. The economical aspect will be considered profitable if the new converter is performing better, since the new converter will be constructed internally instead of by an external producer.

Auxiliary power will be supplied externally. To decrease the number of components, complexity of the circuit and decrees the time needed to design the circuit, auxiliary power will be supplied from external power supplies.

PCB design will be excluded. Due to time limitations the Printed circuit board (PCB) design will be conducted externally and therefore is not included in this project. However, the final design will be discussed in order to evaluate the converter performance and discuss future improvements.

1.4 Societal, ethical and ecological aspects

There are severe ethical aspects associated to this project since Saab is a company mainly operating in the defence industry. This prototype could be a basis for future installations in Saab products, which might be used in future conflicts. However, it is also important to take into account that some countries might try to force other countries to comply to their agenda. A strong defence can be a tool for defending lives, liberties and independence.

Environmental aspects mainly consist of E-waste from the components used. E-waste which is electronic components at the end of a use cycle can be problematic

since improper recycling could cause unnecessary waste and expose workers to toxic materials [2]. However unnecessary waste and exposure to toxic materials can be reduced by recycling properly and according to local regulations.

2

Theory

2.1 Full bridge DC/DC converter

Full bridge converters are the standard for high power DC applications. Example applications for full bridge converters are chargers for electrical vehicles and to drive electrical motors [3]. The converter utilises four switches, T1 to T4 in Figure 2.1, on the primary side which allows both a positive and a negative voltage polarity across the transformer.

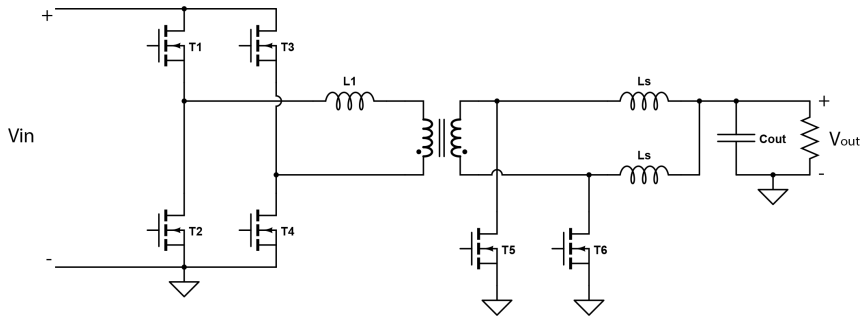

Figure 2.1: A general DC/DC converter topology using a full bridge and current doubler design

The switching pattern on the primary side of a conventional full bridge consists of three switching stages, where the switches are operated in pairs. In Figure 2.1 transistor T1 and T4 forms one pair whilst T2 and T3 form the other pair. The pairs will be turned on during a time period which depends on the converter switching frequency. When the pair is turned off, the other transistor pair will not immediately be turned on. The time period where no pair of transistors are conducting is called dead time and is there to avoid short circuiting the input source. After the dead time the other switch pair is turned on. The voltage over the transformer wingdings thus equals the source voltage but will flip polarity depending on which switching pair that is conducting. The result is a square wave with an amplitude of $2V_{in}$ peak to peak over the transformer.

By using a transformer, the voltage on the secondary side can effectively be converted to a desired secondary voltage level with the advantage of having galvanic isolation from the primary side. However, the voltage on the secondary side of the transformer

will have a similar waveform pattern as the primary side of the transformer. This consists of positive and negative square-waves with varying duty cycle. Therefore, there is an additional requirement to include a rectification process on the secondary side of the transformer to enable it for DC applications. Rectification on the secondary side can be done by utilising either diodes or metal-oxide-semiconductor field-effect transistors (MOSFETs).

2.2 Transistor design and selection

When designing high power converters there are mainly two different transistor types of interest, IGBT and MOSFET transistors. The two types differ in practical applications where the IGBT has a lower conduction loss but high switching losses. This causes the IGBT to be preferable in high current, low frequency operations, mainly below 20 kHz [4]. The MOSFET has a low gate capacitance compared to the IGBT, allowing for fast switching at low gate energies. Therefore, the switches in this converter will consist of MOSFETs since the converter is designed for high frequencies. A MOSFET can be controlled by applying a voltage over the MOSFETs gate and source pins. The MOSFET will then form a conducting channel between its drain and source pin. The voltage applied across its drain and source will limit how much current that can pass through the drain source channel. In general terms, a MOSFET can be seen as a voltage-controlled switch.

2.2.1 Parasitic elements

MOSFETs are not ideal components, the switching time is not infinitely small and there are parasitic capacitors that needs to be charged and discharged to enable operation of a MOSFET [5]. The input capacitance correlates to how much energy that is required to turn on/off the transistor. A low parasitic input capacitance needs less energy to switch and can be operated faster for the same gate driver and same gate source voltage [6].

A MOSFET also contain a parasitic output capacitance in addition to the parasitic input capacitance. The parasitic output capacitance can cause the circuit to alter its behaviour by interfering with other components. The capacitance can, for example, in combination with an inductor cause high frequency ringing which could damage other components in the circuit and the MOSFET itself [5]. The output capacitance influences the behaviour of the MOSFETs, current can flow through the capacitance even though the MOSFET is off. The parasitic output capacitance also influences the time to turn off the transistor. A PSFB in comparison to a conventional full bridge is designed to discharge the output capacitance before switching in order to improve efficiency and utilise soft switching, which will be discussed in Section 2.3.

2.2.2 MOSFET losses

A MOSFET is not an ideal switch or conductor, hence the non-ideal MOSFET will cause power losses when it is operating. Power dissipates as heat and the converter

will therefore heat up. Limiting losses will limit how much the temperature will rise which in turn sets the requirements on converter cooling. Managing losses and cooling will increase the life span of the selected components.

When a MOSFET is either turned on or off, there will be a short time interval where the transistor has a voltage across the drain source terminals and conducts current, as seen in Figure 2.2.

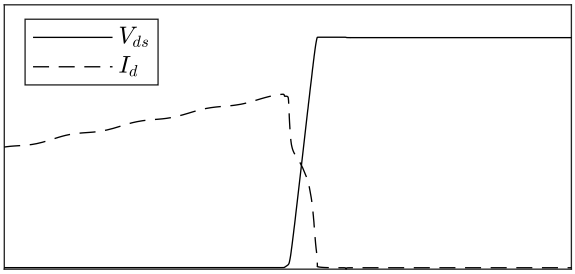

Figure 2.2: Typical turn off waveform for a MOSFET.

The overlap between current and voltage during switching is the switching loss. Switching losses are a significant portion of the overall losses for a MOSFET. To improve efficiency, soft switching could be implemented as in the case of a PSFB, which implements ZVS (Zero voltage switching). ZVS means there is no voltage across the transistor as it switches thus reducing losses and reducing the heat dispersed due to switching.

Switching losses are calculated according to

$$P_{sw} = f_{sw} \int v_{ds}(t) i_d(t)\, dt \tag{2.1}$$

where V_{ds} is the drain to source voltage over the transistor, I_d is the drain current through the transistor and f_{sw} is the switching frequency of the converter [7]. The total amount of energy dispersed during a switch event can be calculated from (2.1) by neglecting to multiply with the switching frequency. Both turn on and turn off losses can be calculated in the same manner. Conduction losses in a MOSFET can be determined according to

$$P_{cond} = R_{on} I_d^2 \tag{2.2}$$

where R_{on} is the on-resistance for a MOSFET and I_d is the root mean square (RMS) value for the current through drain to source. According to (2.2), conduction losses for a converter can be reduced by either using MOSFETs with lower on-resistance or by reducing the current through the MOSFET. Decreasing the current is a more effective approach to decrease the conduction losses since the conduction losses are proportional to the square of the current. By decreasing the current, the voltage must be increased to maintain the same power level, due to the relation between voltage and current according to

$$P = UI \tag{2.3}$$

this relation offers the possibility to increase the voltage and therefore allow the current across the primary MOSFETs to be decreased leading to a decreased conduction losses. However, on the secondary side of the converter the voltage is kept constant and thus there is no possibility to decrease the current for a given load. There is however a possibility to use multiple MOSFETs in parallel in order to decrease the on resistance and thus also decrease conduction losses.

2.3 Phase shifted full bridge operation

A PSFB builds upon the conventional full bridge whilst improving the efficiency by utilising soft switching. Soft Switching refers to the fact that the transistor will experience less stress and losses during a switching event since it switches when the voltage is close to zero [8]. In order to achieve ZVS a PSFB utilises a more complex switching pattern compared to a conventional full bridge [8]. The switching pattern for a PSFB converter is explained below.

Figure 2.3 displays the current flow through the primary side when transistor A and D are conducting. When transistor A and D are conducting, the operation is identical as for a conventional full bridge. When MOSFET A and D are turned on, it possible to transfer energy from the source to the transformer windings [8]. Transistor A and D will conduct for a finite amount of time which is determined by the duty cycle and switching frequency.

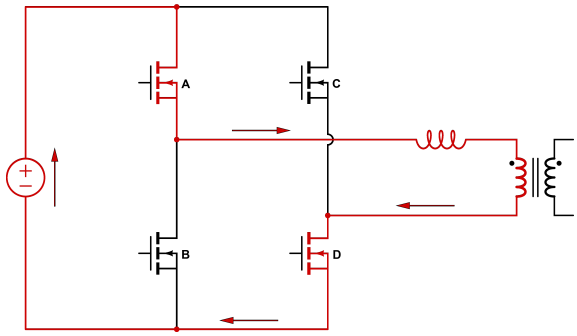

Figure 2.3: The first step of the ZVS switching sequence.

When the first step of the switching sequence is over, only transistor D is turned off unlike the conventional full bridge where both A and D are turned off at this stage. Only turning off transistor D means that the voltage over transistor D starts to increase and will in effect charge the equivalent parasitic output capacitance of the transistor [9]. At the same time the voltage over transistor C will be zero since the potential will be the same on both sides of the transistor and the parasitic capacitance will therefore discharge the output capacitance of the transistor [10]. Current will flow through transistor A and the parasitic capacitance in transistor C and D as displayed in Figure 2.4.

When the output capacitance of transistor C is discharged, the body diode of the transistor will conduct throughout the MOSFET [10]. Minimising this time period

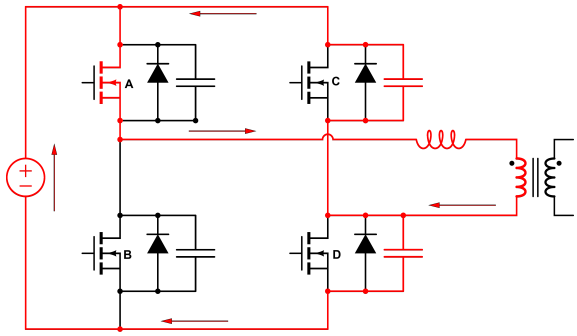

Figure 2.4: The Second step of the ZVS switching sequence.

will limit power losses since conducting through the body diode causes power losses. The sequence when the body diode of transistor C is conducting is displayed in Figure 2.5. During the next step MOSFET C will be turned on and thus both MOSFET A and C will be turned on and effectively short the transformer winding. The current flowing thorough MOSFET C will not go through the body diode when MOSFET C is turned-on [10]. Since the output is shorted, there will be no power flow from the source to the transformer, but Current will instead flow in a circle according to Figure 2.6.

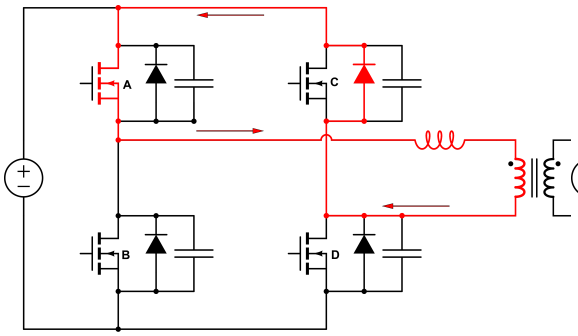

Figure 2.5: The third step of the ZVS sequence.

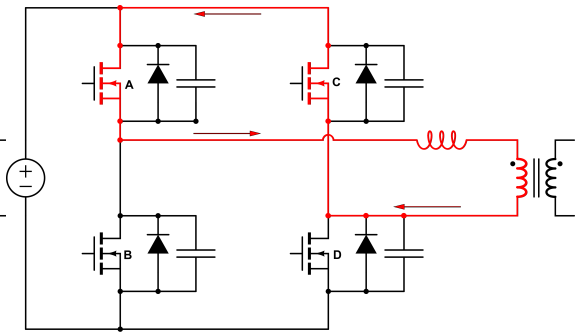

Figure 2.6: The fourth step of the ZVS sequence.

MOSFET A will be turned off in the next step in preparation for activating MOSFET B. When MOSFET A is turned off, the capacitor for MOSFET A will be charged whilst MOSFET B will be discharged [9]. The current will flow through MOSFET C and the parasitic capacitors for MOSFET A and B which can be seen in Figure 2.7.

When the parasitic capacitance of MOSFET B is discharged, MOSFET B should immediately be turned on to achieve a soft switch [10]. If the MOSFET is not immediately turned on the body diode will conduct, and current will flow from the negative to positive input, which can be observed in Figure 2.8. Ideally this time instance should be as short as possible to avoid losses. When MOSFET B is turned on, the current direction will flip, causing the current direction to flow from the positive to the negative terminal, see figure 2.9 [10].

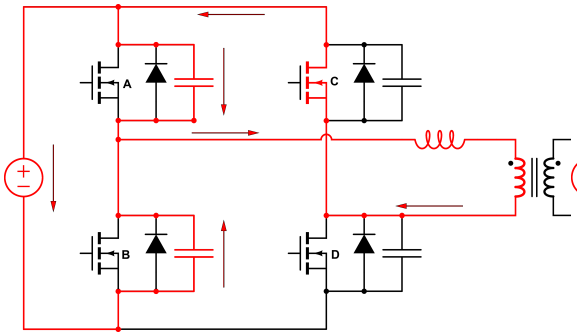

Figure 2.7: The fifth step of the ZVS sequence.

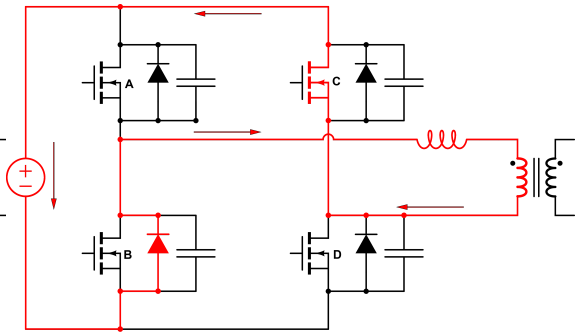

Figure 2.8: The sixth step of the ZVS sequence.

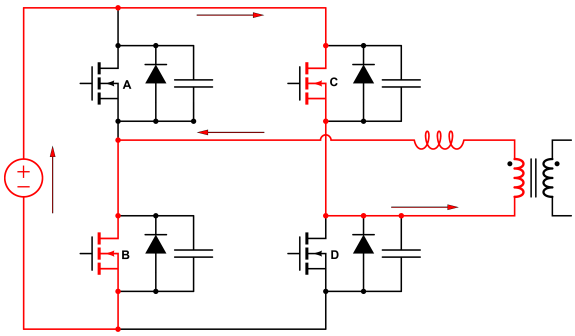

Figure 2.9: The seventh step of the ZVS switching sequence.

At the point where transistor B and C are turned on, the converter has completed the transition from MOSFET A and D conducting to MOSFET B and C conducting. The converter will now repeat the same process but mirrored in order to activate MOSFET A and D again. The converter will cycle through all the above mentioned ZVS steps in order to decrease and limit turn on losses. Turn off losses will still occur for the converter between the first and second step of the ZVS switching sequence.

2.3.1 Zero-voltage switching conditions

The condition required in order to enable ZVS for a converter is given by

$$\frac{4}{3}C_{oss}V^2 < \frac{1}{2}L_{lk}i^2 \tag{2.4}$$

where C_{oss} is the parasitic capacitance of the primary MOSFETs, V is the voltage applied over the capacitance and L_{lk} is the leakage inductance from the transformer which is discussed in Section 2.6.3 [9]. The expressing comes from that the inductive energy in the PSFB needs to be larger than the capacitive energy.

Furthermore, the time required (freewheeling time) to obtain ZVS can be approximated using one fourth of the resonant frequency of the MOSFET and leakage inductance, see figure 2.10 [11].

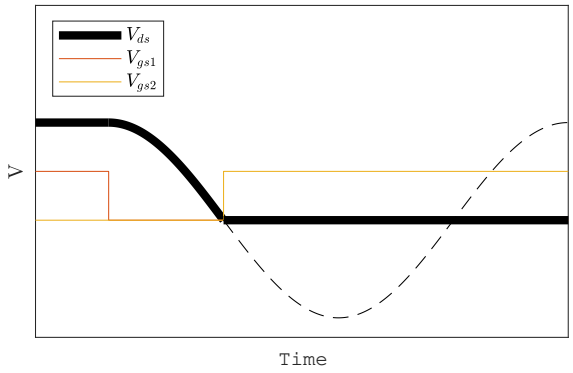

Figure 2.10: Visualisation of the resonant frequency

The figure presents how the voltage over drain to source decreases with a sinusoidal pattern when the gate signal switches to 0 V. The potential V_{ds} reaches 0 V at T/4 for the sinus waveform marked as a dashed line in the figure. The resonant frequency can be obtained using

$$f_r = \frac{1}{2\pi\sqrt{L_{lk} \cdot 2C_{oss}}} \tag{2.5}$$

The time required to enable ZVS can be obtained using

$$T_D \geq \frac{\pi}{2}\sqrt{L_{lk} \cdot 2C_{oss}} \tag{2.6}$$

2.4 Secondary side circuit design

To rectify the voltage and current from the full bridge, either a center-tapped or current doubler configuration can be used, the different circuits are presented in Figure 2.11 [12].

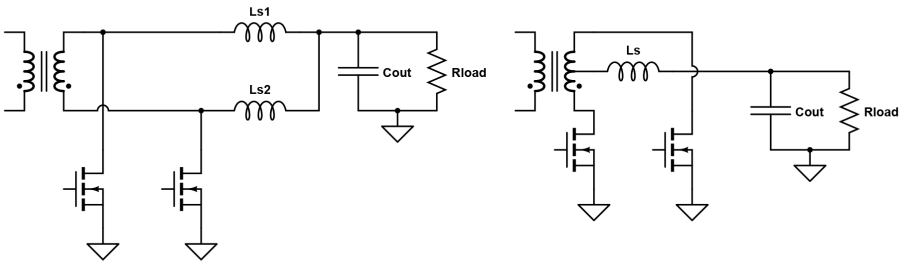

Figure 2.11: Left: Current doubler. Right: Center tapped

The two approaches are more suitable for different applications, since the working principle is different. The current doubler offers easier transformer implementation on the secondary side with less copper losses, but instead requires two inductors. The current to the output can however be divided between the two inductors, resulting in

half the RMS current in each inductor compared to using a center-tapped circuitry, see Figure 2.12.

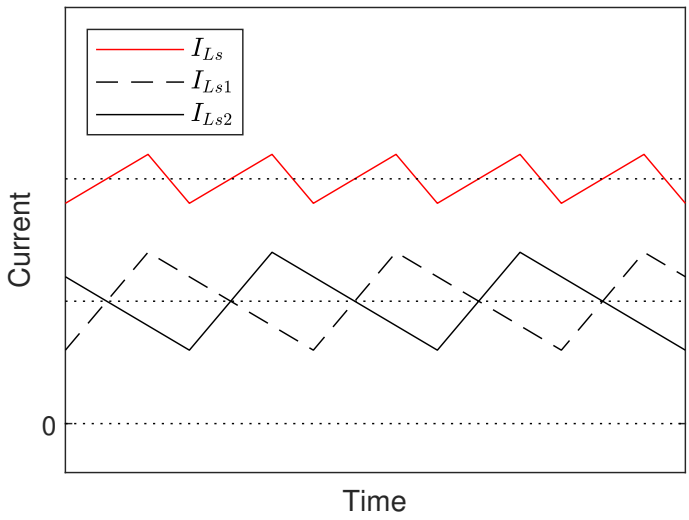

Figure 2.12: Waveform patterns for an equivalent center-tapped configuration compared to a current doubler.

The trade-off for half the RMS compared to the center-tapped circuitry is that the current ripple at each inductor approximately doubles due to the halved frequency over each inductor. However, due to the possibility to divide the RMS current and the simpler design of the transformer with less copper losses, the current doubler will be further investigated in the project.

2.4.1 Current doubler operation

The Current doubler operates using two inductors and two switches, for example MOSFETs. Depending on the polarity over the transformer, the current flows in different patterns. How the current flows is presented in Figure 2.13 [12].

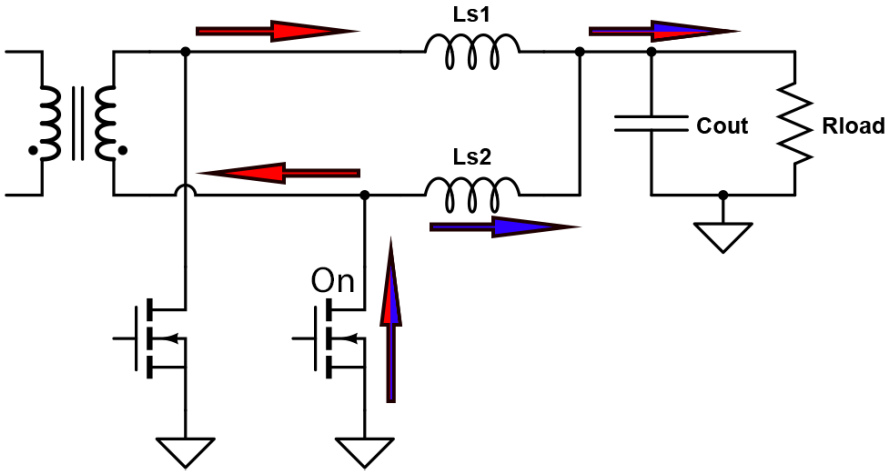

Figure 2.13: Current flow patterns of a current doubler circuit.

In the figure one of the rectifier MOSFETs are conducting where the red arrows symbolise the power transfer current through the transformer which is the current charging inductor Ls1. The blue arrow marks the current path through Ls2 which is the decreasing current due to discharge of Ls2. The time interval where the currents flow as in Figure 2.13 equals the time period when I_{Ls1} increases and I_{Ls2} decreases simultaneously in Figure 2.12. When the polarity over the transformer switches the other MOSFET starts conducting in the same pattern as the other MOSFET did, where Ls2 instead is charged and Ls1 discharged. This time interval instead equals the time period when I_{Ls2} increases and I_{Ls1} decreases simultaneously in Figure 2.12. A final state occurs when the voltage over the transformer is zero, resulting in no power transfer over to the current doubler secondary side. In this case both inductors are discharged through the MOSFETs according to Figure 2.14 and the time period equals the time where both I_{Ls2} and I_{Ls1} decreases simultaneously in Figure 2.12.

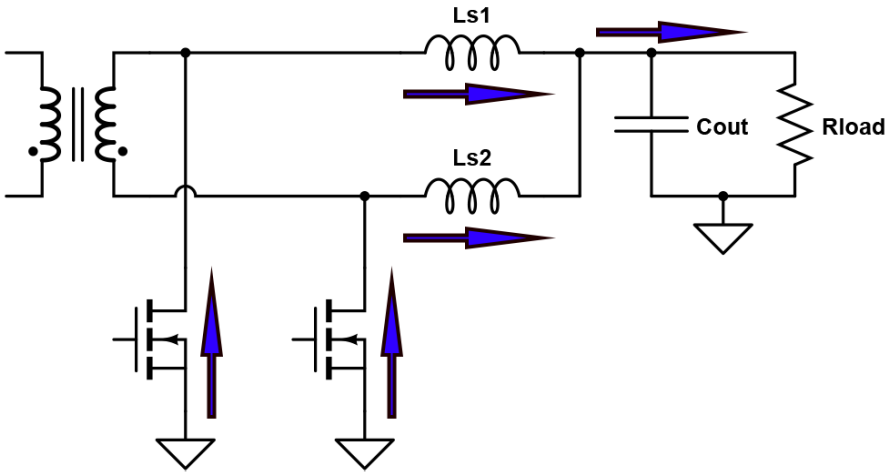

Figure 2.14: Current flow patterns of a current doubler circuit.

The current doubler can be operated in CCM (continuous conduction mode), where the current marked with blue arrows never stops before the polarity over the transformer changes and therefore starts to instead charge the inductor Ls2 through the other MOSFET [13]. The current doubler can also operate in DCM (discontinuous conduction mode). This means that the inductor Ls2 runs out of energy before the polarity over the transformer switches and therefore eventually stops the flow of current through Ls2.

2.4.2 Snubber design

The secondary side uses hard-switching MOSFETs, there is a possibility of LC resonances created during turn-off that could damage or destroy components. There are several options available for implementation in order to decrease the voltage spikes, all at various levels of power loss and complexity. One common approach is using a RC snubber in parallel with the MOSFET that causes the ringing [14]. This

approach can significantly reduce oscillations, at the cost of increased power losses over the snubber.

Another approach is the RCD snubber. The RCD snubber requires an additional component but reduces power losses in the snubber. Due to the diode, the RCD snubber can only protect against spikes of one polarity, leading to the requirement of two RCD snubbers in a full bridge configuration since the potential at the transformer switches polarity. Both a general approach of an RC and RCD snubber can be observed in Figure 2.15 where the grey area "A1" and "A2" are the RCD snubbers and the grey areas marked with "B" are the RC snubbers. Noteworthy is that "A1" is connected to the input voltage of the converter in order to protect against positive voltage transients above V_{in}, whilst "A2" is connected to ground, protecting against negative voltage spikes.

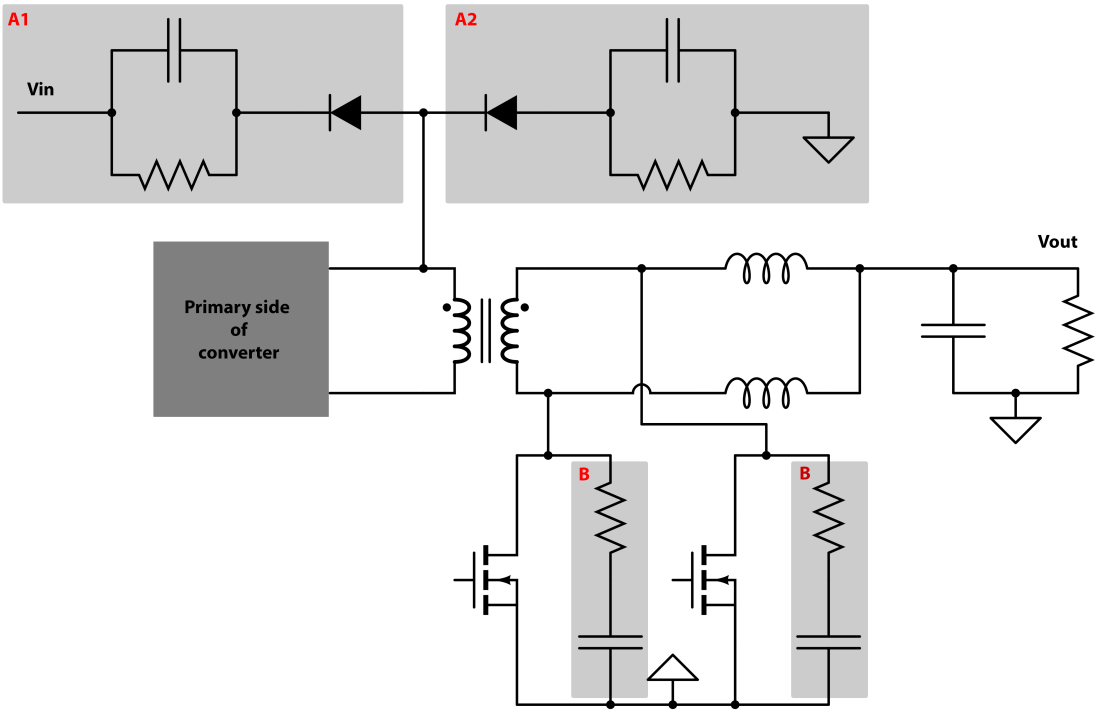

Figure 2.15: RCD and RC snubbers in a full bridge design

2.5 Gate drivers for MOSFETs

The MOSFET in both the primary and secondary side require additional circuitry in order to function together with the converter.

2.5.1 Primary side

The driver circuit LTC3722-1 shares the same ground as the input voltage on the primary side of the converter, therefore an output signal from the driver circuit on

pins OutA to OutC (see Appendix B.1) is required surpass the voltage level of the source reference of MOSFETs A and C in order to trigger their conduction [15].

For the upper primary MOSFETs (A and C) in the PSFB the source voltage is floating and will change from 0 to 400 V depending on which lower transistor that is conducting. In order to power the gate of the transistors the gate voltage thus need to be able to fluctuate with source voltage and even surpass the source voltage [15]. However, the circuit driver can only supply an output voltage of approximately 10 V which is not sufficient to power the upper MOSFETS A and C. In order to power the said MOSFETs, a bootstrapping circuitry can be used [16]. This type of solution consists of a resistor, a diode and a capacitor combined with a gate driver. The general approach can be observed in Figure 2.16

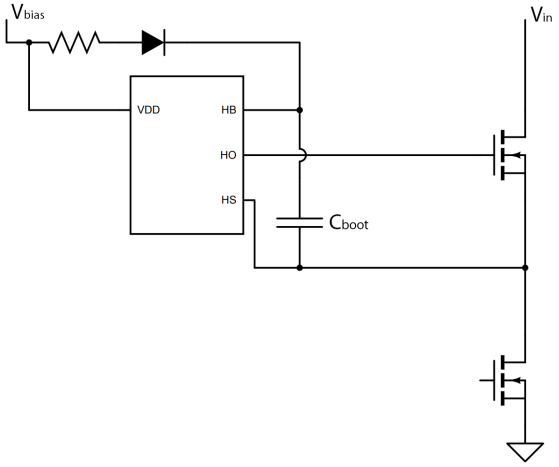

Figure 2.16: Bootstrap design using a general gate driver

The concept consists of using the capacitor C_{boot} as an energy storage, where it is charged from V_{bias} when the pin HS is connected to ground through the conducting lower MOSFET. This stored energy is then used as an extra voltage boost when the upper MOSFET is conducting, pushing the input pin HB to $V_S + V_{bias}$. This setup ensures a voltage across gate and source to be equal to V_{bias} during on-time, assuming no voltage drop in C_{boot} when discharging. The size of C_{boot} that ensures enough energy storage to accomplish bootstrapping can be found using the correlation $C_{boot} > 10 \cdot C_g$.

2.5.2 Secondary side

Since the MOSFETs are directly connected to the negative leg of the output voltage, there are risks of a surge of negative current through the MOSFETs. This is commonly handled using circuitry that senses the current direction through the MOSFET and forces shutoff if it changes direction. One component of interest is the LTC3901 which can be used to accomplish this [17]. In order for this gate driver circuit to operate correctly and use the negative current protection, some external resistors are required, see Figure 2.17.

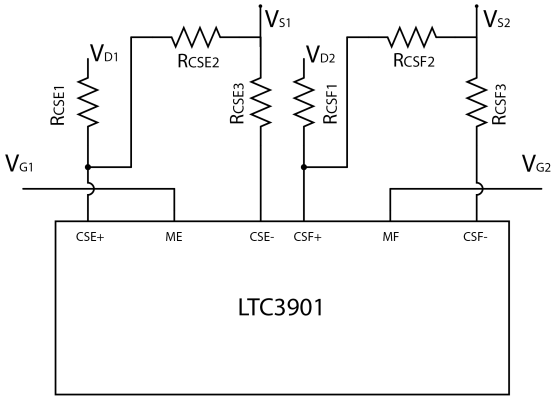

Figure 2.17: Model of LTC3901 showing placement of resistors

Where V_{G1} and V_{G2} is the gate signal for the two MOSFETs on the secondary side. V_{D1} and V_{D2} connects to the drain of the two MOSFETs. Thus V_{S1} and V_{S2} connects to the source leg of the transistors. The resistors R_{CSX1}, R_{CSX2} and R_{CSX3} can be calculated using

$$k = (48\Delta I \cdot R_{DS.on}) - 1 \tag{2.7}$$

$$R_{CSX2} = \frac{200V_{in.MAX} \cdot \frac{N_s}{N_p} - 2200(1+k)}{k} \tag{2.8}$$

$$R_{CSX1} = k \cdot R_{CSX2} \tag{2.9}$$

$$R_{CSX3} = \frac{R_{CSX1}R_{CSX2}}{R_{CSX1} + R_{CSX2}} \tag{2.10}$$

ΔI is the peak-peak current ripple in the output inductors, $R_{DS.on}$ is the conduction resistance of the MOSFET controlled, N_s and N_p is the secondary and primary windings of the transformer.

LTC3901 can directly power the MOSFETS from the gate signal without a boot-strapping circuit since the soruce pin of the MOSFETs are referenced to ground in a current doubler circuit. LTC3722-1 provides the main control of the gate signal used for MOSFET E and F but LTC3901 powers the amplifies the gate signal with the added current protection as mentioned above. LTC3722-1 however is placed on the primary side of the converter and therefore does not share the same ground as the secondary side due to the galvanic isolation. Therefore, a middle step like a transformer can be added to the two circuits can communicate properly.

2.6 Transformer design

The use of a transformer allows for power transmission whilst isolating the input from the output. By using a transformer, the converter voltage and current can be scaled to the required levels by changing the turn ratio [18]. The turn ratio is the ratio between the number of turns on the primary side and the number of turns on

the secondary side. For a secondary side current doubler rectifier, the turn ratio N is determined according to

$$N = \frac{V_{in(min)} D_{max}}{2V_{out}} \tag{2.11}$$

where $V_{in(min)}$ is the lowest possible input voltage, D_{max} is the highest possible duty cycle, V_{out} is the desired output voltage [12]. A lower turn ratio will give a higher secondary voltage for a given input voltage. Which in turn lowers the maximum duty cycle needed [18].

2.6.1 Magnetic design aspects

When designing a transformer it is important that the magnetic core does not saturate. When a magnetic material saturates it means that the magnetic permeability of the material changes which disrupts the linear relationship between the magnetic field and the flux density, as seen in

$$B = \mu H \tag{2.12}$$

where B is the magnetic flux density, μ is the magnetic permeability of the core material and H is the magnetic field strength. The magnetic flux density has also reached a maximum value when a core saturates. A saturated core can damage components in the circuitry since the primary side current increases when the core saturates [19]. To avoid saturation, the primary wingdings need to be designed in such a way that the peak magnetic flux density is always lower than the saturation flux density level for the material. Limiting the magnetic flux density will also limit core losses. The flux swing of the transformer is determined according to

$$\Delta B = \frac{VDT}{N_p A_e} \tag{2.13}$$

where V is the applied voltage over the primary transformer windings, D is the maximum allowed duty cycle and T is the switching period as seen from the transformer, where the transformer will experience half the switching frequency compared to the oscillator of LTC3722-1 [15]. N_p is the number of primary turns on the transformer and A_e is the effective area for the transformer. The numerator of (2.13) can be seen as the volt-second product for the transformer which is equivalent to the magnetic flux through the transformer core [20]. Since the voltage over the transformer will be both positive and negative for an equal time interval during a switching cycle, the average magnetic flux will be zero over the core, whilst the magnetic flux density will swing in accordance with (2.13). The peak magnetic flux density will therefore be half of the magnetic flux density swing. Therefore, if the peak magnetic flux density is lower than the given saturation limit for the core material, the core will not saturate [18].

Small voltage deviations for different pulses can cause an equivalent DC offset for the voltage. These deviations can be caused by differences in the MOSFET manufacturing [21]. The small offset will cause the flux density to slowly increase towards

saturation. The imbalances can be solved by applying current control mode to the circuit [21]. Current limitation is an essential feature to avoid transformer saturation. When a core is close to saturation, the primary current will rise quickly, which will be sensed by the controller. If the set current limit is exceeded, the switching cycle will be terminated and thus avoids damaging the converter [19],[21].

2.6.2 Material selection and losses

The material selected for the core depends on the use case, where ferrite is typically used for switching converters [6]. Ferrite is suitable at high frequency operation due to low hysteresis and low Eddy current losses, compared to other magnetic materials. A drawback with ferrite is that it saturates for lower magnetic flux density compared to other magnetic materials and can thus not be magnetized as much as other materials. The hysteresis can be seen from the materials B-H curve, where the B-H curve follows the relation in (2.12). For a ferrite core, hysteresis is the dominating core loss, other losses such as Eddy current losses are negligible due to high electrical resistivity of the material [6]. The hysteresis loss for a core is dependent on the overall volume of the core, flux density, temperature and frequency [6]. The hysteresis loss can be determined from studying data sheets from the core manufacture which often gives the specific power loss as a function of frequency and magnetic flux density [22].

Except for the magnetic losses, copper losses from the winding's are prevalent and will determine the overall effectiveness of the transformer together with the magnetic losses. The copper losses originate from the ohmic losses of the long copper windings, which can be determined using

$$P_{cu} = i^2 R \tag{2.14}$$

where i is the RMS value of the current through the windings and R is the resistance of the wire. The resistance can be determined when the length, area and conductivity of the material is known, according to

$$R = \rho \frac{l}{A} \tag{2.15}$$

The length of the wire depends on both primary and secondary side number of turns and the turn ratio between them. The circumference around the core also determines the overall length of the windings. Losses where the current is high yields higher losses according to (2.15). By decreasing the number of turns the ohmic losses will decrease, but from (2.13) it can be seen that increased number of turns will allow for a lower flux density swing and therefore lower magnetic losses, resulting in an optimisation problem. To minimise overall losses, the resistivity of the windings can be decreased to further increase efficiency. However, decreasing the resistance is not as trivial as increasing the conducting area, since the available space for the wingdings is limited.

Skin effect, an effect occurring when using high frequency current, will limit the conduction area and therefore the resistance of a conductor since current will only flow close to the surface of the conductor [6]. The depth at which the current penetrates due to skin effect can be determined as

$$\delta = \sqrt{\frac{2}{2\pi f \mu_0 \mu_r \sigma}} \tag{2.16}$$

where δ is how deep into the conductor current will penetrate in the material, μ_0 and μ_r is the magnetic permeability for air and the relative magnetic material respectively. σ is the conductivity of the material [6]. The overall effective conducting area determines the resistance and the losses. One approach to have a large conducting area is by using litz wires, which are small conducting wires bundled together but isolated from each other, resulting in a reduction of the skin effect [18].

2.6.3 Leakage and magnetic inductance

A real model of a transformer includes several parasitic parameters, such a model is displayed in Figure 2.18 [6]. Resistances R_1 and R_2 are the respective winding resistances from the primary and secondary windings. L_{lk1} and L_{lk2} is the leakage inductance for the primary and secondary side of the transformer. Leakage inductance arises from a transformer when magnetic flux from the primary coil leak and does not reach or link with the secondary side coil [6]. Normally, leakage inductance should be minimised to avoid overvoltage and LC resonances, however for a PSFB, leakage inductance is used to discharge the parasitic capacitance's of the MOSFETs in order to achieve ZVS. L_m is the magnetizing inductance through the core, and the current through L_m is the magnetizing current which is used to magnitize and maintain flux inside the core [23]. R_m is a symbolic resistance that represents the hysteresis losses through the transformer.

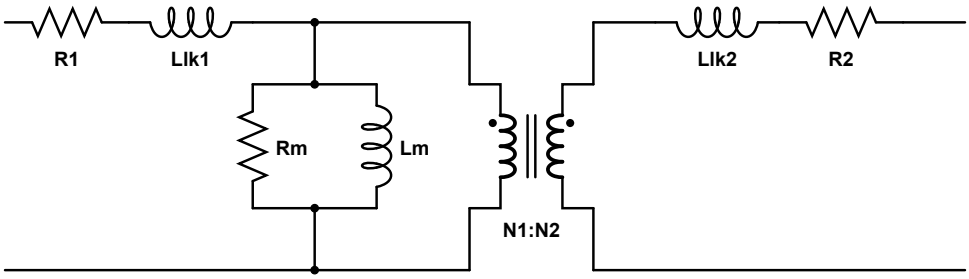

Figure 2.18: A circuit of a non-ideal transformer

L_{lk1} and L_m can be determined by performing open-circuit and short-circuit tests on the transformer [24]. Conducting an open-circuit test means measuring the inductance on the primary winding when the secondary winding is an open line. This test provides the sum of L_{lk1} and L_m. A short circuit test is conducted by short-circuit either side and measuring the inductance on the other side, resulting in a measurement of L_{lk1} or L_{lk2}. Thus, by subtracting the result from the short circuit

test to the open circuit test, the magnetizing inductance can be determined [24]. Ideally the magnetizing current should be as small as possible, in an ideal case there is no magnetizing current due to a perfect core material that does not need energy to stay magnetized, in the ideal case the permeability of the core is infinite and the magnetizing inductance is also infinitely large.

2.6.4 Transformer windings

The physical dimensions of a transformer also needs to be considered in the design process to be able to have enough physical space to fit the windings. Transformer cores comes in different sizes and shapes in order to fit different use cases. The core type and size needs the be selected in accordance to limit the aforementioned winding and core losses. The windings should fit around the transformer and through the window area of transformer. The window area is a cross-sectional area where the windings are supposed to wound. The window area should be larger than the total amount of conducting area for both the primary and secondary windings and also have enough space for electrical isolation between the primary and secondary windings. The window area for a typical E-core is displayed in Figure 2.19.

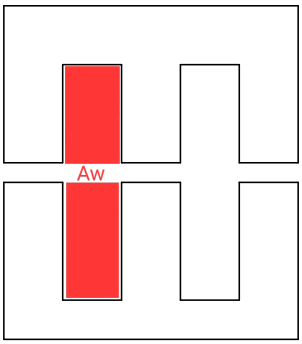

Figure 2.19: Window area of a E-core transformer.

2.7 Output capacitor and inductor

In order to filter and reduce the ripple to a DC signal on the output current and voltage, output capacitors and inductors are required. The output current ripple should be small in comparison to the DC value of the output current, since the magnitude of the ripple decides the stress over the capacitor [25].

One approach to decide the limit of allowed current ripple is to use an inductor large enough to avoid operating in DCM at the rated power levels of the converter, since the gate driver LTC3901 is mainly designed for CCM [17][11]. Using the lower limit of power output with the output voltage gives the lowest DC current output

according to

$$I_{out.min} = \frac{P_{out.min}}{V_{out}} \tag{2.17}$$

where the current is evenly shared over the 2 inductors L_{s1} and L_{s2} in Figure 2.11. Due to the shared current between the inductors, the maximum ripple allowed to ensure no negative currents equals the magnitude of the output current. Using this limit the size of the inductors required can be determined according to

$$L_S = \frac{1}{\Delta I_{LS.pp}} V_{out}(1 - ph)T \tag{2.18}$$

where $\Delta I_{LS.pp}$ equals the inductor current ripple and T is the period time for the transistors. The parameter ph is the effective phase shift and can be calculated using

$$ph = \frac{V_{out} N_p}{V_{in} N_s} \tag{2.19}$$

where N_p and N_s are the primary and secondary windings of the transformer.

When designing the output capacitor, the internal ESR (equivalent series resistance, notation R_c) is of importance, where the amount of ESR will determine the losses over the capacitor according to

$$P_{C_{out}} = I^2_{C_{out.rms}} R_c \tag{2.20}$$

This loss will decrease the efficiency of the circuit but also risk overheating the capacitor, which must be taken into consideration when selecting capacitors.

The amount of ESR of the output capacitor will also determine the voltage ripple of the output during steady state, with the relation

$$R_c = \frac{\Delta V_{out}}{\Delta I_{C_{out}}} \tag{2.21}$$

where ΔV_{out} is the allowed voltage ripple over the load [26]. The current $\Delta I_{C_{out}}$ is the peak to peak ripple current for the bulk capacitor, which can be calculated using

$$\Delta I_{C_{out}} = \frac{V_{out}}{L_S} T(1 - 2ph) \tag{2.22}$$

Thereafter the output capacitor can be determined with the calculated requirement of maximum ESR allowed.

2.8 Converter waveforms

With the presented components from previous sections, the correlation between different components and their corresponding waveform can be studied. The waveforms of the PSFB are presented in Figure 2.20. The waveforms are simplified in order to provide a clear picture of its operational pattern of the PSFB. Signals V_{G-A} to V_{G-D}

is the gate signal for the four MOSFETs in the full bridge. Signals V_{G-A} and V_{G-B} are part of the passive leg of the converter [15]. V_{G-C} and V_{G-D} are part of the active leg of the PSFB. Active leg means that the signals are actively controlled to allow for a certain overlap to MOSFET A and B of the passive leg. This means that MOSFET D is modulated to overlap MOSFET A for a certain time, and the same for MOSFET C which is modulated to overlap MOSFET B. The overlap involves the switching pattern of the PSFB as presented in Section 2.3. The overlap is seen as a phase shift and hence the name of the converter topology.

The transformer voltage correlates to the switches that are turned on and off [27]. By altering the phase shifting the pulse width of the transformer voltage can be increased or decreased. The same is true for the primary side transformer current where the pulses will form more of a triangle shaped pulse with increased load. Note that the transformer voltage is bipolar, meaning that the upper value of the voltage in 2.20 corresponds to the positive input voltage whilst the lower edge corresponds to negative input voltage over the transformer. The same is true for the current through the transformer.

The secondary side MOSFETs can be powered on simultaneously if there is no voltage over the transformer [15]. When both are conducting the transformer secondary side is shorted, but since no energy is transferred from the primary side due to the voltage over the primary winding is zero. When there is voltage over the transformer only one transistor can be turned on.

The current over the inductors are also linked to when there is voltage over the transformer and the secondary MOSFETs are conducting [11]. A positive current slope for inductor L_{S2} occur when MOSFET F is conducting and the transformer voltage is positive. And for inductor L_{S1} a positive current slope occurs when MOSFET E is turned on and the transformer voltage is negative.

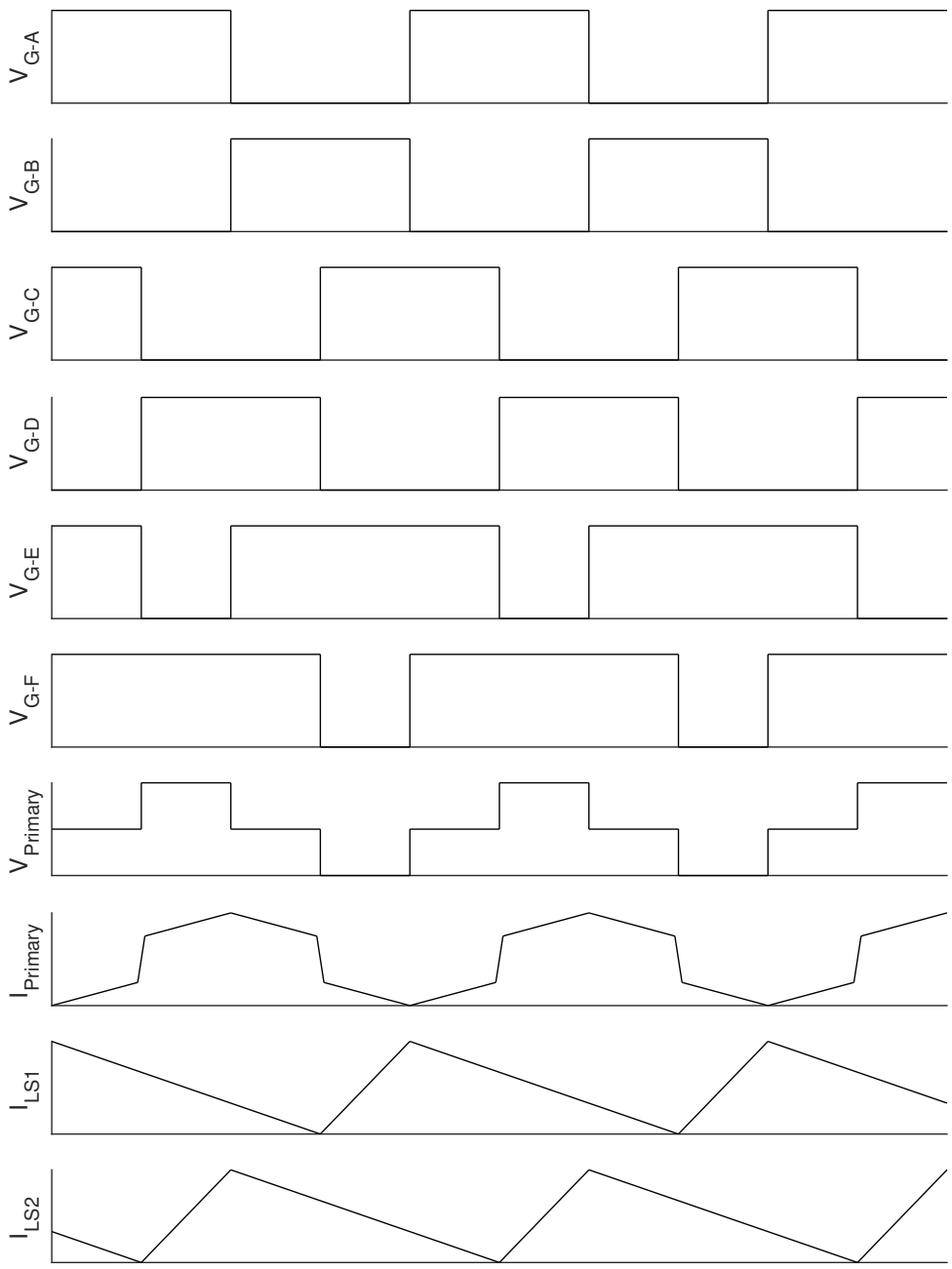

Figure 2.20: Characteristic waveforms of components in a phase shifted full bridge.

2.9 Circuit controller

In order to control the gates of the PSFB converter, the driver circuit LTC3722-1 from Analog Devices will be implemented [15]. The circuit controller both have features that influence other components and will determine how the converter is implemented.

2.9.1 Adaptive delay

The controller includes options to have an adaptive delay for MOSFET switching in order fix the timing for ZVS [15]. By including the switching delay for the MOSFET in combination with the gate driver delay the controller can anticipate when to switch in order to achieve accurate ZVS. The controller measures the input voltage and the voltage on the passive and active leg of the full bridge. The controller also includes a maximum delay where it will try to achieve ZVS since ZVS might not be possible for all load conditions and thus will only wait for the maximum set delay before switching.

2.9.2 Oscillator frequency and external clock

The internal oscillator of the driver circuit can be set to a maximum frequency of 1 MHz depending on the application [15]. The frequency is determined by placing a capacitor which will repeatedly be charged and discharged. The circuit also allows for use of external clocks if the converter is to be used in combinations with other converters. Paralleling more than one converter allows for current sharing and more converters can thus be stacked in parallel to increase the power range. By coupling two converters they can be configured to be out of phase to each other in order to have a more even power delivery.

2.9.3 Current control mode and slope compensation

The LTC3722-1 uses peak current mode control which means that the current on the primary side of the converter is monitored in order to control the converter [15]. The current is monitored by placing a resistor on the source leg of the lower MOSFETs in the full bridge and measuring the corresponding voltage over the resistor. The input from the current sense and the input from the feedback circuit is compared in order to determine an appropriate value for the PWM modulation. The circuit can thus instantly detect if the current is abnormal such in the case of a saturated transformer. Current mode control will also alter the behaviour of the converter which will influence the feedback system which is discussed in Section 2.10.1 [28],[29].

Drawbacks with peak current mode compensation include that current spikes due to switching noise can trigger the set current limit [28]. Faulty triggering due to switching noise can be mitigated by implementing a blanking period which effectively turns off the current sense during a programmable time interval when the converter is switching. When utilising peak current mode control, subharmonic oscillations might occur and cause instabilities when the duty cycle is over 50%. The subharmonic oscillations are a natural part of controller utilising peak current mode, but can be mitigated by the use of slope compensation which is the case for LTC3722-1. The circuit controller introduces a small current to correct for the subharmonic instabilities. Both the blanking time and slope compensation is set when designing the circuit in order to operate correctly for the specific use case.

2.9.4 Circuit protection

The controller includes several protection mechanisms to ensure safe and stable protection of the circuit [15]. The limits need to be set by the designer in a proper manner to ensure that the safety features works as intended. The circuit monitors the input voltage and will stop operating if the voltage is too low. The current will also be monitored and the circuit will firstly turn off the switching state, but if the current is consistently over a threshold, the controller can restart the circuit by initialising a soft start. A soft start in the case of the LTC3722-1 means that it is current-limited and thus will slowly ramp up the current in order to not overload the circuit at start up.

2.9.5 Galvanic isolation

Since there are large voltage differences between the primary, secondary sides, there is a need for physical isolation between the two circuits areas mentioned. The approach that will be approached in this report is by using transformers and an optocoupler. The optocoupler will be required for the feedback signal required for the driver circuit, since its input is acquired directly from the output voltage. The optocoupler will take an input voltage and adjust its output accordingly. This transfer occurs in the optocoupler by emitting light depending on the input to a receiver on the output [30].

2.10 Feedback control

When implementing a converter, it is important to study how the converter can handle load transients since the converter does not always operate in steady state or with a constant load. A converter should be able to respond in a controlled manner to load steps and load surges to ensure a stable output voltage level. The response time is crucial since too slow response times can result in severe output voltage deviations, while a too fast system might result in an unstable output voltage oscillation.

When the load changes, the output voltage will initially rise if the load drops, or decrease if the load increases. By monitoring the change in voltage it is possible to regulate the PWM (pulse width modulation) signal on the primary side MOSFETs in order to correct the output voltage. Connecting the output back to the PWM modulator involves creating a closed control loop of the converter. The connection from output to the modulator must be connected through an error amplifier in order to translate the output voltage to a voltage level that can be interpreted by the control circuit LTC3722-1 in order to regulate the voltage. A typical block scheme of the control loop can be seen in Figure 2.21.

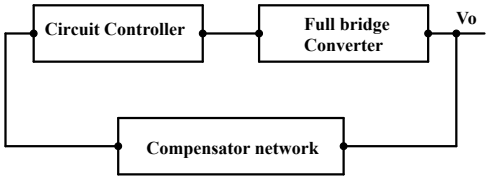

Figure 2.21: Control loop for a PSFB

2.10.1 Modelling of full bridge

In order to construct a compensator circuit, the transfer function characteristics for the PSFB must be determined first, in order for the compensator network to be effective. Important aspects that need to be determined before the designing the feedback system is the output filter. In the case of a current doubler the output filter consists of an output capacitance two inductors in parallel. Another important aspect for the feedback system is the type of control mode used by the control circuit. Common control modes are peak current mode, average current mode and voltage mode [31]. When using any of the two current mode controllers, the converter will consist of two control loops, one inner current loop and the outer feedback loop that will regulate the output voltage specifically. The LTC3722-1 used for this converter uses peak current mode which will slightly alter the behaviour of the converter [15], [32]. Peak current mode reduces the noise immunity compared to average current control mode but has other advantages such as detecting current faults earlier as in the case of transformer saturation. Voltage mode control only is severely slower to detect errors that peak current mode. Current control mode which is discussed more in detail in section 2.9.3.

To model a PSFB with a current doubler, the converter behaviour will be somewhat simplified in order to be able to derive a transfer functions of its behaviour, where the circuit is linearized with a small signal circuit equivalent. From [33]-[34] the PSFB transfer function can be modelled as

$$\frac{v_o}{d} = \frac{R_{load}V_{in}}{NLC_{out}R_2} \cdot \frac{(1 + R_cC_{out}s)}{s^2 + (\frac{R_1}{L} + \frac{1}{C_{out}R_2})s + \frac{1}{LC_{out}}(\frac{R_1}{R_2} + (\frac{R_{load}}{R_2})^2)} \tag{2.23}$$

where R_{load} is equivalent load resistor, L is half of the output filter inductors due to the fact that a current doubler uses two inductors in parallel [33]. R_c is the equivalent series resistance of the output capacitor. R_1 och R_2 can be determined as

$$R_1 = \frac{L_{lk}f}{N^2} + \frac{R_cR_{load}}{R_c + R_{load}} \tag{2.24}$$

$$R_2 = R_{load} + R_c \tag{2.25}$$

Where L_{lk} is the leakage inductance and f is the switching frequency experienced by the transformer.

2.10.2 Compensator network

A compensator network is added in order to close the voltage loop from the output, back to the circuit controller and also compensate the PSFB in order to achieve a stable operation [35]. The compensator network consists of an error amplifier and the complexity of the compensator network depends on the gain and phase of the converter.

The compensator is designed whilst knowing the behaviour of the converter from (2.23) in order to create a stable feedback system [15]. The compensator is designed in order to compensate for the converter behaviour by placing the poles and zeros of the compensator in accordance with the converter. Generally, the compensator should be designed in such a way that the crossover frequency of the system is placed before the zero created by the output capacitance ESR, which is the numerator of (2.23) [15]. The crossover frequency should be placed with a margin to the ESR zero, however, what frequency margin to use is impossible to determine, since small deviations in for example ESR causes the zero to be moved substantially. A type III regulator can be seen in the Figure 2.22. The type III compensator network is regulated and adjusted by selecting the values of the components in the regulator.

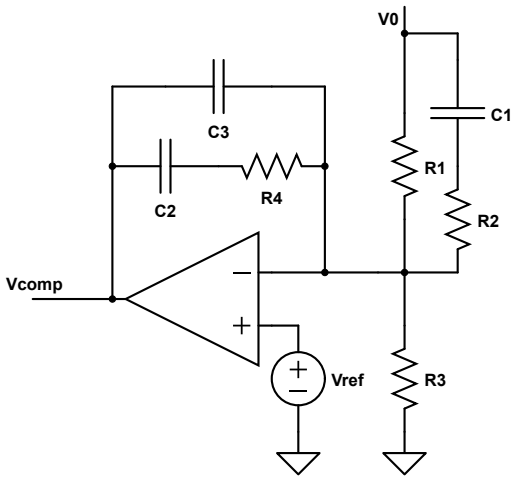

Figure 2.22: Type III regulator

The type III compensator in Figure 2.22 has three poles and two zeros which can be determined as

$$f_{z1} = \frac{1}{2\pi(R_1 + R_2)C_1} \tag{2.26}$$

$$f_{z2} = \frac{1}{2\pi R_4 C_2} \tag{2.27}$$

$$f_{p0} = \frac{1}{2\pi R_1 (C_2 + C_3)} \tag{2.28}$$

$$f_{p1} = \frac{1}{2\pi R_2 C_1} \tag{2.29}$$

$$f_{p2} = \frac{1}{2\pi R_2} (\frac{1}{C_2} + \frac{1}{C_3}) \tag{2.30}$$

Each of these poles and zeros combined with the poles and zeros of the converter in order to combine and create a stable feedback system. A type III compensator will thus have an asymptotic Bode plot and phase response characteristics as displayed in Figure 2.23 and 2.24. f_{p2} will appear at a high frequency where the converter will likely be attenuating signals and the influence of C_3 is negligible and can be disregarded [15]. A type III regulator has a phase boost which will improve on the phase margin of the system in order to keep it stable.

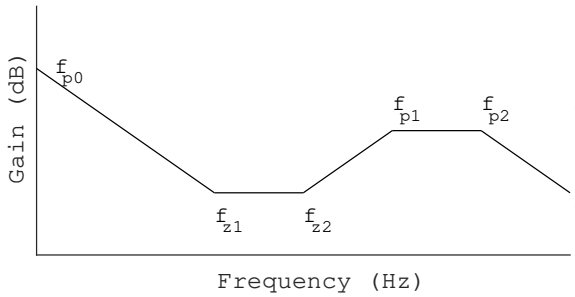

Figure 2.23: Bode plot of type III compensator

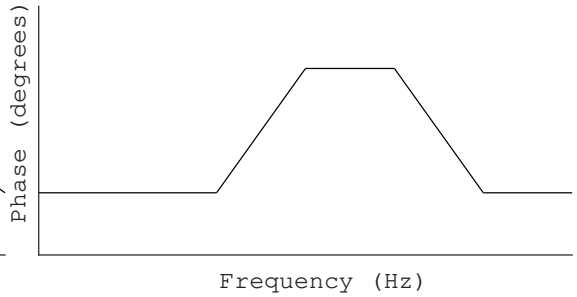

Figure 2.24: Bode phase plot of a type III regulator

2.10.3 Criteria for a stable feedback system

By compensating poles and zeros of the converter with the compensator network, the gain and phase of the system can be specified during the design phase, and a stable feedback system can be created. Important characteristics of the feedback system is the gain crossover frequency which is the point where the gain crosses the zero dB in amplification [36]. All frequencies below the crossover frequency will be amplified whilst all frequencies above the crossover frequency will be attenuated. In general, placing the crossover frequency at higher frequencies will make the converter quicker to respond to variations of the load but might also make the converter overshoot if it is too quick.

The phase margin of the converter, which is the phase difference from -180°at the gain crossover frequency is also important [36]. It is a indication of stability of the system. A phase margin of 45 to 60 degrees could be considered stable.

2.11 LLC converter

The LLC converter is similar to the PSFB construction, utilising either a full-bridge or a half-bridge on the primary side of the converter [37]. There is one significant difference from the PSFB however, the LLC tank. This additional setup presented in Figure 2.25 enables soft switching due to the generation of resonance behaviour. The PSFB instead uses a phase-shifting control to achieve ZVS.

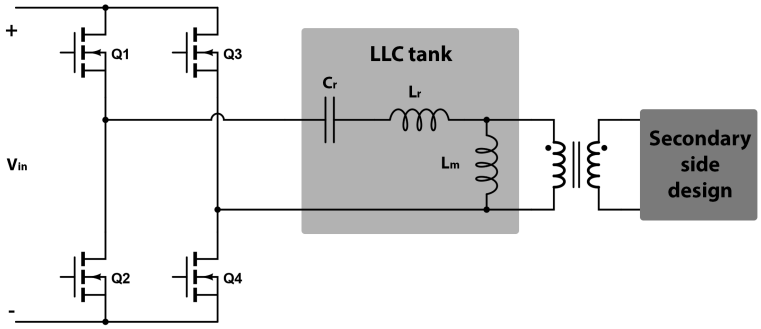

Figure 2.25: LLC

The LLC tank will generate a sinusoidal current waveform with the frequency equal to the switching frequency of the square-wave fed to the LLC tank from the full bridge, offering a possibility of soft switching operation. Both ZVS and ZCS is possible when the switching frequency equals the resonant frequency of the LLC tank, which can be defined as

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.31}$$

where L_r and C_r are the resonant components presented in Figure 2.25. Since the LLC converter can achieve both ZVS and ZCS at the resonant frequency, the LLC converter is generally designed to operate at the resonant frequency during nominal operation in order to maximise the efficiency.

The LLC has two additional operational regions apart from operating at resonance frequency: Below resonance and above resonance, visualised in Figure 2.26. In this Figure multiple gain functions has been plotted with different values of the quality factor Q. The quality factor can be determined using

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} \tag{2.32}$$

$$R_{ac} = \frac{8N_p^2}{\pi^2 N_s^2} R_{load} \tag{2.33}$$

$$R_{load} = \frac{V_{out}^2}{P_{load}} \tag{2.34}$$

It is observable that the quality factor has a linear relation to the load and therefore gives the behaviour of the system during different load conditions. The region when the LLC operates below the resonance frequency occurs when the input voltage is lower than the output voltage. Operating below the resonance frequency is when the risk to enter capacitive mode is largest. During capacitive mode ZVS is not possible, but ZCS can instead be achieved. This is however in most cases not preferred over ZVS due to large voltage spikes occurring when MOSFETs are hard switching.

The converter will operate above the resonance frequency when there is a larger input voltage than the output voltage. The frequency of the switching will vary when load steps occur, where the load rapidly changes. A general approach to ensure resonant frequency during nominal operation is to define the turns ratio of the transformer accordingly.

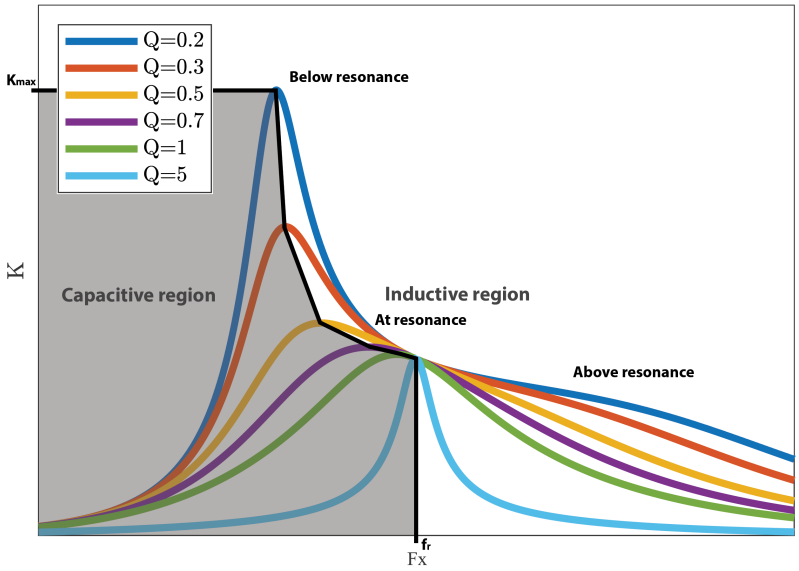

Figure 2.26: LLC

A design parameter that is of interest for LLC converters is the lowest power rating the converter is supposed to deliver. This parameter is of importance since light loads risk to set the LLC into the capacitive region during voltage drops at the load, ultimately resulting in current leading the voltage in phase. In this operation ZVS cannot occur and there is also risk of generating large current spikes during switching that can result in device failure. However, the converter can also be designed to operate in the capacitive region and could be operated with zero current switching (ZCS).

An LLC converter in comparison with the PSFB is operated with a variable switching frequency to achieve different gain for different scenarios according to Figure 2.26. Varying the frequency to achieve ZVS and ZCS implements another level of

complexity compared to only the PWM modulation in the PSFB. The frequency is controlled by modulating the gate signal on the primary side bridge configuration [38]. Modulating the frequency can decrease the switching losses when using ZVS and/or ZCS, however frequency modulation can also cause other components to increase their power losses. When operating far from the resonant frequency, current in the converter will increase which in turn will increase conducting losses. Also, the transformer losses will vary depending on frequency, higher frequency will cause higher core losses but lower frequencies will magnetize the core harder and thus also cause increased core losses. So, in the case of an LLC, the magnetic components needs to be designed to keep the losses at a minimum for a wide frequency range. For the LLC it is therefore important to compare if it is beneficial to always operate with soft switching or if other components might decrease the efficiency instead.

Current sharing LLC converters can be cumbersome due to the frequency dependence compared to the fixed frequency. With resonant converters the tolerances of the components will vary the resonant behaviour which can make the converters have different gain for different frequencies [39]. In such a case the converters will not equally share the load. To better balance the power delivery more complex control strategies would have to be implemented [40].

3

Case set-up

The project consists of five main objectives: design, develop, construct, verify and compare the PSFB converter. The aim is to reach the goals stated in chapter 1.2

3.1 Design process

There is a requirement to follow several design limitations when designing the circuit meant to replace the present converter solution. The design limitations exists partly since Saab has already ordered some components in order to save time. Other design limitations exists to ensure that converter is suitable for the application that it is supposed to be used for. The project will investigate the usage of a phase shifted full bridge as the circuit design, with the driver circuit LTC3722-1 used to operate the converter [15]. The main design task is to design a functional phase shifted DC/DC converter for the given operational requirements. The selection of components and implementation of the driver circuit will be an essential early step in the project process.

The design of the converter will be influenced by the data-sheet of the driver circuit LTC3722-1 provided by Analog devices, the manufacturer to the driver circuit. Furthermore many design choices will be implemented with the aid of calculations and research in scientific reports.

3.2 Developing the circuit

A circuit model will be constructed, simulated, tested, further developed and verified. This will be conducted using LTspice, a simulation software published by Linear Technologies, now part of Analog devices. Caution will be taken when considering the obtained results due to the fact that simulations often miss problems that occur in the physical hardware. All simulated components are to some degree ideal, resulting in non-realistic results.

3.3 Construction of the converter

Eventually the required components will be ordered after sufficient simulation data has been obtained. There will also be a requirement of designing a transformer with the availability to arrange order of windings, allowing for more flexibility when calibrating the output voltage during the construction of the prototype.

The full bridge circuit will be constructed using the selected components and the LTC3722-1 driver circuit according to the final design model. Tests will be conducted in parallel with the construction to ensure that construction errors are excluded.

3.4 Verification process

Finally there will be a verification process of the circuit board. During this process, measurements will be conducted to ensure operation within the required specifications. The obtained data will be used to analyse the differences in performance compared to the prior solution. Interesting parameters to verify includes the output voltage and current ripple as well as the input and output voltages and currents to enable efficiency measurements.

The verification process will involve a risk of electrical shock, since there will be high voltages up to 400 V DC present during operation of the circuit. To eliminate risking the health to the person/persons conducting the verification, all tests are done in accordance to safety regulations for high voltage applications.

3.5 Comparison with an alternative solution

There will be an interest in comparing the final product with another solution for its given task to ensure the legitimacy of the constructed PSFB. The other solution that this PSFB will be compared to is a LLC converter. The LLC converter is designed towards another power level and therefore the comparison will be tested at the rated values of each converter in order to ensure adequate comparison of their operation.

Areas of interest when comparing the solutions consists of mainly efficiency, amount of output disturbance, load variation response and design complexity.

3.6 Measurement setup and methodology

In order to verify and compare the converters against each other, certain measurements of the converters were required. The general setup of how the converters were connected is presented in Figure 3.1. The power supply unit (PSU) were set to desired voltage level to power the converter. The converter is powering a current controlled DC electronic load where the current is adjusted to meet the desired output power of the converter. In order to make the PSFB converter operate it requires

a 12 V input signal to its driver circuits, therefore an additional PSU is used to feed the primary and secondary side of the converter individually. the two separate 12 V signals are isolated from each other in order to maintain the galvanic isolation. This signal side PSU is not required for the LLC converter since the signal is generated internally through an extra transformer setup.

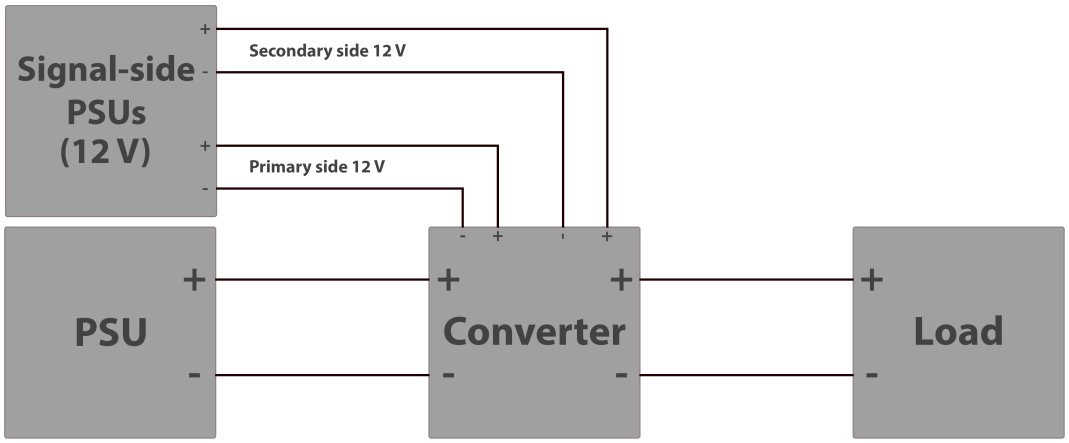

Figure 3.1: The general approach of how the converters were tested

The PSFB converter was measured in several different approaches, where all the positions used for the measurement instruments are presented in Figure 3.2. Noteworthy is that the current measurement was conducted using a clamp-on current probe in order to disturb the circuit as little as possible. The LLC converter was only tested by measuring the input and output voltages and currents, which allowed for an efficiency approximation.

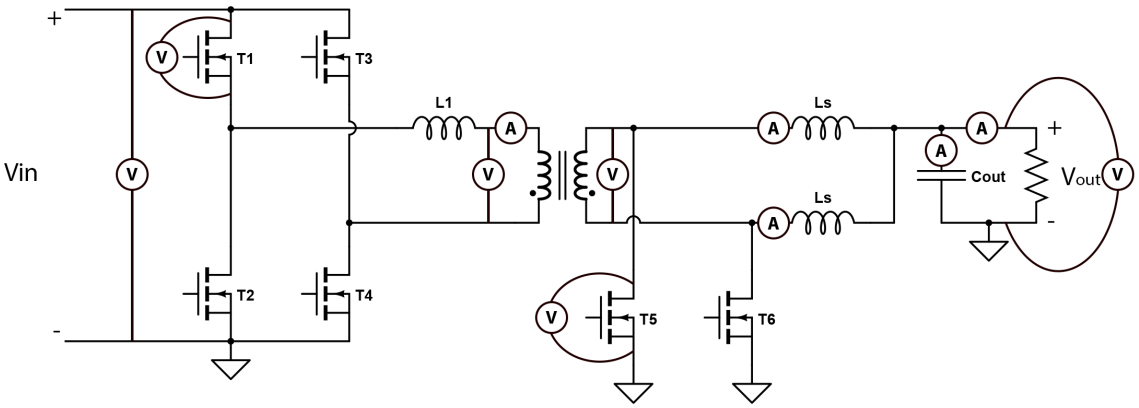

Figure 3.2: Placements of voltage and current measurements of the PSFB converter

3.7 Converter specifications

This section includes the ratings of the converter used for this project. The nominal PSFB ratings are displayed in Table 3.1.

Table 3.1: Phase shifted full bridge specifications

	Value	Unit
P_{max}	1.2	kW
$V_{in.min}$	350	V
$V_{in.max}$	400	V
$V_{out.nom}$	56	V
f_{min}	200	kHz

The specifications of the LLC converter that the PSFB converter was compared against are presented in Table 3.2.

Table 3.2: LLC specifications

	Value	Unit
P_{max}	5	kW
$V_{in.min}$	340	V
$V_{in.max}$	500	V
$V_{out.nom}$	29	V
f_{min}	170	kHz
f_{max}	230	kHz

4

Results

In this chapter the results of the design choices selected for the PSFB are presented. The design choices are based on the theoretical background. Thereafter the measured results on the physical converter is presented. Due to an error in the current sense feedback loop, the converter was tested up to an input voltage of approximately 200 V and a maximum output power of 400 W. At the end of this chapter, the performance of the LLC converter is presented.

4.1 Phase shifted full bridge circuit design

The designed circuit schematic for the PSFB converter can be observed in Figure 4.1, more in depth results will be presented in more detail further along in the chapter. More information regarding the components can be obtained from appendix A.1.

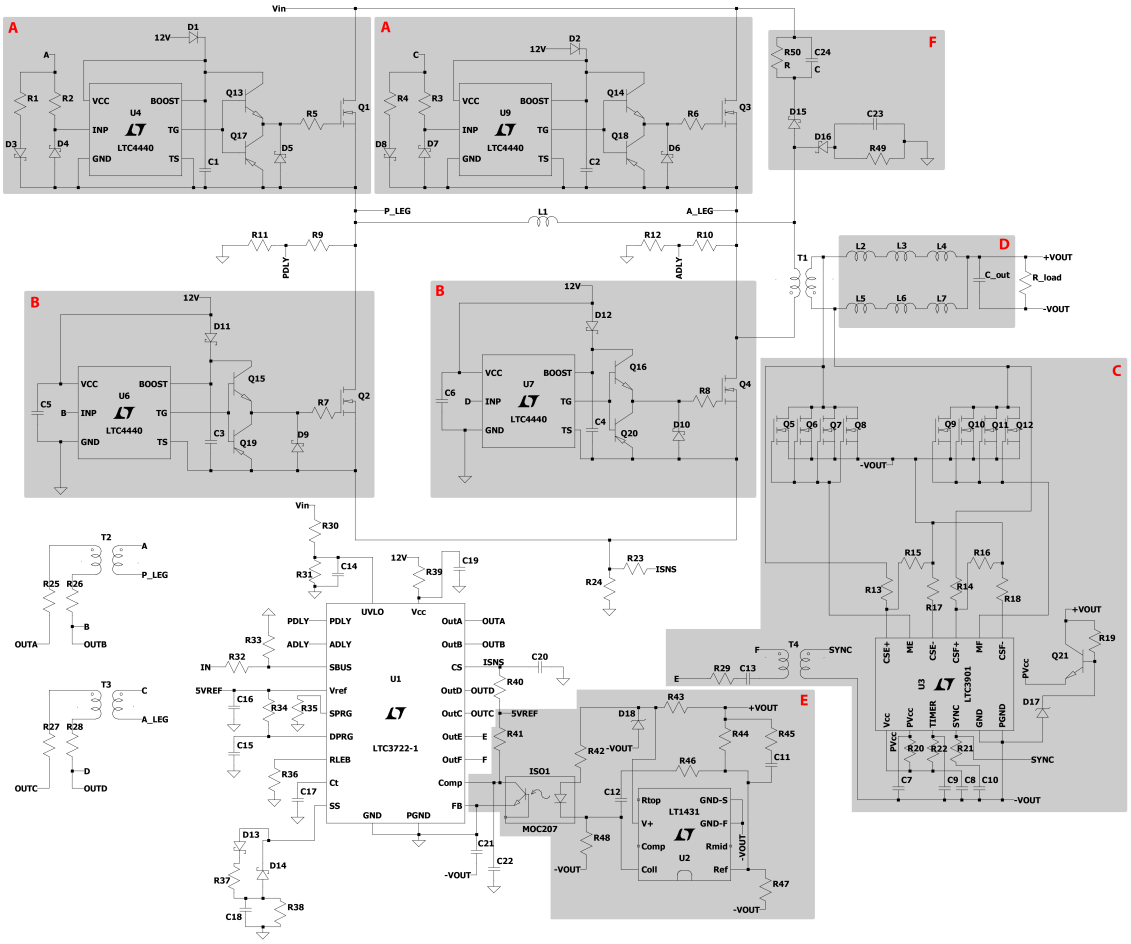

Figure 4.1: Circuit design including all components.

4.1.1 MOSFET selection

The transistors used for the circuit are MOSFETs SCT4026DW7TL, developed by ROHM Semiconductors for the primary side. This decision is based on conduction losses, low output capacitance and sufficient breakdown voltage to survive input voltages with transients. The setup consists of one MOSFET for each gate, 4 in total for the primary side. Each of the MOSFETs have an on-resistance R_{ds} of 26 mΩ. The parasitic output capacitance for one MOSFET is 111 pF, which can be determined by studying the data sheet of the MOSFET. The conduction loss for one transistor can be determined to 0.32 W using (2.2) for an ideal converter with an input voltage of 350 V and output power of 1200 W. Switching losses for the MOSFET are presented in Section 4.2.2.3 where the actual MOSFET waveforms are presented.

The transistor chosen for the secondary side was the MOSFET UF3SC065030B7S, developed by UnitedSiC. In this case a total of three MOSFETs are connected in parallel per side which can be seen in section C in Figure 4.1. This design of using three per signal gives a reduced conduction loss due to the decreased R_{ds}, see (2.2). Dissipating the losses over three MOSFETs will also decrease the temperature development per MOSFET. The trade-off will be that this setup increases the total capacitance of the equivalent MOSFET, but this is a sufficient trade-off since the secondary side draws large amounts of current. Further the capacitance value is most important for the primary side since it affects the availability to enable ZVS, which the secondary side MOSFETs does not influence. The on-resistance R_{ds} for one of the MOSFETs on the secondary side is 27 mΩ, resulting in a total of 9 mΩ for each signal when using three in parallel. The Conduction loss for each MOSFET trio can therefore be determined to 2.65 W using an RMS current of 16 A determined from simulations.

4.1.2 Primary side gate driver

In order to enable the gate signal to reach a potential where it surpasses the MOSFET source signal for Q1 and Q3 in Figure 4.1, the bootstrapping driver LTC4440 will be used [41]. The LTC4440 usually has a 100 V limit when TS is referenced to ground. But by connecting TS together with LTC4440s ground to the source leg of the MOSFET, the LTC4440 will have the same reference as the MOSFET. However, the signal from the driver circuit LTC3722-1 thus needs to be isolated by using a signal transformer in order to make the design function, see T2 and T3 in Figure 4.1. Diodes and resistors are connected to the input signal according to R1, R2, D3 and D4 with the purpose of limit the current flow into pin INP while also enable a direct connection to the floating reference ground for the signal transformer to enable discharge of energy stored in the signal transformer, see Figure 4.2.

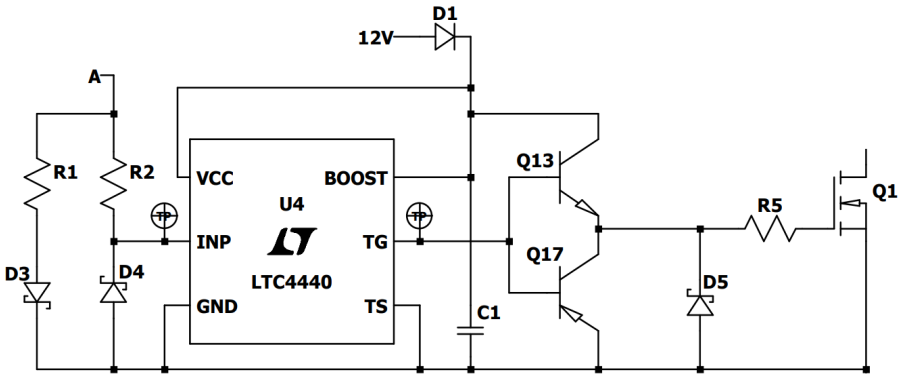

Figure 4.2: Circuit design for implementation of LTC4440 mattering MOSFETs Q1 and Q3

The external supply voltage of 12 V will be protected using diode D1, where the 12 V signal will be forwarded to the MOSFET gate through transistor Q13 when an on-signal is obtained from signal A. During turnoff the gate will instead be connected to the source leg through Q17. By using the setup of Q13 and Q17 to send a 12 V signal to the gate of Q1 instead of directly connection output pin TG to the gate of Q1 removes the restriction of maximum current flow from the gate driver circuit LTC4440 and instead places the current restriction only upon the 12 V power supply when enabling Q1. This setup potentially allows for faster switching due to a faster gate charge of Q1. D5 offers extra protection for the MOSFET, intending to limit the maximum voltage applied between gate and source. R5 is added before the gate of the MOSFET in order to control the switch speed by limiting the current flow, essentially to regulate turn on/off oscillations at the cost of efficiency. C1 plays a crucial role in order to ensure 12 V to boost according to the bootstrapping method mentioned in chapter 2.5.1. The complete implementation to the final circuit for gate signals A and C is marked with "A" in Figure 4.1.

The circuitry surrounding LTC4440 for signals B and D will be similar to the circuitry for signals A and C, however some differences are present as shown in Figure 4.3.

The pins TS and GND are not connected since the voltage connected to TS will not reach above 100V, therefore that extra circuitry becomes redundant. By separating the pins there is no need for a signal transformer and signal OutB and OutD from LTC3722-1 can be directly connected to LTC4440s Input pin. Otherwise, the principle is identical to the setup for signals A and C. This implementation in the complete circuit is marked with "B" in Figure 4.1.

The results of the physical implementation of the gate driver is displayed in figures 4.4 to 4.6 below where the gate-source voltage is presented, before and after the gate driver circuit. From the figure it is observable that the gate source voltage is delayed compared to the signal emitted from the driver circuit LTC3722-1. The gate source voltage reaches close to 12 Volts but due to the diodes D1 and D11 in Figure 4.2 and 4.3 there is a small voltage drop due to the forward voltage of the diodes.

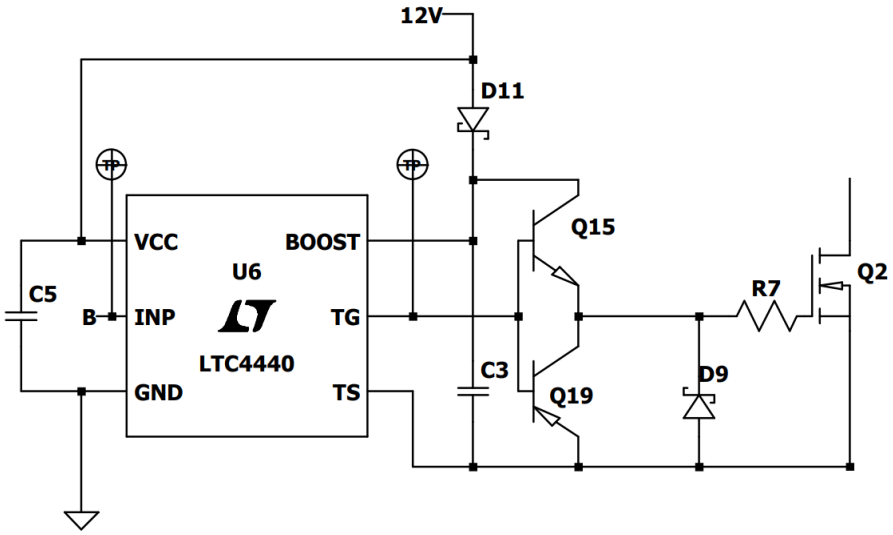

Figure 4.3: Circuit design for implementation of LTC4440 mattering MOSFETs Q2 and Q4.

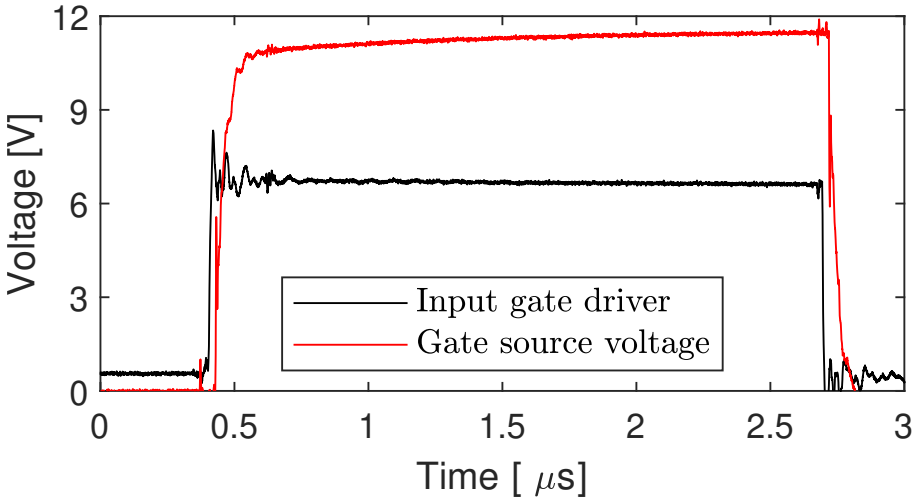

Figure 4.4: Measured input and output voltage of the primary side gate drivers. Input gate driver = B & Gate source voltage = V_{GS} for Q2 in Figure 4.3.

The delay present in Figure 4.4 is of importance since it affects the tuning of the switching signals and needs to be considered in order to achieve ZVS. Further visualisation of the delay imposed by the gate driver is presented in Figures 4.5 and 4.6. The turn on delay is determined by the time differnace between the two signals at the point where they have reached 50% of its expected voltage amplitude. With this definition the turn on delay is determined to 41 ns.

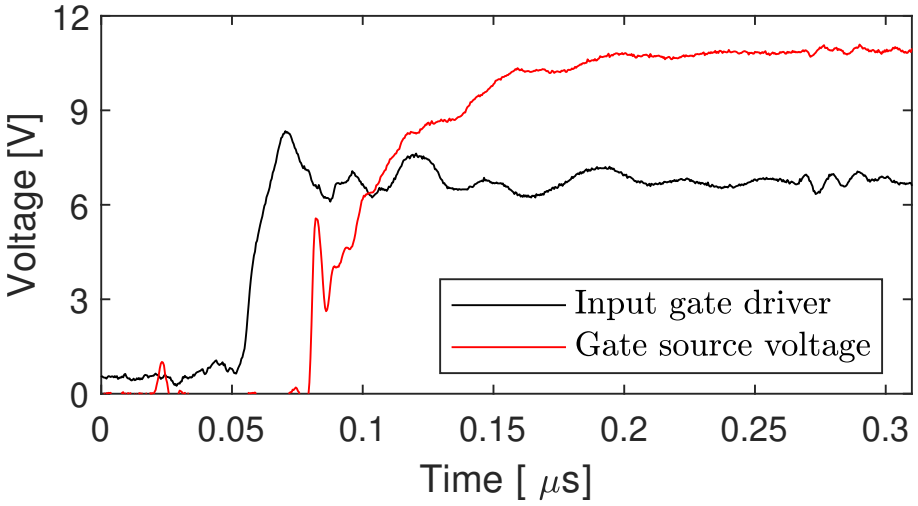

Figure 4.5: Measured turn on delay on the primary side gate drivers.

The turn off delay is determined using the same definition as for the turn on delay, where it is determined to 42ns. Both the turn on and off delays are presented in the data sheet of the driver circuit to be 30 and 28 ns, that delay correlates to driving a MOSFET with input capacitance of 1000 pF [41]. The MOSFETs used in this circuit, which are presented in Figure 4.1, has an input capacitance of approximately 2300 pF, resulting in an increased delay compared to the one offered in the data sheet.

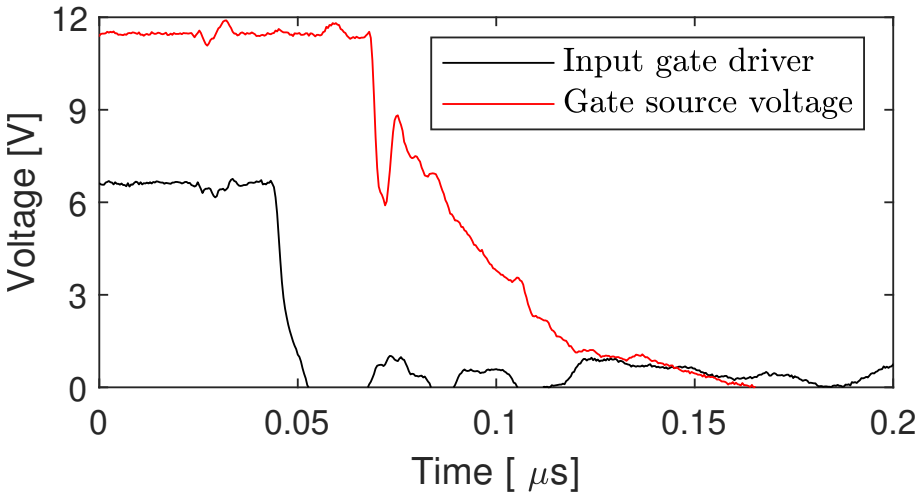

Figure 4.6: Measured turn off delay on the primary side gate drivers.

4.1.3 Secondary side design

4.1.3.1 MOSFET gate driver

As mentioned in chapter 2.5.2, the resistors R13 to R18 are crucial for negative current protection provided by the gate driver LTC3901, where the calculated values using (2.7) to (2.10) can be found in Appendix A.1. Furthermore, the gate signals

OutE and OutF from LTC3722-1 will be connected to the gate driver through a signal transformer in order to keep the isolation between the primary and secondary side of the circuit, see T4 in Figure 4.7.

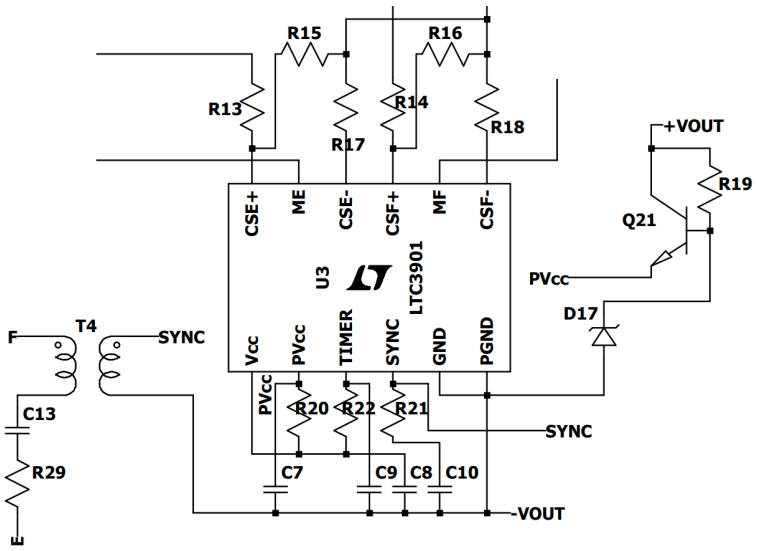

Figure 4.7: Circuit design for implementation of LTC3901.

One way to power the gate driver through pin PV_{CC} is using the design consisting of Q21, R19 and D17 combined with the output voltage. This design will ramp up the input voltage to 10 V in accordance with the output voltage, which provides a soft start and removes the requirement of an external power source. The components C7 to C10 and R20 to R22 are determined using standard values provided from the data sheet of the driver circuit LTC3901 [17]. Those components are mainly used for signal filtering and tuning for LTC3901. The implementation of this gate driver is marked with "C" in Figure 4.1.

However, just as in the case of the primary side gate driver, using a secondary side gate driver will generate delays. Further delays will also be present due to the signal transformer T4 in Figure 4.1. The delay of the gate signal is presented in Figure 4.8, where a more detailed image of the turn-on and off delay is observable in Figures 4.9 and 4.10. The turn on delay was determined in the same manner as for the primary gate drivers and was determined to be 50 ns whilst the turn off delay was determined to 42 ns.

The delay presented in the data sheet for the LTC3901 circuit was 60 ns when using a MOSFET with an input capacitance of 4700 pF [17]. When the gate driver operates in this circuit, powering MOSFETs Q5 to Q12 in Figure 4.1, each equivalent input capacitance is 4500 pF, resulting in less delay than what was presented in the data sheet.

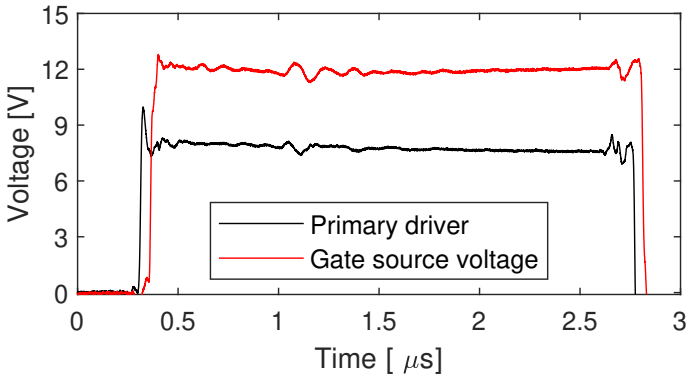

Figure 4.8: Measured input and output voltage of the secondary side gate driver. Primary driver = F & Gate source voltage = MF in Figure 4.7.

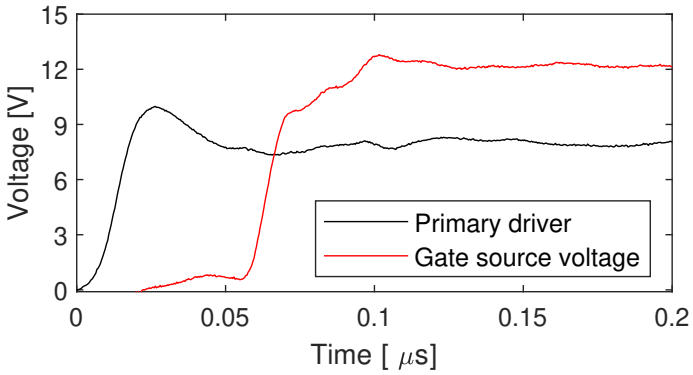

Figure 4.9: Zoomed in turn on delay for secondary side MOSFETs from Figure 4.8.

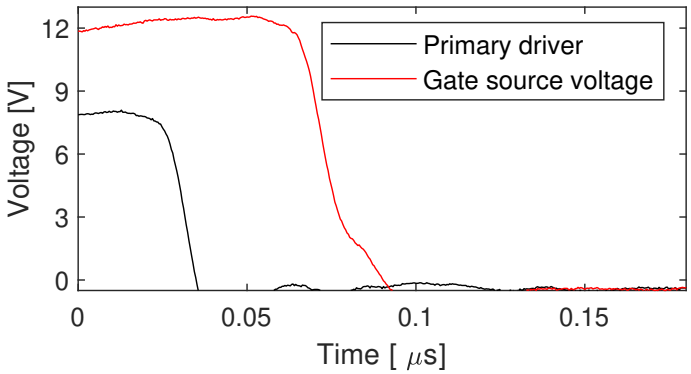

Figure 4.10: Zoomed in turn off delay for secondary side MOSFETs from Figure 4.8.

4.1.3.2 Snubber design

To ensure limited oscillations due to the hard-switching MOSFETs on the secondary side of the converter, the snubber block "F" in figure 4.1 was implemented. It consists of two RCD snubbers, since the full bridge switches polarity and therefore requires protection against both positive and negative voltage transients. It was decided to implement the snubber on the primary side of the transformer since then the positive over-voltage protection snubber was able to be connected to V_{in}, setting the lowest threshold of the snubber operation to only occur when surpassing the input voltage. This would not be possible if located on the secondary side since the positive voltage amplitude over the secondary side transformer will always be approximately two times larger than the output voltage, leading to a constant damping of the positive voltage to half the expected voltage magnitude. Therefore, to ensure correct operation the RCD snubber is located on the primary side.

4.1.3.3 LC-filter and bulk cap selection

The output capacitor, inductors L_{S1} and L_{S2} according to Figure 2.11 are designed using the specifications listed in Table 4.1 combined with (2.17) to (2.22). The design parameters are presented in Table 4.2.

Table 4.1: Reference values used for determining the output inductor and capacitor.

	Value	Unit
V_{out}	56	V
ΔV_{out}	1	%
$P_{out.min}$	400	W
$P_{out.max}$	1200	W
T	5	µs

Table 4.2: Calculated values for the inductors and the bulk capacitor.

	Value	Unit
I_{out}	7.14-21.43	A
I_{LS}	3.57-10.71	A
$\Delta I_{LS.pp}$	7.14	A
L_S	28.22	µH
$\Delta I_{C_{out}}$	4.37	A
R_c	128	mΩ

The implementation of the LC-filter in the complete circuit is marked with "D" in Figure 4.1.

4.1.4 Transformer Selection and design

The use of a current doubler simplifies the secondary side of the transformer, since there is only one secondary side winding used. The turn ratio for a current doubler can thus be determined from (2.11) where $V_{in(min)}$ and V_{out} are from the converter specification set to 350 V for the input voltage and 56 V on the output. The maximum allowable duty cycle was set to 0.9. The maximum allowable turn ratio was then determined to 2.8. Since the turn ratio needs to be fractions between even number of turns for both primary and secondary side the turn ratio was selected to 2 which will also give some headroom for the duty cycle.

The oscillator frequency was set to 400 kHz, and the transformer will experience half of the oscillator frequency. The high switching frequency means that material selection is important. Due to Eddy currents the most suitable material for the core is ferrite. A comparison between different sized ferrite cores allows the possibility to compare which core are suitable set for different number of turns in terms of peak flux density which is presented in Table 4.3.

Table 4.3: Peak flux density for different ferrite cores for different number of primary turns.

N_p	E100/60/28	E65/32/27	ETD59/31/22	E42/21/20
	Magnetic Flux density [mT]			
2	612	841	1222	1923
4	306	420	611	961
6	204	280	407	640
8	153	210	305	480
10	125	168	245	385
12	102	140	203	320
14	87	120	175	275
16	76	105	153	240
18	68	93	136	214
20	61	84	122	192

The flux densities calculated in Table 4.3 is calculated from (2.13) using the nominal input voltage of 400 V, a maximum duty cycle of 0.9 and a time period of 5 μs which corresponds to the transformer switching frequency of 200 kHz. From Table 4.3, a higher turn ratio yields lower flux peaks which in turn will yield lower core losses. The ferrite material also saturates at 300 mT and thus eliminates the use of most of the low number of primary turns from all cores. In the end the core E65/32/27 from TDK was selected since it has a rather large effective area and a large window area for the windings. The E100/60/28 yields a lower flux density, but the overall size of the core is much larger and would increase the overall size of the converter significantly and the core losses are only slightly reduced.

To achieve a low flux swing in the transformer, 18 turns was wound on the primary to have a low flux swing while still ensure enough space to fit the windings in the window area. The layout through the sectional window area of the transformer was determined according to Figure 4.11.

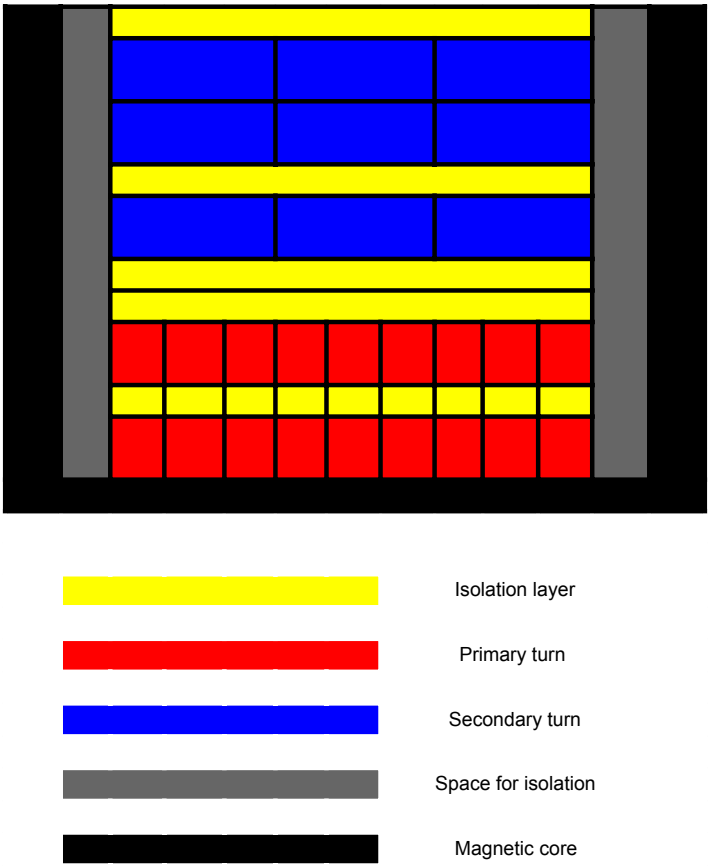

Figure 4.11: Cross-sectional transformer winding.

The layout of the windings was chosen to keep the winding procedure manageable, by alternating windings the leakage inductance would decrease further, but at the cost of increased complexity of the winding procedure. Since a larger leakage inductance would improve ZVS, the layout consists of all the primary wires close to the core and secondary wires on top of the primary windings.

Both primary and secondary side windings consist of litz wire to counteract increased resistances due to skin effect. The skin depth for a round copper conductor at 200 kHz was determined using (2.16), and is 0.145 mm. The litz used consists of multiple 0.1 mm diameter copper wires. Since the skin depth is larger than the diameter of the wire the skin effect will not increase the overall winding resistance. The total amount of copper area seen placed into the window area is 68 mm^2 for the primary side and 78 mm^2 for the secondary side. The core has a window area of 562 mm^2 which gives an ideal copper fill factor of 0.28. The low fill factor is just for the conducting wires, isolation tape and the fact that the wired does not ideally fill up the window area will yield in a fill factor that is close to 1 and thus fills up almost the whole window area.

4.1.4.1 Transformer parameters

The transformer parameters are displayed in Figure 2.18, where the winding resistance R_1 and R_2 were measured with a four-pole resistance measurement. L_{lk1} was determined by short circuiting the secondary side of the transformer whilst measuring the inductance with an LCR-meter. The measurement of L_{lk2} was done in a similar manner but for the secondary side with a short circuited primary winding. L_m was measured with an LCR-meter on the primary side whilst the secondary side was an open circuit. The resulting values from the measurements are displayed in the Table below.

Table 4.4: Resulting Transformer parameters.

	Value	Unit
R_1	12	$m\Omega$
R_2	7	$m\Omega$
L_{lk1}	5	μH
L_{lk2}	1.6	μH
L_m	2.5	mH

4.1.4.2 Transformer loss estimation

Core losses are based on the peak flux density and for the E65/32/27 with 18 primary turns results in a flux density of 93 mT. From the datasheet of the core material, the relative core losses per core volume for a frequency of 200 kHz and a flux swing of 93 mT can be estimated, multiplying with the total volume of the core results in the core losses.

The 93 mT flux swing is a worst-case scenario, where the duty cycle is maxed out at 400 V at the input, in steady state the duty cycle will be lower which will decrease the voltage-second product in (2.13) and thus decrease the flux swing and peak flux density. The voltage-second product can be determined from the numerator in (2.13) and is summarised from different scenarios together with the core losses in Table 4.5 below. The duty cycle used can be determined from rearranging (2.11).

Table 4.5: Resulting magnetic properties and core losses for different scenarios and temperatures at max power.

Scenario Load= 1.2 kW	Voltage-second [mWb]	Flux density [mT]	Core losses [W]	
Maxed duty Vin=400 V D=0.9	1.80	93	100 °C	13.8
			25 °C	23.6
Maxed duty Vin=350 V D=0.9	1.58	82	100 °C	11.2
			25 °C	17.5
Steady state Vin=400 V D=0.56	0.56	60	100 °C	6.2
			25 °C	7.9
Steady state Vin=350 V D=0.64	0.56	60	100 °C	6.2
			25 °C	7.9

At steady state core losses are reduced compared to when the converter is operating at its limits. The core material also operates more efficiently for core temperatures above ambient temperature. Copper losses for the circuit can be estimated using (2.14) where the resistance for ambient temperature copper windings is presented in Table 4.4. By using the simulated current values, it is possible to estimate copper losses. Primary side copper losses can be estimated to 0.77 W for an input voltage of 350 V and a max output power. Whilst the secondary side copper losses are estimated to 1.8 W.

4.1.5 Zero voltage switching capabilities

With the primary MOSFETs having a parasitic output capacitance of 111 pF together with the sum of leakage inductance and primary inductance of 8.3 μH the ZVS minimum load condition can be determined according to (2.4). The input voltage will determine the minimum load to achieve ZVS. A higher input voltage would result in a lower current for a given load. The resulting minimum power required to achieve ZVS is displayed in the Table below for the upper and lower voltage limit.

Table 4.6: Lowest possible input power in order to achieve Zero voltage switching.

Input voltage (V)	Input current (A)	Input power (W)
350	2.1	731.5
400	2.38	955.5

4.1.6 Feedback circuit design

The feedback circuit has been designed as displayed in Figure 4.12 which corresponds to section E for the final circuit design in Figure 4.1. LT1431 is used and corresponds to the error amplifier in Figure 2.22 and works as a shunt voltage regulator. By regulating the voltage seen on the Collector pin (Coll) the circuit can regulate the voltage over the optocoupler MOC207. The optocoupler provides galvanic isolation between the primary and secondary side and based on the current flowing through the optocoupler diode the voltage over the comparator pin on LTC3722-1 will be determined, resulting in PWM modulation. Zener diode D18 and resistance R43 acts as a voltage divider where the breakdown voltage of the Zener diode is used to keep the voltage constant independent of the output voltage. All excess current will flow through the diode keeping the voltage constant over the optocoupler.

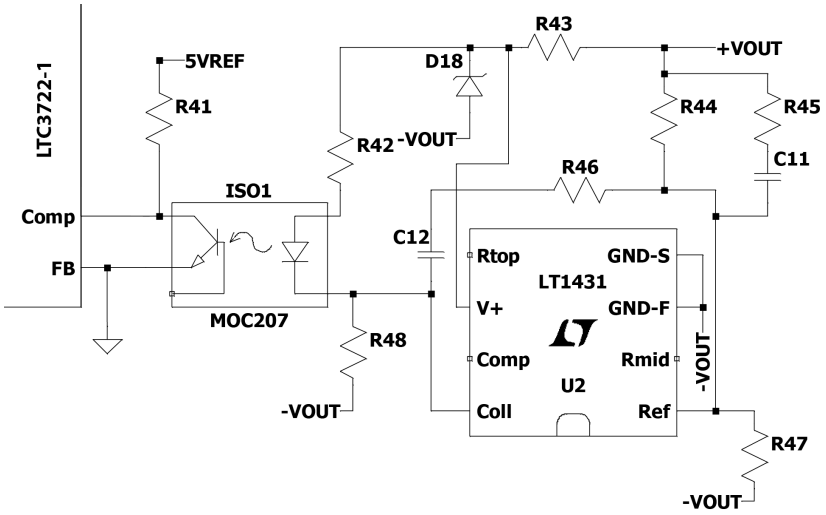

Figure 4.12: Circuit design for implementation of the feedback system.

Resistors R44 to R47 and capacitors C11 and C12 corresponds to the components of the Type III regulator seen in Figure 2.22. But in order to select the components the circuit the behaviour of the converter must firstly be determined. By using (2.23)-(2.25) with the parameters displayed in the Table below, the Bode plot of the converter can be determined.

Table 4.7: Values used for the phase shifted full bridge transfer function.

	Value	Unit
R_{load}	2.6	Ω
V_{in}	400	V
N	2	
L	15	μH
C_{out}	1350	μF
R_c	8.8	$m\Omega$
R_1	0.61	Ω
R_2	2.61	Ω

The resulting Bode plot of the converter thus become

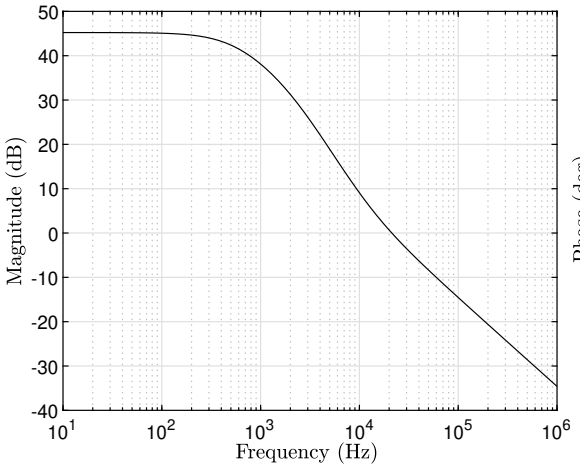

Figure 4.13: Bode gain plot of converter behaviour.

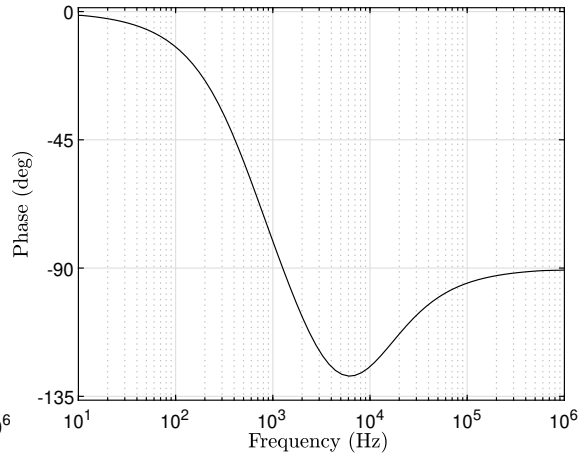

Figure 4.14: Bode phase plot of converter behaviour.

from Figure 4.13, the PSFB will amplify low frequency content and attenuate all frequencies above the crossover frequency which is around 20 kHz. The gain crossover frequency should however be placed before the zero created by the output filter of the converter which is placed at around 14 kHz. The behaviour of the converter is modified by the implementation of the Type III regulator in Figure 2.22. By placing the poles and zeros of the compensator network the phase margin which is seen in Figure 4.14 can be kept stable. The phase margin is around 60 degrees for the converter. The components used in the Type III regulator are presented in Table 4.8 and are referenced to the notations used in Figure 2.22 and 4.12.

Table 4.8: Values used for Type III regulator.

Name used in Type III	Name in Circuit	Value
R1	R44	82 $k\Omega$
R2	R45	82 $k\Omega$
R3	R47	3838 Ω
R4	R46	100 $k\Omega$
C1	C11	1 nF
C2	C12	100 nF
C3	-	-

With the selected values, the poles and Zeros can be calculated using (2.26)-(2.30) and are presented in Table 4.9.

Table 4.9: Zeros and poles for the compensator network.

	Frequency [Hz]
fz1	970
fz2	200
fp0	15
fp1	1940
fp2	-

The pole $fp2$ is neglected due to not using the capacitance. A small would place the pole at high frequencies where the converter would already attenuate the signal. The poles and zeros of Table 4.9 generates the following transfer function behaviour

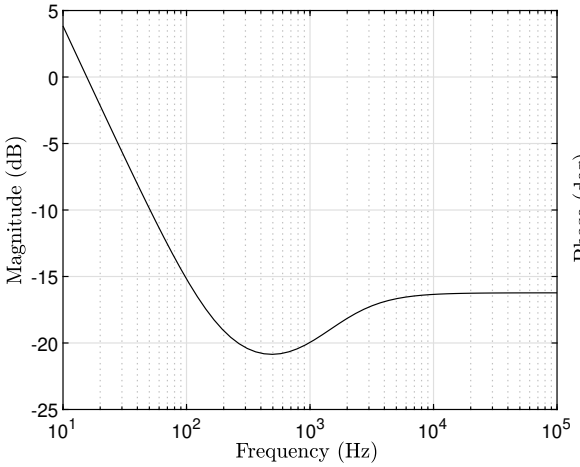

Figure 4.15: Bode gain plot of converter behaviour.

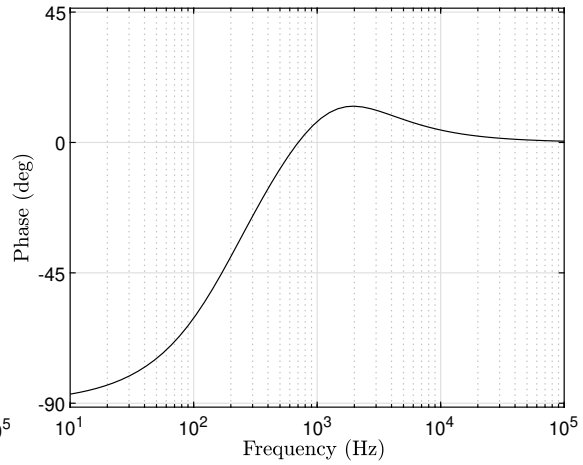

Figure 4.16: Bode phase plot of converter behaviour.

by placing a pole at low frequency as seen in Figure 4.15 the converter speed can be decreased in order to place the crossover frequency below the zero created by

the output capacitor. The phase response seen in Figure 4.16 ensures that the phase margin of the converter is not decreased by the compensator. Combining the converter and compensator behaviour will give the overall system behaviour which is displayed below.

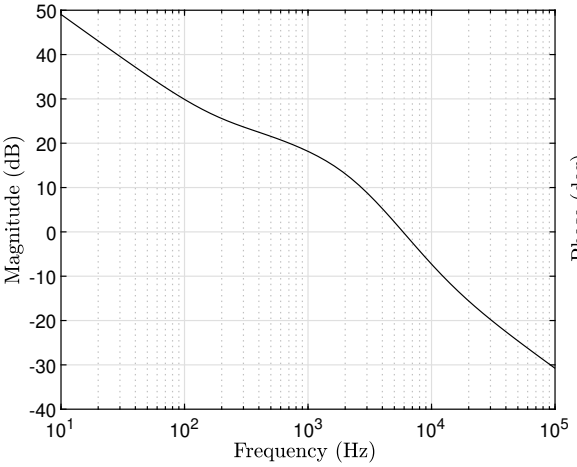

Figure 4.17: Bode gain plot of converter behaviour.

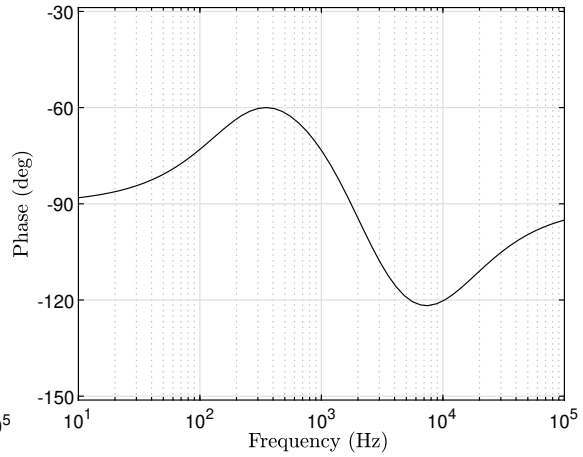

Figure 4.18: Bode phase plot of converter behaviour.

The overall converter can be observed in Figure 4.17 and 4.18 where the converter will have a crossover frequency close to 5 kHz and thus a margin of 9 kHz to the converter zero created by the output filter. The phase margin remains at 60 degrees.

4.1.7 Driver circuit setup

The section covers how LTC3722-1 and corresponding features are implemented. The components presented below can be seen in Figure 4.1 and their specific values are listed in Appendix A.1.

The converter was decided to be designed for a switching frequency of 200 kHz, resulting in a required 400 kHz oscillator frequency. In this case the internal oscillator is used since it will not be coupled in parallel with other converters. The frequency is set by selecting the value of capacitor C17 according to data sheet of the driver circuit.

A soft-start for the converter is implemented to slowly ramp up the converter operation in order to limit large current spikes during start up. The soft start feature is implemented using a capacitor which is slowly charged which will determine the soft start duration. In this case a resistor in series is also used to allow for a small DC offset when starting the circuit. Two diodes are also placed in opposite directions to allow for fast discharging of the capacitor if the circuit need to recommence a soft start. The soft start setup can be seen in Figure 4.19 where its implementation is used in the final design according to Figure 4.1.

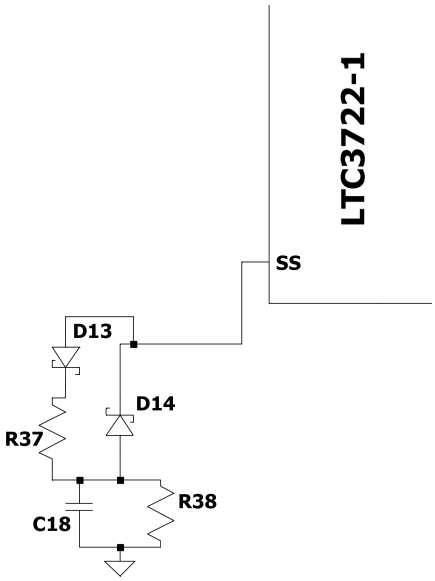

Figure 4.19: Circuit design for implementation of the soft start.

The current sense of the PSFB measures the primary side current in peak current mode. The measured current will be compared to a custom current limit. When the current exceeds the limit, the controller will terminate the switching state and proceed with the next step. Even higher currents cause the controller to recommence a soft start. The current is sensed by placing a resistor to ground at the source leg of the lower MOSFETs of the full bridge. The resistor used is R24 in Figure 4.1. Resistor R23 controls slope compensation by adding a slope to the current to avoid false triggering due to sub harmonic oscillations occurring in the circuit.

The circuit also has an under-voltage lockout set to 320 Volts where the converter will not start to operate unless the input voltage exceeds 320 v. The under-voltage lockout is set by placing a voltage divider to the DC link input voltage. In Figure 4.1 the voltage divider corresponds to R30 and R31.

An active delay is set in order to predict and switch as close to zero volts over the transistor as possible. The delay is based on the switching delay from the MOSFET and the gate driver delay. The tuning of the delay is done by placing a voltage divider at the DC input (R32 and R33), active leg (R10 and R12) and the final one at the passive leg of the full bridge (R9 and R11). The maximum allowable delay for ZVS is set by changing R34 in accordance with LTC3722-1 data sheet.

To ensure that the primary side and secondary side are separated through a galvanic isolation, a signal transformer is required between LTC3722-1 and LTC3901, since LTC3722-1 also controls MOSFET E and F. The signal transformer is labelled T4 in Figure 4.1. The optocoupler marked as ISO1 in Figure 4.1 is implemented to isolate the feedback circuitry from the driver circuit LTC3722-1. By using these two components there is a complete galvanic isolation between the secondary side and the driver circuit, resulting in a preserved isolation between the primary and secondary side of the converter.

As mentioned above, the primary driver controls the entire circuit, by utilising a secondary side driver the circuit can follow the primary driver signals but with added protection. The secondary driver receives the gate signal for the two MOSFET sides from the primary driver by using a signal transformer and will turn the correct gate on in accordance with the primary side signals. The Secondary gate driver will amplify the signal by using an external voltage source in order to drive the MOSFETS properly. The secondary gate adds protection in the form of reverse current protection, by measuring the current direction the transistor can turn off thus only allowing current to flow in one direction.

4.2 Converter implementation

The selected components for the converter were determined using the calculated values from sections above. A detailed list containing each component used for the converter in Figure 4.1 can be observed in appendix A.1. The physical circuit is presented in Figure 4.20, where key components are marked with equal notation as in Figure 4.1.

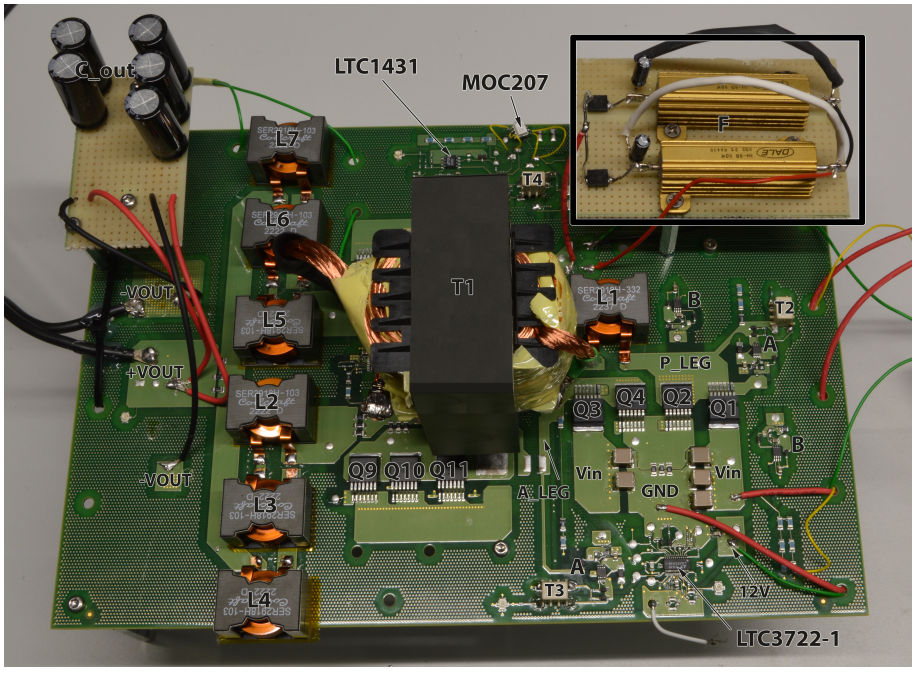

Figure 4.20: Final physical design of the circuit

The heat development for the circuit during operation is of importance, since it indicates where losses are present and the individual component stress. The converter is cooled by a fan and for the primary MOSFETs an extra heatsink is mounted below the PCB. The thermal performance of the circuit board is presented in Figure 4.21 and Figure 4.22 in the form of a heatmap. The output power was limited to 400 W with an output voltage of 40 V, due to the unstable behaviour caused by the current regulation loop. The difference between the figures below is that Fig-

ure 4.21 uses a snubber whilst Figure 4.22 does not use a snubber. Whilst using a snubber, the snubber resistor heated up significantly. The secondary side MOSFET heated up close to 50°C whilst using a snubber. The secondary Transistors did heat up unevenly which indicates an uneven load. The primary side MOSFETs are not evenly loaded either, since some of the transistors increased more in temperature then others during operation.

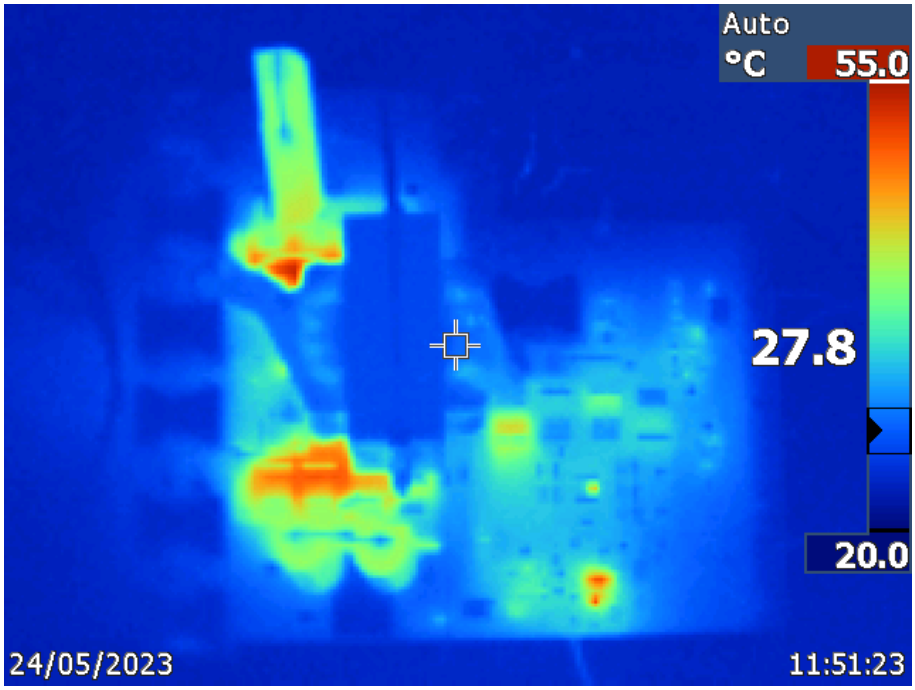

Figure 4.21: Temperature behaviour of the converter with snubber at V_{in}=158 V, V_{out}=40 V and P=400 W

Without a snubber the temperature decreased slightly for the secondary side transistors. Note that the temperature scale has changed between the two scenarios. Without the snubber the same components heat up compared to when the snubber is used.

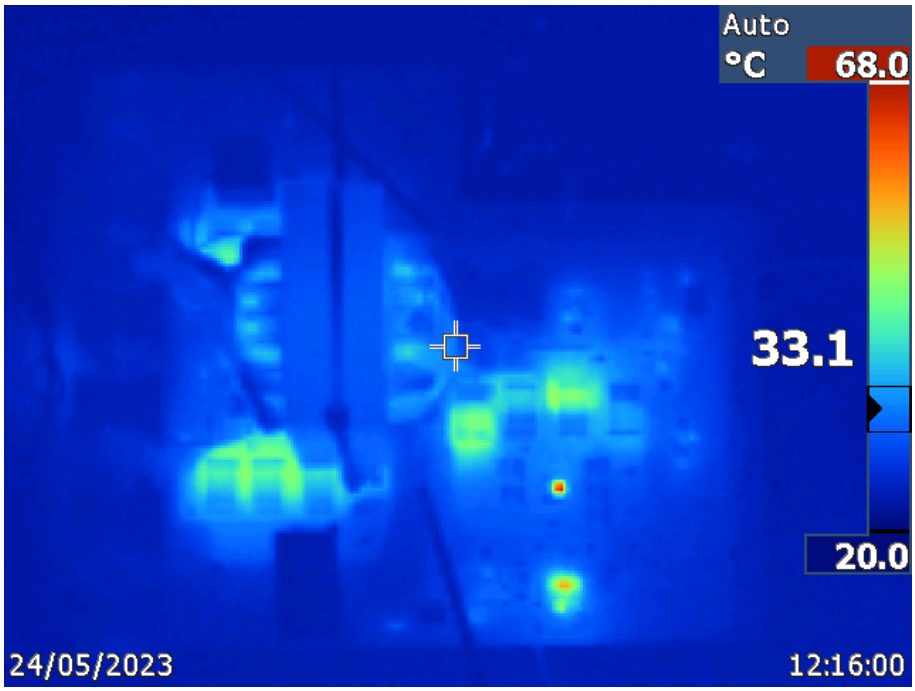

Figure 4.22: Temperature behavior of the converter with snubber at V_{in}=158 V,V_{out}=40 V and P=400 W

4.2.1 Circuitry changes

From the design presented in Figure 4.1 there are parts of the circuitry that did not operate as intended, resulting in certain changes to the circuit design.

4.2.1.1 Snubber design

The snubber was developed with inspiration from a RCD-clamp design. However, during initial testing at low power levels, the snubber did not clamp over-voltages as expected and the thermal development broke the diodes. The snubber circuit was therefore removed from the circuit and instead replaced by an RC snubber according to Figure 2.15.

4.2.1.2 Primary side inductor

Due to the faulty snubber design, there were large oscillations occurring on both sides of the transformer. To solve this, the inductor L1 in Figure 4.1 was removed, resulting in almost no voltage ripple on the primary side of the transformer.

4.2.1.3 Transistor setup for primary side gate drivers

During startup of the converter transistors Q17 and Q19 in Figures 4.2 and 4.3 had a rapid thermal development, reaching approximately 120°C in a few seconds. This resulted in the decision to exclude the BJT design and power the MOSFETs directly with the gate driver circuit LTC4440 from its pin TG through a 4.7 Ω resistor.

4.2.1.4 Optocoupler and error amplifier power

The power supplied to the optocoupler and error amplifier LT1431 in Figure 4.12, was supposed to be supplied from the output through a Zener diode voltage regulator. However, the regulator could not supply enough current for both LT1431 and the optocoupler and the voltage dropped enough during operation to force LT1431 to turn off. The use of an external voltage supply to power the setup was used instead.

4.2.2 Converter performance

In this section the performance of the converter is presented. The performance will be presented in the form of converter efficiency and converter waveforms.

4.2.2.1 Converter efficiency

The power efficiency of the converter was measured at an output voltage of 40 V, in order to not activate the regulating error but still resemble the intended output voltage of 56 V. Table 4.10 displays the efficiency of the circuit with and without snubber circuits for power levels up to 400 W. For both cases, increasing the output power will result in a higher efficiency. Using a snubber decreases the efficiency up to 4.4%. The difference decreases with increased output power.

Table 4.10: Efficiency for the converter with and without snubber with an output voltage of 40 V.

Output power [W]	Efficiency [%] With Snubber	Without snubber
100	77.4	81.8
200	84.0	88.1
300	85.6	88.6
400	86.7	89.3

4.2.2.2 Converter waveforms

The steady state voltage ripple is set to 1% of the total output voltage which corresponds to a peak to peak voltage ripple limit of 1.12 V. The output voltage ripple calculated in (2.21) is based on the total ESR of the output capacitance and ΔI_{Cout} from Table 4.2. With an ESR of 8.8 mΩ, the peak to peak voltage can be determined to $\Delta V_{out} = 38$ mV. The output ripple when using a snubber and without

a snubber can be observed below. In Figure 4.23 and Figure 4.24 there is voltage transients which corresponds to switching in the converter. Using a snubber did not filter out the switching transients. The switching transients resulted in peak to peak voltages of up to 10 V. The peak to peak ripple disregarding the transients could be determined to 1.6 V.

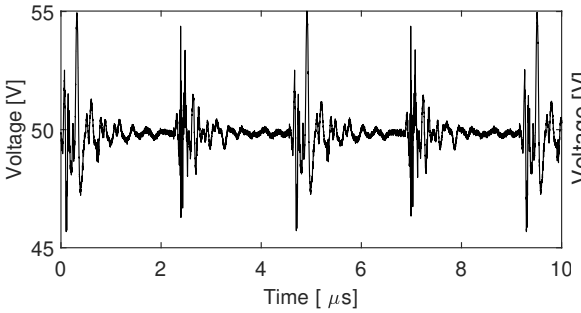

Figure 4.23: Measured output voltage ripple without snubber at V_{out}=50 V, I_{out}=4 A

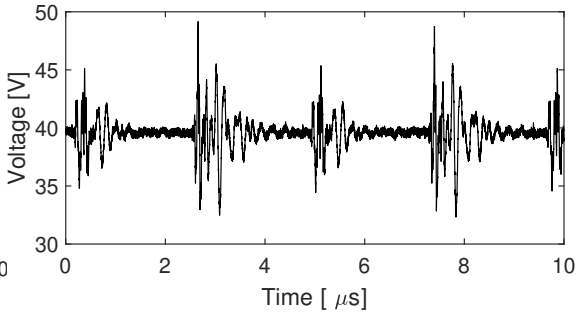

Figure 4.24: Measured output voltage ripple with snubber at V_{out}=40 V, I_{out}=10 A

The simulated output voltage did not contain the switching transients measured on the converter. The simulated peak to peak voltage correlates to the calculated ripple of 38 mV. The simulated voltage ripple is displayed in Figure 4.25.

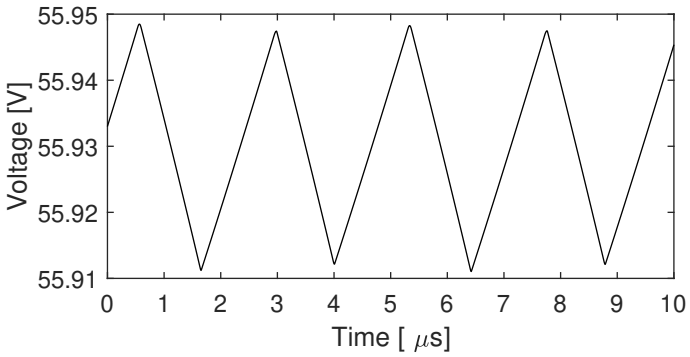

Figure 4.25: Simulated output voltage ripple

The output current of the converter was kept to a steady DC level with negligible ripple since the output capacitors absorbed the current ripple as intended. The level of current ripple in the output capacitor is presented in Figure 4.26. Using a snubber stabilised the current ripple further which is presented in Figure 4.27. However, there are still oscillations occurring at switching which reaches significant magnitudes.

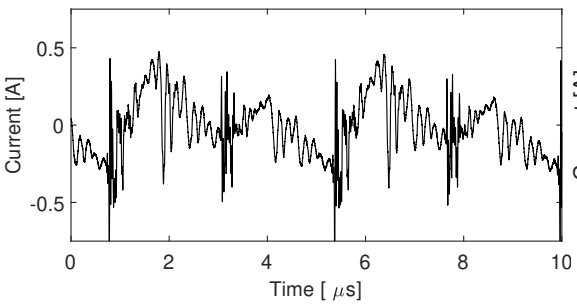

Figure 4.26: Measured current through output capacitor at V_{out}=50 V, I_{out}=4 A. No snubber.

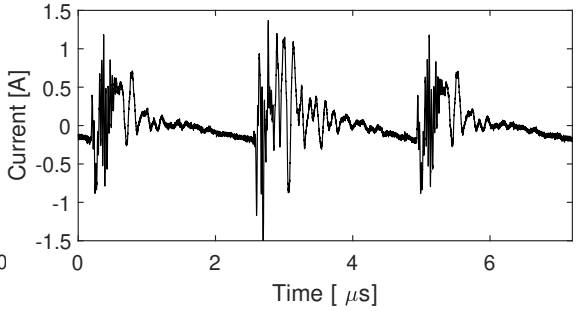

Figure 4.27: Measured current through output capacitor at V_{out}=40 V, I_{out}=10 A. With snubber

The simulated current ripple ΔI_{Cout} in Figure 4.28 equals 4.23 A which is close to the theoretical value calculated in Table 4.2.

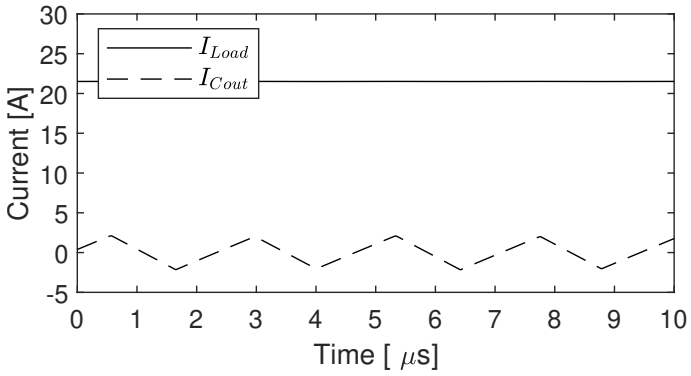

Figure 4.28: Simulated output current through load and capacitor at 1200 W

Furthermore, current waveforms through the output inductors L_{S1} and L_{S2} can be observed in Figure 4.29 and 4.30, where it is observable that the currents are shifted 180 degrees from each other with a ripple amplitude of 6.8 A for the simulated currents, which is slightly less ripple than the calculated value in Table 4.2.

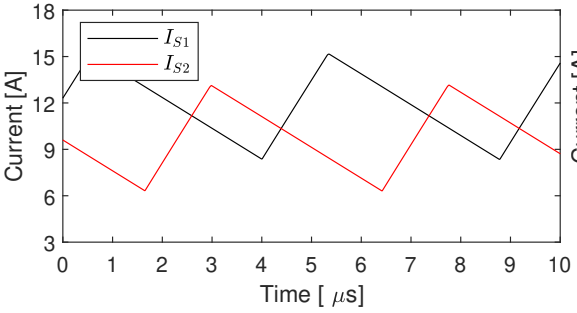

Figure 4.29: Simulated inductor currents at V_{out}=56 V, I_{out}=21.43 A.

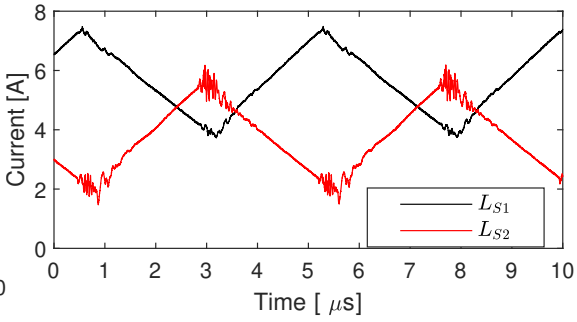

Figure 4.30: Measured inductor currents at V_{out}=40 V, I_{out}=10 A, with snubber.

The transformer voltages of the converter are displayed in Figure 4.31 and the simulated transformer voltages are displayed in Figure 4.32. The transformer voltage is of importance since it shows both the ratio between the primary and secondary voltages as well as distinguishing the duty cycle of the converter. Moreover, it is possible to distinguish if there are oscillations present in the circuit. From the measured and simulated data of the voltages over the transformer there are over-voltage oscillations occurring. The oscillations present peaks at a voltage which is more than twice the amplitude compared to the intended voltage value. The ringing which appears in the real and simulated converter are similar in appearance and occur during switching events. In order to reduce risks of damaging components of the converter, the inductor L1 in Figure 4.1 was removed. This resulted in almost no voltage ripple of the primary side voltage which is why the primary side voltage in Figure 4.31 presents much less oscillations compared to the simulated data in Figure 4.32. The voltage ratio between the primary and secondary side can also be observed to be equal to 2:1 which correlates with the set turn ratio of 18:9 of the transformer.

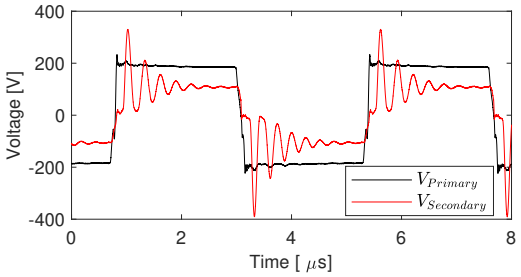

Figure 4.31: Measured transformer voltages at V_{in}=200 V and P_{out}=200 W.

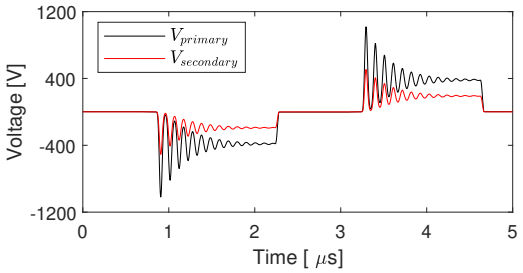

Figure 4.32: Simulated transformer voltages at V_{in}=400 V and P_{out}=1200 W.

Using the RCD snubber decreases the oscillations in the simulations according to Figure 4.34. However, the snubber was faulty and could not be implemented. An alternative solution of an RC snubber according to Figure 2.15 was then implemented instead, which did not work as well as the simulated RCD snubber. To further decrease the oscillations the inductor L_1 in Figure 4.1 could still not be implemented. The voltage waveforms over the real transformer with the RC snubber can be observed in Figure 4.33.

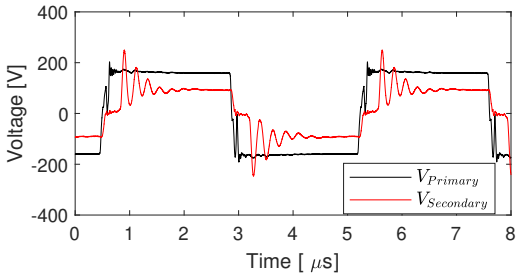

Figure 4.33: Measured transformer voltages with snubber at V_{in}=158 V and P_{out}=400 W.

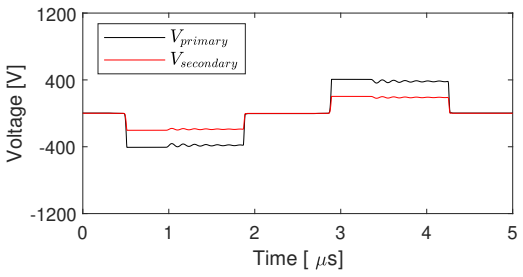

Figure 4.34: Simulated transformer voltages with snubber at V_{in}=400 V and P_{out}=1200 W.

4.2.2.3 Mosfet waveforms

Measuring the current and voltage over the MOSFET it is possible to determine switching losses, if the converter operating with ZVS and if the converter tries to accomplish ZVS. Multiple Switching cycles and the current through the transistor are displayed in Figure 4.35. There is an inrush of current exactly at sequence where the MOSFET is turned on. The measured transistor corresponds to MOSFET Q1 in Figure 4.20 and corresponds to one of the MOSFET that was cooler in temperature during operation, as seen in Figure 4.22.

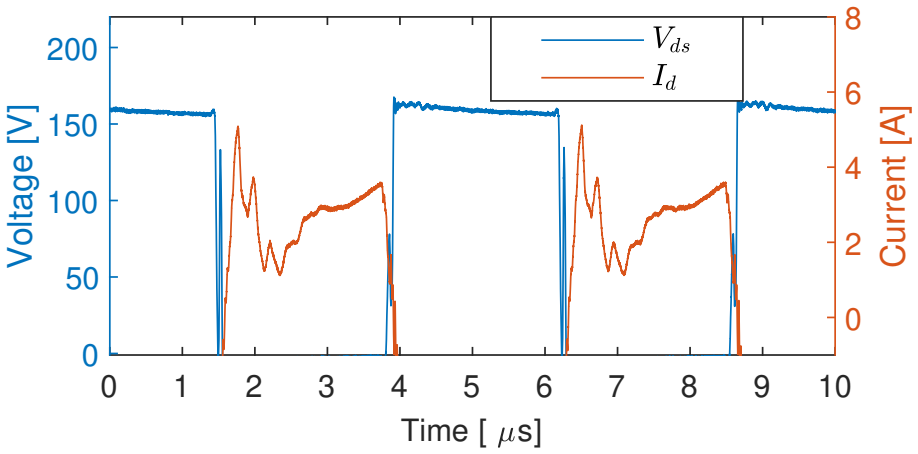

Figure 4.35: Measured Drain source voltage and current through a MOSFET.

During the turn on sequence there is no clear overlap between the current and voltage, as displayed in Figure 4.36. Which in turn means that there is no turn on loss. From the drain source voltage it can be seen that the voltage right before turn on has a oscillating behaviour.

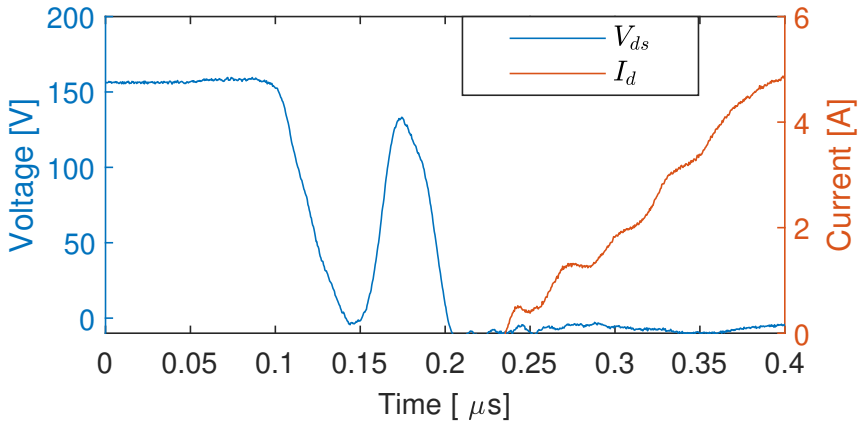

Figure 4.36: Drain source voltage and current when turning on the MOSFET.

At turn off there is a clear intersection between voltage and current and there is thus turn off losses for the MOSFETs. The turn off sequence is presented in Figure 4.37. Using (2.1) the turn off loss can be determined to 1.2 W. The drain source

voltage contains the same oscillating behaviour right before switching as the turn on sequence.

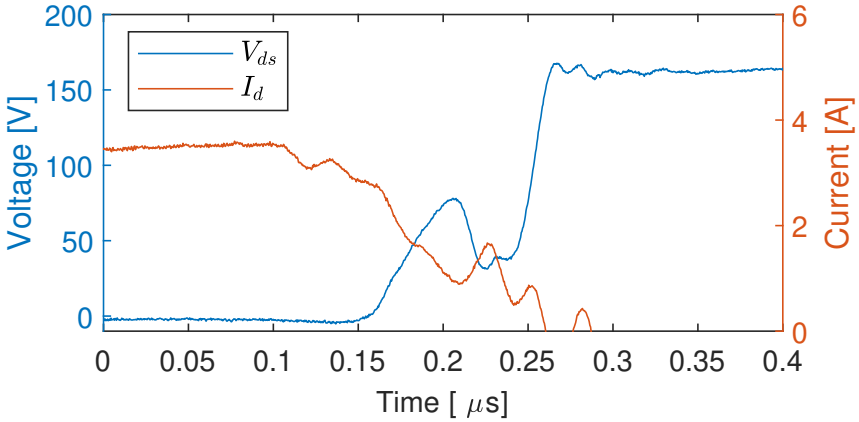

Figure 4.37: Drain source voltage and current when turning off the MOSFET

4.2.2.4 Visualisation of irregular switching pattern

Figure 4.38 displays the transformer voltage, current sense voltage and primary side current at the point where the converter become unstable. The transformer voltage is the topmost figure whilst the current sense is displayed with corresponding voltage in the middle. The primary side current is displayed in the lower figure.

The first period displayed, corresponds to a normal functioning cycle in all three cases. However, the next half cycle becomes unstable where the current sense is triggered by surpassing 0.3 V for a prolonged time and thus terminating the switching cycle. The set lead edge blanking time allows for the measured current sense voltage to surpass 0.3 V for up to 350 ns. From the figure the current sense during switching ripples for more than 350 ns and thus terminates the cycle. Which clearly influences the period time and primary side current. Afterwards, the transformer voltage and the period time then stabilises for one cycle but the primary current and measured current on the current sense does not stabilise the current. This behaviour leaves the converter unstable and limits the power range of the converter. This in turn sets a limit so that the PWM modulation does not work as intended since the regulator acts unstable and a fixed output voltage can not be achieved.

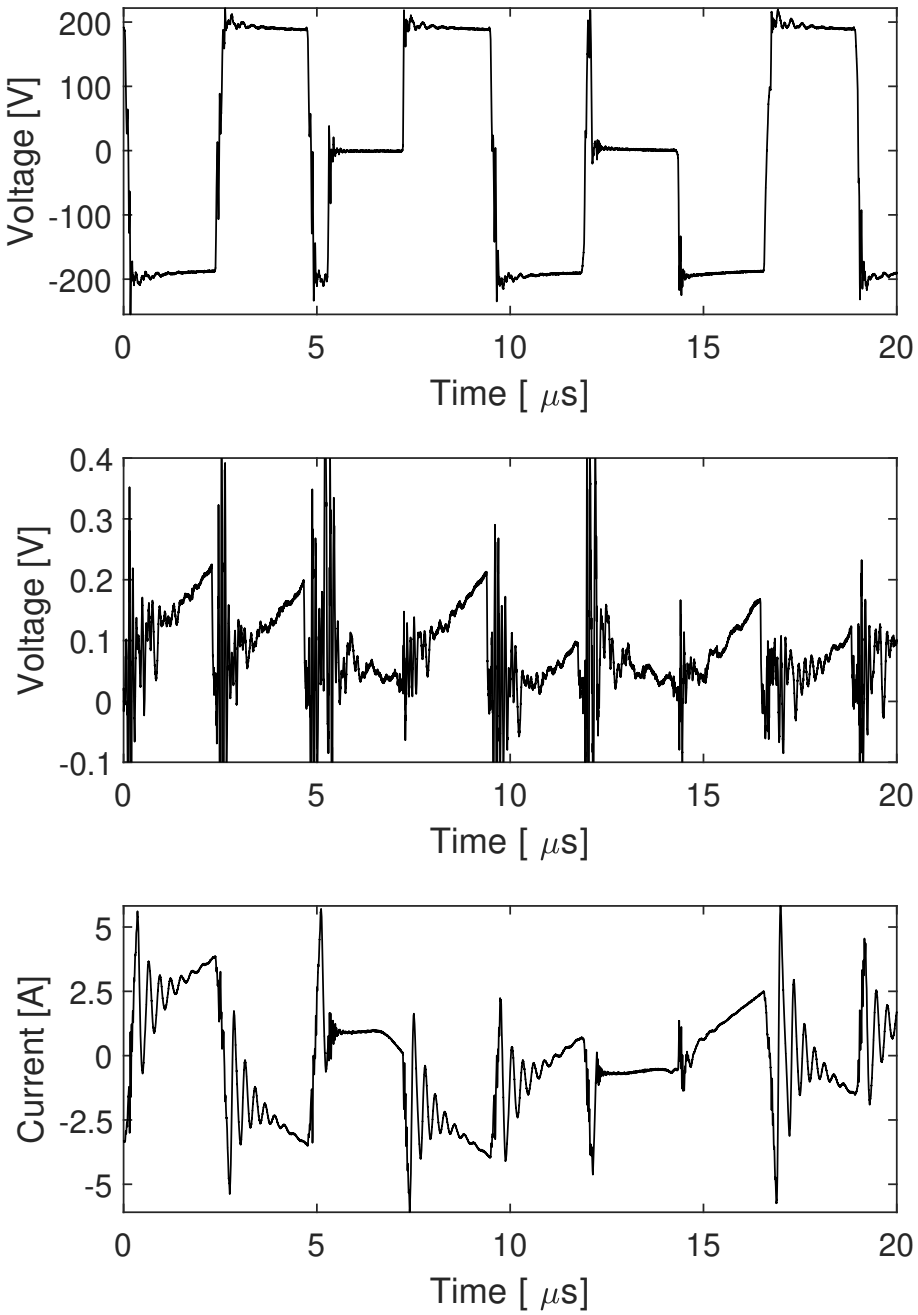

Figure 4.38: visualisation of irregular switching pattern of the converter.

4.3 LLC

The alternative solution for the PSFB converter consisting of an LLC converter which was tested and evaluated. To test the performance of the LLC converter, tests at different loads and input voltages was conducted. the measured efficiency for the tests is summarised in Table 4.11.

Table 4.11: LLC efficiency for different loads and input voltages.

Output power	Input voltage 350 V	375 V	390 V
33% 1650 W	95.55	95.32	95.30
50% 2500 W	95.84	95.94	95.94
75% 3750 W	95.00	95.28	95.49
90% 4500 W	94.00	94.68	94.98

The LLC converter efficiency varies between 94-96% depending on load and input voltage. The converter keeps a steady output voltage of 29.1 V except for 90% load at V_{in} = 350 V where the output voltage decreased to 27 Volts. The converter performs best at 50% load for the entire input voltage range. The efficiency then drops for increased loads.

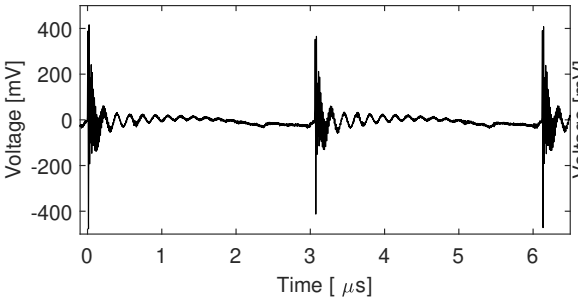

Figure 4.39: LLC output ripple with V_{in}=350 V and P_{out}=1650 W.

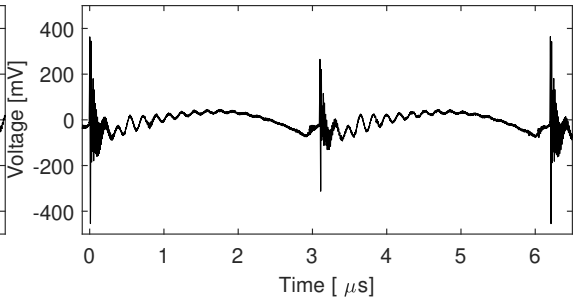

Figure 4.40: LLC output ripple with V_{in}=350 V and P_{out}=4500 W.

The output voltage ripple of the converter is of interest, since sensitive loads cannot operate properly if the voltage is not stable enough. Figure 4.39 and 4.40 displays the voltage ripple when the input voltage is 350 V for different loads. The output ripple has a distinguishable spike during switching which can be seen from the transients in the Figures. The spikes are marginally larger for lower loads. However, the ripple at larger loads becomes more rounded and the peak to peak ripple is larger if the switching transients are not considered.

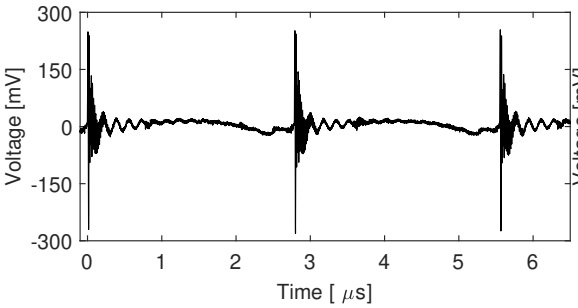

Figure 4.41: LLC output ripple with V_{in}=390 V and P_{out}=1650 W.

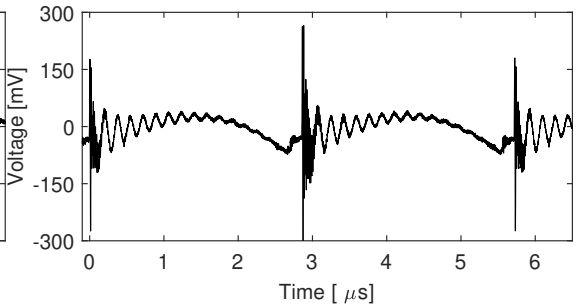

Figure 4.42: LLC output ripple with V_{in}=390 V and P_{out}=4500 W.

With an input voltage of 390 V the same pattern occurs where there are clear switching transients. The same rounding for increased loads is also present as in the case of V_{in}= 350 V. When comparing the different input voltages, it can be seen that a higher input voltage results in lower switching transients. Moreover, it can be seen that the switching frequency is slightly higher for V_{in}= 390 V compared to V_{in}= 350 V.

5

Discussion

5.1 Converter performance

The performance of the converter did not fulfil the design aspirations. The limiting factor is the secondary side oscillations which limit the input voltage range and makes it impossible to test the converter at rated voltages without damaging the converter. The RCD snubber designed to reduce the oscillations was faulty and could not be implemented. Another snubber model, the RC snubber, was implemented to replace the RCD snubber according to Figure 2.15. The RC snubber dampened the oscillations at the cost of decreased efficiency. Using the converter without a snubber limited the input voltage to 220 volts before the feedback started to become unstable. Using a snubber limited the oscillations but caused significant power dissipation in the snubber resistor which increased with increased input voltage. Therefore, the input voltage is still limited to not destroy the RC snubber. In the end, a snubber which limits power losses but still dampens unwanted oscillations is required.

The input voltage range of 350 to 400 Volts is not strictly the upper limit of what this converter could accomplish in theory. From (2.11) the lowest possible input voltage is 224 V whilst the highest voltage is limited by mainly the MOSFETs used and creepage distances. In the case of the primary MOSFETs used the upper limit would likely be around 530 Volts to allow for a 20% margin to the breakdown voltage. This is just theoretical limits and other aspects such as thermal limits and increasing switching or conduction losses would need to be analysed and likely limit the converter performance before the theoretical voltage limit. In a similar manner, the output voltage is adjustable if the converter is to be used for different use cases. With the set input voltage range of 350 to 400 V it is possible to get an output voltage range from 0 to 100 V in theory. In practice the lower and upper range would likely not be practical to accomplish and the efficiency is likely to be degraded if used outside the rated range. To change the output voltage, the feedback system would need to be slightly altered.

As for the ZVS operation of the converter, the ZVS range was reduced since the primary series inductor was removed. From the turn on and turn off figures for the MOSFET, the oscillation occurring right before the switching could be contributed to the driver trying to achieve ZVS, but when it can not achieve ZVS it will just wait a set time limit before forcefully switching. The maximum delay could be decreased

to avoid the oscillation occurring.

5.2 Future improvements

Parts of the PSFB did not work as expected. The use of a PNP and NPN transistor for the primary gate driver resulted in an immediate temperature rise up to 120°C on the PNP transistor and an audible high pitch noise from the transistors. The solution to replace the BJT design with the 4.7 Ω resistor resulted in no apparent faulty operation, but theoretically could have increased the switching delays due to the limited power capabilities of the gate driver LTC4440. The cause of the error of the BJTs could not be determined but is likely due to the internal diodes of the PNP short circuiting the transistor thus overloading it. The use of LTC4440 to charge and discharge the MOSFET gate capacitance worked but resulted in a voltage dip for the turn on signal and a voltage spike for the turn off signal. The spike and dip further increased the delay and could be due to the presence of parasitic Miller capacitances in the MOSFETs. The Miller capacitance increases the turn on and turn off delay but could possibly be negated by a more powerful gate driver which could be accomplished by reducing the gate resistance. However, in the case of LTC4440, decreasing the gate resistance could possibly overload the component.

As mentioned, the RCD snubber design did not work as expected either. The snubber was designed to clamp the voltage over the primary side of the transformer only when the voltage either exceed the input voltage or become negative. During the initial testing, the voltage over the transformer often became larger than the input DC-link, meaning that the diode connected back to the DC link conducted and current could constantly flow through the snubber which at testing resulted in a severe thermal development over the diodes. The snubber constantly conducted current, only limited by the current limit set on the power supply. The RCD snubber design works in principal and in simulations, however when implemented with the physical converter the design did not work.

The over-voltage spikes are likely caused by LC resonance generated by the secondary side MOSFETs and possibly the transformer can be a part of the LC resonance generation. The primary side transistors will not be influenced by these resonances since they are blocked by the transformer which could be seen from studying the drain source voltage over the transistors. A possible improvement is to implement an RC snubber which was the fix used for this project. The solution of using an RC snubber in parallel with the secondary side MOSFETs proved to not be power efficient, ultimately decreases the efficiency of the entire converter by several percent. To ensure stable operation, a new snubber design is required. Further, finding the exact reason for the oscillations in order to remove the problematic components and find a replacement that don't generate the same amount of oscillations will serve towards that purpose of ensuring stable operation.

In order to design a more power-efficient snubber, a solution for the RCD snubber that was designed could be considered. Another solution to reduce the resonances could include the usage of an active snubber, where transistors are actively controlled

to limit resonances and control current flow. The active snubber is generally a solution if efficiency is of importance, but it would increase the complexity of the snubber design. Using an RC snubber will likely not reduce the oscillations enough without decreasing the efficiency significantly. However, it is worth investigating if using the RC snubber together with either an active snubber design or the RCD snubber design could provide an improvement to the converter performance.

The design of the secondary side of the converter can arguably be considered somewhat complex where a simpler approach could've been possible. One alternative solution includes using the output signals for the secondary side from the driver circuit LTC3722-1 through a signal transformer as in the presented solution. But then instead of using a gate driver, the signals coming from the signal transformer could have been sent directly to the gates of the MOSFETs. If the signal is too weak from the driver circuit LTC3722-1 then the signals could be used to send forth another signal, as in the design of the BJT transistors presented in subsection 4.1.2. This type of solution is simple in design and will therefore be limited in its stability and would remove the possibility of current sensing that the gate driver LTC3901 provides.

The use of a planar transformer could decrease copper losses where PCB paths are used instead of wires for the windings. The physical height of the transformer would be decreased, and the overall structure of the transformer would become more stable. As for the functionality the transformer would act in a similar manner and core losses would be similar. However, the use of E-core allows for some more user manoeuvrability where the user can manually remove or add turns to tune the turn ratio of the transformer which is helpful for a prototype.

The Feedback circuit is physically placed far from the driver circuit on the PCB which means that the output from the feedback system had to pass by the high power switching nodes and is thus susceptible to pick up noise. For future iterations of the converter, the placement of the feedback circuit should be reconsidered in order to reduce noise, where the signal paths should be kept away from switching nodes.

Designing a converter is an iterative process. Component selections would likely be changed during the process to further improve converter behaviour. Due to time limits it is not always possible to change components since all components does not fit the PCB layout. An example of this is the primary MOSFETs which are designed to withstand high over-voltages. In hindsight the primary switches did not need to be rated for such a high breakdown voltage and could possibly be replaced and focus more on transistors with lower output capacitance or lower drain source resistance as an example to reduce power losses and/or cost of components.

5.3 Comparison to LLC

The LLC converter performed better in the sense of efficiency and voltage ripple compared to the PSFB. The LLC also outperformed the PSFB by having a wider

power range. The PSFB however shows potential and with tuning of multiple parameters and replacing some components as mentioned above the PSFB can improve efficiency and power demand. It is likely that the LLC will outperform the PSFB in the sense of efficiency since the LLC can accomplish both ZVS and ZCS to decrees switching losses.

Several PSFB converters could be used as an alternative, since it is easier to use in parallel compared to the LLC due to the control scheme of the LLC is more complex and the frequency dependency can cause problems with uneven power delivery. The PSFB can however be set to be out of phase with other converters and the power delivery can be evenly distributed. The LLC will be requiring a more complex control in order to evenly share the current, since small deviations for the resonant tank circuit might influence the gain.

As mentioned above the PSFB can be altered rather easily in order to operate in a wide input and output voltage range using the implemented components in the PSFB. For the LLC it is more difficult to determine the general operating window. Since the input voltage range, output voltage range and power output are coupled to the resonance and also limited by the frequency variation of the LLC controller. If the LLC were to be limited it would likely require redesigning of the resonant tank to alter the power and voltage ranges.

In general, the PSFB would be a more versatile converter which could be adapted into multiple different applications. Whilst an LLC will likely outperform an PSFB in terms of efficiency due to the resonant behaviour allowing soft switching for more specific use cases where the resonant tank can be specifically tuned.

6

Conclusion

This project involved designing, implementing and testing a phase shifted full bridge and comparing it to an LLC converter. A simulation of the converter was developed in LTspice in order to aid in the physical implementation of the converter. With the aid of the simulation software and calculations suitable components was selected and implemented. The functionality of the converter was then verified by testing and measuring the performance of the converter.

The converter could successfully be tested up to 400 W with an efficiency of up to 90 %, but due to an unstable feedback control and oscillations generated on the secondary side of the converter it could not be tested any further during the time span of this project. Comparisons between the simulated converter and the physical converter indicates that the converter acts similar to the intended functions presented by the simulations except for the RCD snubber design.

The LLC converter outperformed the Phase shifted full bridge in every comparison but the PSFB has potential to rival the LLC with further tuning and adjustments. The phase shifted full bridge as a topology is more versatile than a LLC converter since it is more adjustable, has a simpler control and is simpler to connect in parallel with other converters for shared load operation.

For future work some of the shortcomings of this converter could be addressed. Redesigning the snubber circuit and stabilising the malfunctioning feedback loop could stabilise the converter which might enable power ratings of 1200 W of the converter. Another approach to enable the full operation of the converter is by finding the exact reason behind the oscillations, enabling an alternative solution for that specific component.

The design of the gate drivers can be further developed where the primary side gate drivers can include the BJT design once the design error have been located. The secondary side gate driver could also be considered replacing with a driver that provides a simpler design.

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A

Component data for circuit

Type	Component	Manufacturer	Value (R:Ohm, C:F, L:H, D:Vbd[V], T:Np/Ns)	Notation
MOSFET	SCT4026DW7TL	ROHM Semiconductor		Q1-Q4
MOSFET	UF3SC065030B7S	UnitedSiC		Q5-Q12
BJT, NPN	FMMT619TA	Diodes inc		Q13-Q16
BJT, PNP	FMMT718TA	Diodes inc		Q17-Q20
BJT, NPN	MJD340G	Onsemi		Q21
Signal transformer	PA2007NL	Pulse Electronics	1	T2, T3
Signal transformer	PA2008NL	Pulse Electronics	2	T4
Logic circuit	LT1431IS8#TRPBF	Analog Devices		LT1431
Resistor			100	R1-R4, R20, R21
Resistor			4.7	R5-R8
Resistor			2.6 to 7.8	R_load
Resistor			133k	R9, R10
Resistor			1k	R11, R12
Resistor			51k	R13, R14
Resistor			20k	R15, R16
Resistor			12,68k	R17, R18
Resistor			9,2k	R19
Resistor			39k	R22
Resistor			3,3k	R23
Resistor			20m	R24
Resistor			47	R25-R28
Resistor			22	R29
Resistor			2M	R30
Resistor			33k	R31
Resistor			1,97M	R32
Resistor			7,4k	R33
Resistor			270k	R34
Resistor			120k	R35
Resistor			33k	R36
Resistor			8,2k	R37
Resistor			1M	R38
Resistor			68	R39
Resistor			200k	R40
Resistor			750	R41
Resistor			330	R42
Resistor			2,72k	R43
Resistor			82k	R44
Resistor			82k	R45
Resistor			6.33k	R46
Resistor			3838	R47
Resistor			100k	R48
Resistor			60	R49, R50
Inductor	SER2918H-332KL	Coilcraft	3,3u	L1
Inductor	SER2918H-103KL	Coilcraft	10u	L2-L7
Capacitor	UHW2A271MHD	Nichicon	270u	C_out
Capacitor			0,22u	C1-C4
Capacitor			1u	C5-C8
Capacitor			680p	C9
Capacitor			220p	C10
Capacitor			1n	C11
Capacitor			127n	C12
Capacitor			0,1u	C13
Capacitor			220p	C14, C15
Capacitor			0,47u	C16
Capacitor			180p	C17
Capacitor			68n	C18
Capacitor			1u	C19
Capacitor			330p	C20
Capacitor			2,2n	C21, C22
Capacitor			4,7u	C23, C24
Diode	HS1MFL	Taiwan Semiconductor corporation	1k	D1, D2
Diode (Shottky)	BAT54WS-7-F	Diodes inc	30	D3-D14
Diode	S8KC-13	Diodes inc	800	D15, D16
Diode (zener)	MMBZ5240B		10	D17
Diode (zener)	MMBZ5231B		5,1	D18

Figure A.1: Component data for all components present in the built converter

B

Pin layout of driver circuit

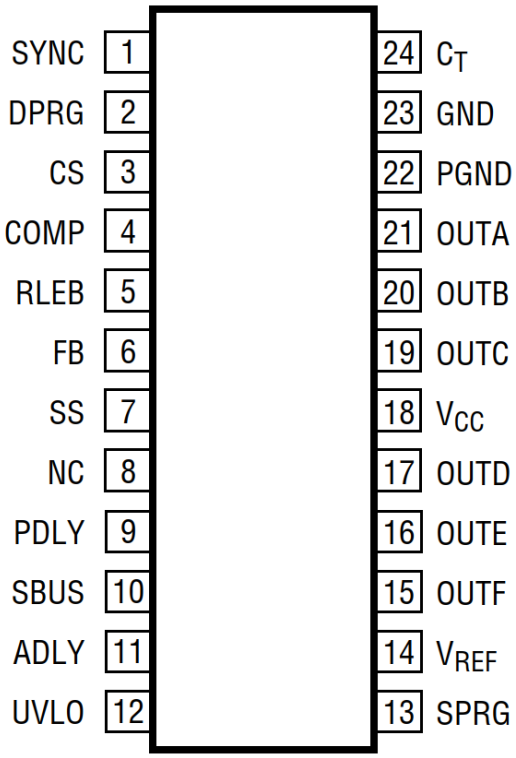

Figure B.1: Pin layout of the driver circuit LTC3722-1 [15]

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