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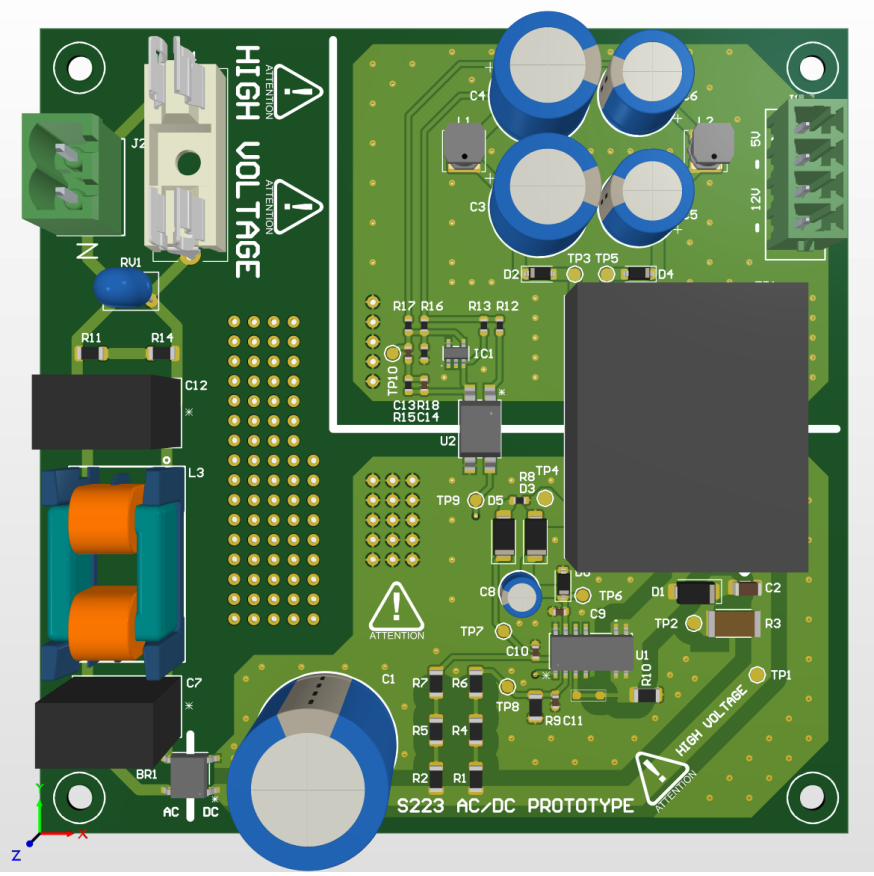

A Multiple Regulated Output Quasi-Resonant Flyback Switched-Mode Power Supply Design

Bachelor's Thesis in Mechatronics

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CHALMERS UNIVERSITY OF TECHNOLOGY
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Cover: Simulated 3D model showing a printed circuit board assembly of a switched-mode power supply constructed in Altium Designer.

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Abstract

The expanding use of utility grid powered appliances gives rise to the need for efficient switched-mode power supply (SMPS) designs. Ready-made modules exist, but designs with discrete components may prove a viable alternative and improve logistical robustness by introducing component redundancies. In addition, the increased flexibility may enable the same SMPS design to be modified for different products and uses.

The objective of this project was to design and construct an off-line SMPS prototype with multiple power outputs. It uses a quasi-resonant (QR) integrated circuit (IC) controller together with discrete components. The SMPS is designed to meet the requirements of an existing product, but also to be a viable platform to further improve and modify upon.

By using electronic design automation (ECAD) software, a schematic capture was created of an electronic circuit. A printed circuit board layout was designed and manufactured according to the schematic capture. The used components were sourced and a printed circuit board assembly (PCBA) was produced.

The PCBA was evaluated using industry-standard testing methodologies. While the output performance measured was modest, several potential reasons for this were identified. Hence, the produced prototype shows promising possibilities for future development.

Keywords: quasi, resonant, switched-mode, power, supply, design, pcb, multiple, regulated, output.

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Joachim Löfwander, Gothenburg, June 2022

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

AC	Alternating Current
BOM	Bill of Materials
DC	Direct Current
DCM	Discontinous Conduction Mode
DVT	Design Validation Test
ECAD	Electronic Design Automation
EVT	Engineering Validation Test
FB	Feedback
IC	Integrated Circuit
MVT	Manufacturing Validation Test
OVP	Over voltage protection
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
QR	Quasi-Resonant
RMS	Root Mean Square
SMPS	Switched-Mode Power Supply
VAC	AC Voltage
VDC	DC Voltage

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1
Introduction

1.1 Background

Today Martinsson Elektronik, a company that develops custom display solutions for the industry, uses ready-made modules for converting 230VAC to required DC voltages in their printed circuit board assembly (PCBA) products. The modules are complete encapsulated switched-mode power supplies (SMPS) as seen in Fig. 1.1 below.

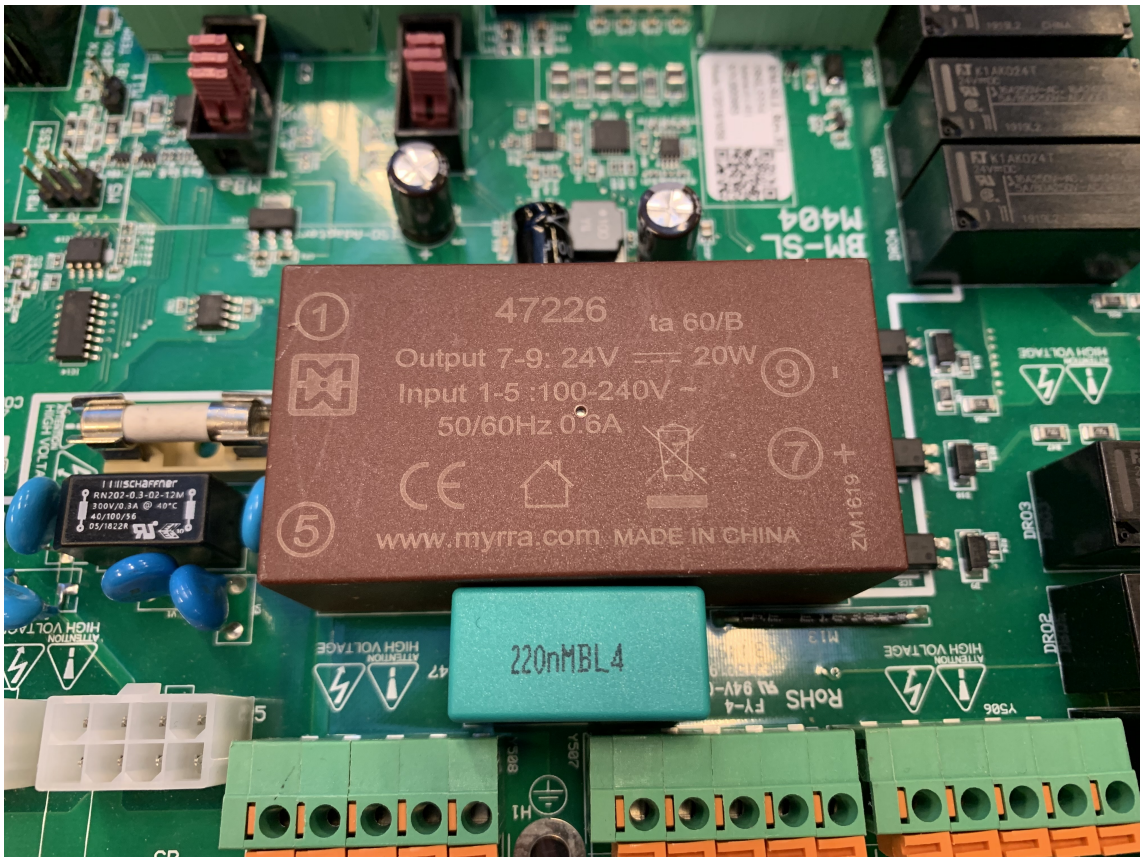

Figure 1.1: Encapsulated AC/DC SMPS (red case) mounted on a Martinsson PCBA.

The red case visible is one of the models used. It is of a single-output design that converts 230VAC to a 24VDC rail.

The products that Martinsson Elektronik develops typically require several dif-

ferent voltages on the PCBs simultaneously. Generally, these voltages are 24VDC, 12VDC, 5VDC, and 3.3VDC. Today these voltages are created from the 24VDC rail by individual voltage regulators.

More specifically, the separate regulators are used in steps to convert 24VDC to 12VDC, 12VDC to 5VDC, and 5VDC to 3.3VDC. Each converter used to step down the voltage introduces losses, depending on the voltage drop required, the current draw of the specific output rail, and the efficiency of the regulator used [1]. Typically, the power losses are lower in switched-mode converters than in linear ones, hence switched ones are often used when the voltage drops or current requirements are significant [2].

The extra regulators required today also increase component count. This may lead to higher costs for the product and higher design and manufacturing complexity.

A multiple output SMPS that could convert and deliver multiple required voltage rails directly from the 230VAC source, without the need for external converters applied on the voltage rails afterwards, may therefore be a viable improvement over the current solution.

In addition to possibly increasing the efficiency and reducing the need for post-regulation, an SMPS constructed by discrete components may also increase the logistical robustness. Instead of the single producer of the ready-made module, several manufacturers may exist for each component or at least equivalent devices. Hence, redundancy may be gained by choosing a discrete solution.

1.2 Aim

The degree project aims to design and manufacture a prototype of an SMPS that converts 230VAC to desired DC voltages. In Fig. 1.2 the proposed development stages of the product are illustrated.

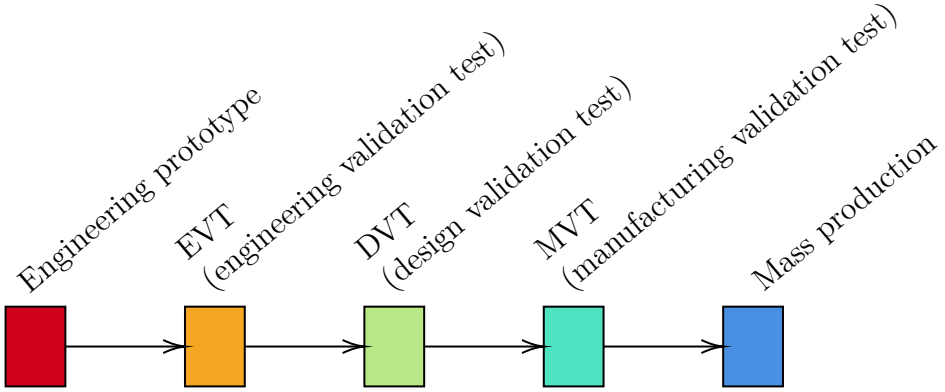

Figure 1.2: The intended stages of the product development. The first two stages are relevant for this project.

The first two stages are included in this project, i.e. the engineering prototype and an early engineering validation test (EVT). In the first stage, the prototype is created, while in the EVT phase the functionality is validated and any critical problems blocking the following stages are identified.

The SMPS will be created with a Quasi-Resonant (QR) controller IC in addition to discrete components. It will be designed to meet the requirements of an existing Martinsson product named M404 BM-SL. This includes supplying required currents and voltages.

The primary aim of the degree project is to fulfil the following objectives:

- An engineering prototype of an SMPS
- The SMPS consists of off-the-shelves components.
- Both a schematic capture and PCB layout are to be created.
- Conforms to the requirements of M404 BM-SL.
- If practical a multiple output SMPS.
- Conduct EVT of the prototype.

1.3 Scope

The design will be optimized for the electrical requirements of M404 BM-SL. It should deliver at least one of the required voltage rails. Choices that are not specified by these requirements are considered as free variables and will be determined on a most-suitable basis, if possible they will be chosen to match the existing encapsulated module used today.

As this project only includes the first two stages of the product development, stress, environmental or manufacturing requirements will not be considered. This is included in the later stages Design Validation Test (DVT) and Manufacturing Validation Test (MVT).

Neither will any consideration be taken for electrical safety or electromagnetic interference (EMI), radiated and conducted.

Only QR controllers will be evaluated and used for the primary conversion between the unregulated 230VAC input and the secondary regulated DC outputs. The controllers will be evaluated on a subjective basis.

The SMPS will be constructed with discrete components. This excludes using any ready-made SMPS solutions on the market. Also, the design will only use off-the-shelf components, i.e. no bespoke components will be used in the project.

The initial test plan to verify the prototype will be based upon standard practices applied by the industry when evaluating SMPS.

1.4 Thesis outline

In chapter 2 some required theory is introduced, while in chapter 3 the applied methods in the project are described.

In chapter 4 the design process of the prototype is presented. Chapter 5 includes the bring-up of the prototype and in chapter 6 the performance of the SMPS is measured.

Finally, in chapter 7, a conclusion of the project is given.

2
Theory

2.1 Introduction to switching converters

The basic function of an SMPS is power processing. In other words, it processes the power input into a modified power output [3].

A linear converter regulates the output voltage by introducing a voltage drop over resistive elements or linear-mode semiconductor devices [1],[3]. In contrast, the switching converter of an SMPS applies the unrestricted voltage in short intervals to a magnetic component, where the energy is stored. This is done by a semiconductor device that either operates in its saturation mode with a low voltage drop, or in its off state with ideally no current flowing through it [3]. The gain of this is that the resulting power dissipation is low compared to a linear converter, increasing the efficiency [3], [1].

Though the main drawback of SMPS is in fact the switching element, as it introduces undesirable harmonics of the switching frequency which is output on both the power input and the power output [3]. Additionally, radiated electromagnetic interference (EMI) is produced [1]. This adds to the importance of adequate filtering and electrical design.

2.2 The buck converter

One of the basic DC-DC converters is the buck converter. It produces a voltage output with lower amplitude than the input [2]. An illustration of the fundamental components of the converter is depicted in Fig. 2.1.

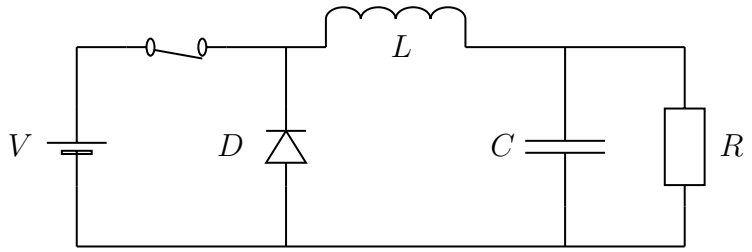

Figure 2.1: The fundamentals of a buck converter.

Here, the magnetic element used is an inductor. The current into the inductor increases linearly during each applied voltage pulse and the energy is stored in the resulting magnetic field [1].

Between each pulse, the magnetic field decays while supplying the output current [2]. The diode in the illustration becomes forward biased due to the counter-electromotive force, i.e. voltage, introduced across the inductor, creating a current loop [2]. In effect, it also limits the amplitude of the resulting kickback voltage. During this phase, all or parts of the stored energy are transferred out of the inductor.

By controlling the frequency and length of the current pulses, the output voltage from the buck converter may be determined [1]. Therefore it typically operates by comparing the output voltage via feedback to a reference voltage and adjusting the pulses accordingly.

The role of the magnetic component in the buck converter is to filter the applied voltage waveform into a DC voltage [3]. This is typically done in union with a capacitive storage element connected afterwards. In essence, creating a low-pass filter [3], [2].

2.3 The boost converter

Another DC-DC converter topology is the boost converter. It is capable of producing a DC voltage output with higher amplitude than the input [3]. The essential circuit is illustrated in Fig. 2.2.

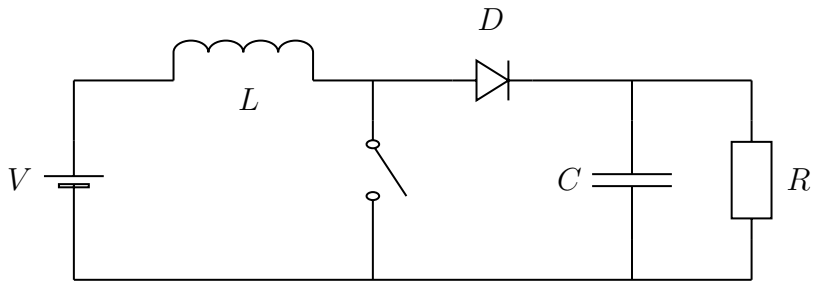

Figure 2.2: The fundamentals of a boost converter.

The circuit operation can be divided into two phases. During the first phase, the switching element is in its conducting state, and a current loop is created. The current flows through the inductor and the switching element into ground [3]. This current charges the magnetic field in the inductor while the capacitor provides the energy for the output. The role of the diode is to block the capacitor from discharging through the switching element.

In the next phase, the switching element is in its off state. Now, the inductor's magnetic field decays and the counter-electromotive force causes the diode to be forward biased. The stored inductor energy supplies the output power while charging the capacitor [3].

2.4 The buck-boost converter

The buck-boost converter is essentially a cascaded connection of a buck and boost converter [3]. As a result of this, depending on the duty cycle applied to the switching element, the output voltage can either be lower or larger than the input voltage. A simplified circuit is presented in Fig. 2.3.

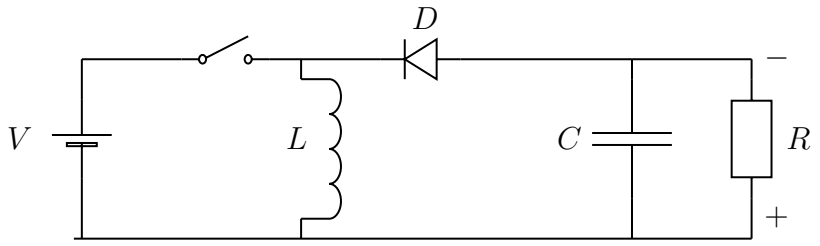

Figure 2.3: The fundamentals of a buck-boost converter. Note the polarity of the output.

The input provides energy to the inductor when the switch is closed, which is stored in the produced magnetic field [2]. When the switch is closed the diode is reverse biased.

During the next phase, when the switch is open, the energy stored is transferred to the output [2], [3]. Consequently, the diode is now forward biased.

The resulting output-to-input voltage ratio is a product of both the cascaded converters' conversion ratios [2].

2.5 The flyback converter

The flyback converter is essentially a derivation of a buck-boost converter with added isolation via a transformer [3]. This galvanic isolation is often a necessity in off-line SMPS, i.e. when supplied from the mains electricity [1].

This transformer does not operate as an ideal transformer, where current flows through all windings simultaneously. Instead, it acts as a two-winding inductor [3], where energy is stored in the magnetizing inductance of primary winding and is then extracted via the secondary winding during the next switching phase. The fundamental construction is presented in Fig. 2.4.

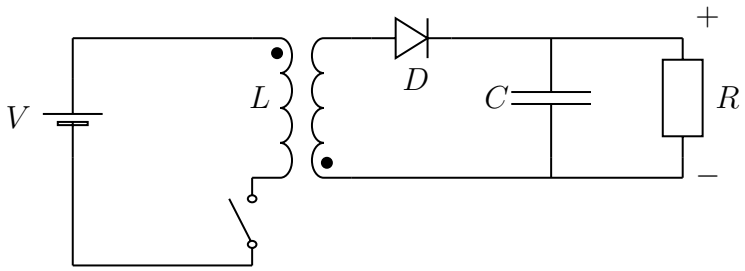

Figure 2.4: The fundamentals of a flyback converter. Note the transformer winding polarities.

The function of the diode is essentially the same as in a buck-boost converter. The important detail is the polarities of the transformer windings. When the switching element, generally a MOSFET, conducts the current the secondary side diode is reverse-biased [3]. Thus, the energy gets stored in the magnetizing inductance.

When the MOSFET changes to its off state, the resulting counter-electromotive force of the inductance causes the secondary side diode to be forward biased. This leads to the stored energy being extracted to the output [3].

The use of a transformer allows for the scaling of the voltage and current output of the secondary winding according to the turns ratio between the windings [3].

2.6 Additional building blocks of an SMPS

2.6.1 Input filter

Utility grid filtering is done by an input filter, generally constructed by capacitors and a series-coupled inductor [1]. Two classes of the capacitors rated for mains electricity exist [1]. They are "X" capacitors and "Y" capacitors. "X" capacitors are used to connect live and neutral traces, where if the capacitor were to fail, it would not result in a shock hazard [1]. In contrast, "Y" capacitors are used if the failure could result in this danger. Hence, they are typically used bypassing ac lines to ground.

The input filter is especially important in a flyback SMPS due to the high peak currents and sharp switching edges present [4].

A discharge resistor is typically used across the input filtering capacitors. Its purpose is to eliminate the risk of voltages present across the input terminals when the device is switched off or disconnected [1].

2.6.2 Rectifier diodes

2.6.2.1 Line-frequency rectifier diodes

Line-frequency rectifier diodes, generally diodes with a current rating above one ampere [5], are used for rectifying the utility grid AC to DC [2].

2.6.2.2 High-frequency rectifier diodes

The diodes used for rectifying the outputs from a high-frequency transformer demand higher capabilities, such as shorter recovery time [5], due to the higher switching frequencies of an SMPS. These frequencies are typically around 20KHz−1MHz, a significant increase from the typical utility grid frequency.

Therefore Schottky-barrier diodes are often used in high-frequency applications, as they have significantly lower recovery times due to negligible storage charges [3]. A larger storage charge affects the transition time between the conducting and non-conducting states negatively [5].

Additionally, they have a lower forward voltage drop. An advantage for efficiency [3]. Still, drawbacks exist and one is lower breakdown voltage capability.

2.6.3 Storage capacitors

Storage capacitors are generally used after rectifier diodes to filter out the ripple created by rectifying AC voltages [2], [1]. Additionally, as a general rule, the ripple current capabilities of the capacitors should be distinctively larger than the calculated worst ripple currents of the rectified DC output [1].

2.6.4 Snubber circuit

Snubber circuits are used to modify and limit switching waveforms, both voltages and currents [2]. They are used when the switching operation of an SMPS introduces stresses on an electronic device that are beyond its rated capabilities.

2.6.5 Switching controller

As both the input power to an SMPS and the applied output load may vary, it is not possible to set a fixed duty cycle [3]. By doing so the produced output voltage would doubtless fall outside of the specified range of the SMPS.

Instead, a controller is used that automatically regulates the duty cycle accordingly [3]. This is possible by introducing a feedback circuit that constantly monitors the output voltage and feeds it back to the controller.

2.6.6 Output filter

The main objective of an SMPS output filter is to eliminate the switching ripple current produced before it is seen by the applied load [3]. In other words, the impedance of the filter at the switching frequency should be lower than the impedance of the load [3]. This will cause the bulk of the switching ripple current to flow through the filter instead of the load.

2.7 Discontinuous Conduction Mode

During discontinuous conduction mode (DCM), all of the energy stored in the transformer's primary inductance are released to the secondary side [6]. This is one of the operation modes of DC-DC converters, the other being Continuous Conduction Mode (CCM), where there is still energy left in the magnetic field over the cycles.

2.8 Quasi-Resonant switching

A QR converter is a converter which switches at a specific stage in the operation of the SMPS [4].

When all the energy has been transferred out of the magnetic element and the core has been demagnetized, resonant ringing occurs in the primary side winding. This ringing is caused by the primary inductance in conjunction with the circuit's parasitic capacitance [4], [7].

The QR controller IC detects the ringing and uses it as an indication to transition to the next phase of the switching operation [4]. Due to this, QR converters require the SMPS to operate in DCM [3].

The transition occurs at the lowest point of the primary side voltage, also the MOSFET's drain-source voltage [4], [7]. This is also known as zero-voltage switching (ZVS) [3].

The result is decreased losses due to the MOSFET's capacitance and thus an increased total efficiency of the SMPS. It may also improve the EMI performance [3].

2.9 Instruments used in the project

The instruments used during the testing phase are presented in Table 2.1.

Table 2.1: Used instruments

Instrument	Model	Function
Oscilloscope	Keysight MSO-X 2004A	Voltage and current time domain measurements
Current probe	Chauvin Arnoux E3N	Oscilloscope current measurements
X10 probe	Keysight N2862B	Oscilloscope voltage measurements
X1 probe	-	Low level oscilloscope voltage measurements
Differential probe	Micsig DP10007	Isolated high voltage oscilloscope measurements
Multimeter 1	Fluke 289	Voltage, current and resistance measurements
Multimeter 2	Fluke 179	Voltage, current and resistance measurements
Multimeter 3	EEVBlog 121GW	Voltage, current and resistance measurements
Electronic load	Siglent SDL1020X-E	Constant current, resistance or voltage loading
Isolation transformer	Breve-Tufvassons PFS250	AC voltage isolation
Variable transformer	Ravistat P1	Adjustable AC voltage supply

To conduct low-level ripple measurements with the oscilloscope an X1 probe may be required, due to the attenuation of an X10 probe. A An X10 probe attenuates by a factor of ten, which may cause the signals of interest to disappear into the noise floor of the oscilloscope [8]. An X1 probes input to output ratio is $1 : 1$.

2.10 Efficiency measurements

The efficiency rating of a power supply is the output power divided by the true input power [9]. The efficiency is calculated as

$$\eta_e = \frac{P_{out}}{P_{in_{true}}} \tag{2.1}$$

To calculate the true input power (2.2) is used, where both the input RMS voltage and the input RMS current are in phase [9].

$$P_{in_{true}} = V_{rms_{inphase}} \cdot I_{rms_{inphase}} \tag{2.2}$$

The measurements should be done with at least two different loads applied to the SMPS [9], with one of the load settings being the maximum specified load rating. Furthermore, the electronic load should be operated in constant current mode for a constant voltage SMPS.

2.11 Output ripple and switching transients measurements

Output ripple and switching transients are unwanted AC components present on the regulated DC output [9], [8]. More specifically, the output ripple is a residue of the input AC voltage that is not successfully filtered out.

In contrast, the switching transients are produced at the time of the transition between the states of the switch [8]. They are short duration spikes superimposed on the DC output [9]. Furthermore, these oscillations are of higher frequency but of lower energy composition and place higher demands on the testing methodology [8].

Fig. 2.5 demonstrates the differences between output ripple and switching transients.

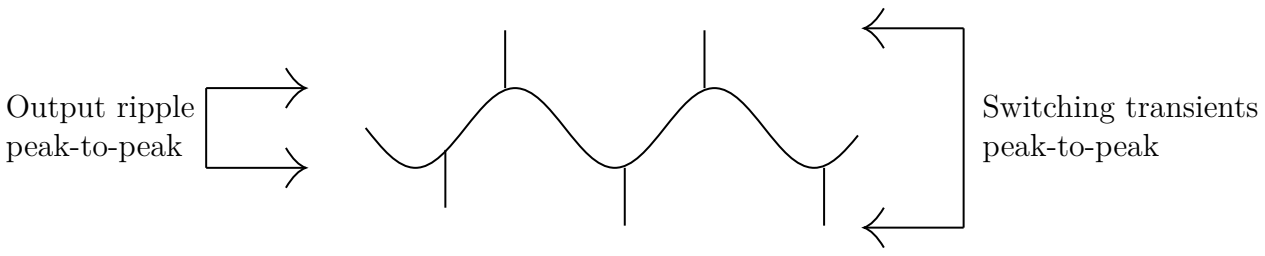

Figure 2.5: Output ripple and switching transients.

Depicted in the figure is the voltage ripple as a sinusoidal waveform while switching transients of significantly higher frequency and imposed upon the ripple waveform.

The main contributors to the output ripple are the magnetic element, i.e. the transformer in a flyback SMPS, and the output filter capacitor [8].

The measurements are typically done with a specified bandwidth range of 20Hz−20MHz, and preferably both RMS or peak-to-peak values are measured. The reason is that individually they will not show the total characteristics of the deviations from the average voltage output [9].

3
Methods

The project was divided into several phases. These phases are demonstrated in Table 3.1.

Table 3.1: Project phases

Phase	Objective
1. Pre-study	Theory study of the subject
2. Specification	Specify the requirements of the SMPS
3. Design	Schematic and PCB design of the SMPS
4. Bring-up	Power up and debugging of the SMPS
5. Verification	Evaluate the SMPS performance

3.1 Pre-study

As no courses on power electronics are included in the mechatronics curriculum, a pre-study of the field was required. The books [2], [3], [1], [5] as well as several application notes gave a primer on the subject.

3.2 Specification

The required capabilities of the SMPS were recognized. These were based on the voltage and current requirements of M404 BM-SL, a Martinsson Elektronik product, which are listed in Table 4.1.

3.3 Design

A circuit, schematic capture and a PCB were designed based on the typical application circuits for the chosen controller IC.

The component specifications were determined based on the calculations provided in the design guide for the controller, as well as relevant rules found in [10] and [11], whichever provided the largest safety margins.

3.4 Bring-up

During this phase, the prototype was brought up into working order, and any identified faults were fixed.

Malfunctions displayed by the prototype were confined to either separate circuit blocks or individual components. This was accomplished by temporary removing traces and components, and by powering isolated circuit blocks individually while measuring with multimeters and oscilloscopes.

When necessary specifications were recalculated and components replaced.

3.5 Verification

To verify and characterize the SMPS protoype's performance, measurements based on [9] and [8] were conducted. More specifically the tests were aimed to measure the efficiency and output ripple and switching transients at different applied constant current loads.

4
Design

The individual steps in this chapter are explained in the same sequence as they were taken. The equations used are based on the ones found in [12], but with different values applied.

4.1 SMPS specification

The SMPS specification is presented in Table 4.1.

Table 4.1: SMPS specification

Paramenter	Symbol	Value
Nominal AC voltage input	$V_{AC_{nom}}$	$230V_{RMS}$
AC voltage input frequency	f_{AC}	50Hz
Maximum total output power	$P_{out_{max}}$	$20W$
Minimum total output power	$P_{out_{min}}$	$5W$
Desired output 1 voltage	V_{out_1}	$5V$
Desired output 2 voltage	V_{out_2}	$12V$
Desired output 1 current	I_{out_1}	$1,5A$
Desired output 2 current	I_{out_2}	$1A$

4.2 Topology and controller evaluation

Due to the component shortage crisis, the selection process complexity was increased. Controller ICs found in the literature on the subject often had lead times of years, presumably because they already were in use in many existing designs. Therefore, the first criterion was that it had to be in stock and orderable.

The second criterion is that it needed to have enough documentation to simplify the design process, as the project was limited by time constraints.

With these two criteria, a selection of controller ICs were evaluated. Through a subjective selection process, a final controller IC was selected. The controller ICE5QR1680BG from Infineon Technologies was chosen as it was in stock, had a thorough design guideline documentation and showed promising performance, such as efficiency and output regulation.

4.3 Component calculations

To calculate the conditions for the components, input parameters in Table 4.2 were used. The minimum AC voltage input was set to 75% of the nominal voltage input of $230V$, and the maximum to 125%.

Table 4.2: SMPS input parameters

Paramenter	Symbol	Value
Specified efficiency	η_e	$0,85$ [12]
Specified power factor	$\cos\varphi$	$0,60$ [12]
Nominal AC voltage input	-	$230V_{RMS}$
Maximum AC voltage input	$V_{AC_{max}}$	$287,50V_{RMS}$
Minimum AC voltage input	$V_{AC_{min}}$	$172,50V_{RMS}$

4.3.1 Input diode bridge rectifier

The maximum input power was calculated as

$$\begin{aligned} P_{in_{max}} &= \frac{P_{out_{max}}}{\eta_e} \\ &= 23,53W \end{aligned} \tag{4.1}$$

With the maximum input power, the maximum input current, $I_{AC_{RMS}}$, can be calculated as

$$\begin{aligned} I_{AC_{RMS}} &= \frac{P_{in_{max}}}{V_{AC_{min}} \cdot \cos\varphi} \\ &= 0,23A \end{aligned} \tag{4.2}$$

4.3.2 Rectifier smoothing capacitor

The requirements for the smoothing capacitor are calculated in the following section.

The maximum peak DC voltage after the rectifier bridge is calculated with (4.3). This calculation does not take the forward voltage drop of a diode into consideration.

$$\begin{aligned} V_{DC_{max_{Pk}}} &= V_{AC_{max}} \cdot \sqrt{2} \\ &= 406,57V \end{aligned} \tag{4.3}$$

The minimum peak DC voltage is calculated as

$$\begin{aligned} V_{DC_{min_{Pk}}} &= V_{AC_{min}} \cdot \sqrt{2} \\ &= 243,95V \end{aligned} \tag{4.4}$$

The minimum DC voltage at the high-voltage DC bus is calculated with (4.5). An arbitrary ripple voltage of 30V was chosen as $V_{DC_{ripple}}$.

$$\begin{aligned} V_{DC_{min}} &= V_{DC_{min_{Pk}}} - V_{DC_{ripple}} \\ &= 213,95V \end{aligned} \tag{4.5}$$

The discharging time of the capacitor is calculated as

$$\begin{aligned} T_D &= \frac{1}{4 \cdot f_{AC}} \cdot \left(1 + \frac{\sin^{-1}\left(\frac{V_{DC_{min}}}{V_{DC_{min_{Pk}}}}\right)}{90} \right) \\ &= 8,41ms \end{aligned} \tag{4.6}$$

The required energy at the discharging time can then be calculated as

$$\begin{aligned} E_{in} &= P_{in_{max}} \cdot T_D \\ &= 0.198J \end{aligned} \tag{4.7}$$

With this the capacitance of the rectifier smoothing capacitor can be calculated as

$$\begin{aligned} C_{in} &= \frac{2 \cdot E_{in}}{V^2_{DC_{min_{Pk}}} - V^2_{DC_{min}}} \\ &= 28,83\mu F \end{aligned} \tag{4.8}$$

The capacitance of the capacitor was rounded up to a commonly available value of $33\mu F$, while the voltage rating was chosen to $500V$ to allow for some safety margins over $V_{DC_{max_{Pk}}}$.

The minimum DC voltage present on the bus with the chosen capacitance was then calculated as

$$\begin{aligned} V_{DC_{mincap}} &= \sqrt{V^2_{DC_{min_{Pk}}} - \frac{2 \cdot W_{in}}{33\mu F}} \\ &= 217,97V \end{aligned} \tag{4.9}$$

This means that the capacitance is enough to not let the voltage decrease below the previously calculated $V_{DC_{min}}$ with the maximum power draw of $P_{in_{max}}$.

4.3.3 Transformer

Initial parameters for use in the transformer calculations are shown in Table 4.3.

Table 4.3: Transformer input parameters

Parameter	Value
Desired auxiliary voltage, V_{aux}	$14V$ [12]
Desired reflection voltage, V_r	$90V$ [12]
Built-in MOSFET drain-source capacitance, C_{ds}	$8pF$ [13]
Max drain-source voltage, $V_{DS_{max}}$	$600V$ [12]
Switching frequency at minimum voltage input and maxmimum power output, f_s	55kHz [12]
Maximum flux density, B_{max}	$300mT$ [12]
Core area, A_e	$32mm^2$ [12]
Leakage inductance, L_{leak}	1% of primary inductance [12]
Rectifier diode voltage drop, $V_{f_{diode}}$	$0,3V$ [12]

The relation between the primary side voltage V_p, secondary side voltage V_s, as well as the turns ratio n_{ratio} between the primary side (N_p) and the secondary side (N_s), are shown as

$$\begin{aligned} \frac{N_p}{N_s} &= \frac{V_p}{V_s} \\ &= \eta_{ratio} \end{aligned} \tag{4.10}$$

The maximal duty cycle is calculated as

$$\begin{aligned} D_{max} &= \frac{V_r}{V_r + V_{DC_{min_{cap}}}} \\ &= 0,29 \end{aligned} \tag{4.11}$$

The required primary winding inductance, L_p, is then calculated as

$$\begin{aligned} L_p &= \frac{1}{\frac{1}{V_{DC_{min_{cap}}}} \cdot \sqrt{2 \cdot f_s \cdot P_{in_{max}}} \cdot (\frac{V_{DC_{min_{cap}}}}{V_r} + 1) + (\pi \cdot f_s \cdot \sqrt{C_{DS}})^2} \\ &= 1,51mH \end{aligned} \tag{4.12}$$

The average primary winding current is then calculated as

$$\begin{aligned} I_{av} &= \frac{P_{in_{max}}}{V_{DC_{min_{cap}}} \cdot D_{max}} \\ &= 0,3A \end{aligned} \tag{4.13}$$

The primary winding's ΔI is calculated through

$$\begin{aligned} \Delta I &= \frac{V_{DC_{min_{cap}}} \cdot D_{max}}{L_p \cdot f_s} \\ &= 0,76A \end{aligned} \tag{4.14}$$

The maximum current of the primary winding is then calculated as

$$\begin{aligned} I_{P_{max}} &= I_{av} + \frac{\Delta I}{2} \\ &= 0.76A \end{aligned} \tag{4.15}$$

The primary windings current valley after the MOSFET switches off is calculated in (4.16). This verifies that the SMPS indeed is working in DCM, as no DC is present over the switching transitions [3].

$$\begin{aligned} I_{valley} &= I_{p_{max}} - \Delta I \\ &= 0A \end{aligned} \tag{4.16}$$

The RMS current of the primary winding is calculated through

$$\begin{aligned} I_{p_{rms}} &= \sqrt{(3 \cdot (I_{av})^2 + (\frac{\Delta I}{2})^2 \cdot \frac{D_{max}}{3})} \\ &= 0,67A \end{aligned} \tag{4.17}$$

To guarantee non-saturation of the transformer, the minimum primary winding count is calculated as

$$\begin{aligned} N_p &\geq \frac{I_{p_{max}} \cdot L_p}{B_{max} \cdot A_e} \\ &\geq 119,44 \\ \Rightarrow N_p &\approx 120 \end{aligned} \tag{4.18}$$

The primary winding count is rounded up to 120 turns.
The output winding turns are calculated as

$$\begin{aligned} N_{s_1} &= \frac{N_p \cdot (V_{out_1} + V_{f_{diode}})}{V_r} \\ &= 7,07 \end{aligned} \tag{4.19}$$

$$\begin{aligned} N_{s_2} &= \frac{N_p \cdot (V_{out_2} + V_{f_{diode}})}{V_r} \\ &= 16,40 \end{aligned} \tag{4.20}$$

$$N_{aux} = \frac{N_p \cdot (V_{aux} + V_{f_{diode}})}{V_r} = 19,07 \tag{4.21}$$

Based on (4.19), (4.20) and (4.21) the turns ratios are calculated with equation (4.10) and displayed in Table 4.4 below.

Table 4.4: Calculated winding turn ratios

Parameter	Calculated value
$\eta_{ratio_{out_1}}$	$16,97$
$\eta_{ratio_{out_2}}$	$7,32$
$\eta_{ratio_{out_{aux}}}$	$6,29$

4.3.4 Sense resistor

With V_{cs} set to $1V$ [13], the resistance value for the sense resistor is calculated as

$$R_{sense} = \frac{V_{cs}}{I_{p_{max}}} = 1,32\Omega \tag{4.22}$$

The power rating of the resistor is calculated as

$$P_{sr} = I_{p_{rms}}^2 \cdot R_{sense} = 0,59W \tag{4.23}$$

4.3.5 Output rectifier diodes

The required minimum reverse voltage tolerance for each output's rectifier diode is calculated as

$$V_{r_{diode_1}} = V_{out_1} + V_{DC_{max_{Pk}}} \cdot \frac{N_{s_1}}{N_p} = 28,96V \tag{4.24}$$

$$V_{r_{diode_2}} = V_{out_2} + V_{DC_{max_{Pk}}} \cdot \frac{N_{s_2}}{N_p} = 67,54V \tag{4.25}$$

$$V_{r_{diode_{aux}}} = V_{out_{aux}} + V_{DC_{max_{Pk}}} \cdot \frac{N_{aux}}{N_p} = 78,64V \tag{4.26}$$

4.3.6 Snubber network

The voltage to be clamped is calculated in (4.27). $V_{DS_{max}}$ is the maximum drain-source voltage of the build-in MOSFET [13].

$$\begin{aligned} V_{clamp} &= V_{DS_{max}} - V_{DC_{max_{Pk}}} - V_r \\ &= 103,43V \end{aligned} \tag{4.27}$$

The value of the clamping capacitor is calculated as

$$\begin{aligned} C_{clamp} &= \frac{I_{p_{max}}^2 \cdot L_{leak}}{(V_r + V_{clamp}) \cdot V_{clamp}} \\ &= 50,43nF \end{aligned} \tag{4.28}$$

The value of the clamping resistor is calculated as

$$\begin{aligned} R_{clamp} &= \frac{(V_{clamp} + V_r)^2 - V_r^2}{0,5 \cdot L_{leak} \cdot I_{p_{max}}^2 \cdot f_s} \\ &= 122,22k\Omega \end{aligned} \tag{4.29}$$

4.3.7 Output capacitors

Due to the output capacitor calculations presented in [12] giving unreasonable results, with ripple currents exceeding 17 A, they were not used. Even when inputting the same values as used in the examples, the results do not match.

Instead the same capacitance were used as in [14], resulting in $C_{out_1} = 1200\mu F$, $C_{out_2} = 1800\mu F$.

4.3.8 Output filter

As the equations for the LC output filters from [12] build upon the equations for the output capacitors, they were not used.

The component values were taken from [14] and then simulated in LTspice for verification.

4.3.9 VCC capacitor

A $22\mu F$ electrolytic with a $100nF$ ceramic capacitor in parallel was used, as specified in [12].

4.3.10 Regulation loop

Initial parameters used for calculating the feedback components are presented in Table 4.5.

Table 4.5: Regulation loop input parameters

Parameter	Value
Shunt regulator reference voltage, V_{ref}	$1,24V$ [15]
Minimum shunt cathode current, $I_{k_{min}}$	$100\mu A$ [15]
Maximum optocoupler diode current, $I_{d_{max}}$	$10mA$ [16]
Forward optocoupler diode voltage drop, $V_{f_{opto}}$	$1,2V$ [16]
Optocoupler gain, G_{opto}	$1,3$ [16]
Selected weight factor for V_{out_1}, W_{out_1}	$0,5$
Selected weight factor for V_{out_2}, W_{out_2}	$0,5$
Internal R_{fb} pull-up resistor	$15k\Omega$ [12]
FB pin voltage, V_{fb}	$3,3V$ [13]
Overload protection voltage level, $V_{fb_{olp}}$	$2,75V$ [13]

As voltage reference TLV431 was chosen, due to the low cathode current requirement [15], and being recommended in [5]. FOD817B3SD [16] was chosen as the feedback optocoupler, essentially due to being in stock at the time and having similar specifications as the optocoupler used in the design guide [12].

The maximum feedback (FB) pin current is calculated as

$$\begin{aligned} I_{fb_{max}} &= \frac{V_{fb}}{R_{fb}} \\ &= 0,22mA \end{aligned} \tag{4.30}$$

The minimum FB pin current is calculated as

$$\begin{aligned} I_{fb_{min}} &= \frac{V_{fb} - V_{fb_{max}}}{R_{fb}} \\ &= 0,036mA \end{aligned} \tag{4.31}$$

An overview of the secondary side of the feedback circuit is depicted in Fig. 4.1.

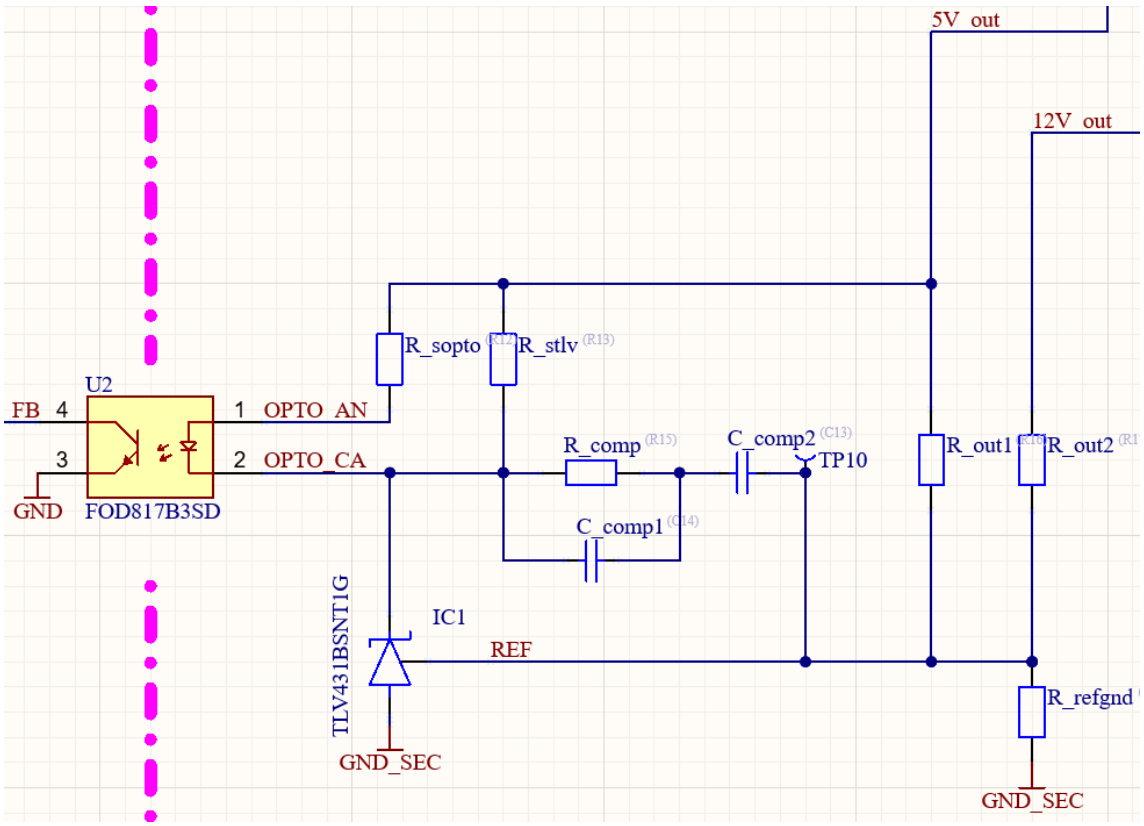

Figure 4.1: Feedback circuit.

As shown in the figure the resistors R_{out_1}, R_{out_2} and $R_{ref_{gnd}}$ create a voltage divider where the output voltage is set to V_{ref} by the shunt regulator $IC1$.

The desired current $I_{R_{ref_{gnd}}}$ through $R_{ref_{gnd}}$ is $100\mu A$, which results in the resistor value given in

$$\begin{aligned} R_{ref_{gnd}} &= \frac{V_{ref}}{I_{R_{ref_{gnd}}}} \\ &= 12,40k\Omega \end{aligned} \tag{4.32}$$

The values of resistors R_{out_1} and R_{out_2} are calculated as

$$\begin{aligned} R_{out_1} &= \frac{V_{out_1} - V_{ref}}{W_{out_1} \cdot R_{ref_{gnd}}} \\ &= 75k\Omega \end{aligned} \tag{4.33}$$

$$\begin{aligned} R_{out_2} &= \frac{V_{out_2} - V_{ref}}{W_{out_2} \cdot R_{ref_{gnd}}} \\ &= 215k\Omega \end{aligned} \tag{4.34}$$

The supply current for the optocoupler is limited by $R_{s_{opto}}$. Its value is calculated as

$$\begin{aligned} R_{s_{opto}} &\geq \frac{V_{out_1} - (V_{f_{opto}} + V_{ref})}{I_{d_{max}}} \\ &\geq 256\Omega \end{aligned} \tag{4.35}$$

The current to supply the TLV431 is limited by $R_{s_{tlv}}$. The resistance is calculated as

$$\begin{aligned} R_{s_{tlv}} &\leq \frac{V_{f_{opto}} + (R_{s_{opto}} \cdot \frac{I_{fb_{min}}}{G_{opto}})}{I_{k_{min}}} \\ &\leq 82,89k\Omega \end{aligned} \tag{4.36}$$

Both output voltages are then calculated again, based on the given regulation loop component values, according to

$$\begin{aligned} V_{out_{1_{rl}}} &= V_{ref} + (R_{out_1} \cdot W_{out_1} \cdot R_{ref_{gnd}}) \\ &= 5,00V \end{aligned} \tag{4.37}$$

$$\begin{aligned} V_{out_{2_{rl}}} &= V_{ref} + (R_{out_2} \cdot W_{out_2} \cdot R_{ref_{gnd}}) \\ &= 12,00V \end{aligned} \tag{4.38}$$

4.3.11 Feedback compensation network

Initial parameters for use in calculations are presented in Table 4.6.

Table 4.6: Feedback compensation network input parameters

Parameter	Value
Chosen crossover frequency, f_g	3kHz [12]
PWM-OP gain, G_{pwm}	2,05 [13]

The FB transfer characteristics is calculated as

$$\begin{aligned} K_{fb} &= \frac{G_{opto} \cdot R_{fb}}{R_{s_{opto}}} \\ &= 76,17 \end{aligned} \tag{4.39}$$

The FB transfer gain is calculated as

$$\begin{aligned} G_{fb} &= 20 \cdot \log(K_{fb}) \\ &= 37,64dB \end{aligned} \tag{4.40}$$

The voltage divider transfer characteristics is calculated as

$$\begin{aligned} K_{vd} &= \frac{R_{ref_{gnd}}}{R_{ref_{gnd}} + R_{out_1}} \\ &= 0,14 \end{aligned} \tag{4.41}$$

The gain of the voltage divider transfer characteristics is calculated as

$$\begin{aligned} G_{vd} &= 20 \cdot \log(K_{vd}) \\ &= -16,96dB \end{aligned} \tag{4.42}$$

The resistance at the maximum and minimum load poles are calculated as

$$\begin{aligned} R_{lh} &= \frac{V^2_{out_{1_{rl}}}}{P_{out_{max}}} \\ &= 7,20\Omega \end{aligned} \tag{4.43}$$

$$\begin{aligned} R_{ll} &= \frac{V^2_{out_{1_{rl}}}}{P_{out_{min}}} \\ &= 28,80\Omega \end{aligned} \tag{4.44}$$

With nc is set to 1, the pole frequencies at maximum and minimum load are calculated as

$$\begin{aligned} f_{oh} &= \frac{1}{\pi \cdot R_{lh} \cdot (nc \cdot C_{out_1})} \\ &= 36,84Hz \end{aligned} \tag{4.45}$$

$$\begin{aligned} f_{ol} &= \frac{1}{\pi \cdot R_{ll} \cdot (nc \cdot C_{out_1})} \\ &= 9,21Hz \end{aligned} \tag{4.46}$$

The zero frequency of the compensation network is set to the middle of the maximum and minimum pole frequencies. It is calculated as

$$\begin{aligned} f_{om} &= f_{oh} \cdot 10^{(0,5 \cdot \log(\frac{f_{oL}}{f_{oh}}))} \\ &= 7,47Hz \end{aligned} \tag{4.47}$$

The transient impedance characterizes the relationship between the FB pin voltage and the peak current. It is calculated as

$$\begin{aligned} Z_{pwm} &= G_{pwm} \cdot \frac{R_{sense}}{V_{cs}} \\ &= 2,71\Omega \end{aligned} \tag{4.48}$$

The crossover frequency power stage is calculated as

$$\begin{aligned} |F_{pwr}(f_g)| &= \frac{1}{Z_{pwm}} \cdot \sqrt{\frac{R_{lh} \cdot L_p \cdot f_s \cdot \eta_e}{2}} \cdot \frac{1}{\sqrt{1 + (\frac{f_g}{f_{oh}})^2}} \\ &= 0,072 \end{aligned} \tag{4.49}$$

The power stage crossover frequency gain is calculated as

$$\begin{aligned} G_{pwr}(f_g) &= 20 \cdot \log(|F_{pwr}(f_g)|) \\ &= -22,85dB \end{aligned} \tag{4.50}$$

The combined gain of the regulation loop at frequency f_g is calculated as

$$\begin{aligned} G_{rl}(\omega) &= G_{fb} + G_{pwr} + G_{vd} \\ &= -2.17dB \end{aligned} \tag{4.51}$$

The separated components of the regulator are calculated as

$$\begin{aligned} G_{rl_{sep}} &= 0 - G_{rl} \\ &= 2.17dB \end{aligned} \tag{4.52}$$

With this, the resistance of the compensation resistor R_{comp} is calculated as

$$\begin{aligned} R_{comp} &= 10^{\frac{G_{rlsep}}{20}} \cdot \frac{R_{out_1} \cdot R_{ref_{gnd}}}{R_{out_1} + R_{ref_{gnd}}} \\ &= 13,66k\Omega \end{aligned} \tag{4.53}$$

The capacitor parallel to R_{comp} is calculated as

$$\begin{aligned} C_{comp_1} &= \frac{1}{2 \cdot \pi \cdot R_{comp} \cdot f_g} \\ &= 3,88nF \end{aligned} \tag{4.54}$$

The series capacitor is calculated as

$$\begin{aligned} C_{comp_2} &= \frac{1}{2 \cdot \pi \cdot R_{comp} \cdot f_{om}} \\ &= 1,56\mu F \end{aligned} \tag{4.55}$$

4.3.12 Zero crossing and output over voltage protection

In Table 4.7 initial parameters for use in calculatios are specified.

Table 4.7: Zero crossing, over voltage protection input parameters

Parameter	Value
Output overvoltage protection limit, $V_{out_{ovp}}$	$16V$
Output overvoltage threshold, $V_{zcd_{ovp_{min}}}$	$1,9V$ [12]
Internal R_{zcd} value	$3k\Omega$ [13]
f_{osc2}	820kHz [12]
Controller delay time, t_{delay}	$100ns$ [12]

The series resistor R_{zc} is calculated as

$$\begin{aligned} R_{zc} &= R_{zcd} \cdot \left(\left(\frac{N_{aux}}{N_{s_1}} \cdot \frac{V_{out_{ovp}} + V_{f_{diode}}}{V_{zcd_{ovp_{min}}}} \right) - 1 \right) \\ &= 66,42k\Omega \end{aligned} \tag{4.56}$$

The capacitor C_{zc} is calculated as

$$\begin{aligned} C_{zc} &= \tan\left(2 \cdot \pi \cdot \left(\frac{1}{4} - t_{delay} \cdot f_{osc2}\right)\right) \cdot \frac{R_{zc} + R_{zcd}}{R_{zc} \cdot R_{zcd}} \cdot \frac{1}{2 \cdot \pi \cdot f_{osc2}} \\ &= 11,94nF \end{aligned} \tag{4.57}$$

4.3.13 Line over voltage protection, brown-out

Initial calculations values are defined in Table 4.8.

Table 4.8: Line over voltage protection, brown-out parameters

Parameter	Value
Defined $V_{line_{ovp_{AC}}}$	$300V$
VIN minimum overvolage, $V_{vin_{lovp}}$	$2,9V$ [13]
VIN brown-out, $V_{vin_{bo}}$	$0,4VV$ [13]
VIN brown-in, $V_{vin_{bi}}$	$0,66V$ [13]
VIN reference voltage, $V_{vin_{ref}}$	$1,52V$ [13]
VIN DC bus supply resistor, $R_{vin_{bus}}$	$9M\Omega$ [12]

The resistor value for the $R_{vin_{gnd}}$ used in the VIN voltage divider is calculated as

$$\begin{aligned} R_{vin_{gnd}} &= \frac{R_{vin_{bus}} \cdot V_{vin_{lovp}}}{(V_{line_{ovp_{AC}}} \cdot \sqrt{2}) - V_{vin_{lovp}}} \\ &= 61,94k\Omega \end{aligned} \tag{4.58}$$

4.4 Schematic capture, component selection

With the calculations done, suitable components were chosen based on the results and the tolerances specified in [10] and [11]. Components used that were not calculated in the previous sections had their specifications based on similar devices found in [14].

To improve the cross-regulation of the outputs, a Zener diode of $9V$ was connected between the outputs. The cathode was connected to the $12V$ output and thus limits the output voltage according to (4.59).

$$\begin{aligned} V_{out_{2_{max}}} &= V_{out_1} + 9V \\ &= 14V \end{aligned} \tag{4.59}$$

A schematic capture of the SMPS circuit was constructed with the ECAD tool Altium Designer. The circuit design was based on the typical application circuit of the chosen controller described in [13], [12], and [14]. The finished schematic is presented in Fig. 4.2, with a larger version in appendix A.

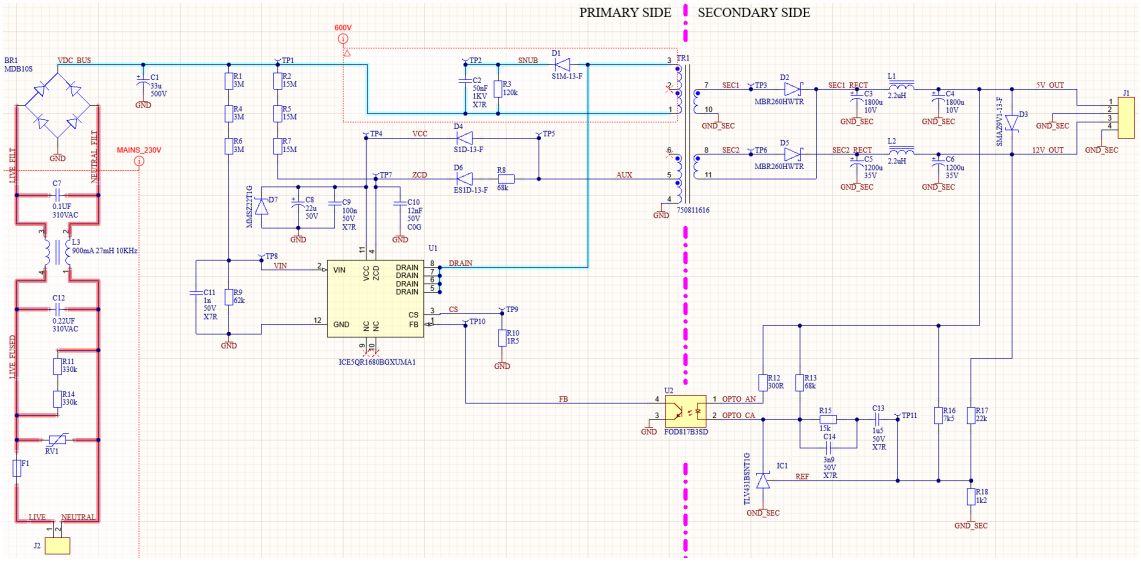

Figure 4.2: Finished schematic capture.

As can be gathered from the figure, the schematic is divided up into two parts with the transformer and optocoupler acting as bridges. On the left side is the primary side, which includes the mains electricity input, rectifier, snubber circuit and QR controller IC circuitry. The secondary side is on the right of the transformer and includes the output rectifiers, filters and feedback circuitry.

Before each component was placed in the schematic, symbols, footprints and 3D models for all individual devices were added to the ECAD component library. These were either sourced from suppliers or created manually. The 3D models were obtained for the possibility of representing the PCBA in a 3D view.

The component analysis including the calculations were done in parallel with the schematic development. Only after a component and its value were finalized, it

was added to the schematic. This was to limit the risk of the schematic capture containing incomplete research.

After the schematic capture was done, a bill of materials (BOM) was exported from the ECAD tool and all required components were sourced from appropriate vendors. This was done before the PCB was designed due to component lead times and the risk of them going out of stock due to shortages. The finalized BOM is presented in appendix B.

4.5 PCB design

With the schematic capture completed, the design process of the PCB was initiated.

First, a layer stackup was chosen. In other words, the number of copper layers of the PCB was chosen. It was decided that a four-layer board would be sufficient for the project, as the price increase over a two-layer board is marginal. A four-layer board may also improve routing flexibility and thus allow for better signal integrity [17]. A view of the layer stackup is presented in Fig. 4.3.

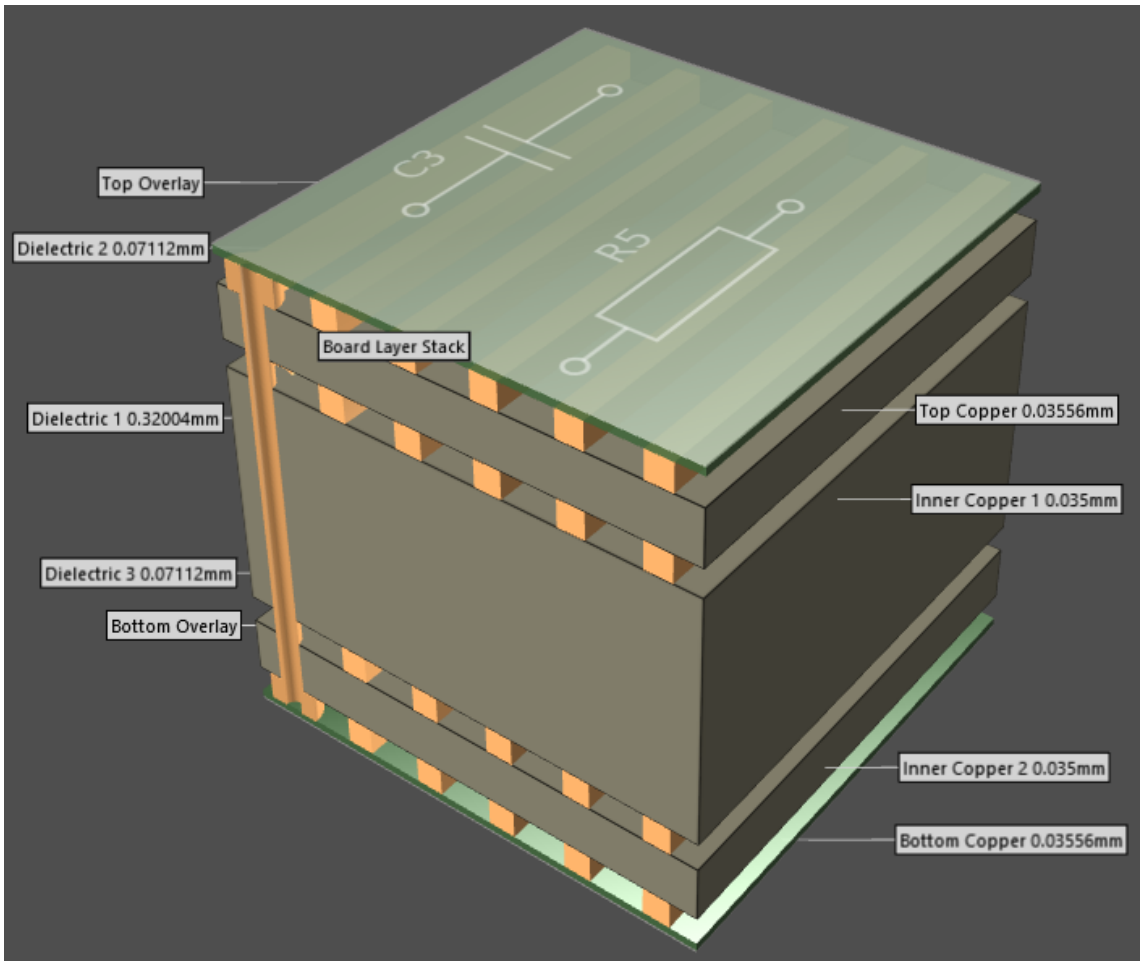

Figure 4.3: Visualization of the layer stackup.

In the figure four copper signal layers are visible, with the dielectric isolation material between them.

Due to the thicker middle dielectric plane, the inner copper layers were used as ground planes, while the outer copper layers were used as signal planes. This was to maximize the coupling between the signals and their return current paths. The potential gain is increased signal quality [17] and decreased radiated EMI, due to the reduction in created magnetic fields.

The PCB design is presented in Fig. 4.4, with a 3D model of the finalized PCB in Fig. 4.5.

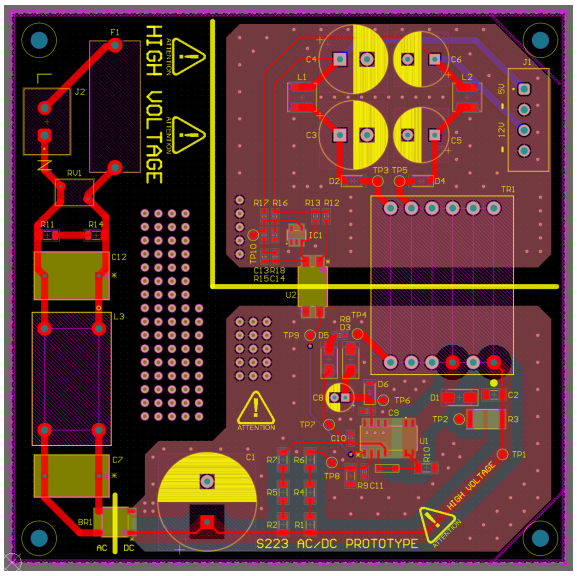

Figure 4.4: PCB in the design view.

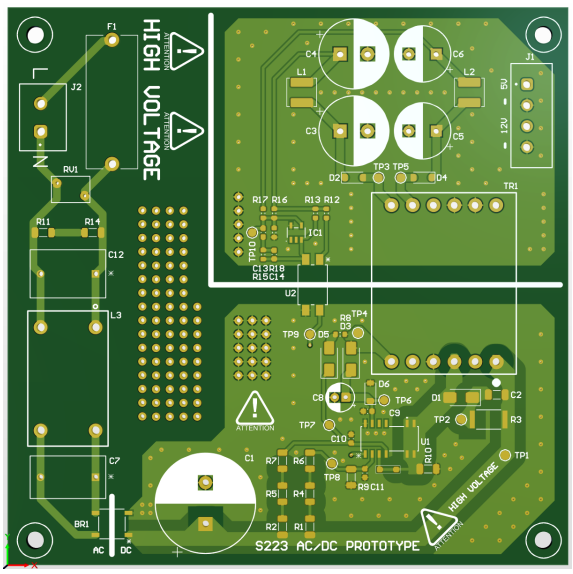

Figure 4.5: PCB in a simulated 3D view.

As can be seen in the figures, the PCB is divided into three parts. One part is for the 230VAC component and traces, which are viewable to the left. This leads to the part with the high voltage DC via the bridge rectifier. This part includes high voltage components such as the DC bus bulk capacitor, the snubber circuit and the QR controller IC.

The final part of the PCB is the low voltage secondary side of the transformer. Positioned to the top right in the figures. It includes the output filtering and feedback circuit, which is connected to the high voltage DC side via the transformer and an optocoupler, which provides galvanic isolation.

In Fig. 4.6, a visual representation of the finished PCBA is presented.

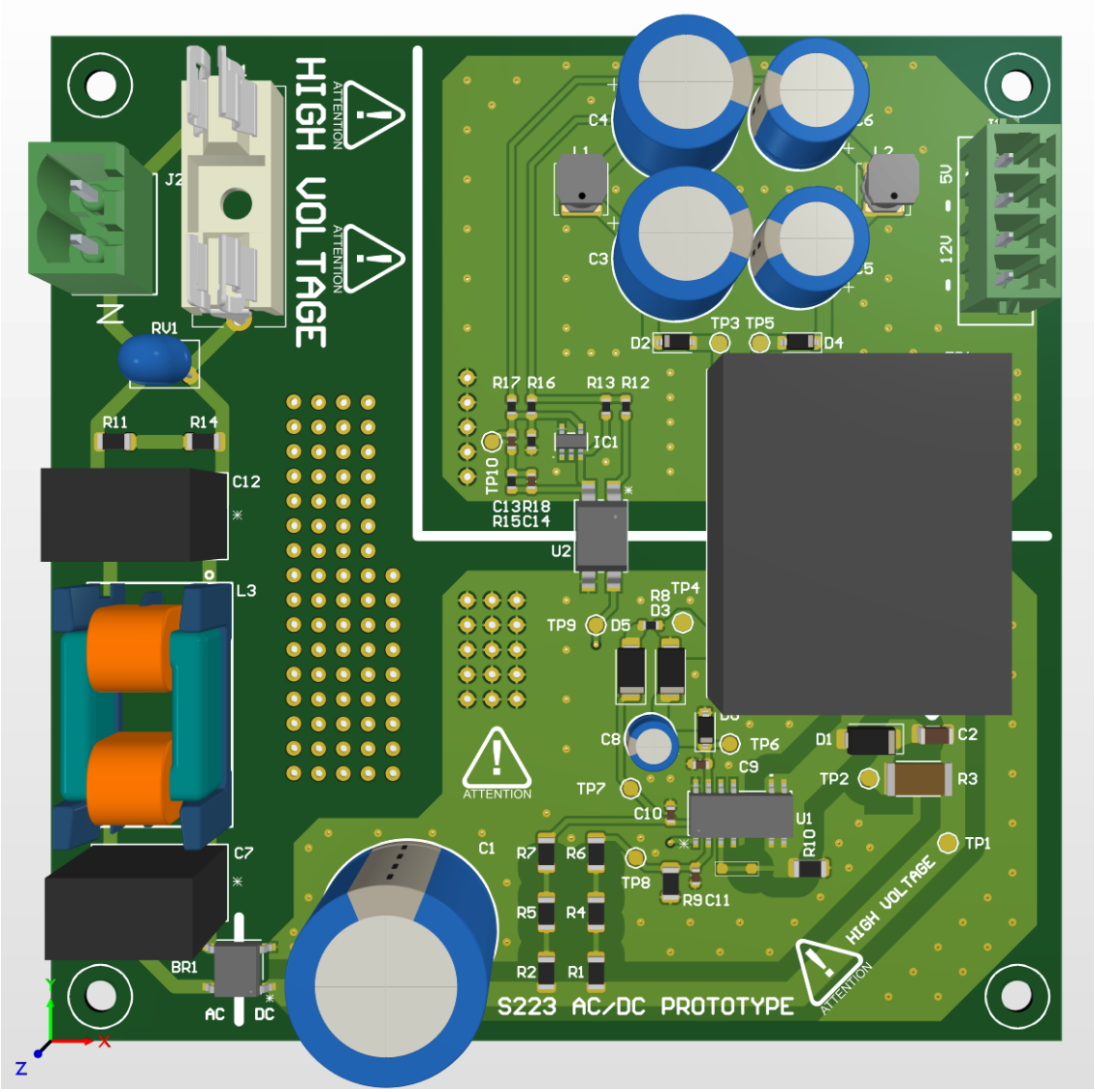

Figure 4.6: Simulated 3D view of the PCBA.

The figure includes all components mounted on the PCB. Notable are the extra distances where high voltage components and traces are present, which are based of the requirements presented in [10] and [11].

Also included are extra unconnected vias on each ground plane as well as on the AC voltage part. These allow for the simple addition of extra components at the prototyping stage.

With the PCB design done, it was exported from Altium Designer and sent to a PCB manufacturer.

4.6 Prototype assembly

When the manufactured boards and components all had arrived, a prototype was assembled. This was done by manually soldering all the required components to the PCB, creating a PCBA. The finished prototype is visible in Fig. 4.7.

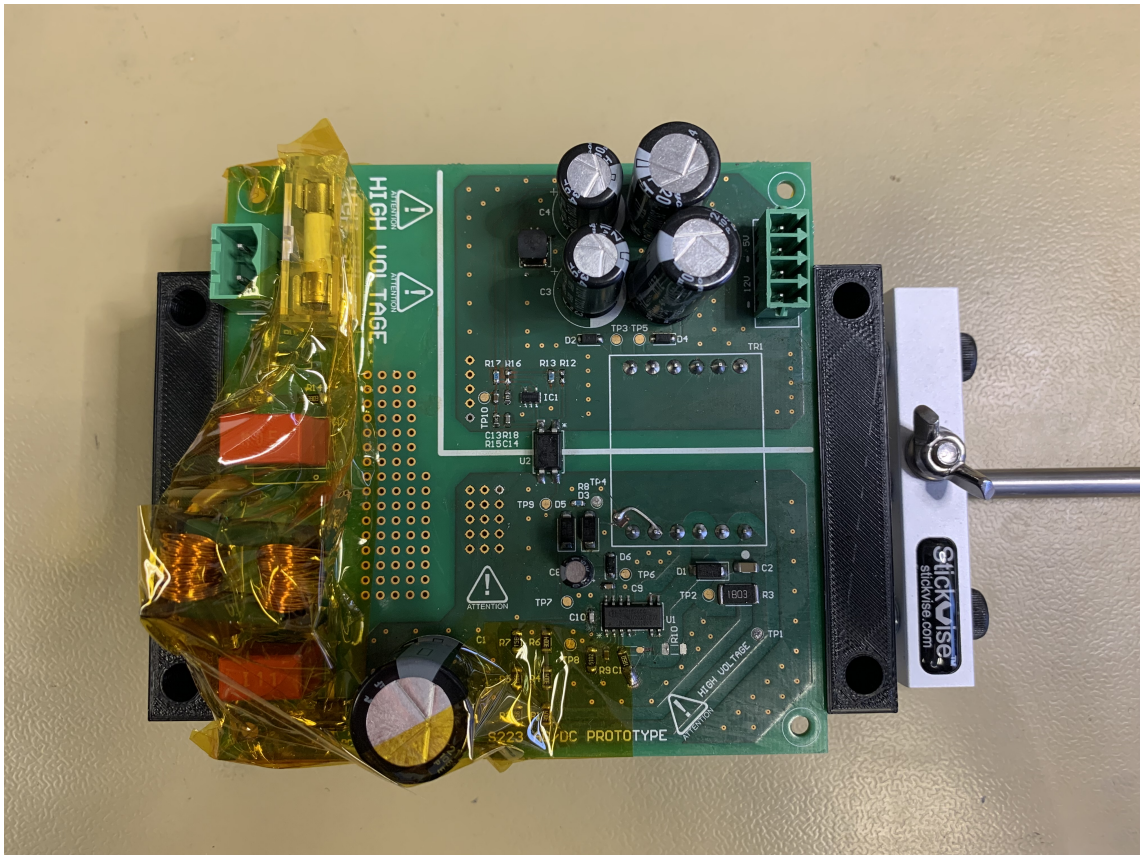

Figure 4.7: Constructed PCBA.

The tape visible in the figure is isolation tape with high voltage tolerance. It is added to increase the safety when handling the device. Some discrepancies are also noticeable when compared to the simulated 3D model of the PCBA. This is due to footprint errors and is discussed further in the following chapters.

5
Bring-up

This section will describe all faults discovered when debugging the SMPS, as well as the measures that are taken to patch them. As SMPS are complicated devices composed of several different circuit functionalities that need to coincide, the debugging phase of this project was extensive.

During the first power-up, the prototype was supplied via a variable transformer to allow for gradual increments of the supply voltage as a safety precaution. The setup included a residual-current circuit breaker and an isolation transformer. This was to protect the operator and the measurement instruments.

The use of differential probes was necessary due to the high voltages present on the primary side of the transformer. Also, it was required to not short-circuit the transformer through the oscilloscope, which can happen if probing on both the primary and secondary sides of a transformer without at least one differential probe. This is due to the inputs usually being referenced to the same ground.

5.1 Fault 1: Fuses blown at startup

The input fuse of the prototype instantly blew when applying power. When measuring the resistance with a multimeter between the live and neutral input connectors, the resulting low resistance indicated a short circuit between them.

By disconnecting components and circuits sequentially closer to the power input on the primary side, while continuously measuring the resistance, the culprit of the short circuit was identified as the input filter inductor. It was discovered that the pin numbering of the component symbol did not match the pin numbering of the component footprint. This led to faulty routing on the PCB.

By soldering wires from the inductor pins to the correct PCB connections, the short circuit between the live and neutral rails disappeared. The solution taken is visible in Fig. 5.1.

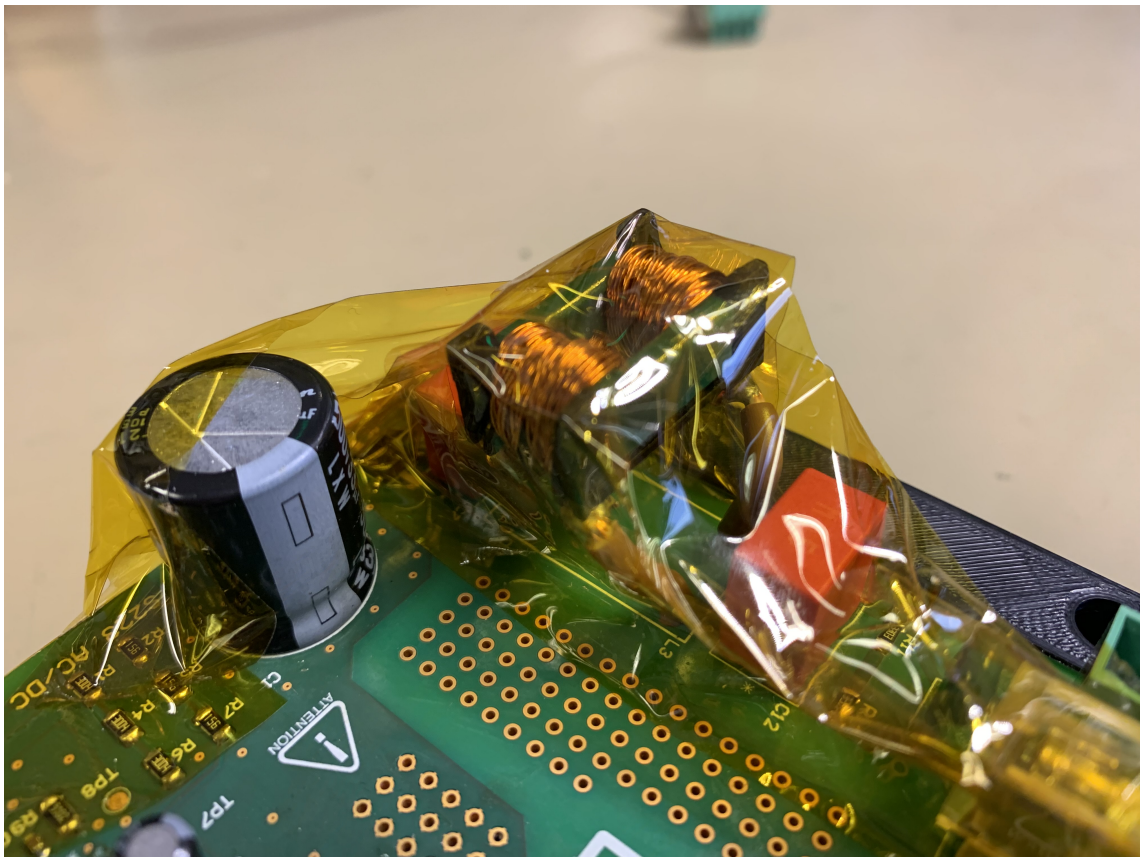

Figure 5.1: Input filter inductor soldered to wires.

The pins of the input filter inductor, the component with two coils, are soldered directly to wires. The wires are in turn are soldered to the correct traces on the PCB.

When troubleshooting the short circuit, it was also detected that the same error had happened with the high-frequency transformer. The footprint of the transformer was mirrored, which resulted in the footprint pins connecting to the wrong symbol pins. This error was corrected by mounting the transformer on the other side of the PCB, which was possible due to it being a through-hole component.

5.2 Fault 2: Dead controller IC

Still, after the short circuit was fixed, the SMPS showed no switching activity when probing the transformer test points with an oscilloscope. Neither were any voltages present on the secondary side circuits, which led to the belief that the controller IC was unable to power up.

Still, the voltage potentials present on the high voltage DC bus and TP8, after the resistor divider, were correct according to the calculations in [12] and the requirements in [13].

After revisiting the datasheet of the transformer, the issue was discovered. By a miscalculation, the wrong auxiliary winding of the transformer had been connected to the VCC of the controller IC.

The controller IC requires a startup current derived from the high voltage DC bus to charge up an internal capacitor [13]. When this capacitor is charged to a predefined level, the controller will start to switch its built-in MOSFET and secure its power supply from the VCC pin instead.

The VCC pin voltage is in turn derived from the auxiliary winding. With the used winding this voltage would have been below the required amplitude, and thus the controller IC would not have started.

By connecting the VCC trace to the correct winding of the transformer, the SMPS started up.

5.3 Fault 3: Instability and substantial output ripple

The output voltage regulation displayed severe voltage regulation issues on both the $5V$ and $12V$ outputs when measuring the voltage directly on the output capacitors. The resulting measurements of the $5V$ output when presented with a load of 34Ω are presented in Fig. 5.2.

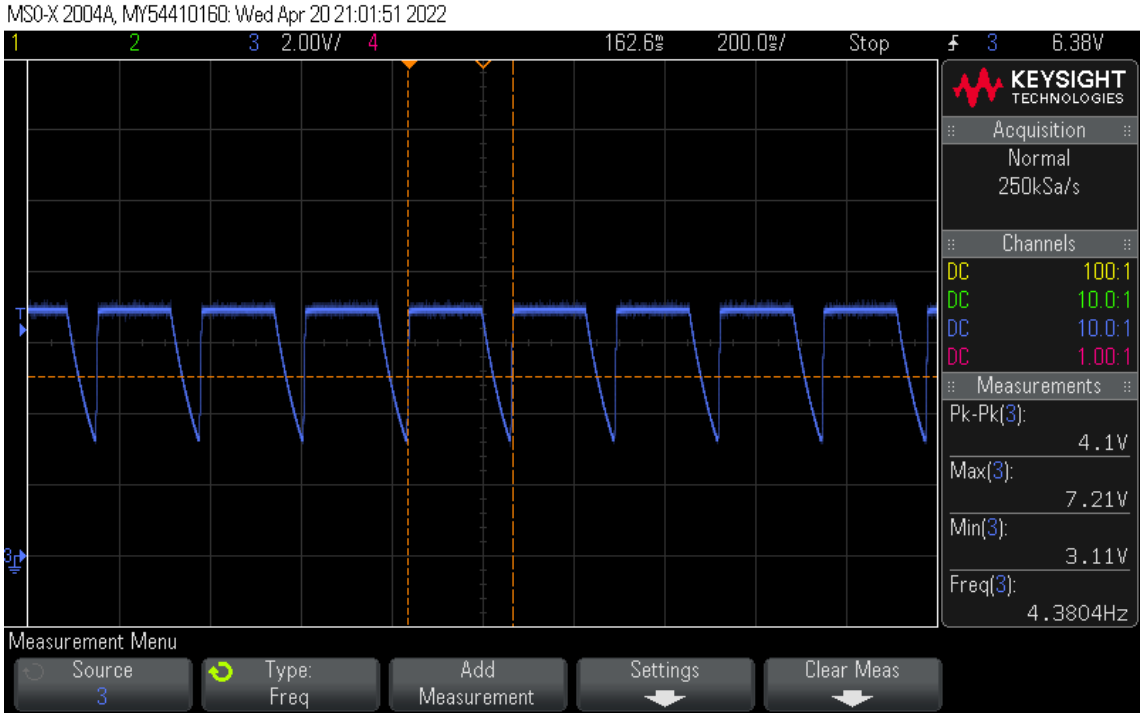

Figure 5.2: Voltage ripple measurements with a 34Ω load.

As demonstrated in the figure peak-to-peak ripple voltages of up to $4,1V$ are present, with the maximum amplitude at $7,2V$ and the minimum at $3,1V$.

One interesting discovery is that at specific loads the output regulation was stable down to a couple of hundred millivolts, as can be seen in Fig. 5.3.

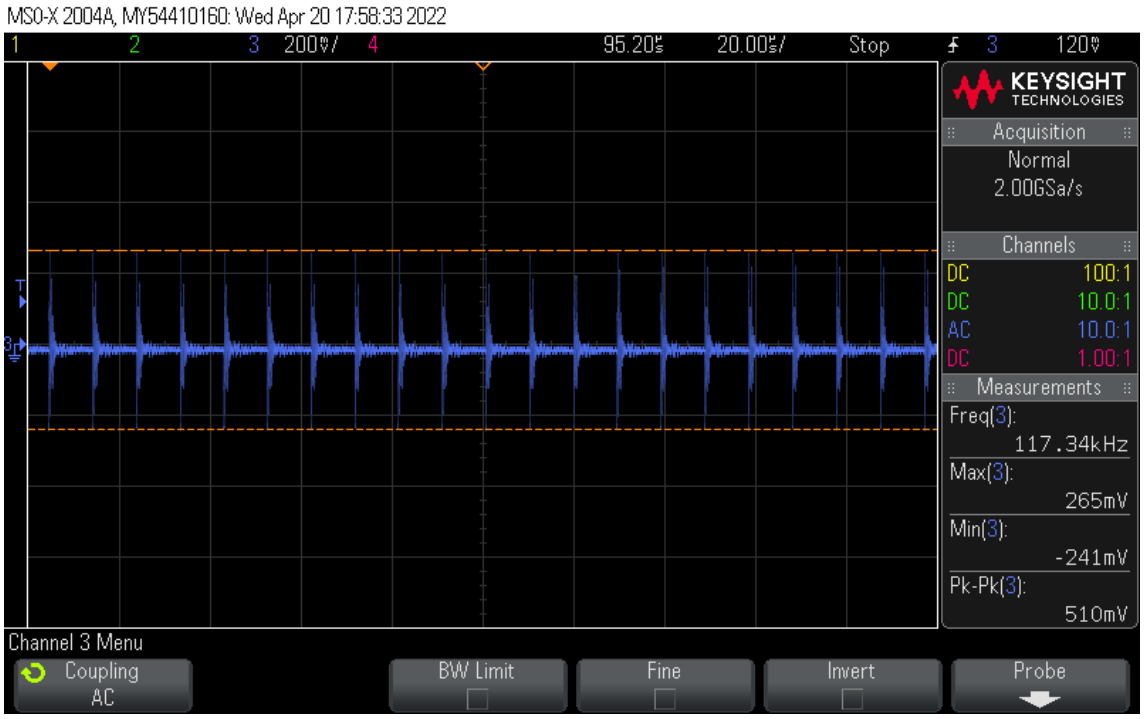

Figure 5.3: Ripple measurements with a 16Ω load.

Depicted above is the $5V$ output loaded with 16Ω. The voltage ripple is now at $510mV$ peak-to-peak, which is a substantial improvement compared to the ripple at a load of 34Ω.

Measurement of test points and other points of interest such as the voltage supplies on the primary side showed no faults. While measuring test points or component pins in the feedback circuit with oscilloscope probes, it sometimes significantly improved or worsened the output voltage ripple, seemingly at random.

This hinted at faults within the feedback circuitry. To simplify further troubleshooting, the $12V$ output rail was disabled by removing D4 and R17 and adjusting R16 to amount to 100% of the required weighting current.

When adjusting the value of R16, a value was chosen that slightly altered the voltage divider made up of R16 and R18. As the REF pin of the voltage reference IC1 is constantly at $1.24V$, it resulted in the $5V$ output rail increasing to $7V$.

This increment improved the voltage regulation significantly over a wider span of resistive loads, which implicated that the error was somehow related to the current going into the feedback circuit, as with a higher output voltage on the $5V$ rail, the current going through R13 would increase.

By greatly reducing the resistance of R13, the voltage regulation showed the same performance with the output configured to $5V$ as with $7V$, which gave the impression that either the voltage reference or the optocoupler was unstable.

The graph in Fig. 5.4, based on a graph from the datasheet of the voltage reference [15], supported the theory that it was the culprit of the instability.

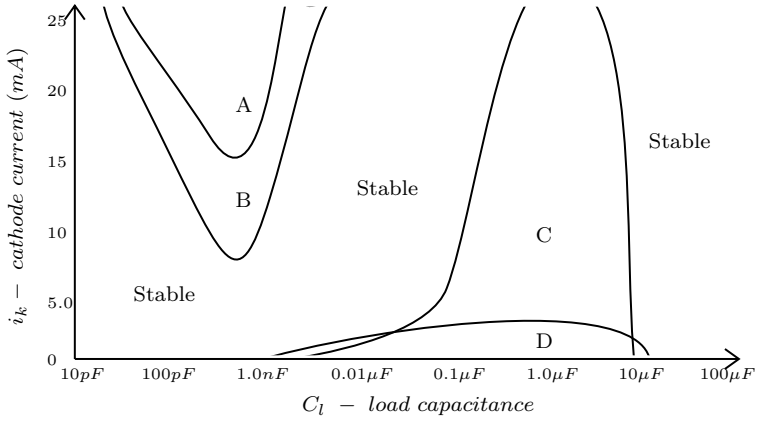

Figure 5.4: Graph of voltage reference instability regions, due to capacitive loading.

As can be viewed in the figure, the voltage reference has unstable regions which depend on the capacitive load applied to the reference, and the current through the cathode. When applying a cathode voltage of $5V$, the relevant regions are B and D [15]. The crucial region is most likely D, due to the original cathode current of $100\mu A$.

By decreasing R13, the current through IC1's cathode would have increased, which might have moved the voltage reference out from a region of instability.

This was further backed by experiments where the feedback filter of the voltage reference, as well as the output filter of the $5V$ rail, were significantly changed before increasing the R13 current, without any difference in the unstable behaviour.

With the resistance of R13 decreased to $1k\Omega$, the performance gained was deemed sufficient to evaluate the prototype.

6
Verification

6.1 Efficiency

An oscilloscope with a differential probe and a current probe is used to measure the input voltage and current, including the phases. A built-in math function of the oscilloscope calculates the average true input power $P_{in_{true}}$, according to (2.2).

An electronic load is used to apply constant current loads to one of the SMPS outputs. The output power will be measured by the electronic load.

The measurements will be conducted at the maximal possible load for each output, while the other output is unloaded. This is a deviation from the testing methodology specified in [9] due to time constraints. The maximum load is determined as the load preceding the safety shutdown of the controller IC.

The testing setup is presented in Fig. 6.1 and in Fig. 6.2.

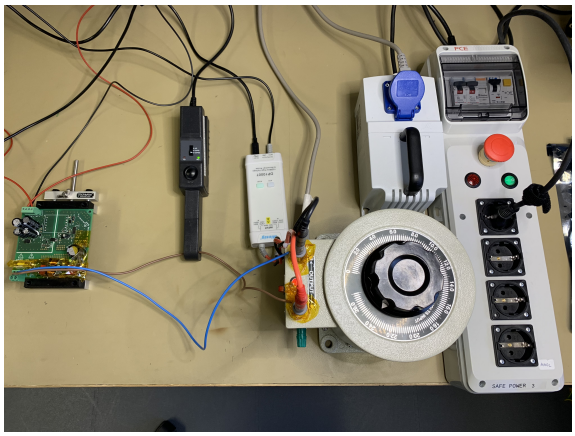

Figure 6.1: Prototype supply setup.

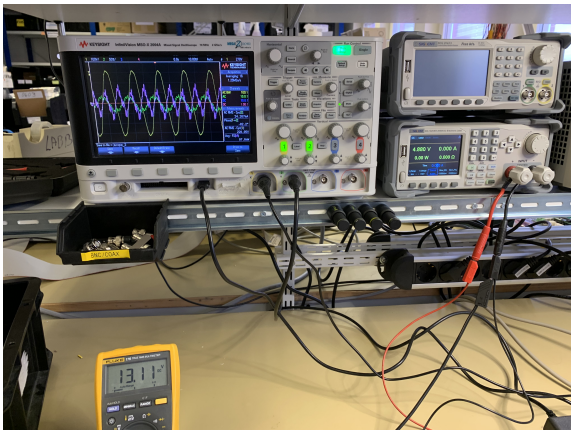

Figure 6.2: Prototype measurement setup.

Observable in the figures above are the equipment used during the measurements, such as the current probe, the differential probe connected to the variable transformer and the oscilloscope.

The results from the measurements at the maximum load for the $5V$ output are presented in Fig. 6.3 respectively Fig. 6.4.

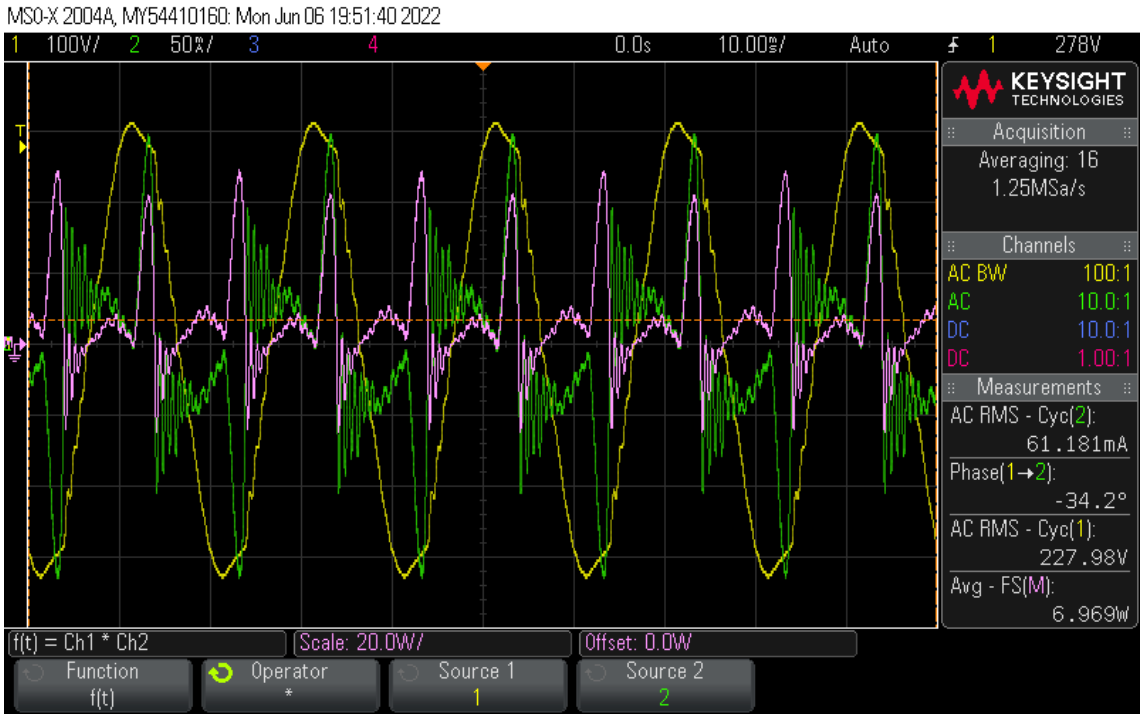

Figure 6.3: The measured input voltage (yellow), input current (green), and the computed power $P_{in_{true}}$ (pink) with the $5V$ output loaded.

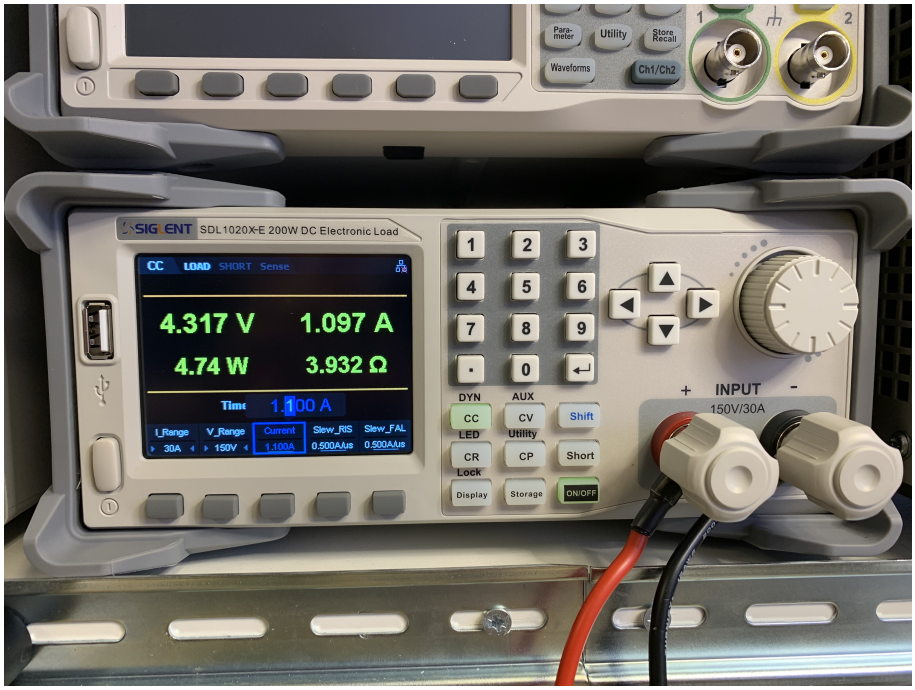

Figure 6.4: The applied load and output measurements for the $5V$ output.

As can be gathered from the figures, the maximum stable load of the $5V$ output with the $12V$ output unloaded was $1,097A$.

The $12V$ output measurements are presented in Fig. 6.5 respectively Fig. 6.6.

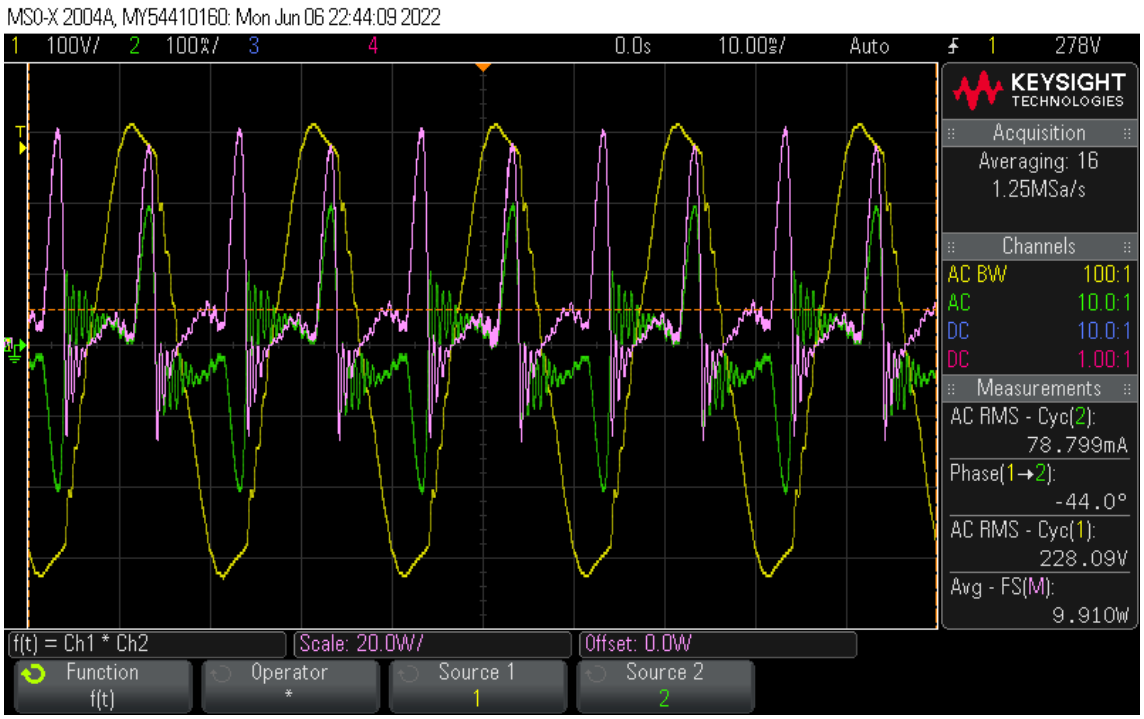

Figure 6.5: The measured input voltage (yellow), input current (green), and the computed power $P_{in_{true}}$ (pink) with the $12V$ output loaded.

Figure 6.6: The applied load and output measurements for the $12V$ output.

As displayed above the maximum achievable stable load for the $12V$ output was $0,898A$.

Using the results from the measurements, the efficiency is calculated with (2.1) and presented in Table (6.1). The input power was also measured without any load applied to either output, which is included in the table.

Table 6.1: Calculated efficiency

Output loaded	Load	Measured $P_{in_{true}}$	Measured P_{out}	Calculated η_e
$5V$	$1,10A$	$6,97W$	$4,74W$	$0,68$
$12V$	$0,90A$	$9,91W$	$8,57W$	$0,87$
None	-	$75mW$	-	-

6.2 Output ripple and switching transients

The test setup in the project uses an isolation transformer, an electronic load, and an oscilloscope. The oscilloscope is used with a custom-built X1 probe.

The X1 probe was constructed using an RG58 coaxial cable with a characteristic impedance of 50Ω. In other words, this means that the ratio of the voltage and current in a travelling wave is 50Ω [5], [17]. A series capacitor of $0,01\mu F$ was connected to the signal path to block DC currents [9]. The X1 probe was terminated into a 50Ω resistor in order to eliminate reflections [5], [9], [17]. The constructed probe is presented in Fig. 6.7.

Figure 6.7: Constructed X1 probe.

Depicted above is the X1 probe, including its DC blocking capacitor and the connected 50Ω termination.

The prototype is supplied by the isolation transformer and the variable transformer. This is to eliminate any ground loops created through the instruments connected [9]. The oscilloscope's custom probes are connected to the output capacitors. An electronic load is connected to one output while a multimeter is connected to the other. The differential probe is connected to the variable transformer to measure the input AC voltage.

Several different measurements are done. With the input ac voltage at the minimum rated value, each output is measured first at no load and then at its maximum achievable load, while the other output is unloaded. This is a deviation from the testing methodology specified in [9] due to time constraints. This is then repeated with the input ac voltage at its maximum rated value.

The connections to the prototype are illustrated in Fig. 6.8.

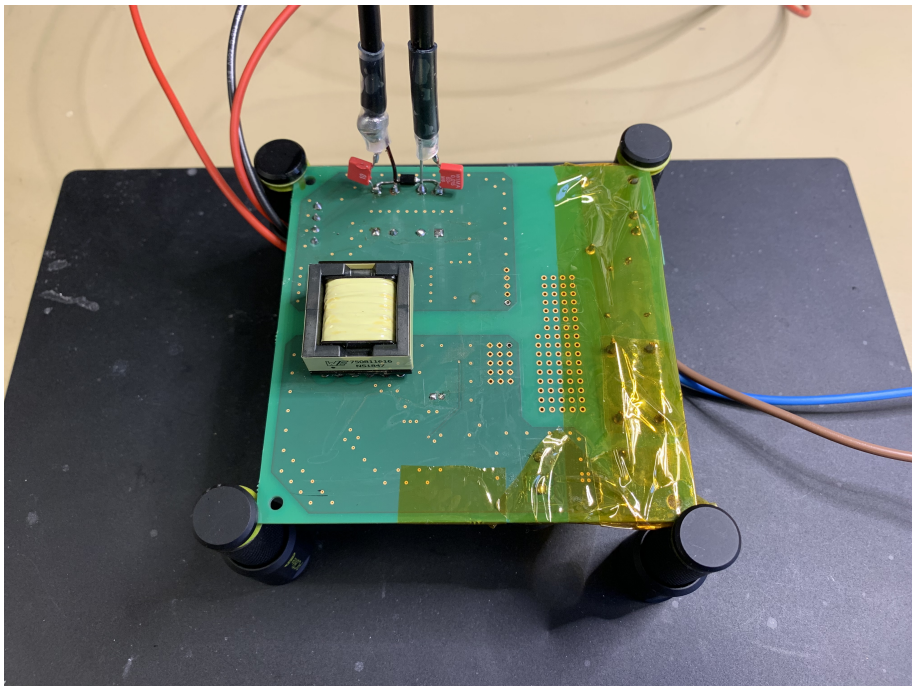

Figure 6.8: X1 probes soldered directly to output capacitors.

The X1 probes are soldered directly to the output capacitors. The cables on the right are the AC voltage input, while the cables to the right are the outputs connected to either an electronic load or a multimeter.

The maximum achievable input AC voltage from the variable transformer was $262V_{rms}$, hence this will be used instead of the maximum rated AC input voltage value.

The results from the measurements of the $5V$ output are presented in Fig. 6.9 respectively Fig. 6.10.

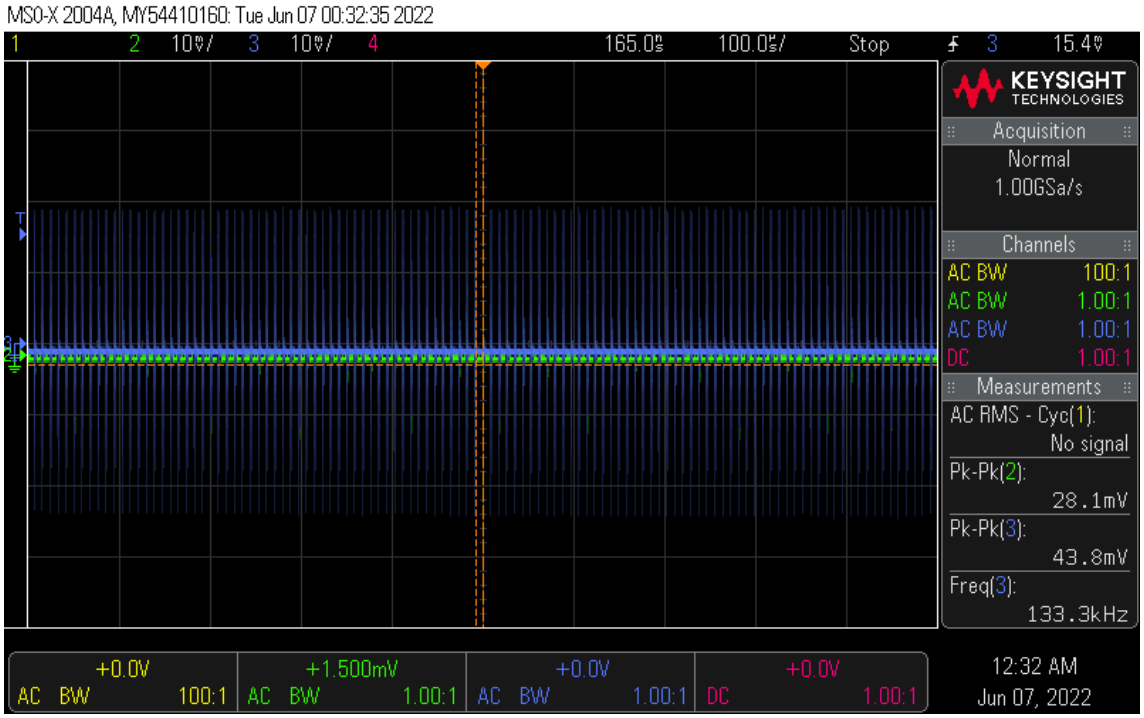

Figure 6.9: $5V$ output (blue) with a load of $1,10A$, supplied by $V_{AC_{min}}$. Green is the unloaded $12V$ output.

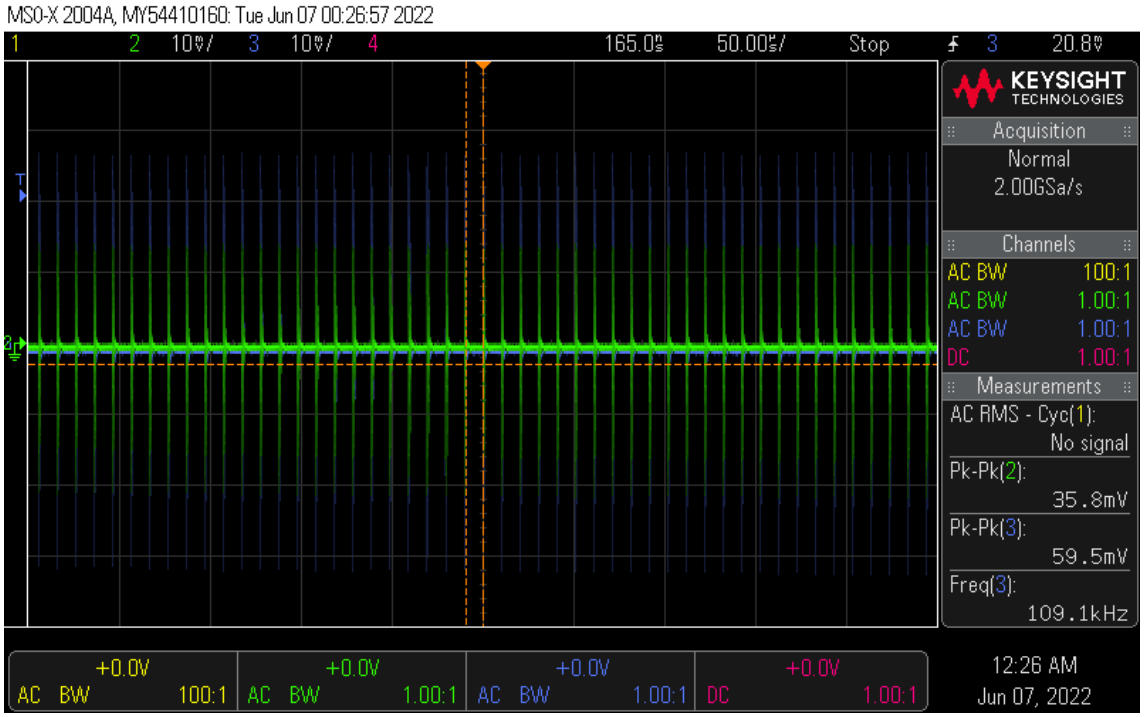

Figure 6.10: $5V$ output (blue) with a load of $1,10A$, supplied by $262V_{rms}$. Green is the unloaded $12V$ output.

Notable in the figures is the frequency of the voltage spikes. Both outputs transients correlate, and the frequency is a plausible frequency of the transformer's

switching.

Likewise the results from the measurements of the $12V$ output are presented in Fig. 6.11 and Fig. 6.12.

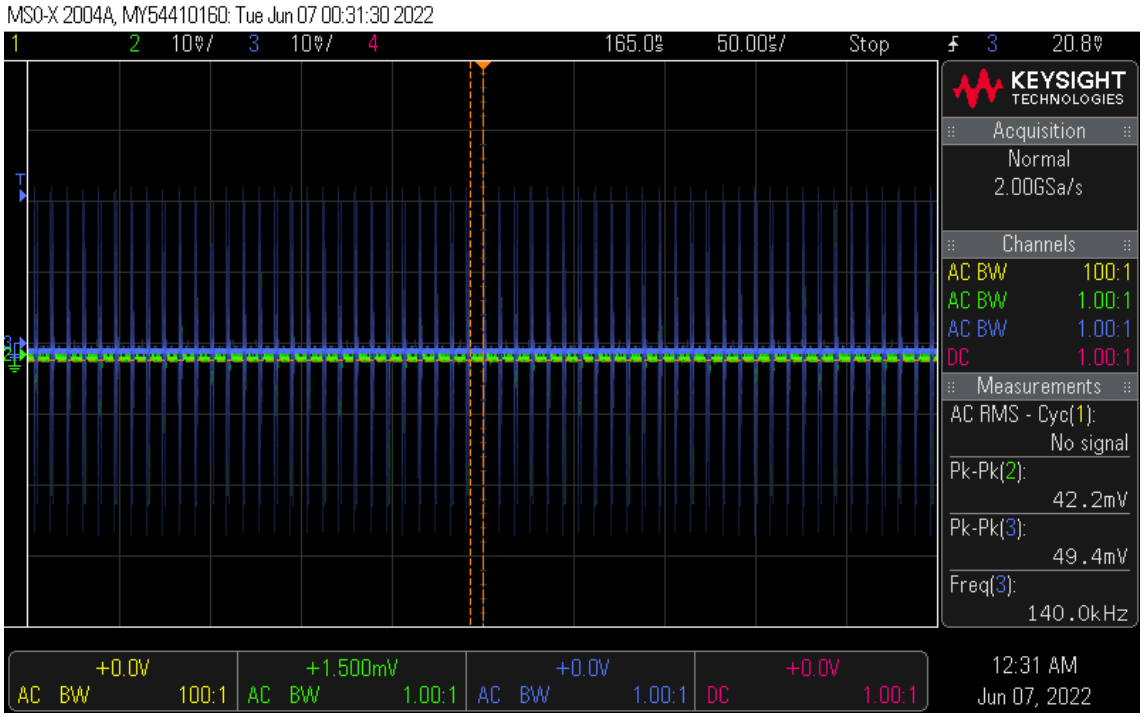

Figure 6.11: $12V$ output (green) with a load of $0,70A$, supplied by $V_{AC_{min}}$. Blue is the unloaded $5V$ output.

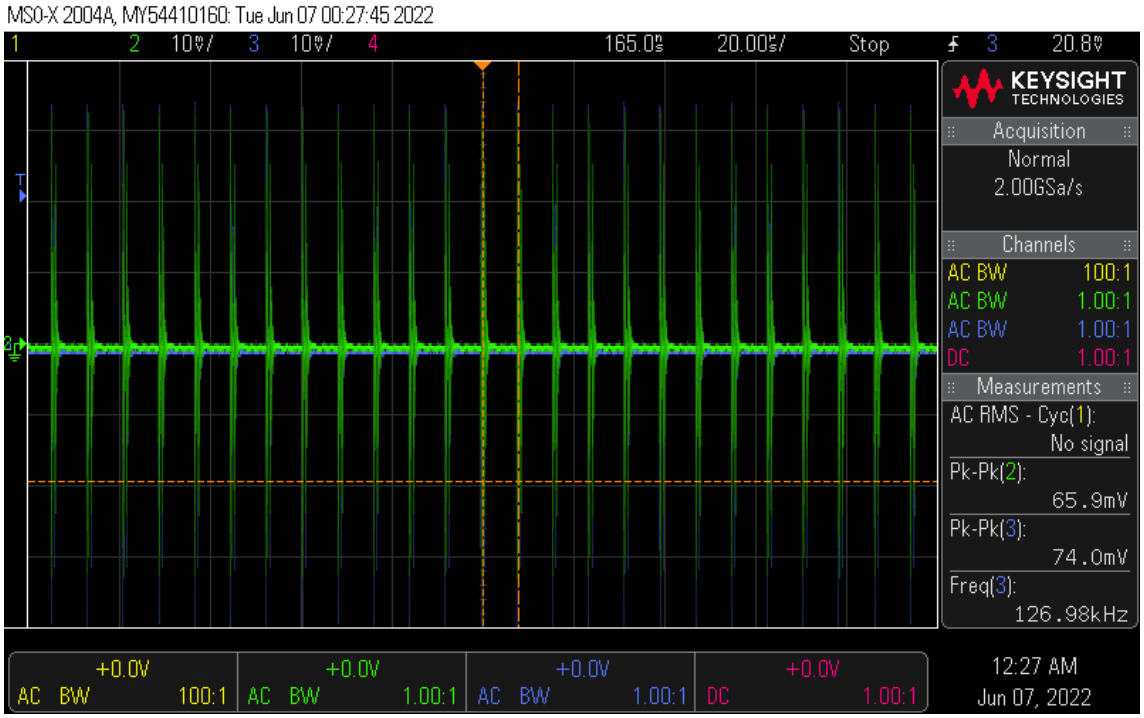

Figure 6.12: $12V$ output (green) with a load of $0,90A$, supplied by $262V_{rms}$. Blue is the unloaded $5V$ output.

Noteworthy here is that the $12V$ output was unable to support a load of $0,90A$ when supplied with $V_{AC_{min}}$. Instead, the load had to be decreased to $0,70A$. The same conclusion regarding the transient frequencies can be taken as before with the $5V$ measurements.

The results of the ripple and transients measurements are compiled in Table 6.2.

Table 6.2: Ripple and transient measurement results

Output loaded	$5V$	$5V$	$12V$	$12V$
AC voltage Supply	$V_{AC_{min}}$	$262V_{rms}$	$V_{AC_{min}}$	$262V_{rms}$
Load	$1,10A$	$1,10A$	$0,70A$	$0,90A$
$5V$ output transient amplitude	$43,8mV_{pp}$	$59,5mV_{pp}$	$49,4mV_{pp}$	$74,0mV_{pp}$
$12V$ output transient amplitude	$28,1mV_{pp}$	$35,8mV_{pp}$	$42,2mV_{pp}$	$65,9mV_{pp}$
Transient frequency	133,3kHz	109,1kHz	140,0kHz	127,0kHz

7
Conclusion

Based on the verification measurements done, the SMPS outputs display mostly transients, which are most likely residues from the switching of the high-frequency transformer. This is believed due to the similarities of the frequencies and that the transients from both the outputs directly correlate.

Another noticeable behaviour of the SMPS is the current capabilities. The achievable current throughput from the outputs was less than the specified requirements. This is most likely an effect of the transformer chosen, as the primary inductance is significantly less than the calculated required value. This was due to an early miscalculation, and when it was discovered it was deemed too late to redesign to fit a new one. The voltage drop evident when loading the outputs is likely correlated to the transformer chosen as well.

In conclusion, all specified objectives but the M404 BL-SL power needs were fulfilled. The next phase of the project is the DVT stage. This includes further optimization of the design and the introduction of new requirements, based on the intended operation environment, stress and EMI.

7.1 Future improvements

The constructed prototype shows many opportunities for improvements. The most obvious is the current capabilities, which do not meet the requirements. Most likely, as discussed before, this is a consequence of the mismatched transformer. It would be interesting to explore the results with a more fitting transformer with higher primary inductance.

Also, the relation between the reflection voltage V_r and the duty cycle D_{max} could be further researched, as a maximal duty cycle of $0,29$ seems low.

Another distinct possibility for enhancement is the transients present on the output. Further measurements are necessary to confirm they are in fact transformer switching residuals. With improved output filtering these transients are estimated to diminish.

The drawback with a multiple output SMPS where both outputs are sensed and shares one feedback point, is that neither of the outputs will be as tightly regulated as if one output had all feedback to itself. Though improvements for this exist, some examples are stacked transformer windings or stacked outputs. One such improvement for the cross-regulation has already been implemented, the output Zener diode.

Depending on the intended use of the SMPS this may not matter, but in use cases

where the demand for stability and low ripple is significant post-regulation may be necessary, or even a completely different topology.

Another future improvement is the PCB itself, which today is influenced by but not completely conforming to IEC standards, due to time constraints. This may be necessary if the SMPS is to be put into production. Also, as no size restraint existed when designing the PCB, an obvious future enhancement is to reduce the size. This task may also allow for optimization of the component placement and make current and feedback loops smaller, which may increase the performance of the SMPS in many categories such as EMI and voltage regulation.

The voltage regulation will likely be improved by improving the feedback circuitry, more specifically the voltage reference. Further analysis of the instability is likely needed to pinpoint the exact reason and thus the most optimal solution.

To improve manufacturability it may be necessary to consolidate the BOM, i.e. reduce the number of unique components and optimize so that more components have the same values. The value of doing this is that it may streamline the component sourcing and decrease the unit cost, as generally with larger quantity orders the price-per-unit drops.

Finally, an important factor today is the environmental impact of the SMPS. To lessen this a straightforward advancement is to increase the efficiency of the SMPS. In the present state, the SMPS displays efficiencies of $68 - 87\%$, depending on the load applied, which shows a margin for improvement exists.

Likely previous mentioned upgrades, such as the transformer, will raise the efficiency but more possibilities exist. One is to add power factor correction on the primary AC side.

Interestingly the SMPS displayed a considerable low standby power consumption of 75mW when unloaded, which is an important environmental criterion when evaluating SMPS that is constantly getting stricter.

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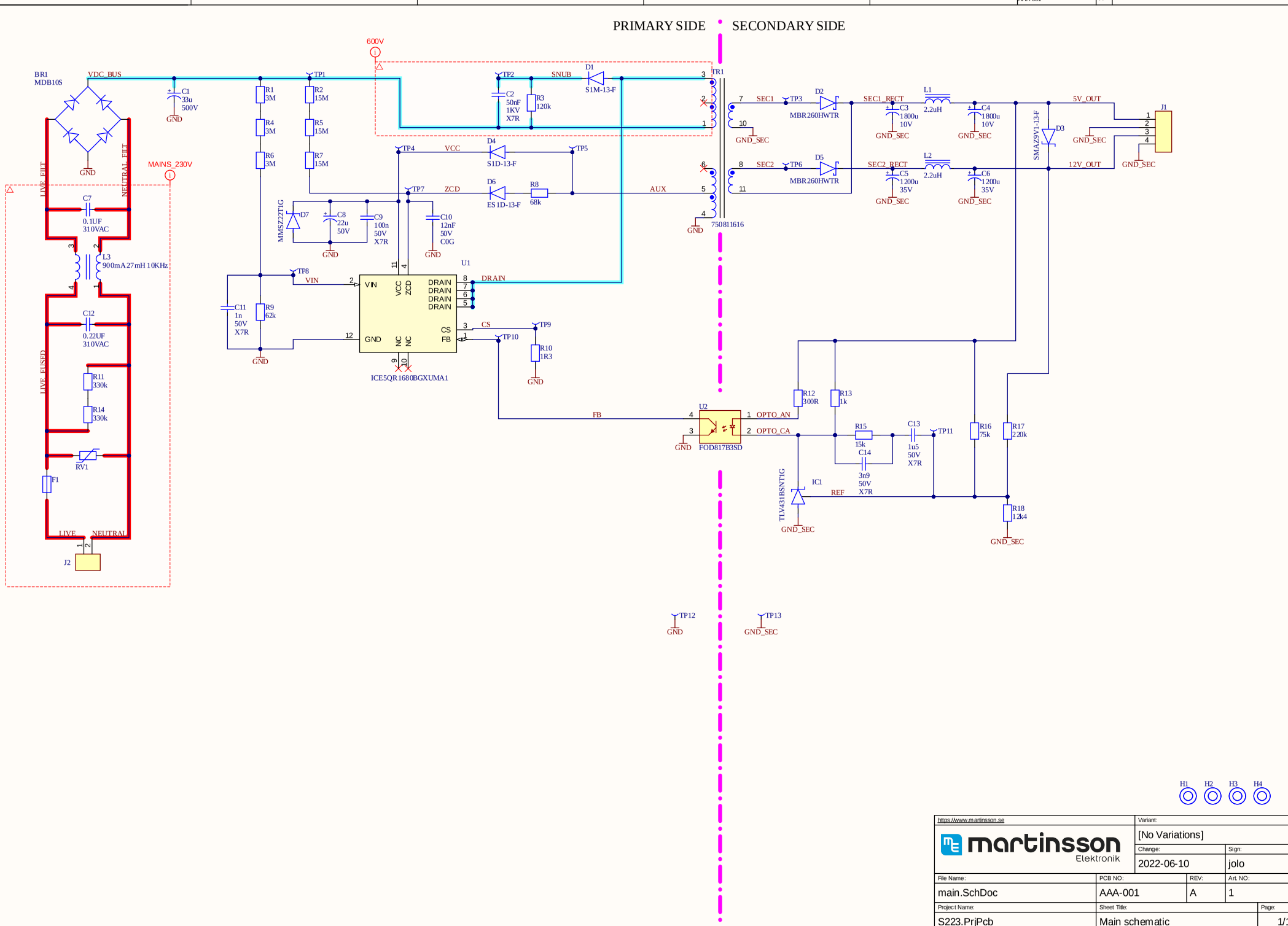
A

Appendix 1



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S223.PrjPcb	Main schematic		1/1

B

Appendix 2

Designator	Quantity	Value	Voltage	Description	Manufacturer A	Manufacturer Part Number A
BR1	1			BRIDGE RECT 1KV 1A 4-MICRODIP	onsemi	MDB10S
C1	1	33u	500V	33 µF 500V 10000 Hrs @ 105°C	Rubycon	500LXW33MEFR18X20
C2	1	50nF	1KV	CAP CER 330p 1KV X7R 1206		
C3, C4	2	1800u	10V	1800 µF 10V 10000 Hrs @ 105°C	Rubycon	10ZLH1800MEFC10X20
C5, C6	2	1200u	35V	1200 µF 35V 10000 Hrs @ 105°C	Rubycon	35ZLH1200MEFC12.5X25
C7	1	0.1UF	310VAC	X2 FILM 0.1UF 10% 310VAC RAD	Würth Elektronik	890334023023CS
C8	1	22u	50V	Capacitor 22u 50V P2 D5 H12.5 5000 Hrs @ 105°C	Rubycon	50YXJ22MTA5X11
C9	1	100n	50V	CAP CER 100n 50V X7R 0603		
C10	1	12nF	50V	CAP CER 1p5 50V C0G 0603		
C11	1	1n	50V	CAP CER 1n 50V X7R 0603		
C12	1	0.22UF	310VAC	X2 FILM 0.22UF 10% 310VAC RAD	Würth Elektronik	890334023028
C13	1	1u5	50V	CAP CER 22n 50V X7R 0603		
C14	1	3n9	50V	CAP CER 1n 50V X7R 0603		
D1	1			Rectifier 1KV 1A SMA	Diodes Incorporated	S1M-13-F
D2, D5	2			SCHOTTKY 60V 2A SOD123 660 mV	SMC Diode Solutions	MBR260HWTR
D3	1			Zener 9.1V 1W SMA	Diodes Incorporated	SMAZ9V1-13-F
D4	1			Rectifier 200V 1A SMA	Diodes Incorporated	S1D-13-F
D6	1			Rectifier Fast Rec 25ns 200V 1A SMA	Diodes Incorporated	ES1D-13-F
D7	1			Zener 22V 5% 500mW	onsemi	MMSZ22T1G
F1	1			Fuseholder 5x20 mm	Wurth	696101000002
IC1	1			VREF SHUNT ADJ 0.5% TSOP5	onsemi	TLV431BSNT1G
J1	1			01x04 3053 Vertical P3.81mm	Wurth Elektronik	691305330004
J2	1			01x02 311 Vertical P5.08mm	Wurth Elektronik	691311500102
L1, L2	2	2.2uH		FIXED IND 2.2UH 4.7A 28.6MOHM	TDK	VLS5045EX-2R2N
L3	1	900mA 27mH 10KHz		CMC 900mA 27mH@10KHz DCR 770mOhm	EPCOS	B82732F2901B001
R1, R4, R6	3	3M		RES 3M 1% 1206		
R2, R5, R7	3	15M		RES 15M 5% 1206		
R3	1	120k		RES 180k 1% 2W 2512		
R8	1	68k		RES 40k2 1% 0603		
R9	1	62k		RES 62k 1% 1206		
R10	1	1R3		RES 1R5 1% 1206		
R11, R14	2	330k		RES 330k 1% 1206		
R12	1	300R		RES 470R 1% 0603		
R13	1	1k		RES 10k 1% 0603		
R15	1	15k		RES 75k 1% 0603		
R16	1	75k		RES 60k4 1% 0603		
R17	1	220k		RES 174k 1% 0603		
R18	1	12k4		RES 10k 1% 0603		
RV1	1			MOV 275VAC 10A	Bourns	MOV-07D431KTR
TR1	1			Flyback transformer 68-170kHz 265VAC 12VAC 2A 5VAC 1.7A	Wurth Elektronik	750811616
U1	1			Offline Flyback VDS 800V RDS 1R53 27W	Infineon	ICE5QR1680BGXUMA1
U2	1			OPTOISOLATOR 5KV TRANSISTOR 4SMD	onsemi	FOD817B3SD

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