CHALMERS
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A High Efficiency and Wideband Doherty Power Amplifier for 5G

Master's thesis in Wireless, Photonics and Space Engineering

HALIL VOLKAN HUNERLI

Department of Microtechnology and Nanoscience-MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
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Supervisor: Göran Granström, Gotmic AB
Examiner: Christian Fager, Department of Microtechnology and Nanoscience

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Department of Microtechnology and Nanoscience
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

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Abstract

In today's wireless communications, mobile networks need high data rates and low power consumption. For this purpose, novel wideband and energy efficient power amplifiers should be designed. This thesis is concerned with this problem. Doherty Power Amplifiers (DPAs) are popular architectures for obtaining high average efficiency for a large range of output power levels. In this work, a DPA is designed using WIN Semiconductor's 50μm GaAs pHEMT process and a monolithic microwave integrated circuit (MMIC) layout ready for tape-out fabrication in Ka-band is created. In this thesis, a power amplifier consisting of two stages; a DPA and a pre-amlifier for improved gain, is designed and simulated. Main and auxiliary cells of the DPA are fed through an unequal Wilkinson power splitter. The simulations show that peak power added efficiency (PAE) of 40% and gain $>$ 15 dB is achieved for the 26.5-31.5 GHz band. The PAE levels of 26% at 6 dB back-off and 18% at 9 dB back off is achieved at the center frequency of 29 GHz. Output power is larger than 26 dBm for the defined band. These properties make this design a promising candidate for future 5G applications.

Keywords: Doherty, MMIC, power amplifier, high efficiency, GaAs, wideband, Ka band.

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Introduction

1.1 Motivation

In modern wireless communications systems, mobile networks need high data rates and low power consumption. For this purpose, novel wideband and energy efficient power amplifiers should be designed. This thesis is concerned with this problem. Below, we present different aspects of this problem.

In today's wireless communications, the frequency spectrum should be fully utilized to be able to support high data rates. In limited bandwidth systems, this is done by the variable modulation methods that result in high peak-to-average ratio signals, which need significant back-off levels for linear operation [1]. This scheme is not always suitable for using traditional power amplifiers (PA) because the PA should be designed so that it can handle the peak power level while, in general, it needs to work at a much lower average output power [2]. The efficiency curve for a traditional PA peaks close to the compression point and drops drastically at back-off levels, which will be the main region for linear operation [3]. The main reason for this efficiency drop is constant energy use through DC biasing even if the input RF signal is very low. The solution to the problem is to use efficiency enhancement techniques that will increase the efficiency at back-off power levels as well.

Another important concern in wireless system design is power consumption. The PA is one of the most important components in the transmitter architecture and usually the most power consuming device. In radio base stations, under maximum load, PA power consumption is more than half the DC power consumption of the whole system [4]. In addition to heat related performance problems, high power systems that work in back-off levels also increase the system complexity [5]. Hence, there is also a significant need for designing power efficient PAs.

Several techniques have been proposed for enhancing the efficiency in back-off, such as, RF-pulse modulation, envelope tracking and dynamic load modulation [6–10]. An example to the latter is Doherty PAs, which has the simplest topology among these methods. It also does not need external circuitry to control the efficiency, hence is self sufficient. For this reason, Doherty PAs are attractive design choices for PA research.

With increasing frequencies, monolithic microwave integrated circuits (MMICs) become more practical to use. MMIC design comes with its advantages and disadvantages. When the frequency is higher than a few GHz, in general both passive and active components become harder to model accurately. On the other hand, using MMIC design, components can be modeled with good accuracy since whole manu-

facturing process can be controlled [11]. Generally MMIC fabrication foundries have component models valid up to a certain frequency point. For frequencies exceeding this point, component models should be extracted and verified manually utilizing measurements. Another down side is the high cost per unit for low volume production. Nevertheless, due to the above advantages MMICs provide promising design choices.

1.2 Aim

The goal of the thesis is to provide a design of Doherty PA operating in 28-30 GHz band with specifications given in Table 1.1, intended for radio links and other communication applications. Achieving these requirements are not straightforward and needs several considerations due to trade-offs between gain, output power and power added efficiency (PAE). It is also worthwhile to mention that the junction temperature specification at high ambient temperature puts a cap for the transistor size.

An MMIC implementation based on Win Semiconductor's pp10-10 process is used during the design. During the design, different operation conditions such as changing bias points and heat are considered. A layout is prepared for the purpose of tape-out creation, fabrication and measurement.

Frequency Range	28-30 GHz	
Gain	15 dB	
Output Power	P_{1dB}: well behaving	$P_{SAT} \geq 26$ dBm
PAE	$> 20\%$ @ P_{SAT}	
	$> 20\%$ @ 3 dB back-off	
	$> 15\%$ @ 6 dB back-off	
	$> 10\%$ @ 9 dB back-off	
Junction Temperature	$T_j < 150°C$ at P_{SAT}	$T_a = 85°C$
Power Dissipation	$<$ 2W @ P_{SAT}	

Table 1.1: Specifications of the targeted amplifier.

1.3 Thesis Outline

Chapter 2 provides a brief theory of traditional power amplifier classes and efficiency enhancement methods. Then, the fundamental theory of Doherty power amplifiers are discussed including combining networks. Chapter 3 presents the proposed designs and explains the design flow of the Doherty PA composed of main and auxiliary cells. For each cell, load pulling and matching network designs are presented. In addition, theory and design of unequal Wilkinson power splitter along with realization of combiner network is given. In Chapter 4, performance evaluation of the proposed designs are presented. Finally in Chapter 5, the thesis is concluded with discussions and presentation of future work.

2

Theory

In this chapter, different PA classes/topologies will be discussed. First, expressions for gain, output power and efficiency will be derived. Then, an explanation of the traditional PA classes will be given. Then, efficiency enhancement methods will be discussed. Finally, Doherty PA fundamental theory will be presented.

2.1 Power Amplifier Basics

Power amplifiers are used to amplify the signal to a desired output power level. Designing a PA needs consideration of several properties at the same time. The main challenge here is getting high efficiency, bandwidth and gain while preserving the linearity. These properties are given as requirements in most of the modern systems. This needs careful consideration of the trade-off between these parameters since improving any of these parameters typically results in performance loss in others. These parameters are discussed in the following sections.

2.1.1 Gain

Power gain of an amplifier is defined as the ratio of its output power to input power. In communications systems, amplifiers are typically used to increase the signal level to the required level in transmitters. Due to the nonlinearities inside the amplifier, the gain of an amplifier goes into compression when a large signal is fed into it. Due to this phenomena, P_{1dB} and P_{SAT} values are defined to characterize the linearity of the amplifier. In a transmitter more than one amplifier may be used to obtain a higher gain.

2.1.2 Output Power

Input and output matching should be done in different ways for maximum small signal gain, low noise level and maximum output power. For maximum gain, simultaneous conjugate matching is needed i.e. $\Gamma_S = \Gamma_{in}^*$ and $\Gamma_L = \Gamma_{out}^*$. For a minimum noise design, input of the active device is matched to an optimum value while output is conjugate matched, i.e $\Gamma_S = \Gamma_{OPT}^*$ and $\Gamma_L = \Gamma_{out}^*$. PA design requires a different approach. For a large input signal, output signal power is not maximized by conjugate of drain to source impedance which only maximizes the small signal power gain. To achieve higher power levels, both current and voltage swings should

be taken into account. Optimum load for this case is defined by "Cripps load"

$$R_{opt} = \frac{V_{max} - V_k}{I_{max}} \tag{2.1}$$

A representation of comparison between power sweeps for maximum gain and maximum power matches can be seen in Figure 2.1.

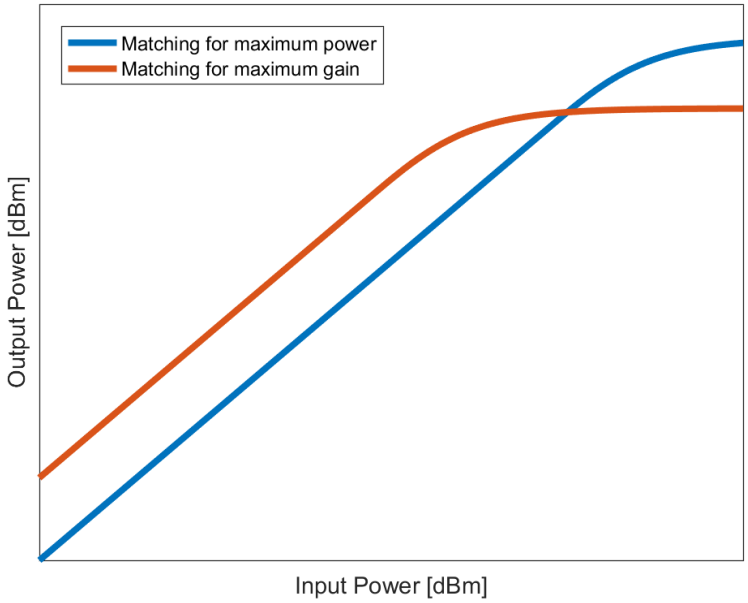

Figure 2.1: Power sweep comparison between small signal matching vs power amplifier matching

2.1.3 Efficiency

One of the highest energy consuming components in a transmitter circuit is the PA. Even though peak efficiency of an amplifier may be high, this number usually drops fast at back-off values. The PA should be designed using additional techniques for the PA to work efficiently at back-off levels as well. The efficiency of a PA can be described in terms of energy balance. To have the highest efficiency, heat dissipation should be minimum. Also the overlap between voltage and current and the power delivered to the harmonics causes the efficiency to drop.

Efficiency can be numerically represented using either drain efficiency or power added efficiency. Drain efficiency is defined as

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

Another way to represent the efficiency is to include the input power in the equation. This approach becomes particularly suitable when the gain of the PA is relatively low. Power added efficiency is defined as follows

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} = \eta(1 - \frac{1}{Gain}). \tag{2.3}$$

2.2 Traditional PA Classes

Power amplifiers can be divided into two in terms of operation mode: transconductance-mode and switch-mode. The difference between them is the drain current and voltage waveforms, the latter having never overlapping current and voltage. Switch-mode amplifiers are hard to model at GHz frequencies because the device does not sweep through its linear region fast enough to behave like a switch [3]. The traditional classes; A, B, AB and C are transconductance-mode PAs with different conduction angles. Each of these classes are explained next.

2.2.1 Class A

This class of PAs have a conduction angle of 2π, which means that the transistor is conducting during the whole period of the input signal. DC current and voltage is biased in the middle of the DC maximums and minimums to ensure conduction at all times as seen in Figure 2.2. The resulting load line is represented with the red line on the same figure. The response of a class A amplifier can be well approximated by a linear function until it reaches its compression point. This class also has high gain and low distortion. The main drawback is the low efficiency due to DC power consumption even when there is no RF input signal. The efficiency is calculated using DC and RF powers. In ideal case,

$$P_{DC} = \frac{I_{max}V_{max}}{4} \tag{2.4}$$

$$P_{out} = \frac{I_{out}V_{out}}{2} = \frac{I_{max}V_{max}}{8} \tag{2.5}$$

Then the maximum efficiency can be calculated using (2.2) as 0.5. This value drops even more for the non-ideal case due to the knee voltage further limiting P_{out}.

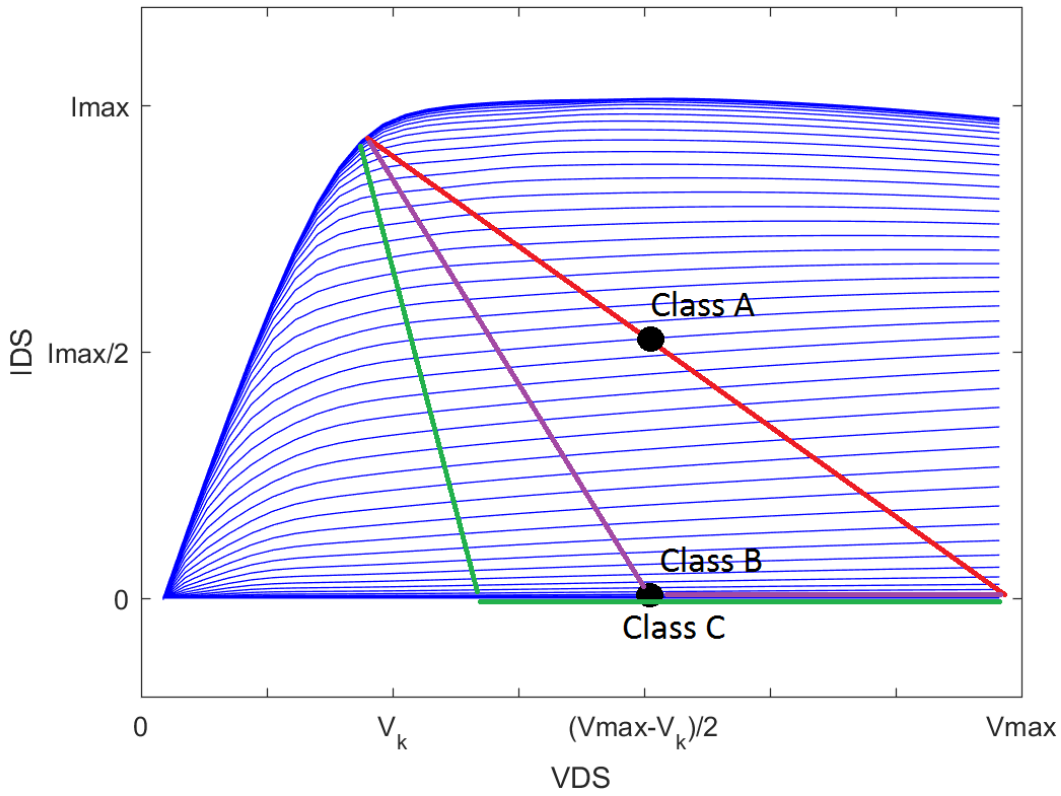

Figure 2.2: Bias points and load lines for different power amplifier classes.

2.2.2 Class B

Class B amplifier has a conduction angle of π, so the transistor conducts during half of the input signal's cycle. This is accomplished by biasing the transistor at the pinch-off as seen in Figure 2.2. Its resulting load line is represented with purple line on the same figure. It has both advantages and disadvantages when compared to a class A PA. While its efficiency is higher, it loses some linearity due to increased harmonic content. To achieve a class B waveform, the harmonics should be filtered from the output by a short circuit. For a class B PA, the bias point changes to $I_{DC} = I_{max}/\pi$ and $V_{DC} = V_{max}/2$ so the DC power becomes

$$P_{DC} = \frac{I_{max}V_{max}}{2\pi} \tag{2.6}$$

When the same input power level is used, output power for a class B bias condition results in 1/4th of class A biasing. This means that theoretically the gain is also 6 dB lower than class A. Using equations (2.2) and (2.5), the ideal drain efficiency for a class B PA can be found to be $\pi/4 = 78.5\%$.

2.2.3 Class AB

Class AB has conduction angle between π and 2π. The transistor is biased somewhere between Class A bias point and cut-off point. Similar to the class B, this class

also have some harmonic content but its efficiency is higher than a class A both at peak and backed-off values. Large set of bias points means a freedom of choice for either linearity or a higher efficiency. Since the conduction angle is a variable for this class, a more general bias point equation for the current can be given by [3]

$$I_{DC} = \frac{I_{max}}{2\pi} \cdot \frac{2\sin\alpha/2 - \alpha\cos\alpha/2}{1 - \cos\alpha/2} \tag{2.7}$$

Similarly, 1^{st} order output current waveform is given by

$$I_1 = \frac{I_{max}}{2\pi} \frac{\alpha - \sin\alpha}{1 - \cos\alpha/2} \tag{2.8}$$

Figure 2.3 provides a plot of these currents versus conduction angle. Another important aspect of the conduction angle is its effect on the efficiency and the output power. Since $P_{out} = V_{DC}I_1/2$ for the first harmonic output power, we can state the following

$$P_{out} \propto \frac{\alpha - \sin\alpha}{1 - \cos\alpha/2} \tag{2.9}$$

Drain efficiency is then given by

$$\eta = \frac{I_1}{2I_{DC}} = \frac{1}{4} \cdot \frac{\alpha - \sin\alpha}{\sin\alpha/2 - \alpha/2\cos\alpha/2} \tag{2.10}$$

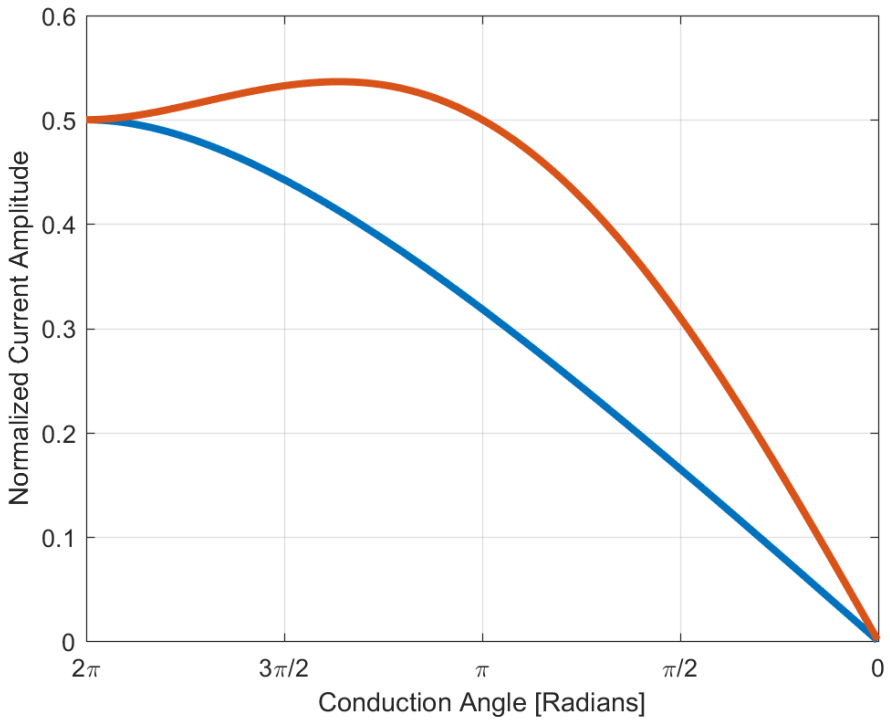

Figure 2.3: Normalized DC (blue) and fundamental (red) currents versus conduction angle

A plot of the normalized output power and the drain efficiency as a function of conduction angle can be seen in Figure 2.4. As seen in the figure, the output power peaks around 245° in class AB region. Another important thing to note is that when the conduction angle goes to zero, output power drops to zero while efficiency increases. Mostly a bias point close to the pinch-off is used since conduction angle becomes closer to π and odd harmonics become smaller.

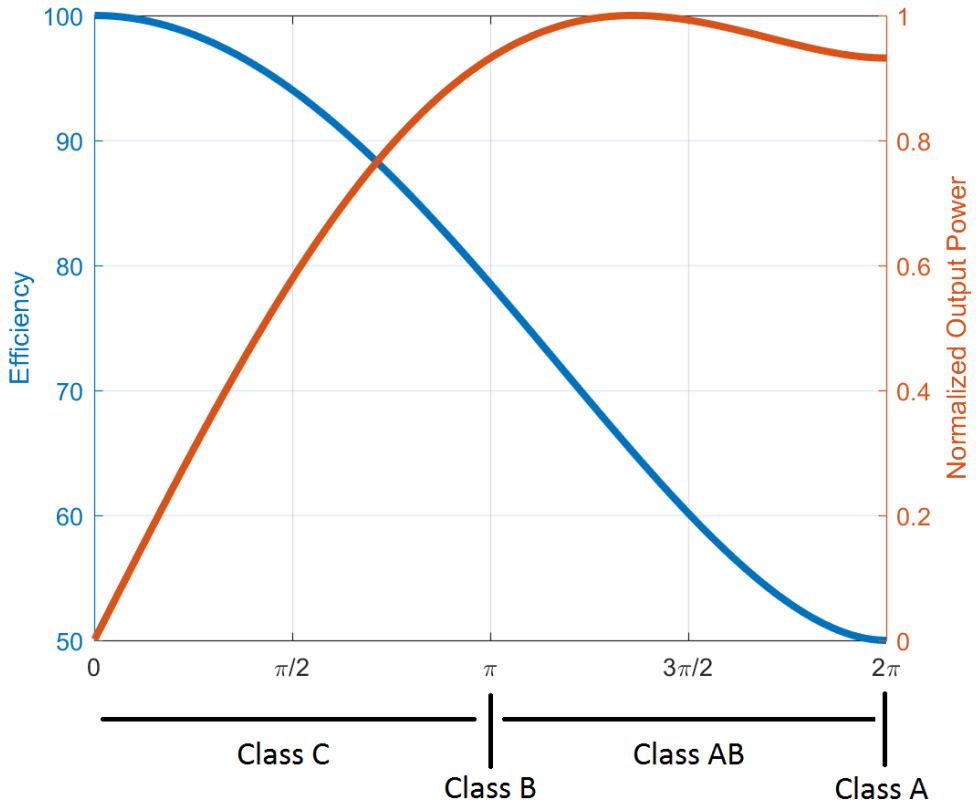

Figure 2.4: Drain efficiency (blue) and normalized output power (red) versus conduction angle

2.2.4 Class C

A class C device is biased below the pinch-off level so that it conducts less than 50% of the time. The conduction angle is less than π resulting in higher efficiency when compared to other classes discussed so far. Its load line is represented with the green line on Figure 2.2. It also has the lower gain and power output in addition to the higher harmonics which makes it highly nonlinear. Lower gain means that the device should be driven heavily which in turn decreases the power added efficiency. Similar to a class B amplifier, the harmonics should be shorted out at the output to achieve a class C waveform. Relative power and efficiency level to other classes can be seen in Figure 2.4.

One issue when using a transistor in class C mode is large negative voltage swings at the input due to small conduction angles. This creates an even higher voltage difference between gate and drain since drain is subjected to high output voltage

peaks. Combination of input and output voltage swings may send the device to breakdown if the PA is not designed considering this effect.

2.3 Efficiency Enhancement Methods

Traditional PA classes operate at their maximum efficiency at a single power level usually close to their saturation levels. Working at these levels causes signal distortion due to operation at nonlinear region. One way to decrease this distortion is using linearization techniques, which is out of scope of this work. An alternative way to get rid of this distortion is to operate the PA at backed-off power levels but this in turn decreases the efficiency significantly. Hence methods to increase the efficiency at back-off power levels have been developed. Two common categories for enhancing the efficiency are dynamic supply modulation (DSM) and dynamic load modulation (DLM). These methods can be implemented using PA's operating in any class. We now look into these methods more closely.

DSM is an efficiency enhancement method where the drain bias is dynamically reduced when the transistor drive level is backed-off. Efficiency is kept at a high level using the fact that (2.2) tries to keep the ratio of P_{out}/P_{DC} constant. It should be kept in mind that the load lines of different bias points will be different than the ideal case and this will cause the efficiency to be lower than the maximum available value. One possible implementation of this method is using envelope tracking. Here V_{DS} is made proportional to the drive level by dynamically modulating it along with the input signal, which is both amplitude and phase modulated. [12, 13] An important drawback of DSM is that an external circuit, like another amplifier connected to drain, is needed. This amplifier also consumes power and this decreases the overall efficiency. Additionally, it should be designed to work for a larger bandwidth than the actual amplifier since the envelope has a much wider bandwidth than the signal itself.

DLM method theoretically frees the efficiency from the dependence on the drive level. This is made possible by dynamically increasing the load impedance (R_L) when the transistor is backed-off. In reality the drain efficiency is also dependent on R_P and C_{ds} of the transistor along with operating frequency so the efficiency enhancement becomes limited at the backed-off levels [14, 15]. There are two major types of DLM; varactor-based and active load modulation based. The first one uses varactors to tune the load. The latter uses active current injection to modulate the load of the transistor. An example to active load modulation based DLM technique is Doherty PA implementation. This technique will be discussed in more detail in the next section.

2.4 Doherty Power Amplifiers

Due to its low complexity, a very popular DLM method is Doherty PA (DPA). It was first introduced in 1936 using vacuum tubes as active elements [16]. Since then, the concept has been applied to modern wireless communication systems extensively. The original application focuses on a specific configuration where the efficiency peaks

at 6 dB back-off. Extensive studies were done on further increasing back-off level [17–22] and bandwidth [23–27].

Classical topology of a DPA consists of a main transistor and an auxiliary transistor. Operation principle is basically modifying the resistance/reactance of the main amplifier by injecting phase coherent current from the auxiliary amplifier. A better way to define this method is active load-pulling [3]. Usually a class B or a deep AB amplifier is used as the main amplifier while a class C amplifier is used for the auxiliary amplifier. Ideally, the auxiliary amplifier is expected to be off for the power levels lower than the designed back-off level. When it is turned on, it acts as an active current source, dynamically decreasing the main amplifier's load. As a result, the maximum voltage swing and efficiency is maintained, which in turn increases the output power. The final output power is the combined power of these two devices.

In a conventional DPA, output power is delivered after a combining network consisting of a quarter-wave transformer and a resistive load. This network results in a 90 degrees phase delay requirement at the input. Figure 2.5 shows this architecture. The characteristic impedance of the quarter-wave transformer and load are obtained during the design of main and auxiliary amplifiers.

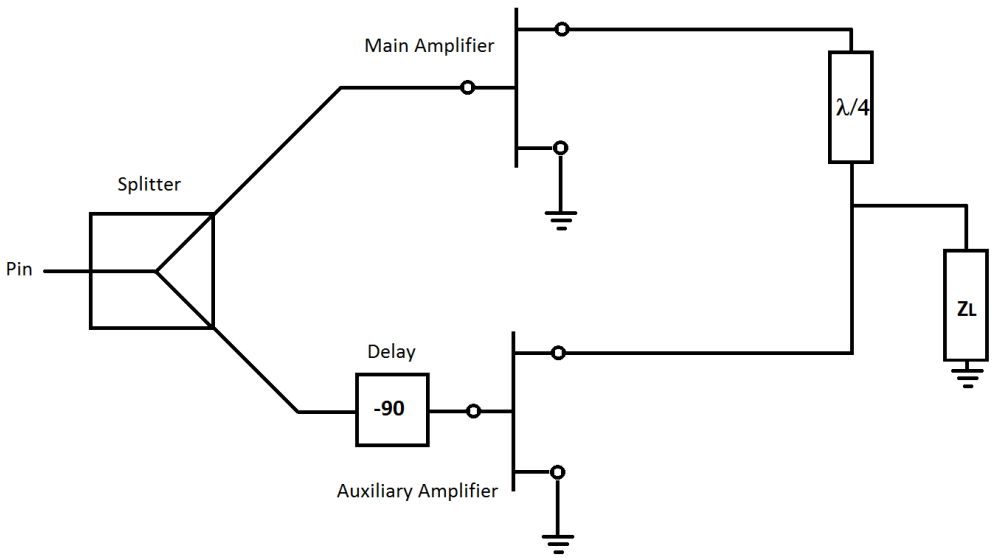

Figure 2.5: Conventional DPA Topology

For the ideal case, voltage and currents of main and auxiliary amplifiers can be given by V_m, I_m, V_a and I_a. The relations between the currents of DPA can be given by [28]

$$\left|I_a|_{\beta=1}\right| = \left(\frac{1}{\beta_{bo}} - 1\right)\left|I_m|_{\beta=1}\right|, \tag{2.11}$$

$$\left|I_a|_{\beta=\beta_{bo}}\right| = 0, \tag{2.12}$$

$$\angle I_a/I_m = -90°. \tag{2.13}$$

Here β is the normalized voltage drive level and β_{bo} is the intended drive level where the auxiliary amplifier is turned on. In Figure 2.5, the characteristic impedance of the $\lambda/4$ transmission line should be the same as optimum load resistance (R_{opt}) of the main amplifier. Then the output load impedance becomes

$$Z_L = \beta_{bo} R_{opt}. \tag{2.14}$$

Output power back-off (OPBO) level, γ, relates the power delivered to the load to the power levels of auxiliary and main amplifiers as

$$P_L|_{\beta=1} = P_m|_{\beta=1} + P_a|_{\beta=1} = \gamma P_m|_{\beta=\beta_{bo}} \tag{2.15}$$

where P_m and P_a are the powers of main and auxiliary amplifiers. Voltage and power back-off levels are related to each other with

$$\gamma = \frac{1}{\beta_{bo}^2}. \tag{2.16}$$

The current and voltage profiles of the conventional DPA can be seen in Figure 2.6. Here piece-wise linear approximation is used for simplicity.

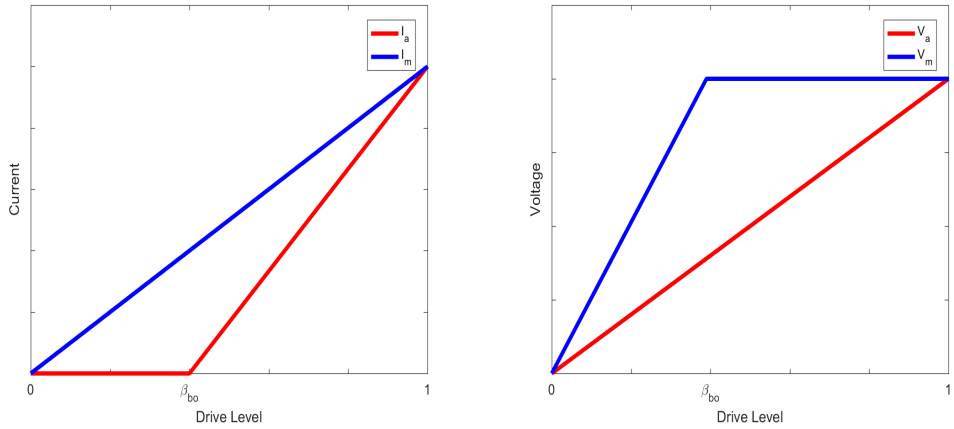

Figure 2.6: Normalized current and voltage versus drive level of the main and auxiliary amplifiers

It is possible to generalize the output combining network by choosing arbitrary back-off level and output power for each transistor. Different methods have been proposed for this purpose but due to its ease of implementation, black box combiner network approach by Ozen et. al. [29] and Halberg et. al. [30] is used in this work. The theoretical background for the design of this network is given next.

2.4.1 Combining Network

Output combining network of the DPA can be represented by a lossy and reciprocal two-port network with the load termination inside or a lossless and reciprocal three-port network with the load termination outside [30]. These network representations can be seen in Figures 2.7 and 2.8.

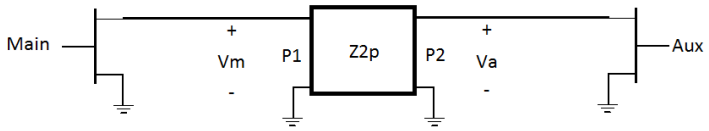

Figure 2.7: Lossy and reciprocal 2-port representation of the combiner network

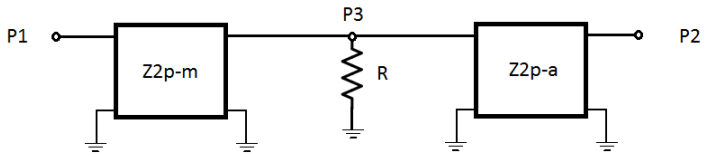

Figure 2.8: Combiner network transformed to two lossless and reciprocal 2-port networks and a termination resistor

For the non-ideal case, when bias points of the main and the auxiliary amplifiers are different, waveforms experience different phase delays on each transistor/cell. In the conventional DPA design, maximum fundamental intrinsic currents $I_{a,i,P_{max}}$, $I_{m,i,P_{max}}$ are related to each other [30], [28]

$$I_{a,i,P_{max}} = (\sqrt{\gamma} - 1) I_{m,i,P_{max}}, \tag{2.17}$$

where γ is the back-off power level. In the black box method, this current ratio is independent of γ

$$I_{a,i,P_{max}} = r_c I_{m,i,P_{max}}, \tag{2.18}$$

where r_c is an arbitrary current ratio. Assuming that the fundamental drain voltage swings at maximum power for the main and auxiliary transistors are equal to each other, the intrinsic power levels can be shown to be related to each other with:

$$P_{a,P_{max}} = r_c P_{m,P_{max}}, \tag{2.19}$$

The **Z** parameters of the lossy, reciprocal two-port network seen in Figure 2.7 can be solved and transformed into lossless, reciprocal three-port using fundamental voltages and currents at the peak power level and the load pull data of the main and auxiliary transistors [29]. These voltages and currents are related to each other with

$$\begin{bmatrix} V_m \\ V_a \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_m \\ I_a \end{bmatrix} \tag{2.20}$$

where $Z_{12} = Z_{21}$ due to reciprocity. These **Z** parameters are found from the following equations: [30]

$$Z_{11} + Z_{12}\alpha_1 = Z_{L,m,P_{max}}, \tag{2.21}$$

$$Z_{22} + Z_{12}/\alpha_1 = Z_{L,a,P_{max}}, \tag{2.22}$$

$$Z_{11} + Z_{12}\alpha_2 = Z_{L,m,P_{bo}}, \tag{2.23}$$

$$Z_{22} + Z_{12}/\alpha_2 = -Z_{off,a}. \tag{2.24}$$

Here Z_L are load impedances of main and auxiliary transistors at maximum power and OPBO (P_{bo}). $Z_{off,a}$ is the output impedance of the auxiliary transistor when it is off. Here α_1 and α_2 are given by

$$\alpha_1 = \frac{I_{a,P_{max}}}{I_{m,P_{max}}} = \sqrt{\frac{\Re\{Z_{L,m,P_{max}}\}P_{a,P_{max}}}{\Re\{Z_{L,a,P_{max}}\}P_{m,P_{max}}}}e^{-j\theta}, \tag{2.25}$$

$$\alpha_2 = \frac{I_{a,P_{bo}}}{I_{m,P_{bo}}} = -\frac{Z_{12}}{Z_{off,a} + Z_{22}}. \tag{2.26}$$

where θ is the phase offset between output currents of main and auxiliary transistors. $Z_{off,a}$ can be found using the small signal S-parameters. Rest of the load impedances can be extracted by transistor load pull simulations or measurements because the analysis presented here can be done both intrinsically and extrinsically. Load pulling will be explained in more detail in the following chapter.

The condition for realization of three-port lossless reciprocal network terminated with a resistive load from the two-port network parameters is given by [29]

$$\Re\{Z_{12}\}^2 = \Re\{Z_{11}\}\Re\{Z_{22}\} \tag{2.27}$$

This condition is satisfied for four different θ values, $\{\pm\theta_x, \pm(\pi - \theta_x)\}$. Solving θ_x analytically is difficult so usually numerical methods are used. Using the roots of equation (2.27) is one method to find θ_x values.

The three-port network shown in Figure 2.8 can be represented as two lossless two-port networks with ABCD parameters T_{2Pm} and T_{2Pa}, each in front of main and auxiliary transistors respectively and a termination resistor R in between. It can be assumed that the ABCD parameters of the two-port lossy network is of the following form:

$$\mathbf{T_{2P}} = \begin{bmatrix} A_r + jA_i & B_r + jB_i \\ C_r + jC_i & D_r + jD_i \end{bmatrix} \tag{2.28}$$

This matrix is composed of the following ABCD matrices:

$$\mathbf{T_{2P}} = \mathbf{T_{2Pm}}\mathbf{T_R}\mathbf{T_{2Pa}}. \tag{2.29}$$

Since the two-port networks T_{2Pm} and T_{2Pa} are lossless and reciprocal, real values can be assigned to the diagonal elements and imaginary values can be assigned to the off-diagonal elements: [29]

$$\mathbf{T_{2P}} = \begin{bmatrix} A_m & jB_m \\ jC_m & D_m \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} A_a & jB_a \\ jC_a & D_a \end{bmatrix} \tag{2.30}$$

The solution set to the equation (2.30) is found to be [29]:

$$B_m = \frac{A_i D_m}{C_r}, \tag{2.31}$$

$$C_m = \frac{C_r - A_m C_r D_m}{A_i D_m}, \tag{2.32}$$

$$D_m = \pm \frac{C_r \sqrt{R} \sqrt{A_i B_i + A_r B_r}}{A_i}, \tag{2.33}$$

$$A_a = \frac{C_r R}{D_m}, \tag{2.34}$$

$$B_a = -\frac{B_r C_r R}{A_i D_m}, \tag{2.35}$$

$$C_a = \frac{A_m C_r^2 R}{A_i D_m^2} - \frac{A_i D_m}{B_r C_r R} + \frac{B_i C_r}{B_r D_m}, \tag{2.36}$$

$$D_a = \frac{C_r (A_i B_i D_m + A_m B_r C_r R)}{A_i^2 D_m^2}, \tag{2.37}$$

This solution set is acquired by choosing A_m as a free design parameter. Lumped element realization is done by converting the ABCD parameters back to **Z** parameters and represent it by either a Π or a T-network for simplicity. For the lowest losses, A_m is chosen to be 1 along with T-network topology for both auxiliary and main networks. This is also important for a more compact design. The realized circuit is of the form seen in Figure 2.9. Using equations (2.31)-(2.37), these lumped element values can be found to be:

$$C_1 = \frac{C_m}{w_0}, \tag{2.38}$$

$$L_1 = \frac{D_m - 1}{C_m w_0}, \tag{2.39}$$

$$C_2 = \frac{C_a}{w_0}, \tag{2.40}$$

$$L_2 = \frac{D_a - 1}{C_a w_0}, \tag{2.41}$$

$$L_3 = \frac{A_a - 1}{C_a w_0}, \tag{2.42}$$

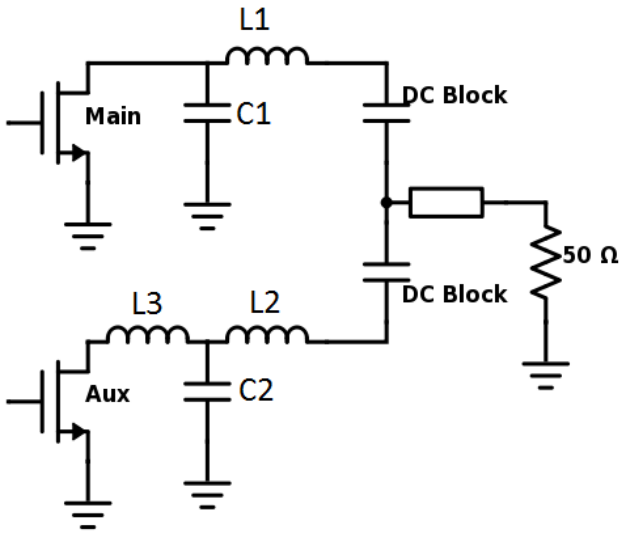

Figure 2.9: Combiner network transformed to lumped circuit elements

The final circuitry may consist of either lumped, distributed or a combination of both depending on the operating frequency and element values.

3

MMIC Doherty Amplifier Design

The specifications of the targeted power amplifier is given in Table 1.1. The frequency range is selected to be in Ka-band given that this bands are among the targeted bands for early deployments of 5G, such as in Korea, Sweden and US [31]. The remaining requirements for the amplifier are all selected to improve the efficiency in back-off while keeping the gain, output power and power dissipation in check when compared to a class AB amplifier.

The amplifier is designed using WIN Semiconductor's pHEMT technology (pp-1010) that uses a 50 μm thick GaAs substrate. Thin substrate may come as an advantage since it enables smaller sized layouts.

3.1 Design Flow

The design of the DPA consists of several steps. These steps are shaped according to the target specifications given in Table 1.1. Realizing these steps need initial analysis of the models provided by Gotmic AB. There are more than one property that requires additional steps to be taken when compared to a basic design. At these frequencies and using the pp1010 technology, getting the P_{SAT} and gain specifications with a single stage is a challenge. This will be more obvious after taking a look at the transistor parameters in the next section.

A summary of the design flow consists of active device selection, in-band stabilization, setting of optimum load and source impedances, designing each cell of the DPA, power splitter and combining network designs and finally the pre-amplifier design.

3.1.1 Transistor Choice

Choosing the size of the two transistors depends on the frequency of operation, power dissipation, gain, temperature and linearity. Output power and gain cannot be maximized at the same time since there is a trade of between them. The transistor models given in Gotmic library are based on Angelov's model [32].

Output power is limited by the power components of main and auxiliary cells fed to the combining network. Although there are more than one option to implement this requirement, initial design trials showed that heat dissipation also becomes an important factor if very large transistors are used. This is important because the excessive heat causes the gain, hence the efficiency to drop significantly. One method to reduce heat problems is using two or more smaller transistors in parallel while

sacrificing some gain. Two 4x50μm or larger transistors in parallel are found to be sufficient to obtain the required output power specification of $P_{SAT} \geq 26$ dBm.

Maximum stable gain curves of different sized transistors versus frequency can be seen in Figures 3.1 for a class A biasing and maximum voltage swing with $V_D = 4$V and $V_G = -0.4$V. These curves also show that the gain of the DPA consisting of only main and auxiliary cells will not be enough to get the required gain specification of 15 dB. Depending on the bias point of the transistors, the gain of the DPA will be between the gain of both cells, so another stage is needed to further amplify the input signal. The design of this pre-amplifier along with main and auxiliary cells will be explained in the following sections.

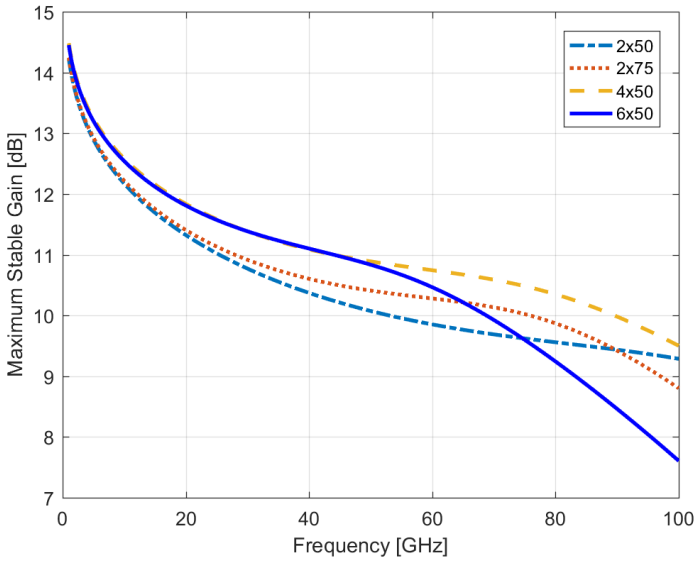

Figure 3.1: Maximum stable gain curves for different sized transistors

3.1.2 Stability Considerations

The stability network of a transistor has to be checked before load pulling since it will modify the behavior of the transistor. An overall picture of the stability network can be seen in Figure 3.2. It is common practice to use a parallel RC circuit at the gate of the transistor. This introduces an out of band series resistance which increases the stability by increasing the real part of Z_{11}. In addition to stability improvement, this network also flattens the gain to some extent. Another parallel resistance (R_p) going towards the DC feed increases low frequency stability by reducing the input impedance. Finally the RF signal is shorted with $\lambda/4$ line and the parallel capacitance, C_p.

The stability network of each transistor in DPA differs due to different bias point. Using more than one transistor in parallel in each cell introduces another problem to the MMIC design. The stability network should feed each transistor equally, which means a symmetrical layout is needed to introduce the RF signal to each gates equally. This can be accomplished by dividing the resistance into two parallel resistors instead. Final layout of stability networks for each DPA cell can be seen in

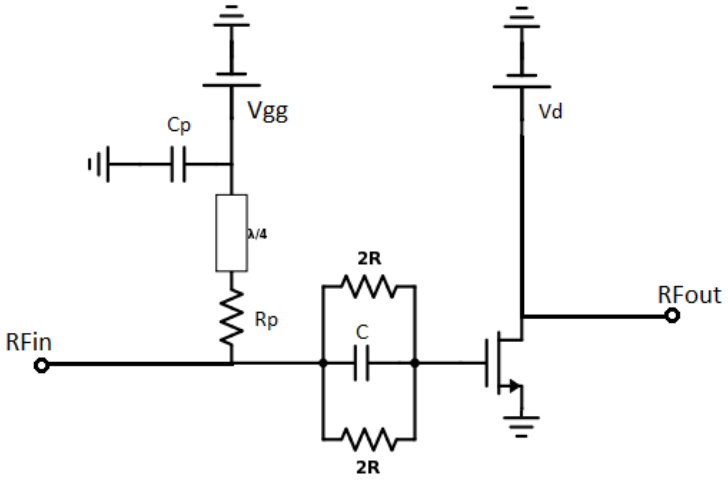

Figure 3.2: Stability network

Figure 3.3. Ports 2 (P2) and 3 (P3) of each network is connected to a 6x50 transistor gate. Port 1 (P1) is connected to DC path and power splitter. The resistors and the capacitor for each cell is tuned to the values seen in 3.3 by keeping the gain high while keeping an eye at the stability factor. Both cells are unconditionally stable from DC to 100 GHz.

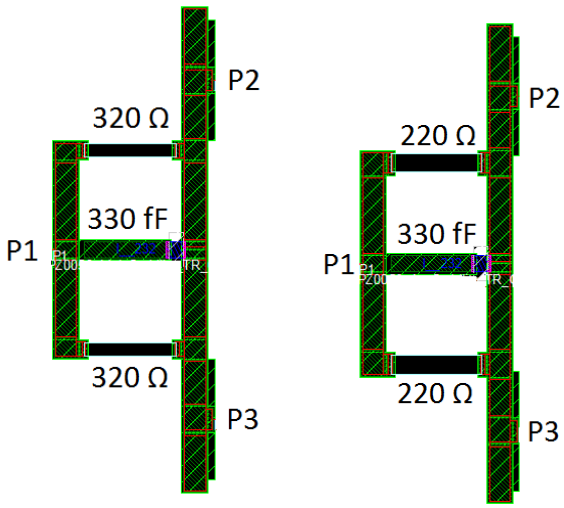

Figure 3.3: Stability networks for main (left) and auxiliary (right) transistors

3.1.3 Load Pulling

Load pull simulations are needed to determine the operation of the transistor at required power, gain and efficiency. It is important to add stability network before performing load pulling. It should be noted that DC bias networks of each transistor also introduce, even if minimal, performance degradation hence s-parameter

modification to the system. The load pulling tool of ADS is used to extract the possible load and source impedances to satisfy the DPA requirements. The basic principle of load pulling is varying the impedance presented to the active device in order to find power, gain and efficiency at each impedance point simulated. This impedance sweep is used to find the best matching impedances for both input and output. These values then will be used to design input matching networks and the combining network. Implementation of this will be shown for main and auxiliary cells in the following sections.

3.2 Main Amplifier Design

The main amplifier is biased such that gain is kept at high level while keeping the efficiency maximized. Practically it is implemented with a class B or deep class AB biasing. Another important factor is looking out for high voltage swings that could result in voltage break-down. The most probable voltage swing to cause break-down is gate-to-drain voltage. Finding the optimum bias point that will give the best result is an iterative process. The foundry's tech-specifications give the break-down voltage (V_{br}) value as 9 volts on average and pinch-off voltage as -0.95 volts. After the iteration process, the bias point is chosen to be $V_{DS} = 3V$ and $V_{GS} = -0.8V$.

3.2.1 Load Pulling

In order to extract the parameters needed for the combining network given in (2.21) to (2.24), load pulling should be performed for both saturation and back-off power levels of the main cell. Load pulling results for output power and PAE circles can be seen in Figure 3.4.

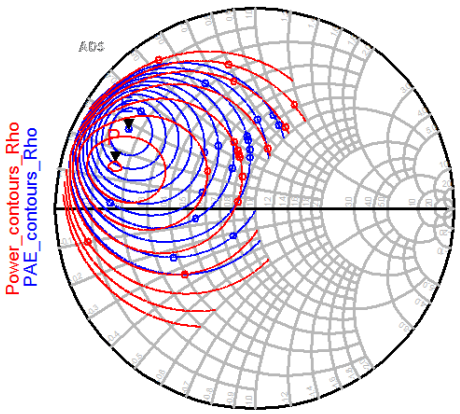

Figure 3.4: Constant Power and PAE circles of the main amplifier load pulling

Here, for a better input return loss in the band of interest, optimum source impedance is chosen to be $Z_S = 6.65 + j24.2$. There are a number of possible saturation and back-off load impedance combinations available. For the purpose of

increasing the maximum PAE, $Z_{L,m,P_{max}} = 8.3 + j5.4$ and $Z_{L,m,P_{bo}} = 8.3 + j15.4$ are chosen. Using these loads and the optimum source impedance, resulting main amplifier power levels are: $P_{SAT} = 25$dBm and $P_{bo} = 22$dBm, respectively, with similar PAE figures of around 50%. Before the matching networks are introduced, the small signal gain peaks at 10 dB for the center frequency. PAE and η curves for P_{max} and P_{bo} can be seen in Figure 3.5.

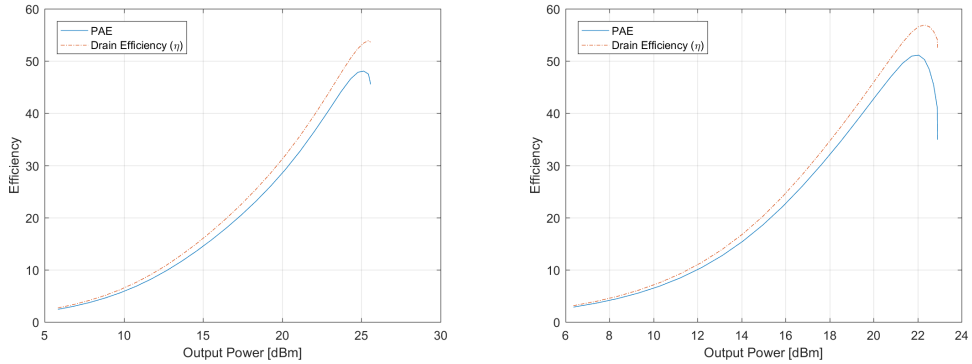

Figure 3.5: Drain efficiency and PAE curves when $Z_{L,m,P_{max}}$ (left) and $Z_{L,m,P_{bo}}$ (right) is introduced to the main amplifier at the center frequency

3.2.2 Input Matching Network

Although the whole amplifier is terminated with 50Ω, input of the main amplifier is matched to 35 Ω which is the output impedance of the power splitter. The reason for this is explained in the Power Splitter Design section.

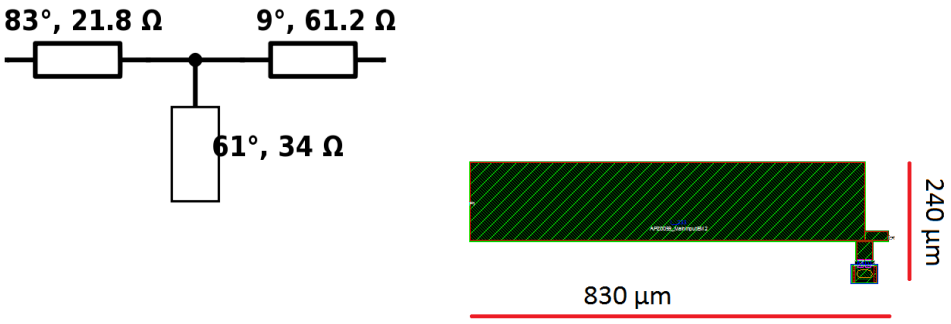

Figure 3.6: Main amplifier's input matching network schematics (left) and realized layout (right)

Input matching network circuit is composed of a T network for simplicity. Resulting network parameters are found using the optimization tool of ADS. Matching is done for low power transfer loss and high return loss between 26.5 GHz and 31.5

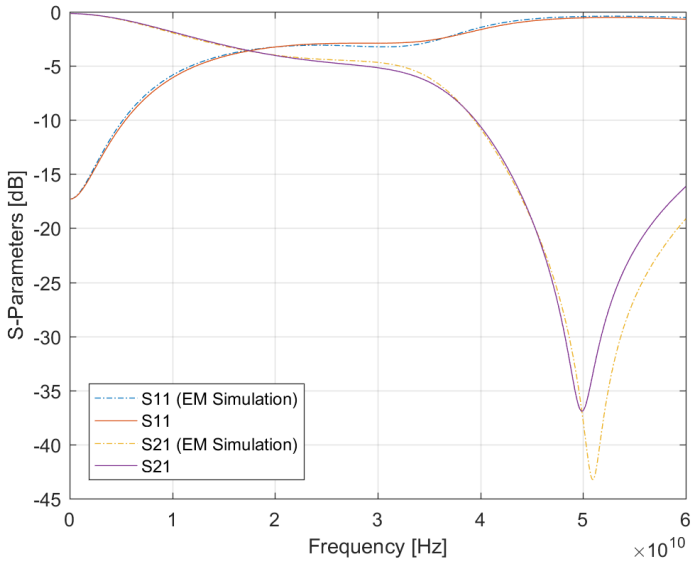

Figure 3.7: Comparison of schematics and EM-simulated s-parameters of the main amplifier's input matching network

GHz. After parameters of the transmission lines seen in Figure 3.6 are found, they were converted to layout components. The open stub in the T network is converted to a shorted capacitor with compactness in mind. The resulting layout is EM-simulated (both Momentum and RF) and optimized to match the s-parameters found in the schematics. The resulting S_{11} and S_{21} curves can be seen in Figure 3.7. The resulting circuit can be seen in Figure 3.6.

3.2.3 Gate and Drain Biasing Networks

The simulated biasing networks include RF termination circuits, DC paths to the pads and wire bonding connected to these pads for measurements. The schematic circuit shown in Figure 3.8 (left) is converted to layout and the resulting circuit is optimized to match the EM simulations to ADS simulations. The results and their comparison can be seen in Figure 3.8 (right). An important note is that bias line thicknesses are set to values which would carry the current flowing through them without burning the lines at P_{max}. While the gate current is negligible, the magnitude of the intrinsic drain current can be as high as 200 mA per transistor. The resulting minimum thickness of the drain bias lines are found to be 40 μm using the current density limits given in Win Semiconductors' pp1010 design manual [33].

3.3 Auxiliary Amplifier Design

Similar to the main amplifier design, the auxiliary amplifier is also designed keeping both gain and efficiency high in mind. Although the latter is easier to achieve for an auxiliary cell of the DPA due to class C biasing, high gain is fundamentally harder to get as it can be seen in Figure 2.4. The same V_{br} and pinch-off conditions as the

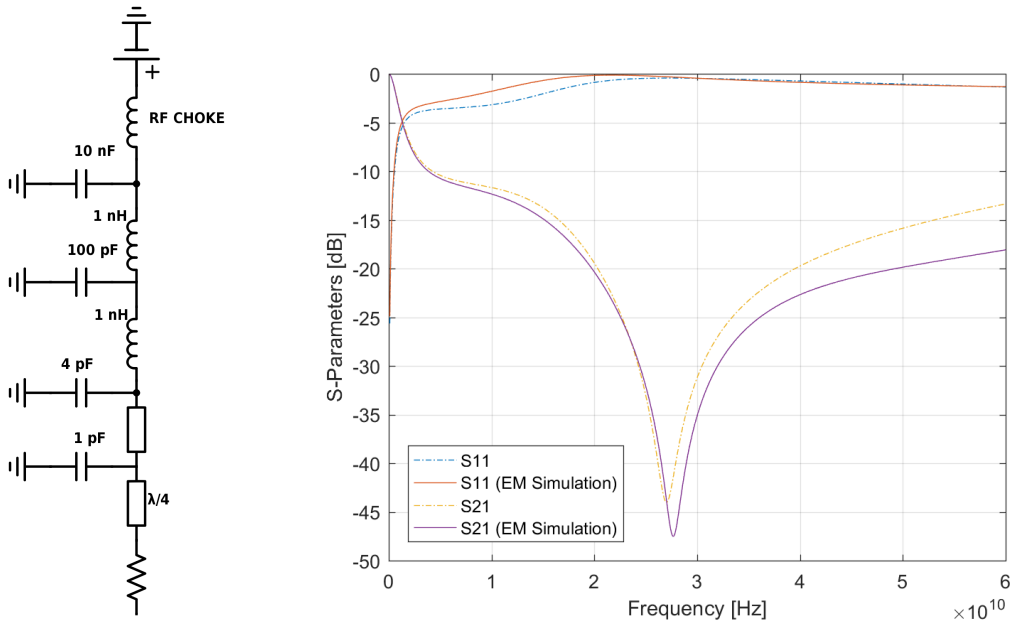

Figure 3.8: Gate biasing network schematics that includes RF termination, DC paths to the pads and wire bonding (left) and s-parameters of the network compared with the realized layout's EM simulation (right)

main amplifier apply for the auxiliary cell as well.

Ideally the auxiliary amplifier is turned off at the predetermined 6 dB back-off level. This requires $V_{GS} = -2.4$V. Since the transistors are turned off, the small signal gain is below zero. At this bias point, the large signal gain is also below 2 dB. Low level of gain decreases the efficiency of the auxiliary cell along with DPA itself. The gain of the DPA is pulled below 6 dB, which is not sufficient for a two-stage solution. At this stage a compromise is made from the efficiency to increase the overall gain by increasing the gate voltage. After an iteration process similar to the main cell, bias point is chosen to be $V_{DS} = 3.3V$ and $V_{GS} = -1.05V$.

3.3.1 Load Pulling

Extracting the needed parameters for the combining network given in (2.21) to (2.24), load pulling should be performed similar to the main amplifier. This time only the load value for the saturation level is needed. For a class C device, it is usually required to include the second harmonic load impedance for more accurate results. Since the bias point is close to pinch-off, it was possible to extract the parameters with enough accuracy only using the fundamental load impedance. Load pulling results showing constant output power and PAE circles can be seen in Figure 3.9. For a class C amplifier, there exists a harsh trade-off between output power, gain and PAE. Since the transistor will be off for low power levels, large signal s-parameters are of interest. For the purpose of finding a point to balance the values of all three parameters, $Z_{L,a,P_{max}} = 8+j5$ is chosen. This results in a peak PAE of 42%, maximum large signal gain of 6 dB and $P_{SAT} = 24.2$dBm with $Z_{a,off} = 1.1 - j12.7$.

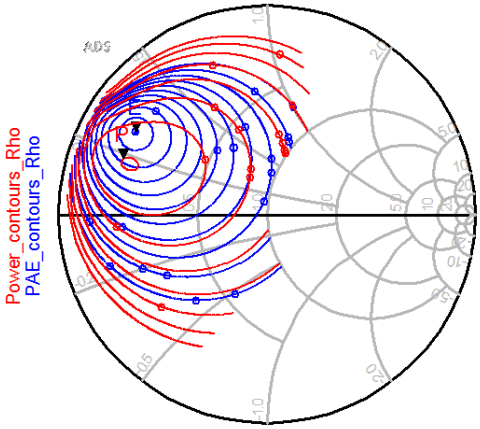

Figure 3.9: Constant Power and PAE circles of the auxiliary amplifier load pulling

3.3.2 Input Matching Network

Similar to the main amplifier, input of the auxiliary amplifier is matched to 35 Ω, which is the output impedance of the power splitter.

Input matching network circuit is again composed of a T network for simplicity. Resulting network parameters are found using the optimization tool of ADS. Matching is done for low power transfer loss and high return loss between 26.5 GHz and 31.5 GHz. After parameters of the transmission lines seen in Figure 3.10 are found, they were converted to layout. The open stub in the T network is again converted to a shorted capacitor with compactness in mind. The resulting layout is EM-simulated (both Momentum and RF) and optimized to match the s-parameters found in the schematics. The resulting S_{11} and S_{21} curves can be seen in Figure 3.11. The resulting circuit can be seen in Figure 3.10.

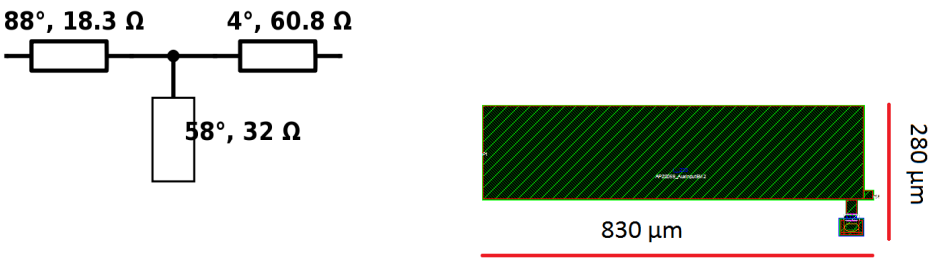

Figure 3.10: Auxiliary amplifier's input matching network schematics (left) and realized layout (right)

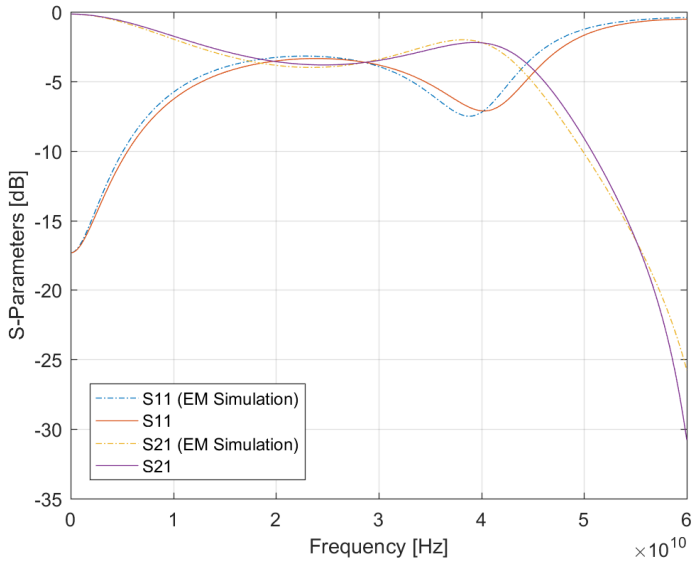

Figure 3.11: Comparison of schematics and EM-simulated s-parameters of the auxiliary amplifier's input matching network

3.4 Power Splitter Design

The gains and power outputs of each cell of the DPA is different. This requires feeding of each cell with different power levels which can be implemented using an unequal Wilkinson power splitter. In Figure 3.12, a topology of such a splitter is presented. Using the tuning tool of ADS, P_a/P_m is found to be 7/3. This ratio is enough for the design of the power splitter cell. In terms of the characteristic impedance, Z_0 and power levels, $P_A = P_m$ and $P_B = P_a$, it is possible to find all of the parameters seen in Figure 3.12: [34, 35]

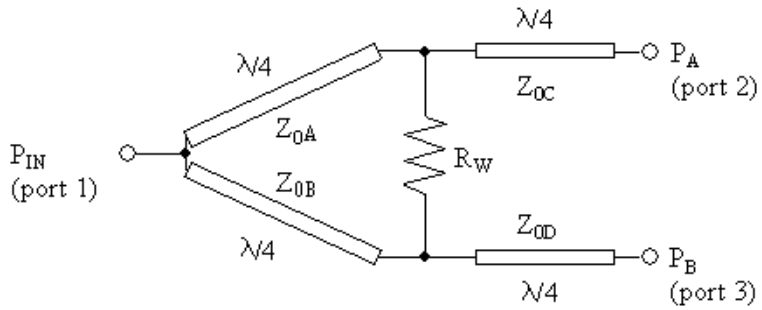

Figure 3.12: Topology of unequal Wilkinson power splitter [35]

$$Z_{0A} = Z_0\left(\left(\frac{P_A}{P_B}\right)^{-1.5} + \left(\frac{P_A}{P_B}\right)^{-0.5}\right)^{0.5} \tag{3.1}$$

$$Z_{0B} = Z_0\left(\left(1 + \frac{P_A}{P_B}\right)^{-1.5}\left(\frac{P_A}{P_B}\right)^{-0.5}\right)^{0.5} \tag{3.2}$$

$$Z_{0C} = Z_0 \left(\frac{P_A}{P_B} \right)^{-0.25} \tag{3.3}$$

$$Z_{0D} = \left(\frac{P_A}{P_B} \right)^{0.25} \tag{3.4}$$

$$R_W = Z_0 \left(\left(\frac{P_A}{P_B} \right)^{0.5} + \left(\frac{P_A}{P_B} \right)^{-0.5} \right) \tag{3.5}$$

Initial design trial assumed a Z_0 of 50Ω. This resulted in one of the $\lambda/4$ branches (Z_{0B}) to have a characteristic impedance of 91Ω. Realization of this branch requires a line thickness of 4.5 μm. In the pp1010 process, the minimum thickness for a microstrip line is limited to 5 μm. To have a safety margin, in practice it is preferable to go towards 10 μm. For this reason Z_0 is chosen to be 35Ω. The input matching networks of the main and auxiliary cells and output of the pre-amplifier cell are therefore set to this value. To have a power ratio of 7/3 in the ports, transfer parameters S_{21} and S_{31} should have a difference of 3.6 dB.

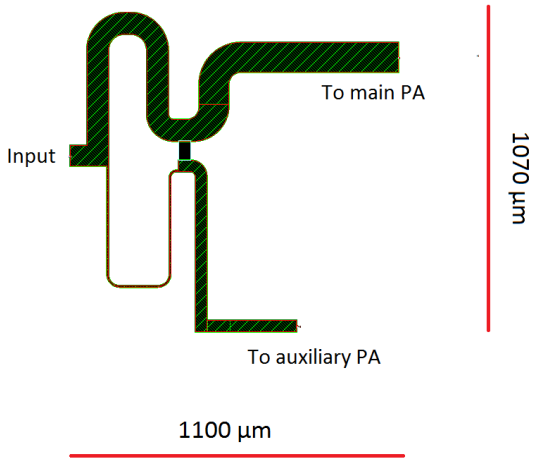

Figure 3.13: Layout of unequal Wilkinson power splitter [35]

The parameters for the unequal splitter are calculated to be $Z_{0A} = 34\Omega$, $Z_{0B} = 78\Omega$, $Z_{0C} = 46\Omega$, $Z_{0D} = 29\Omega$ and $R_W = 76\Omega$ using equations (3.1) to (3.5). The realized layout circuit can be seen in Figure 3.13.

The designed circuit is simulated with both ADS and Momentum. The resulting S-parameters (left) and phase difference between two output ports (right) can be seen in Figure 3.14. Return loss is simulated to be larger than 20 dB in the band of interest. Similarly isolation between the output ports is larger than 25 dB. Phase difference in the band should be minimal in order for the DPA to have a consistent performance.

3.5 Combining Network Design

The combining network consists of ideal lumped components with values summarized in equations (2.38)-(2.42). The schematics of the combiner circuit between the

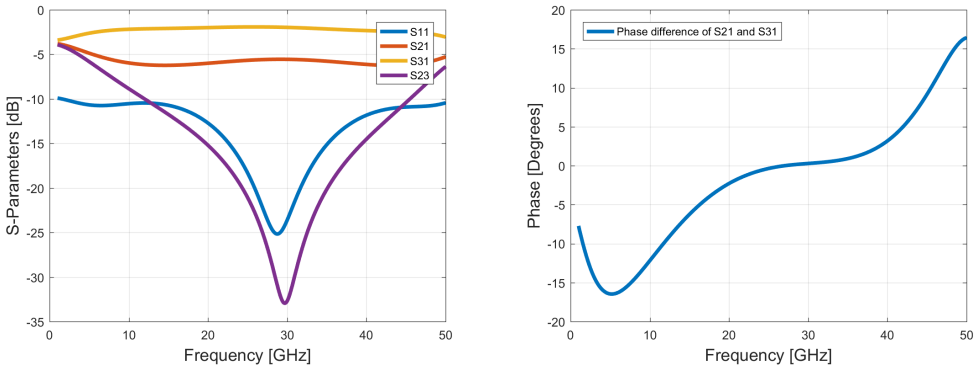

Figure 3.14: S-parameters of the Wilkinson power splitter (left). The difference between S_{21} and S_{31} is designed to be 3.6 dB in band. S_{23} is the isolation between the output ports. The phase difference between S_{21} and S_{31} (right) is designed to be minimum in the band to introduce main and auxiliary amplifiers constant phase difference at all times

main and auxiliary transistors and the quarter wave transformer that converts the termination resistance to 50Ω can be seen in Figure 3.15.

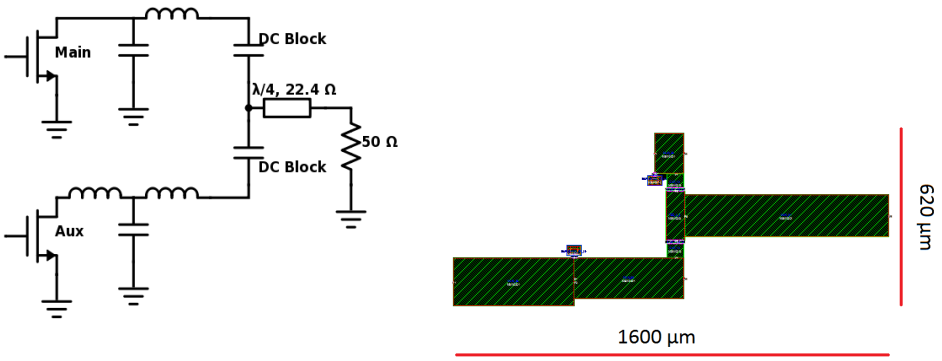

Figure 3.15: Schematics of the combiner circuit realized with ideal components (left) and realized layout (right)

Although the termination resistance is a free parameter, it can be tricky to choose since all the components in the combiner should be realizable. Realizable means that, after the conversion of ideal components to distributed, they should be within the foundry limitations. 50Ω termination may be the most compact solution but results in non-realizable inductor values. Using values resistance values lower than 10Ω can be hard to transform into 50Ω. As a starting point 20Ω is selected and later optimized to 10Ω.

The realized combining network's ADS and EM simulations can be seen in Figure 3.16.

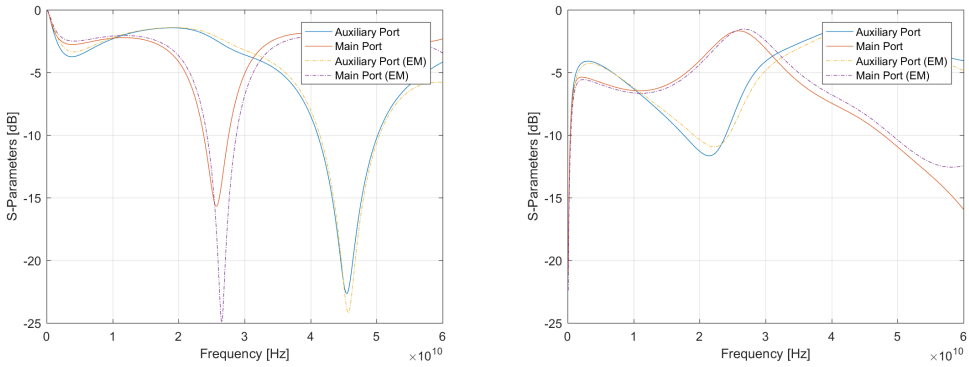

Figure 3.16: Return loss from auxiliary and main ports (left) and transfer parameters to the termination resistance (right)

3.6 Doherty PA Design

The resulting Doherty PA can be seen in Figure 3.17. The small signal s-parameters for the cell is given in Figure 3.18 (left). As seen in the figure, the gain peaks at 8.4 dB at the center frequency, staying above 7 dB in 26.5-31.5 GHz band. The input and output return loss of the cell are larger than 10 dB for the small signals. For large signals, where the PA will work most of the time, these values are modified as seen in Figure 3.18 (right). Here an input power level of 20 dBm is introduced to the amplifier. This results in $P_{out} = 25.8dBm$, where the amplifier is in compression region. Even in compression, it can be seen that S_{11} and S_{22} is lower than -10 dB in 26.5-31.5 GHz band. The drain efficiency and PAE curves are plotted for the center frequency in Figure 3.19. The peak drain efficiency reaches 48% at $P_{out} = 26.3$ dBm and the peak PAE is 40.6% at $P_{out} = 25.3$ dBm. The difference between the two efficiency figures is mainly due to low gain. Since the gain drops further when moved away from the center frequency, PAE is expected to go down as well.

3.7 Pre-amplifier Design

The pre-amplifier located in front of the Doherty cell has two main purposes; increasing the overall gain of the PA while keeping the efficiency high and promote a relatively flat gain in the band of interest. The latter is more difficult to accomplish since the gain response of the pre-amplifier should have the reverse of the gain response of the Doherty cell. This causes a valley in the gain response with the center frequency having the lowest gain. Having a low gain can cause the PAE to drop for the whole amplifier. With this in mind, the gain of the pre-amplifier is not designed for the flattest possible overall response.

The P_{SAT} of the Doherty cell is close to 27 dBm with a 3 dB compressed gain of 5.5 dB. The driver should therefore have a P_{1dB} of 21.5 dBm in order to accommodate this power level. A deep class AB amplifier with a single 6x50 transistor is chosen for this task. The reasons for this choice are relatively linear response and high gain, in addition to low power consumption when compared to the DPA cell. The

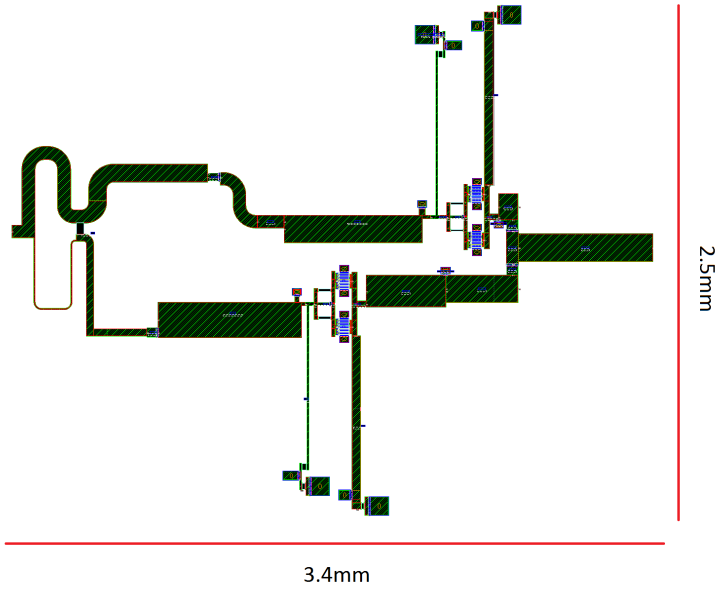

Figure 3.17: Layout of the Doherty cell. The y-dimension will shrink further after meandering of DC feed lines.

designed pre-amplifier should affect the efficiency response minimally.

With a bias point of $(V_{DS}, V_{GS}) = (3.3V, -0.8V)$, optimum source and load impedances are found to be 5-20j and 12-10j, respectively, resulting in a gain of 9 dB and P_{1dB} of 21.7 dBm at the center frequency. The IMN are OMN are matched to 50Ω and 35Ω respectively.

A second order T network is chosen as the IMN for better control of the flatness of the gain accompanied by a T OMN. The resulting s-parameters of the pre-amplifier can be seen in Figure 3.20. It is important to note that S_{21} has a 'U' shaped curve in the frequency band. At 26.5, 29 and 31.5 GHz the gain values are 8 dB, 7.6 dB and 8.8 dB respectively.

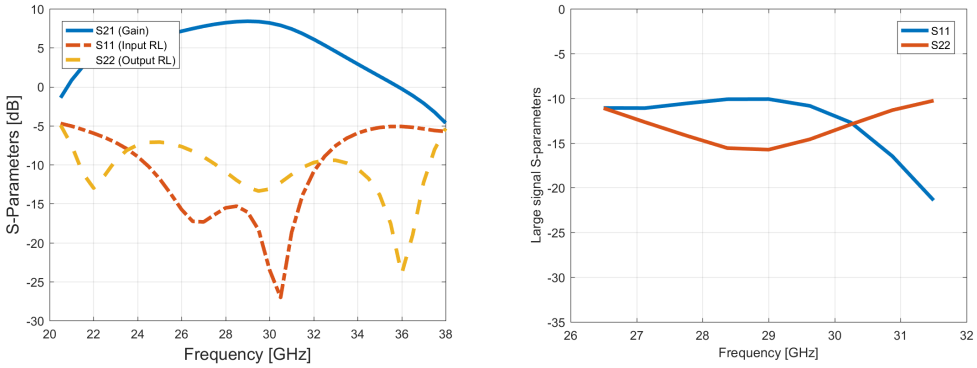

Figure 3.18: S-parameters of the Doherty cell: Small signal gain, input and output return losses (left) and large signal input and output return losses at $P_{in} = 20dBm$ (right)

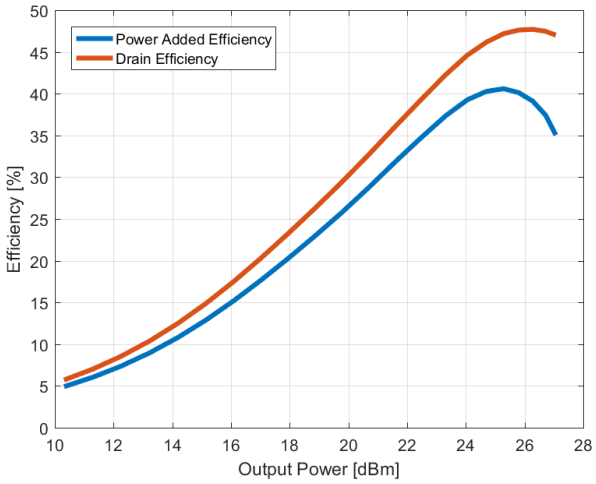

Figure 3.19: PAE and drain efficiency (η) of the Doherty cell

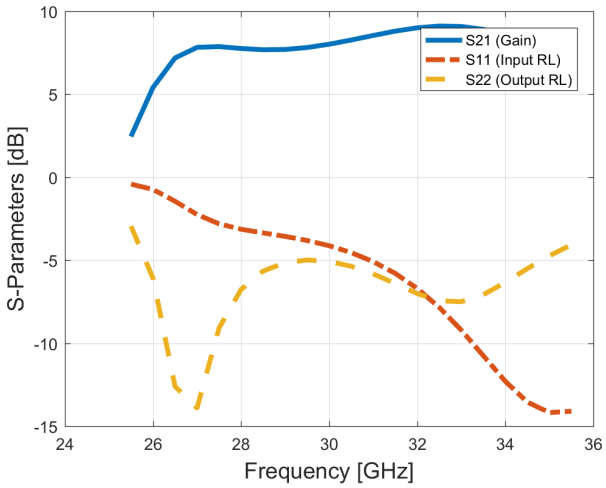

Figure 3.20: S-parameters of the designed pre-amplifier

4

Results

The complete power amplifier is implemented by assembling each network designed in the previous chapter. The schematic representation of the overall circuit can be found in the Appendix. The layout is created for one of the available cell sizes on the tape-out wafer. Two sizes were possible: $(x, y) = (2\text{mm}, 2.5\text{mm})$ or $(x, y) = (5\text{mm}, 1.6\text{mm})$. It was only possible to fit the DPA cell in a $2\text{mm}x2.5\text{mm}$ chip. Since separating the pre-amplifier from the monolithic design can degrade the performance this chip size was not used. Hence the second size option is chosen, which required a horizontal design. The final layout can be seen in Figure 4.1. Each designed network is highlighted at their particular region.

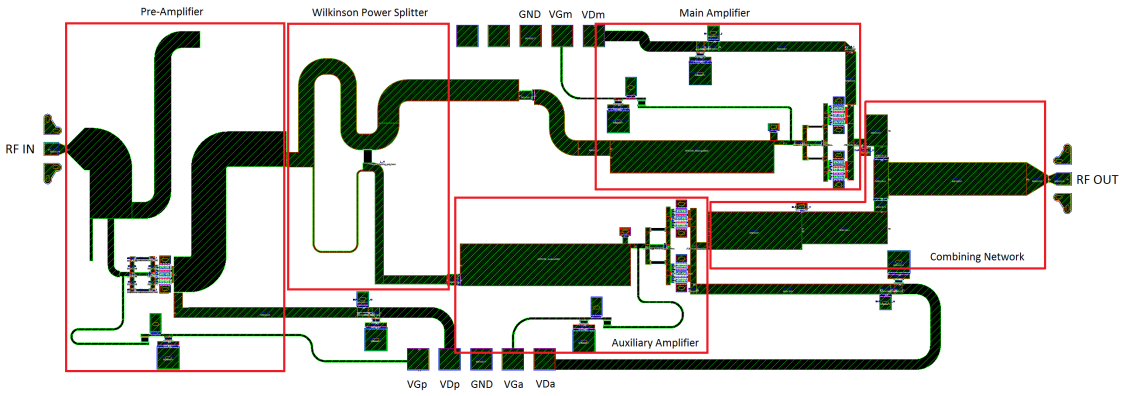

Figure 4.1: The layout of the complete DPA with each network highlighted.

The simulated small signal and large signal s-parameters can be seen in Figure 4.2 and Figure 4.3, respectively. The large signal amplitude is chosen such that it gives the maximum output power, P_{max}. Here the gain is compressed 3 dB at P_{SAT} as expected. Due to the effect of the RF signal itself, biasing of the each transistor also changes, which in turn modifies the return losses. As shown in Figure 4.3, both input and output reflection is reduced, with S22 going below -10 dB in the band of interest. The 3 dB bandwidth of the amplifier is 7 GHz, between 25.5 and 32.5 GHz, which corresponds to 24%.

PAE at 29 GHz is plotted in Figure 4.4 and has a maximum value of 42 % with saturation power of 27 dBm. The main aim of the thesis is having better efficiency figures at back-off levels. For better comparison, an additional simulation was performed by designing a class A amplifier in the same frequency range with same size transistors and P_{SAT} level. In this frequency range the amplifier has less than 5% efficiency at 9 dB back-off as seen in Figure 4.5. However, the simulated

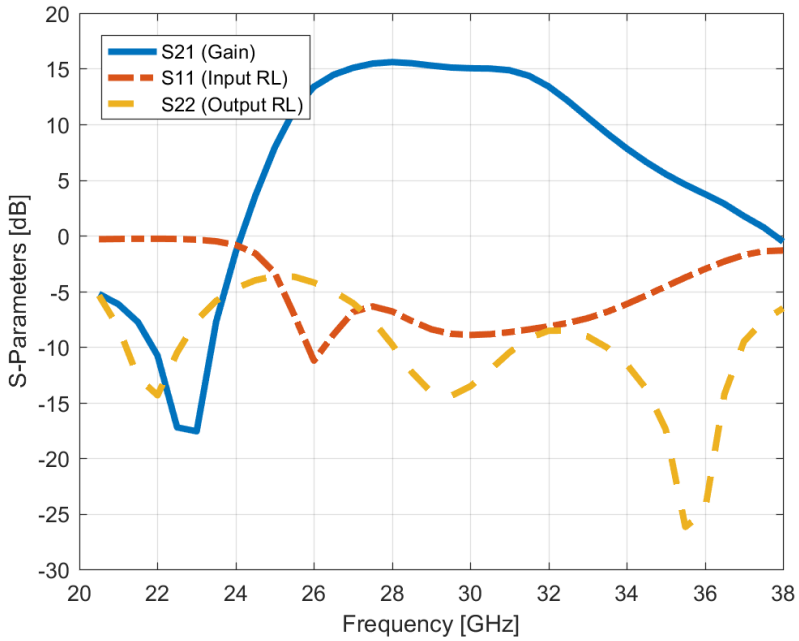

Figure 4.2: Small signal gain, input and output return loss of the DPA

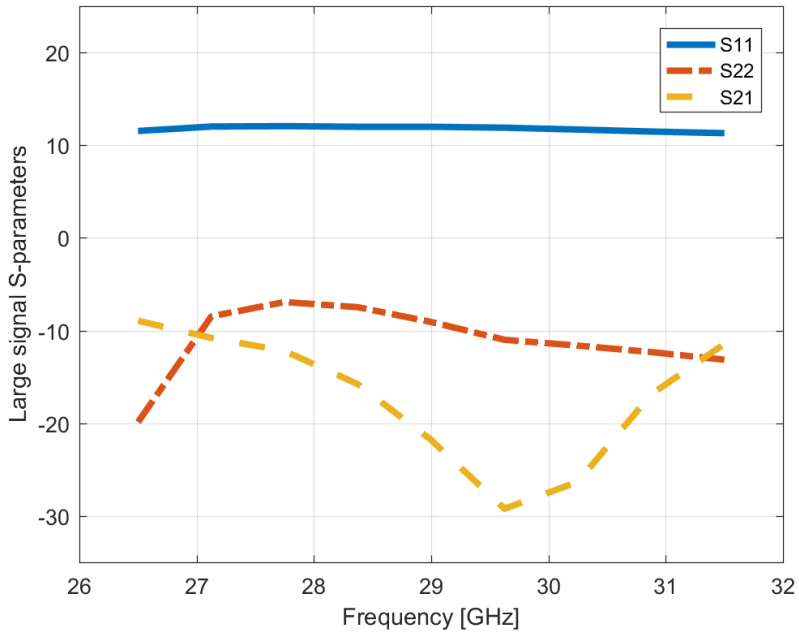

Figure 4.3: Large signal gain, input and output return loss of the DPA

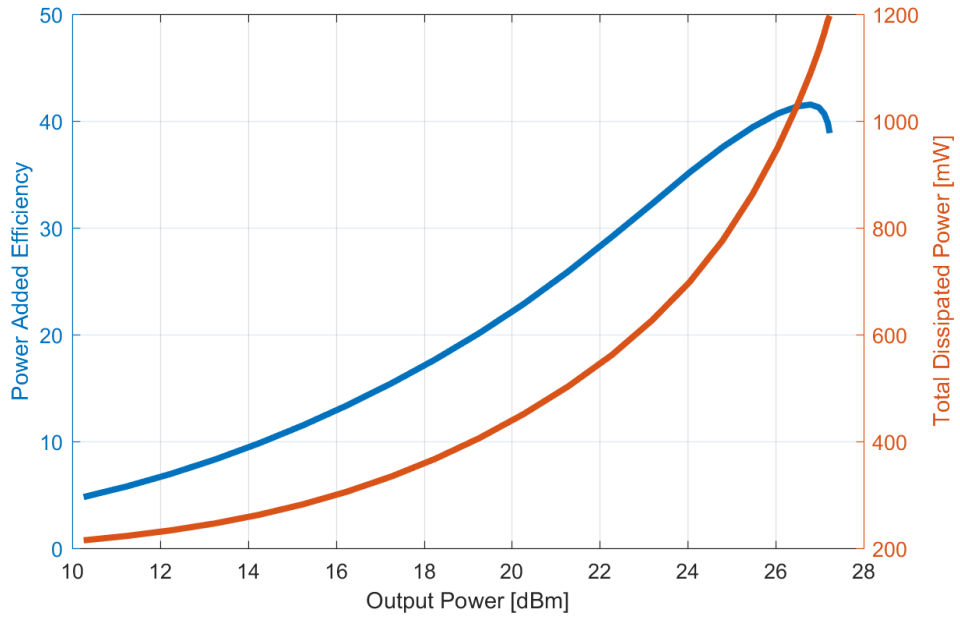

Figure 4.4: Power Added Efficiency and total dissipated power of the DPA at 29 GHz

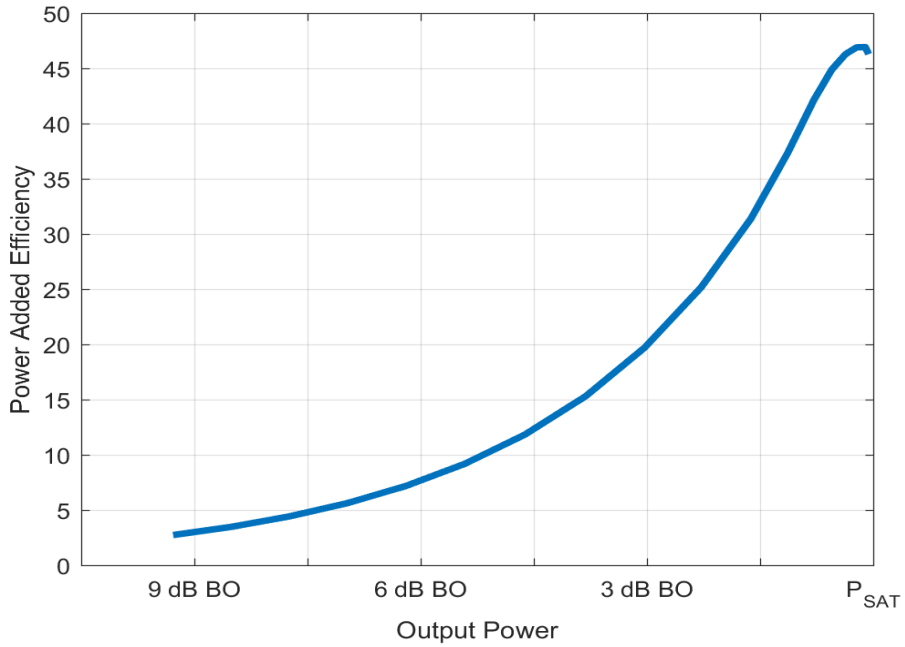

Figure 4.5: Power Added Efficiency of a class A amplifier at 29 GHz and P_{SAT} = 27dBm

amplifier has 35%, 26% and 18% PAE at 3, 6 and 9 dB of output back-off respectively. The total dissipated power for the whole circuit is 1.2 Watts as shown in Figure 4.4. While the pre-amplifier consumes 300 mW, each transistor in the DPA cell consumes around 225 mW. Using these values, the junction temperature of each transistor is calculated to be 143.5° C for the pre-amplifier and 129° C for DPA transistors at an ambient temperature of 85° C.

P_{1dB} and P_{SAT} figures with respect to frequency band of design is plotted in Figure 4.6 (top). The saturation power level is higher than 26 dBm. P_{1dB} is also higher than 26 dBm in the lower end of the design band, it gradually drops to 23.5 dBm for higher frequencies. The peak PAE level with respect to frequency band of design is plotted in Figure 4.6 (bottom). PAE stays above 35% for the whole band and above 40% between 27.5 and 30 GHz. Table 4.1 presents a comparison between the DPA of this work and other reported mm-wave PAs.

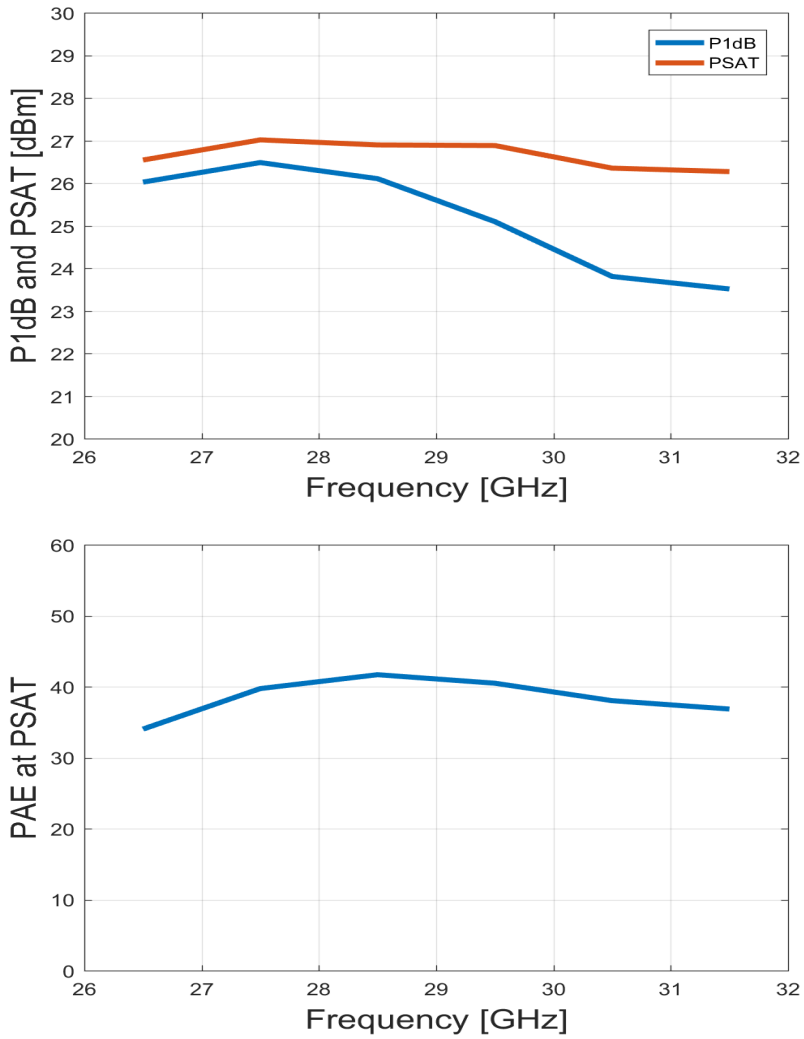

Figure 4.6: P_{1dB} and P_{SAT} vs frequency (top) and PAE at P_{SAT} vs frequency (bottom)

Reference	f_0 [GHz]	P_{SAT} [dBm]	Peak PAE [%]	BO PAE [%]	Gain [dB]
This work	26.5-31.5	27	42	26	15
[36]	26.6	26.9	42	32	10.5
[37]	27-32	33.5	26	9	21
[38]	22.8-25.2	30.9	38	20	12.5
[39]	23	36.8	48	34	16
[40]	31-35	26	39.2	19.8	>5.5

Table 4.1: Comparison of this work to other reported mm-wave PAs

Another important parameter to check is the intrinsic voltage swings between the terminals. One of the main issues in this design was to limit the gate-to-drain voltage of the auxiliary transistors due to the class C biasing. V_{dd} is reduced from 4 V to 3.3 V in order to minimize this problem. The pre-amplifier and main amplifier transistors were not effected to this degree since their bias point was deep class AB. Minimum and maximum intrinsic terminal voltages with respect to input power is plotted in Figure 4.7. Here we see that the transistor reaches breakdown at an input power of 18 dBm, which is 3 dB more than the drive level needed for P_{SAT}.

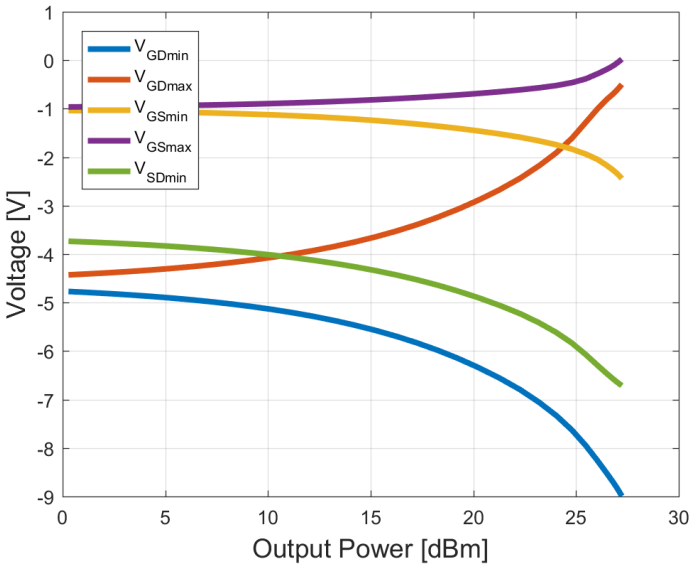

Figure 4.7: Minimum and maximum voltage swings of intrinsic terminal voltages with respect to output power

Finally AM-to-AM and AM-to-PM conversion performance is simulated. The gain and phase response with respect to input power is plotted in Figure 4.8 (top). The gain stays fairly constant until it goes into compression. The phase also stays constant until a certain power level is reached and then it starts to increase gradually. The phase difference between input and output as a function of P_{out} is plotted in Figure 4.8 (bottom). It can be seen that the the phase difference reaches 18 degrees at P_{SAT} (27 dBm).

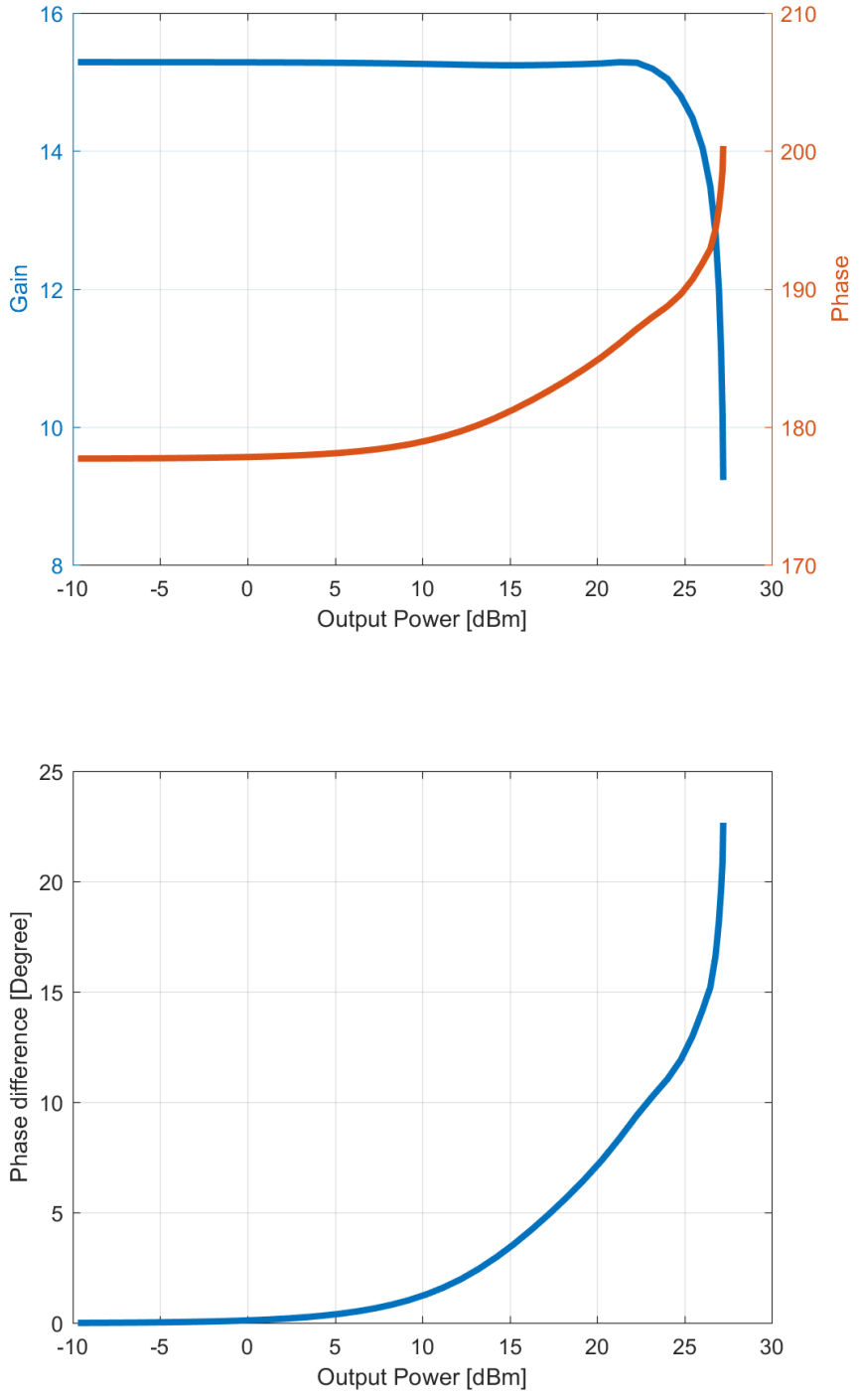

Figure 4.8: Gain (AM-to-AM) and phase (AM-to-PM) response (top) and phase difference between input and output signals (bottom) with respect to output power

5
Conclusion and Future Work

5.1 Conclusions

In this thesis, design procedure and final performance of a high efficiency Ka-band MMIC power amplifier is presented. The amplifier consists of two stages: A Doherty PA cell and a pre-amplifier to improve the overall gain. A layout is created for future fabrication and measurements. The targeted specifications given in Table 1.1 are achieved with a safety margin for possible frequency shifts that can happen after the fabrication process.

Simulated results of the final amplifier show a peak PAE of 42% for 27 dBm output power at 29 GHz, with 35%, 26% and 18% at 3, 6 and 9 dB of output back-off, respectively. The output power is over 26 dBm in 26-32 GHz band. The gain is larger than 15 dB in 27-31 GHz band. These results make this design a promising candidate for future 5G millimeter wave applications.

During the design, different operation conditions such as changing bias points and heat are considered. Overall power consumption of the amplifier is 1.2W, which is well below the targeted consumption level of 2 Watts. The junction temperature of each transistor is calculated to be less than $150°C$, which is needed for MILSTD requirements at a maximum operating temperature of $85°C$. With different bias points, it is possible to achieve higher in-band gain or higher output power depending on the drain bias of the main amplifier.

It is also shown that this amplifier is a promising alternative compared to traditional PA classes, especially at back-off power levels. For a Doherty PA, it is possible to achieve better back-off efficiency figures. In order to achieve higher gain, the auxiliary amplifier is biased closer to class B, which decreased the turn-on point. Since the auxiliary amplifier is turned on earlier, the back-off efficiency is lowered. This trade-off in turn helped to achieve the required gain of 15 dB in two stages.

5.2 Future Work

Measurements are going to be performed after the fabricated circuits become available to us. It will be checked whether the measurement results are consistent with the simulated results.

An interesting future research direction is to investigate different circuit topologies other than the presented topology in this thesis. One example circuit is implemented in [38], where two driver amplifiers are used after the power splitter instead of a single pre-amplifier before the splitter. This topology is shown to have better

efficiency compared to the single pre-amplifier [38]. Although this kind of circuit is not implemented in this thesis due to its relatively high complexity, it provides an attractive future line of research.

Another interesting research direction would be the investigation of different fabrication technologies and/or foundries, where better break down voltage-gain-P_{max} trade-off may be possible.

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A

Appendix

Schematics representation of the complete DPA circuit is given below in Figure A.1.

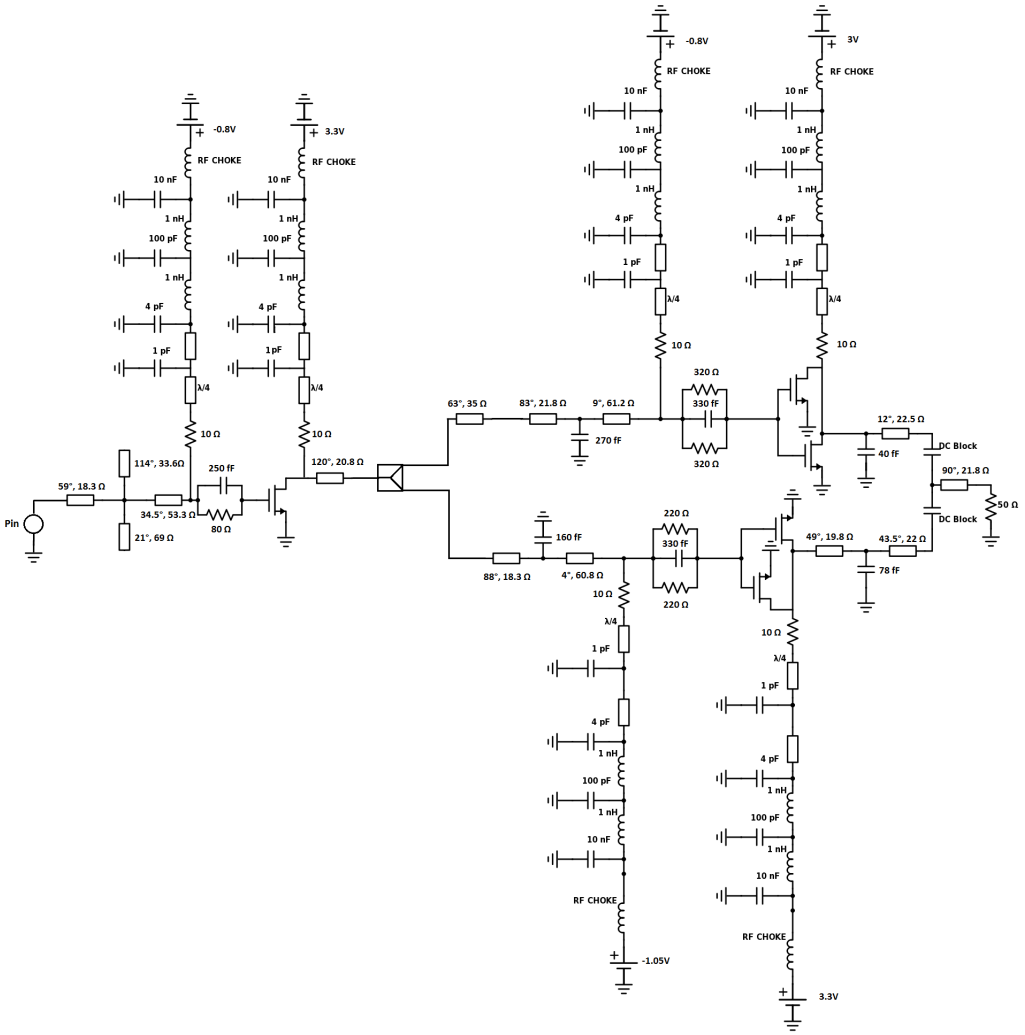

Figure A.1: Schematics of the overall DPA circuit