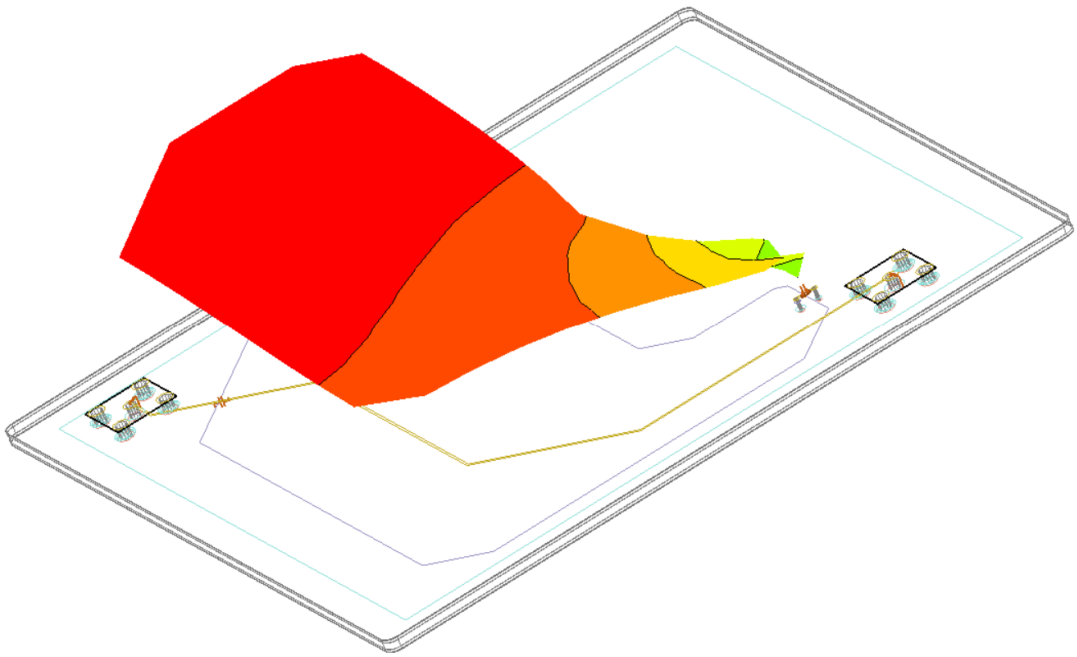

Electrical and Thermal Optimization of Inverter PCB Design

A simulation-driven investigation of signal integrity, electromagnetic interference, DC resistance, and thermal effects in high performance automotive PCB systems

Master's thesis in Sustainable Electric Power Engineering and Electromobility

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Cover: Resonance modes of a power plane in a PCB identified using Ansys SIwave.

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Abstract

Automotive inverter PCBs have to carry both high-speed switching signals and large currents on the same layers, which makes the layout far more sensitive than it might first appear. A trace that is a few tenths of a millimeter too narrow, or a via that is not back-drilled, can show up later as excessive insertion loss, an EMI compliance failure, unexpected heating, or all of these together. This thesis examines how such layout decisions affect signal integrity, electromagnetic interference, DC resistance, and thermal performance, using a set of purpose-built test boards that were simulated and then measured in hardware to confirm the results. Rather than analyzing a full inverter PCB where every effect is tangled together, dedicated structures were designed to isolate specific mechanisms individually: via stubs, return-path discontinuities, crosstalk, current distribution, and power-plane resonance. The results tell a fairly consistent story: small layout details matter more than one might expect. Via stubs degrade signal transmission at high frequency, and back-drilling largely fixes it. A return-path split increases insertion loss above 1 GHz, but a 100 nF stitching capacitor recovers much of that loss. Widening trace spacing from 1W to 3W cut near-end crosstalk from 96.7 mV to 52.9 mV, though far-end crosstalk actually went up, since the wider-spacing structure also had a longer coupled section. On the DCIR side, going from one via to four dropped current density from 34.45 A/mm^2 to 13.14 A/mm^2, and widening a trace from 0.25 mm to 10 mm brought the voltage drop down from 584.5 mV to 26.4 mV, with a corresponding thermal improvement from roughly 182 °C down to 27 °C. In the EMI test board, the third harmonic of an 80 MHz signal excited a power-plane resonance around 240 MHz, and adding a second decoupling capacitor cut the measured near-field emission peak by about 17 dB. Taken together, the work shows that fairly modest changes to a PCB layout can shift electrical and thermal performance substantially, and it offers a simulation methodology, validated against hardware, for catching these effects before a board is built.

Keywords: PCB design, signal integrity, electromagnetic interference, DCIR, thermal analysis, via parasitics, crosstalk, inverter systems.

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Gothenburg, Sweden, 2026

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

DCIR	Direct Current Internal Resistance
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FEXT	Far-End Crosstalk
NEXT	Near-End Crosstalk
PCB	Printed Circuit Boards
PDN	Power Distribution Network
SI	Signal Integrity
VNA	Vector Network Analyzer

Contents

1

Introduction

1.1 Background

Modern automotive inverter systems operate with high switching speeds and large voltage gradients, where both power and control signals coexist on the same printed circuit board (PCB). In such environments, the PCB layout becomes a critical factor for system performance, electromagnetic compatibility, and thermal reliability.

Once switching speeds get high enough, a PCB trace stops acting like a simple wire. Its behavior becomes frequency dependent instead, shaped by trace geometry, via placement, and how close a reference plane sits underneath it. Reflections, crosstalk, and EMI all trace back to this same shift.

The power stage adds its own complications. Large currents cause voltage drop and current crowding at narrow sections or vias, and the resulting heat has to go somewhere. Between these electrical and thermal pressures, it becomes clear that layout, not just circuit topology, ends up deciding how well an inverter PCB actually performs.

1.2 Previous Work and Problem Formulation

Previous research and industrial design practices have addressed signal integrity, electromagnetic interference, DC power distribution, and thermal behavior individually. However, in practical inverter systems, these effects are coupled and influenced simultaneously by the PCB layout.

A major challenge in current design approaches is the difficulty in isolating the contribution of individual layout features, such as vias, return paths, and trace spacing, when analyzing complex boards. This often leads to a limited understanding of how specific design decisions affect overall system performance.

As a consequence, PCB optimization is frequently carried out through iterative design cycles rather than through a systematic and structured approach. There

is therefore a need for methods that allow clear identification and evaluation of individual layout-driven effects.

1.3 Purpose

The purpose of this thesis is to analyze inverter PCB design from both electrical and thermal perspectives.

The work focuses on:

- Signal integrity (SI)
- Electromagnetic interference (EMI)
- DC resistance (DCIR)
- Thermal behavior

To achieve this, simplified test structures are developed to isolate key physical mechanisms such as via parasitics, return-path degradation, and inter-trace coupling. These insights are then applied to a real inverter PCB, where simulation and measurement are used to evaluate performance and identify design improvements.

2

Theory

2.1 Signal Propagation in PCB Interconnects

In high-speed electronic systems, PCB interconnects cannot be treated as ideal conductors [1, 2]. Instead, they must be modeled as transmission lines, where electrical signals propagate as electromagnetic waves. This behavior becomes significant when the electrical length of the interconnect is comparable to the signal wavelength, which depends on the rise time of the signal rather than only its fundamental frequency.

A transmission line is characterized by distributed electrical parameters, namely resistance R, inductance L, capacitance C, and conductance G per unit length. These parameters define the characteristic impedance of the line

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.1}$$

At high frequencies, the reactive components dominate, and the impedance becomes primarily dependent on the ratio between inductance and capacitance. This impedance is determined by the geometry of the trace and the surrounding dielectric materials, which makes PCB layout a critical factor in signal propagation [1, 3].

2.1.1 Signal Reflection and Impedance Discontinuity

Whenever a signal encounters a change in impedance along the transmission path, part of the signal is reflected back toward the source. This phenomenon is described by the reflection coefficient

$$\Gamma = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{2.2}$$

where Z_{in} is the input impedance at the discontinuity and Z_0 is the characteristic

impedance of the transmission line.

If $Z_{in} = Z_0$, the reflection coefficient becomes zero, meaning that no reflection occurs. However, in practical PCB layouts, perfect matching is rarely achieved due to vias, connectors, and changes in trace geometry. These mismatches result in reflections that can distort the signal, leading to ringing, overshoot, and timing errors [1, 2].

2.1.2 Return Loss and Insertion Loss

The reflection coefficient is commonly expressed in decibels as return loss

$$\text{Return Loss} = -20 \log_{10} |\Gamma| \tag{2.3}$$

A higher return loss (i.e., a more negative value) indicates better impedance matching and lower reflections.

Insertion loss describes the attenuation of the signal as it propagates along the interconnect

$$\text{Insertion Loss} = 20 \log_{10} |S_{21}| \tag{2.4}$$

This loss includes conductive losses, such as skin effect and dielectric loss, as well as reflective losses caused by impedance discontinuities. While return loss describes the reflected portion of the signal, insertion loss describes the portion that reaches the receiver [3, 2].

2.2 Via Parasitics and Discontinuities

Vias are essential elements in multilayer PCB design, providing electrical connections between different signal layers [1, 4]. However, they introduce discontinuities in the signal path that affect signal integrity, particularly at higher frequencies.

At low frequencies, a via can be approximated as an ideal conductor. As frequency increases, the electromagnetic behavior becomes more complex, and both inductive and capacitive parasitics must be considered. The via can be modeled as a combination of series inductance and shunt capacitance, leading to a frequency-dependent impedance

$$Z_{via}(j\omega) = j\omega L_{via} + \frac{1}{j\omega C_{via}} \tag{2.5}$$

This impedance variation introduces mismatch relative to the transmission line, resulting in partial signal reflection.

2.2.1 Via Stub Effects

In practical PCB designs, vias often extend beyond the signal layer, creating an unused section of the via barrel commonly referred to as a stub. This unused portion behaves as an open-ended transmission line segment.

The input impedance of such a stub is given by

$$Z_{stub} = -jZ_0 \cot(\beta L_{stub}) \tag{2.6}$$

This expression shows that the impedance varies with frequency and introduces reactive behavior that modifies the local impedance seen by the signal [4, 5].

2.2.2 Resonance Behavior

At sufficiently high frequencies, the via stub can reach resonance. The first resonance occurs approximately at

$$f_{res} = \frac{c}{4\sqrt{\varepsilon_{eff}} L_{stub}} \tag{2.7}$$

At this frequency, the stub behaves as a strong discontinuity, causing significant reflections [6, 7]. Even below resonance, the stub introduces phase shifts and energy storage, which degrade signal transmission.

2.2.3 Impact on Signal Integrity

The effect of a via stub on signal integrity is primarily observed as increased insertion loss at higher frequencies. This occurs because part of the signal energy is reflected and does not propagate to the load.

In contrast, the impact on return loss may appear less significant, since the dominant impedance discontinuity is still associated with the via transition itself. The stub mainly introduces distributed reflections rather than a large input mismatch.

2.2.4 Design Considerations

The severity of via parasitics depends on parameters such as stub length, dielectric properties, and via geometry. Longer stubs result in lower resonance frequencies and therefore affect a wider frequency range.

To mitigate these effects, techniques such as back-drilling, blind vias, or optimized via placement are commonly used to reduce or eliminate the unused via length [8, 9].

2.3 Crosstalk Mechanisms

Crosstalk is an undesired coupling phenomenon that occurs when electromagnetic fields from one signal trace influence a nearby conductor. As signal transition speeds increase and routing density becomes higher, crosstalk becomes a major limitation for signal integrity in PCB design.

Crosstalk originates from the interaction of electric and magnetic fields between adjacent conductors and depends strongly on trace geometry, spacing, layer configuration, and the presence of a reference plane [10, 3].

2.3.1 Electromagnetic Coupling Between Conductors

Two primary coupling mechanisms contribute to crosstalk, namely capacitive coupling and inductive coupling.

Capacitive coupling is caused by electric fields between conductors. A time-varying voltage on the aggressor line induces a displacement current in the victim trace, which is proportional to the rate of change of voltage

$$V_{induced} \propto \frac{dV}{dt} \tag{2.8}$$

Inductive coupling arises due to magnetic fields generated by changing currents, which induce voltages in nearby conductors proportional to the rate of change of current

$$V_{induced} \propto \frac{dI}{dt} \tag{2.9}$$

This shows that fast switching edges, rather than the fundamental signal frequency, are the dominant contributors to crosstalk .

2.3.2 Near-End Crosstalk (NEXT)

Near-end crosstalk (NEXT) appears at the same end of the victim trace as the signal source and is primarily dominated by capacitive coupling.

NEXT can be expressed as

$$V_{NEXT}(t) \propto K_{NEXT} \tag{2.10}$$

where K_{NEXT} depends on trace geometry and spacing.

Since NEXT is a local effect, it does not depend significantly on the total trace length, but rather on the coupling near the source region [3, 10].

2.3.3 Far-End Crosstalk (FEXT)

Far-end crosstalk (FEXT) appears at the opposite end of the victim trace. Unlike NEXT, FEXT depends on both capacitive and inductive coupling and is governed by their imbalance.

This relationship can be expressed as

$$V_{FEXT} \propto (k_L - k_C) \tag{2.11}$$

where k_L and k_C represent inductive and capacitive coupling coefficients.

If k_L and k_C are approximately equal, cancellation occurs and FEXT is reduced. This explains why symmetric routing configurations can exhibit reduced far-end crosstalk [3, 10].

In addition, FEXT accumulates along the length of the coupled region, making it more dependent on trace length compared to NEXT.

2.3.4 Dependence on Geometry and Routing

Crosstalk magnitude is strongly influenced by physical layout parameters. The most important factors include distance between traces, length of parallel routing, layer configuration, and the quality of the return path.

Reducing spacing increases electric field interaction and leads to stronger coupling. Similarly, longer parallel routing sections increase the coupling length and therefore amplify the overall crosstalk.

Routing on adjacent layers does not eliminate coupling, but instead creates broadside coupling, which can also be significant depending on dielectric thickness.

2.3.5 Relation to Practical PCB Design

In practical inverter PCB designs, crosstalk is often observed between fast-switching control signals and sensitive communication lines. Even when signals operate at

relatively low frequencies, fast edges introduce high-frequency components that drive coupling.

Understanding these mechanisms is essential for designing robust layouts, where trace spacing, routing strategy, and layer configuration are carefully controlled to minimize interference [2, 11].

2.4 DC Resistance and Current Distribution

2.4.1 DC Resistance of Conductors

The resistance of a conductor is given by

$$R = \rho \frac{L}{A} \tag{2.12}$$

where ρ is the resistivity, L is the length, and A is the cross-sectional area.

Although this expression is straightforward, practical PCB geometries introduce non-uniform current distribution, which deviates from this simplified relation [12].

2.4.2 Current Density and Crowding

Current density is defined as

$$J = \frac{I}{A} \tag{2.13}$$

In real PCB layouts, current does not distribute uniformly. Instead, it tends to concentrate in regions with lower impedance paths. This leads to current crowding, particularly at vias, trace bends, and narrow sections [12, 11].

Current crowding increases local resistance and results in higher power dissipation, which directly affects both electrical performance and thermal behavior.

2.5 Thermal Behavior in PCBs

Thermal performance is a critical aspect of PCB design, particularly in high-power applications such as automotive inverter systems. In these systems, electrical losses in conductors and components are converted into heat, which must be effectively dissipated to ensure reliable operation [13, 14].

The temperature distribution in a PCB is governed by three primary heat transfer mechanisms, namely conduction, convection, and radiation. The relative importance of each mechanism depends on geometry, material properties, and operating conditions.

2.5.1 Heat Conduction in PCB Structures

Heat conduction is the dominant heat transfer mechanism within the PCB material and copper traces. It describes the transfer of thermal energy due to temperature gradients and is governed by Fourier's law

$$q = -k\nabla T \tag{2.14}$$

where q is the heat flux, k is the thermal conductivity, and ∇T is the temperature gradient [13].

In PCBs, copper has significantly higher thermal conductivity than dielectric materials. As a result, heat spreads more efficiently along copper planes and traces than through the substrate. This leads to anisotropic thermal behavior, where lateral heat spreading is more effective than vertical conduction.

2.5.2 Thermal Resistance and Temperature Rise

The temperature rise in a system can be expressed using thermal resistance

$$R_{th} = \frac{\Delta T}{P} \tag{2.15}$$

where ΔT is the temperature difference between the source and the surroundings, and P is the dissipated power [13, 14].

Thermal resistance represents the difficulty of heat transfer through the system. In PCB design, it consists of multiple contributions, including conduction through materials, heat spreading, convection to the surrounding air, and radiation from the surface.

A high thermal resistance results in a larger temperature rise for a given power dissipation, which can negatively affect component lifetime and system reliability.

2.5.3 Convective and Radiative Heat Transfer

Heat transfer from the PCB to the surrounding environment occurs primarily through convection and radiation.

Convective heat transfer can be approximated as

$$q_{conv} = h(T_s - T_a) \tag{2.16}$$

where h is the convective heat transfer coefficient, T_s is the surface temperature, and T_a is the ambient temperature.

Radiative heat transfer follows the Stefan–Boltzmann law

$$q_{rad} = \epsilon\sigma(T_s^4 - T_a^4) \tag{2.17}$$

where ϵ is the emissivity and σ is the Stefan–Boltzmann constant [13].

At lower temperatures, convection dominates heat transfer, while at higher temperatures radiation becomes more significant due to its strong dependence on temperature.

2.5.4 Effect of Material Properties

Material properties have a strong influence on thermal performance. Copper enables efficient heat spreading, whereas dielectric materials typically have lower thermal conductivity and act as thermal barriers.

Additional layers, such as conformal coatings, also influence heat transfer. These coatings are commonly used for environmental protection but introduce additional thermal resistance due to their low thermal conductivity.

2.5.5 Impact of Conformal Coating

The presence of a conformal coating affects both conduction and convection at the PCB surface. The coating introduces an additional thermal barrier through which heat must be transferred.

At lower temperatures, the impact of this additional resistance is limited due to smaller temperature gradients. However, at higher temperatures, the increased heat flux makes the system more sensitive to this added resistance.

In such conditions, the conformal coating can act as a thermal bottleneck, reducing heat dissipation and leading to higher operating temperatures [14].

2.5.6 Relation to Practical PCB Design

In practical inverter PCB designs, thermal behavior is closely coupled with electrical performance. Regions with high current density, such as vias and narrow traces, generate localized heating due to increased resistive losses.

This implies that layout decisions affecting current distribution also influence temperature distribution. Therefore, optimizing PCB design requires a combined consideration of both electrical and thermal effects [15, 16].

2.6 Electromagnetic Interference and Plane Resonance

Electromagnetic interference (EMI) is a major challenge in high-speed electronic systems, particularly in automotive inverter PCBs where fast switching signals coexist with power distribution networks. EMI originates from unintended electromagnetic radiation or coupling between different parts of the circuit, leading to signal distortion, performance degradation, or failure to meet regulatory requirements.

In PCB structures, EMI is strongly influenced by layout geometry, return paths, and the interaction between signal traces and power distribution networks. One of the dominant mechanisms for EMI generation is the excitation of resonances in the power and ground planes.

2.6.1 Power Distribution Network as a Resonant Structure

The power distribution network (PDN) of a PCB typically consists of parallel power and ground planes, which can be modeled as a cavity structure capable of supporting electromagnetic wave propagation.

The resonance frequencies of such a cavity can be approximated as

$$f_{mn} = \frac{c}{2\sqrt{\varepsilon_r}}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2} \tag{2.18}$$

where a and b represent the dimensions of the PCB plane, ε_r is the relative permittivity of the dielectric material, and m and n are the mode indices [17, 18].

At these resonance frequencies, the impedance of the PDN increases significantly, resulting in large voltage variations between the planes. This makes the structure highly sensitive to excitation from nearby signal traces.

2.6.2 Signal-Induced Excitation of Resonance

Digital signals with fast rise times contain a wide range of frequency components extending well beyond the fundamental clock frequency. The effective bandwidth of such a signal can be approximated as

$$f_{max} \approx \frac{0.35}{t_r} \tag{2.19}$$

where t_r is the rise time of the signal.

Even if the fundamental frequency is relatively low, higher-order harmonics can extend into the megahertz or gigahertz range. When one of these harmonic components coincides with a resonance frequency of the PCB plane, strong excitation occurs [15, 10].

This excitation leads to increased electromagnetic field intensity, which can be observed both as near-field coupling and far-field radiation.

2.6.3 Coupling Mechanisms Between Signal and Plane

The coupling between signal traces and the power plane occurs primarily through capacitive and inductive interactions.

Capacitive coupling arises from electric fields between the signal trace and the reference plane. When the signal trace references a power plane instead of a continuous ground plane, the electric field can directly excite the plane.

Inductive coupling arises from time-varying currents that generate magnetic fields, which induce currents in nearby conductive structures. These induced currents can further excite resonant modes in the plane.

The induced voltage due to these mechanisms can be described qualitatively as

$$V_{induced} \propto \frac{dV}{dt} \tag{2.20}$$

for capacitive coupling, and

$$V_{induced} \propto \frac{dI}{dt} \tag{2.21}$$

for inductive coupling.

This indicates that fast switching edges, rather than low-frequency operation, are the primary contributors to EMI generation [10, 16].

2.6.4 Near-Field and Far-Field Radiation

The electromagnetic fields generated by PCB structures can be categorized into near-field and far-field regions.

The near-field region is dominated by reactive electric and magnetic fields that exist close to the PCB surface. These fields do not propagate over long distances but can strongly couple to nearby circuits and cause interference.

The far-field region consists of radiated fields that propagate away from the PCB and contribute to electromagnetic emissions that must meet regulatory limits.

At resonance, both near-field and far-field radiation increase due to the high impedance of the PDN, which allows larger voltage variations between the planes.

2.6.5 Effect of Decoupling Capacitors

Decoupling capacitors are used to reduce the impedance of the power distribution network and suppress resonant behavior.

The impedance of a capacitor is given by

$$Z_C = \frac{1}{j\omega C} \tag{2.22}$$

At higher frequencies, the capacitor provides a low-impedance path between the power and ground planes, effectively reducing voltage fluctuations [19, 18].

When placed close to excitation sources or resonant hotspots, decoupling capacitors damp resonances by reducing the stored energy and lowering the quality factor of the cavity.

This results in reduced electromagnetic emissions and improved stability of the power distribution network.

2.6.6 Relation to Practical PCB Design

In practical inverter PCB designs, EMI is often caused by the interaction between fast-switching signals and resonant structures in the power distribution network.

Signals such as clock lines or PWM control signals can excite plane resonances through their harmonic content, resulting in increased electromagnetic radiation.

The theory presented in this section explains the behavior observed later in the thesis, where resonance in the power plane is excited by signal harmonics and subsequently reduced using a decoupling capacitor.

This demonstrates that EMI behavior in PCB design is strongly influenced by both signal characteristics and layout geometry, and must be addressed through careful design of signal routing and power distribution networks [15, 20].

3

Case Set-up

3.1 Overview of the Study

The work presented in this thesis is carried out using simplified test structures designed to isolate and analyze fundamental electrical phenomena in PCB interconnects. These structures enable a clear understanding of the impact of layout features such as vias, trace spacing, and return paths on signal integrity and electromagnetic behavior.

A simulation-driven approach is used to investigate these effects systematically, ensuring that individual mechanisms can be studied independently of system-level complexity.

To validate the observed behavior, dedicated hardware test boards are implemented for selected cases, specifically for signal integrity and electromagnetic interference (EMI) analysis. These measurements provide experimental support for the trends identified through simulations.

3.2 Simulation Environment and Tools

The PCB layouts used in this work are developed using Altium Designer, which enables precise control of stack-up definition, routing geometry, and design constraints [21].

Electromagnetic and electrical simulations are performed using ANSYS SIwave, which is used for signal integrity, DCIR, and EMI analysis [22]. Thermal simulations are carried out using ANSYS Icepak, where power dissipation from electrical simulations is used as input [23].

For signal excitation and system-level modeling, ANSYS AEDT Circuit is used to define realistic switching behavior and signal conditions. This tool chain enables a consistent simulation workflow across electrical and thermal domains.

3.3 PCB Set-up

3.3.1 Signal Integrity Test Board Structures

The signal integrity test board is designed to isolate fundamental high-frequency effects in PCB interconnects. Each structure is implemented with controlled geometry so that specific physical mechanisms can be analyzed independently.

All structures are implemented using an identical multilayer stack-up, ensuring that variations in electrical behavior arise only from geometric differences. The stack-up used in this work is shown in Figure 3.1.

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
1	Top Layer		Signal	1oz	0.035mm		
	Dielectric 6	PP-006	Prepreg		0.0994mm	4.1	0.02
2	Layer 2	CF-004	Signal	1/2oz	0.0152mm		
	Dielectric 2	PP-006	Prepreg		0.55mm	4.1	0.02
3	Layer 3	CF-004	Signal	1/2oz	0.0152mm		
	Dielectric 3	FR-4	Prepreg		0.1088mm	4.8	
4	Layer 4	CF-004	Signal	1/2oz	0.0152mm		
	Dielectric 4	PP-006	Prepreg		0.55mm	4.1	0.02
5	Layer 5	CF-004	Signal	1/2oz	0.0152mm		
	Dielectric 7	PP-006	Prepreg		0.0994mm	4.1	0.02
6	Bottom Layer		Signal	1oz	0.035mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
	Bottom Overlay		Overlay				

Figure 3.1: Layer stack-up used in the signal integrity test board.

The PCB consists of multiple signal and dielectric layers with defined thicknesses and material properties. The outer copper layers have a thickness of approximately 35 μm (1 oz copper), while the inner layers use thinner copper of approximately 15 μm (1/2 oz copper). The dielectric layers are primarily FR-4 and prepreg materials with relative permittivity values in the range of 4.1 to 4.8.

The dielectric thicknesses vary between approximately 0.1 mm and 0.55 mm, resulting in a total stack-up thickness comparable to that used in industrial automotive inverter PCBs. This ensures that the propagation environment and coupling mechanisms closely represent real applications.

The overall geometry of the signal integrity test board is shown in Figure 3.2.

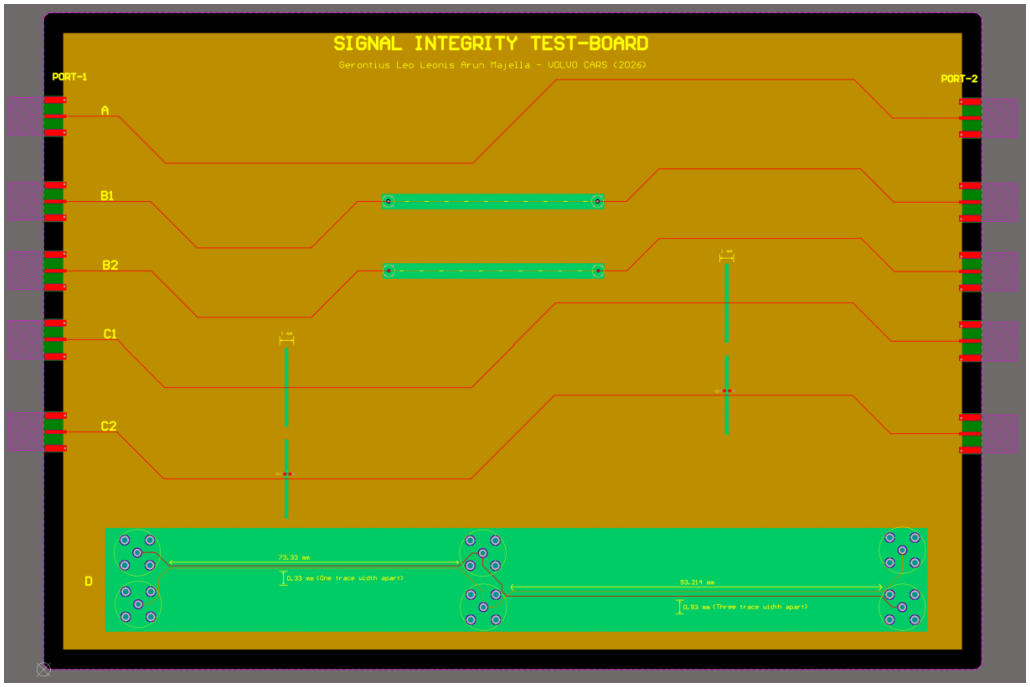

Figure 3.2: Signal integrity test board layout showing structures A, B, C, and D.

3.3.1.1 Structure A – Baseline Transmission Line

Structure A serves as the reference case for signal propagation in the test board. As shown in Figure 3.3, the structure consists of a single-ended transmission line routed between Port 1 and Port 2 without intentional discontinuities such as vias or nearby coupled traces.

Figure 3.3: Structure A consisting of a single-ended transmission line between Port 1 and Port 2.

The trace width is selected based on the stack-up to achieve a characteristic impedance close to 50 Ω. A continuous reference plane is maintained beneath the trace, allowing the return current to flow directly below the signal path and minimizing loop inductance.

Since no intentional discontinuities are introduced, the signal is expected to propagate with minimal reflection. This structure therefore serves as a baseline for comparison with the other test structures.

3.3.1.2 Structure B – Via Transition and Stub Effect

Structure B is designed to investigate the effect of via transitions on signal integrity, with particular focus on the influence of via stubs. As shown in Figure 3.4, the signal trace transitions from the top layer to internal signal layers and then returns back to the top layer through plated through-hole vias.

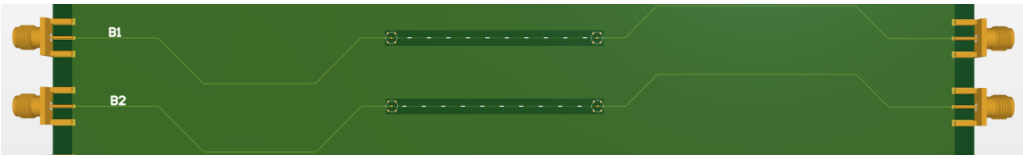

Figure 3.4: Structure B showing signal transition through vias between layers.

The vertical transition introduces a discontinuity in the transmission path, as the signal propagates between different layers of the PCB stack-up. The via extends through the full thickness of the board, while only a portion of the via is used for signal routing.

Two configurations are implemented in this structure:

- B1: the via stub is left intact, resulting in an unused portion of the via barrel below the signal layer
- B2: the via stub is removed using a back-drilling process, eliminating the unused portion of the via

The unused portion of the via, present in B1, behaves as an open-ended stub that introduces frequency-dependent impedance variation. The back-drilled via structure within the multilayer PCB is illustrated in Figure 3.5.

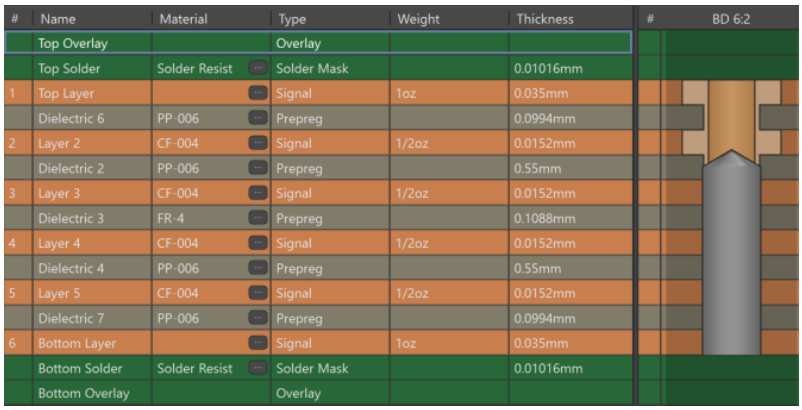

Figure 3.5: Via structure within the multilayer stack-up illustrating the removal of the unused stub using back-drilling.

In the B1 configuration, the unused via segment causes additional reflections and increased insertion loss at higher frequencies due to its resonant behavior. In con-

trast, B2 reduces these effects by removing the stub through back-drilling, resulting in improved signal transmission.

This structure enables direct comparison of via implementations and demonstrates the impact of stub removal on high-frequency performance.

3.3.1.3 Structure C – Return Path Disruption

Structure C is designed to investigate the effect of return-path discontinuities on signal integrity. As shown in Figure 3.6, the reference plane beneath the signal trace is intentionally interrupted using a slot.

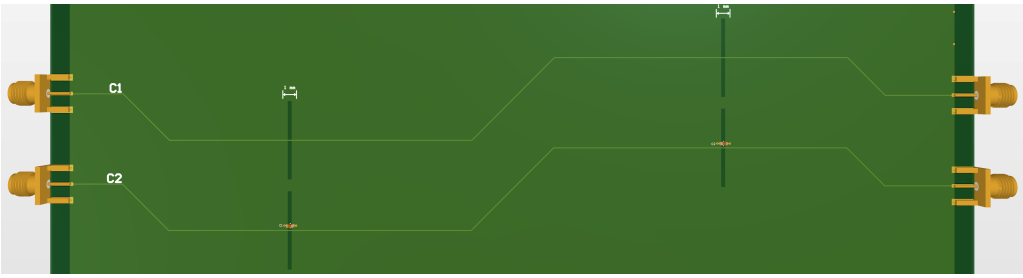

Figure 3.6: Structure C showing return-path discontinuity with a 1 mm plane split and stitching capacitor.

The width of the discontinuity gap is approximately 1 mm, which prevents the return current from flowing directly beneath the signal trace. As a result, the return current is forced to take a longer path around the split, increasing the loop area and inductance.

Two configurations are implemented:

- C1: plane split without stitching capacitor
- C2: plane split with a 100 nF capacitor placed across the split

In the C1 configuration, the absence of a direct return path leads to increased loop inductance and degraded signal transmission, resulting in higher insertion loss.

In the C2 configuration, the 100 nF capacitor provides a low-impedance path at high frequencies, allowing the return current to effectively bypass the discontinuity. This reduces loop inductance and improves signal propagation.

This structure enables evaluation of the impact of return-path integrity and demonstrates the effectiveness of stitching capacitors in mitigating signal degradation caused by plane discontinuities.

3.3.1.4 Structure D – Crosstalk Coupling

Structure D is designed to evaluate electromagnetic coupling between adjacent signal traces. As shown in Figure 3.7, two parallel traces are routed over a controlled length to study crosstalk behavior.

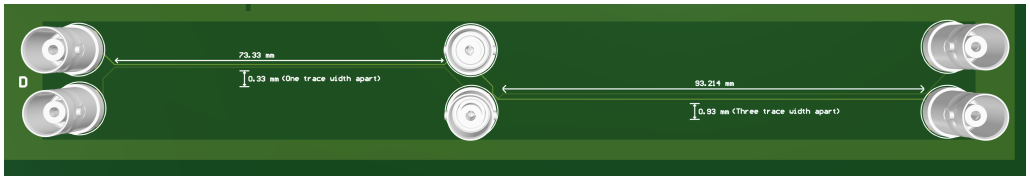

Figure 3.7: Structure D showing parallel trace routing with controlled spacing and coupling length.

The traces are routed in parallel over two distinct regions with different spacing. In the first region, the spacing between the traces is approximately 0.33 mm, corresponding to one trace width ($1W$), which results in strong coupling. In the second region, the spacing is increased to approximately 0.93 mm, corresponding to three times the trace width ($3W$), leading to reduced coupling.

The parallel routing lengths are approximately 73.33 mm and 93.21 mm for the two regions, respectively, allowing the coupling effects to accumulate along the transmission path.

This structure is used to investigate:

- near-end crosstalk (NEXT)
- far-end crosstalk (FEXT)
- the influence of trace spacing and coupling length

The controlled variation in spacing and routing length enables a clear comparison of coupling strength, demonstrating how layout geometry influences electromagnetic interference between adjacent signals.

3.3.2 DC Resistance Test Board Structures

The DCIR test board is designed to evaluate current distribution, voltage drop, and resistive losses under different PCB layout conditions. The board includes multiple structures that isolate the impact of via density, trace geometry, routing features, and interaction between power and signal traces.

The overall layout of the test board is shown in Figure 3.8.

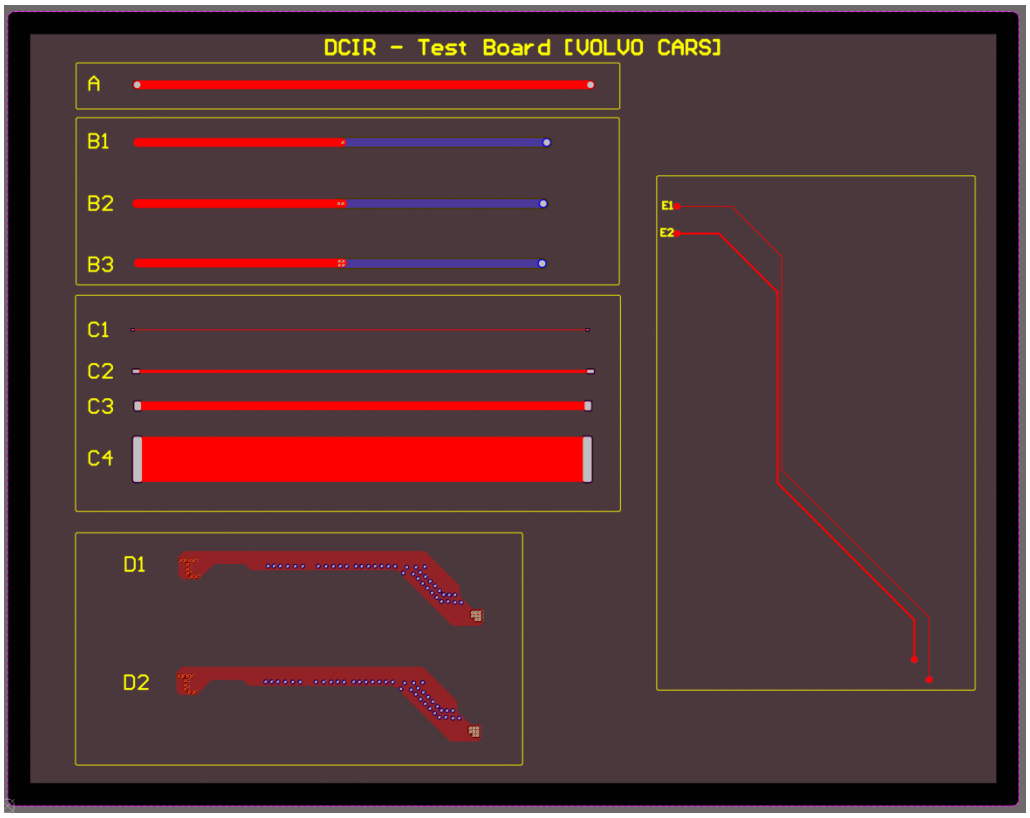

Figure 3.8: DC resistance test board showing structures A–E for evaluating current distribution and resistive behavior.

3.3.2.1 Structure A – Baseline Conductor

Structure A serves as the reference case for DC resistance analysis. As shown in Figure 3.9, the structure consists of a straight conductor with uniform width and length between the input and output terminals.

Figure 3.9: Structure A consisting of a uniform conductor used as a baseline for DC resistance evaluation.

The geometry is intentionally kept simple, with no vias, bends, or changes in cross-sectional area. This ensures that the current distribution remains uniform along the conductor.

The voltage drop across this structure is therefore primarily determined by the intrinsic resistance of the material, given by

$$R = \rho \frac{L}{A} \tag{3.1}$$

where ρ is the resistivity, L is the length of the conductor, and A is the cross-sectional area.

This structure is used as a baseline for comparison with the other test cases, allowing the impact of layout features such as vias, geometry changes, and routing variations on resistance and current distribution to be clearly identified.

3.3.2.2 Structure B – Via Array Effect

Structure B is designed to evaluate the effect of via arrays on current distribution and DC resistance. As shown in Figure 3.10, the current path transitions between layers through plated through-hole vias.

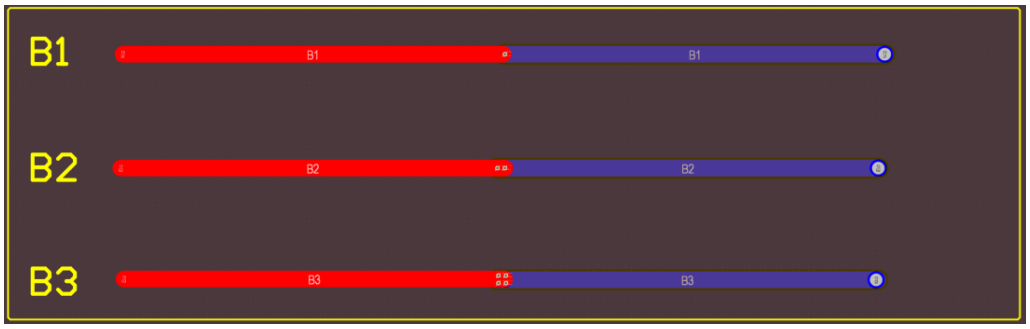

Figure 3.10: Structure B showing via arrays with increasing number of vias for current transition between layers.

Three configurations are implemented to investigate the influence of via count:

- B1: single via
- B2: two vias in parallel
- B3: four vias in parallel

In each case, the current flows from the top conductor to an internal layer through the via structures and continues along the routing path. The via transition introduces vertical current flow and non-uniform distribution due to the limited conductive path available.

This structure enables the evaluation of how via density affects current distribution, highlighting the importance of using multiple vias in high-current PCB designs to minimize resistive losses.

3.3.2.3 Structure C – Trace Width and Thermal Effect

Structure C is designed to investigate the effect of trace width on DC resistance, current distribution, and thermal behavior. As shown in Figure 3.11, multiple conductors with increasing width are implemented to study the impact of cross-sectional area.

Figure 3.11: Structure C showing conductors with increasing width from C1 to C4.

Four configurations are included:

- C1: 0.25 mm trace width
- C2: 0.75 mm trace width
- C3: 2 mm trace width
- C4: 10 mm wide conductor

As the trace width increases, the cross-sectional area available for current flow also increases, which reduces resistance according to

$$R = \rho \frac{L}{A} \tag{3.2}$$

and leads to lower voltage drop along the conductor.

In addition to electrical performance, trace width strongly affects thermal behavior. This structure is also used to evaluate thermal performance with and without conformal coating. The coating introduces additional thermal resistance, which limits heat transfer from the PCB surface. This effect is more pronounced for cases with

higher power dissipation, allowing the combined influence of electrical and thermal design parameters to be assessed.

3.3.2.4 Structure D – Effect of Polygon Geometry

Structure D is designed to investigate the effect of polygon geometry on current distribution and DC resistance. As shown in Figure 3.12, two configurations are implemented using wide copper polygon structures with different corner profiles.

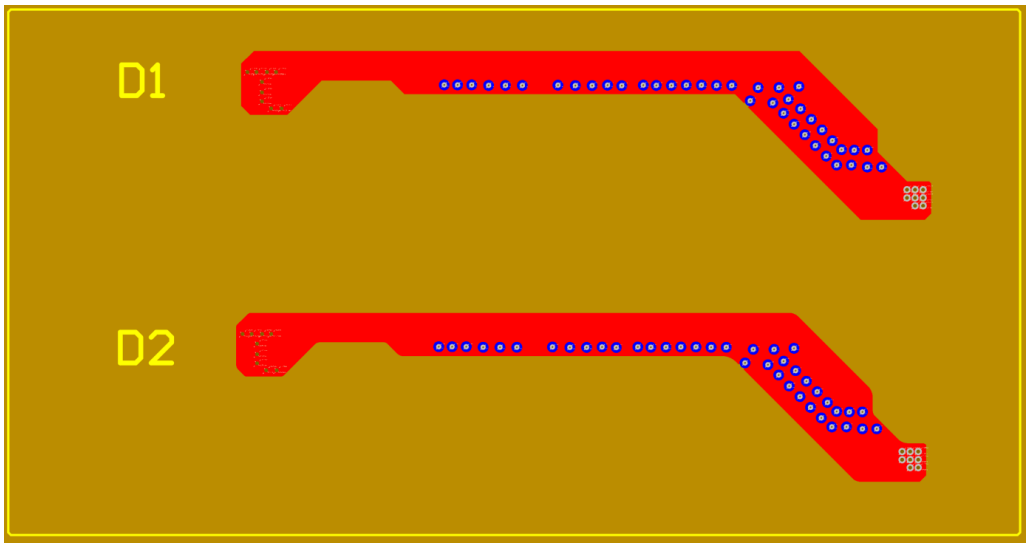

Figure 3.12: Structure D showing polygon routing with sharp corners (D1) and smooth corners (D2).

In the D1 configuration, the polygon includes sharp corners and abrupt transitions in geometry. In the D2 configuration, the polygon uses smooth, rounded transitions between segments.

This structure enables evaluation of how polygon design influences current flow in high-current PCB layouts, highlighting the importance of smooth transitions in power distribution paths.

3.3.2.5 Structure E – Power and Signal Trace Interaction

Structure E is designed to investigate the interaction between a power trace and a nearby signal trace. As shown in Figure 3.13, two traces are routed in close proximity along a shared path, allowing the influence of the power conductor on the adjacent signal trace to be evaluated.

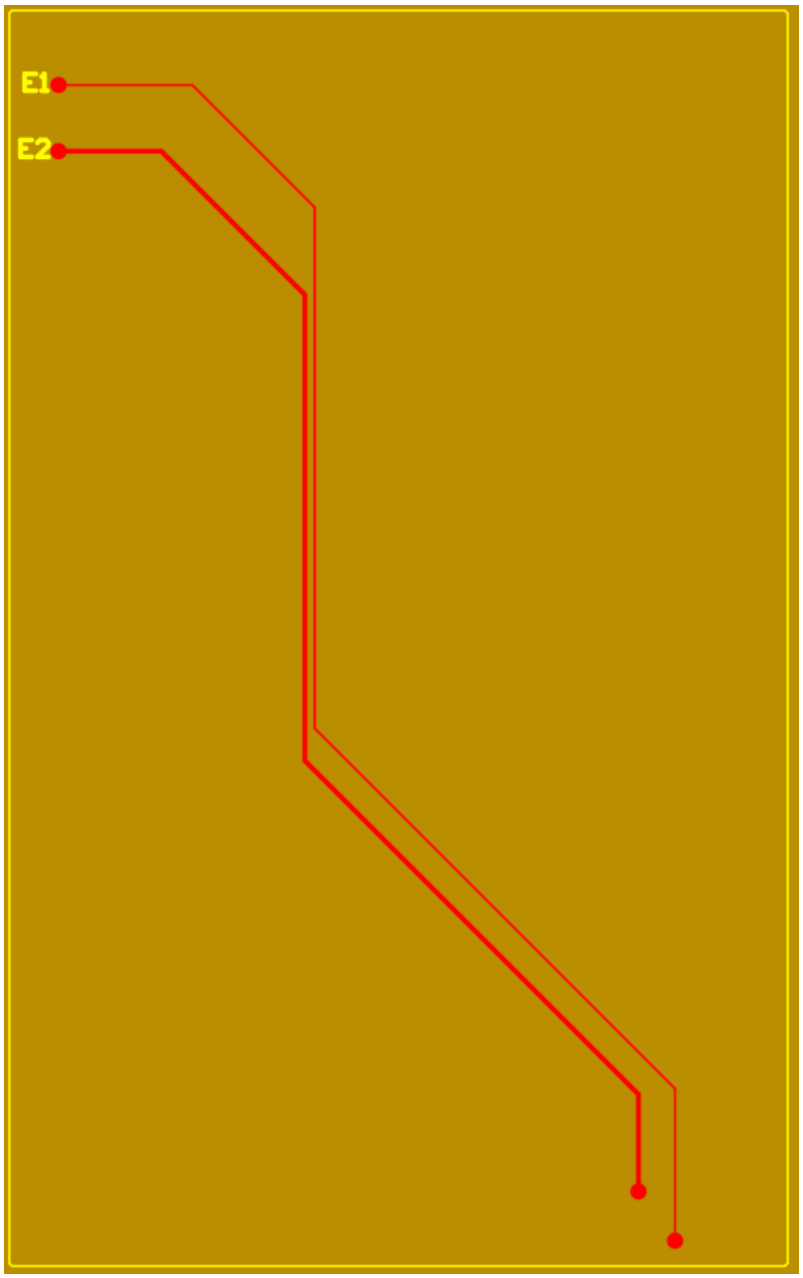

Figure 3.13: Structure E showing a power trace routed close to a parallel signal trace.

The structure consists of two routing paths, denoted as E1 and E2, which run parallel over a significant length and include multiple bends. One trace represents a high-current power path, while the other represents a signal line routed in close proximity.

The current flowing through the power trace generates electromagnetic fields, which can influence the adjacent signal trace. In addition, the presence of a nearby conductor affects current distribution and return path behavior, particularly in regions where the traces are closely spaced.

This structure is particularly relevant in practical PCB designs, where power and signal traces often share limited routing space, and improper placement can lead to performance degradation.

3.3.3 EMI Test Board

A dedicated EMI test board is used to analyze electromagnetic interference mechanisms related to power-plane resonances. The structure consists of a signal trace routed close to a power distribution plane, enabling coupling between the signal and the plane. A fast-switching signal is applied to excite resonant modes in the power-plane structure. The EMI test board is used to investigate:

- power-plane resonance excitation
- near-field electromagnetic emissions
- effect of decoupling capacitors

The layout of the EMI test board is shown in Figure 3.14.

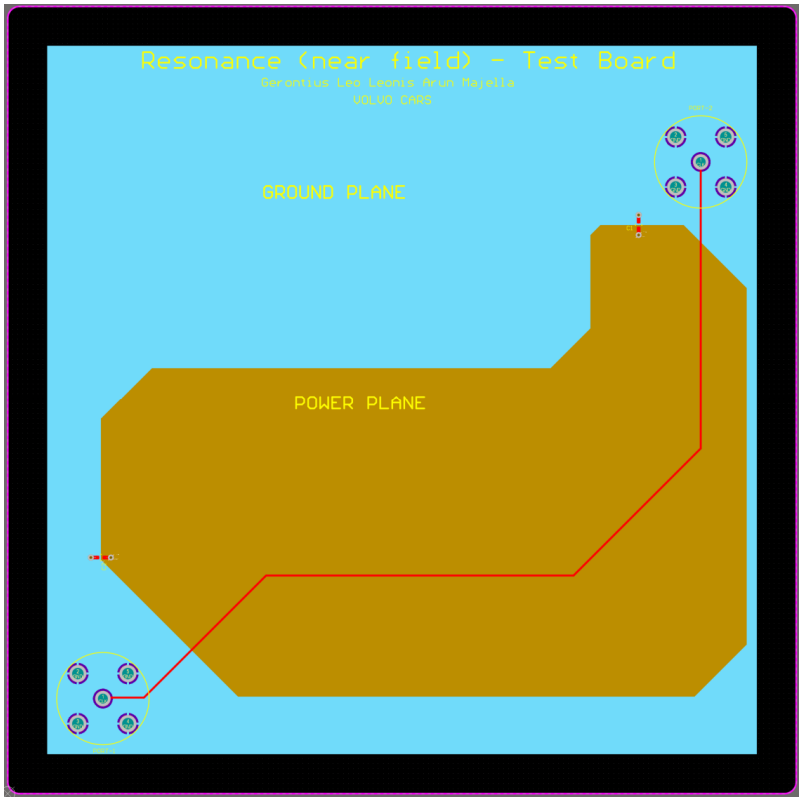

Figure 3.14: EMI test structure showing coupling between signal trace and power plane.

Both simulations and measurements are carried out for this structure to study EMI generation and mitigation.

3.4 Simulation Set-up

3.4.1 Signal Integrity Simulation Setup

Signal integrity simulations are performed on the SI test board using ANSYS SIwave to evaluate reflection, transmission, and coupling behavior. The complete PCB model used for the simulations is shown in Figure 3.15.

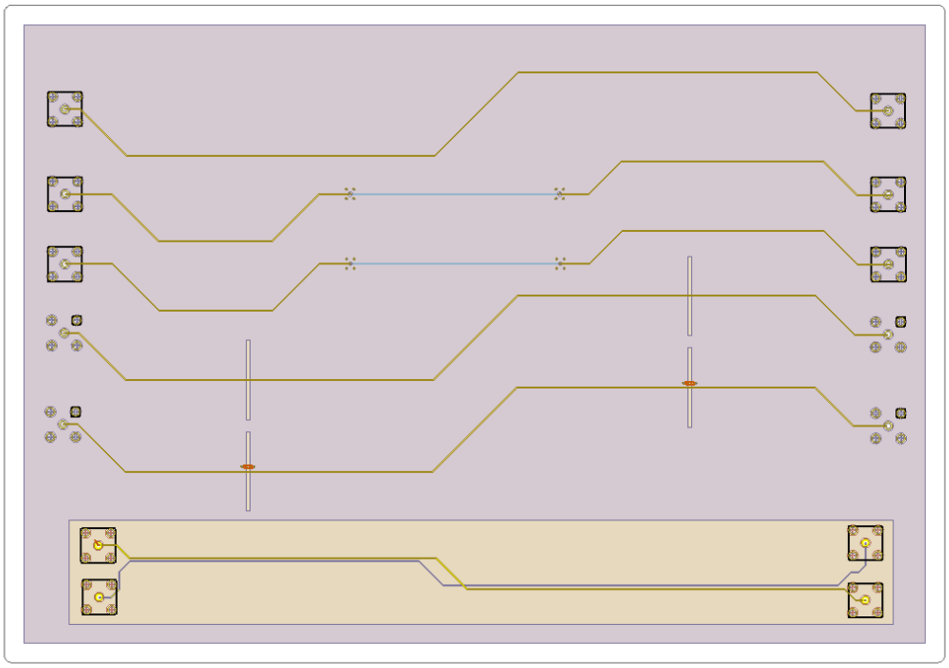

Figure 3.15: SIwave model of the signal integrity test board showing all structures used for simulation.

The model includes all test structures (A–D), each designed to isolate specific signal integrity effects such as impedance discontinuities, via transitions, return-path disruption, and crosstalk. The full PCB stack-up, including dielectric layers and copper thickness, is included to accurately model transmission line behavior.

Signal excitation is applied using wave ports defined at the input and output pads of each structure. The port configuration used in the simulation is illustrated in Figure 3.16.

The ports are defined with a reference impedance of 50 Ω, consistent with standard measurement systems used in hardware testing. The port region includes the signal pad and surrounding ground conductors, allowing accurate representation of both the signal excitation and the corresponding return current path.

Simulations are performed in the frequency domain. Different frequency ranges are selected for each structure based on the physical effects being analyzed:

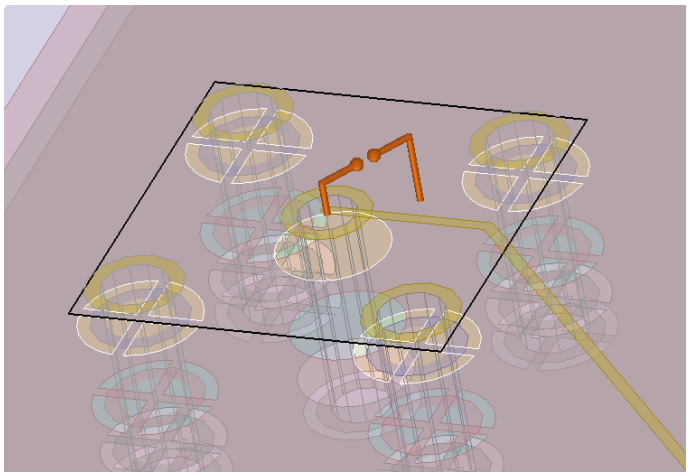

Figure 3.16: Wave port definition in SIwave showing port assignment at the PCB pads with reference conductors.

- Structure A: 1 MHz to 1 GHz
- Structure B: 1 MHz to 20 GHz
- Structure C: 1 MHz to 5 GHz

The extended frequency range for Structure B is required to capture the resonance behavior introduced by the via stub, while Structure C focuses on lower-frequency return-path effects.

For crosstalk analysis in Structure D, a time-domain excitation is used. The aggressor signal is defined with a driver amplitude of 1.5 V and a rise time of 30 ps. This fast transition ensures sufficient high-frequency content to excite both near-end and far-end coupling mechanisms.

The consistent simulation setup across all structures allows direct comparison of results, ensuring that differences in performance are solely due to layout variations.

3.4.2 DCIR Simulation Setup

DCIR simulations are performed using ANSYS SIwave to evaluate voltage drop, current distribution, and resistive losses in the PCB structures. The complete DCIR test board used for the simulations is shown in Figure 3.17.

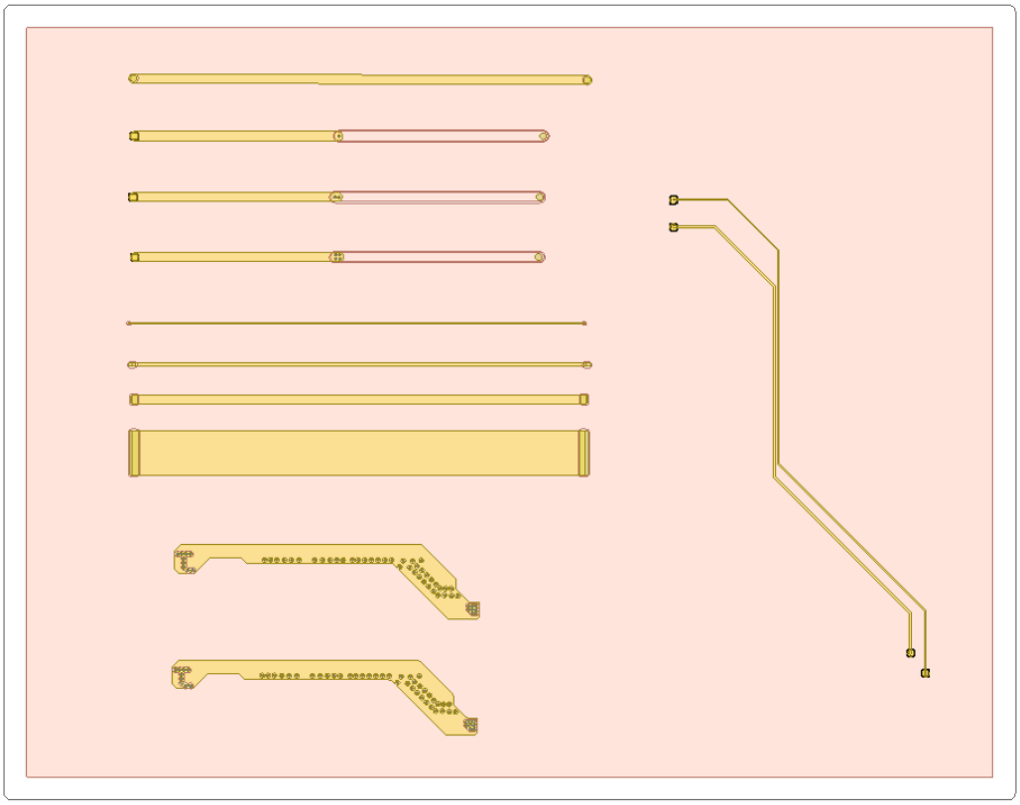

Figure 3.17: SIwave model of the DC resistance test board including all structures (A–E).

The model includes all structures (A–E), which are designed to investigate the effect of via arrays, trace width variations, polygon geometry, and interaction between power and signal traces. The full PCB stack-up is included in the simulation to accurately model current flow through the copper layers and vias.

A constant current source is applied at the input terminal of each structure, while the output terminal is defined as the return path. The resulting voltage drop across each structure is used to determine the effective DC resistance.

Different current levels are applied depending on the geometry of the structures:

- Structures A and B are simulated with a current of 2 A
- Structures C and D are simulated with a current of 5 A

The higher current applied to Structures C and D ensures sufficient power dissipation to observe current crowding and thermal effects in wider conductors and polygon geometries.

For Structure E, a combined circuit and field simulation approach is used to model

realistic operating conditions.

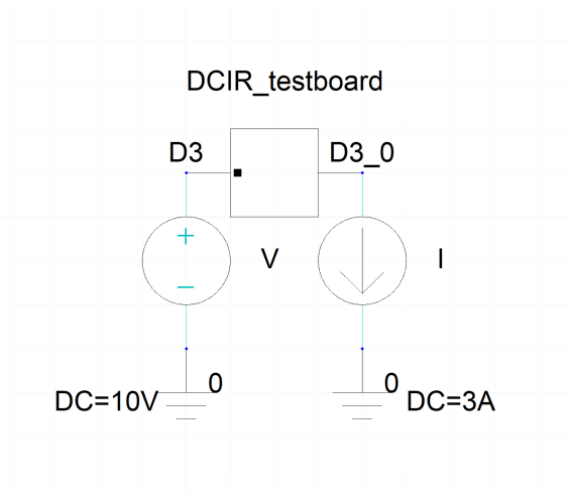

Figure 3.18: Nexxim transient circuit setup used for Structure E excitation.

The power trace (E1) is excited using a circuit model implemented in ANSYS Electronic Desktop (Nexxim). The excitation consists of a DC voltage source of 10 V and a current source of 3 A representing the operating current in the power path. A Nexxim transient simulation is performed to obtain time-domain current and voltage behavior in the circuit. The resulting waveforms are then exported and back-annotated into ANSYS SIwave.

The imported transient excitation is used as input for electromagnetic simulations in SIwave, allowing evaluation of near-field and far-field behavior under realistic operating conditions. This combined workflow enables analysis of the interaction between a high-current power trace and a nearby signal trace, capturing both electrical and electromagnetic effects.

In addition to voltage drop, current density distribution is extracted for all structures to identify regions of current crowding, particularly in vias, narrow traces, and sharp geometry transitions.

The power dissipation obtained from DCIR simulations is used as input for thermal simulations, enabling evaluation of temperature distribution under different operating conditions.

A consistent simulation framework is maintained across all structures, allowing direct comparison of the influence of layout variations on current distribution, resistive behavior, and electromagnetic performance.

3.4.3 EMI Simulation Setup

EMI simulations are performed on the dedicated test board to analyze electromagnetic coupling and power-plane resonance behavior. The PCB model used for the

EMI analysis is shown in Figure 3.19.

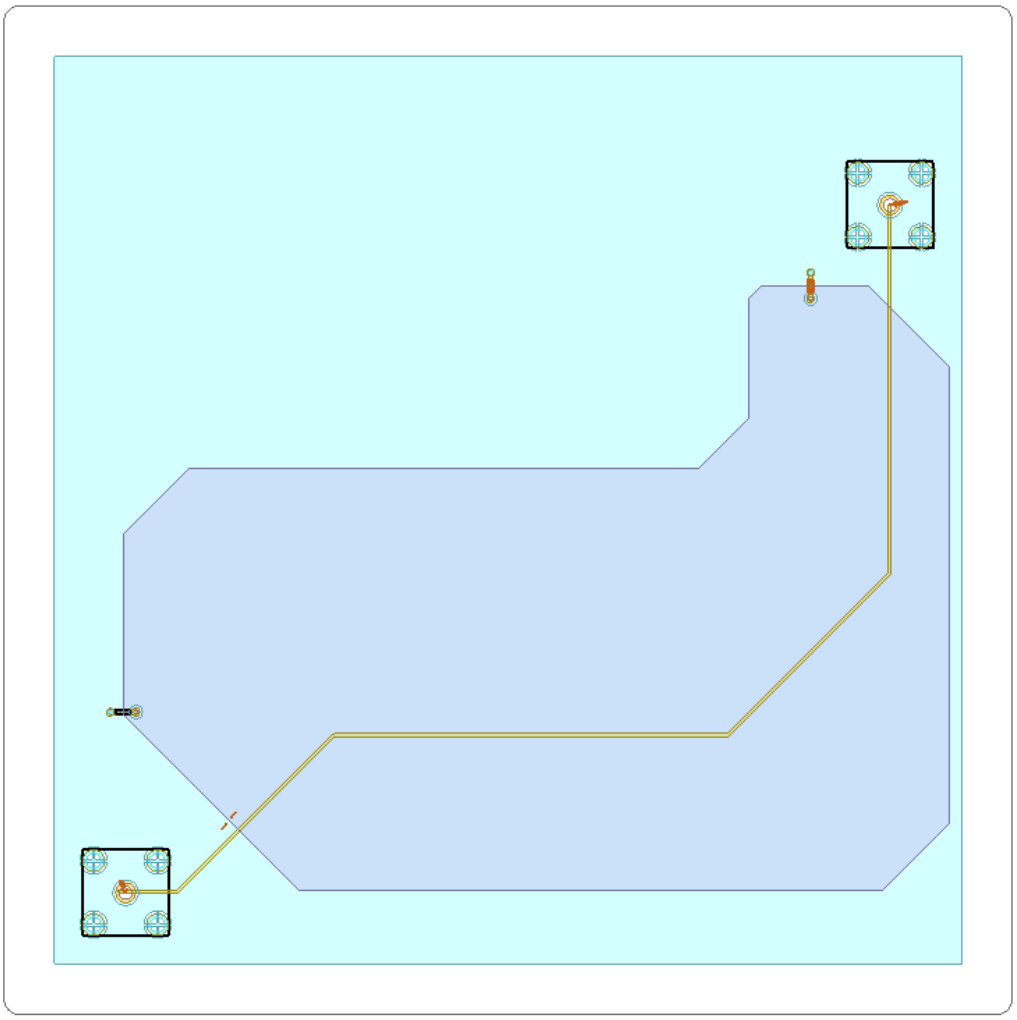

Figure 3.19: EMI test board used for investigating coupling between signal trace and power plane.

The structure consists of a signal trace routed over a power plane in an adjacent layer. This configuration enables coupling between the signal and the power distribution network, allowing investigation of resonance excitation.

The simulation workflow begins with identifying the resonant behavior of the power plane.

A resonant mode analysis is performed in ANSYS SIwave to determine the dominant resonance frequencies of the power-plane structure. To validate these results, a Z-parameter sweep is carried out across the power plane. Peaks in the impedance response confirm the resonance frequencies obtained from the modal analysis.

Once the dominant resonance frequency is identified, a circuit-level transient sim-

ulation is performed using ANSYS Electronic Desktop (Nexxim). The excitation circuit used for this purpose is shown in Figure 3.20.

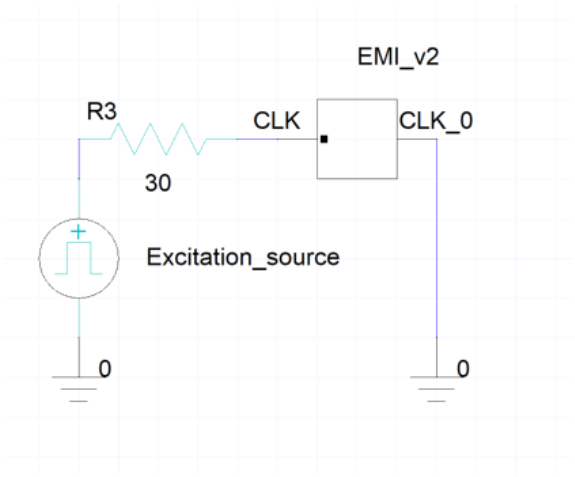

Figure 3.20: Nexxim circuit used to excite the signal trace with controlled source conditions.

The excitation signal is applied to the signal trace routed above the power plane. The frequency of the excitation is set equal to the identified resonance frequency of the power plane to ensure maximum coupling and worst-case electromagnetic behavior.

Using the imported excitation, electromagnetic simulations are conducted in SIwave. Near-field analysis is performed to observe the distribution of electromagnetic fields on the PCB and to evaluate how the signal trace excites the power-plane resonance.

The effect of decoupling capacitors is studied by placing capacitors at different locations on the power plane and repeating the simulations. The resulting field distributions are compared to evaluate how capacitor placement influences electromagnetic emissions.

This approach also allows identification of optimal locations for additional capacitor placement to reduce field intensity and mitigate EMI. The combined use of resonance analysis, circuit excitation, and field simulation provides a comprehensive understanding of EMI generation mechanisms and supports the development of effective mitigation strategies.

3.5 Hardware Measurement setup

3.5.1 Signal integrity test board

The hardware measurements were performed to validate the signal integrity behaviour predicted by the simulations. The measurement setup consisted of a Rohde & Schwarz ZNB Vector Network Analyzer (VNA), precision RF coaxial cables, SMA

connector adapters, and the fabricated signal integrity test board [24]. The complete measurement setup used during testing is shown in Figure 3.21.

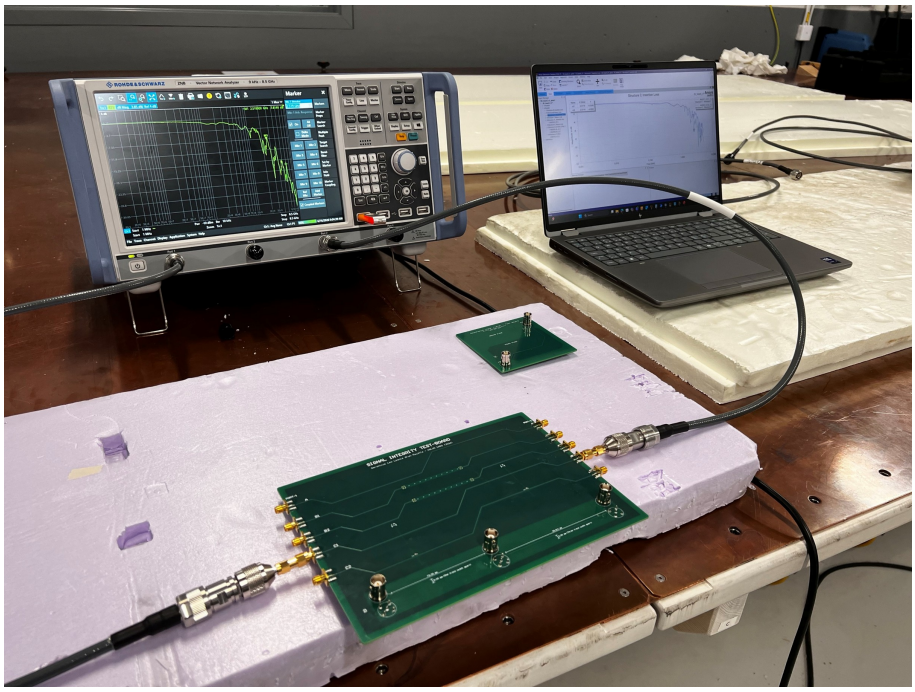

Figure 3.21: Overall signal integrity measurement setup including the VNA, test board, coaxial cables, and measurement computer.

A Rohde & Schwarz ZNB Vector Network Analyzer was used to measure the scattering parameters of the different test structures. The instrument supports broadband frequency-domain characterization and enables accurate measurement of both insertion loss (S_{21}) and return loss (S_{11}). The VNA used during the measurements is shown in Figure 3.22.

The fabricated signal integrity test board was connected to the VNA using coaxial cables terminated with SMA edge-launch connector adapters, as shown in Figure 3.23. The adapters provide a reliable transition between the measurement equipment and the PCB transmission lines while minimizing additional parasitic effects. Individual structures were measured by connecting the selected input and output ports to the VNA test ports.

For transmission and reflection measurements, a two-port VNA configuration was employed. Prior to testing, a full two-port calibration was performed using open, short, load, and thru (OSLT) standards to remove systematic errors introduced by cables, connectors, and adapters. The reference impedance was set to 50 Ω, consistent with both the PCB design and simulation setup.

The calibrated measurements provided the S-parameters of each test structure, enabling direct comparison with the corresponding simulation results. Insertion loss

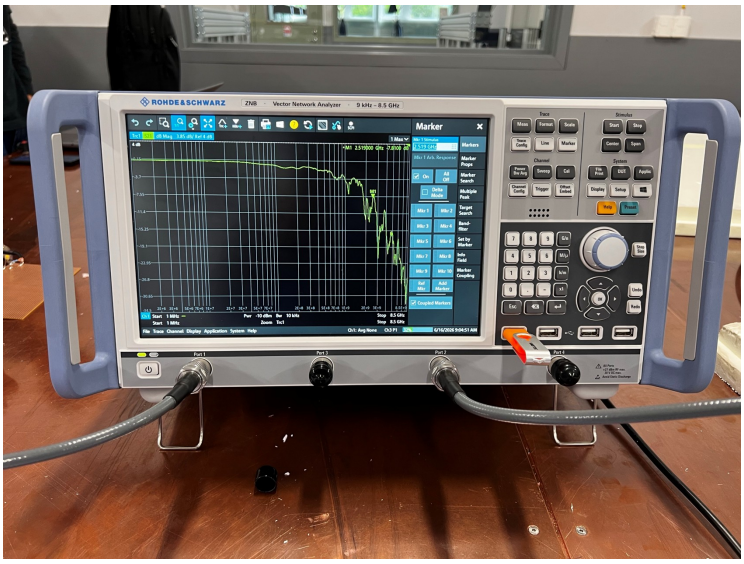

Figure 3.22: Rohde & Schwarz ZNB Vector Network Analyzer used for signal integrity measurements.

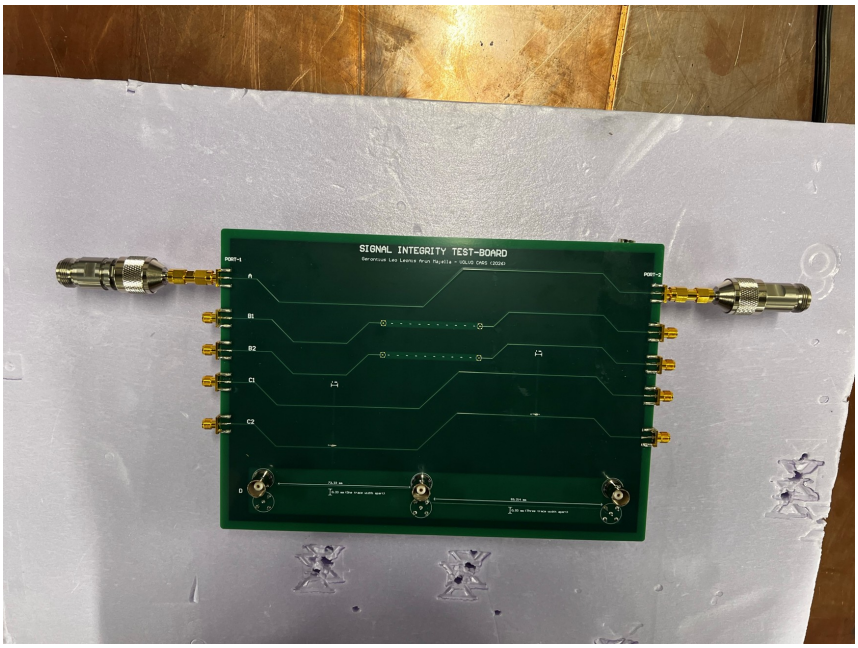

Figure 3.23: Signal integrity test board equipped with SMA connector adapters for VNA measurements.

(S_{21}) was used to evaluate signal transmission performance, while return loss (S_{11}) was used to assess impedance matching and signal reflections. For the crosstalk structure, a fast pulse signal with an amplitude of 1 V and a rise time of approximately 30 ps was applied to the aggressor trace. The induced voltages on the victim trace were then measured to determine the near-end crosstalk (NEXT) and far-end crosstalk (FEXT) levels.

The combination of hardware measurements and simulation results provides experimental validation of the investigated signal integrity phenomena, including transmission loss, via-stub effects, return-path discontinuities, and electromagnetic coupling between adjacent traces.

3.5.2 EMI test board

Hardware measurements were performed to validate the resonance behaviour and near-field emissions observed in the EMI simulations. The measurement setup consisted of a Tektronix 6-Series Mixed Signal Oscilloscope, which was used to generate the excitation signal, the fabricated EMI test board, and a Teledyne LeCroy NFP3000 near-field probe system for measuring the resulting electromagnetic emissions [25]. The complete measurement setup is shown in Figure 3.24.

An 80 MHz square-wave signal was generated using the integrated function generator of the Tektronix oscilloscope and applied to the signal trace routed adjacent to the power plane. The signal frequency was intentionally selected such that its harmonic content could excite the resonant modes of the power-plane structure. Resonance analysis performed during the simulation stage identified the dominant power-plane resonance at approximately 240 MHz, which closely corresponds to the third harmonic of the 80 MHz excitation signal.

Near-field emissions were measured using the Teledyne LeCroy NFP3000 near-field probe system. The probe was positioned above the region of interest on the PCB surface to capture the localized electromagnetic fields generated by the interaction between the signal trace and the resonant power plane. The measured near-field signals were transferred to the oscilloscope and analysed in the frequency domain using the integrated spectrum analysis functionality.

Two capacitor configurations were evaluated during the measurements. The first configuration utilized a single decoupling capacitor connected between the power and ground planes, while the second configuration included an additional decoupling capacitor placed at a location determined from the simulation results. The resulting near-field emission spectra were compared to evaluate the effectiveness of the decoupling strategy in suppressing power-plane resonance.

This measurement setup enabled direct experimental validation of the simulated EMI behaviour and provided insight into the relationship between signal harmonics, power-plane resonance, and near-field electromagnetic emissions.

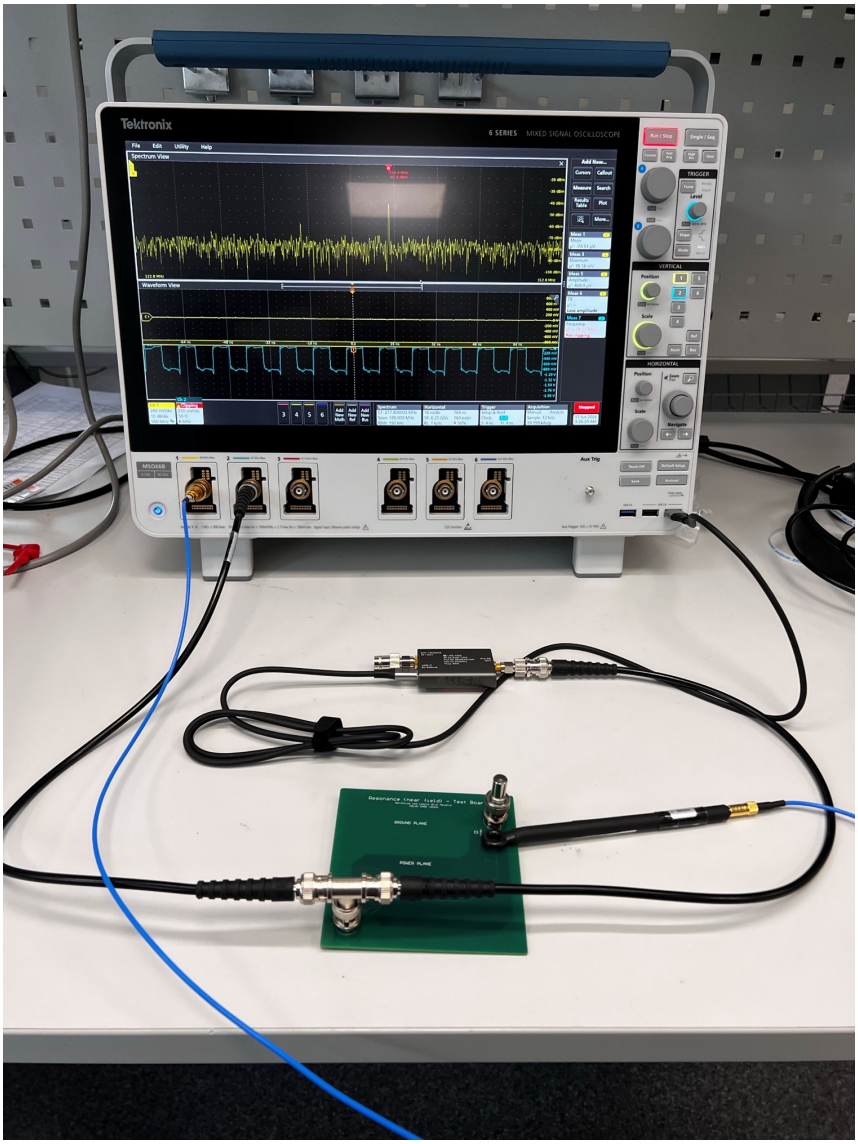

Figure 3.24: EMI measurement setup showing the Tektronix oscilloscope, EMI test board, and Teledyne LeCroy NFP3000 near-field probe.

4

Results

4.1 Signal integrity test board

4.1.1 Signal Integrity Results – Simulation

The signal integrity performance of the test structures is evaluated using SIwave simulations. Based on the theoretical expectations, each structure is analysed to identify the impact of layout variations on signal transmission.

Structure A – Baseline

Structure A is expected to exhibit minimal reflections due to the absence of discontinuities. The simulation results show low insertion loss and good transmission performance across the frequency range, confirming uniform impedance behaviour.

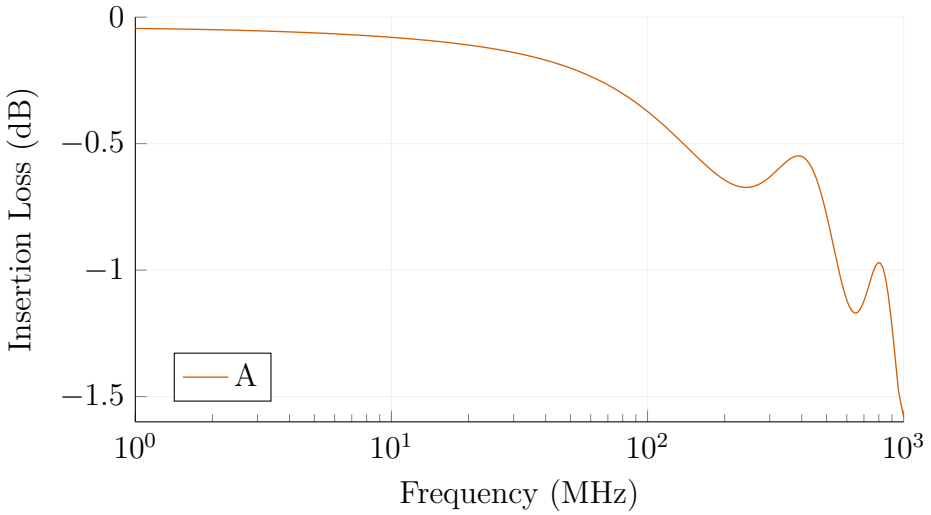

Figure 4.1: Structure-A Insertion Loss

Structure B – Via Stub Effect

The via stub in B1 is expected to introduce a frequency-dependent impedance dis-

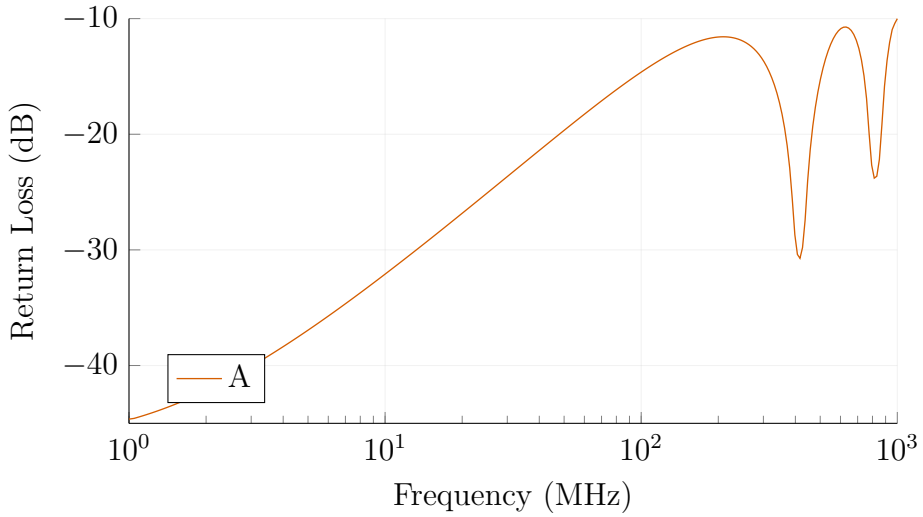

Figure 4.2: Structure-A Return Loss

continuity. The simulation results show increased insertion loss at higher frequencies for B1, while B2, with back-drilled vias, shows improved performance. This confirms the effect of stub-induced resonance.

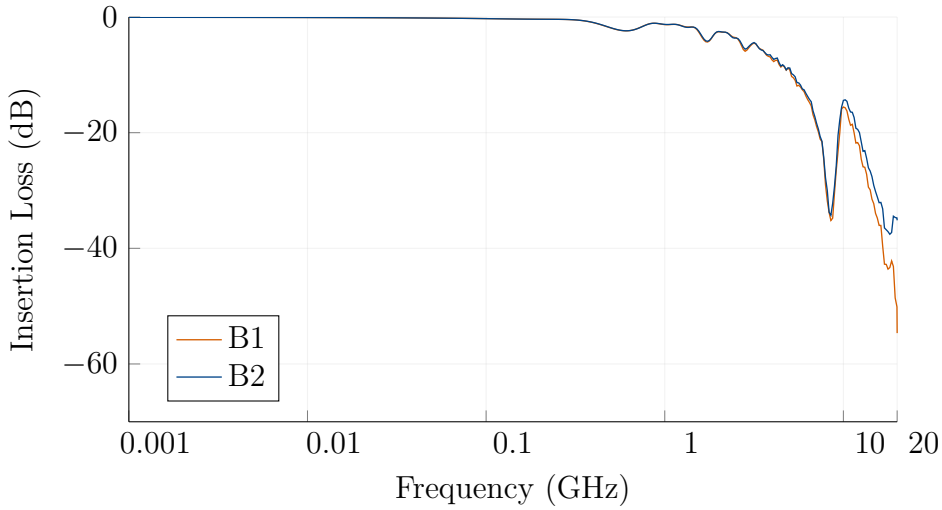

Figure 4.3: Structure-B Insertion Loss

Structure C – Return Path Disruption

The interruption of the return path is expected to increase loop inductance and degrade signal transmission. The results show higher insertion loss for the split-plane case (C1), while the addition of a 100 nF stitching capacitor (C2) improves the response by restoring high-frequency return current flow.

Structure D – Crosstalk

For crosstalk analysis, the aggressor signal with 1.5 V amplitude and 30 ps rise time

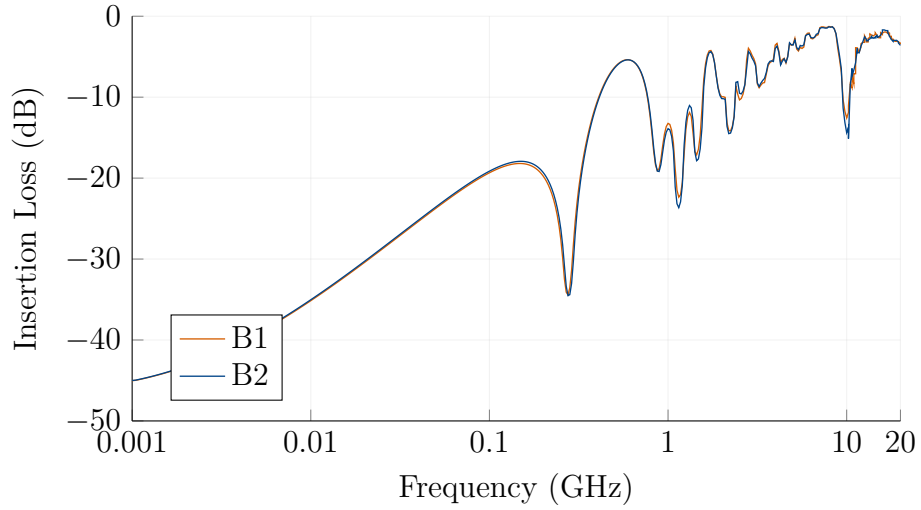

Figure 4.4: Structure-B Return Loss

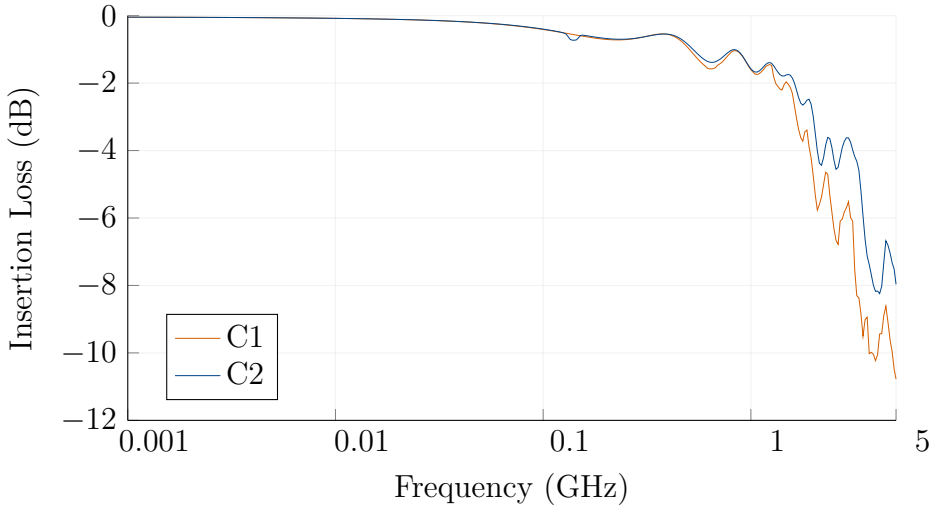

Figure 4.5: Structure-C Insertion Loss

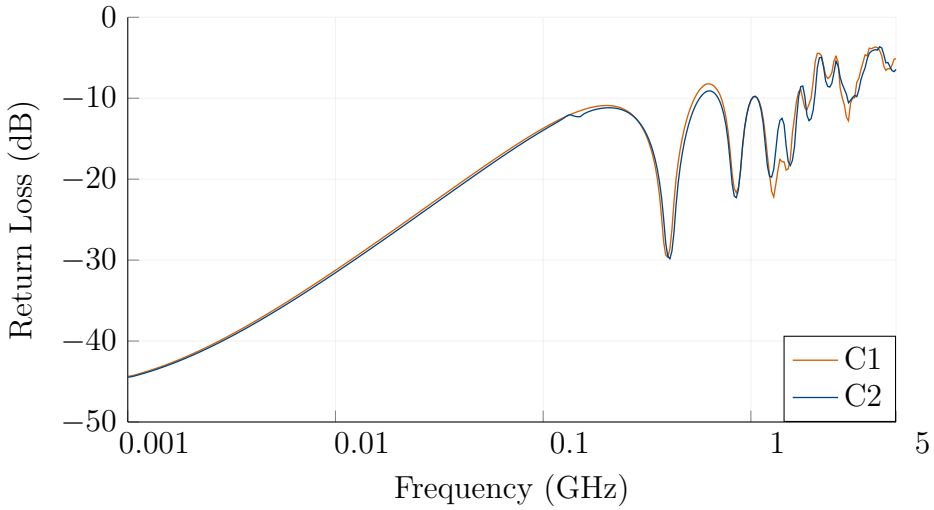

Figure 4.6: Structure-C Return Loss

introduces strong high-frequency components. The simulation results show that tight spacing (1W) leads to significantly higher coupling compared to 3W spacing. Both near-end and far-end crosstalk increase with reduced spacing and longer parallel routing.

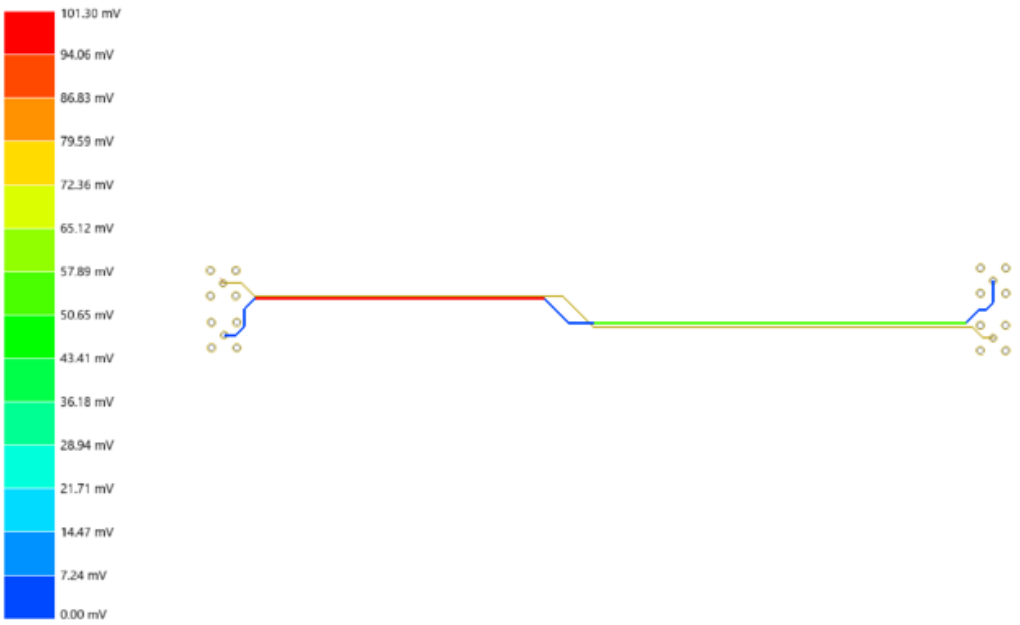

Figure 4.7: Structure-D Near end Crosstalk

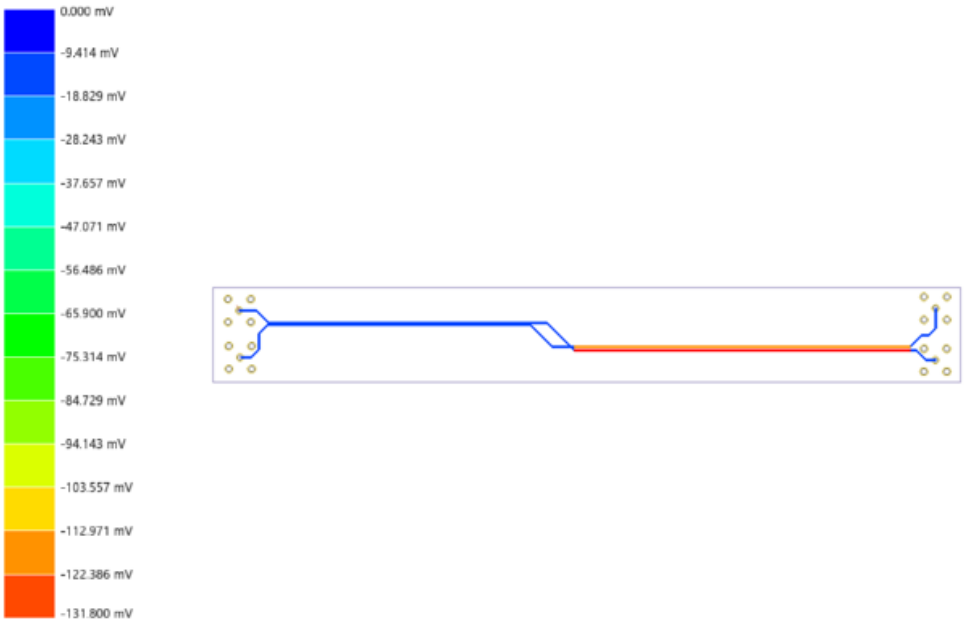

Figure 4.8: Structure-D Far end Crosstalk

4.1.2 Signal Integrity Results – Hardware Measurements

Structure A – Baseline

The hardware measurements for Structure A were performed using a Vector Network Analyzer (VNA) to evaluate the transmission and reflection characteristics of the baseline transmission line. The measured insertion loss and return loss are shown in Figures 4.9 and 4.10, respectively.

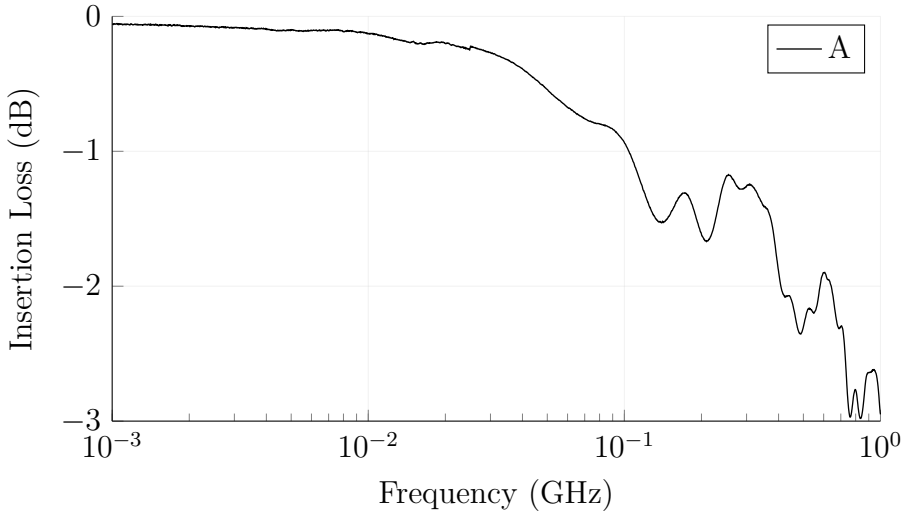

Figure 4.9: Structure A – Insertion Loss

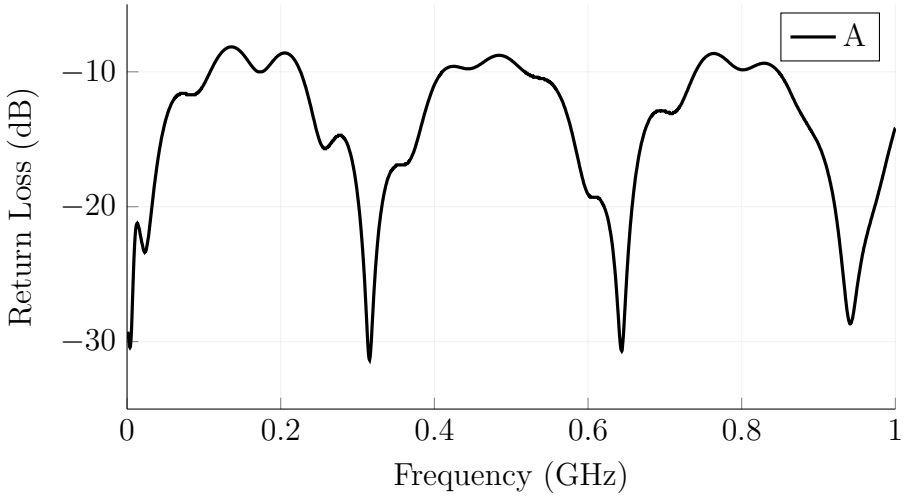

Figure 4.10: Structure A – Return Loss

The insertion loss remains close to 0 dB at lower frequencies and gradually decreases with increasing frequency, reaching approximately −3 dB near 1 GHz. This indicates that the transmission line exhibits low attenuation over most of the investigated frequency range. The increased attenuation at higher frequencies is primarily attributed to conductor and dielectric losses, which become more pronounced as frequency increases.

The return loss remains below approximately −10 dB throughout most of the frequency range, indicating acceptable impedance matching and limited signal reflections. Several local minima can be observed, corresponding to frequencies where the transmission line exhibits improved matching characteristics. Since the structure consists of a continuous transmission line with an uninterrupted reference plane, significant reflection mechanisms are not expected.

Overall, the measured results confirm the expected behaviour of the baseline structure and are in good agreement with the simulation results presented in Figures 4.1 and 4.2. The low insertion loss and acceptable return loss demonstrate that Structure A provides a stable transmission path and serves as a suitable reference for comparison with the remaining signal integrity test structures.

Structure B – Via Stub Effect

Structure B is used to investigate the influence of via stubs on signal transmission. The measured insertion loss and return loss for the conventional via structure (B1) and the back-drilled configuration (B2) are shown in Figures 4.11 and 4.12, respectively.

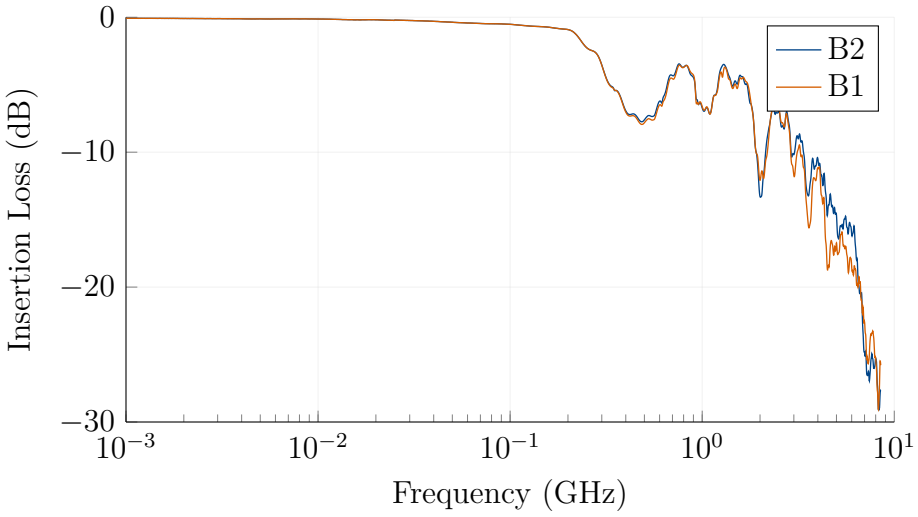

Figure 4.11: Structure B – Insertion Loss

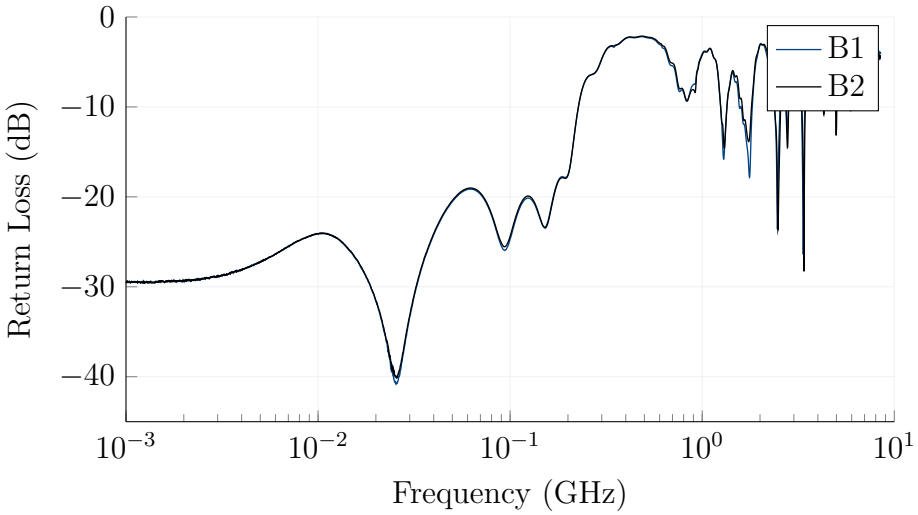

Figure 4.12: Structure B – Return Loss

The insertion loss results show that both structures exhibit similar performance at lower frequencies, where the effect of the via stub is limited. As the frequency increases, the transmission response becomes increasingly frequency dependent and several resonant features can be observed. B2 generally exhibits slightly lower insertion loss than B1 across portions of the higher-frequency range, indicating improved signal transmission due to the removal of the unused via stub. The difference becomes more noticeable as the frequency increases, where the resonant behaviour of the stub has a greater influence on the signal path.

The measured return loss results indicate that both configurations have similar reflection characteristics over much of the investigated frequency range. However, several resonant points can be observed at higher frequencies where the impedance

matching varies significantly. These resonances are associated with the via transition and the frequency-dependent behaviour introduced by the stub structure. The back-drilled configuration reduces the electrical length of the via and consequently mitigates the impact of the stub on the overall response.

Overall, the measurements confirm that via stubs introduce additional high-frequency degradation in the transmission path. The back-drilled configuration demonstrates improved signal integrity performance by reducing the frequency-dependent effects associated with the unused portion of the via barrel. Furthermore, the measured trends show good agreement with the simulation results presented in Figures 4.3 and 4.4, validating the simulated behaviour of the via structures.

Structure C – Return Path Disruption

The hardware results for Structure C are presented in Figures 4.13 and 4.14. The measurements compare the performance of the split-plane structure without a stitching capacitor (C1) and the structure with a 100 nF stitching capacitor placed across the split (C2). This comparison enables evaluation of the impact of return-path discontinuities on signal transmission.

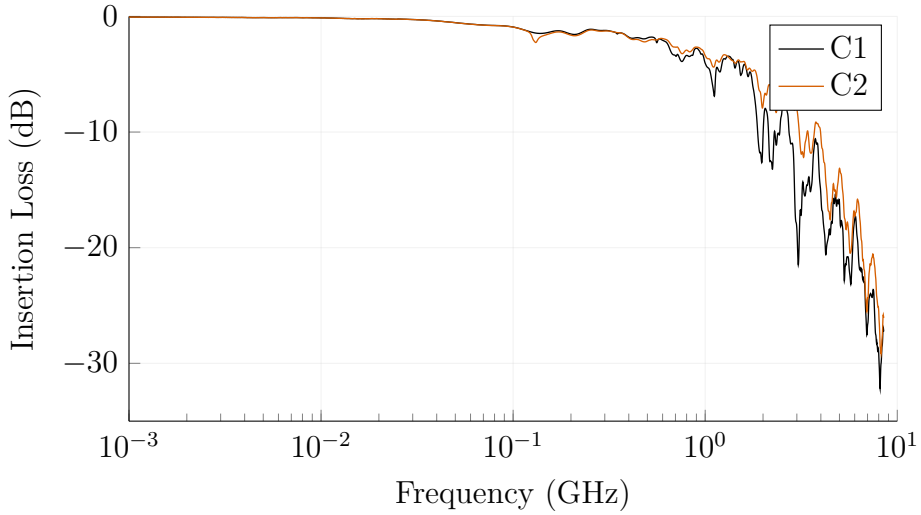

Figure 4.13: Structure-C Insertion Loss

The insertion loss results show similar behaviour for both configurations at lower frequencies, indicating that the return-path discontinuity has a limited effect in this region. As the frequency increases, the difference between the two structures becomes more apparent. C2 generally exhibits lower insertion loss than C1, particularly above 1 GHz, demonstrating improved signal transmission. This improvement is attributed to the stitching capacitor providing a low-impedance path for the high-frequency return current, thereby reducing the effective loop inductance introduced by the plane split.

The return loss measurements show that both structures exhibit comparable behaviour over a large portion of the investigated frequency range. However, several

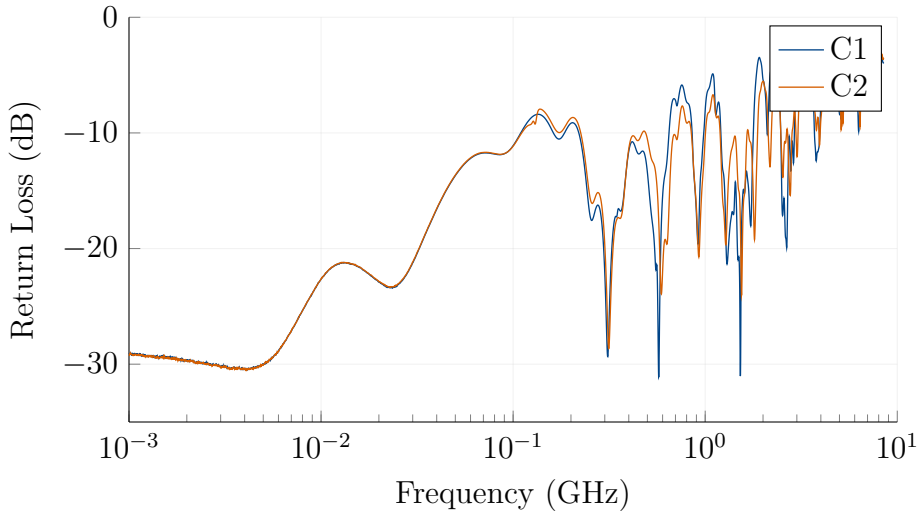

Figure 4.14: Structure-C Return Loss

resonant features are observed at higher frequencies due to the frequency-dependent nature of the return path. The structure with the stitching capacitor generally maintains slightly improved matching characteristics, indicating that the capacitor helps reduce the impedance discontinuity associated with the interrupted reference plane.

Overall, the measured results confirm that disruption of the return current path degrades signal transmission, particularly at higher frequencies. The addition of a stitching capacitor partially restores the return-path continuity and improves the high-frequency performance of the structure. Furthermore, the measured trends are consistent with the simulation results presented in Figures 4.5 and 4.6, validating the effectiveness of stitching capacitors in mitigating signal integrity degradation caused by reference-plane discontinuities.

Structure D – Crosstalk Coupling

Structure D is used to evaluate electromagnetic coupling between adjacent signal traces. The hardware measurements were performed for two different spacing configurations, namely 1W and 3W, and the results were compared with the corresponding simulation results. The measured and simulated near-end crosstalk (NEXT) and far-end crosstalk (FEXT) values are summarized in Table 4.1.

Table 4.1: Comparison of simulated and measured crosstalk results for Structure-D

Configuration	NEXT (Sim.) (mV)	FEXT (Sim.) (mV)	NEXT (Exp.) (mV)	FEXT (Exp.) (mV)
1W	101.30	18.82	96.70	23.42
3W	50.65	122.38	52.93	101.43

The results show good agreement between simulation and hardware measurements

for both configurations. For the 1W configuration, the measured NEXT voltage of 96.7 mV closely matches the simulated value of 101.3 mV, while the measured FEXT voltage of 23.42 mV is also comparable to the simulated value of 18.82 mV. Similarly, the measured and simulated results for the 3W configuration show good correlation, demonstrating that the simulation model accurately captures the dominant coupling mechanisms.

A reduction in NEXT is observed when the trace spacing is increased from 1W to 3W. The measured NEXT decreases from 96.7 mV to 52.93 mV, corresponding to a reduction of approximately 45%. This behaviour is expected, as increasing the spacing reduces the electric and magnetic field coupling between the adjacent traces.

In contrast, the FEXT level increases for the 3W configuration. While larger spacing generally reduces coupling, the 3W structure also contains a longer parallel routing section than the 1W structure. Since far-end crosstalk accumulates along the coupled length, the increased coupling length has a stronger influence on the FEXT response than the reduction in spacing. As a result, the measured FEXT increases from 23.42 mV for the 1W configuration to 101.43 mV for the 3W configuration. The same trend is observed in the simulation results.

Overall, the hardware measurements validate the simulation results and demonstrate that both trace spacing and parallel routing length play an important role in determining crosstalk behaviour. While increased spacing reduces near-end coupling, longer coupling lengths can significantly increase far-end crosstalk. The close agreement between simulation and measurement confirms the accuracy of the developed signal integrity model.

4.2 DC resistance test board

4.2.1 DCIR Results – Simulation

DCIR simulations are used to evaluate voltage drop and current distribution across different structures.

Structure A

The simulation results for Structure A are obtained under a constant current excitation of 2 A. The voltage distribution along the trace is shown in Figure 4.15, and the corresponding power dissipation is shown in Figure 4.16.

The voltage gradually decreases from approximately 0 mV at the source end to about -50.47 mV at the load end. A smooth and continuous voltage gradient is observed along the entire length of the conductor.

The power dissipation is relatively uniform along the trace, with values around

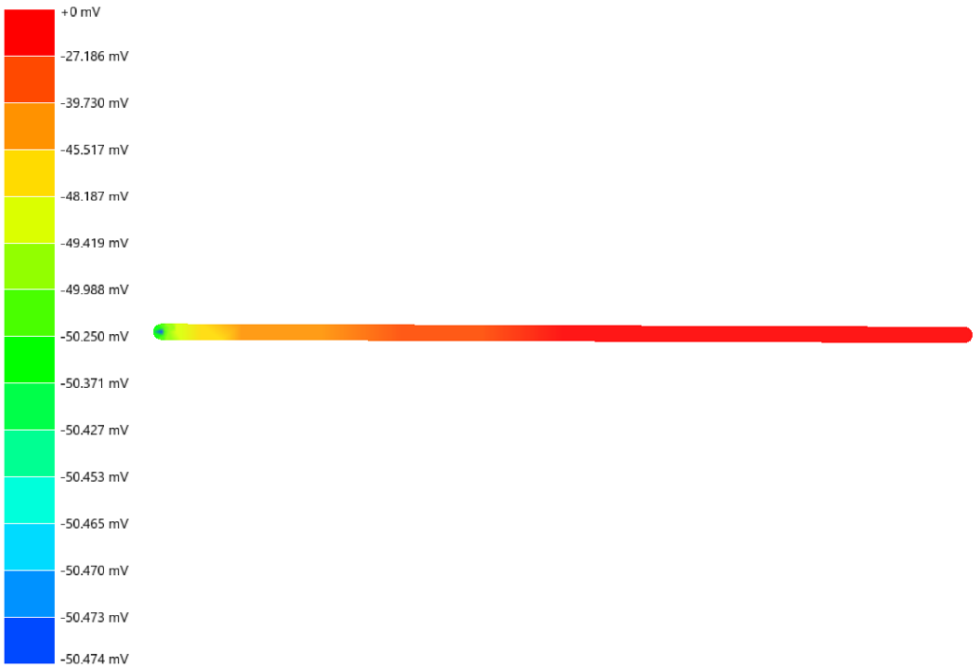

Figure 4.15: Voltage distribution across Structure A at 2 A input current.

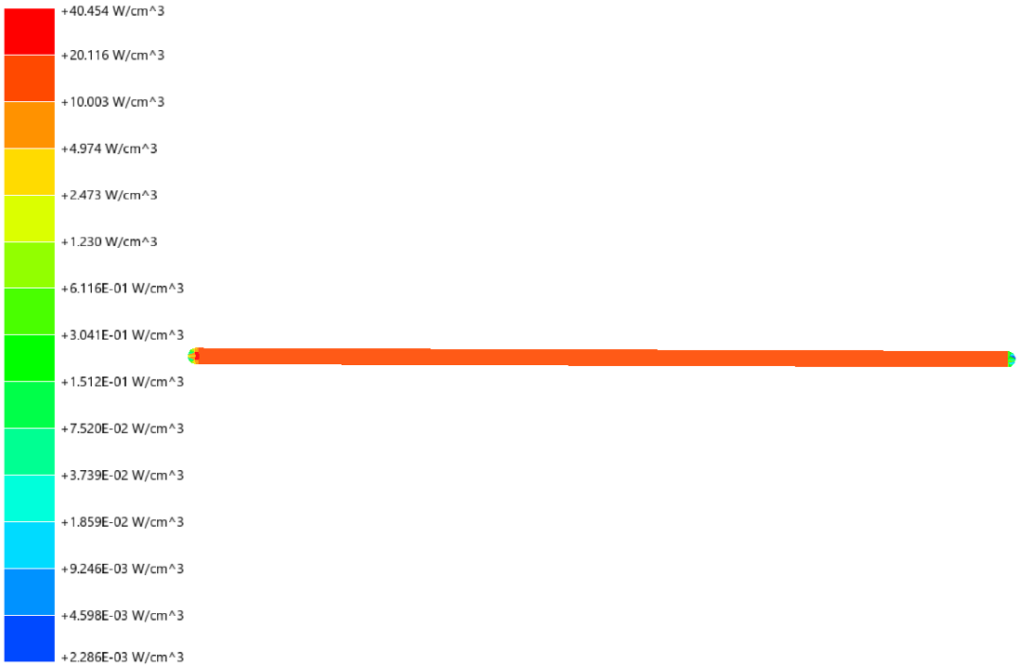

Figure 4.16: Power dissipation distribution across Structure A at 2 A input current.

0.3 W/cm^3 for most of the conductor. Slight variations are observed near the terminal regions.

The results indicate a consistent voltage drop and uniform power dissipation behaviour along the conductor under the applied current condition.

Structure B – Via Array

The DCIR simulation results for Structure B are obtained under an applied current of 2 A. The evaluated parameters include voltage drop across the trace, via current distribution, power dissipation near the via, and current density.

The simulation results are summarized in Table 4.2.

Table 4.2: Simulation results for Structure B at 2 A input current

Structure	Voltage (mV)	Via Current (A)	Power Density (W/cm^3)	Current Density (A/mm^2)
B1	49.671	2.0	27.63	34.45
B2	47.183	1.0	19.9	18.6
B3	45.642	0.5	10.6	13.14

The results show a gradual decrease in the voltage difference across the trace from B1 to B3. The via current is distributed differently across the configurations, with B1 carrying the full current through a single via, while B2 and B3 split the current across multiple vias.

A corresponding reduction in power dissipation near the via region is observed as the number of vias increases. Similarly, the current density near the via decreases significantly from B1 to B3.

This trend indicates that increasing the number of vias results in improved current distribution and reduced localized electrical stress, which is reflected in lower voltage drop and reduced power density.

Structure C – Trace Width

The DCIR simulation results for Structure C are obtained under a constant current excitation of 5 A. The structures consist of conductors with different trace widths, ranging from 0.25 mm to 10 mm.

The evaluated parameters include voltage difference across the trace, power density, current density, and temperature. The simulation results are summarized in Table 4.3.

The results show a significant reduction in voltage difference across the trace as the width increases from 0.25 mm to 10 mm. The highest voltage drop is observed in

Table 4.3: Electrical simulation results for Structure C at 5 A input current

Structure	Voltage difference across the trace (mV)	Power Density (W/cm^3)	Current density (A/mm^2)
C1 (0.25 mm)	584.54	5742	571
C2 (0.75 mm)	336.41	638	190
C3 (2 mm)	125.65	89.72	71.42
C4 (10 mm)	26.36	3.58	14.28

C1, while C4 exhibits the lowest value.

A strong variation in current density is observed across the structures. The narrowest trace (C1) shows the highest current density, while wider traces show a substantial decrease. The reduction in current density becomes more pronounced with larger increases in trace width.

Similarly, the power density decreases significantly as the trace width increases, with the highest values observed in C1 and the lowest in C4. It can also be observed that the reduction is not linear, with the most significant change occurring between the narrower and intermediate widths.

These results indicate that increasing the trace width improves current distribution along the conductor and reduces localized electrical loading, particularly in narrow geometries where current concentration is highest.

Additionally, thermal analysis was performed using the power map derived from the DCIR simulation. The maximum and minimum temperatures obtained from the DCIR power map are summarized in Table 4.4. This approach captures localized heating effects caused by non-uniform current distribution. The maximum and minimum temperatures obtained for each structure are:

Table 4.4: Maximum and minimum temperatures from DCIR power map for Structure C

Structure	Maximum Temperature (°C)	Minimum Temperature (°C)
C1 (0.25 mm)	181.896	95.876
C2 (0.75 mm)	92.361	60.959
C3 (2 mm)	49.170	40.019
C4 (10 mm)	27.284	25.420

These results reveal a large temperature gradient in the narrower traces, particularly for C1, where severe current crowding leads to pronounced localized heating. As the trace width increases, both the peak temperature and the temperature variation across the conductor decrease significantly. This indicates improved heat spreading and reduced formation of localized hot spots in wider traces.

Furthermore, the influence of conformal coating can be observed in Table 4.5. In all cases, the coated structures exhibit slightly lower temperatures compared to the uncoated ones. This behaviour can be attributed to the coating providing an

additional thermal conduction path and promoting more uniform heat distribution. Although the temperature reduction is relatively small, it becomes more relevant in narrower traces where localized heating and thermal stress are more critical.

Table 4.5: Thermal simulation results for Structure C

Structure	Temperature without conformal coating (°C)	Temperature with conformal coating (°C)
C1 (0.25 mm)	124.886	127.815
C2 (0.75 mm)	92.788	94.250
C3 (2 mm)	80.304	82.521
C4 (10 mm)	66.679	67.279

Overall, both the steady-state and power map based thermal results confirm that increasing trace width improves thermal performance by reducing peak temperatures, minimizing temperature gradients, and enhancing current distribution.

Structure D – Polygon Geometry

DCIR simulations were performed to evaluate the power density distribution, with particular focus on the corner regions where current crowding effects are expected to be most prominent. The results are illustrated in Fig. 4.19, where representative hotspots for both geometries are highlighted.

The results clearly show that D1 exhibits significantly higher power density at the sharp corners, with localized peaks reaching approximately 6.720 W/cm^3. In contrast, D2 demonstrates a noticeably lower power density in the corresponding regions, with peak values around 3.470 W/cm^3. Similar reductions are observed at other corner locations, where D1 shows values around 5.226 W/cm^3 compared to approximately 2.159 W/cm^3 in D2.

This reduction in power density for D2 can be attributed to the smoother transition provided by the rounded corners, which facilitates a more uniform current flow and reduces current crowding. In sharp geometries (D1), the abrupt change in current path leads to localized concentration of current, which in turn increases resistive losses and power dissipation.

Overall, the results indicate that even minor geometric modifications, such as corner rounding, can significantly reduce localized electrical stresses. This improvement is particularly important for enhancing reliability, as lower power density directly translates to reduced thermal hotspots and improved long-term performance of the conductor.

Structure E – Power and Signal Interaction

Structure E investigates the electromagnetic interaction between a high-current power trace (10 V, 30 A) and a nearby signal trace. Due to the large current flowing through the power trace, strong electromagnetic fields are generated, which

0.48

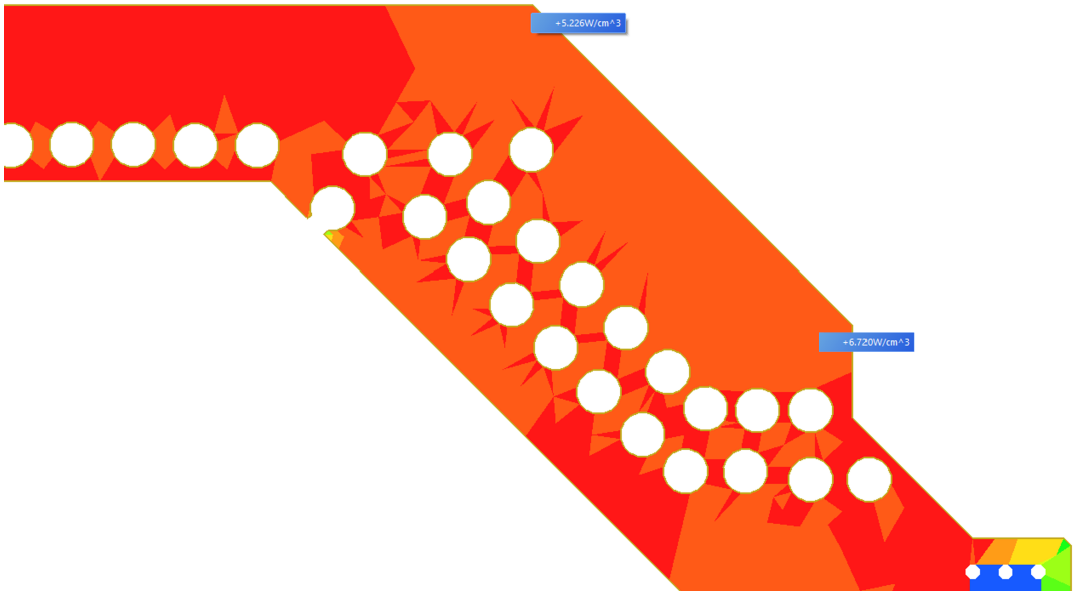

Figure 4.17: D1 - Sharp corners showing higher localized power density

0.48

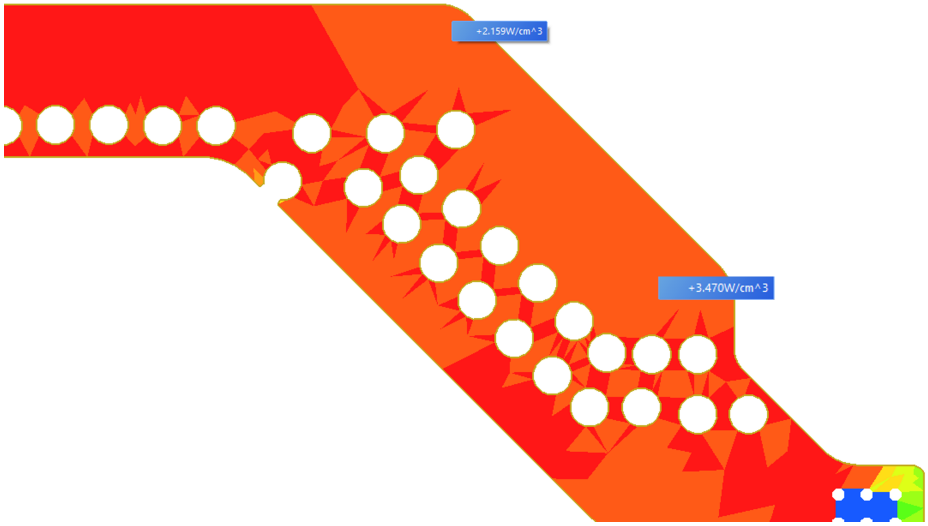

Figure 4.18: D2 - Rounded corners showing reduced power density

Figure 4.19: Comparison of power density distribution in Structure D for sharp and rounded polygon geometries under 5 A DC excitation.

can potentially couple into adjacent signal traces and impact signal integrity.

To analyse this behaviour, both near-field and far-field simulations were performed. The near-field electric field distribution is first examined to understand localized coupling effects, as shown in Fig. 4.20.

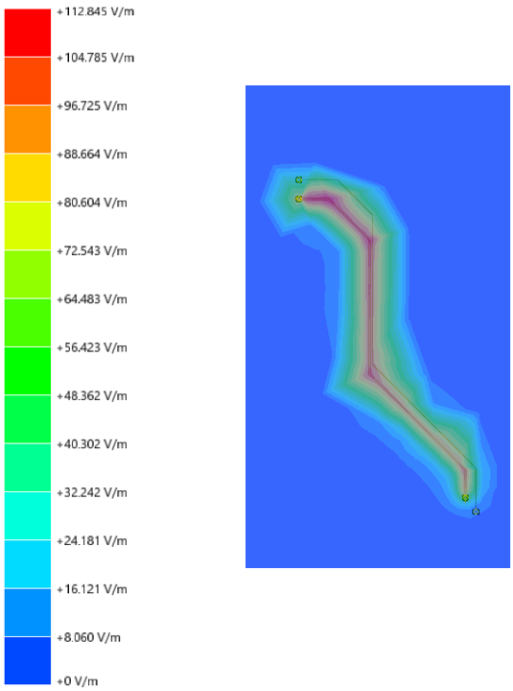

Figure 4.20: Near-field electric field distribution around the power and signal traces (V/m).

The near-field results indicate strong electric field concentration along the power trace, particularly at bends and geometrical discontinuities. Peak electric field values exceed 110 V/m in localized regions, while the field strength gradually decreases away from the trace. The signal trace is located within this field region, indicating a potential coupling path that may introduce noise or disturbances in signal transmission.

The far-field radiation characteristics are analysed next and are illustrated in Fig. 4.21, which shows the radiated electric field as a function of frequency.

The far-field plot represents the radiated electric field in decibels (dB), which is a logarithmic measure of the field magnitude relative to a reference value. The dB scale is defined as:

$$E_{\mathrm{dB}} = 20 \log_{10} \left(\frac{E}{E_{\mathrm{ref}}} \right) \tag{4.1}$$

where E is the electric field magnitude and E_{ref} is the reference field level. This

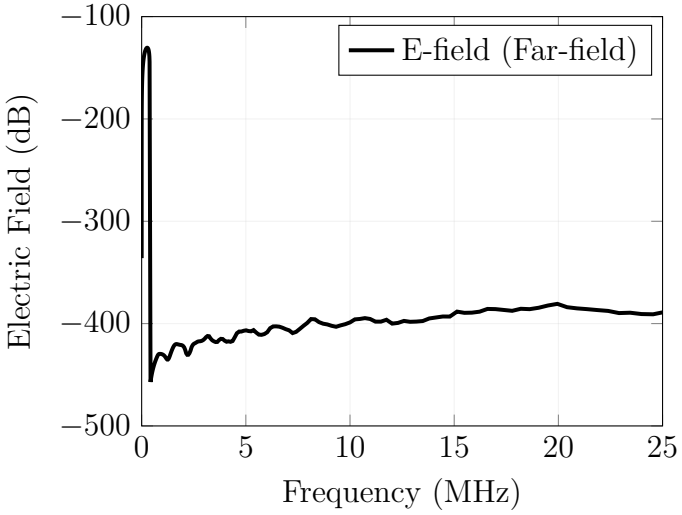

Figure 4.21: Far-field radiation showing electric field magnitude in dB as a function of frequency for Structure E.

logarithmic representation is useful for visualizing a wide dynamic range of electromagnetic emissions.

From Fig. 4.21, it can be observed that the radiated emissions remain extremely low across the analysed frequency range, with values predominantly below −350 dB. A slightly higher response is seen at very low frequencies, followed by a relatively stable emission profile with minor fluctuations up to 25 MHz.

Overall, the results indicate that while far-field radiation is minimal, the near-field effects are significant and dominate the electromagnetic interaction between the power and signal traces. These localized fields are more critical for signal integrity, highlighting the importance of layout optimization, spacing, and shielding techniques in high-current PCB designs.

4.3 EMI test board

4.3.1 EMI Results – Simulation

The EMI behaviour of the test board is analysed using a combination of resonance analysis and circuit-field co-simulation.

Resonant mode analysis identifies dominant resonance frequencies in the power plane, which are confirmed through Z-parameter sweep results [20, 17]. By exciting the signal trace at the resonance frequency, strong electromagnetic field concentration is observed in the power plane region.

Near-field analysis shows significant field intensification near the excitation point and along the edges of the power plane, indicating strong coupling.

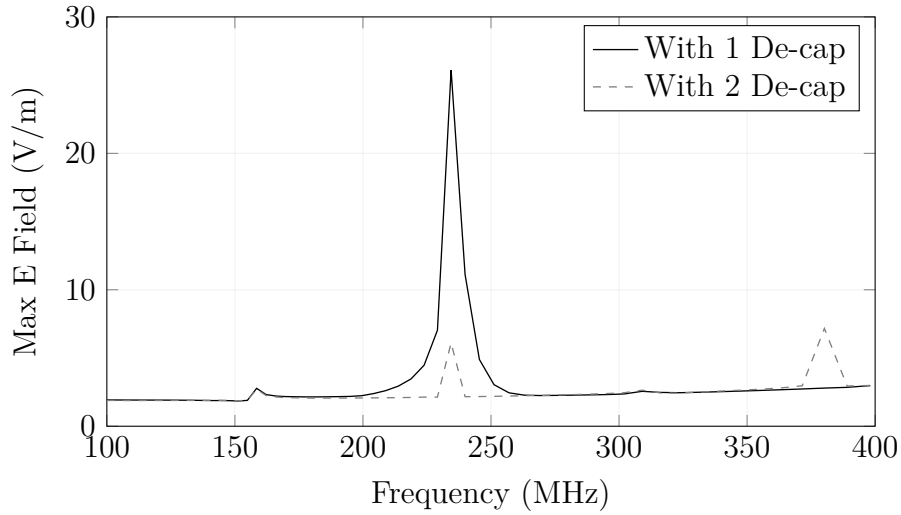

Figure 4.22: Near field comparison

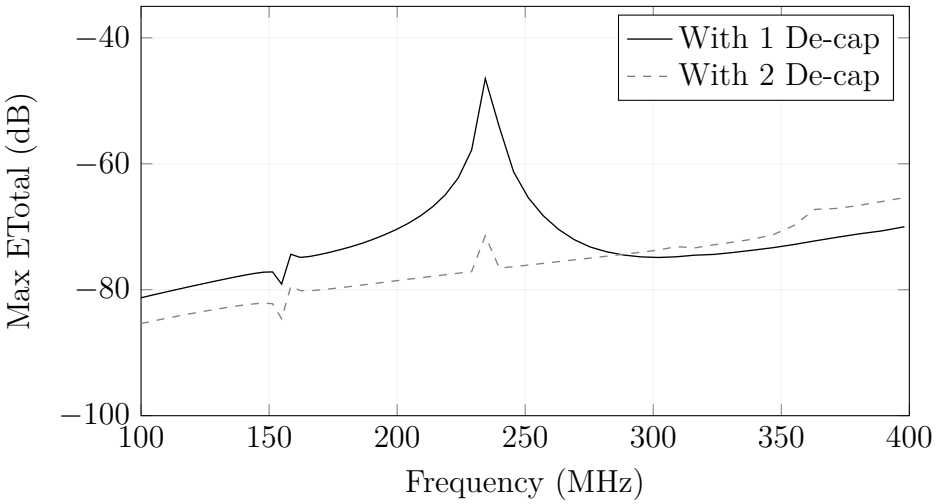

Figure 4.23: Far field comparison

4.3.2 EMI Results - Hardware Measurements

The introduction of decoupling capacitors reduces the field intensity by providing low-impedance paths and damping the resonance. The simulations show that the placement of the capacitor significantly influences the effectiveness of emission reduction.

The measured near-field emissions for the EMI test board are shown in Figure 4.24. The measurements compare the emissions obtained with a single decoupling capacitor and with two decoupling capacitors connected to the power plane.

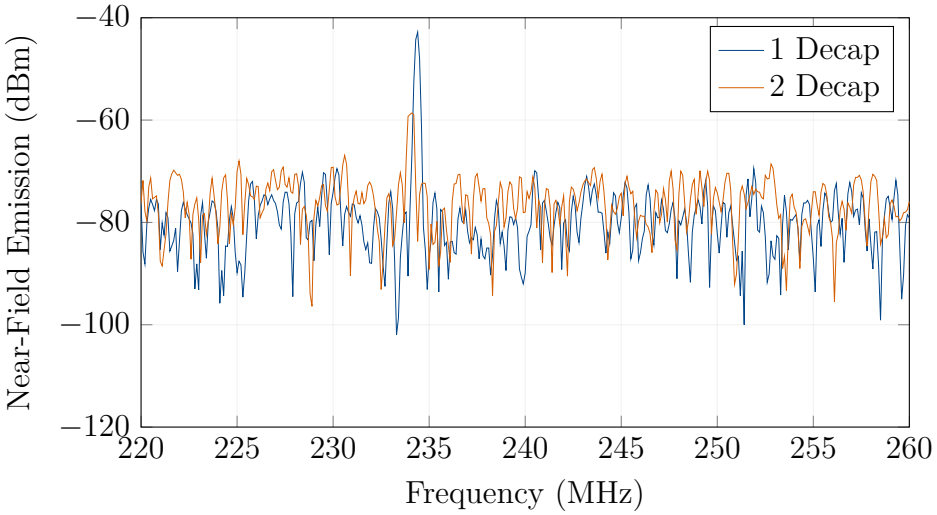

Figure 4.24: Nearfield

A distinct emission peak is observed around 233 MHz for both configurations. This frequency corresponds closely to the resonant frequency of the power plane identified in the simulations. The power-plane resonance is excited by the harmonic content of the 80 MHz signal propagating through the signal trace routed adjacent to the plane. In particular, the third harmonic of the 80 MHz excitation coincides with the resonance frequency of the power plane, leading to enhanced electromagnetic emissions.

For the single-capacitor configuration, the peak emission reaches approximately −43 dBm. When a second decoupling capacitor is added, the peak emission is reduced to approximately −60 dBm, corresponding to a reduction of about 17 dB. Away from the resonance frequency, both configurations exhibit similar background emission levels, indicating that the dominant difference between the two cases is associated with the suppression of the resonant mode.

These measurements are consistent with the simulation results presented in Figure 4.22, where the addition of a second decoupling capacitor significantly reduced the maximum electric field intensity around the plane resonance frequency. Although the simulation results are represented in terms of electric field strength and

the measurements are represented as received power levels, both approaches show the same overall trend.

Overall, the hardware measurements confirm that the observed emissions are primarily driven by excitation of the power-plane resonance. The addition of a second decoupling capacitor effectively damps the resonant mode, resulting in a significant reduction in near-field emissions and improved electromagnetic compatibility performance.

5

Conclusion

5.1 Results from present work

This thesis investigated how PCB layout influences signal integrity, electromagnetic interference (EMI), DC resistance (DCIR), and thermal behaviour in automotive inverter systems. Dedicated test boards were developed to isolate individual physical mechanisms and enable systematic evaluation of their impact on electrical and thermal performance. Hardware measurements were conducted to validate the simulation results and assess the accuracy of the modeling approach.

The signal integrity test board demonstrated how common PCB discontinuities influence high-frequency signal propagation. The baseline transmission line (Structure A) exhibited low insertion loss, reaching approximately 3 dB at 1 GHz, while the return loss remained below 10 dB over most of the measured frequency range, making it a suitable reference structure. Via stubs (Structure B) were found to degrade performance at higher frequencies. Back-drilling the unused via barrel in B2 reduced insertion loss and mitigated the resonant behaviour observed in B1, both in simulation and hardware measurements. Return-path disruption (Structure C) increased insertion loss above 1 GHz compared to the continuous reference plane configuration, while the addition of a 100 nF stitching capacitor restored part of the high-frequency transmission by providing a low-impedance return-current path. The crosstalk measurements (Structure D) showed that NEXT and FEXT respond differently to layout changes. Increasing the trace spacing from 1W to 3W reduced NEXT by approximately 45%, from 96.7 mV to 52.9 mV. However, FEXT increased from 23.4 mV to 101.4 mV because the 3W configuration also contained a longer parallel routing section. These results demonstrate that trace spacing and coupling length must be evaluated together when addressing crosstalk. Across all signal integrity structures, simulation and hardware measurements showed good agreement, validating the SIwave modeling approach used in this work.

The DC resistance test board highlighted the strong influence of PCB geometry on current distribution and resistive losses. Increasing the number of vias from one to four (Structure B) reduced the current density near the via transition from 34.45 A/mm^2 to 13.14 A/mm^2, while simultaneously reducing both voltage drop and local

power density. Trace width investigations (Structure C) showed an even larger impact. Increasing the conductor width from 0.25 mm to 10 mm reduced the voltage drop from 584.5 mV to 26.4 mV and lowered the current density from 571 A/mm^2 to 14.3 A/mm^2. The associated thermal effect was substantial, with the narrowest structure reaching a predicted peak temperature of approximately 182°C, while the widest conductor remained close to 27°C. Polygon geometry (Structure D) also affected performance. Replacing sharp corners with rounded transitions reduced the localized power density from 6.72 W/cm^3 to 3.47 W/cm^3 at one hotspot and from 5.23 W/cm^3 to 2.16 W/cm^3 at another, corresponding to a reduction of approximately 45–50%. These results demonstrate that even small geometric changes can significantly improve current distribution and reduce localized electrical stress. The thermal investigations performed using the DCIR test structures showed that conductor geometry is the dominant factor governing temperature rise. Conformal coating produced only a minor influence on thermal performance, with coated and uncoated structures differing by approximately 2–3°C across the investigated trace widths. Although the coating introduced an additional conduction path, its effect was considerably smaller than that of trace width and via density. Consequently, increasing copper cross-sectional area and improving current distribution were found to be substantially more effective thermal design measures than the application of conformal coating.

The EMI test board revealed the importance of power-plane resonance and decoupling strategy in controlling electromagnetic emissions. Resonance analysis identified a dominant resonant mode between approximately 233 MHz and 240 MHz. Hardware measurements confirmed this behaviour, showing that the third harmonic of the applied 80 MHz excitation signal strongly excited the resonant power plane. A clear near-field emission peak appeared near the predicted resonance frequency. The addition of a second decoupling capacitor reduced the measured peak emission from approximately −43 dBm to −60 dBm, corresponding to a reduction of about 17 dB. The measured results closely followed the simulation predictions, demonstrating that proper placement of decoupling capacitors is an effective method for suppressing resonance-driven emissions.

Overall, the results demonstrate that relatively small PCB layout modifications can produce substantial changes in electrical and thermal performance. A single back-drilled via, a 1 mm return-path discontinuity, an increase in trace width, the rounding of polygon corners, or the addition of a strategically placed decoupling capacitor each produced measurable improvements in performance. Since strong agreement was obtained between simulation and hardware measurements across the signal integrity, DCIR, thermal, and EMI investigations, the methodology developed in this work provides a reliable framework for evaluating PCB design alternatives before hardware implementation. The results show that simulation-driven PCB design can be used as a systematic engineering tool for optimizing inverter PCB layouts, reducing design iterations, and improving the electrical, electromagnetic, and thermal performance of future automotive inverter systems.

5.2 Ethics and Sustainability

While this thesis focuses on PCB design and simulation rather than direct human interaction, ethical engineering practices directly shape the validity of the work. The conclusions rely on a combination of simulation data and physical hardware measurements. To maintain research integrity, the models have been strictly validated against observed laboratory behavior, ensuring that limitations are transparently reported and avoiding unsupported performance claims. In automotive applications, this reliability is safety-critical; robust PCB layout minimizes electrical failures that could compromise vehicle performance or passenger safety.

From a sustainability perspective, this work directly targets the efficiency and reliability of electric vehicle (EV) power electronics. The design optimizations explored, specifically mitigating current crowding, reducing I^2R and switching losses, and suppressing electromagnetic interference (EMI), directly lower energy dissipation as waste heat, maximizing inverter efficiency. Additionally, shifting the development focus to a simulation-driven methodology cuts down the physical prototyping loop. By reducing the number of necessary board iterations, this approach directly saves substrate materials, components, and manufacturing energy, contributing to a more resource-efficient product development cycle in automotive engineering.

5.3 Future Work

While the simplified test structures used in this work provided valuable insight into the influence of individual PCB layout features, further validation at the inverter level would strengthen the conclusions. Future work could therefore focus on performing signal integrity and DCIR measurements directly on a complete inverter PCB. Such investigations would enable evaluation of the combined effects of multiple layout features acting simultaneously and provide additional validation of the simulation methodology under realistic operating conditions.

Another area of interest is the development of a fully coupled electro-thermal simulation workflow. In the present work, electrical and thermal analyses were performed sequentially, where electrical losses were used as input for thermal simulations. A more advanced approach would involve simultaneous solution of electrical and thermal behaviour, allowing temperature-dependent material properties and loss mechanisms to continuously interact during the simulation process. This would provide a more realistic representation of inverter operating conditions, particularly in regions with significant current crowding and localized heating.

The EMI study may also be extended from the simplified test board to a complete inverter PCB. Future investigations could include correlation between simulation results and measured near-field, conducted, and radiated emissions. Such work would provide a more comprehensive understanding of how power-plane resonances, switching signals, and PCB layout interact in practical inverter systems and could

support the development of improved EMI mitigation strategies.

Additional improvements can be achieved by incorporating more detailed thermal models. Future simulations could include temperature-dependent material properties, detailed component representations, package-level thermal effects, cooling paths, and mechanical assembly influences. These factors become increasingly important as power density increases and thermal margins become smaller in modern electrified powertrain systems.

Automation of the simulation workflow also represents a promising area for further development. By utilizing scripting and automated post-processing tools, a large number of PCB design variations could be evaluated with minimal manual intervention. This would enable systematic design-space exploration and allow engineers to identify optimal design solutions more efficiently than through traditional iterative approaches.

Finally, several PCB design parameters investigated only partially in this work could be studied in greater detail. Future research may include the influence of stack-up configuration, copper thickness, grounding strategies, shielding techniques, and advanced decoupling network optimization. These parameters are all closely linked to signal integrity, electromagnetic compatibility, thermal performance, and power distribution behavior, and their combined investigation would contribute to a more complete understanding of inverter PCB design.

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A

DCIR thermal simulation - Structure C

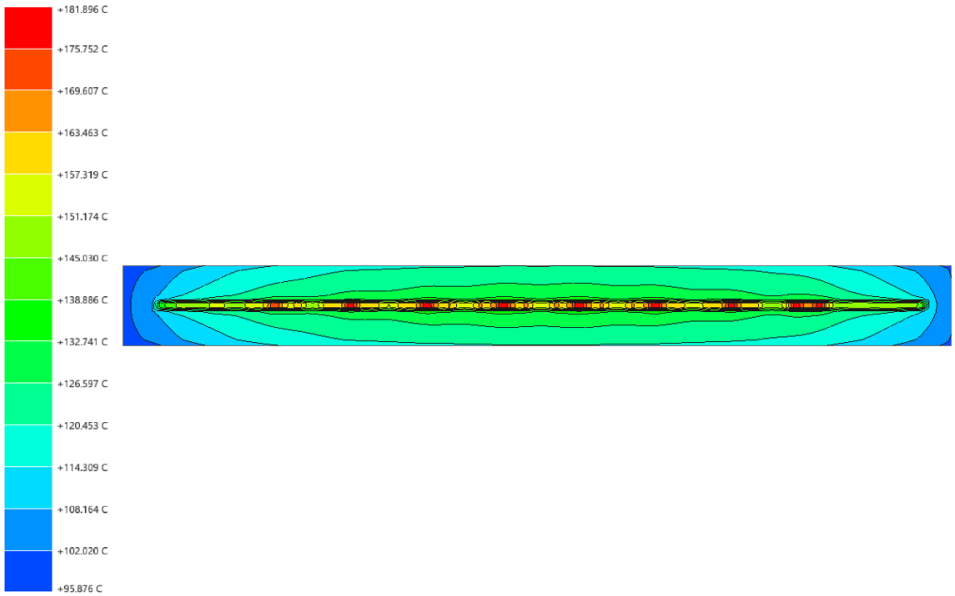


Figure A.1: Temperature distribution for C1 (0.25 mm trace width).

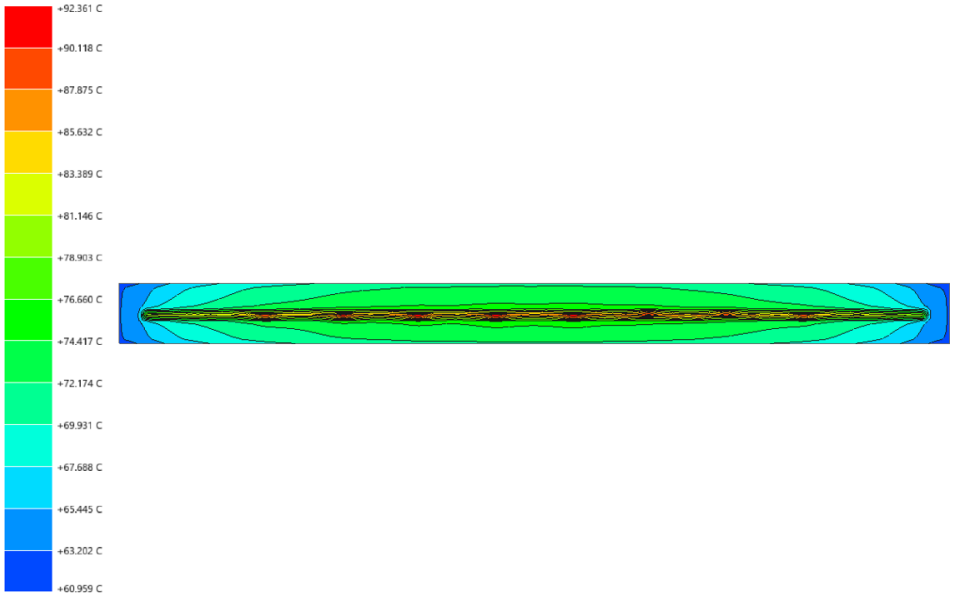


Figure A.2: Temperature distribution for C2 (0.75 mm trace width).

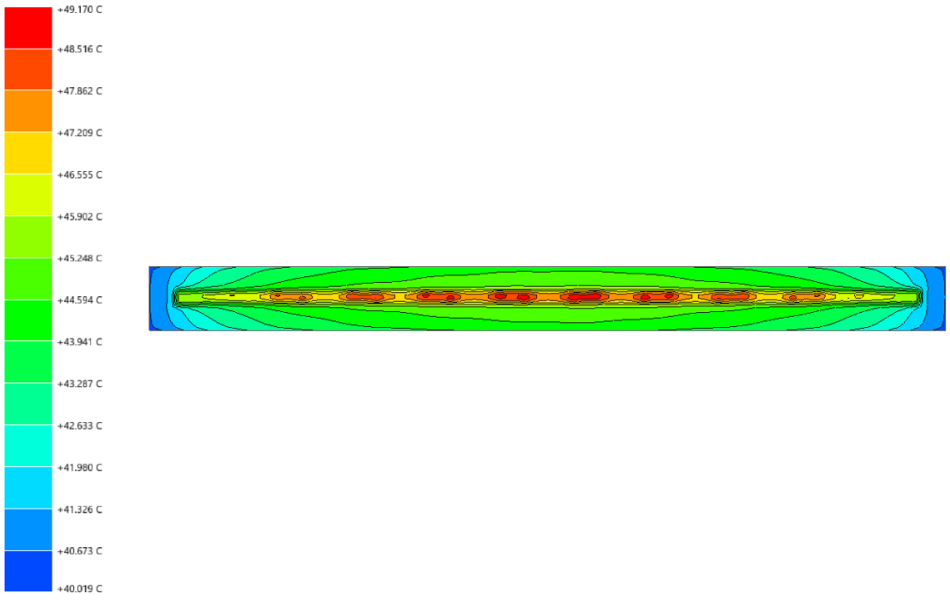


Figure A.3: Temperature distribution for C3 (2 mm trace width).

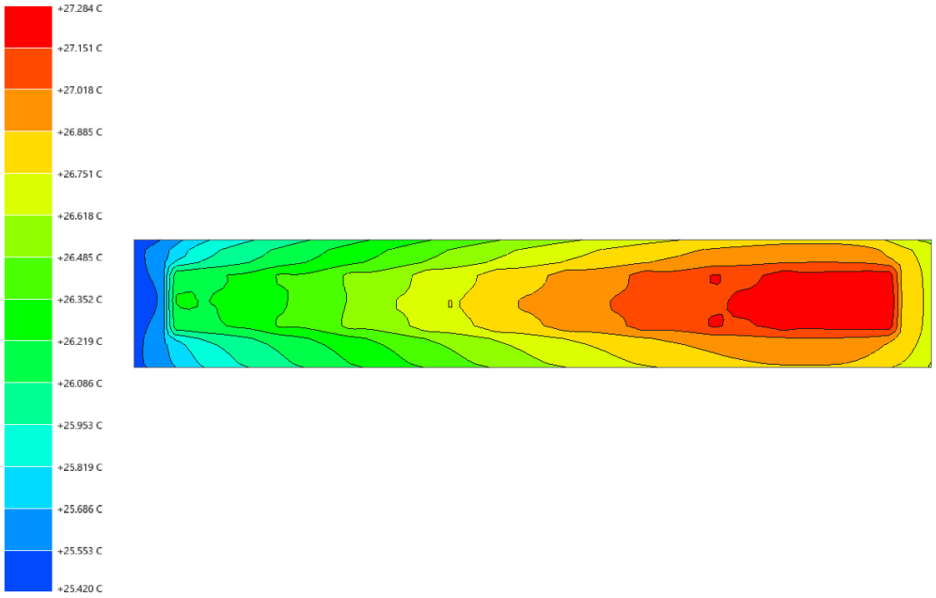
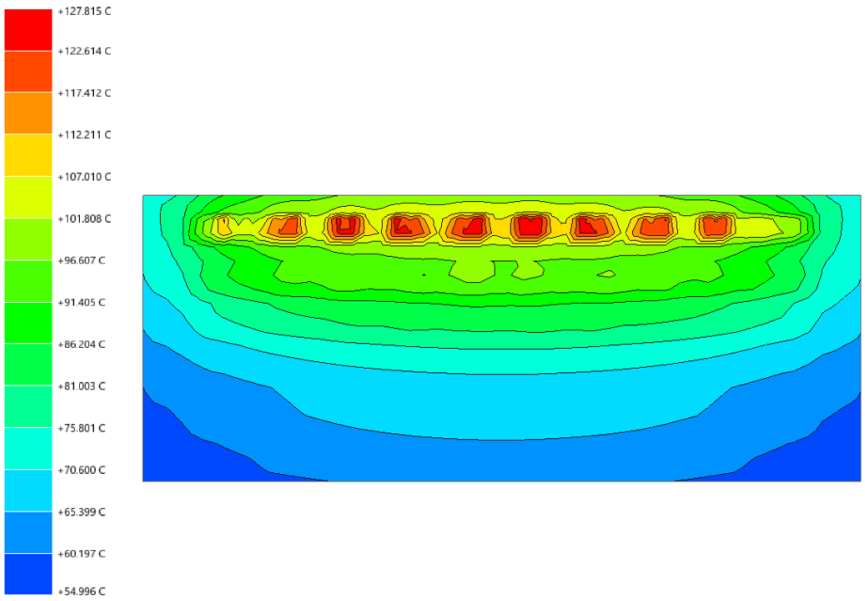
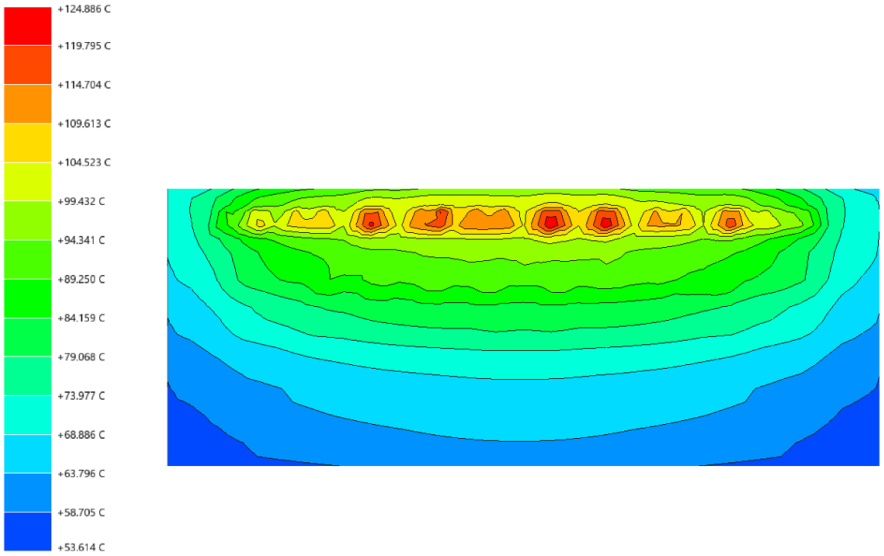


Figure A.4: Temperature distribution for C4 (10 mm trace width).



(a) Without conformal coating



(b) With conformal coating

Figure A.5: Temperature distribution for Structure C1 under 5A excitation with and without conformal coating.

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