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Hybrid GaN-SiC 3-Level Inverter Topologies for High-Performance Power Conversion

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Abstract

The electrification of road transport demands power electronics that are simultaneously efficient, compact, and reliable across a wide range of operating conditions. This thesis investigates the loss performance of four inverter topologies the three-level Active Neutral-Point-Clamped (3L-ANPC), the three-level Sparse Neutral-Point-Clamped (3L-SNPC), the three-level T-type Neutral-Point-Clamped (3L-TNPC), and the two-level inverter as a reference using wide-bandgap semiconductors from the SiC and GaN(GIT) families, as well as hybrid SiC-GaN(GIT) device combinations. All configurations are evaluated through parametric PLECS simulations across a switching frequency of 10–100 kHz, output peak phase current 40–50 A, and an ambient temperature of 45–85°C, representative of an 800 V EV drivetrain.

The hybrid SiC-GaN(GIT) SNPC achieves the lowest total losses of any configuration tested 175.2 W at the reference operating point was achieved for 13.5kW transmitted power, approximately 20% lower than the ANPC configuration, approximately 20% lower than the hybrid SiC-GaN(GIT) TNPC in same device configuration.

In the 3L-ANPC, the SiC-GaN(GIT) hybrid configuration achieves the lowest total losses among all five device configurations across all three parametric sweeps frequency, current, and temperature. It combines GaN's low switching losses with SiC's stable conduction performance, delivering a consistently flat and low loss profile that no single-technology configuration can match.

For the T-type inverter, the hybrid SiC–GaN(GIT) reduces switching losses compared with the full-SiC configuration, particularly at higher switching frequencies. However, due to the device characteristics and current commutation behavior of the selected configuration, the reduction in switching losses is insufficient to compensate for the increased conduction losses, which become dominant under the investigated operating conditions.

The results demonstrate that inverter topology, device property, and device placement configuration must be optimised jointly the right device in the wrong position will prevent the topology from delivering its best outcome.

Keywords: lorem, ipsum, dolor, sit, amet, consectetur, adipisicing, elit, sed, do.

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From Nazma: I would like to thank my husband Shiraj Shekh Gutti for his continuous support and standing by my side all the time.

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List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

ANPC	Active Neutral-Point-Clamped
EV	Electric Vehicle
GaN	Gallium Nitride
GIT	Gate Injection Transistor
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NPC	Neutral-Point-Clamped
PCB	Printed Circuit Board
PLECS	Piecewise Linear Electrical Circuit Simulation
PWM	Pulse-Width Modulation
Si	Silicon
SiC	Silicon Carbide
SM	Switching Module
SNPC	Sparse Neutral-Point-Clamped
SVM	Space-Vector Modulation
VSI	Voltage Source Inverter
WBG	Wide-Bandgap
2L	Two-Level
3L	Three-Level

Nomenclature

Roman Symbols

Symbol	Description	Unit
C	DC-link capacitance	F
E_{off}	Turn-off switching energy	J
E_{on}	Turn-on switching energy	J
f_{sw}	Switching frequency	Hz
f_{out}	Output fundamental frequency	Hz
I_{pk}	Peak output current	A
I_{rms}	RMS output current	A
M	Modulation index	—
P_{cond}	Conduction loss	W
P_{sw}	Switching loss	W
P_{tot}	Total power loss	W
$R_{\text{DS(on)}}$	On-state drain-source resistance	Ω
T_{amb}	Ambient temperature	$^{\circ}\text{C}$
T_{j}	Junction temperature	$^{\circ}\text{C}$
V_{dc}	DC-link voltage	V
V_{AO}	Phase-to-neutral output voltage	V
$V_{\text{CE(sat)}}$	Collector-emitter saturation voltage	V
V_{F}	Forward voltage drop	V

Greek Symbols

Symbol	Description	Unit
φ	Power factor angle	rad
η	Efficiency	—
ω	Angular frequency	rad/s

Subscripts

Subscript	Description
cond	Conduction
dc	Direct current
off	Turn-off
on	Turn-on
pk	Peak
rms	Root mean square
sw	Switching
tot	Total

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1

Introduction

The electrification of road transport has placed new and demanding requirements on power electronic systems. The traction inverter is a key component responsible for converting DC energy from the battery into AC power required by the electric motor. Its performance directly affects efficiency, thermal behaviour, and overall system reliability.

Conventional two-level inverters are widely used due to their simplicity and technological maturity. However, they introduce large voltage steps across switching devices, elevated harmonic distortion in the output waveform, and significant switching losses particularly at the high power levels characteristic of modern electric drivetrains. These limitations make them less suitable for next-generation high-performance traction applications.

Multilevel inverter topologies offer a compelling alternative. By producing stepped output waveforms, they reduce voltage stress on individual devices, lower harmonic content, and enable operation at higher effective switching frequencies without a proportional increase in losses. Among the available options, three-level topologies have attracted considerable research interest, largely because they strike a practical balance between circuit complexity and achievable performance [1, 2].

Wide-bandgap semiconductor technologies have, in parallel, begun to reshape what is possible in power electronics. Silicon Carbide (SiC) devices combine high breakdown voltage, strong thermal conductivity, and robust high-current conduction performance, making them well suited for positions in a circuit where continuous current flow dominates the loss budget. Gallium Nitride (GaN) devices take a different character: their exceptionally fast switching transitions and near zero reverse recovery energy mean that switching losses remain low even as frequency climbs well beyond what conventional silicon can sustain [3, 4].

Neither technology is without limitation. SiC devices, despite their conduction strengths, accumulate meaningful switching losses as frequency rises, which constrains the power density achievable in practice. GaN devices, for their part, carry a higher on-state resistance at the current ratings demanded by traction inverters, making them a poor fit for positions where current is large and switching is infrequent [5]. These complementary profiles one excelling where the other falls short have naturally prompted the question of whether the two technologies can be combined within a single converter to capture the advantages of both.

This idea has gained traction in the recent literature. Hybrid GaN-SiC configurations in multilevel inverters have been shown to reduce total device losses relative to single-technology designs, by matching each device type to the circuit position that suits its characteristics [6, 7]. In three-level Active Neutral-Point-Clamped (ANPC) topologies, the modulation strategy creates a clear structural distinction between devices that switch at the carrier frequency and those that operate at the fundamental a distinction that makes selective device placement particularly effective. Research has demonstrated that routing high-frequency switching events through GaN while retaining SiC in the main conduction path can produce a notably flatter loss profile across frequency, extending the practical operating range of the inverter [8].

Despite these advances, unified comparative studies covering multiple three-level topologies

under consistent, automotive-relevant conditions remain scarce. The Sparse Neutral-Point-Clamped (SNPC) converter [9] a topology that reduces the active device count through a cascaded two-stage architecture and offers an inherent loss advantage as a result has received comparatively little attention in the context of hybrid wide-bandgap device configurations. Alongside the ANPC and SNPC, the T-type topology represents a further alternative whose simpler structure and distinct loss characteristics make it a relevant point of comparison. Whether the structural efficiency of these topologies and the device-level advantages of GaN-SiC hybridisation can be combined effectively, and how the configurations compare under consistent automotive-relevant conditions, is a question this thesis sets out to answer.

1.1 Objectives

The central aim of this work is to provide a quantitative, parametric comparison of hybrid GaN(GIT)-SiC device configurations across four inverter topologies the 3L-ANPC, the 3L-SNPC, the three-level T-type, and the two-level inverter as a reference case under operating conditions representative of an 800 V electric vehicle drivetrain. Specifically, the study investigates how total power losses vary with switching frequency, output current, and ambient temperature, and identifies which combination of topology and device technology that delivers the best loss performance across these conditions.

1.2 Limitation

All loss evaluations are carried out in PLECS using device loss models derived from manufacturer datasheets. While this approach captures the dominant loss mechanisms with reasonable accuracy, it does not account for parasitic inductances, PCB layout effects, or gate driver non-idealities that influence switching transients in a physical prototype. The trends reported here are expected to hold in hardware, but the absolute loss figures may shift somewhat in practice.

Within the GaN family, this study is restricted to the Gate Injection Transistor (GIT) variant only. Other GaN device types including the Self-commutated GaN Transistor (SGT), depletion-mode GaN, and bidirectional GaN are not investigated. The SGT and depletion-mode GaN devices exhibit an on-state resistance that remains largely constant with increasing current, unlike the GIT whose $R_{DS(on)}$ rises with current due to its injection mechanism. This characteristic could result in lower conduction losses at high current levels, potentially changing the conclusions drawn here regarding GaN performance in conduction-dominant positions. Bidirectional GaN devices present a further unexplored opportunity: a single bidirectional switch can replace two anti-series unidirectional devices in certain converter positions, reducing component count, lowering on-state resistance, and offering higher power density at lower cost. These alternatives represent promising directions for future work as their commercial availability continues to grow.

2

Theory

2.1 Three-Phase Two-Level VSI Topology

The basic structure of a three-phase VSI consists of three inverter legs [10] with parallel capacitor. The circuit diagram is shown in Fig. 2.1, each leg contains two semiconductor switches arranged in a complementary manner. The midpoint of each leg forms one phase output, resulting in the three output terminals generally denoted as phases a , b , and c .

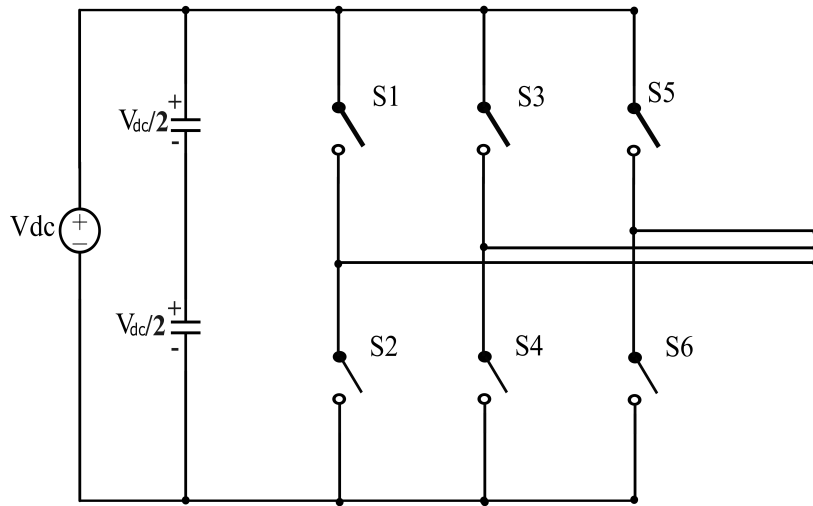


Figure 2.1: Circuit diagram of a three-phase two-level voltage source inverter (VSI).

The operation of the inverter is based on controlled switching of the semiconductor devices. At any instant, the upper and lower switches of the same leg must never conduct simultaneously, since this would create a direct short circuit across the DC source. Therefore, a small dead-time interval is normally introduced between switching transitions to ensure safe operation. By turning the switches ON and OFF in a specific sequence, the inverter synthesizes an alternating three-phase voltage waveform from the available DC input.

For an ideal two-level three-phase inverter, each phase output can be connected either to the positive DC bus or to the negative DC bus. Consequently, the generated phase voltage alternates between two discrete voltage levels. The line-to-line voltages are formed from the difference between two phase voltages and exhibit a quasi-square waveform before filtering. In practical applications, pulse width modulation (PWM) techniques are employed to improve waveform quality and reduce harmonic distortion.

Among the different modulation strategies, Sinusoidal Pulse Width Modulation (SPWM) is one of the most widely used methods because of its simplicity and reliable performance [10]. In SPWM, a sinusoidal reference signal is continuously compared with a high-frequency triangular carrier waveform. The comparison determines the switching instants of the semiconductor devices. When the sinusoidal reference is greater than the carrier signal, the upper switch of the corresponding phase leg is turned ON, otherwise the lower switch conducts. This process generates a PWM voltage waveform whose average value follows the desired sinusoidal reference. The modulation index is generally expressed as

$$M = \frac{\hat{V}_{\text{ref}}}{\hat{V}_{\text{carrier}}} \quad (2.1)$$

where $\hat{V}_{\text{ref}}$ represents the amplitude of the sinusoidal reference signal and $\hat{V}_{\text{carrier}}$ represents the amplitude of the carrier waveform. By adjusting the modulation index, the amplitude of the AC output voltage can be controlled without changing the DC-link voltage.

For a balanced three-phase system, the phase voltages can be represented as

$$v_a = \hat{V} \sin(\omega t) \quad (2.2)$$

$$v_b = \hat{V} \sin\left(\omega t - \frac{2\pi}{3}\right) \quad (2.3)$$

$$v_c = \hat{V} \sin\left(\omega t + \frac{2\pi}{3}\right) \quad (2.4)$$

where $\hat{V}$ is the peak phase voltage and ω is the angular frequency of the output waveform. These three voltages are phase shifted by 120° , producing a balanced rotating magnetic field when connected to a three-phase motor.

One of the main advantages of a VSI is its ability to decouple the control of output voltage magnitude and output frequency, allowing each to be adjusted independently through the modulation index and switching frequency respectively. Despite its advantages, the inverter also introduces switching harmonics due to the rapid ON/OFF transitions of semiconductor devices. These harmonics can lead to additional losses, electromagnetic interference, and stress on connected equipment. To reduce these effects, filters and advanced modulation methods are commonly used in practical converter systems.

2.2 Three-Phase Three-Level VSI Topology

The three-level voltage source inverter was developed to overcome the fundamental limitations of the two-level topology at high DC-link voltages. By introducing an additional output voltage level-zero, in addition to $+V_{\text{dc}}/2$ and $-V_{\text{dc}}/2$ the three-level inverter reduces the voltage stress on some switch to $V_{\text{dc}}/2$, allows the use of lower-voltage devices, and produces an output waveform with significantly lower harmonic distortion [2].

The reduced switch voltage stress is the advantage. For ANPC topology, all the devices are rated half of the input voltage as the blocking voltage; for SNPC and TNPC topology, only the devices connected to the neutral point are rated half of the input voltage as the blocking voltage. Lower voltage ratings generally mean lower on-state resistance, faster switching, and lower switching energy loss. This is precisely why three-level topologies are attractive for wide-bandgap device applications [1].

Three distinct three-level topologies are investigated in this project:

- **Active Neutral-Point Clamped (ANPC)** inverter-uses six active switches per phase leg with active clamping to the neutral point, providing flexible loss distribution through modulation strategy selection [11].
- **Sparse Neutral-Point Clamped (SNPC)** inverter-uses a cascaded two-stage architecture with only ten active semiconductors per three-phase system, naturally separating switching and conduction functions between stages [9].
- **T-type Neutral Point Clamped (TNPC)** inverter-connects the output terminal to the neutral point through a bidirectional switch, forming a T-shaped phase leg where outer switches block the full DC-link voltage [8].

2.2.1 Operating Principle of the Hybrid SiC-GaN ANPC Inverter

The Active Neutral Point Clamped (ANPC) inverter is a three-level converter topology well suited for high-performance electric drive applications. Unlike a conventional two-level inverter, where each switching device must block the full DC-link voltage V_{dc} , the three-level structure limits the voltage across each device to $V_{dc}/2$. This reduction in voltage stress allows the use of lower-rated semiconductor devices, which typically exhibit lower on-state resistance and faster switching characteristics. In addition, the three-level output waveform produces smaller voltage steps, resulting in lower harmonic distortion and reduced dv/dt stress on the connected motor windings compared to a two-level inverter.

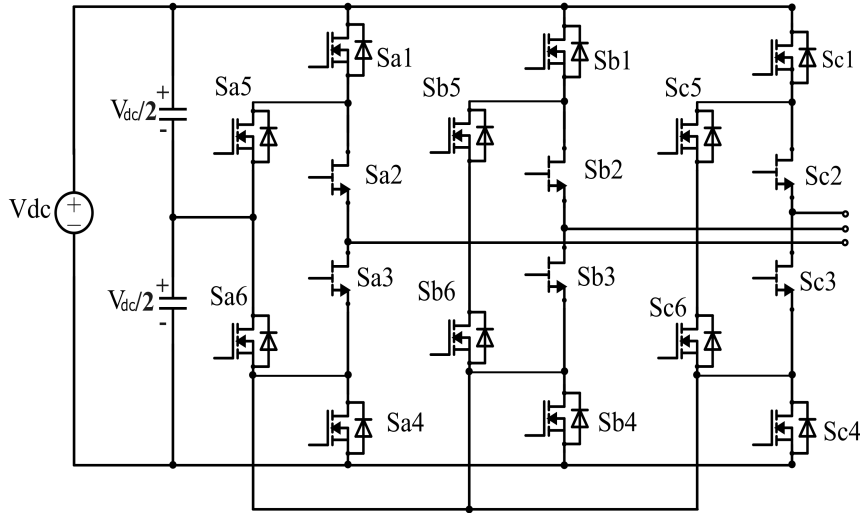


Figure 2.2: Circuit diagram of a Hybrid SiC-GaN ANPC Inverter

The Active Neutral-Point Clamped (ANPC) inverter solves one of the most persistent problems in multilevel converter design: unequal loss distribution among the switches. In a standard NPC inverter, the inner switches carry current during every commutation state while the outer switches only conduct part of the time—a structural imbalance that forces the whole converter to be derated to protect the most stressed device. The ANPC addresses this by replacing the passive clamping diodes with active switches, giving the modulation strategy the freedom to redirect zero-state current and spread the thermal burden more fairly [11].

In this work, a hybrid device configuration is used rather than a single-technology design. The reasoning is straightforward: SiC and GaN devices have complementary strengths, and the ANPC topology creates a structural asymmetry in switching behaviour that allows each technology to be placed where it performs best.

As shown in Fig. 2.2, a single phase-leg of the ANPC inverter consists of six active switches. The outer switches S_1 , S_4 , S_5 , and S_6 operate at the fundamental output frequency and carry current for the majority of each cycle, making conduction loss the dominant concern in these positions. The inner switches S_2 and S_3 , by contrast, commute at the full carrier frequency and therefore generate the majority of the switching losses. This clear separation between high-conduction and high-frequency switching positions creates a natural opportunity for selective device placement: SiC MOSFETs, with their lower on-state resistance, are assigned to the outer positions where conduction dominates, while GaN Gate Injection Transistors (GITs), with their near-zero switching energy and zero reverse recovery charge, are placed in the inner positions where fast commutation is required [3, 6]. This functional separation maps well with the properties of the two device technologies. SiC MOSFETs are placed in the outer switch positions, where their lower on-state resistance reduces conduction losses in the high-current, low-frequency path. GaN Gate Injection Transistors (GITs) are placed in the inner positions, where their near-zero switching energy and zero reverse recovery charge [3] make fast commutation efficient.

2.2.1.1 Output Voltage States

Like any three-level inverter, the hybrid ANPC produces three distinct output voltage levels at the phase terminal: $+V_{dc}/2$, 0, and $-V_{dc}/2$, where V_{dc} is the DC-link voltage. The positive level is denoted state P, the negative level state N. The zero level is more interesting: it can be generated by two redundant states, O^+ and O^- , which shows the zero-state current through different paths in the phase leg. This gives the ANPC its loss redistribution capability by choosing between O^+ and O^- , the modulation strategy controls which devices carry the zero-state current and therefore which devices heat up. The switching states of one ANPC phase-leg are summarised in Table 2.1.

Table 2.1: Switching states of one phase-leg in the hybrid ANPC inverter

State	v_{AO}	S_1	S_2	S_3	S_4	S_5	S_6
P	$+V_{dc}/2$	1	1	0	0	0	1
O^+	0	1	0	1	0	0	1
O^-	0	0	1	0	1	1	0
N	$-V_{dc}/2$	0	0	1	1	1	0

2.2.1.2 PWM-2 Modulation and Current Paths

Several sinusoidal PWM strategies exist for the ANPC, differing in which switches carry the high-frequency switching burden [7]. PWM-2 is selected in this study because it concentrates all switching events in the inner switch positions S_2 and S_3 , which aligns directly with the hybrid GaN-SiC placement strategy. GaN devices occupy precisely these positions to exploit their low switching energy. Additionally, it has been demonstrated that [7] PWM-2 achieves a natural doubling of the apparent switching frequency in the output voltage waveform, reducing harmonic distortion without increasing the actual device switching frequency. Fig. 2.3 illustrates this modulation scheme: during the positive half-cycle the output toggles between state P and state O^+ at the carrier rate, and during the negative half-cycle it toggles

between state N and state O^- . The outer switches S_1 and S_6 simply follow the sign of the reference voltage, changing state only once per fundamental period.

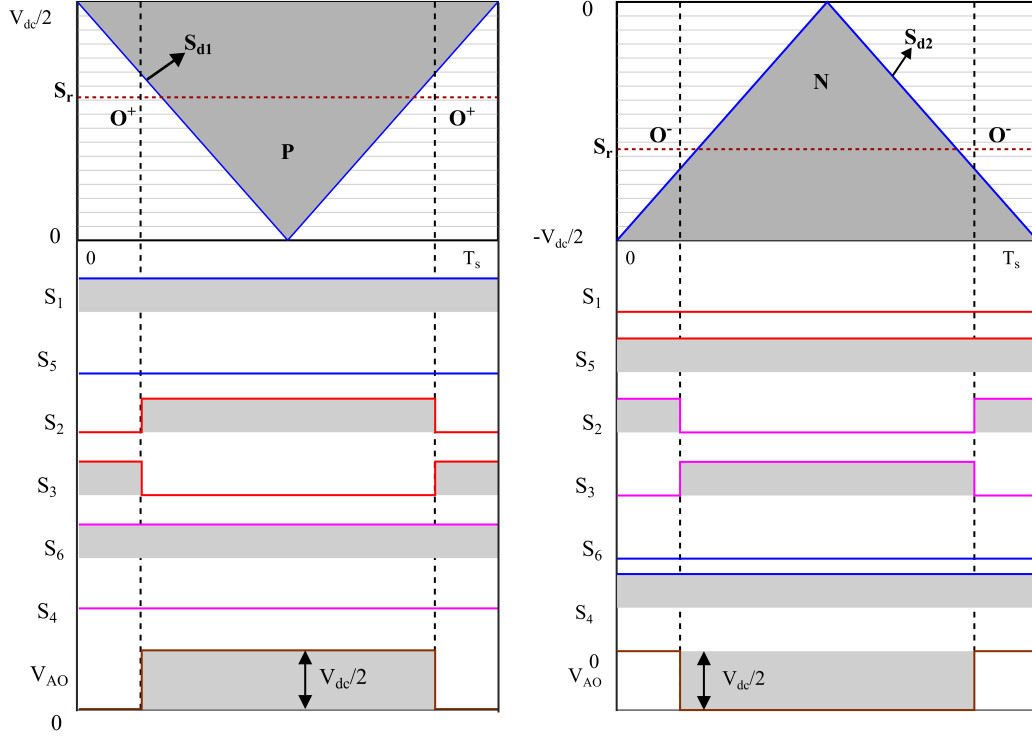


Figure 2.3: PWM-2 modulation scheme for the 3L-ANPC inverter. Cell 2 switches at the carrier frequency; outer switches operate at the fundamental frequency only [7].

The consequence for loss distribution is direct: under PWM-2, all switching losses are generated in S_2 and S_3 . The outer SiC switches operate at the fundamental frequency and commute under near zero-voltage or zero-current conditions, resulting in negligible switching losses compared to the inner switches. Fig. 2.4 shows the six current conduction paths corresponding to each switching state. In state P, current flows through the upper SiC devices S_1 and S_6 together with the GaN device S_2 . As the converter transitions to state O^+ , S_2 turns off and current commutates to the zero-state path the commutation event that generates switching loss falls entirely on the GaN inner switch. During state O^+ , current freewheels through S_1 , S_3 , and S_6 . In state O^- , current flows through the switch S_2 , S_4 , and S_5 . As the converter transitions to state N, switch S_2 turns off and S_3 turns on, so current flows through the switch S_3 , S_4 , and S_6 .

The hybrid ANPC therefore achieves something that neither pure SiC nor pure GaN can match on its own: conduction losses are dominated by the SiC devices, while switching losses are minimised by GaN. The result is a converter that stays efficient across a wider range of switching frequencies than a single-technology design [6, 3].

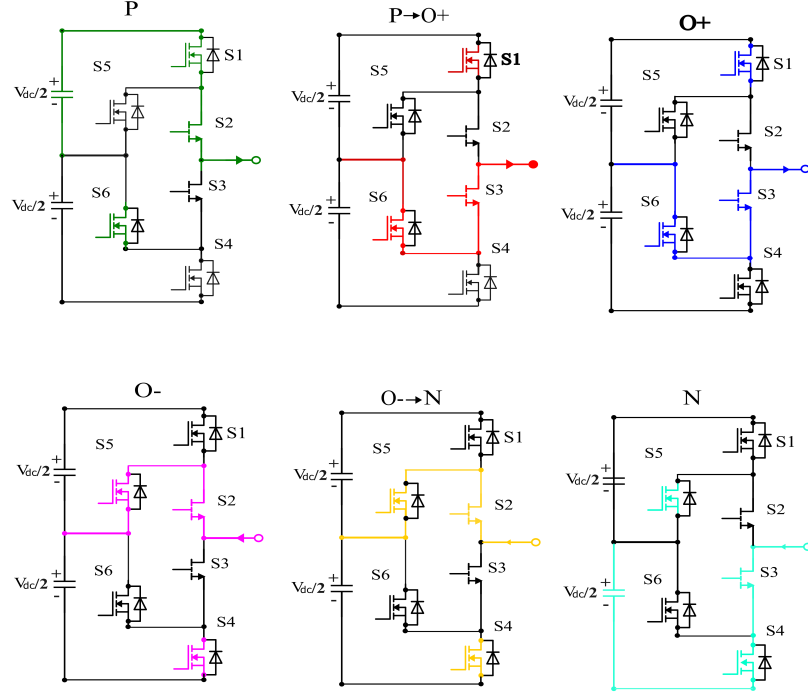


Figure 2.4: Current conduction paths for all switching states of the hybrid SiC-GaN ANPC inverter under PWM-2 modulation.

2.2.2 Three-Level Sparse Neutral-Point Clamped (3L-SNPC) Inverter

The 3L-SNPC has a fundamentally different structure from the ANPC [9]. Circuit diagram of Hybrid SiC–GaN SNPC Inverter is shown in Fig. 2.5. Rather than a single multilevel phase leg, it cascades two stages: a three-level switching matrix (SM) followed by a conventional three-phase two-level inverter. The entire three-phase system uses only **10 active semiconductors**, compared with 12 in the ANPC or T-type [12].

The two stages operate under different constraints:

- **3L Switching Matrix (SM):** four devices per three-phase system, each blocking only $V_{dc}/2$. This stage generates the three voltage levels and carries the high-frequency switching events.
- **2L Inverter stage:** six devices in three half-bridge legs, each blocking the full DC-link voltage V_{dc} . This stage carries the full output current and therefore dominates the conduction losses.

The clean separation between these two roles—fast switching at low voltage in the SM, high current at full voltage in the 2L inverter—makes the SNPC an almost ideal candidate for hybrid device placement: GaN in the SM, SiC in the 2L inverter stage. That is exactly the configuration investigated in this study.

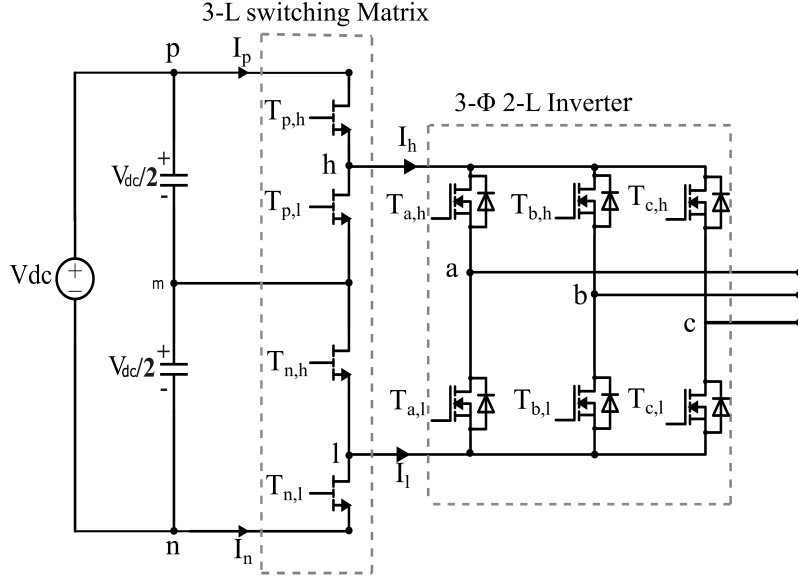


Figure 2.5: Circuit diagram of Hybrid SiC–GaN SNPC Inverter

2.2.2.1 Space-Vector Modulation for the 3L-SNPC

The SNPC is modulated using a space-vector approach [12]. The reference voltage vector $\vec{V}^*$ is synthesised by time-averaging combinations of adjacent space vectors within each switching period T_s . The possible SM states map onto zero, small, and large vectors that form the standard hexagonal space-vector diagram. By symmetry, the analysis reduces to one 60° sector, subdivided into two areas. [12] identified eleven switching sequences for the SNPC; this study follows their recommendation and uses the symmetric Sequence U, which provides a good balance between semiconductor stress and output current quality.

2.2.3 Three-Level Three-Phase T-type Neutral Point Clamped (3L-TNPC) Inverter

The three-phase 3L T-type inverter is shown in Fig. 2.6. This topology is an extension of the three-phase 2L inverter with another two switches connecting in series, becoming an active bidirectional switch to the DC-link midpoint in each phase [13].

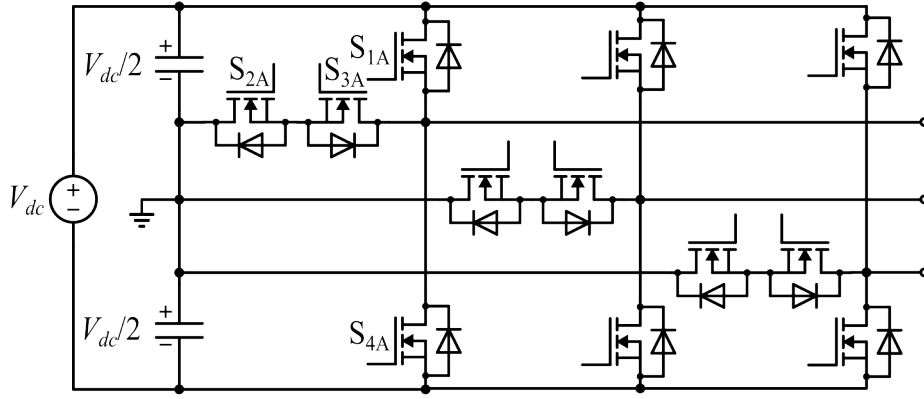


Figure 2.6: Circuit diagram of the 3-level T-type inverter with all SiC MOSFETs

For the placement of the inner switches connecting to the DC-link midpoint, two most common configurations to realize bidirectional switches are introduced here, shown as Fig. 2.7 (a) and Fig. 2.7 (b), a common-source configuration and a common-drain configuration [14]. In this project, common-source configuration was employed in the T-type inverter because it is a more widespread application in practice.

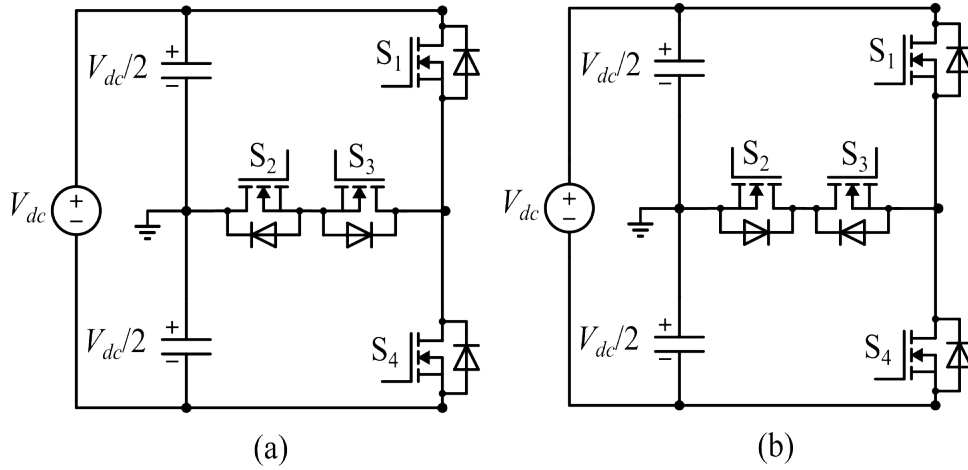


Figure 2.7: Inner switches configurations of three-level T-type inverter. (a) Common-source configuration and (b) common-drain configuration.

2.2.3.1 Output Voltage States

Table 2.2 summarized the output phase voltage with according switching states of one phase leg in the T-type inverter, illustrating that the output of one phase leg can be connected to the positive (P), neutral (O), or the negative (N) operating states [15]. The output current is considered positive when flowing from the inverter leg to the load and negative when flowing from the load into the inverter leg [13].

To reach the operating state "P", corresponding to an output phase voltage of $+V_{dc}/2$, switches S_1 and S_2 are turned on. The current flows through S_1 ; while S_2 associates current commutation process during transitions to other operating states. To reach the operating state "O", corresponding to an output phase voltage of 0 V, switches S_2 and S_3 are turned on. The current flows through S_2 and S_3 . To reach the operating state "N", corresponding to an output phase voltage of $-V_{dc}/2$, switches S_3 and S_4 are turned on. The current flows through S_3 ; similarly, S_4 associates current commutation processes. These operating states

remain the same regardless of the current direction, whereas the corresponding current commutation processes will be further illustrated in the following section [13].

Table 2.2: Switching states of one phase leg in the T-type inverter

State	Phase Voltage	S_1	S_2	S_3	S_4
P	$+V_{dc}/2$	1	1	0	0
O	0	0	1	1	0
N	$-V_{dc}/2$	0	0	1	1

2.2.3.2 PD-PWM Modulation and Current Paths

In this project, phase disposition pulse width modulation (PD-PWM) is adopted for the three-phase three-level T-type inverter since it's simple to implement and capable of generating positive, neutral, and negative output voltage states. Also PD-PWM is widely used in three-level inverter applications.

Fig. 2.8 illustrates the PD-PWM modulation applied in this three-level T-type inverter, with the modulation index set to $M = 0.9$. Two carrier signals are compared with the sinusoidal reference signal to generate the gate signals of switches S_{1A} , S_{2A} , S_{3A} and S_{4A} . Phase A is taken as an example, while phases B and C operate according to the same principle with a phase shift of 120° . The sinusoidal reference signal and positive carrier signal determine the switching status of S_{1A} and S_{3A} , and the sinusoidal reference signal and negative carrier signal determine the switching status of S_{2A} and S_{4A} . S_{1A} and S_{3A} are complementary, while S_{2A} and S_{4A} are complementary [16]. According to the comparison results between carrier signals and reference signal, the 3L T-type inverter can produce phase output voltage $+V_{dc}/2$, 0 and $-V_{dc}/2$, as listed in Table 2.2.

In this T-type inverter modulation, no extra dead-time was implemented. Since the employed PD-PWM only allows transitions through the neutral state (O) between positive (P) and negative (N). Besides, the Plecs model is ideal, and the device models in Plecs have turn-on and turn-off delay time. These are sufficient to prevent dc-link short-circuit conditions on outer switches.

Fig. 2.9 (a) zooms in on the comparison between the sinusoidal reference signal and positive carrier signal. When the reference signal is higher than the positive carrier signal, S_{1A} is turned on and S_{3A} is turned off, corresponding to state "P" with the phase output voltage $+V_{dc}/2$. When the reference signal is lower than the positive carrier signal, S_{1A} is turned off and S_{3A} is turned on, corresponding to state "O" with an output voltage of 0. Throughout the positive half-cycle, S_{2A} remains on while S_{4A} remains off. Fig. 2.9 (b) shows the switching state generation during the negative half-cycle. Similar to the positive half-cycle, state "N" results from when S_{2A} is turned off and S_{4A} is turned on, producing a phase output voltage of $-V_{dc}/2$. State "O" results from when S_{2A} is turned on and S_{4A} is turned off, producing a phase output voltage of 0. Throughout the negative half-cycle, S_{1A} remains off while S_{3A} remains on.

Fig. 2.10 (a) and (b) illustrates the current commutation paths of the 3L T-type inverter under positive phase current conditions ($I_a > 0$), corresponding to the state transitions from "P" to "O" (P-O) and from "O" to "P" (O-P), respectively, as shown in Fig. 2.9 (a). The

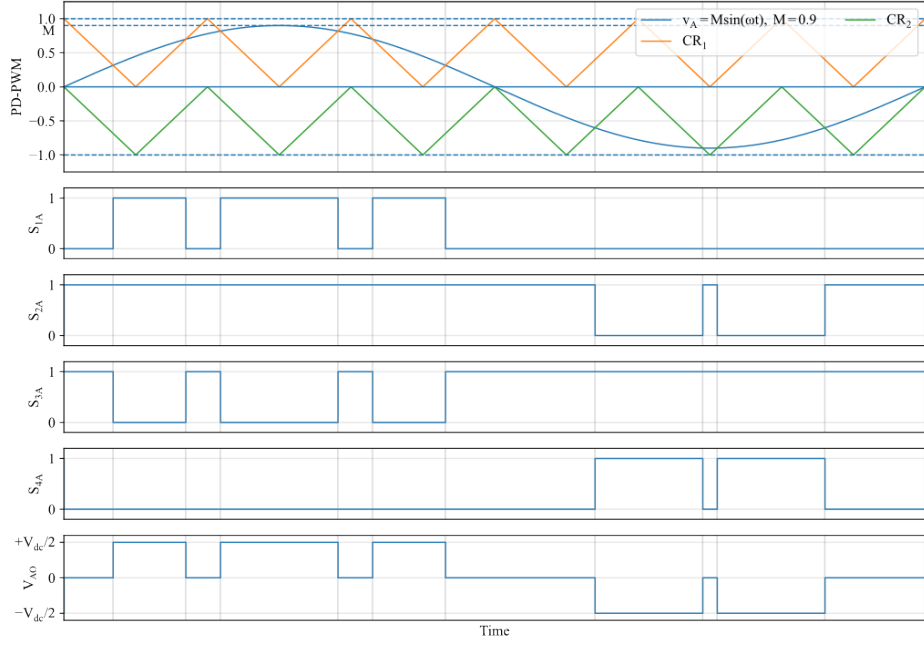


Figure 2.8: PD-PWM modulation, corresponding switching states and phase output voltage states of the three-level T-type inverter

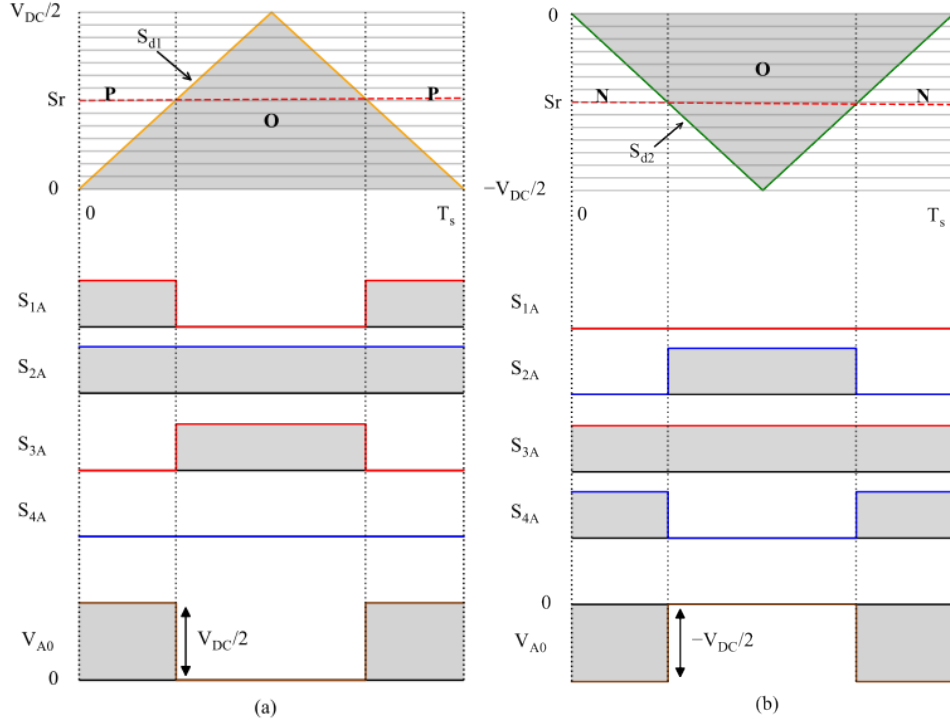


Figure 2.9: Switching state generation of the three-level T-type inverter under PD-PWM control. (a) Positive half-cycle (P-O-P) operation. (b) Negative half-cycle (N-O-N) operation.

red lines represent the current flow paths, while the switches highlighted in red denote the devices that are turned on.

The commutation paths shown in this figure are based on a full-SiC configuration, with all SiC MOSFETs. It should be noted that SiC MOSFETs are capable of bidirectional current conduction. When a SiC MOSFET is turned on, reverse current can be conducted through

both the MOSFET channel and the body diode, with the channel carrying the majority of the current due to its lower voltage drop. When the SiC MOSFET is turned off, reverse current can only flow through the antiparallel body diode. [17]. Therefore, although S_{3A} is turned off, the load current can still be maintained through the reverse-conduction path via the body diode to implement the current commutation process. When the inner switches S_{2A} and S_{3A} are replaced by GaN GITs in the hybrid SiC-GaN configuration, the current commutation paths still operate in the same way. However, the GaN GIT doesn't have a body diode, current flows from the drain to the source or vice versa.

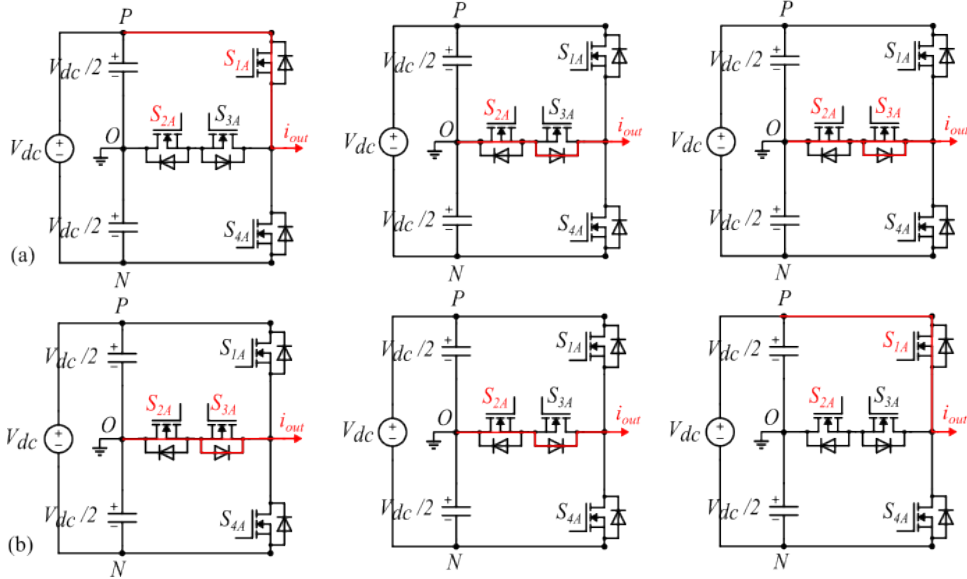


Figure 2.10: Current commutation paths of the three-level T-type inverter during positive phase current operation ($I_a > 0$). (a) Transition from the positive state to the neutral state (P-O). (b) Transition from the neutral state to the positive state (O-P).

Similarly, Fig. 2.11 (a) and (b) illustrates the current commutation paths of the 3L T-type inverter under negative phase current conditions ($I_a < 0$), corresponding to the state transitions from "N" to "O" (N-O) and from "O" to "N" (O-N), respectively, as shown in Fig. 2.9 (b).

From the current commutation paths of the three-level T-type inverter, it can be observed that inner switches (S_{2A}) and (S_{3A}) participate in every P-O-P and N-O-N transition, resulting in significantly higher switching activity than the outer switches (S_{1A}) and (S_{4A}). Therefore, the inner switches are expected to contribute a larger portion of the switching losses, particularly at high switching frequencies.

Since the outer switches mainly provide higher voltage blocking capability, while the inner switches experience most of the switching transitions, the hybrid configuration can replace the SiC MOSFETs with GaN GITs at inner switches (S_{2A}) and (S_{3A}) for better switching performance at high frequency and retain SiC MOSFETs at outer switches (S_{1A}) and (S_{4A}) for higher voltage blocking. The hybrid configuration is expected to achieve lower losses by reducing the switching losses of the most frequently commutated switches in the T-type inverter.

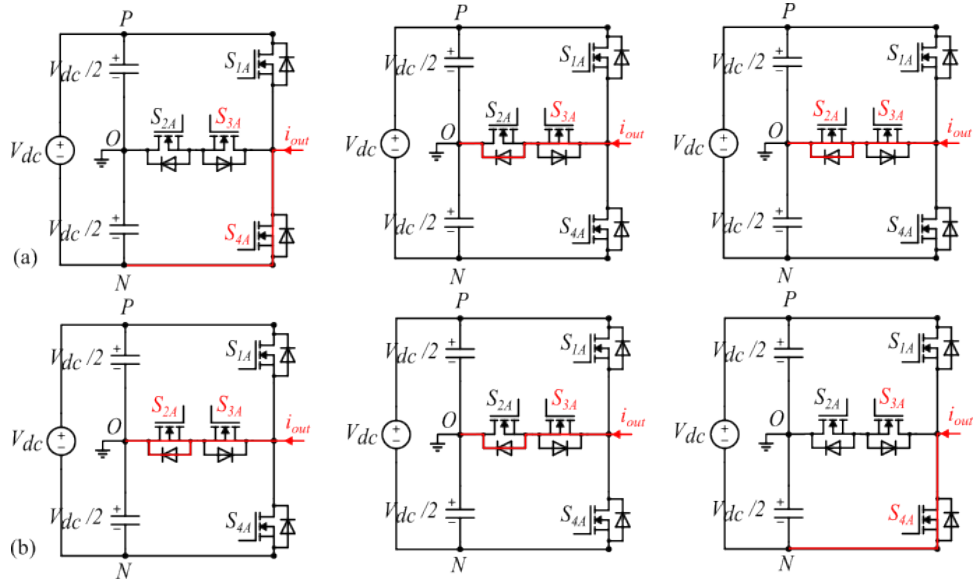


Figure 2.11: Current commutation paths of the three-level T-type inverter during negative phase current operation ($I_a < 0$). (a) Transition from the negative state to the neutral state (N-O). (b) Transition from the neutral state to the negative state (O-N).

3

a comparative analysis is carried out between Gallium Nitride Gate injection transistor (GIT) and Silicon Carbide (SiC) devices using the same inverter topology and operating conditions.

Based on commercially available GaN GIT and SiC MOSFET devices provided by Infineon and Wolfspeed, a technology-level qualitative comparison is presented in Table 3.1. The comparison provides a qualitative understanding of the advantages and limitations of each technology before the further device-level and inverter-level analyses presented in the following sections.

Table 3.1: Summary of Key Qualitative Comparison of GaN GITs and SiC MOSFETs

Characteristic	GaN GIT	SiC MOSFET
Cost	Medium	Medium
Available voltage range	Currently up to 700 V	Up to 1700 V
Current capability	Medium	High
Gate charge (Q_g)	Low	High
Output capacitance (C_{oss})	Medium	Medium
Reverse recovery charge (Q_{rr})	Negligible	Low
Switching speed	Very High	High
High-frequency capability	High	Medium–High

For the two-level inverter, each switching device must block the full DC-link voltage. Since the GaN and 650 V SiC devices are rated at 650 V, the DC-link voltage is set to 400 V for these configurations to remain within safe operating limits. For the 1200 V SiC configuration, the full 800 V DC-link voltage is applied. This difference in operating voltage must be taken into account when comparing two-level results against the three-level topologies.

Due to the limited availability of GaN GIT devices on the current market, the device selection process is constrained. Therefore, GaN GIT devices are first selected based on the required voltage rating of 650 V, while prioritizing higher current capability and lower on-state resistance. Corresponding SiC MOSFETs with comparable specifications are subsequently chosen to ensure a fair basis for comparison.

To ensure consistency in the evaluation, both GaN and SiC devices are implemented in the same PLECS simulation environment. To further enhance the reliability of the analysis, two groups of devices are selected.

The group 1 consists of a 650 V Infineon CoolGaN™ transistor (IGLT65R025D2), a 650 V Wolfspeed SiC MOSFET (C3M0025065J1) and a 1200 V Wolfspeed SiC MOSFET (E4MS025120J2). The group 2 consists of a 650 V Infineon CoolGaN™ transistor (IGOT65R025D2), a 650 V Wolfspeed SiC MOSFET (C3M0025065L) and a 1200 V Wolfspeed SiC MOSFET (E4MS025120K). The 1200 V Wolfspeed SiC MOSFET (E4MS025120K) employs a TO-247 through-hole package, whereas all other devices use surface-mount device (SMD) packages. Compared with through-hole packages, SMD packages generally offer a more compact structure, higher power density, lower parasitic inductance and capacitance, and are therefore more suitable for high-frequency switching applications. To investigate whether the package type influences the thermal performance of the devices, a through-hole packaged device with comparable electrical characteristics to other SMD devices was selected for comparison experiments. Static parameters such as on-state resistance $R_{DS(on)}$ and forward voltage drop V_F are taken directly from the respective manufacturer datasheets. The switching loss characterisation data, including E_{on} and E_{off} as functions of current and voltage, are obtained from the validated

PLECS thermal models provided by the device manufacturers, which are based on measurements performed under specified test conditions.

This approach enables cross-validation of the results and helps verify whether the observed performance differences reflect inherent physical characteristics of the technologies rather than device-specific variations.

Unlike traditional silicon-based devices, GaN and SiC technologies exhibit different switching and conduction characteristics. GaN devices are known for their extremely fast switching capability and negligible reverse recovery, while SiC devices offer better thermal robustness under high-power and high-temperature operating conditions.

With the same DC voltage requirement, both devices are subjected to identical electrical stress conditions. The resulting performance differences are primarily influenced by their intrinsic device properties, such as on-state resistance, switching energy, and capacitance.

The key characteristics of the selected GaN and SiC devices, based on datasheet values, are summarized in table 3.2 and table 3.3.

Table 3.2: Datasheet-Based Electrical Characteristics of Selected GaN and SiC Devices (Group 1)

Parameter	GaN 650 V	SiC 650 V	SiC 1200 V
Device	IGLT65R025D2	C3M0025065J1	E4MS025120J2
Technology	GaN GIT	SiC MOSFET	SiC MOSFET
Package	SMD	SMD	SMD
Voltage rating (V_{DS})	650 V	650 V	1200 V
Current rating (I_D)	67 A	80 A	82 A
On-state resistance ($R_{DS(on)}$)	25 m Ω	25 m Ω	25 m Ω
Gate charge (Q_g)	11 nC	109 nC	125 nC
Output capacitance (C_{oss})	130 pF	178 pF	103 pF
Turn-on switching energy (E_{on})	N/A	116 μ J	394 μ J
Turn-off switching energy (E_{off})	N/A	59 μ J	57 μ J
Reverse recovery charge (Q_{rr})	0 nC	274 nC	742 nC

* E_{on} and E_{off} for the GaN device are not available in the datasheet; switching loss data is obtained from the manufacturer-provided PLECS thermal model as described above. Current ratings are given at $T_C = 25^\circ\text{C}$.

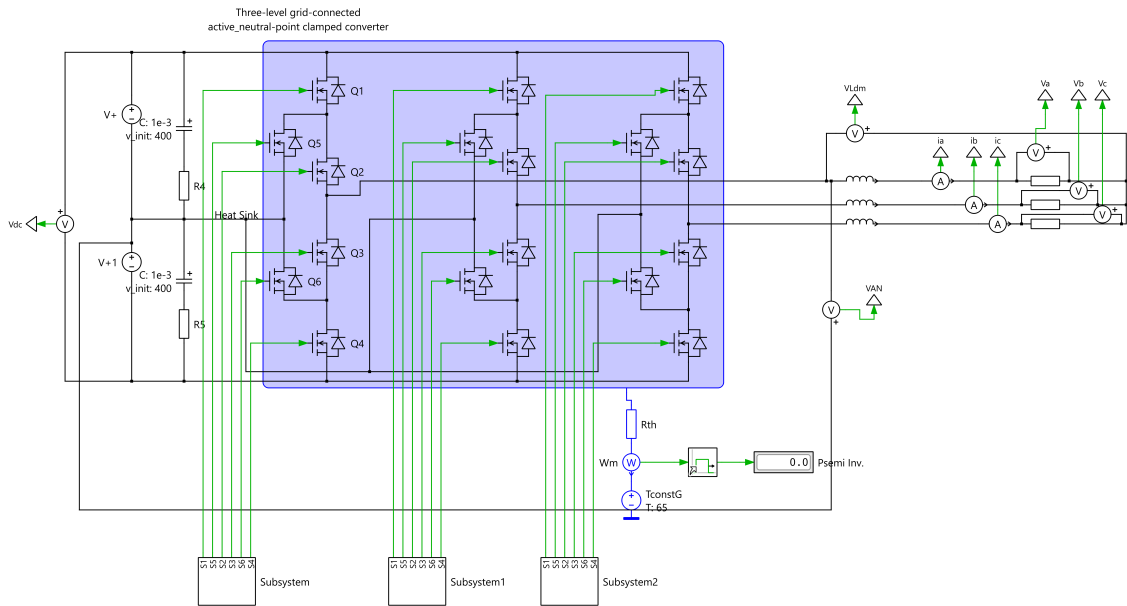
Table 3.3: Datasheet-Based Electrical Characteristics of Selected GaN and SiC Devices (Group 2)

Parameter	GaN 650 V	SiC 650 V	SiC 1200 V
Device	IGOT65R025D2	C3M0025065L	E4MS025120K
Technology	GaN GIT	SiC MOSFET	SiC MOSFET
Package	SMD	SMD	Through-Hole
Voltage rating (V_{DS})	650 V	650 V	1200 V
Current rating (I_D)	61 A	77 A	77 A
On-state resistance ($R_{ds(on)}$)	25 m Ω	25 m Ω	25 m Ω
Gate charge (Q_g)	11 nC	111 nC	125 nC
Output capacitance (C_{oss})	130 pF	186 pF	103 pF
Turn-on switching Energy (E_{on})	N/A	123 μ J	394 μ J
Turn-off switching Energy (E_{off})	N/A	14 μ J	57 μ J
Reverse recovery charge (Q_{rr})	0 nC	164 nC	742 nC

* E_{on} and E_{off} for the GaN device are not available in the datasheet; switching loss data is obtained from the manufacturer-provided PLECS thermal model as described above. Current ratings are given at $T_C = 25^\circ\text{C}$.

3.2.0.1 Simulation Model of the 3L ANPC Inverter

The three-level Active Neutral-Point Clamped (ANPC) inverter is implemented in PLECS as shown in Fig. 3.2. The model consists of a split DC-link with two series-connected voltage sources of $V_{dc}/2 = 400\text{ V}$ each, giving a total DC-link voltage of $V_{dc} = 800\text{ V}$. The phase leg contains six active switches arranged in three commutation cells. In the hybrid configuration, the outer switches (S_1, S_4, S_5, S_6) are implemented using Wolfspeed SiC MOSFET loss models, while the inner switches (S_2, S_3) use Infineon CoolGaN GIT loss models. Each device is represented by a thermal loss block in PLECS, with conduction and switching loss look-up tables derived directly from the manufacturer datasheets. The PWM-2 modulation signals are generated by comparing a sinusoidal reference S_r against two vertically offset triangular carriers, producing the four switching states P, O^+ , O^- , and N [7].

**Figure 3.2:** PLECS simulation model of the 3L-ANPC inverter

3.2.0.2 Simulation Model of the 3L SNPC Inverter

The three-level Sparse Neutral-Point Clamped (SNPC) inverter is modelled in PLECS as shown in Fig. 3.3. The three-level Sparse Neutral-Point-Clamped (SNPC) inverter is modelled in PLECS as shown in Fig. 3.3. As described in Section 2.2.2, the topology consists of two cascaded stages which are implemented here as separate subcircuits connected in series. The SM devices each block only $V_{dc}/2$ and are represented in PLECS using GaN GIT loss models in the hybrid configuration, while the 2L inverter stage devices block the full V_{dc} and use 1200 V SiC MOSFET loss models. The total device count across both stages is ten active semiconductors per three-phase system, compared with twelve in the ANPC [12]. Space-vector modulation is applied using the symmetric Sequence U, implemented as a vector-based switching sequence generator within the PLECS model. As with the ANPC model, Loss data are handled in the same manner as described for the ANPC model above, and entered as two-dimensional look-up tables indexed by current and junction temperature.

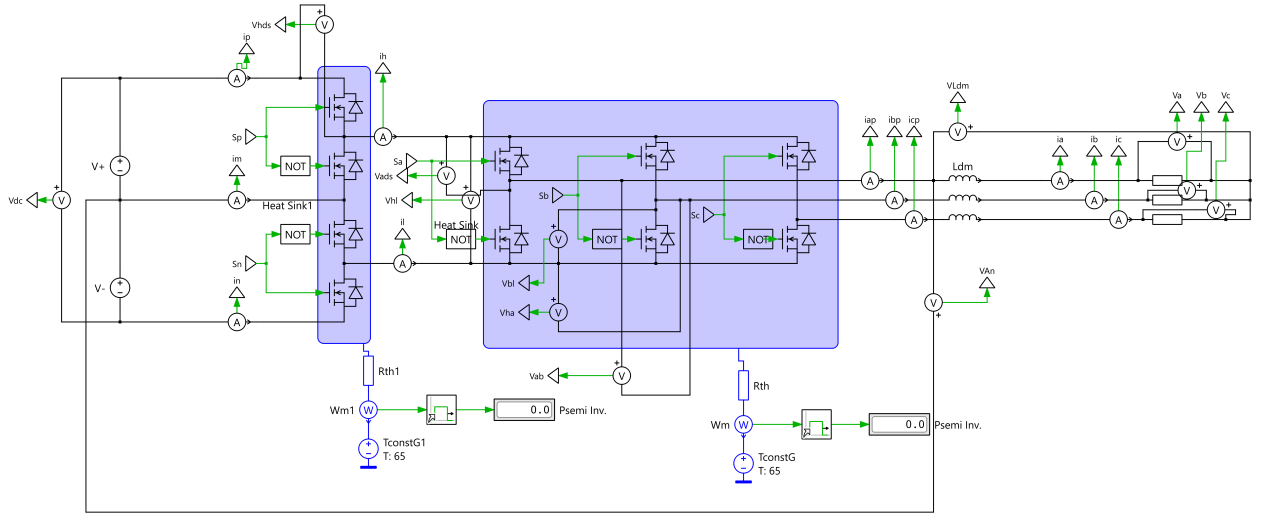


Figure 3.3: PLECS simulation model of the 3L-SNPC inverter

3.2.0.3 Simulation Model of the 3L T-type Inverter

The three-level T-type inverter is modeled in PLECS, as shown in Fig. 3.4. The model operates under conventional hard-switching conditions and employs an open-loop control structure. PD-PWM modulation is applied to all three phases, with a phase shift of 120° between each phase. An RL load is used to emulate the electrical characteristics of an electric motor. Parasitic capacitances and EMI-related effects are not considered in this project.

In the hybrid configuration, the outer switches (S_1 , S_4) employ Wolfspeed SiC MOSFET thermal models, and the inner switches (S_2 , S_3) employ Infineon CoolGaN GIT thermal models.

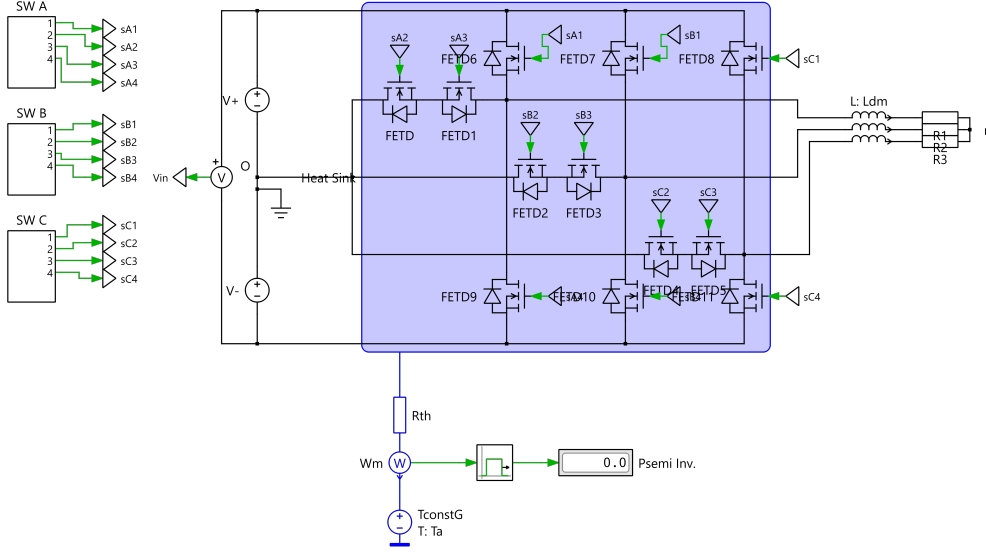


Figure 3.4: PLECS simulation model of the 3L T-type inverter

3.2.1 Operating Point and Load Parameters

The simulation is configured to represent a realistic operating point for an automotive traction inverter. The derived operating point quantities are summarised in Table 3.4.

Table 3.4: Summary of Simulation Operating Conditions

Parameter	Symbol	Value
DC-link voltage	V_{dc}	800 V
Fundamental frequency	f	50 Hz
Peak phase current	I_{pk}	50 A
Power factor angle	ϕ	60°
Modulation index	M	0.9
Switching frequency	f_{sw}	10 kHz
Gate resistance	R_g	2.5 Ω
Ambient temperature	T_a	65 °C
Peak phase voltage	V_{pk}	360 V
RMS phase voltage	V_{rms}	254.6 V
RMS phase current	I_{rms}	35.36 A
Three-phase output power	P_{out}	13.5 kW

The DC-link voltage, fundamental frequency, modulation index, peak phase current, modulation index, switching frequency, gate resistance and ambient temperature are predefined simulation parameters. The remaining parameters, including peak phase voltage, RMS phase voltage, RMS phase current and three-phase output power are derived from these operating conditions and are calculated as follows.

The peak phase voltage is therefore:

$$V_{pk} = 0.5 \times M \times V_{dc} = 0.5 \times 0.9 \times 800 = 360 \text{ V} \quad (3.1)$$

The corresponding RMS phase voltage and current are $V_{rms} = 254.6 \text{ V}$ and $I_{rms} = 35.36 \text{ A}$, respectively. The three-phase output power at this operating point is

$$P_{out} = 3 \times V_{rms} \times I_{rms} \times \cos \phi = 3 \times 254.6 \times 35.36 \times 0.5 \approx 13.5 \text{ kW} \quad (3.2)$$

The load resistance and inductance are derived from the required phase impedance as follows:

$$Z = \frac{V_{\text{pk}}}{I_{\text{pk}}} \quad (3.3)$$

$$R = Z \cos \phi \quad (3.4)$$

$$L = \frac{Z \sin \phi}{2\pi f} \quad (3.5)$$

The values of R and L are set according to the operating point under investigation for each topology and passed directly to the PLECS model as the load parameters R and L_{dm} . The parametric sweeps carried out in this study are summarised in Table 3.5. Each parameter is varied independently while the remaining parameters are held at their reference values.

Table 3.5: Parametric sweep ranges for loss analysis

Parameter	Values investigated	Reference value	Unit
Switching frequency f_{sw}	10, 20, 50, 70, 100	10	kHz
Peak output current I_{pk}	40, 45, 50	50	A
Ambient temperature T_{amb}	45, 65, 85	65	°C

4

Results

4.1 Simulation results Analysis of the 2-Level 3-Phase Inverter

This section presents the simulation results of the two-level inverter implemented in PLECS using 650 V GaN and 650 V SiC semiconductor devices. The performance is evaluated in terms of conduction losses, switching losses, and total losses under varying operating conditions.

The general operating conditions are shown in table 4.1. Sine PWM was employed as the controller configuration.

Table 4.1: General operating conditions for the 2-level inverter

Parameter	Description	Value
V_{dc}	Inverter DC input voltage	400 V
V_{rms}	RMS phase voltage	140 V
I_{rms}	RMS phase current	35.5 A
f_{sw}	Switching frequency	10 kHz
R_g	Gate resistance	2.5 Ω
T_a	Ambient temperature	65 $^{\circ}\text{C}$

4.1.1 Group 1 devices

4.1.1.1 Loss Analysis at Different Output Currents

The inverter was simulated at a fixed switching frequency of 10 kHz while varying the output current. It should be noted that for the two-level inverter analysis, a DC-link voltage of 400 V is used for the all-GaN and 650 V SiC configurations, since GaN devices are today typically rated at 650 V and cannot block the full 800 V DC-link voltage. The 1200 V SiC configuration is evaluated at the full 800 V DC-link voltage. This distinction is important when comparing results across configurations, as the operating voltage directly affects both conduction and switching loss.

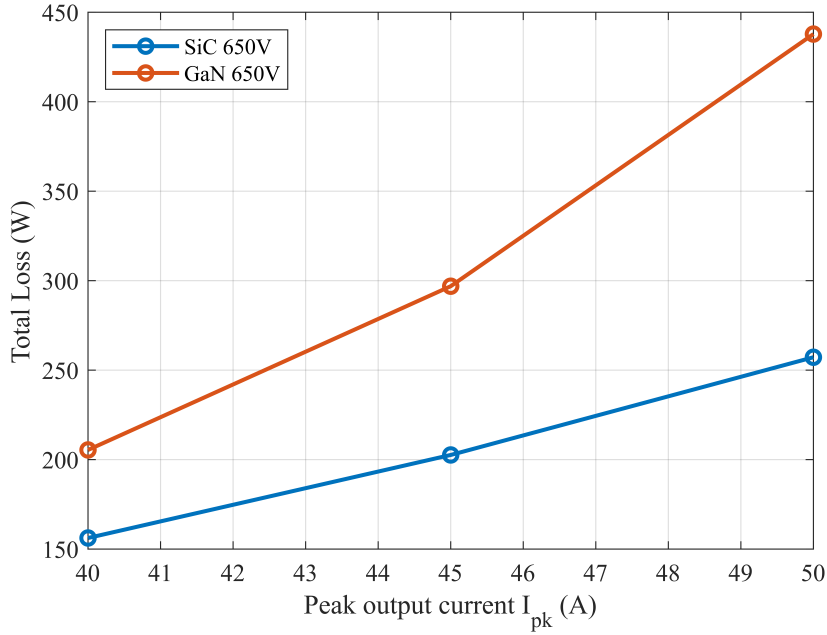


Figure 4.1: Two-level inverter: Total loss vs output current ($V_{dc} = 400$ V, $f_{sw} = 10$ kHz, $T_a = 65^\circ\text{C}$)

Fig. 4.1 shows total loss versus output current at 10 kHz. SiC losses increase moderately with current, while GaN losses rise steeply, reaching 437.8 W at 50 A compared to 257.2 W for SiC. This confirms that GaN is at a significant disadvantage in high-current, conduction-dominant conditions. From the results, it can be observed that:

- Conduction losses increase significantly with output current for both devices.
- GaN exhibits higher conduction losses compared to SiC at all current levels. This is because the $R_{DS(on)}$ of GaN GIT devices increases strongly with drain current due to the gate injection mechanism, whereas SiC MOSFETs show only a weak current dependence, resulting in more stable conduction losses.
- Switching losses are much lower in GaN compared to SiC.
- At 10 kHz, total losses are dominated by conduction losses, making SiC the better choice at low switching frequency.

4.1.1.2 Loss Analysis at Different Switching Frequencies

The inverter was further analyzed at different switching frequencies while maintaining a constant operating condition of 14 kW output power and 33.3 A RMS current.

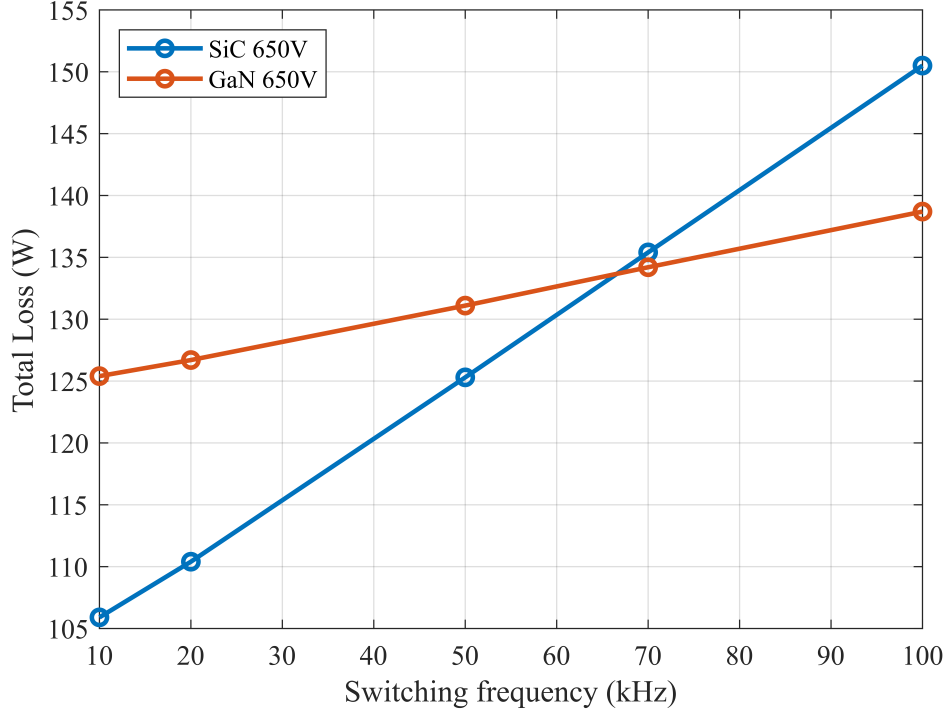


Figure 4.2: Two-level inverter: Total loss vs switching frequency ($V_{dc} = 400\text{ V}$, $I_{pk} = 50\text{ A}$, $T_a = 65^\circ\text{C}$)

The following observations can be made from Fig. 4.2:

- At 10 kHz, SiC achieves lower total losses (105.9 W) compared to GaN (125.4 W), as conduction losses dominate at low switching frequencies and SiC has a lower $R_{DS(on)}$.
- As switching frequency increases, SiC losses rise steeply due to higher switching energy, while GaN losses increase only gradually owing to its near-zero switching energy.
- At approximately 70 kHz, the two configurations reach near-parity (SiC: 135.4 W, GaN: 134.2 W), marking the crossover frequency beyond which GaN becomes the more efficient choice.
- At 100 kHz, GaN achieves 138.7 W compared to 150.5 W for SiC, confirming GaN as the superior option at high switching frequencies.

4.1.2 Group 2 devices

4.1.2.1 Loss Analysis at Different Switching Frequencies

To evaluate the effect of switching frequency, the switching frequency is varied among 10 kHz, 20 kHz, 50 kHz, 100 kHz and 150 kHz, while the dc-link voltage, output current, ambient temperature, and gate resistance are maintained constant at the nominal operating conditions listed in Table 4.1.

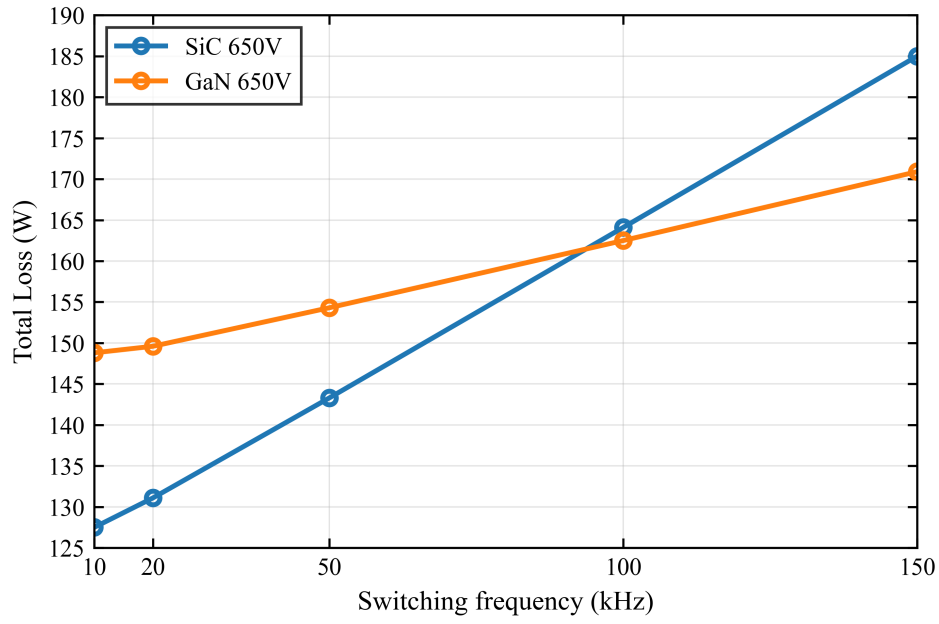


Figure 4.3: Two-level inverter: total loss under different switching frequency, for $V_{dc} = 400$ V, $I_{pk} = 50$ A, $T_a = 65$ °C and varying of $f_{sw} = 10$ kHz, $f_{sw} = 20$ kHz, $f_{sw} = 50$ kHz, $f_{sw} = 100$ kHz and $f_{sw} = 150$ kHz

The following observations can be made from Fig. 4.3:

- GaN switching loss is much lower. If lower the current level when conduction losses are not dominating the total losses, GaN GIT exhibits advantages over SiC.

4.1.2.2 Loss Analysis at Different Output Power

To evaluate the effect of output current, the output power is varied among 2500 W, 5000 W, 10000 W and 15000 A, while the dc-link voltage, switching frequency, ambient temperature, and gate resistance are maintained constant at the nominal operating conditions listed in Table 4.1.

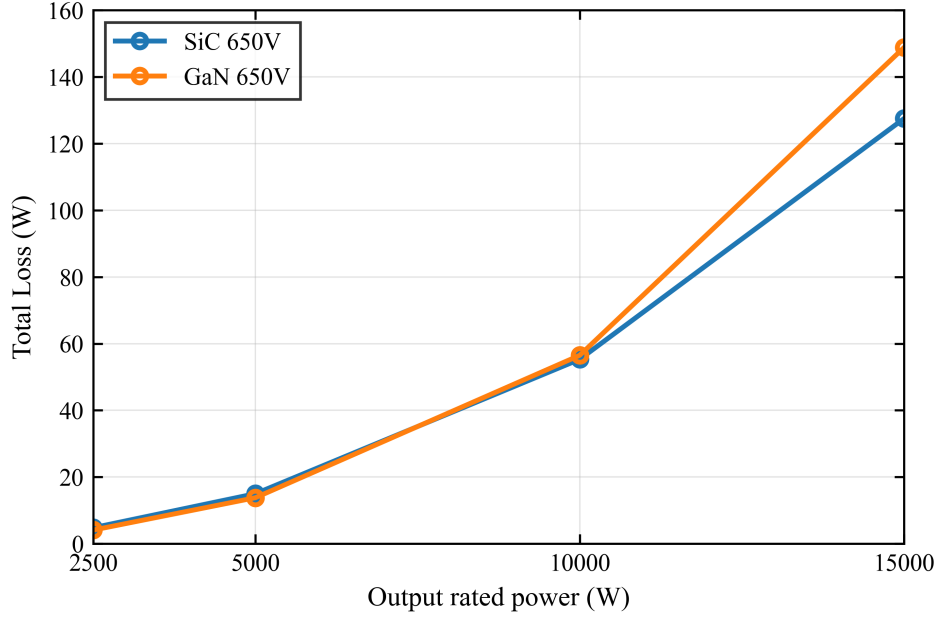


Figure 4.4: Two-level inverter: total loss under different output power, for $V_{dc} = 400$ V, $T_a = 65$ °C, $f_{sw} = 10$ kHz and varying of $P_{out} = 2500$ W, $P_{out} = 5000$ W, $P_{out} = 10000$ W, and $P_{out} = 15000$ W

The following observations can be made from Fig. 4.4:

From the results, observed an unsolved problem:

- At high power level 15000W, GaN shows higher conduction losses than SiC, while at lower power both become similar, which is not clearly supported by the datasheet $R_{ds(on)}$ values.

4.1.2.3 Loss Analysis at Different Temperatures

To evaluate the effect of ambient temperature, the ambient temperature is varied among 25°C, 45°C and 65°C, while the dc-link voltage, switching frequency, output current, and gate resistance are maintained constant at the nominal operating conditions listed in Table 4.1.

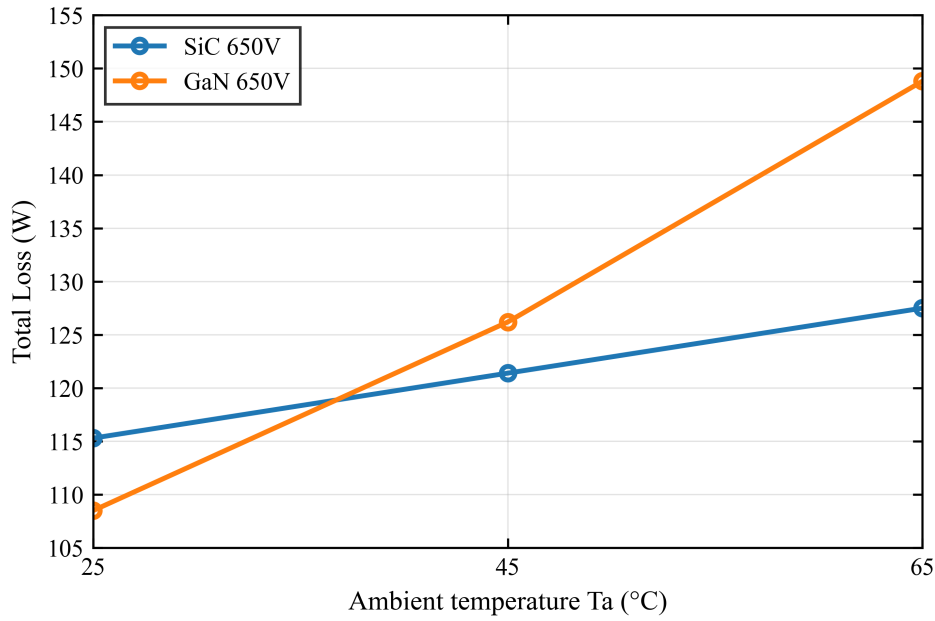


Figure 4.5: Two-level inverter: total loss under different ambient temperature, for $V_{dc} = 400$ V, $I_{pk} = 50$ A, $f_{sw} = 10$ kHz and varying of $T_a = 25$ °C, $T_a = 45$ °C and $T_a = 65$ °C

The following observations can be made from Fig. 4.5:

- At lower temperature, GaN has lower conduction losses. GaN GIT conduction losses increase when temperature increases while SiC does not increase as much which indicates the current Infineon GIT technology is not mature regarding thermal performance and needs to be improved for high temperature applications. Combined with previous varying rated power simulations, it is observed that GaN GIT is not preferred for high current applications.

4.2 Loss Analysis of the 3-Level ANPC Inverter

The loss performance of the 3L-ANPC inverter was evaluated across six semiconductor configurations. The investigated cases include 650 V SiC, 1200 V SiC, GaN, 650 V SiC–GaN hybrid, and 1200 V SiC–GaN hybrid devices. The comparison was carried out at a DC-link voltage of 800 V. The main objective was to observe how the conduction loss, switching loss, and total semiconductor loss vary with switching frequency, output current, and ambient temperature.

4.2.1 Simulation Validation

Before presenting the loss results, the correct operation of the ANPC simulation model is confirmed through the steady-state output waveforms shown in Fig. 4.6. The phase current reaches the expected peak of $I_{pk} = 50$ A at the fundamental frequency of 50 Hz, confirming that the load parameters are correctly set. The three-level phase leg voltage v_{AO} clearly shows three distinct voltage levels: $+V_{dc}/2 = +400$ V, 0 V, and $-V_{dc}/2 = -400$ V, validating the correct implementation of the PWM-2 modulation strategy [7]. The sinusoidal shape of the output current confirms that the RL load is operating at the intended power factor angle of $\phi = 60^\circ$.

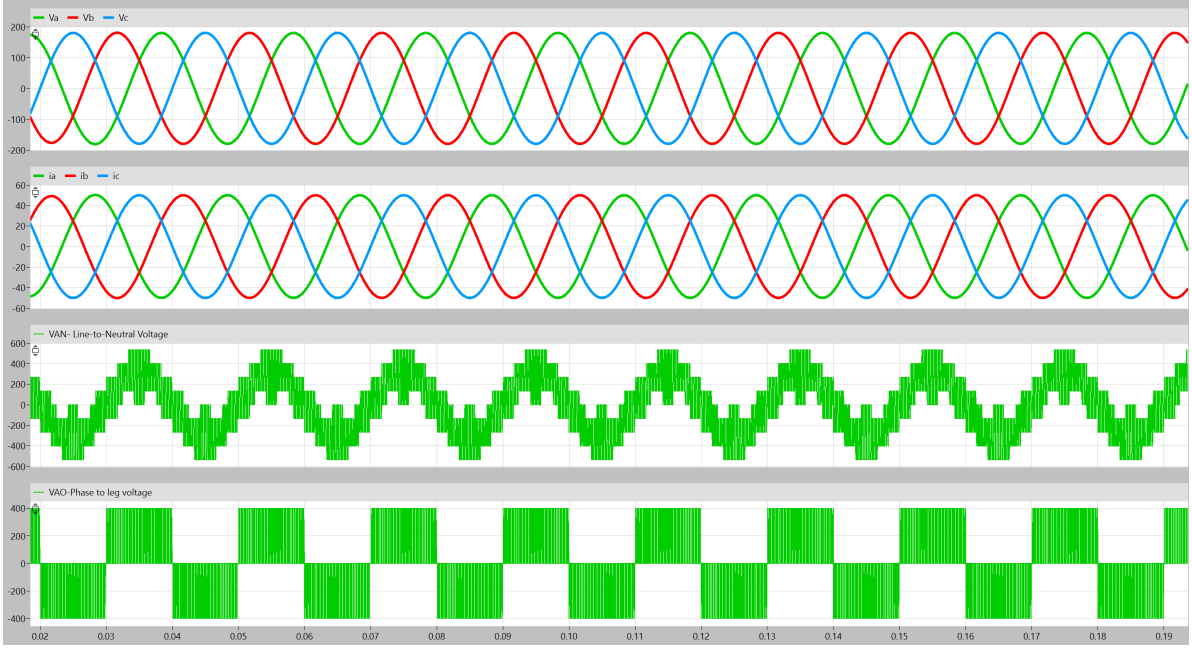


Figure 4.6: Steady-state output waveforms of the 3L-ANPC inverter: (a) filtered phase voltage, (b) phase current, (c) Line-to-Neutral voltage, (d) phase-to-leg-voltage

In addition to the output waveforms, as shown in Fig. 4.7 the thermal operating conditions of each device are verified to ensure that the junction temperature does not exceed the maximum rated value. The PLECS thermal model assigns a thermal resistance from junction to ambient for each device, and the steady-state junction temperatures are monitored under the reference operating conditions ($V_{dc} = 800$ V, $I_{pk} = 50$ A, $T_a = 65$ °C, $f_{sw} = 10$ kHz). All devices remain within their rated junction temperature limits throughout the simulation, confirming that the selected operating conditions are thermally feasible for the chosen device configurations.

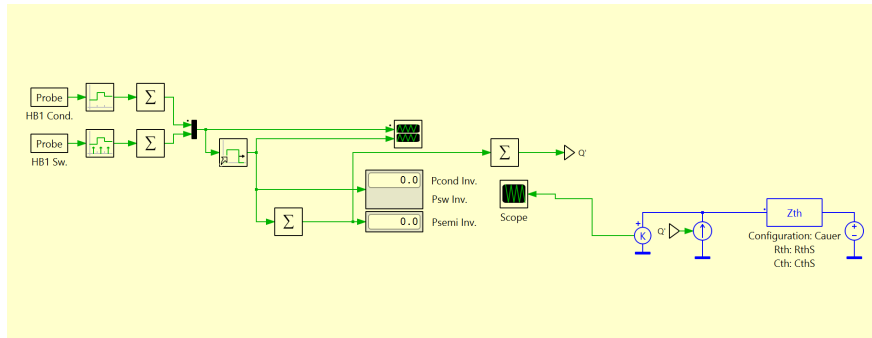


Figure 4.7: Causer thermal model used in the 3L-ANPC simulation to verify that junction temperatures remain within rated limits $V_{dc} = 800$ V, $f_{sw} = 10$ kHz, $I_{pk} = 50$ A, $T_a = 65$ °C.

4.2.2 Loss Variation with Switching Frequency

Figure 4.8 shows the loss variation with switching frequency for the different ANPC semiconductor configurations. As expected, the switching loss increases as the switching frequency is increased from 10 kHz to 100 kHz. This is because the number of switching transitions per second increases in proportion with the switching frequency. The conduction loss remains almost constant for each device case because the output current and operating temperature are fixed during this comparison.

The 1200 V SiC case shows the highest total loss at higher switching frequencies due to its larger switching loss contribution. In contrast, the GaN-based and hybrid configurations show much lower switching loss. This indicates that GaN devices are more suitable for high-frequency operation, especially when switching loss becomes a dominant part of the total loss. Among the investigated ANPC cases, the hybrid SiC-GaN configurations provide a good balance between conduction and switching losses. Fig. 4.8 shows the total loss versus switching frequency for the five device configurations evaluated in the 3L-ANPC inverter:

- **650 V SiC**: all six switches are Wolfspeed 650 V SiC MOSFETs (C3M0025065J1)
- **1200 V SiC**: all six switches are Wolfspeed 1200 V SiC MOSFETs (E4MS025120J2)
- **GaN**: all six switches are Infineon 650 V CoolGaN GIT devices (IGLT65R025D2)
- **650 V SiC+GaN**: hybrid configuration: GaN devices in the inner switch positions (S_2, S_3) and 650 V SiC MOSFETs in the outer positions (S_1, S_4, S_5, S_6)
- **1200 V SiC+GaN**: hybrid configuration: GaN devices in the inner switch positions (S_2, S_3) and 1200 V SiC MOSFETs in the outer positions (S_1, S_4, S_5, S_6)

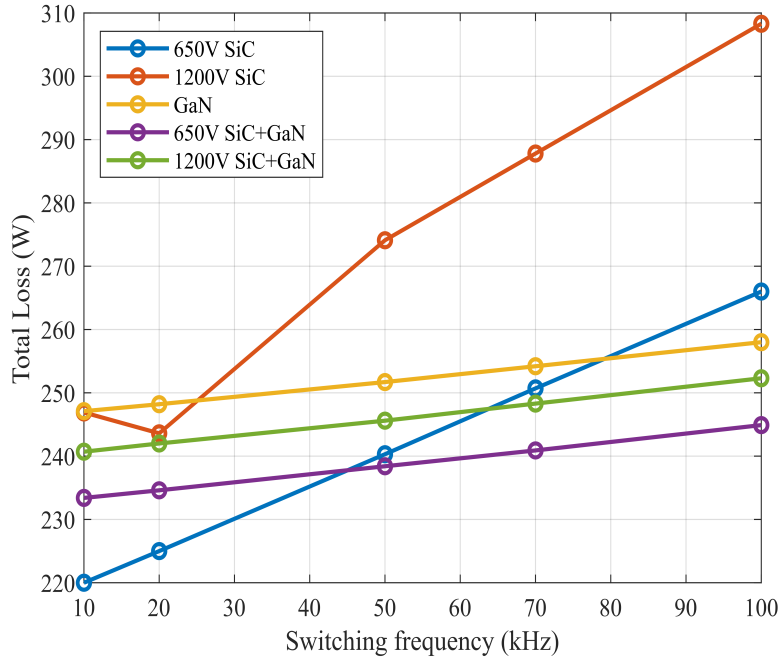


Figure 4.8: 3L-ANPC total power losses vs. switching frequency at $V_{dc} = 800$ V, $P_{out} = 13.5$ kW, $I_{pk} = 50$ A, $T_a = 65$ °C

Fig. 4.9 shows the corresponding inverter efficiency across switching frequencies, calculated as

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \times 100\% \quad (4.1)$$

where $P_{out} = 13.5$ kW.

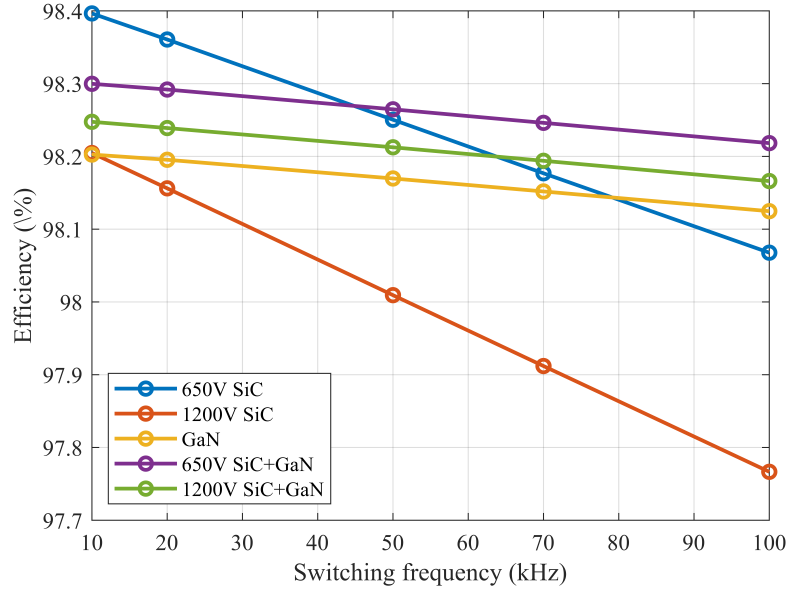


Figure 4.9: 3L-ANPC inverter efficiency vs switching frequency ($V_{dc} = 800\text{ V}$, $P_{out} = 13.5\text{ kW}$, $I_{pk} = 50\text{ A}$, $T_a = 65^\circ\text{C}$)

4.2.3 Loss Variation with Output Current

Figure 4.10 presents the loss variation with output current. The total loss increases clearly as the peak output current increases from 40 A to 50 A. This trend is mainly caused by the increase in conduction loss, since conduction loss is strongly dependent on current. The switching loss changes only slightly with current in comparison with the conduction loss. For all ANPC configurations, the conduction loss is the dominant loss component at the investigated operating points. The hybrid configurations show lower total loss compared with the pure SiC cases, especially at lower and medium current levels. This behaviour suggests that combining SiC and GaN devices can improve the overall efficiency of the ANPC inverter when the device placement is selected properly.

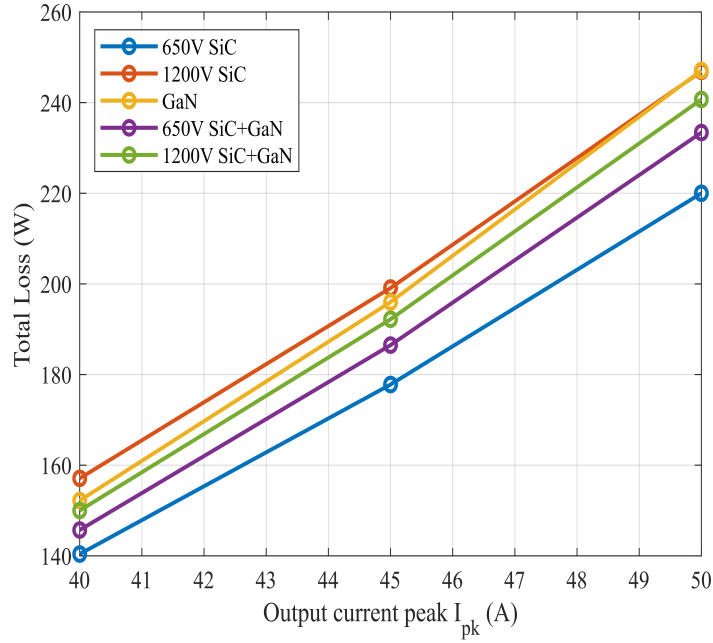


Figure 4.10: 3L-ANPC total power losses vs. peak output current at $V_{dc} = 800$ V, $P_{out} = 13.5$ kW, $f_{sw} = 10$ kHz, $T_a = 65$ °C

Fig. 4.11 shows the inverter efficiency as a function of output current.

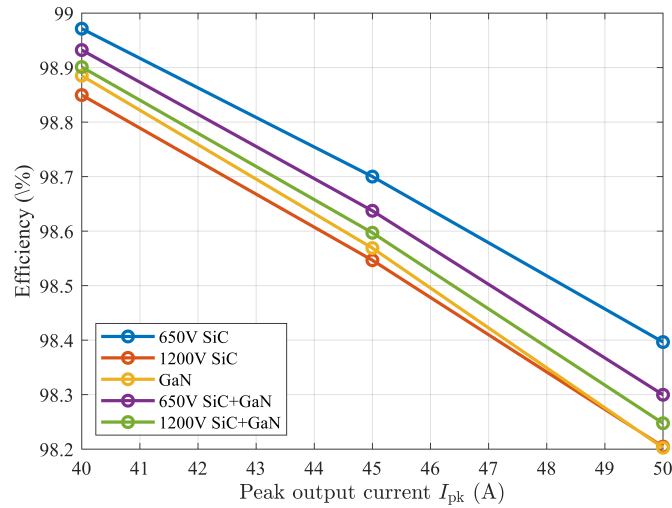


Figure 4.11: 3L-ANPC inverter efficiency vs output current at $V_{dc} = 800$ V, $P_{out} = 13.5$ kW, $f_{sw} = 10$ kHz, $T_a = 65$ °C

4.2.4 Loss Variation with Ambient Temperature

Figure 4.12 shows the influence of ambient temperature on the inverter losses. When the ambient temperature increases from 45°C to 85°C, the total loss also increases. This increase

is mainly related to the rise in conduction loss, since the on-state resistance of semiconductor devices generally increases with temperature.

The switching loss remains almost unchanged with temperature in the investigated range. Therefore, the temperature sensitivity of the total loss is mainly determined by the conduction behaviour of the devices. The GaN and hybrid configurations show noticeable loss variation with temperature, while the SiC-based configurations also follow the same general increasing trend. This confirms that thermal conditions must be considered carefully when selecting the semiconductor configuration for high-power inverter operation.

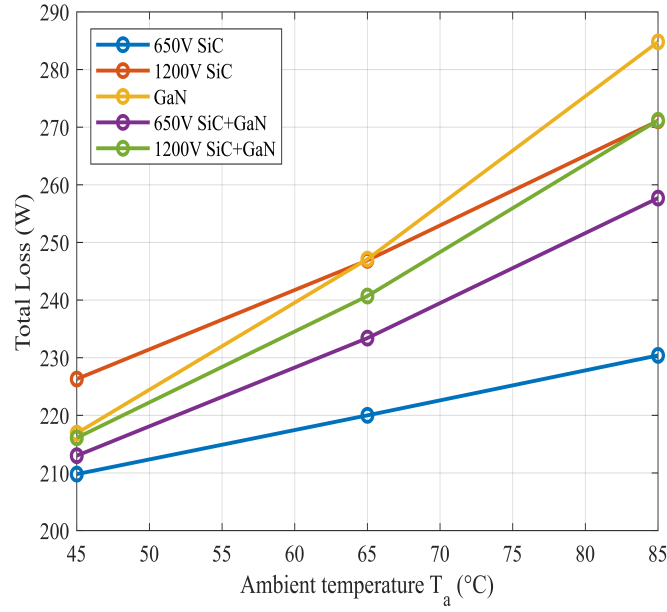


Figure 4.12: 3L-ANPC total power losses vs. ambient temperature at $V_{dc} = 800$ V, $P_{out} = 13.5$ kW, $f_{sw} = 10$ kHz, $I_{pk} = 50$ A

Fig. 4.13 shows the inverter efficiency as a function of ambient temperature.

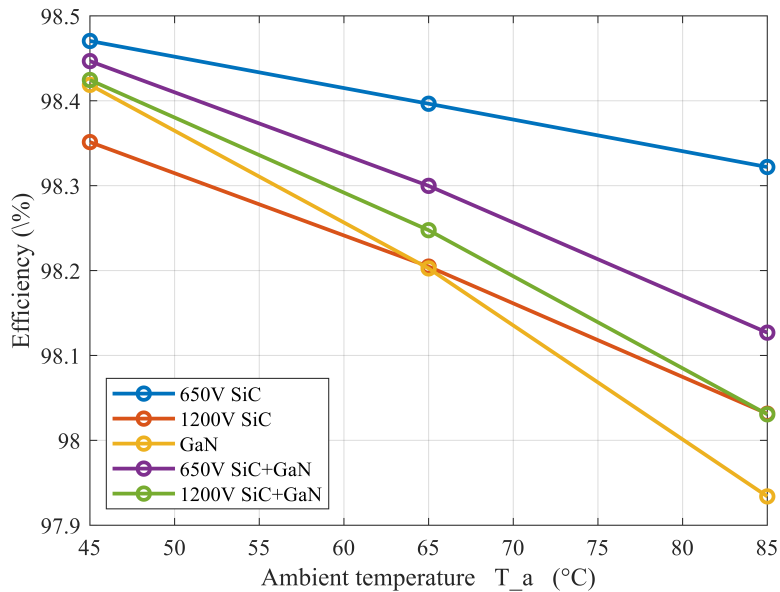


Figure 4.13: 3L-ANPC inverter efficiency vs ambient temperature at $V_{dc} = 800$ V, $P_{out} = 13.5$ kW, $I_{pk} = 50$ A, $f_{sw} = 10$ kHz

4.2.5 Summary

From the ANPC loss comparison, it can be observed that the switching frequency is the dominant factor affecting switching loss, increasing it proportionally with frequency. However, switching loss is also influenced by output current, since the switching energy E_{on} and E_{off} are current-dependent quantities in the device loss models. The output current and ambient temperature primarily influence conduction loss, as $R_{DS(on)}$ increases with both current and junction temperature. The pure 1200 V SiC case gives higher total loss at high switching frequency due to its larger switching loss. The GaN and SiC-GaN hybrid configurations reduce switching losses by up to 75% compared to the pure SiC cases at 100 kHz and are therefore more attractive for high-frequency operation. Overall, the hybrid ANPC structure provides a good compromise between conduction loss, switching loss, and thermal performance.

4.3 Loss Analysis of the 3-Level SNPC Inverter

The loss behaviour of the 3-level Stacked Neutral Point Clamped (SNPC) inverter was analysed for two semiconductor configurations: a 1200 V SiC-based SNPC inverter and a hybrid SNPC inverter. The analysis was performed at a DC-link voltage of 800 V. The loss comparison includes the effect of switching frequency, output current, and ambient temperature on conduction loss, switching loss, and total inverter loss.

4.3.1 Simulation Validation

The correct operation of the SNPC simulation model is confirmed through the steady-state output waveforms shown in Fig. 4.14. The three-phase output currents reach the expected peak of $I_{pk} = 50$ A at 50 Hz, and the phase leg voltage v_{AO} clearly shows three distinct voltage levels: $+V_{dc}/2 = +400$ V, 0 V, and $-V_{dc}/2 = -400$ V, validating the correct switching behaviour of the SNPC topology under space-vector modulation. The sinusoidal output current confirms operation at the intended power factor angle of $\phi = 60^\circ$.

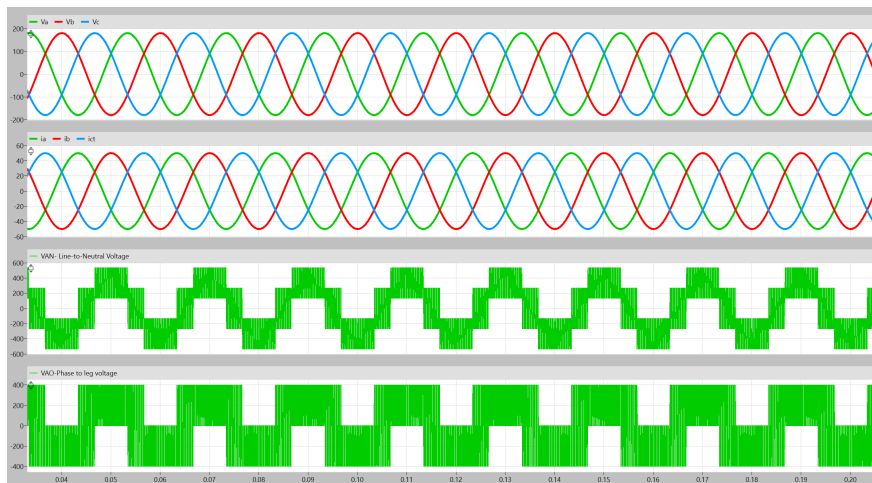


Figure 4.14: Steady-state output waveforms of the 3L-SNPC simulation model at $V_{dc} = 800$ V, $P_{out} = 13.5$ kW, $f_{sw} = 10$ kHz, $I_{pk} = 50$ A, $T_a = 65^\circ\text{C}$: (a) filtered phase voltage, (b) phase current, (c) Line-to-Neutral voltage, (d) phase-to-leg-voltage

4.3.2 Loss Variation with Switching Frequency

Figure 4.15 shows the loss comparison of the SNPC inverter as the switching frequency is varied from 10 kHz to 100 kHz. For both configurations, the conduction loss remains nearly constant over the full frequency range. This is expected because the current and temperature are kept constant during this comparison.

The switching loss increases significantly with frequency. The 1200 V SiC SNPC case shows a much larger increase in switching loss compared with the hybrid SNPC case. At 100 kHz, the switching loss contribution becomes very large for the pure SiC case, which results in a higher total loss. The hybrid SNPC configuration gives lower switching loss over the complete frequency range, showing its advantage for high-frequency operation.

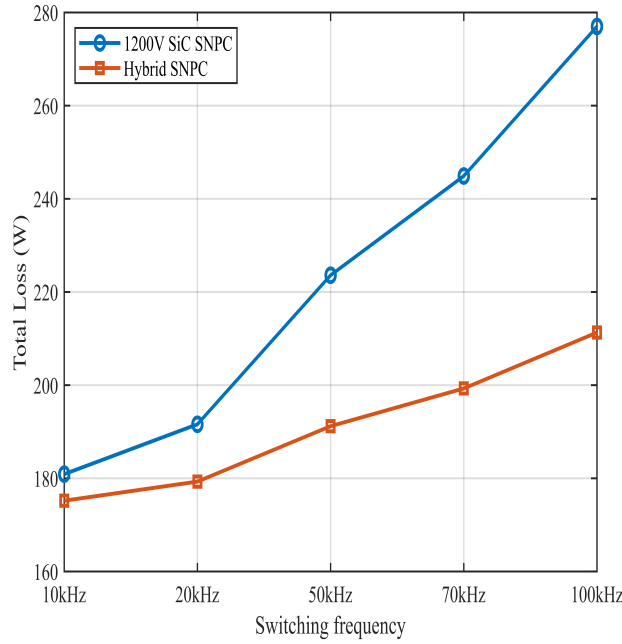


Figure 4.15: 3L-SNPC total power losses vs. switching frequency at $V_{dc} = 800\text{ V}$, $P_{out} = 13.5\text{ kW}$, $I_{pk} = 50\text{ A}$, $T_a = 65^\circ\text{C}$

Fig. 4.16 shows the corresponding SNPC inverter efficiency across switching frequencies.

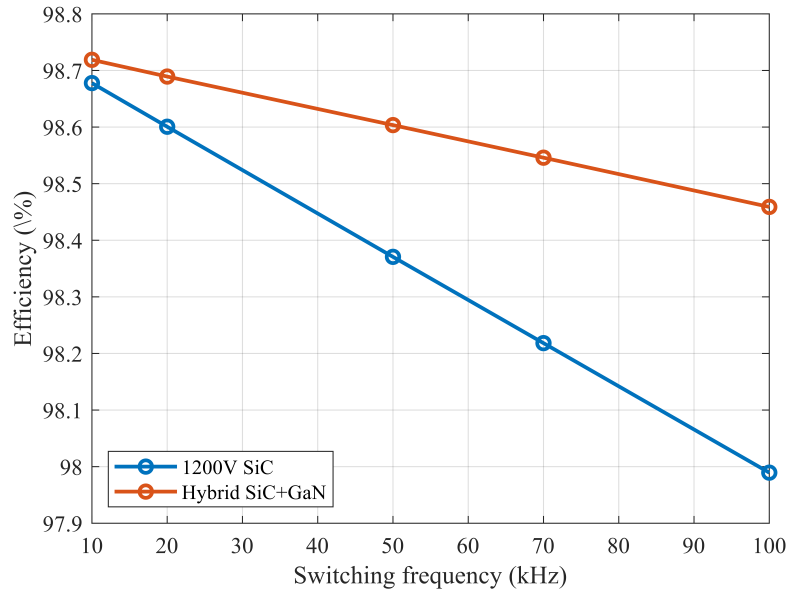


Figure 4.16: 3L-SNPC inverter efficiency vs switching frequency $V_{dc} = 800\text{ V}$, $P_{out} = 13.5\text{ kW}$, $I_{pk} = 50\text{ A}$, $T_a = 65^\circ\text{C}$

4.3.3 Loss Variation with Output Current

Figure 4.17 presents the SNPC loss variation with output current. The total loss increases as the peak output current increases from 40 A to 50 A. The main reason for this increase is the higher conduction loss at larger current. The switching loss changes only slightly with current compared with the conduction loss.

Both SNPC configurations show similar conduction loss behaviour, but the hybrid SNPC has lower switching loss. As a result, the hybrid configuration gives lower total loss at all investigated current levels. This makes the hybrid SNPC structure beneficial when both efficiency and switching performance are important. Fig. 4.18 shows the SNPC inverter efficiency as a function of output current.

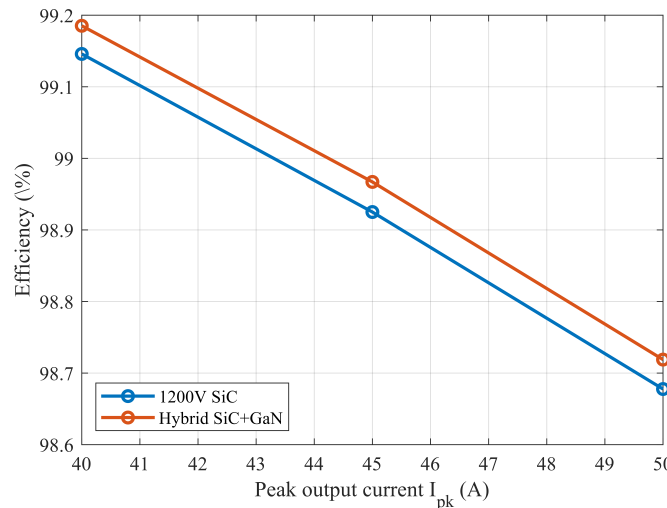


Figure 4.18: 3L-SNPC inverter efficiency vs output current $V_{dc} = 800\text{ V}$, $P_{out} = 13.5\text{ kW}$, $f_{sw} = 10\text{ kHz}$, $T_a = 65^\circ\text{C}$

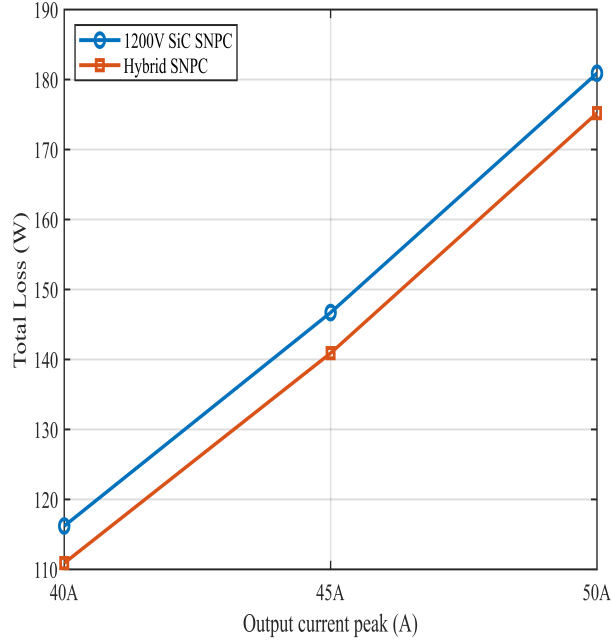


Figure 4.17: 3L-SNPC total power losses vs. peak output current at $V_{dc} = 800\text{ V}$, $P_{out} = 13.5\text{ kW}$, $f_{sw} = 10\text{ kHz}$, $T_a = 65^\circ\text{C}$

4.3.4 Loss Variation with Ambient Temperature

The effect of ambient temperature on SNPC inverter losses is shown in Figure 4.19. When the temperature increases from 45°C to 85°C , the conduction loss increases for both semiconductor configurations. This is mainly due to the temperature dependency of the semiconductor on-state resistance.

The switching loss remains almost constant with temperature for both cases. Therefore, the increase in total loss is mostly caused by the rise in conduction loss. The hybrid SNPC inverter still maintains lower switching loss than the pure SiC SNPC inverter, but its conduction loss also increases with temperature. This shows that thermal design and cooling are important for maintaining high efficiency.

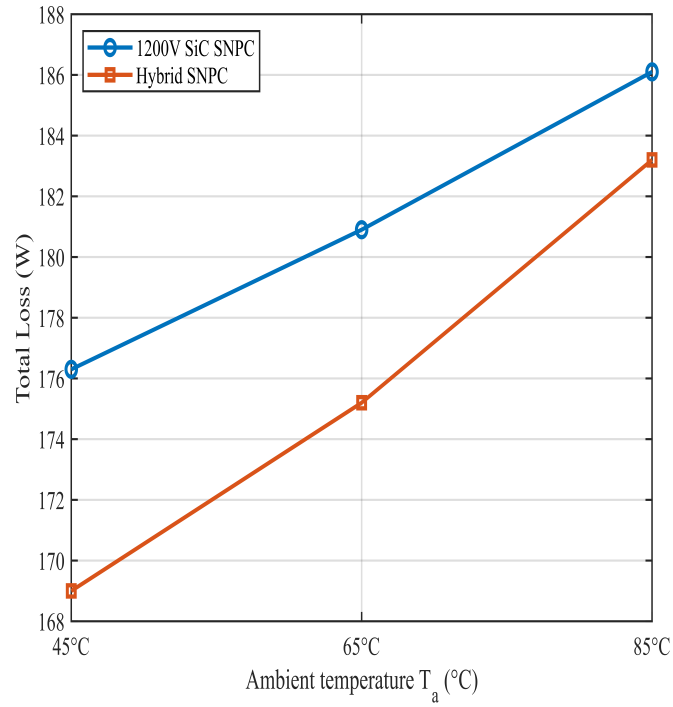


Figure 4.19: 3L-SNPC total power losses vs. ambient temperature at $V_{dc} = 800\text{ V}$, $P_{out} \approx 13.5\text{ kW}$, $f_{sw} = 10\text{ kHz}$, $I_{pk} = 50\text{ A}$

Fig. 4.20 shows the SNPC inverter efficiency as a function of ambient temperature.

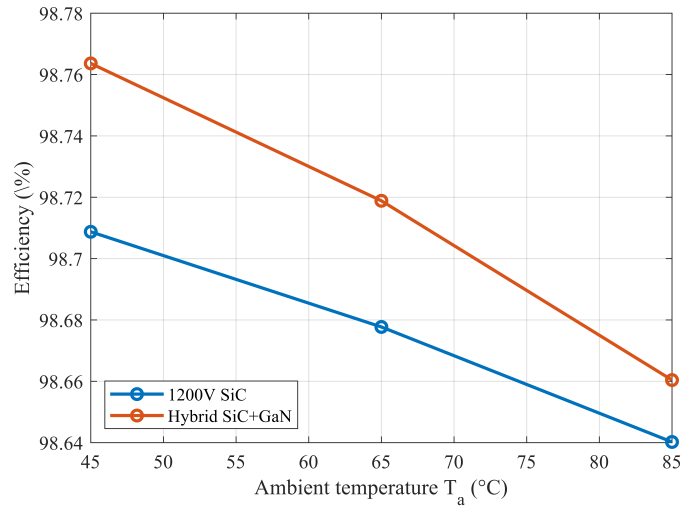


Figure 4.20: 3L-SNPC inverter efficiency vs ambient temperature ($V_{dc} = 800\text{ V}$, $I_{pk} = 50\text{ A}$, $f_{sw} = 10\text{ kHz}$)

4.3.5 Line Plot Comparison

The total loss trend was also compared using line graphs. These plots make it easier to observe the overall trend of total loss for the pure SiC and hybrid SNPC configurations. The line plots confirm that the hybrid SNPC inverter gives lower total loss, especially when the switching frequency is increased.

4.3.6 Summary

The hybrid SNPC inverter has a clear advantage in terms of switching loss reduction compared with the 1200 V SiC SNPC inverter. The hybrid SNPC configuration achieves lower total losses than the pure 1200 V SiC SNPC across all investigated switching frequencies, with the advantage growing from 5.7 W (3.2%) at 10 kHz to 65.7 W (23.7%) at 100 kHz. This confirms that hybridisation becomes increasingly beneficial at higher switching frequencies, where GaN's near-zero switching energy provides the greatest advantage over pure SiC.

4.3.7 Key Observations

Based on the SNPC simulation results, the following observations are drawn:

- With ambient temperature increasing, GaN $R_{ds(on)}$ increases more than SiC, affecting conduction loss.
- At low switching frequency (10 kHz), SiC devices exhibit lower total losses due to reduced conduction losses.
- At high switching frequencies, GaN devices outperform SiC due to lower switching losses.
- GaN losses increase slowly with frequency, while SiC losses increase rapidly.

4.4 Simulation Results and Analysis of the 3-phase T-type Inverter

The T-type inverter topology is particularly suitable for hybrid GaN–SiC implementation since the neutral-clamped inner switches only experience half of the dc-link blocking voltage compared to the outer switches. This allows lower-voltage GaN devices to be utilized in the inner switch positions, where high-frequency switching commutation mainly occurs. In addition, GaN devices are known to exhibit significantly lower switching losses than SiC devices with comparable voltage ratings.

Therefore, under the general operating conditions listed in Table 3.4, PD-PWM is adopted as the modulation strategy for all simulations. Considering the 800 V dc-link voltage and applying a safety margin of approximately 1.5 to ensure reliable device operation and lifetime performance, 1200 V SiC MOSFETs are selected for the outer switches of the T-type inverter. In contrast, the neutral-clamp inner switches only experience approximately half of the dc-link blocking voltage in the T-type topology, allowing the use of 650 V GaN GIT devices in these positions.

Based on this configuration, two inverter topologies are investigated in this study: The first configuration is a full-SiC T-type inverter employing 1200 V SiC MOSFETs in the outer switch positions and 650 V SiC MOSFETs in the neutral-clamp inner switch positions. The second configuration is a hybrid T-type inverter in which the neutral-clamp inner switches are replaced by 650 V GaN GIT devices while the outer switches remain the same 1200 V SiC MOSFETs. This arrangement enables a fair comparison between the full-SiC and hybrid SiC-GaN T-type inverter configurations under comparable voltage stress conditions. The performance of both configurations is evaluated under different operating conditions to investigate their loss distribution, efficiency, and thermal characteristics.

In this section, two groups of commercially available 650 V GaN GITs, 650 V SiC MOSFETs and 1200 V SiC MOSFETs, listed in Table 3.2 and Table 3.3, are considered. All the data are extracted from the corresponding manufacturer datasheets. The selected 650 V GaN and 650 V SiC devices are the same devices previously investigated in the 3-phase 2-level inverter study. For the T-type inverter configuration, 1200 V SiC MOSFETs are selected to satisfy the higher blocking voltage requirement of the outer switches while maintaining similar electrical characteristics to the 650 V SiC devices used in the previous study.

The datasheet parameters are extracted under the manufacturers' specified test conditions, which may include different drain-source voltages, gate-drive conditions, operating currents, and junction temperatures. Therefore, these parameters are intended for qualitative comparison only. For the selected GaN GIT devices, the switching energy values (E_{on} and E_{off}) are not explicitly provided in the datasheets. In the simulations, the manufacturer-provided PLECS semiconductor models are used, from which the switching behavior can be evaluated.

In the simulations, the initial junction temperatures of all semiconductor devices are set to 65°C. Since the initial junction temperature setting in PLECS does not affect the steady-state loss results, it only influences the transient thermal response and the required simulation time before reaching steady-state operation. All simulation results presented in this section are extracted after both the electrical and thermal simulations have reached steady-state conditions, with the semiconductor junction temperatures fully stabilized.

Group 2 is selected as the primary case study for detailed analysis, while Group 1 is used to validate the observed trends and conclusions.

4.4.1 Waveform Verification

According to the simulation operating conditions listed in Table 3.4, both full-SiC and hybrid SiC-GaN T-type inverter configurations produce the same steady-state output waveforms. The inverter-side voltage waveforms and three-phase load waveforms are shown in Fig. 4.21 and Fig. 4.22 respectively.

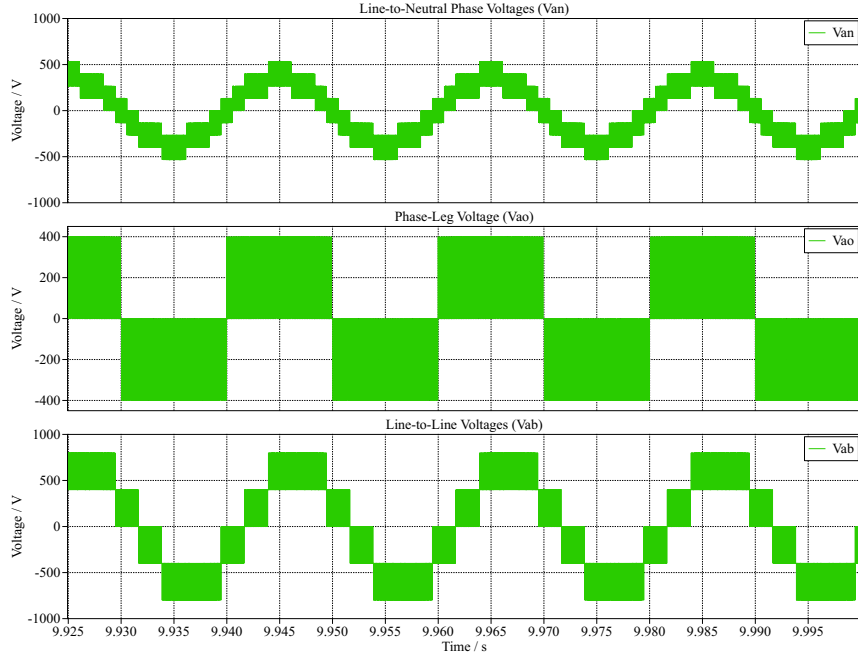


Figure 4.21: Steady-state inverter-side output waveforms of the T-type inverter at value of modulation index $M = 0.9$: (a) line-to-neutral phase voltage (V_{an}), (b) phase-leg voltage (V_{ao}), (c) line-to-line voltage (V_{ab}).

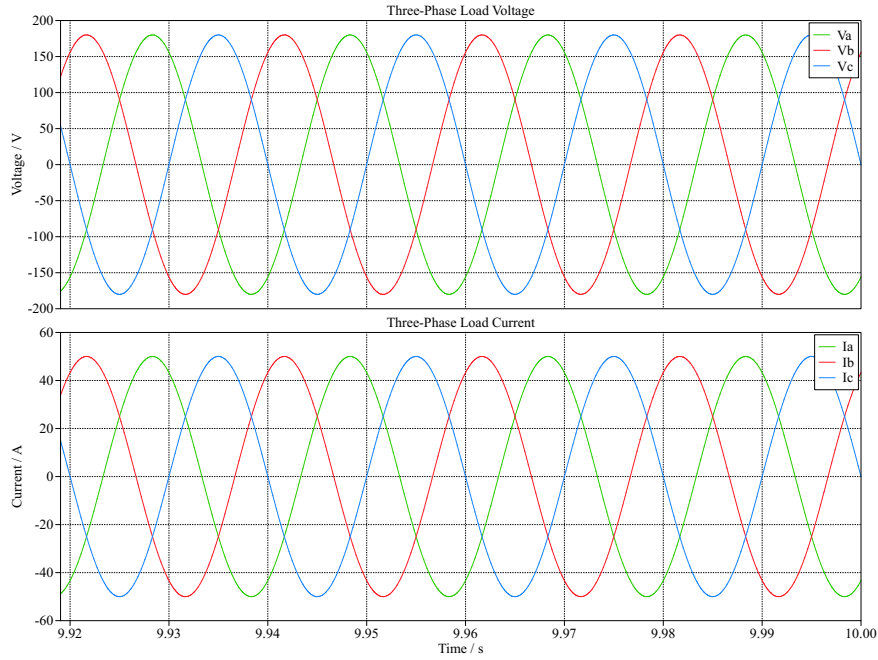


Figure 4.22: Steady-state three-phase load waveforms of the T-type inverter at value of modulation index $M = 0.9$: (a) three-phase load voltage, (b) three-phase load current.

Fig. 4.21 (a) presents the line-to-neutral phase voltage (V_{an}), which is expressed by

$$V_{an} = V_{ao} - \frac{V_{ao} + V_{bo} + V_{co}}{3} \quad (4.2)$$

has a multilevel staircase waveform. Fig. 4.21 (b) presents the phase-leg voltage (V_{ao}) as expected to switch among these three switching states.

$$V_{ao} \in \left\{ +\frac{V_{dc}}{2}, 0, -\frac{V_{dc}}{2} \right\} = \{+400 \text{ V}, 0 \text{ V}, -400 \text{ V}\} \quad (4.3)$$

This confirms the correct implementation of the T-type inverter topology and the PD-PWM control strategy. Consequently, Fig. 4.21 (c) line-to-line voltage (V_{ab}) exhibits the expected five-level waveform with voltage levels of +800 V, +400 V, 0 V, -400 V, and -800 V [18].

Fig. 4.22(a) shows the steady-state three-phase load voltages after the output filter, with a phase displacement of 120° between phases. The voltages are measured across the load resistance. Based on the specified power factor angle and the calculated load parameters presented in Section 3.2.1, the expected peak voltage across the load resistance is approximately 180 V. The simulated waveform agrees well with this calculated value. Fig. 4.22 (b) shows the steady-state three-phase load currents, which are also displaced by 120° between phases. The measured peak phase current is approximately 50 A, which agrees with the operating conditions specified in Table 3.4.

Therefore, both the inverter-side voltage waveforms and three-phase load waveforms verify the correct steady-state operation of the proposed T-type inverter under the operating conditions listed in Table 3.4. The simulation model is considered valid for the subsequent loss and thermal performance evaluation.

Two groups of components exhibit the same trends and similar simulation results; therefore, only the results of group 2 are presented in the following sections as a representative example. The comparison indicates that the different package types considered in this study have a negligible impact on the simulated thermal performance of the devices.

4.4.2 Effect of Switching Frequency

To verify the hypothesis that GaN GITs have significantly lower turn-on and turn-off switching energies compare to SiC MOSFETs with similar ratings, which leads to reduced switching-loss sensitivity with increasing switching frequencies. This section investigated that the proposed hybrid SiC–GaN T-type inverter improves performance with switching frequency increasing.

To evaluate the effect of switching frequency, the switching frequency is varied among 10 kHz, 20 kHz, 50 kHz and 100 kHz, while the dc-link voltage, output current, ambient temperature, and gate resistance are maintained constant at the nominal operating conditions listed in Table 3.4.

4.4.2.1 Simulation Results with Group 2 Devices

Fig. 4.23 shows the conduction loss, switching loss and total loss distribution of the full-SiC and hybrid SiC–GaN T-type inverters. Since the inner switches S_2 and S_3 in the hybrid SiC–GaN configuration are replaced by 650 V GaN GIT devices, which have negligible turn-on and turn-off switching energy, the switching losses of the hybrid configuration increase more slowly with switching frequency compared with the full-SiC configuration. However, the conduction losses of the hybrid configuration remain consistently higher over the entire

switching frequency range, and the reduction from hybrid switching losses is not enough to offset the higher conduction losses under the investigated switching frequency range. Consequently, the hybrid configuration exhibits higher total losses than the full-SiC configuration from 10 kHz to 100 kHz.

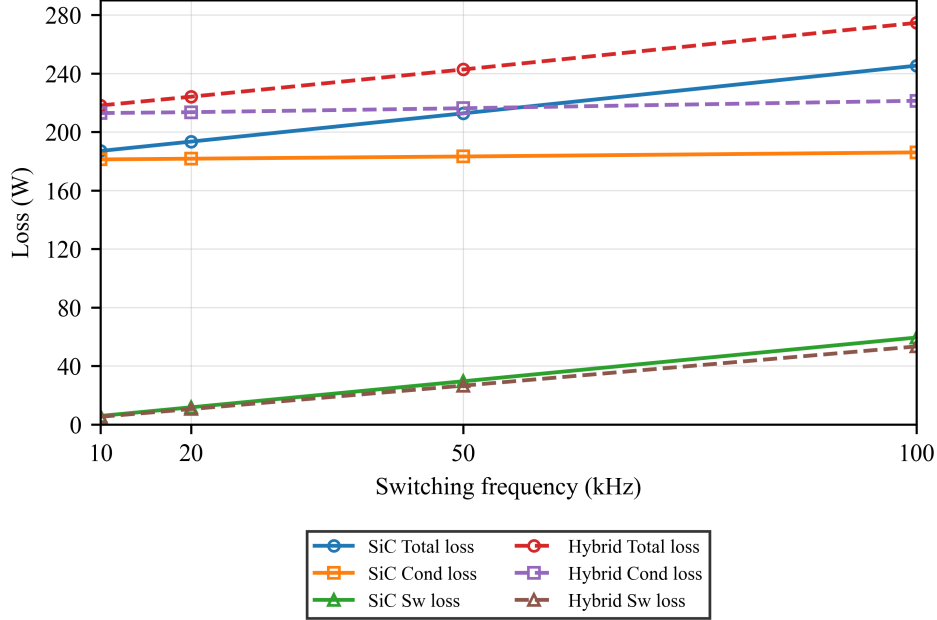


Figure 4.23: Loss distribution under different switching frequency, for $V_{dc} = 800$ V, $I_{pk} = 50$ A, $T_a = 65$ °C and varying of $f_{sw} = 10$ kHz, $f_{sw} = 20$ kHz, $f_{sw} = 50$ kHz and $f_{sw} = 100$ kHz

Fig. 4.24 shows the conduction loss, switching loss and total loss distribution of the outer switches S_{A1}/S_{A4} in the full-SiC and hybrid SiC–GaN configurations. Due to the symmetry of the topology and configuration, the loss distributions of S_{A1} and S_{A4} can be considered the same. Since the outer switches S_{A1} and S_{A4} employ the same 1200 V SiC MOSFETs in both configurations, the conduction losses remain almost constant, while the switching losses increase with switching frequency, resulting in similar total losses for both configurations.

Fig. 4.25 shows the conduction loss, switching loss and total loss distribution of the inner switches S_{A2}/S_{A3} in the full-SiC and hybrid SiC–GaN configurations. It can be observed that the conduction losses of S_{A2}/S_{A3} are significantly higher than those of S_{A1}/S_{A4} . This is mainly caused by the control strategy of the T-type inverter, where the inner switches S_{A2}/S_{A3} experience frequent current commutations and conduct a substantial portion of the load current during the zero-voltage states generated by the PD-PWM modulation strategy.

In addition, the employed Infineon GaN GIT devices exhibit a strong increase in on-state resistance with increasing drain current and junction temperature, whereas the on-state resistance of the Wolfspeed SiC MOSFET devices is less sensitive to current and temperature variations under the investigated operating conditions. Consequently, the conduction losses of the GaN GIT devices at the S_{A2}/S_{A3} positions are significantly higher than those of the corresponding SiC MOSFET devices.

Fig. 4.26 shows the efficiency of the comparison of full-SiC and hybrid SiC–GaN. The full-SiC configuration achieves higher overall efficiency than the hybrid SiC–GaN configuration

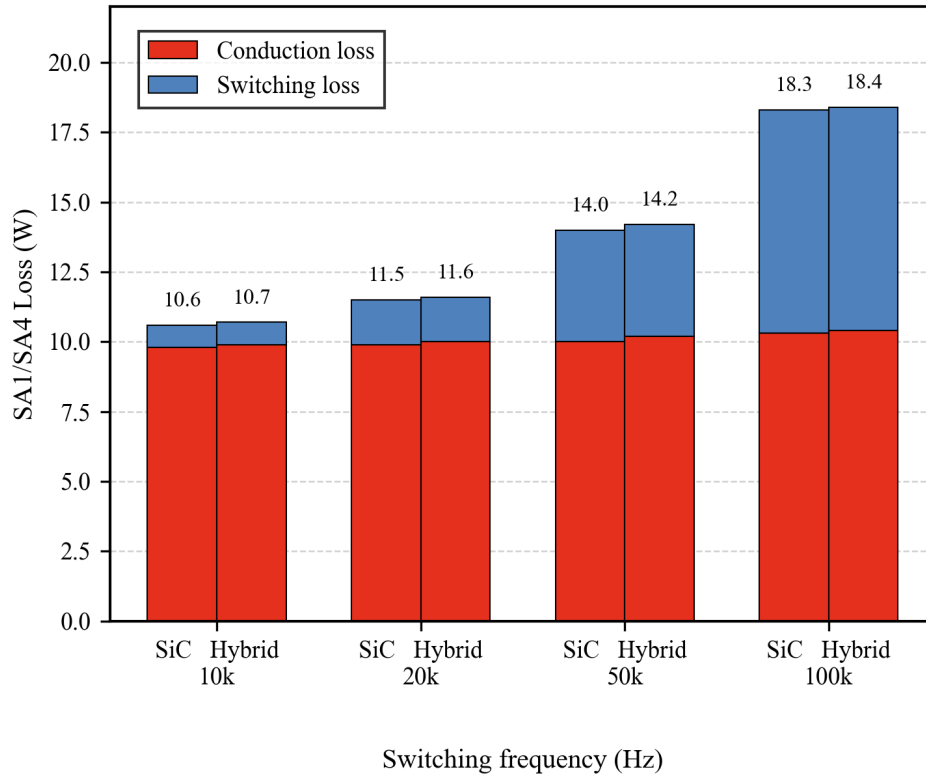


Figure 4.24: S_{A1}/S_{A4} Loss distribution under different switching frequency

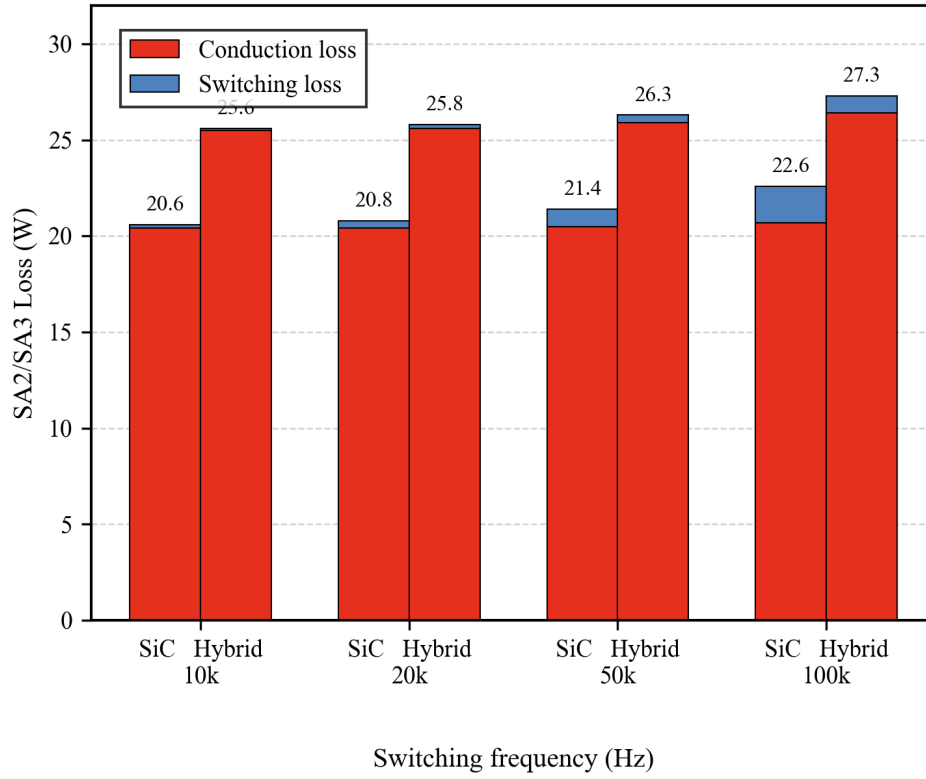


Figure 4.25: S_{A2}/S_{A3} Loss distribution under different switching frequency

throughout the investigated switching-frequency range.

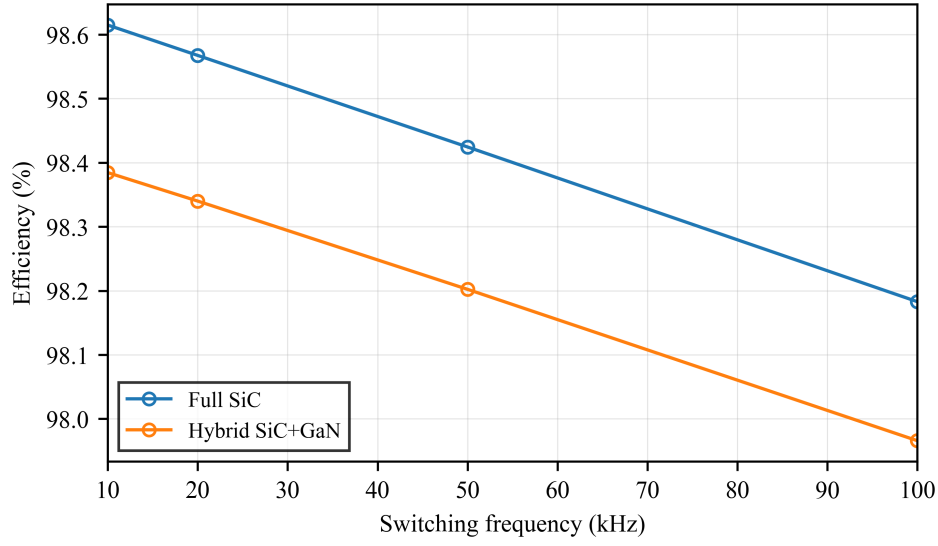


Figure 4.26: Efficiency under different switching frequency

4.4.3 Effect of Output Current

For the intended EV traction application considered in this work, the loss performance under high output current conditions is of particular interest. In practical electric vehicle applications, the inverter output current can reach several hundreds of amperes. However, due to the currently limited current ratings of commercially available GaN GIT devices, the selected Infineon GaN GIT used in this study has a maximum current rating of approximately 70 A.

In practical high-power converter implementations, parallel connection of semiconductor devices is commonly adopted to satisfy the high current requirements of EV traction systems. Therefore, multiple devices can be connected in parallel to achieve the required output current capability. Since the objective of this study is to comparatively evaluate the switching and conduction characteristics of the semiconductor devices and inverter topologies, the simulation is performed based on the electrical and thermal behavior of a single device unit, which is considered representative for the parallel-connected implementation.

To evaluate the effect of output current, the output current is varied among 40 A, 45 A and 50 A, while the dc-link voltage, switching frequency, ambient temperature, and gate resistance are maintained constant at the nominal operating conditions listed in Table 3.4.

4.4.3.1 Simulation Results with Group 2 Devices

Fig. 4.27 shows the conduction loss, switching loss and total loss distribution of the full-SiC and hybrid SiC–GaN T-type inverters. The switching losses of both configurations remain relatively constant with the peak phase current increasing, since the switching frequency is fixed. The conduction losses increase significantly with the peak phase current increasing, and the hybrid configuration has consistently higher conduction losses than full-SiC configuration, resulting in higher total losses over the investigated peak phase current range.

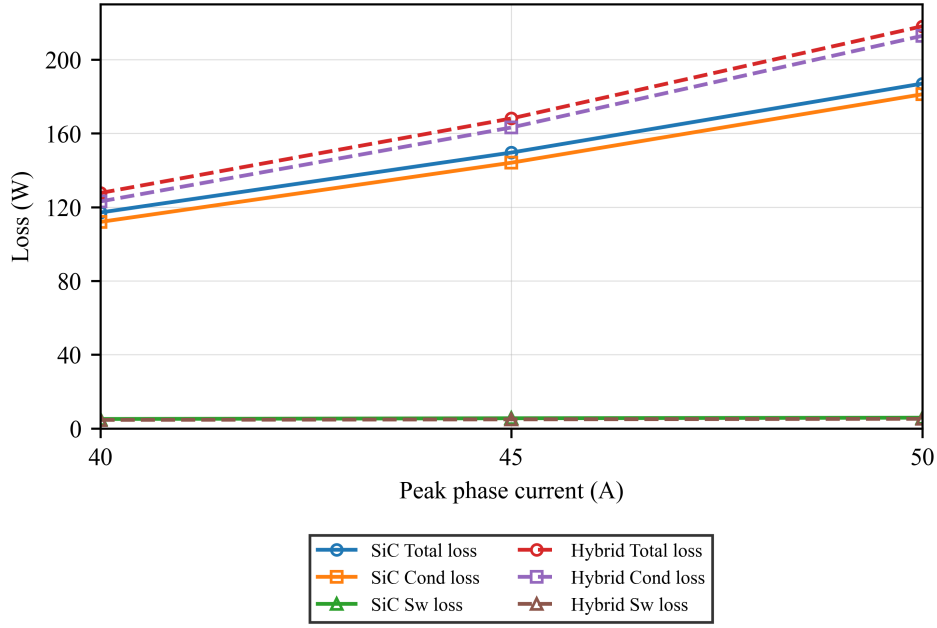


Figure 4.27: Loss distribution under different peak phase current, for $V_{dc} = 800$ V, $f_{sw} = 10$ kHz, $T_a = 65$ °C and varying of $I_{pk} = 40$ A, $I_{pk} = 45$ A and $I_{pk} = 50$ A

Fig. 4.28 shows the conduction loss, switching loss and total loss distribution of the outer switches S_{A1}/S_{A4} in the full-SiC and hybrid SiC-GaN configurations. When the peak phase current increases, the conduction losses increase, while the switching losses remain nearly constant, resulting in similar total losses increasing for both configurations.

Fig. 4.29 shows the conduction loss, switching loss and total loss distribution of the inner switches S_{A2}/S_{A3} in the full-SiC and hybrid SiC-GaN configurations. The conduction losses contribute most for the total losses and increase with current increasing. Hybrid configurations always has higher conduction losses than full-SiC configuration over the entire current range. This is resulted from the on-state resistance of the selected GaN GIT has stronger dependence on drain current and junction temperature, the on-state resistance gets bigger under higher current.

Fig. 4.30 shows the efficiency of the comparison of full-SiC and hybrid SiC-GaN. The efficiency of hybrid configuration decreases faster than full-SiC configuration with current increasing, this is due to the significant conduction losses increasing from inner switches S_{A2}/S_{A3} in hybrid configuration.

All these results indicate that, under the investigated current range, conduction losses dominate the overall inverter performance.

4.4.4 Effect of Ambient Temperature

From the semiconductor device datasheets and the simulation results of the previously investigated 3-phase 2-level inverter, it is observed that the drain-source on-state resistance increases with increasing junction temperature, resulting in increased conduction losses. Therefore, this section further investigates and validates the influence of ambient temperature on the loss performance of the 3-phase 3-level T-type inverter.

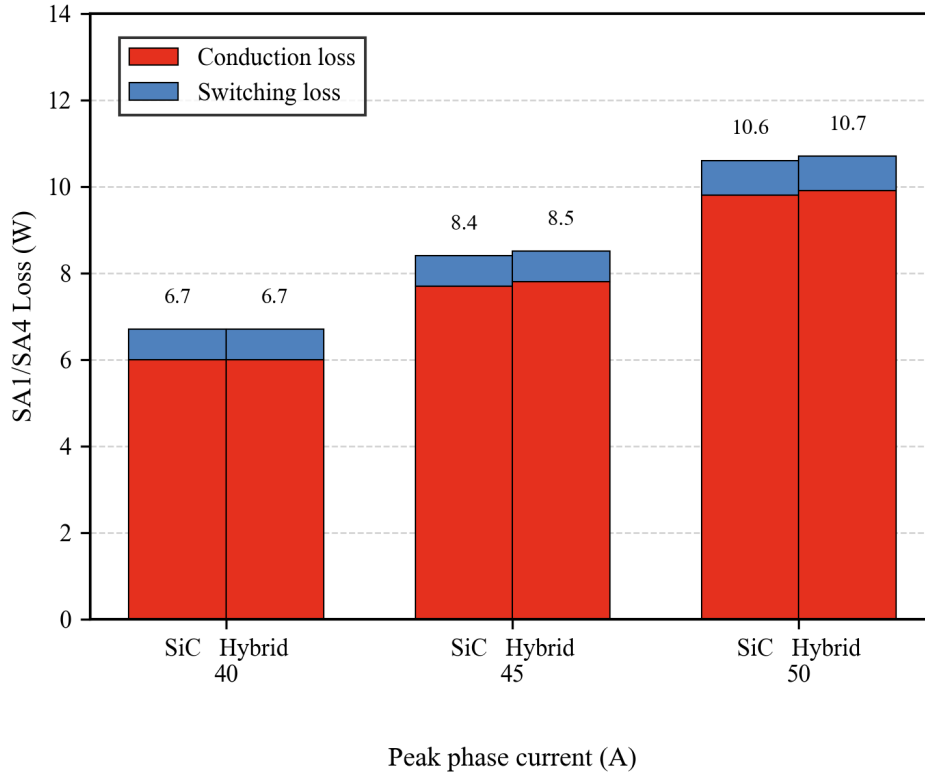


Figure 4.28: S_{A1}/S_{A4} Loss distribution under different peak phase current

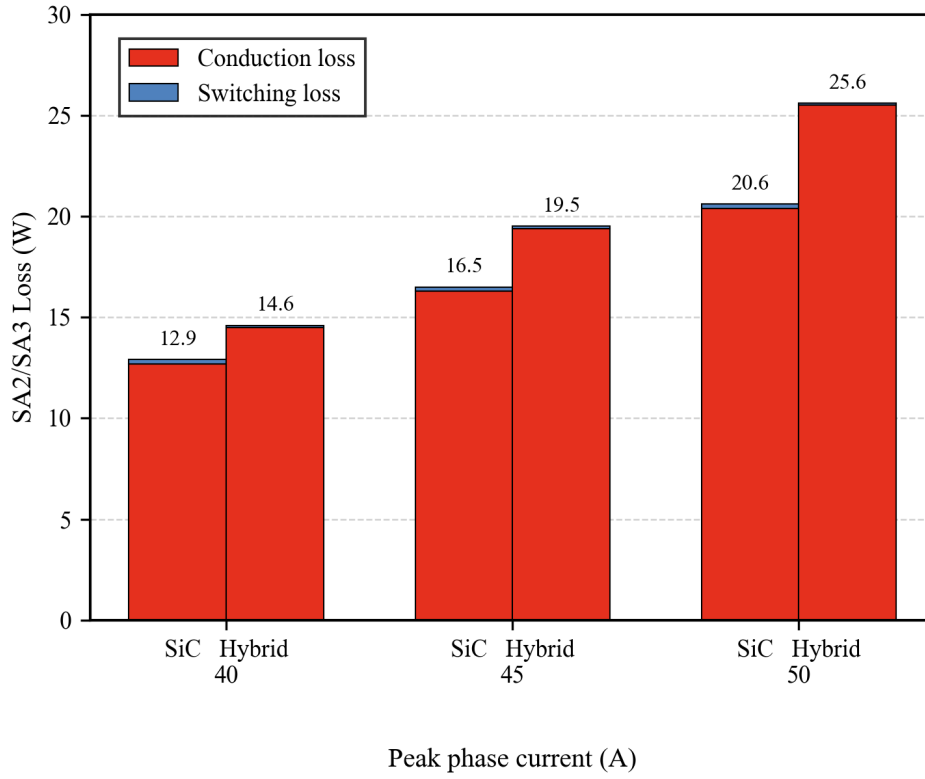


Figure 4.29: S_{A2}/S_{A3} Loss distribution under different peak phase current

To evaluate the effect of ambient temperature, the ambient temperature is varied among 45°C, 65°C and 85°C, while the dc-link voltage, switching frequency, output current, and gate resistance are maintained constant at the nominal operating conditions listed in Table 3.4.

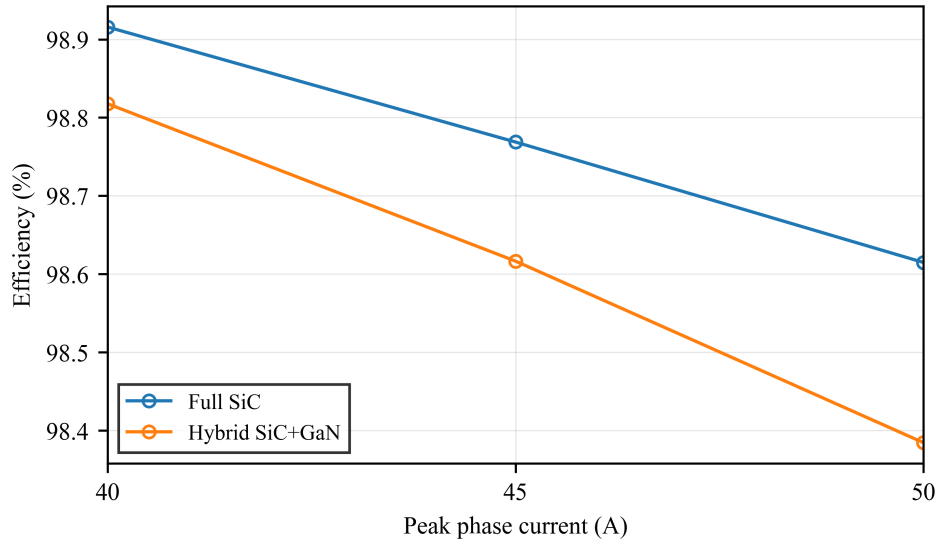


Figure 4.30: Efficiency under different peak phase current

4.4.4.1 Simulation Results with Group 2 Devices

Fig. 4.31 shows the conduction loss, switching loss and total loss distribution of the full-SiC and hybrid SiC–GaN T-type inverters. Similar to the results with current changing, the conduction losses increase and the switching losses remain nearly constant with the ambient temperature increasing. The hybrid configuration gets higher total losses than the full-SiC configuration across the investigated temperature range.

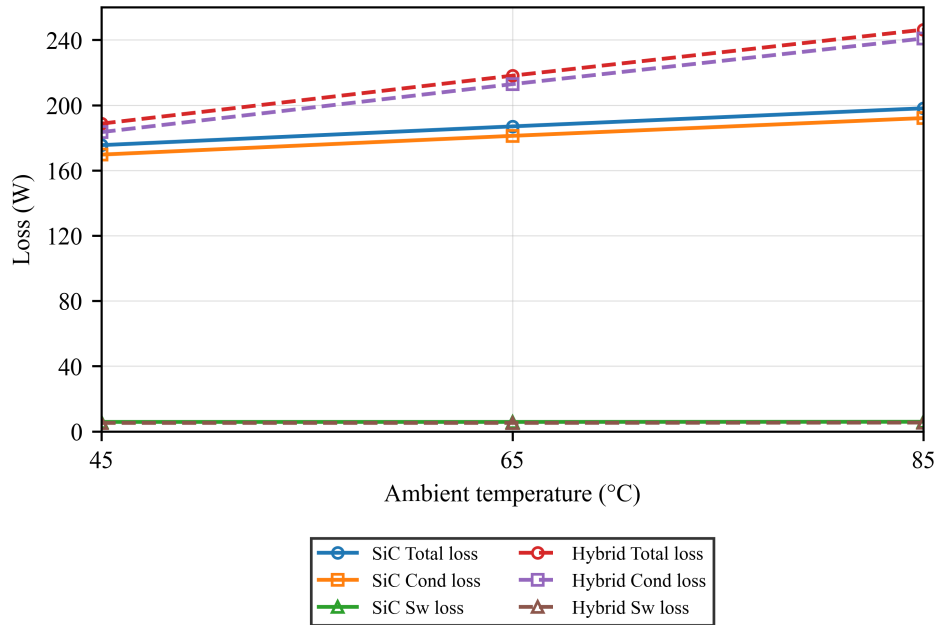


Figure 4.31: Loss distribution under different ambient temperature, for $V_{dc} = 800$ V, $I_{pk} = 50$ A, $f_{sw} = 10$ kHz and varying of $T_a = 45$ °C, $T_a = 65$ °C and $T_a = 85$ °C

Fig. 4.32 and Fig. 4.33 show the conduction loss, switching loss and total loss distribution of the outer switches S_{A1}/S_{A4} and the inner switches S_{A2}/S_{A3} in the full-SiC and hybrid SiC–GaN configurations. The losses distribution behaves similarly to the results with the current changes.

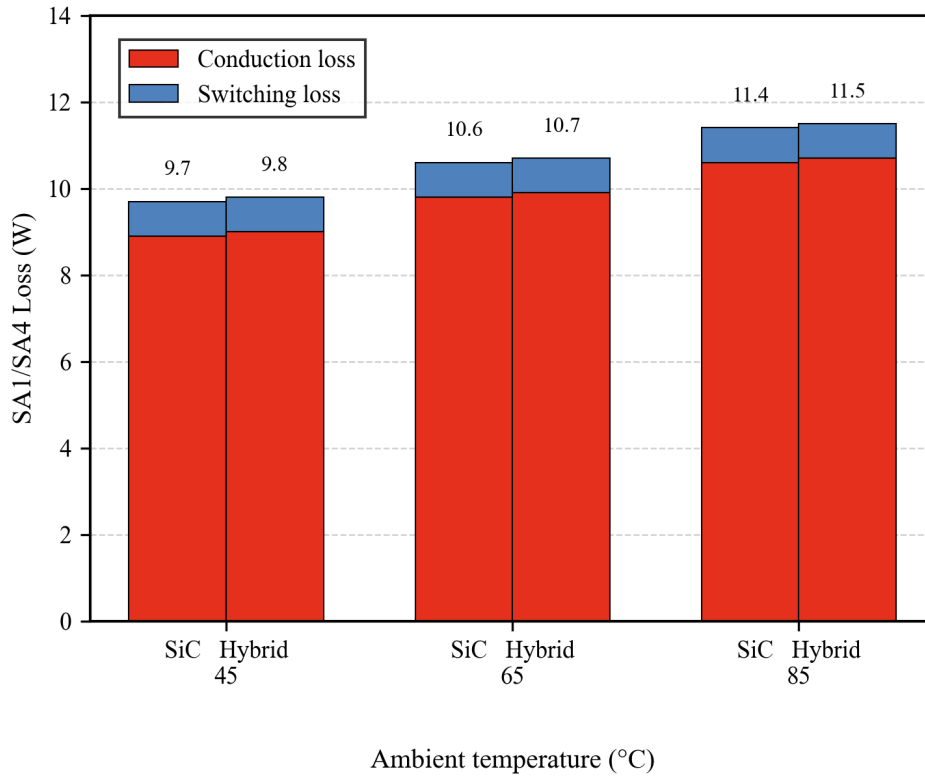


Figure 4.32: S_{A1}/S_{A4} Loss distribution under different ambient temperature

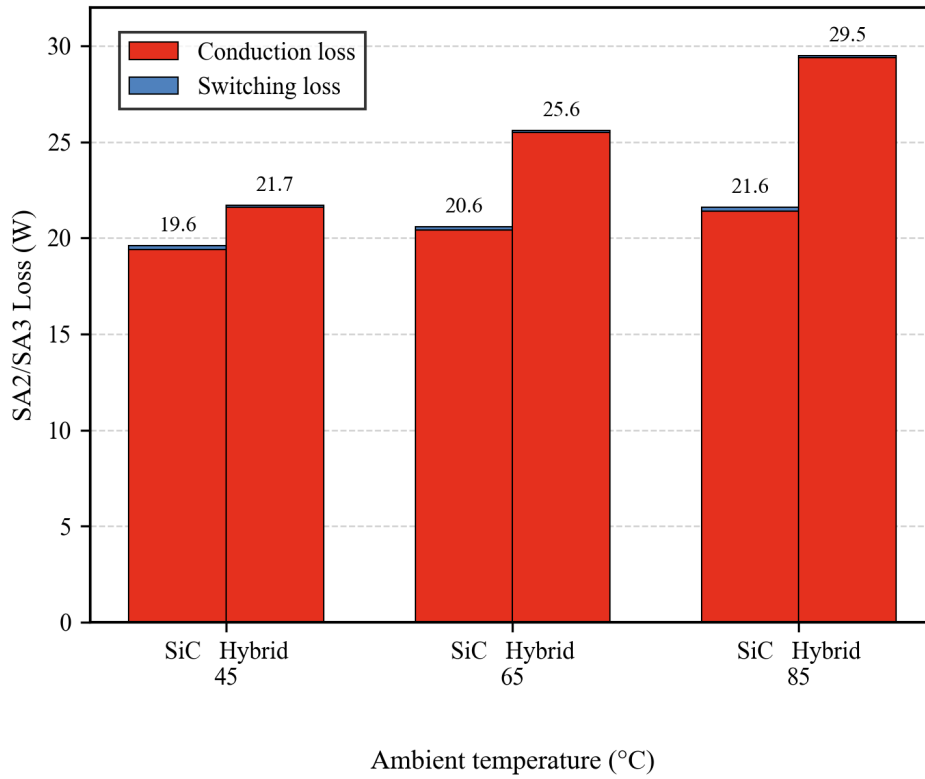


Figure 4.33: S_{A2}/S_{A3} Loss distribution under different ambient temperature

Fig. 4.34 shows the efficiency of the comparison of full-SiC and hybrid SiC-GaN. The efficiency of hybrid configuration decreases faster than full-SiC which can take the analysis from efficiencies with current changing as reference.

At higher ambient temperatures, conduction losses become dominant, reducing the relative

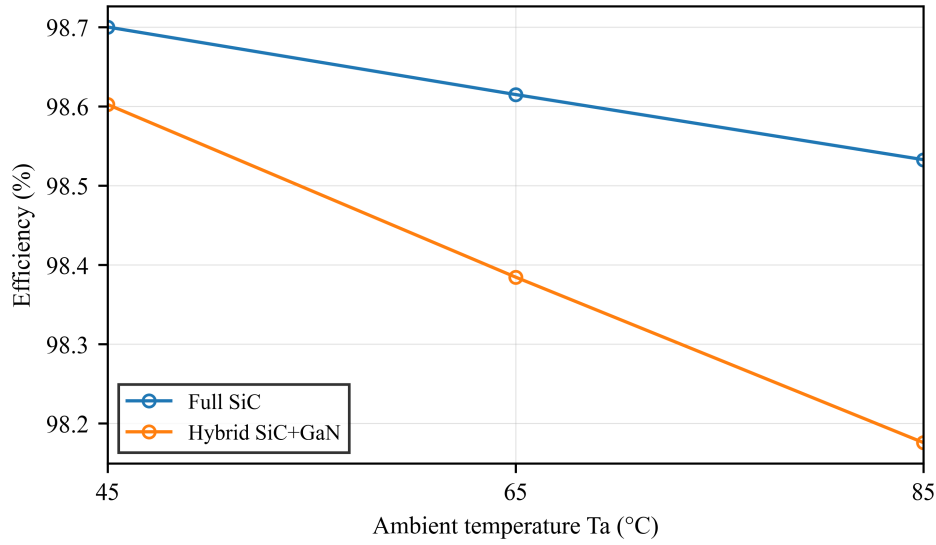


Figure 4.34: Efficiency under different ambient temperature

benefit of the lower switching losses provided by the GaN devices. The obtained results indicate that the performance advantage of hybrid GaN–SiC T-type inverters strongly depends on the balance between switching-loss reduction and conduction-loss increase. Under the investigated operating conditions, the temperature-dependent conduction characteristics of the employed GaN GIT devices dominate the overall loss performance, limiting the achievable efficiency improvement of the hybrid configuration.

4.5 Discussion

This section brings together the simulation results from all four inverter topologies to provide a unified comparison of efficiency performance across the three parametric sweeps. The goal is to identify which combination of topology and device configuration delivers the best overall performance under the investigated operating conditions.

4.5.1 Efficiency Comparison in Different Topologies

Table 4.2 compares the efficiency of all configurations across switching frequencies from 10 kHz to 100 kHz. At 10 kHz, the 3L-SNPC hybrid SiC–GaN achieves the highest efficiency of 98.73%, followed by the pure SiC SNPC at 98.68%. Among the ANPC configurations, the 650 V SiC achieves the best result at 98.39%.

Table 4.2: Efficiency comparison at different switching frequencies ($V_{dc} = 800$ V, $I_{pk} = 50$ A, $T_a = 65$ °C)

Topology	Configuration	η at 10 kHz (%)	η at 50 kHz (%)	η at 100 kHz (%)
3L-ANPC	650 V SiC	98.39	98.24	98.07
	1200 V SiC	98.22	98.01	97.80
	GaN	98.21	98.18	98.14
	650 V SiC+GaN	98.30	98.27	98.24
	1200 V SiC+GaN	98.25	98.22	98.19
3L-SNPC	1200 V SiC	98.68	98.39	97.99
	Hybrid SiC+GaN	98.73	98.62	98.47
3L-T-type	1200 V SiC+650 V SiC	98.67	98.47	98.23
	1200 V SiC+650 V GaN	98.39	98.21	97.97

As switching frequency increases, the efficiency gap between topologies widens significantly. The pure SiC configurations suffer the greatest degradation, the 1200 V SiC ANPC drops to 97.80% at 100 kHz, while the hybrid configurations maintain considerably higher efficiency. The SNPC hybrid retains 98.47% at 100 kHz, and the ANPC 650 V SiC+GaN hybrid achieves 98.24%. This confirms that GaN-SiC hybridisation is most beneficial at high switching frequencies, where GaN's near-zero switching energy provides the greatest advantage. Table 4.3 compares efficiency across output current levels from 40 A to 50 A at a fixed switching frequency of 10 kHz. All configurations show decreasing efficiency with increasing current, as conduction losses rise with the square of current. The 3L-SNPC hybrid achieves the highest efficiency at all current levels, reaching 99.20% at 40 A and 98.73% at 50 A.

Table 4.3: Efficiency comparison at different output currents ($V_{dc} = 800$ V, $f_{sw} = 10$ kHz, $T_a = 65$ °C)

Topology	Configuration	η at 40 A (%)	η at 45 A (%)	η at 50 A (%)
3L-ANPC	650 V SiC	98.97	98.71	98.39
	1200 V SiC	98.86	98.57	98.22
	GaN	98.89	98.58	98.21
	650 V SiC+GaN	98.95	98.66	98.30
	1200 V SiC+GaN	98.91	98.62	98.25
3L-SNPC	1200 V SiC	99.15	98.94	98.68
	Hybrid SiC+GaN	99.20	98.98	98.73
3L-T-type	1200 V SiC+650 V SiC	98.95	98.81	98.67
	1200 V SiC+650 V GaN	98.82	98.62	98.39

Among the ANPC configurations, the 650 V SiC achieves the best efficiency at all current levels, while the all GaN configuration shows the steepest efficiency drop with increasing current, falling from 98.89% at 40 A to 98.21% at 50 A. This reflects the strong current dependence of $R_{DS(on)}$ in GaN GIT devices, which causes conduction losses to rise rapidly at high current levels. The SNPC topology maintains a consistent advantage over the ANPC across the full current range, with the hybrid SNPC always achieving the lowest total losses. Table 4.4 compares efficiency across ambient temperatures from 45 °C to 85 °C at the reference operating point. The SNPC hybrid again achieves the highest efficiency across the full temperature range, varying from 98.77% at 45 °C to 98.68% at 85 °C — a drop of only 0.09 percentage points.

Table 4.4: Efficiency comparison at different ambient temperatures ($V_{dc} = 800$ V, $I_{pk} = 50$ A, $f_{sw} = 10$ kHz)

Topology	Configuration	η at 45 °C (%)	η at 65 °C (%)	η at 85 °C (%)
3L-ANPC	650 V SiC	98.47	98.39	98.32
	1200 V SiC	98.36	98.22	98.05
	GaN	98.43	98.21	97.96
	650 V SiC+GaN	98.46	98.30	98.13
	1200 V SiC+GaN	98.43	98.25	98.05
3L-SNPC	1200 V SiC	98.72	98.68	98.65
	Hybrid SiC+GaN	98.77	98.73	98.68
3L-T-type	1200 V SiC+650 V SiC	98.75	98.67	98.59
	1200 V SiC+650 V GaN	98.60	98.39	98.18

The all-GaN ANPC shows the greatest temperature sensitivity, dropping from 98.43% at 45 °C to 97.96% at 85 °C a reduction of 0.47 percentage points. This is attributable to the strong temperature dependence of $R_{DS(on)}$ in selected GaN GIT devices. The SNPC configurations, by contrast, show the smallest efficiency variation with temperature, confirming their superior thermal robustness, a particularly important advantage for automotive applications where ambient temperature varies significantly across geographic regions and drive cycles.

5

Conclusion

5.1 Summary of Work

This thesis started with a practical question from an automotive industry partner: given the wide-bandgap semiconductor devices now commercially available, which combination of inverter topology and device technology actually delivers the best loss performance under real operating conditions. The answer, it turns out, is not as simple as picking the best device—it depends entirely on where that device sits within the topology, and how the modulation strategy assigns switching duties.

Four topologies were investigated through PLECS simulation as part of this collaborative study: the 3L-ANPC, the 3L-SNPC, the three-level T-type inverter, and the conventional two-level inverter as a reference baseline. All topologies were evaluated across switching frequency (10–100 kHz), peak output current (40–50 A), and ambient temperature (45–85 °C) a range deliberately chosen to reflect real automotive operating conditions rather than a single optimistic datasheet point.

5.2 Key Findings

5.2.1 3L-ANPC Inverter

The ANPC results tell a consistent story. The 650 V SiC configuration achieves the lowest total losses at low switching frequencies (220 W at 10 kHz), but its losses climb steadily with frequency, reaching 266 W at 100 kHz. The 1200 V SiC configuration carries a heavier conduction loss burden from the start (246.8 W at 10 kHz) and ends up as the worst performer at high frequency, reaching 308.4 W at 100 kHz. The all-GaN configuration produces the flattest loss curve of any ANPC option losses rise by barely 11 W across the full 10–100 kHz range (247.1 W to 258 W) but its high conduction losses mean it never achieves the lowest total losses at any frequency tested.

The hybrid configurations are where the real engineering insight lies. By placing GaN only in Cell 2 the position that carries all high-frequency switching under PWM-2, the 650 V SiC+GaN hybrid captures the switching efficiency of GaN while keeping SiC’s lower conduction losses everywhere else. The result is a nearly flat total loss profile, rising from only 233.5 W at 10 kHz to 244.9 W at 100 kHz an increase of just 11.4 W across the full frequency range. Above 50 kHz, it becomes the second-best ANPC option after the 650 V pure SiC configuration. The 1200 V SiC+GaN hybrid follows a similar trend, achieving 240.8 W at 10 kHz and 252.2 W at 100 kHz. For applications that need to operate efficiently across a wide frequency range, the hybrid configuration is the preferred choice.

5.2.2 3L-SNPC Inverter

The SNPC results are arguably the most significant finding of this thesis. At the reference operating point, the pure 1200 V SiC SNPC achieves 180.9 W total losses -18% lower than the best ANPC configuration without any hybrid device strategy. That advantage comes purely from the topology itself: the SM stage devices only block $V_{dc}/2$, which means lower-voltage devices with lower on-state resistance handle the switching events, and the overall conduction losses are structurally lower as a result.

The frequency sweep reveals an important limitation of pure SiC in the SNPC. Switching losses increase tenfold between 10 kHz and 100 kHz—from 10.6 W to 106.3 W—effectively eroding the topology’s structural efficiency advantage at high frequency. The Hybrid GaN-SiC SNPC resolves this directly: switching losses fall to 4.1 W at 10 kHz and only 41.1 W at 100 kHz, a 61% reduction relative to pure SiC at 100 kHz, while conduction losses remain virtually unchanged. The total loss saving from hybridisation grows from 5.7 W at 10 kHz to 65.7 W at 100 kHz. Both SNPC configurations show the lowest thermal sensitivity of any topology investigated in this work—the hybrid increases by only 14.3 W across the full 45–85 °C range, compared with 67.9 W for the all-GaN ANPC.

5.2.3 3L T-Type Inverter

The simulation results of the 3L T-type inverter demonstrate that, although the GaN GIT devices provide a switching-loss advantage in the hybrid configuration, the overall loss performance depends on whether this reduction is sufficient to compensate for the dominant conduction losses. This trade-off is strongly influenced by the topology operating principle, device placement, and operating conditions. In addition, the thermal characteristics of the semiconductor devices significantly affect their loss behavior, particularly the sensitivity of the on-state resistance to drain current and junction temperature.

5.2.4 Two-Level Inverter

The 2L inverter establishes a clear and quantitative crossover between GaN and SiC at approximately 70 kHz. Below this frequency, SiC achieves lower total losses because its conduction performance is superior. Above it, GaN pulls ahead because its switching energy losses grow so slowly with frequency. The current sweep delivers the starkest single result in the entire study: at 50 A, GaN total losses in the 2L topology reach 437.8 W compared with 257.2 W for SiC a difference of 180 W from conduction losses alone. This makes unmistakably clear that GaN’s value depends entirely on keeping it away from high-current positions.

5.3 Limitations and Future Work

The results of this study are based on PLECS simulation using device loss models from manufacturer datasheets. Physical hardware introduces parasitic elements, gate driver non-idealities, and layout-dependent effects that simulation cannot fully capture. The quantitative numbers are specific to the devices modelled; trends and relative comparisons are expected to be broadly valid. All results are per-phase and at a fixed modulation index three-phase interactions, neutral-point balancing, and modulation index variation are not addressed here.

The natural next steps are experimental validation on physical hardware, extension to a complete four-way topology comparison including the T-type, and investigation of the PWM-3 modulation strategy [7] with hybrid device configurations. Extending the frequency sweep beyond 100 kHz would be particularly valuable for GaN-based configurations, where the full switching advantage has not yet been reached within the range investigated here. Also, there are new GaN GITs with higher voltage rating published by Infineon, which should be tested to prove GaN devices' benefit.

5.4 Sustainability and Ethics

The IEEE Code of Conduct outlines ten key ethical responsibilities for engineers. During this project, we were committed to complying with these ethical principles and ensuring that all work was conducted in a professional, responsible, and ethical manner. All the results and analyses respect the truth.

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Appendix 1



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