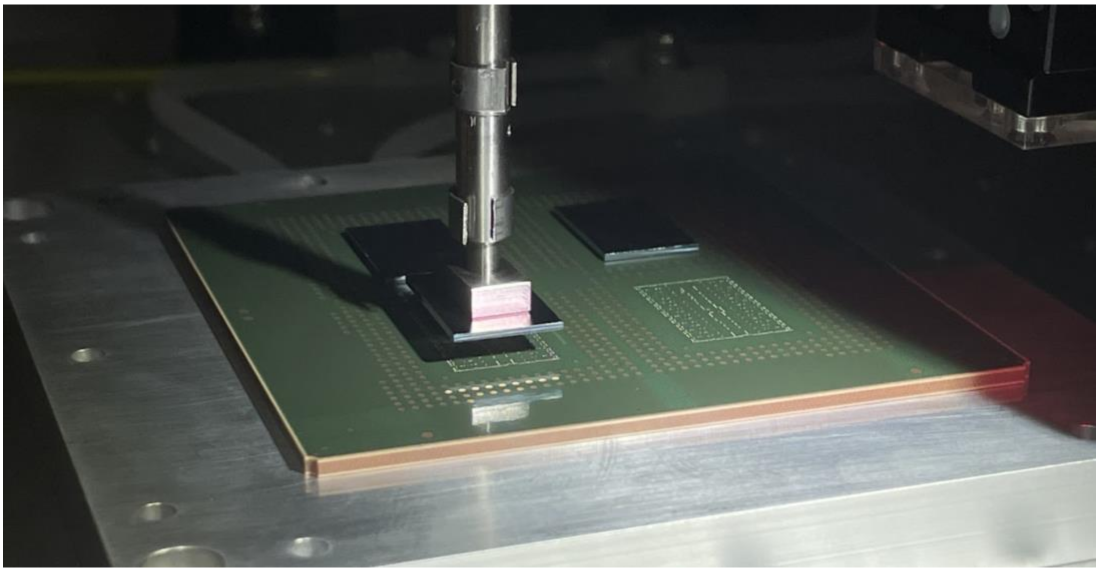

Flip-chip Assembly and Reliability Testing

An experimental study comparing two techniques for attaching microchips: Reliability and mechanical stability over time.

Bachelor thesis in mechanical engineering

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CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2025
www.chalmers.se

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Cover: Flip chip assembly using Tresky-5300.

Department of Industrial and Materials Science
Gothenburg, Sweden 2025

Preface

This bachelor's thesis was carried out during the spring term of 2025 at Chalmers University of Technology, as part of the course IMSX20 within the Mechanical Engineering program. The project was conducted in Borås in collaboration with Ericsson.

We would like to express our sincere gratitude to Ericsson for the opportunity to conduct this thesis in cooperation with your organization. Special thanks to Tony Josefsson, our external supervisor, and the rest of the team in the cleanroom for their valuable insights and continuous support throughout the project.

We also wish to thank our examiner and supervisor at Chalmers, Peter Hammerberg, for his guidance and support during the course of this work.

– Axel Krusten & Alex Olsson, Gothenburg, May 2025

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ABSTRACT
This thesis investigates the assembly and reliability processes of two different flip chip technologies, C4 solder bumps and gold stud bumps. The thesis mainly focuses on how underfill affects the mechanical and electrical reliability of the flip chip assemblies when going through temperature cycling. The reliability of the assemblies were tested using various methods such as measuring resistance, performing shear tests and cross sections.

The result of the project clearly shows that underfill significantly improves both mechanical and electrical reliability. This was especially clear on the C4 chips were the ones with underfill seemed almost unaffected by the temperature cycling while the chips without underfill deteriorated significantly over time. For the Au stud bumps assemblies, problems with underfill application were observed, mainly because of low standoff height. Even though there were challenges the underfill still improved the mechanical reliability of the Au stud bump assemblies. The thesis concludes that the underfill process is crucial to achieve reliable flip chip assemblies and recommends further improvements of the assembly processes to reduce defects.

The report is written in English.

Keywords: Microelectronic packaging, Flip Chip technology, C4 interconnects, Au stud bumps, Underfill, Temperature cycling, shear testing, reliability analysis

Dictionary

- Flip-Chip: A method where a microchip is flipped upside down and connected directly to the substrate using bumps instead of wires.
- Stand-off: The length between the chip and the substrate
- C4 (Controlled Collapse Chip Connection): A flip-chip technology using solder balls to create connections between the chip and substrate.
- Au Stud Bumps: Gold-based micro-bumps formed using wire bonding to connect a chip to a substrate.
- Die: A small block of semiconducting material on which a circuit is fabricated (a microchip).
- Pitch: The distance between the centers of two adjacent solder bumps or gold studs.
- Underfill: An epoxy material applied between the chip and substrate to increase mechanical strength and reliability.
- Voids: Air pockets or unfilled areas in the underfill or solder, which can weaken the structure.
- Substrate: The base layer onto which microchips are mounted; it provides mechanical support and electrical connections.
- Capillary force: Capillary force is the movement of liquid within narrow spaces without external assistance, caused by the combination of surface tension and adhesive forces between the liquid and surrounding surfaces.

Table of contents

1. Introduction

In this project, assembly trials using different flip-chip processes are performed. On half of the samples, an epoxy underfill is applied between the die and the substrate to reduce wear on the interconnections. The reliability of the assemblies is then evaluated using temperature cycling. The focus of this paper is to study two flip-chip processes and to enhance the understanding of how different process parameters affect reliability.

1.1 Background

A general trend in modern electronics is smaller and more efficient designs. Flip-chip technology is becoming increasingly important in the industry due to ongoing miniaturization. (Yoon, & Jang, 2024) Market-driven demands for more compact and functional components influence both consumer electronics and the military/aerospace sectors. In consumer products such as smartphones and tablets, reduced size and increased functional density are key factors, while military and aerospace applications require high reliability and resilience to extreme conditions. As flip-chip technology becomes more widely used in advanced electronics such as 5G base stations, new demands arise for long-term reliability and mechanical strength. An important issue in flip-chip assembly to consider is that the connections between the chip and the substrate are sensitive to mechanical stress, particularly during repeated shifts in temperature, which can lead to fatigue in the solder joints. Underfill is commonly used to improve reliability, but it comes with new challenges such as avoiding void formation, uneven flow, or poor adhesion. These are factors that can compromise the overall performance of the component. The specific problem investigated in this project is how different process parameters in flip-chip assembly, with a focus on underfill application, affect reliability. This is of relevance to Ericsson, who aim to incorporate flip-chip technology as a possible alternative to traditional wire bonding in their 5G prototype components at their facility in Borås.

1.2 Purpose

The purpose of this report aims to analyse and evaluate two different flip-chip processes while testing key parameters to assess reliability. Special focus is placed on the underfill process, using correct material application and adhesion to analyse the mechanical stability and performance. From these results help Ericsson get a deeper understanding of the flip-chip process.

1.3 Specification of the research question

Main question:

What results, in terms of reliability and mechanical stability, are achieved for two specific flip-chip configurations based on predetermined process parameters and materials?

Sub-questions:

- How reliable are the connections between the die and the substrate when subjected to temperature cycling?
- Will the selected underfill material and application method provide sufficient mechanical stability, or could issues such as voids and other defects occur?
- What limitations exist in the chosen testing methods, and how do these affect the reliability of the collected results?

1.4 Limitations

This thesis only tests a small sample size of C4 and gold stud bump flip-chips, around 20 of each. The thesis will focus on a few prototypes, using only one method for the C4 chip process and one for the Au gold stud bumps. There will be no trial and error. The project is limited to the assembly and analysis equipment available at the site in Borås. The experiment includes steps that are performed manually, such as the application of underfill for the C4 components. This can lead to variation in the dies, such as voids. The quality control is limited to analysing cross-section, shear testing and daisy chain testing. Also, the daisy-chain tests are limited to a standard multimeter. X-ray inspection will only be used to check if the bumps are correctly lined up. No deeper analysis will be performed because the site does not have the necessary equipment.

2. Theory

This section will cover the theory needed to better understand this project.

Flip chip bonding is an interconnection and assembly technology where the ICs active side is facing down (Tummala, 2019). The active side is electrically connected to the substrate. The connection between the active side of the IC and the substrate most commonly consists of solder bumps but can also be connected using other methods such as gold stud bumps or copper pillars. The flip chip method creates short interconnections between chip and substrate resulting in low resistance and inductance. The C4(Controlled collapse chip connection) flip-chip technology was developed by IBM in 1962. The new method was an attempt to solve limitations of wire bonding regarding I/O density and electrical efficiency. Solder balls were preferred as a means of connecting the chip to the substrate, but gold and copper were also used. Solder balls work especially well because of their ability to self-align in the assembly process. Unlike wire bonding, flip chip bonding places the chip directly over the active circuitry which makes more compact assemblies possible.

2.1 Summary of C4 flip-chip method

Solder-based flip-chip is a process that usually starts with the application of an under-bump metallization (UBM) layer on the wafer (Sahoo, K., Harish, V., Ren, H., & Iyer, S. S.; 2025). The UBM ensures good adhesion between the connection pads on the chip and the solder balls, and it also protects against diffusion and oxidation. Solder bumps are then placed onto the connection pads. This can be done in different ways. One method is a stencil process, where solder paste is applied to the connection pads and then heated to form the bumps. Another method is to use an electrochemical process to electroplate the solder onto the UBM.

After the solder bumps have been connected to the wafer surface, the wafer is divided into individual dies. This process is known as dicing or singulation and cutting is performed either by a laser or by mechanical sawing (Wu, Y., Yuan, L., & Xia, H., 2024). After the dies have been separated, the next step is to place them on a substrate. The dies are flipped so that the solder bumps are facing down and aligned with the corresponding connection pads on the substrate. Before the die is placed on the substrate, the solder bumps are dipped in flux, which reduces oxidation and prevents void formation in the solder. The die and substrate are then placed in an oven for the reflow process, where the solder is heated until it collapses and attaches to the substrate's connection pads. The reflow also enables the die to self-adjust its position before the solder solidifies. Underfill is often applied in the gap between die and substrate to increase mechanical stability and reliability (Sahoo, K., Harish, V., Ren, H., & Iyer, S. S., 2025).

Different techniques such as an X-ray machine can be used to check the quality of the finished package with interconnections between die and substrate. Lastly the die can be encapsuled to protect it from the environment. Flip chip technology compared to wire bonding, another semiconductor interconnect technique, offers a more compact assembly with shorter interconnect paths, higher signal density and improved electrical and thermal performance (Yan, S., Zhao, L., Song, Z., Li, R., Hao, Y., & Zhang, Z. 2024).

2.1.1 Under bump metallization (UMB)

Under bump metallization (UMB) is commonly used in the flip chip process. Its function is to maintain the stability of the solder connections under thermal and electrical stress (Mohanram, H., Kim, C.-U., Chen, Q., Thompson, P., & Kusi, S. A., 2024). UMB consists of a metallic layer which is placed between the solder and the die, improving adhesion and limiting the diffusion between different materials. An important step for the reliability and longevity of electrical connections in the components.

A study by (Mohamram, H., Kim, C.-U., Chen, Q., Thompson, P., & Kusi, S. A., 2024), examens how different UBM materials and structures affects the durability of solder joints when exposed to high temperatures and strong electric currents. The study concludes that optimizing the layers, using different materials like nickel, copper, and palladium, will significantly enhance resistance to issues such as diffusion, electromigration, and thermal fatigue. Ultimately, the key to UBM design is a balance between thermal and electrical demands for reliable and high performing solder joints.

2.1.2 Flux

Fluxing is an important step in the flip-chip process. Making the soldering more reliable by cleansing the contact pads on both the chip and substrate. This process minimizes oxides, contaminants, and impurities that can disturb solder adhesion. The flux is applied to the solder balls using either spraying or dipping methods. (Su, H.-P., Hsu, M.-H., & Horng, C.-H. 2024).

There are different kinds off fluxes, according to (Lim, S., Chou, J., Durham, M., and Mackie, A. 2015). Most used is water-soluble flux, but standard no-clean flux and ultra-low residue (ULR) no-clean flux are also used. After the reflow process, flux residues are typically removed to improve the flow of capillary underfill material, minimize voids, and to ensure strong adhesion between the underfill, solder joints, and substrate. Water -soluble fluxes require cleaning after soldering. This becomes more difficult and riskier as components shrink and become more fragile. Standard no-clean and ULR no-clean fluxes, however, leave behind minimal residue, eliminating the need for aggressive cleaning and reducing the risk of damaging delicate chips. Selecting the right flux is critical. Poor flux choice can lead to defects like voids, weak joints, and delamination, all of which threaten the performance and durability of the product.

As the industry moves toward smaller and more complex designs, flux solutions become more significant, impacting production yields, product lifespan, and manufacturing efficiency (Lim, S., Chou, J., Durham, M., and Mackie, A. 2015). The transition toward advanced fluxes like ULR no-clean types further proves this point. Focusing on high-performance assembly processes while meeting the strict demands of modern semiconductor packaging.

2.1.3 Reflow process

During flip chip assembly, the die is placed on top of the substrate, and the pads on the substrate are aligned with the bumps on the die. After placement, the next step is the solder mass reflow process (Lau, 2024). The die and substrate are placed in a reflow oven, where the reflow process follows a specific temperature profile divided into four stages: ramp-up (heating), soak zone, reflow zone, and ramp-down (cooling) (Li, Lee, Evans, & Baldwin, 2011). During the ramp-up stage, the temperature increases steadily. Once the temperature reaches a certain level, the soak zone begins, where the temperature is held constant for a set period to activate the flux. In this stage, the flux removes oxidation from the surfaces on the pads and solder bumps in preparation for soldering. The soak zone also ensures that the entire assembly reaches the same temperature. Next is the reflow zone, where the temperature rises to its peak and exceeds the melting point of the solder. The solder remains above this melting point for a period called TAL (Time Above Liquidus), allowing the solder to properly melt and form the joints. The final stage is ramp-down, where the oven cools the assembly at a controlled rate to prevent thermal stress and cracks in the solder joints. Careful control of each stage is essential to manage the formation of IMCs (intermetallic compounds), which are critical for the long-term reliability of the solder connections.

2.1.4 Underfill (C4)

Underfill plays a critical role in the reliability and performance of solder-based flip-chip interconnections and serves two primary functions. (Sahoo, K., Harish, V., Ren, H., & Iyer, S. S.; 2025). First, it acts as a binding layer between the chip and substrate. Improving the mechanical stability, compensating for the relatively weak solder joints. Second, it provides a barrier against moisture, reducing the risk of corrosion and deterioration over time.

The conventional process for connecting a die to a board typically uses solder-balls. Due to the difference in thermal expansion coefficient (CTE) and small contact surface between the die and the substrate, significant shear strain develops in the interconnects during temperature cycling. Over time, this leads to fatigue cracking and eventual electrical failure (Sejin Han, & Wang, K. K.;1997). The method to reduce this problem is filling the space between the solder joints with an encapsulant. This enhances mechanical durability, underfill materials are applied to redistribute thermal loads across the package. Since this encapsulation primarily occurs beneath the chip, the process is referred to as underfill encapsulation. There are three primary methods for underfill application: post-bonding capillary dispensing, pre-applied no-flow underfill before bonding, and incorporation into an epoxy moulding compound using a pressure-driven process (Sahoo, K., Harish, V., Ren, H., & Iyer, S. S.; 2025).

Underfill does introduce additional challenges, particularly related to voids formation. Voids commonly develop near the solder bumps, leading to localized stress concentrations that may compromise long-term reliability. To counteract these effects, underfill formulations with low CTE and high modulus are preferred. These materials are often reinforced with silica fillers to improve mechanical stability and thermal performance (Sahoo, K., Harish, V., Ren, H., & Iyer, S. S.; 2025). Another problem can also be flux residues that can interfere with proper underfill application. Therefore, thorough flux cleaning is essential. As flip-chip packaging continues to evolve, precise control over underfill composition and processing techniques remains a key factor in achieving robust and high-performance electronic assemblies.

2.2 Au-stud bumps

The flip-chip method can be used with different types of bumps. The Au stud bump method uses a gold wire to create small gold "stud bumps" on the connective pads (Yan et al., 2024). The process begins by threading ahigh-purity gold wire through a bonding capillary. The chip is heated, and the tip of the wire is melted, which forms a small gold sphere called free air ball. With the use of bonding pressure and ultrasonics, the free air ball is then pressed onto the pad. The gold bonds to the surface of the pad. The capillary tool is then lifted, and the wire clamp closed and moved upwards. This causes the wire to break near the tip which forms a stud bump attached to the pad. There are also the option place bumps to onto the bumps. This can be an advantage because the pitch can be reduced, which improves performance.

2.3 Reliability

The packaging technique flip chip has many advantages that have made it popular such as, great electrical performance, enabling higher number of input/output(I/O) than traditional wire bonding method and small packaging size (Wang et al., 2020). The flip chip technology also comes with challenges. The interconnections between substrate and die are vulnerable to mechanical failure due to both mechanical stress and temperature changes. The package consists of different materials with different coefficients of thermal expansion which causes the different components to expand at different rates leading to stresses in the bumps or solder balls. These stresses can lead to mechanical failures and reliability issues. If these issues are not addressed, for example by using underfill, they will limit the high-reliability applications of the flip chip.

2.3.1 Temperature cycling test and Daisy chain

To test the reliability of a flip-chip assembly a temperature cycling test can be used. A temperature cycling test is a commonly used method to evaluate how electronic components are affected by repeated, significant temperature fluctuations (Lau, 2024). These temperature fluctuations can cause fatigue, particularly in the solder joints and intermetallic compounds, which over time may lead to crack formation and ultimately complete failure. The test is conducted by placing the components in a special oven where the temperature can be precisely monitored. A program is set that shifts between high and low temperature, in a predetermined time, for a number of cycles. The number of cycles varies between a few hundred to thousands depending on the goals of the test.

To evaluate the results, a daisy chain structure can be utilized (Lau, 2024). The chip is prepared with an integrated daisy chain, which, once the chip is bonded to the substrate, forms a continuous circuit through some or all the solder ball connections. This configuration usually allows for continuous monitoring of the circuit's resistance. Under thermal fatigue loading, most solder joints develop cracks, leading to an increase in electrical resistance. As the cracks grow larger, the resistance gradually increases from low to high.

Before conducting the reliability test, specific failure criteria are defined (Lau, 2024). These criteria may be a certain percentage increase in resistance, a fully open circuit, or the presence of cracks exceeding a specified size. When a solder joint completely fractured, the resistance cannot be read, indicating that the circuit has been broken. Resistance is measured before, during, and after the temperature cycling test. The data collected is then analyzed to determine the time or number of cycles required for failure to occur.

To examine the intermetallic compounds, as well as potential microcracks and voids within the solder balls, the completed assembly can be cross sectioned through the solder balls, polished to a fine surface, and analyzed under a microscope. This is done both before and after a temperature cycling test to observe the impact of the temperature cycles.

3. Method

This chapter outlines the methods and procedures applied throughout the project, including literature review, assembly processes, and reliability testing, to systematically investigate the performance of the flip-chip configurations.

3.1 Literature study

The work began with a literature study to get an understanding of the process and technology of flip-chip. Academic databases such as IEEE Xplore and Chalmers library were used to identify relevant sources, prioritizing peer-reviewed journal articles, conference papers, and technical reports to maintain credibility.

3.2 Assembly of flip-chip

This section details the procedures used for assembling chips onto substrates, including placement, bonding, reflow, and underfill application techniques.

3.2.1 Placement of chip

The placement was done using a semi-automated die bonder. It is a machine with a camera that allows the user to see both the bumps of the chip and the substrate simultaneously. This enables precise alignment of the chip with the substrate. Once the alignment is verified, the camera moves away, and the chip is accurately placed onto the substrate.

3.2.2 Reflow

The reflow process was done using a specialized oven that carefully controls the temperature. It heats both the chip and the circuit board according to a set temperature profile, with different stages like preheating, melting the solder, and cooling. This ensures that the solder joints form correctly without damaging the components. The same oven was also used to heat the underfill material, but with a different temperature profile customized to that process.

3.2.3 Au-stud bumps

The Au-stud bump flip chips were assembled using a wire bonder to place bumps on the substrate, followed by thermocompression bonding to attach the chip to the pre-deposited bumps.

3.2.4 Underfill application

The underfill was applied manually using a dispensing needle and a heating pad. Air pressure was used to dispense the underfill, while the substrate was simultaneously heated by the pad to lower the viscosity of the underfill and assist with flow.

3.3 Reliability

To assess the reliability of the flip-chip assemblies, tests were conducted to simulate the types of stress that components are exposed to during operation in the real world. This included temperature cycling to simulate temperature fluctuations, resistance measurements using daisy chain circuits, and shear testing to evaluate mechanical strength over time. The goal was to identify how different assembly methods and the use of underfill affect long-term durability.

3.3.1 Temperature cycling

To test how changes in temperature affects the reliability of the interconnections between die and substrate the assembly was placed in a temperature cycling box where the temperature was repeatedly raised and lowered over several weeks. Various tests were performed before the temperature cycling to see if results would change as the number of cycles increased. The same tests were performed on two occasions during the temperature cycling as well as after the temperature cycling was complete.

3.3.2 Daisy chain

The chips and substrate used in this project comes prepared with a circuit called daisy chain running through the substrate and via a solder bump, into the chip then back into the substrate. When placing the probes of a multimeter on the two connection pads to the daisy chain it completes the circuit and allows the resistance to be read. There are different types of daisy chains, but the one used here only pass through two bumps on the corner of each chip. We tested the resistance of daisy chain in the C4 chips before, during, and after the temperature cycling. Since the chips and substrate that were assembled using Au stud bumps did not come prepared with a daisy chain, the resistance was not tested.

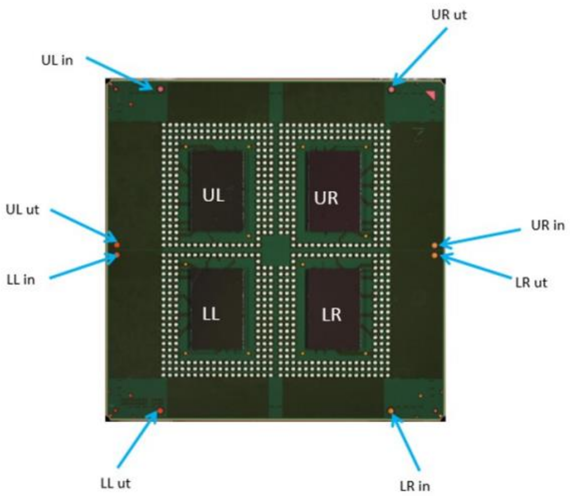


Figure 1. Daisy chain measure pads on substrate

3.3.3 Shear test

A shear test was used to test the mechanical strength of the solder joints. The test was performed on both the chips assembled using the C4 method and the chips assembled using Au stud bumps. The chip on the substrate is placed parallel with the edge of the tool and then held in place using vacuum. A shear program is then selected and started. The tool pushes on the edge of the chip until the bond between substrate and chip breaks or the machine reaches its maximum force. The test was used to see if the amount of force needed to break the bonds changed because of temperature cycling and what the difference was between chips with and without underfill applied.

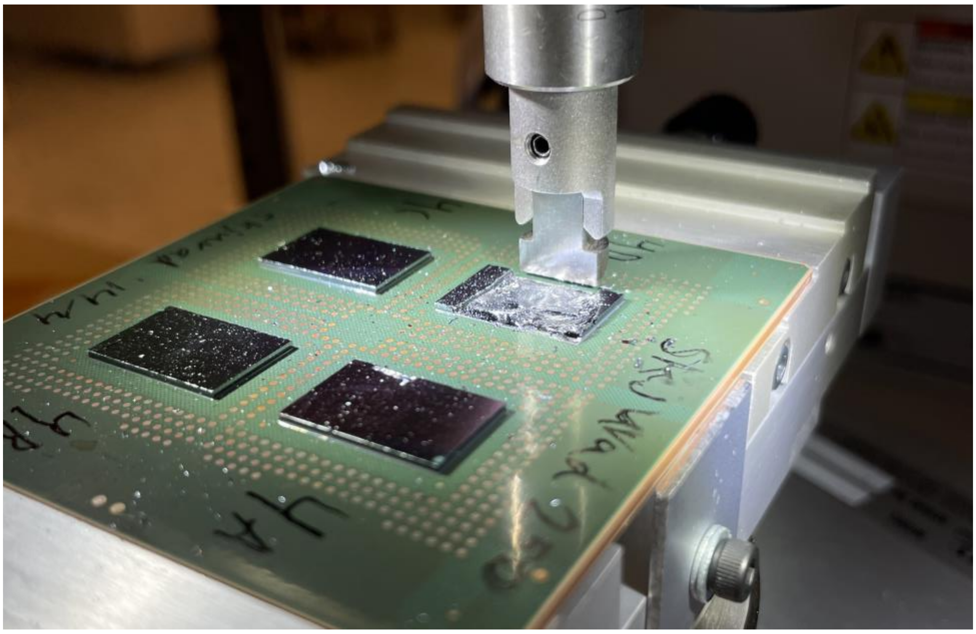


Figure 2. Chip breaking during shear test

3.3.4 Assembly cross section

During the reflow process flux residues can cause voids to form in the solder bumps weakening the connection. When applying underfill it can appear that the underfill has filled the entire gap between the chip and the substrate because the underfill can be seen all around the edges of the chip. But voids in the underfill might still have formed under the chip due to poor application technique or gas forming from left over flux. To investigate the amount of voids, the stand-off, bump collapse cross sections were used. First the assembled chip was cut in half using a thin saw. The cut chip and substrate were then placed in a mould and covered with epoxy and left to cure overnight. A rotating sanding machine was then used to achieve a fine surface through the centre of the solder bumps. This allowed the cross section to be easily examined under a microscope.

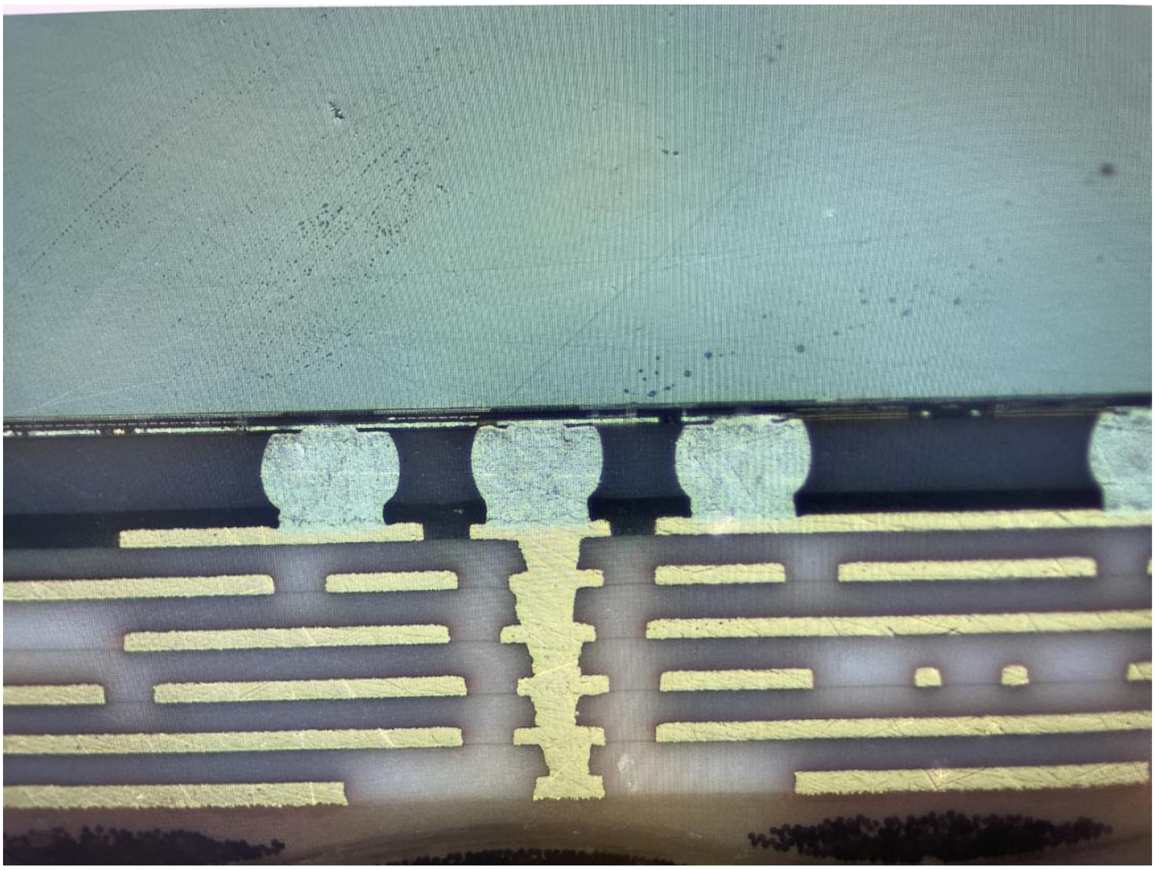


Figure 3. Cross section of a C4 chip assembly

4. Implementation

This section explains in detail how the different methods were applied in practice, including how the flip-chip assemblies were carried out, how the tests were performed, and how the equipment and materials were used to achieve the goals of the project.

4.1 Assembly of C4 flip-chip

The assembly was made using a die-bonder machine called Tresky-5300. Four chips were mounted on each substrate, and ten substrates were produced, resulting in a total of 40 assembled chips.

The first step involved dipping the solder balls in flux to their midpoint. Flux BM1-RMA-NC was used during the process. Each solder bump had a measured diameter of 0.092 mm using a microscope, making the optimal dipping depth 0.046 mm. However, due to equipment limitations, the actual dipping depth was set to 0.050 mm (50 µm). The die was dipped for 500 milliseconds before being placed onto the substrate.

Figure 4. Dipping in flux

After the solder balls on a chip had been dipped in flux the next step was to align the solder balls on the chip and the connection pads on the substrate and place it there.

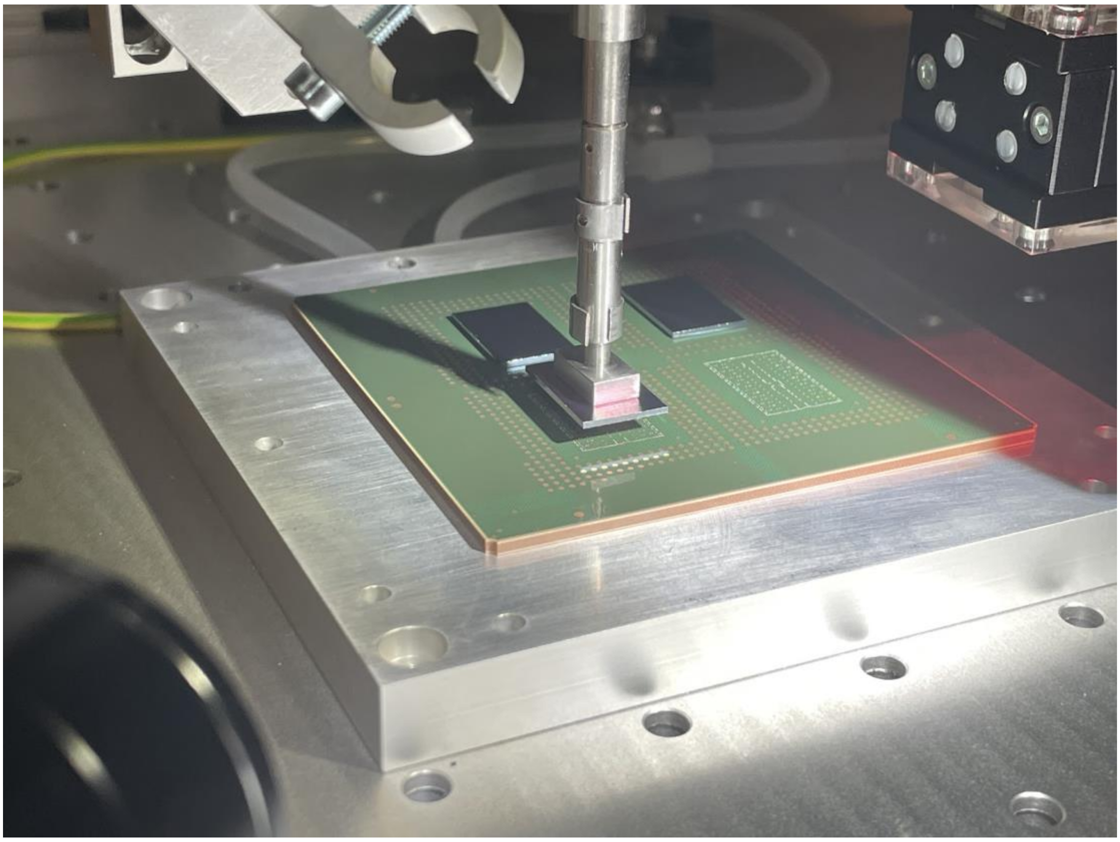


Figure 5. Chip placed onto the substrate.

4.2 Reflow process

The C4 substrate and chip were placed in a reflow oven using the LEAD-FREE-245-N2 process, where "245" refers to the peak temperature in the reflow process.

The Au-stud bumps were assembled by Ericsson using thermocompression.

4.3 Cross section

C4 chips were cut in half using a specialized saw. This was made though out the process in different stages of the thermocycle. They were then infused in epoxy, followed by grinding with sandpaper of progressively finer grit. This was done to reveal potential voids or determine if the bump had been incorrectly placed. The Au-stud bumps chips were too small to go through this process.

4.4 Underfill

The underfill was applied by hand using a pressure needle. Meanwhile, the substrate was heated to 100 degrees Celsius. The application was made in an L-form over several rounds. The underfill used was UF 9000AE. The substrates were then placed in the reflow process again. This time with a different process with different reflow profile to cure the underfill. This was done one 20 chips (C4) or 5 substrate.

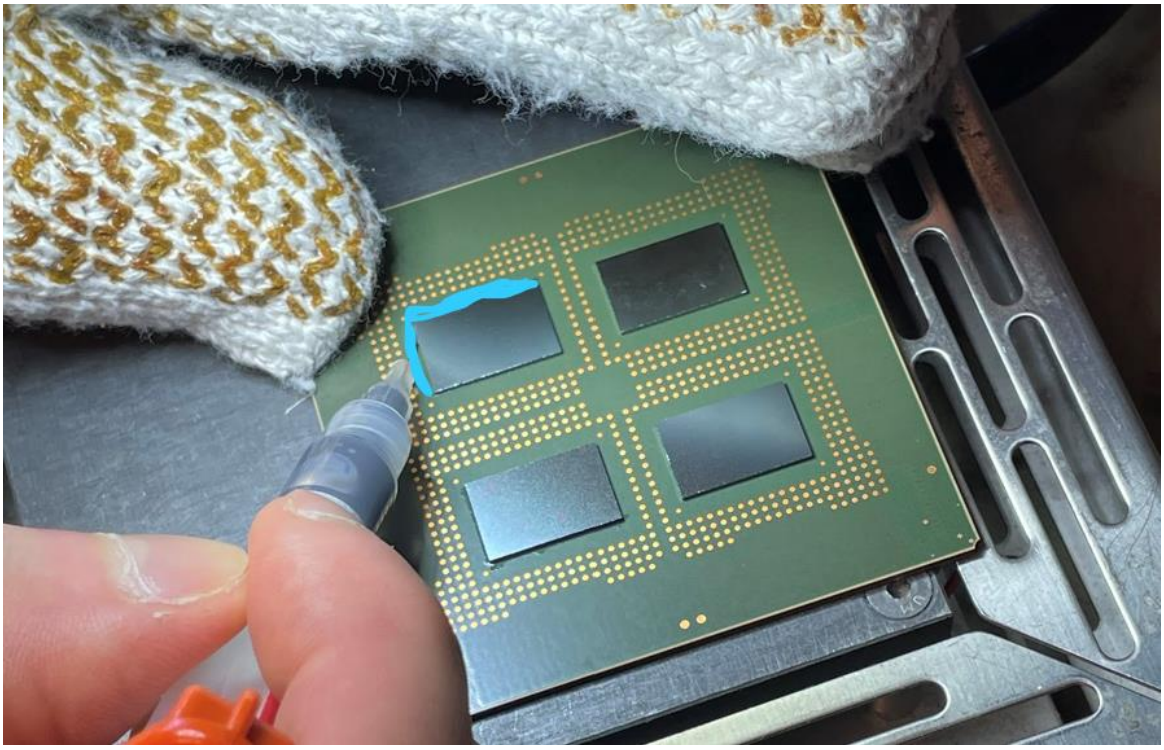


Figure 6.Underfill being applied

The same process was done with the Au-studbumps chips but only applied to one side and with a smaller needle.

4.5 Temperature cycling

The cycling planned to be in total 1000 cycles and taken out and tested at 250,500,750 and 1000. Each cycle ranged from minus 40 to 125 degrees Celsius. There were some complications with the thermobox, which means the number of completed cycles was not exactly 250 or 500, but rather approximate. In total was 16 chips (C4) with underfill and 16 without underfill taken through the cycling.

The Au-Stud bumps joined later and were tested at around 300, 550, and 800 cycles.

4.6 Testing

This section provides a clear and structured explanation of how the various tests were performed. Each testing procedure is described in detail to illustrate how it was used to assess the quality, mechanical strength, and reliability of the assembled components.

4.6.1 Daisy-chain test

The resistance in the chips were tested using a multimeter. Each chip was tested individually at 250, 500, 750, and 1000 cycles. However, due to the shear test that was also carried out at these cycle steps, the sample available for resistance testing progressively decreased. As expected, the chips without underfill failed the shear test, which further reduced the sample size for resistance testing.

4.6.2 Shear test

The shear test was done by a machine called DAGE Series 4000 plus. The machine pushed on the side of the chip with a shear force increasing until the chip were detached from the substrate or the machine reached its maximum force of around 100kg. A total of eight chips underwent shear testing at each step, four with underfill and four without. In total there was five steps of testing, one before the cycling and then at 250, 500, 750, and 1000 cycles.

A similar procedure was followed for the Au-stud bumps, but only four test steps were performed. This was because the Au-stud bump chips were assembled later and had to join the cycling when the C4 chips had already reached 200 cycles. As a result, testing was conducted at around 300, 550, and 800 cycles, with five chips tested at each step.

All the results were put in an excel document.

4.6.3 Height measurement for Au-stud bumps

The Au-stud bumps were measured at all four corners of the chip to check whether the chip was mounted evenly, i.e., at the same height in all corners, and to confirm if the stand-off height was 15µm as desired.

5. Results

This section presents the results obtained from the measurements and observations made during the assembly and testing of the flip-chip samples. The focus is on how different assembly methods and how underfill affect electrical resistance and mechanical strength over time. Results are reported separately for C4 and Au-stud bump configurations, based on resistance measurements, shear testing, and cross-sectional analysis.

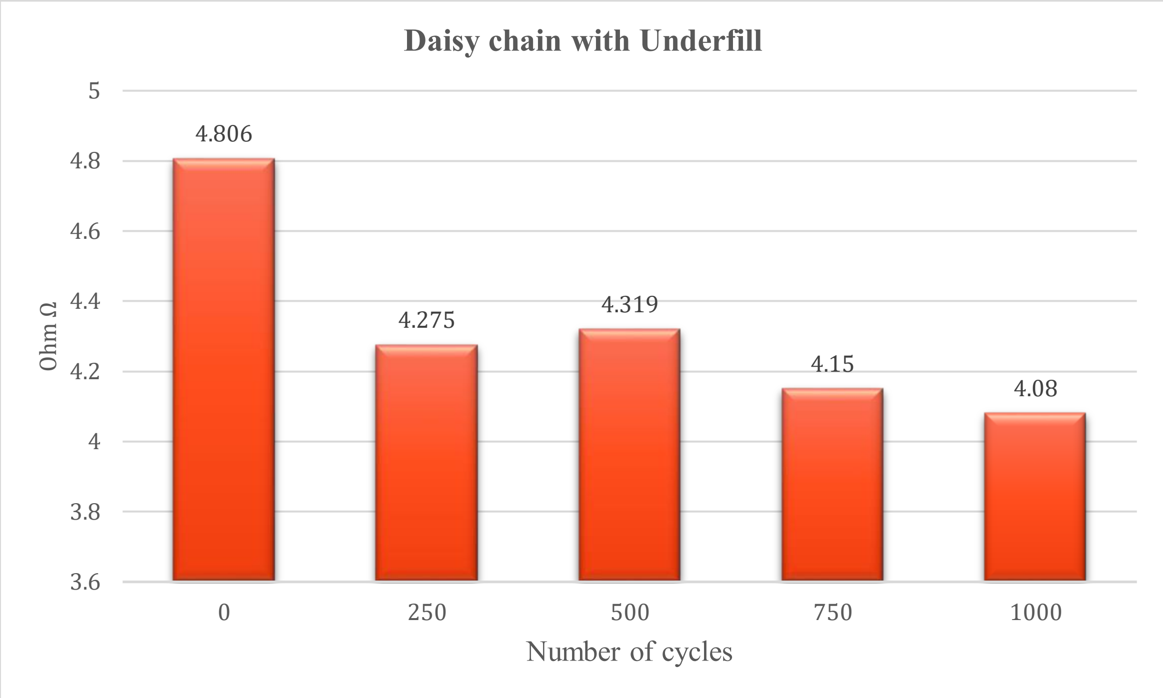
5.1 C4 flip-chip

This subsection presents the results for the C4 flip-chip assemblies. The evaluation includes resistance measurements from daisy chain testing, mechanical strength from shear tests, and visual inspection through cross-sectional analysis.

5.1.1 Daisy-chain

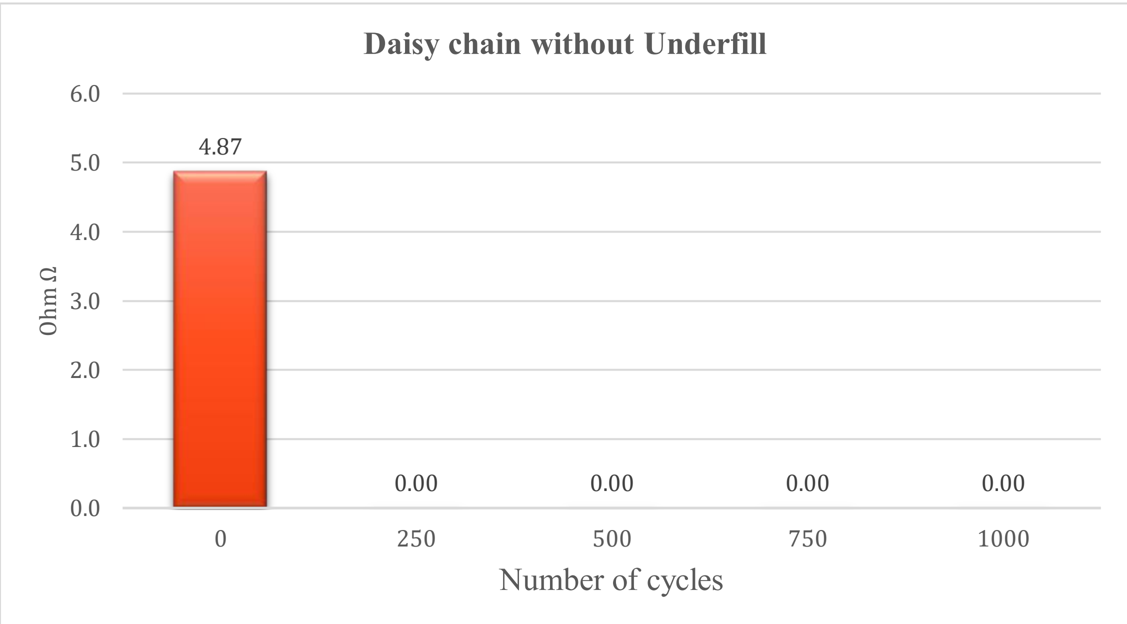
The resistance through the daisy chain was tested at every chip at 0, 250, 500, 750 and 1000 cycles and at each stage an average value of the resistance was calculated. The chart below shows the average resistance at different stages of the temperature cycling for the chips with underfill. Before the temperature cycling starts the average resistance is measured to about 4,8 ohm and as the test progresses the average resistance drops to about 4,1 when all the cycles are done.

Chart 1 Daisy-chain resistance testing with underfill.



The chart below shows the average reading of resistance through the daisy chain on the chips with no underfill. These chips were tested at the same occasions as the chips with underfill. Before the temperature cycling began the average resistance of the chips with no underfill was measured to 4,87 ohms. At the next measurement at 250 cycles all chips without underfill had lost connection and read 0 ohm.

Chart 2 Daisy-chain resistance testing without underfill



5.1.2 Shear test

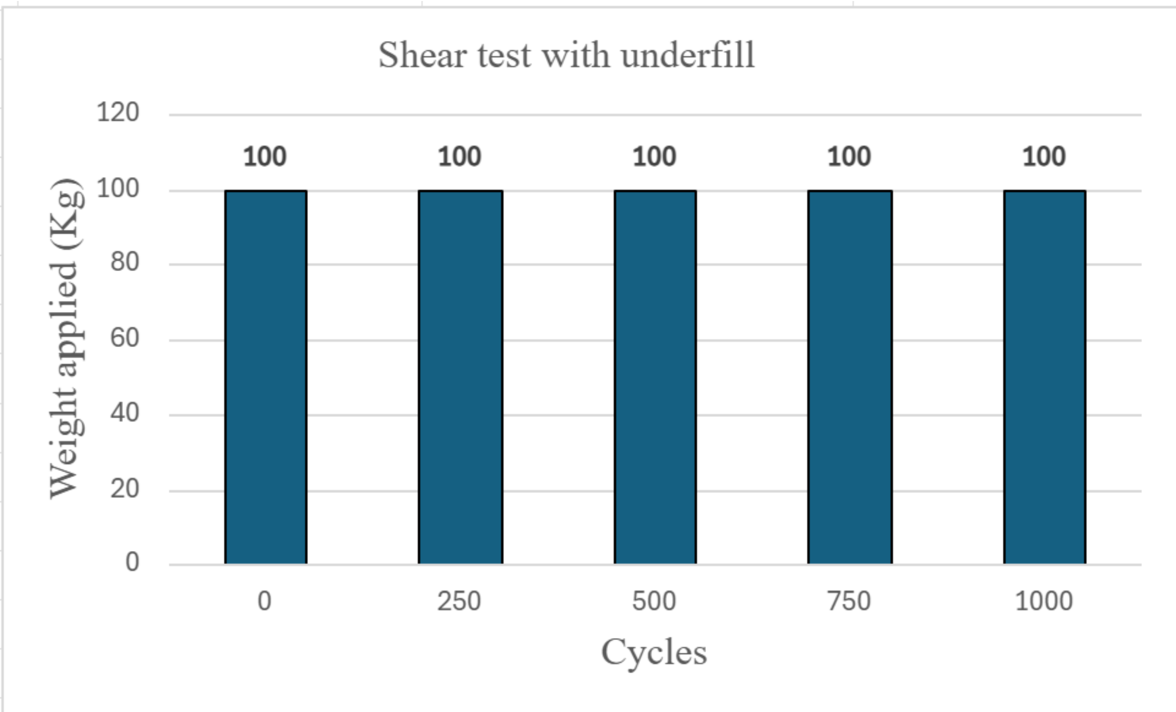
The tables and charts below show the results of the shear tests on the C4 chips with and without underfill. To keep track of all the chips that went into the temperature cycling each substrate was marked with number 1-8 with 1-4 being with underfill and 5-8 with no underfill. Each substrate had 4 chips that were marked with A, B, C, D. When testing the chips with underfill the machine reached its maximum force before the bond between chip and substrate were broken. Instead of testing new substrates every time we reused the same chips when they did not break in the previous test. When the test had run for 750 cycles chip 4D broke. The bond between chip and substrate did not break but instead the chip shattered.

Table 1 The shear test of C4 chip with underfill

	3/20/2025	4/2/2025	4/14/2025	4/25/2025	4/14/2025
Shear test	Before thermocycling	250 cycles	500 cycles	750 cycles	1000 cycles
Chip with underfill	no name	(4A-4D)	(4A-4D)	(4A-4D)	(3A-3D)
A	over 100	over 100	over 100	over 100	over 100
B	over 100	over 100	over 100	over 100	over 100
C	over 100	over 100	over 100	over 100	over 100
D	over 100	over 100	over 100	43.311(silicone broke)	over 100
Average value	N/A	N/A	N/A	N/A	N/A

The chart below shows the average shear force of each test with underfill.

Chart 3. Shear test with underfill



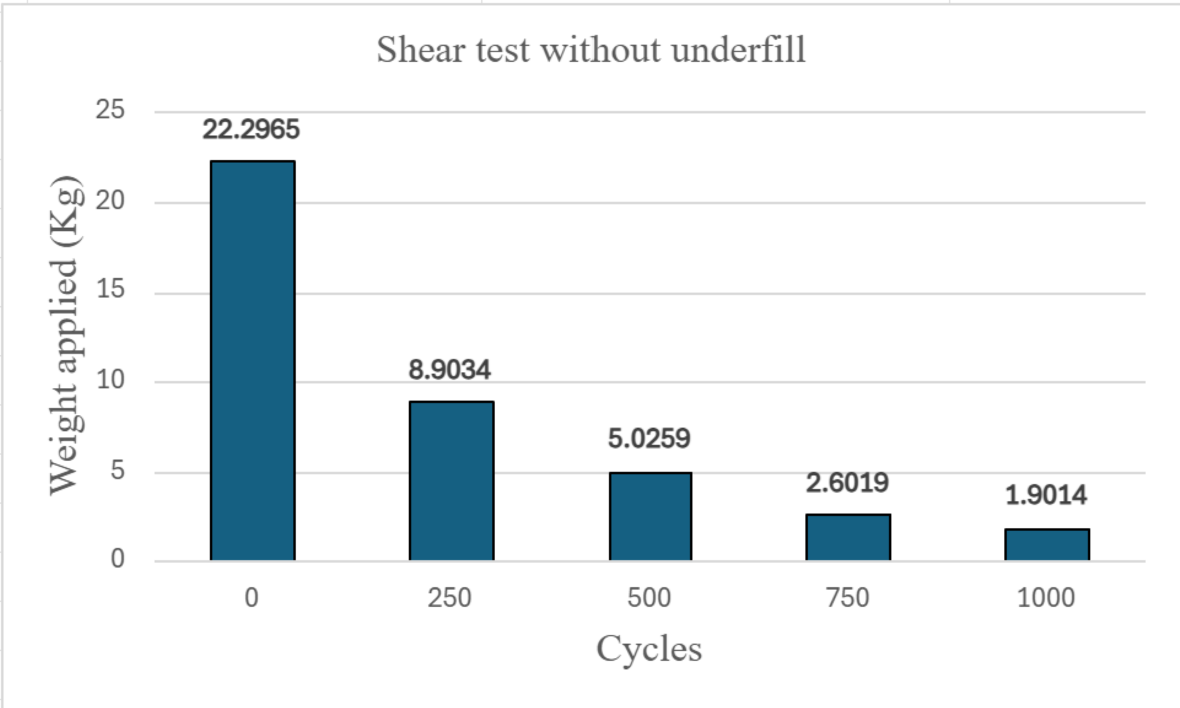
The chips with no underfill broke after each test as seen below. Therefor a new substrate was used at each test. At the last test two of the chips dethatched from the substrate when handling the substrates shown as “Broke by temp” in the table below.

Table 2 The shear test of C4 chip without underfill

	3/20/2025	4/2/2025	4/14/2025	4/25/2025	4/14/2025
Shear test	Before thermocycling	250 cycles	500 cycles	750 cycles	1000 cycles
Chip without underfill	no name	8(A-D)	7(A-D)	6(A-D)	5(A-D)
A	22.1620	8.9286	4.6083	2.8112	*Broke by temp
B	22.1860	9.1167	5.1879	2.2044	*Broke by temp
C	22.3450	8.7339	5.3228	2.4040	1.4125
D	22.4930	8.8344	4.9846	2.9881	2.3902
Average value	22.2965	8.9034	5.0259	2.6019	1.9014

The chart below shows the average shear force of each test without underfill.

Chart 4 Shear test without underfill



5.1.3 Cross section C4 chip

The figure below shows a cross-sectional image of a C4 chip without underfill. The solder bump structure and its dimensions can be observed. The bump height is approximately 131.6 µm and the total stand-off distance from substrate to chip is measured to be around 69,51 µm. The cross section shows that the bump has collapsed as expected.

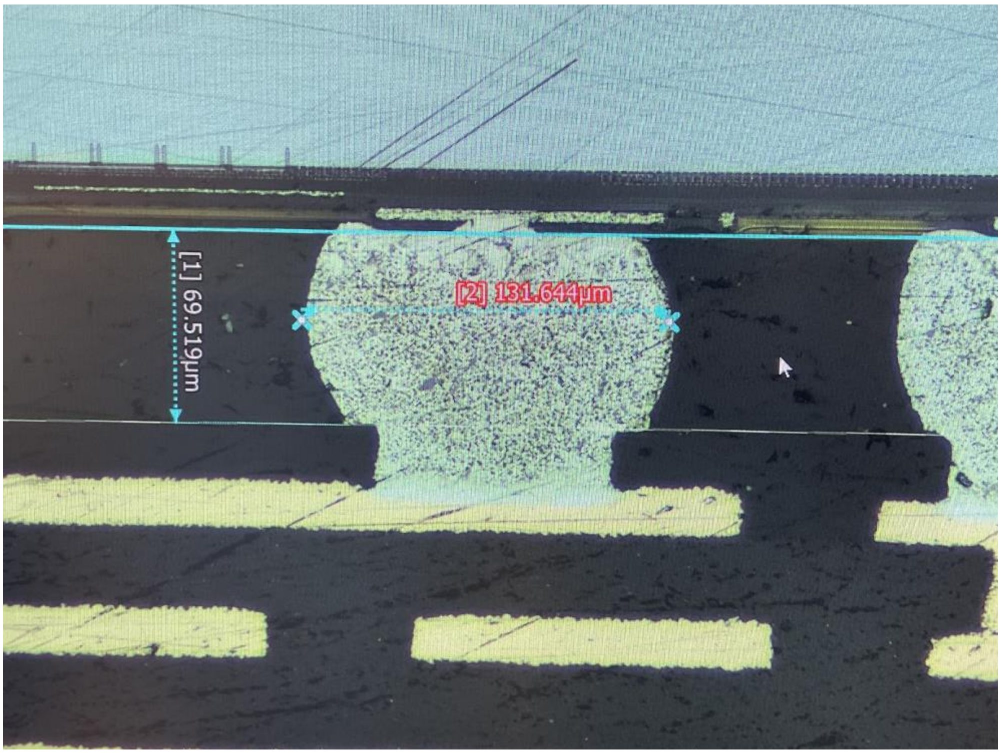


Figure 7. Cross section of C4 chip without underfill, before temperature cycling

Figure 8. Cross section of a C4 chip with underfill. One of the cross sections revealed the presence of voids in the underfill layer, indicating areas beneath the chip where the underfill did not flow properly. The other cross sections showed no signs of void formation.

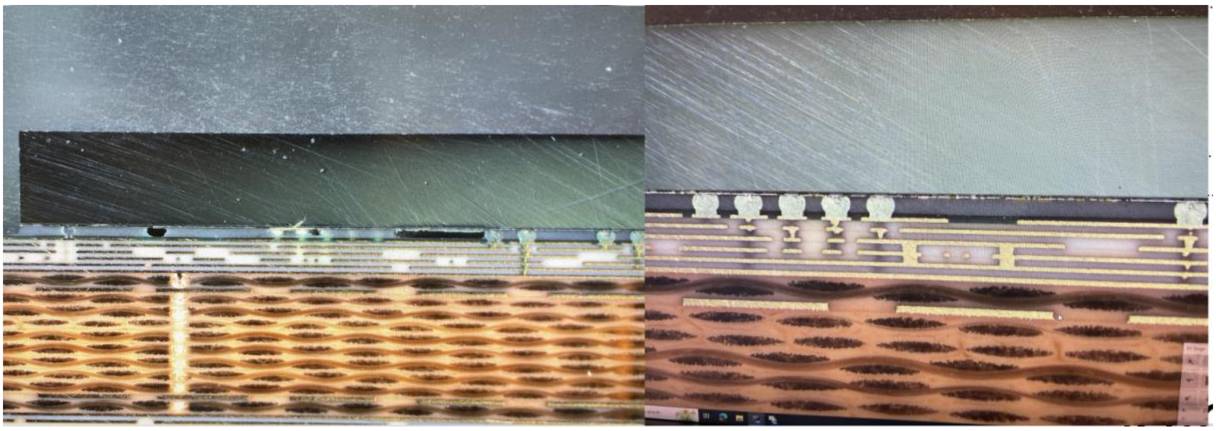


Figure 8. Cross section of C4 chip with underfill, before temperature cycling

The image below shows another cross section of the C4 chip assembly with no voids precent.

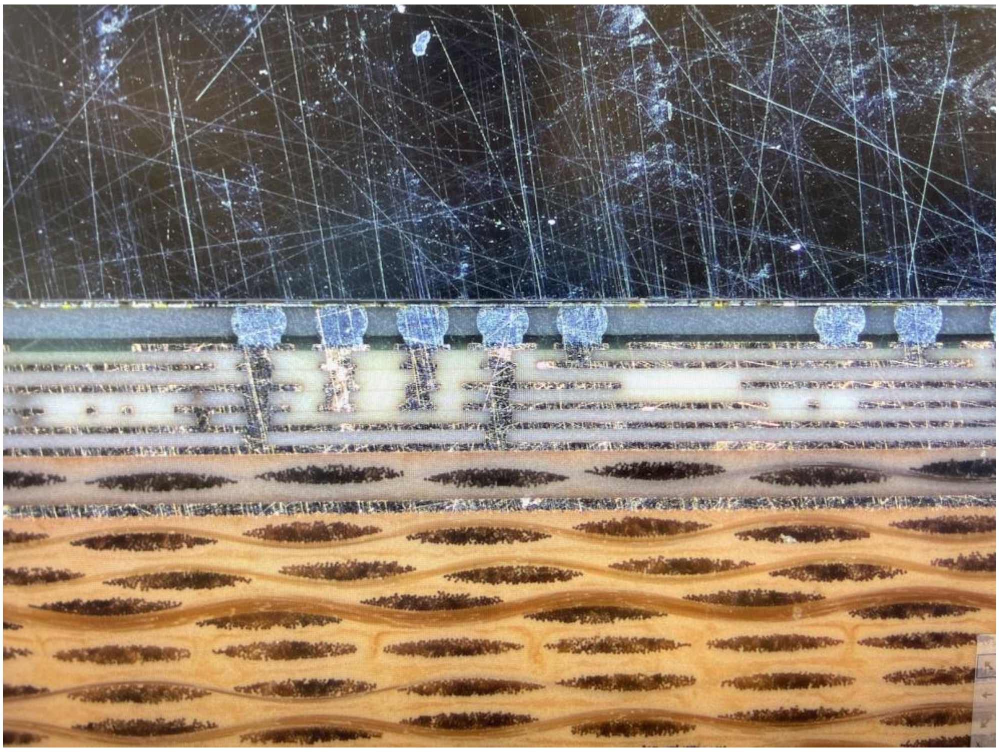


Figure 9. Cross section of C4 chip with underfill, before temperature cycling

The four images below show cross section of 4 different chips. The chips have underfill and all have gone through 1000 cycles in the temperature cycling. No voids were discovered and no signs of visible cracks in the solder bumps.

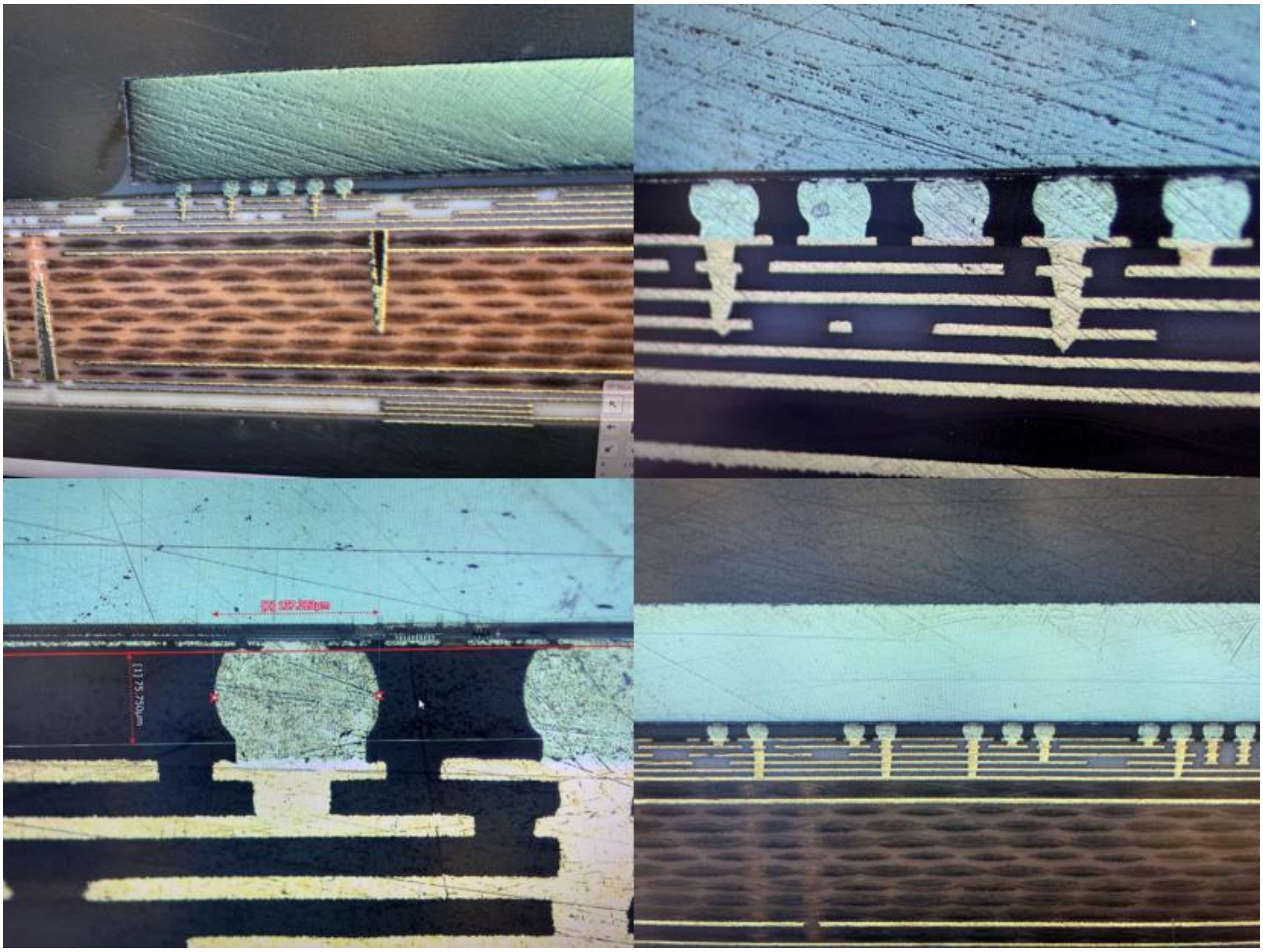


Figure 10. Cross section of C4 chips with underfill, after temperature cycling

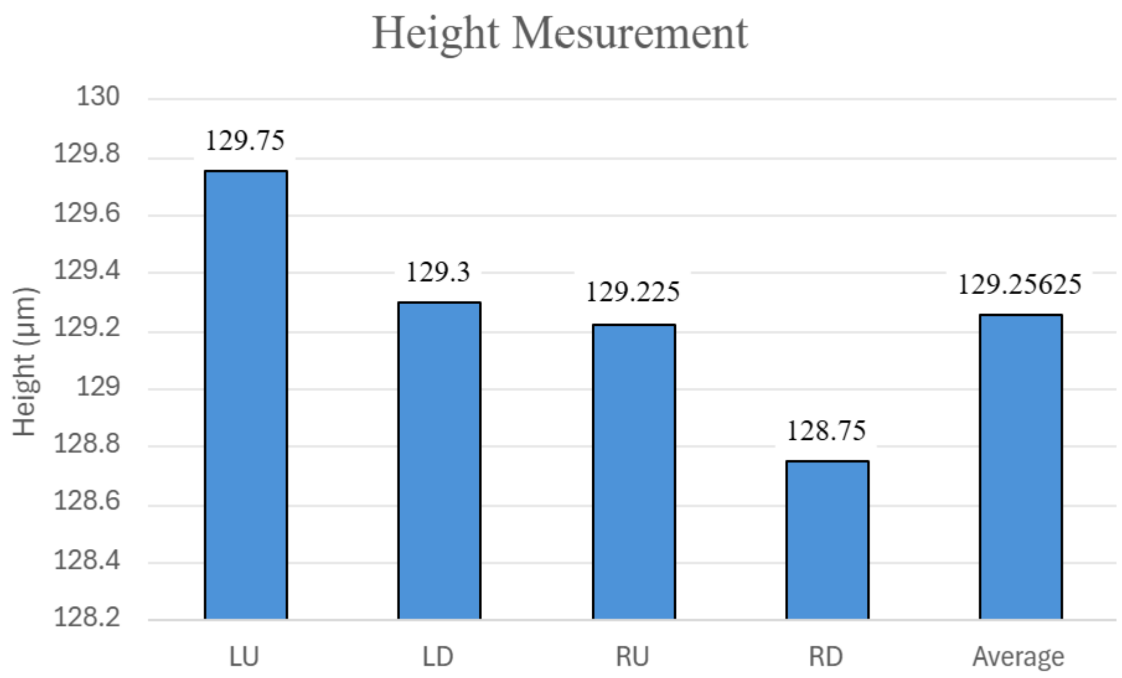
5.2 Stud bumps

This section presents the results from the testing of the Au stud bump assemblies, including measurements of height uniformity, mechanical strength, and visual inspection.

5.2.1 Height measurement

The chart below shows the average height measurement for each corner and the total average. The left down (LD) corner and right up (RD) were about the same height while the corner up to the left (LU) was a bit higher and the corner down to the right (RD) were a bit lower. This shows that the chips on average were leaning slightly.

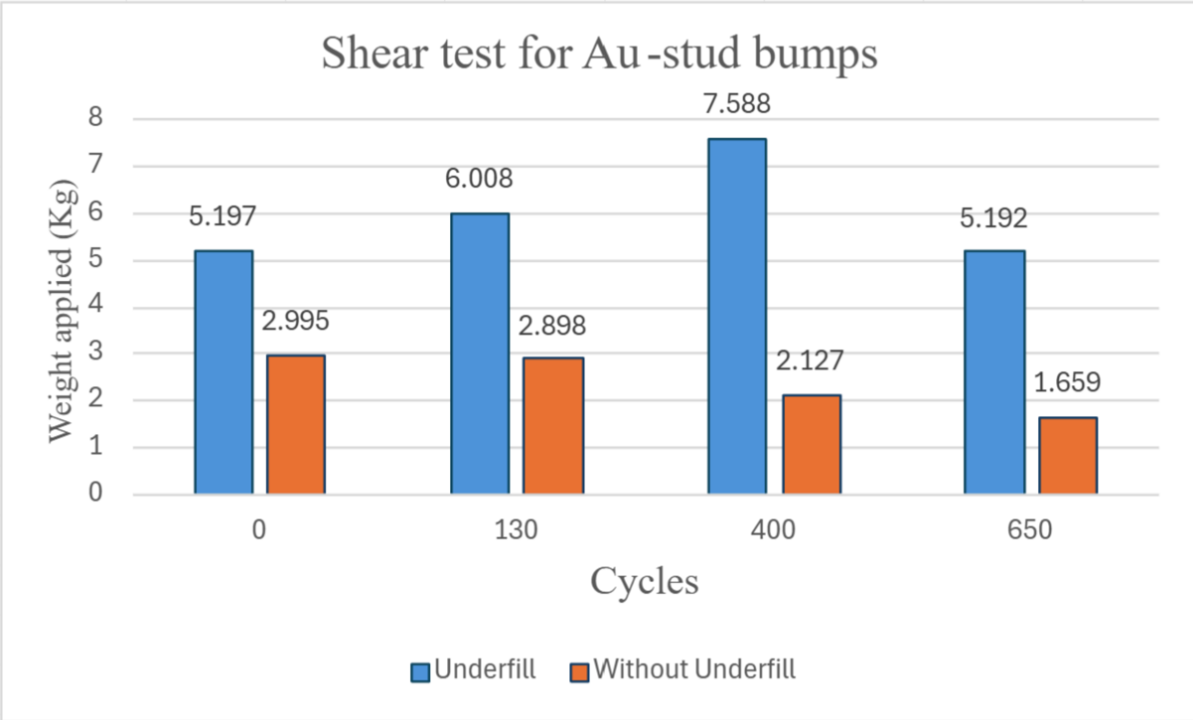
Chart 5, Shows the height of each corner of the chip and an average height.



5.2.2 Shear test

The chart below shows the result of the shear tests for the chips assembled using Au stud bumps both with and without underfill. The amount of shear force that the chips with no underfill could withstand steadily declined as the thermal cycles increased. The chips with underfill could withstand more shear force but the change in result did not steadily decline.

Chart 6. Shear test for Au -stud bumps.



5.2.3 Images after shear test

This image below shows a chip after shear testing. This chip has no underfill applied to it has not undergone temperature cycling. The highlighted studs, marked with red circles, shows where the stud bumps were mounted. The image indicate that the failure occurred at the interface between the bumps and the chip.

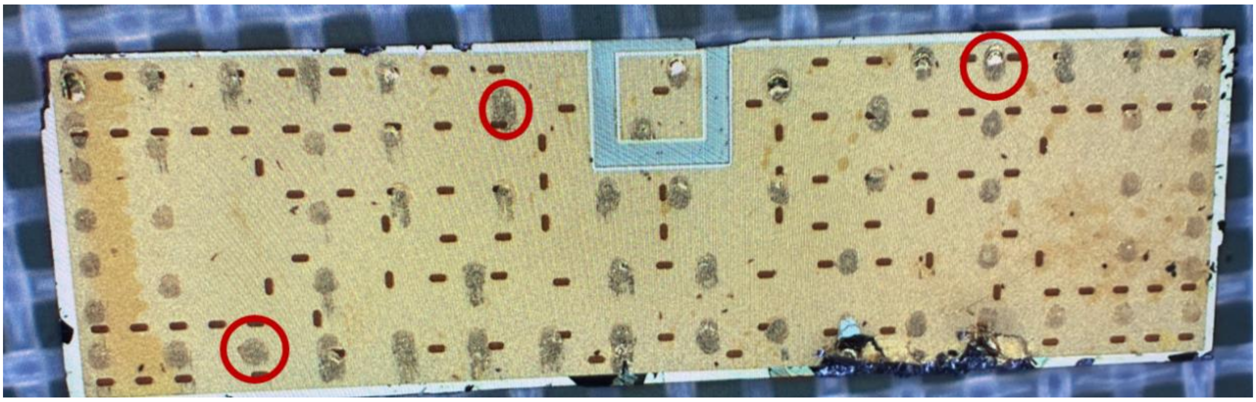


Figure 11 Shows the underside of a chip

This chip has underfill applied to it and undergone temperature cycling for 400 cycles. The chip has very little or no residues of underfill. Which also indicate the same failure as in previous images.

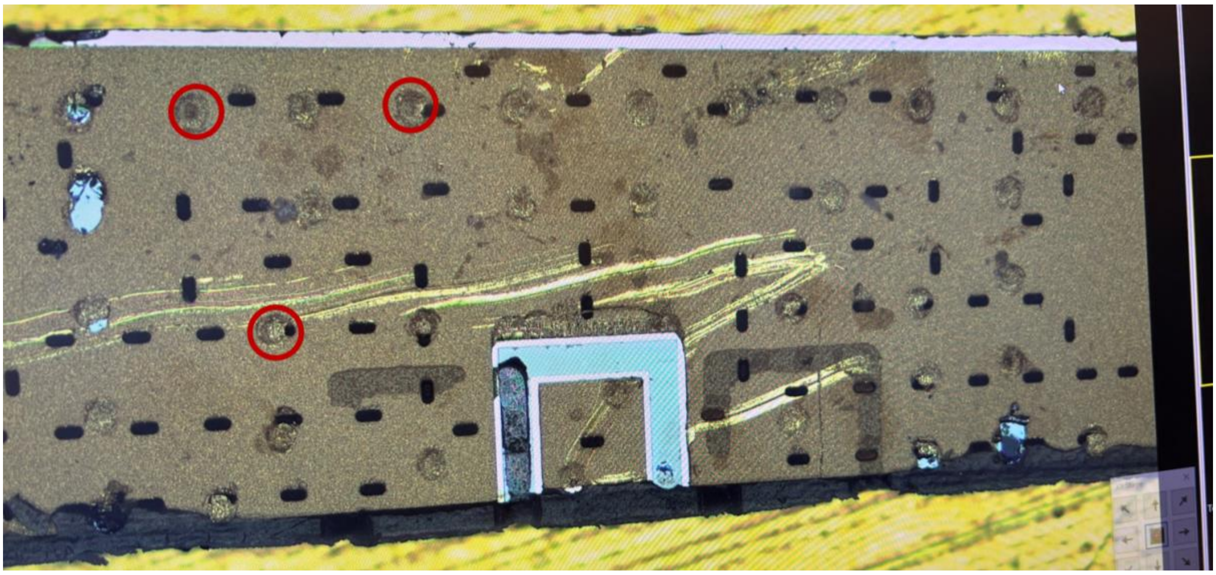


Figure 12 Shows the underside of a chip with underfill

The images below show the substrate with underfill applied. They indicate that the adhesion between the underfill and the substrate is stronger than between the underfill and the chip. The underfill appears to be well distributed with no visible voids, except around the submersion, which is expected.

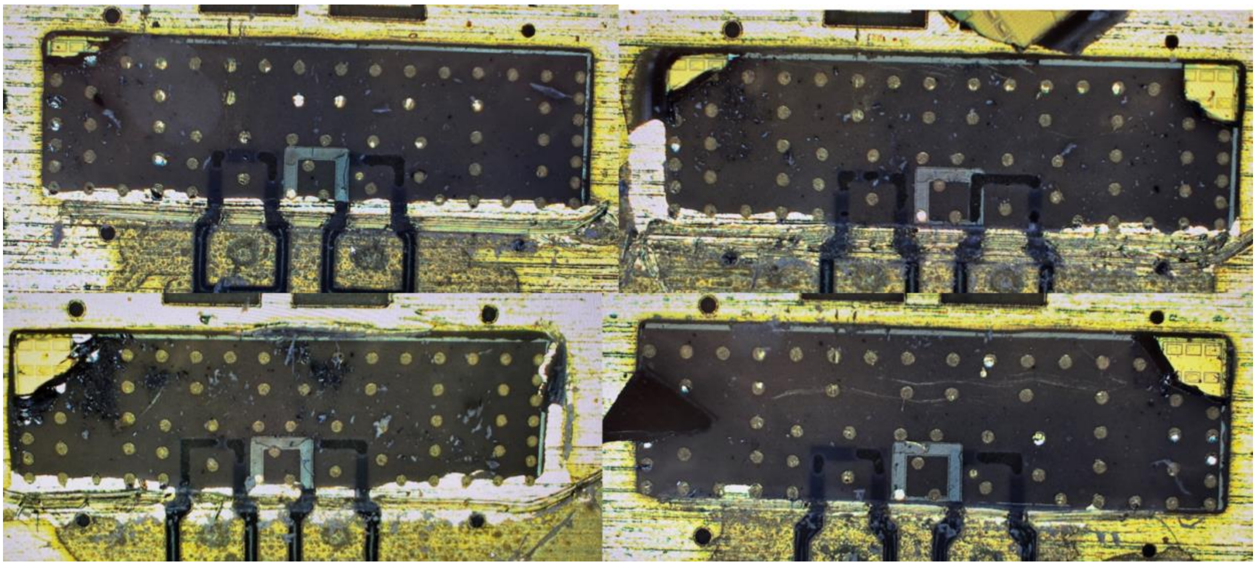


Figure 13, Shows the substrate with underfill applied

6. Discussion

This section presents an analysis of the results, highlighting key findings, addressing any unexpected outcomes, and offering potential explanations based on theoretical and practical considerations.

6.1 C4 flip chip

This section reviews the test results for C4 flip chips, comparing those with and without underfill in terms of electrical resistance, mechanical strength, and cross-section analysis to assess their reliability under temperature cycling.

6.1.1 Daisy chain

The results from measuring the resistance through the daisy chain on the chips without underfill show that the resistance was within the acceptable range specified by the manufacturer, which was 4–5 ohms. This indicates that the assembly was done correctly. It only took 250 thermal cycles before all the chips without underfill had lost their daisy chain connection. As seen in the results for the assembled chips with underfill, the resistance in the daisy chain was highest before the temperature cycling began and then decreased slightly over the course of the test. This outcome was unexpected, as it contradicts theoretical expectations. According to theory, the difference in thermal expansion coefficients between the chip and the substrate should create mechanical stress in the solder balls, gradually leading to cracks forming and thereby increasing the daisy-chain resistance.

However, the observed decrease in resistance was likely due to human error rather than an actual reduction in resistance. The measurements were performed using a multimeter with two metal probes that were manually placed on small connection pads on the substrate to complete the circuit. These pads were small and difficult to probe accurately, introducing measurement uncertainty. Additionally, the metal probes caused small dents in the contact surfaces that deepened with repeated measurements. This likely improved the contact between the probe and the pad over time, resulting in slightly lower measured resistance values with each measurement.

A test was considered to evaluate the accuracy of the multimeter and to determine how much inaccuracy was due to the operator versus the device itself. However, it was decided not to perform this test as it was deemed unnecessary. This is because the goal of the temperature cycling test was not to determine exactly how the resistance changes for every thermal cycle but rather if there would be any large changes in resistance and if the circuit would be broken.

Another reason why the exact value of the resistance is not as important as just seeing if the circuit breaks or not is the fact that the daisy chain only passes through two bumps on each corner of the chip. If the goal was to find out exactly how the resistance changes due to temperature cycling, having a more precise method for measuring would not be enough. Instead, a substrate and chip prepared with a daisy chain that passes through every bump combined with a more accurate way of measuring would be optimal. However, the equipment used for this project worked well considering what we wanted to investigate.

6.1.2 Shear test C4 flip chip

The shear tests performed on the C4 chips in this project showed clearly differences in mechanical strength between chips with and without underfill, both before and after temperature cycling. The results confirm the theory that underfill is an important part in a flip chip assembly to ensure mechanical stability.

The first measurement, before the temperature cycling had begun, showed that a chip with underfill could withstand significant higher shear force than a chip without underfill. The machine could only apply a force equivalent of 100kg which was not enough to push the chip with underfill of the substrate. Since the temperature cycling did not degrade the chips with underfill enough for the machine to be able to break the bond between chip and substrate we can’t know exactly how much force it could withstand. But the results still show a massive increase in mechanical stability thanks to the underfill. Only one chip with underfill broke and it was the chip that shattered. This means that the adhesion between chip and substrate was stronger than the chip itself.

The chips without underfill broke during the first shear test and were able to withstand an average force of 22.3 kg. The connections degraded severely during temperature cycling, and after 1000 cycles, the average shear strength had dropped to around 2 kg. Two of the chips even detached from the substrate solely due to the temperature fluctuations. This deterioration aligns with known material properties, where differences in thermal expansion coefficients between the chip and substrate cause repeated stress as the temperature fluctuates, leading to crack formation in the bumps and ultimately to failure.

6.1.3 Cross section C4 flip chip

The cross section of the C4 flip chip gave good insight into the solder joints quality and enabled the underfill under the middle of the chip to be examined. It was confirmed that the bumps had been lined up properly with the connection pads on the substrate. The shapes of the bumps shows that they have collapsed as expected indicating that the reflow process had worked well.

One surprising observation was the presence of voids in the underfill under one chip. The voids are areas under the chip that has not been filled by underfill. These voids weaken the mechanical stability and can form due to different reasons such as the substrate having a to low temperature when applying the underfill, to low standoff or pitch or not applying the underfill smoothly and therefor trapping air under the chip. Another possible reason is the fact that we did not clean the residue flux from the assembly before applying the underfill. If flux residues are left it may evaporate in the reflow process and create gas bubbles in the underfill. The voids were only found in one out of 8 samples indicating the manual application method to be the reason of the voids. The remaining cross section showed no sign of voids further indicating that the process parameters and material properties is sufficient.

When the temperature cycling had reached 1000 cycles, and all chips had been shear tested there were only one chip with underfill that were destroyed. We made cross sections in 4 chips with underfill after temperature cycling to see if anything had changed. We found no cracks or other deformations. This together with the fact that the resistance was not affected by the temperature cycling show how effective the underfill had been.

6.2 Au- stud bumps

This section reviews the test results for Au-stud bumps chips, comparing those with and without underfill in terms of mechanical strength, and images to assess their reliability under temperature cycling. It is important to note that the complications were expected, as the material used in this test does not meet manufacturing standards.

6.2.1 Height measurement

After the Au-stud bump chips were assembled using thermocompression, several complications appeared. It was unclear how much the bumps had been compressed and how well the adhesion between the chip and the bumps had been achieved. As a result, the height of all chips had to be measured. The intended stand-off (the gap between the chip and the substrate) was 15 µm, but it was measured to be approximately 20 µm. This suggests that the thermocompression process was suboptimal, which may influence the later results. Nevertheless, the chip height was relatively uniform, with only a 1 µm difference between the highest and lowest corners on average.

6.2.2 Underfill

The underfill process also had some complications. There were problems with getting the underfill to properly flow beneath the chip. This may have been due to a couple of reasons. The first issue, which was visually observed, was that the underfill had strong adhesion to the substrate. Stronger than the capillary force between the chip and the substrate. This meant that a lot of underfill had to be applied before it was certain that it had filled the entire area beneath the chip. This was somewhat difficult to verify due to the very small size of the chips. The entire first substrate, containing 10 chips, was processed this way. On the second substrate, it proved more efficient to apply the underfill in the small recess in the substrate and try to guide the underfill to the correct position. This was an easier and more efficient method.

Another issue is that the standoff height was too small for this type of underfill. According to the underfill instructions (Henkel, 2024), the minimum optimal standoff height is 30 µm. The standoff for this chip was as mentioned above around 20µm. The problem with going against the instructions is that the underfill may suffer from high viscosity, large particle size, or a combination of the two.

6.2.3 Shear test

The shear test results show values that contradict the theory of the chips deteriorating due to temperature cycling, especially those with underfill. The chips should not be able to withstand more weight as temperature cycling progresses. Their mechanical stability is expected to decrease over time. The reason the chips tested with underfill showed increased values is due to the complications mentioned above. The underfill was applied to the chips with too much variation. The chips tested at 0 cycles were the first ones to have underfill applied. The applying technique improved during the process, which likely explains why the chips tested after 400 cycles withstood the most.

Another possible explanation is suboptimal assembly during the thermocompression process, which likely had some effect. However, the fact that the chips without underfill showed a declining trend contradicts this theory. It suggests that while poor assembly may have contributed, the main issue lies with the underfill.

6.2.4 Images after shear test

The chip without underfill shows poor adhesion between the bumps and the chip itself. One likely reason for this is suboptimal thermocompression. The solder bumps adhered well to the substrate, indicating significantly stronger adhesion on that side. This difference is because the bumps were applied directly to the substrate, whereas the chip was attached using thermocompression. Further suggest that the compression was not optimal during assembly.

The chip with underfill has the same issues. The underfill clearly has stronger adhesion to the substrate than the chip surface.

6.3 Further development

While this thesis provided valuable insights into the reliability and mechanical performance of flip-chip assemblies with and without underfill, several areas remain open for further exploration. Future work could focus on automating the underfill application process to improve consistency and reduce void formation. Additionally, expanding the sample size and incorporating more precise measurement tools, such as X-ray inspection or advanced electrical testing equipment, would enhance the reliability of the results. Investigating alternative underfill materials optimized for lower stand-off heights could also yield improved performance in miniaturized assemblies. Finally, repeating the tests under different environmental conditions or incorporating more extensive thermal cycling profiles would provide a deeper understanding of long-term reliability.

7. Conclusion

This study has investigated the reliability and mechanical stability of two flip-chip assembly methods: C4 solder bumps and Au-stud bumps, with and without the use of underfill. The results show the importance of underfill when considering mechanical stability and durability under temperature cycling. For the C4 chips with underfill the electrical connectivity did not change, in contrast the chips without underfill failed after the first step. The shear test had similar results. The underfill chips withstood more weight than the machine could output. Were as the ones without had a substantial drop off. Cross-sectional analyses showed proper bump collapse and alignment, with only minimal void formation in underfill, suggesting that the manual application method was effective but could be improved to reduce defects. The Au-stud bump assemblies experienced some complications, which was expected since they did not use manufacturing-level parts. Nevertheless, the use of underfill also improved the mechanical robustness of Au-stud assemblies. Overall, the study highlights the importance of underfill in terms of mechanical stability and reliability, especially under temperature stress.

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Appendix

Table 3 Height of the Au-stud bump chips measured.

Underfill:A,B	VÖ	VN	HÖ	HN	Average
A1	130	128	127	127	128
A2	131	130	128	127	129
A3	132	132	129	129	130.5
A4	128	127	128	126	127.25
A5	133	131	130	130	131
A6	128	128	127	127	127.5
A7	132	131	130	130	130.75
A8	129	133	126	128	129
A9	134	133	130	130	131.75
A10	129	128	127	128	128
Average:A	130.6	130.1	128.2	128.2	129.275
B1	130	130	126	126	128
B2	131	128	130	127	129
B3	131	129	129	129	129.5
B4	129	127	129	127	128
B5	127	128	125	125	126.25
B6	129	131	131	131	130.5
B7	128	128	130	130	129
B8	130	131	128	130	129.75
B9	129	129	128	127	128.25
B10	129	131	128	132	130
Average:B	129.3	129.2	128.4	128.4	128.825
C1	131	128	131	129	129.75
C2	131	128	132	130	130.25
C3	131	129	131	127	129.5
C4	129	128	130	129	129
C5	129	127	132	128	129
C6	131	129	131	130	130.25
C7	130	129	131	130	130
C8	129	130	128	131	129.5
C9	130	132	129	132	130.75
C10	128	130	129	131	129.5
Average:C	129.9	129	130.4	129.7	129.75
D1	131	128	130	126	128.75
D2	132	128	131	127	129.5
D3	128	127	127	128	127.5
D4	132	131	132	130	131.25
D5	129	128	131	129	129.25
D6	128	127	128	127	127.5
D7	128	130	130	131	129.75
D8	128	131	129	130	129.5
D9	127	129	129	128	128.25
D10	129	130	132	131	130.5
Average:D	129.2	128.9	129.9	128.7	129.175
	129.75	129.3	129.225	128.75	129.25625

Table 4 Shear test of the Au-stud bump chips in Kg.

Skjuvtets(Kg)	0 cykler	130 cykler	400 cykler	650 cykler	
A1			7.9177		
A2			7.619		
A3			5.6766		
A4			9.78		
A5			6.9462		
A6				5.1253	
A7				5.5763	
A8				4.7543	
A9				5.2555	
A10				5.2483	
Average:A			7.5879	5.19194	6.38992
B1	4,6338*				
B2	3.9239				
B3	6.6321				
B4	4.9808				
B5	5.2512				
B6		5.7691			
B7		5.9513			
B8		6.6227			
B9		4.6796			
B10		7.0171			
Average:B	5.197	6.00796			5.60248
C1	2.9483				
C2	2.1554				
C3	3.0463				
C4	3.6195				
C5	3.2055				
C6		2.7969			
C7		2.9546			
C8		3.1975			
C9		3.0698			
C10		2.4718			
Average:C	2.995	2.89812			2.94656
D1			2.5056		
D2			1.2022		
D3			1.7973		
D4			2.1138		
D5			3.0142		
D6				1.3878	
D7				1.7304	
D8				1.6669	
D9				2.0189	
D10				1.4916	
Average:D			2.12662	1.65912	1.89287

Table 5 C4 chip daisy-chain without underfill.

Chip without underfill					
5A	4.7	No Contact	No Contact	No Contact	No Contact
5B	5	No Contact	No Contact	No Contact	No Contact
5C	4.8	No Contact	No Contact	No Contact	No Contact
5D	4.9	No Contact	No Contact	No Contact	No Contact
6A	5	No Contact	No Contact	No Contact	Destroyed
6B	4.9	No Contact	No Contact	No Contact	Destroyed
6C	4.8	No Contact	No Contact	No Contact	Destroyed
6D	4.9	No Contact	No Contact	No Contact	Destroyed
7A	5	No Contact	No Contact	Destroyed	Destroyed
7B	4.9	No Contact	No Contact	Destroyed	Destroyed
7C	4.8	No Contact	No Contact	Destroyed	Destroyed
7D	5.1	No Contact	No Contact	Destroyed	Destroyed
8A	4.8	No Contact	Destroyed	Destroyed	Destroyed
8B	4.8	No Contact	Destroyed	Destroyed	Destroyed
8C	4.7	No Contact	Destroyed	Destroyed	Destroyed
Average without	4.86875	0	0	0	0
Cycles	0	250	500	750	1000

Table 6 C4 chip daisy-chain with underfill.

Chip with underfill	Measured ohm 20/3	Measured ohm 2/4	Measured ohm 14/4	Measured ohm 20/6	Measured ohm 20/7
			(4A-4D) Sheer tested last time.	(4A-4D) Sheer tested	4D chip was broken
1A	4.8	4.3	4.5	4.1	4.0
1B	4.6	4.3	4.3	4.1	4.0
1C	4.7	4.5	4.4	4.1	4.0
1D	5.1	4.6	4.3	4.5	4.0
2A	5.2	4.4	4.2	4.2	4.0
2B	4.8	4.4	4.2	4.3	4.1
2C	4.6	4.1	4.2	4.0	4.3
2D	4.8	4.5	4.3	4.0	4.2
3A	4.8	4.1	4.3	4.1	4.1
3B	4.5	4.6	4.2	4.0	4.1
3C	4.8	4.2	4.3	4.0	4.0
3D	4.8	4.1	4.3	4.0	4.2
4A	5.0	4.0	4.3	4.3	4.1
4B	4.6	4.1	4.3	4.0	4.1
4C	4.8	4.0	4.4	4.3	4.0
4D	5.0	4.2	4.6	4.4	*0,7
Average Underfill	4.806	4.275	4.319	4.150	4.080
Cycles	0	250	500	750	1000

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