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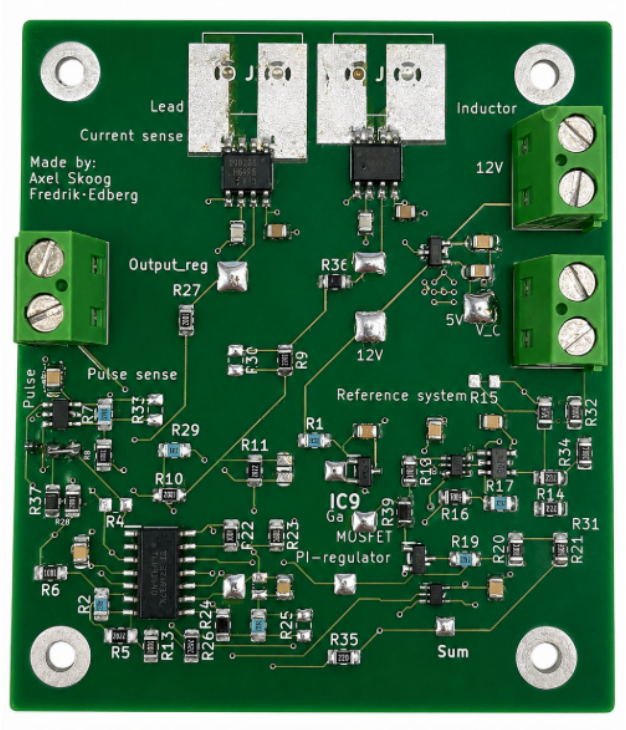

Analogue Controlled Active Power Filter for Pulsating Loads

Master's thesis in Sustainable Electric Power Engineering and Electromobility

FREDRIK EDBERG AND AXEL SKOOG

DEPARTMENT OF ELECTRIC POWER ENGINEERING

CHALMERS UNIVERSITY OF TECHNOLOGY
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Supervisor: David Prytz Arcombe, SAAB and Lowe Blank, SAAB
Examiner: Torbjörn Thiringer, Electric Power Engineering

Master's Thesis 2026
Department of Electric Power Engineering
Division of Electrical Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: The final design of the APF's regulation PCB.

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Abstract

This master thesis demonstrates an analogue controlled active power filtration for pulsing load used in radar systems. The main tasks of this thesis was to simulate, design, build and verify a regulation control system on a printed circuit board. This regulation card was connected with a separate power card and should be able to handle 40 A pulsed loads without any critical drop in output voltage. The active power filter together with the control card was simulated in LTspice before component selection and a schematic and a layout was designed in KiCad. Then the active power filter with the regulation control system was constructed and verified to make sure it works as intended.

The active power filter managed to maintain the output voltage during pulses within a certain limit, dropping to 27.1 V, resulting in a viable solution for handling pulsating loads. However, the duty cycle specified of 10% had to be reduced to 9.1% in order to maintain steady state operation due to high transient currents up to 150 A during 40 A pulses. Improvements, such as a less aggressive control loop and dynamic limits, needs to be implemented to achieve stable operation at higher duty cycle.

Keywords: APF, Pulsed loads, Control, Regulation, PCB, filter, power, design.

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We would like to express the deepest of gratitude towards our supervisors David Prytz Arcombe, Lowe Blank, Jacob Viktorsson and Per Lundberg. They have provided us with guidance when it was needed and a lot of patience. They have help us through the bureaucratic jungle that is Saab AB and supported us tirelessly though out the project. We also want to show gratitude toward Leonard Jegerås and Mattias Linnér, for they have help us solder everything correctly so that this project could be handed in before the deadline.

And of course we would like to express our deepest gratitude towards Torbjörn Thiringer, who has helped, guided and always set us towards the correct path along this journey.

Fredrik Edberg and Axel Skoog, Gothenburg, May 2026

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

RF	Radio Frequency
PPF	Passive Power Filter
APF	Active Power Filter
AESA	Active Electronically Scanned Array
GaN	Gallium-Nitride
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PI	Proportional-Integral
PSU	Power Supply Unit
PCB	Printed Circuit Board
IC	Integrated Circuit
EMI	Electromagnetic Interference

Contents

1

Introduction

1.1 Background

The power electronic industry is always striving for better performance, smaller components, and lower cost. One of the bigger challenges in the power electronic industry is to deliver power to a radar, where the loads are delivered in pulses putting extra challenges in designing the power supply. The radar in question is an Active Electronically Scanned Array (AESA) that sends out repeatedly pulsed Radio Frequency (RF) towards the intended target. The receiver of the radar collects the reflected RF waves coming back from the target. This gives the AESA time to collect the signal and use that data to determine the speed, position and range to the target. Due to the fact that the AESA sends out a wide transmitter pulses repeatedly strains the system with pulsed loads.

To mitigate the pulsed loads effect on the power supply it is common to place different type of filters. There are two ways to go about choosing the filters, doing a Passive Power Filter (PPF) or an Active Power Filter (APF). PPF is a filter that is composed of passive components places at the input and output, the components are heavy and big and in a radar setting, especially in the aviation where weight management is crucial. So the other option is using an APF, where active switching filters the input and gives a more even output. Since the filter switches, it can use more of its components compared to a passive filter, and therefore lower the volume of the capacitor.

The more technology has evolved, the need for smaller devices increased. Due to the fact that higher switching frequencies call for smaller components, since there is less energy per switching cycle, capacitors can be smaller and a lower inductance needed, means smaller inductors. Since semiconductor and semiconductor material is a giant research area, a replacement for the widely used material silicon is always researched, is case of shortages material-wise or due to political reason. Then, because of these reasons, Gallium-Nitride (GaN) transistors have been developed, which are used in this project. To control these switches the feedback and regulation needs to be as fast as the switches. Since this is the case, digital regulation is slower since it has calculation steps in its regulation. Therefore analogue regulation is used where electronic signals control the switching and therefore it will be faster.

1.2 Previous work

In a previous work "Digitally Controlled Active Power Filter for AESA Radar" a digital APF was constructed and tested so that a physically larger PPF could be replaced with a smaller digital solution. The conclusion of that project was that an APF together with a PPF and a DC/DC-converter could get an undisturbed power supply. With the digital component creating the possibility of an adjusting system.

In the present work, an analogue solution to an APF is explored. This is due to the half-bridge used, LMG2100R026VBNR, where the switching speed increase up to 1.2 MHz. This makes a digital solution hard due to the calculation steps it needs to go through to regulate. Therefore analogue regulation will be explored where a separate analogue PCB will be designed and constructed and then connected to an already exciting PCB with the power part.

1.3 Purpose

The aim of this thesis is to design, build and verify an APF with analogue regulation that is able to maintain the output voltage during high frequency current pulses.

1.4 Scope

In this master thesis, the local point will be on an analogue controlled APF which will be simulated, designed and constructed into a hardware prototype. The main goal is to see if analogue control of a half-bridge at high switching frequency is possible, and if it can replace a PPF. The size of the test-card is not of importance.

The half-bridge and the power stage has already been chosen and constructed. This is to limit the size of the master thesis. A duty cycle of 10% has been chosen for the pulses.

2

Theory

2.1 DC-DC converters

A switching DC-DC converter takes an unregulated DC supply voltage that has ripples and difference in magnitudes and converts into a controlled DC output at a specified level. There are three different basic types of converters, the step-down converter (buck), the step-up converter (boost) and the step-down/step-up converter (buck-boost). These different types of converters transfers the voltage from one level to another level.

2.1.1 Buck converter

The buck converter takes supply DC-voltage value, V_d and converts it to a lower voltage value.

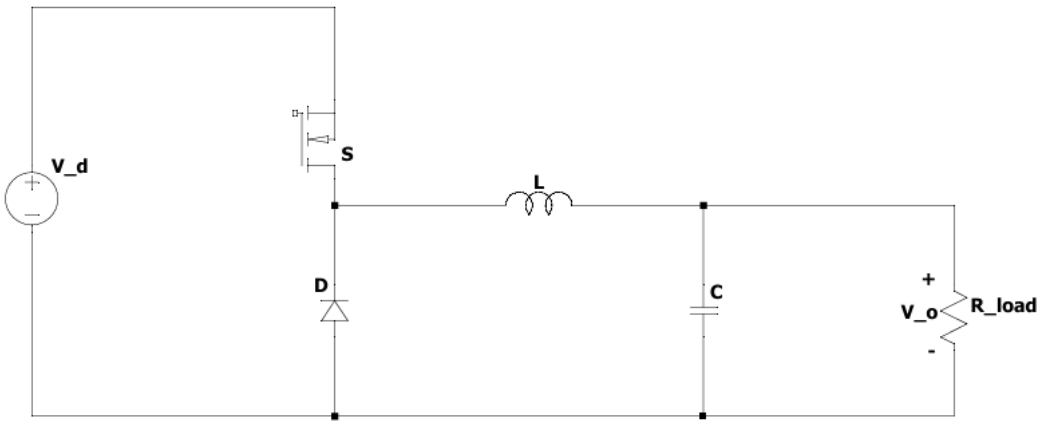

Figure 2.1: Buck converter.

In Fig. 2.1 There is a DC-supply voltage V_d, a switch (S) connected to that supply voltage that goes down to a diode (D) and an inductor (L) with a capacitor (C) connected in parallel. At the end it is connected to a load that has a output voltage (V_o). In this case the switch has two states, on and off, and based on that, two equivalent circuits.

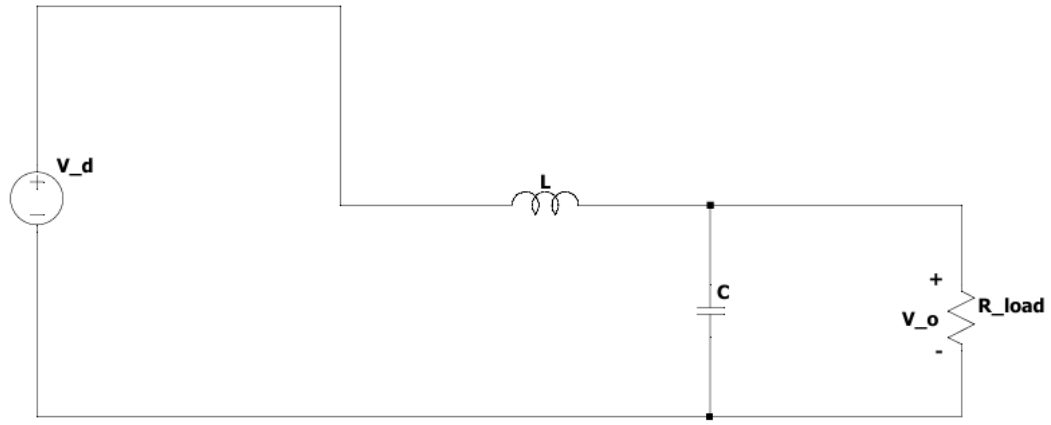

Figure 2.2: Buck converter with switch turned on.

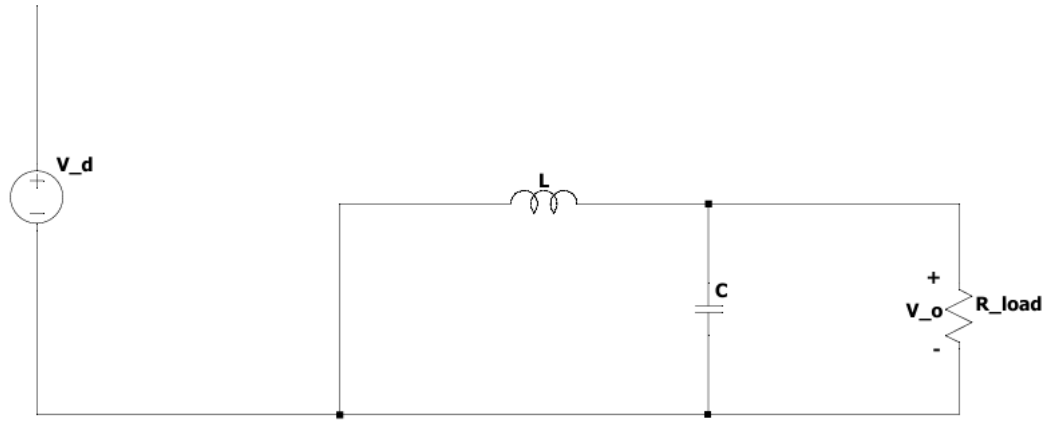

Figure 2.3: Buck converter with switch turned off.

The first case, Fig. 2.2 is when the switch is on. The supply voltage will be in series with the inductor where current will flow and charge the capacitor and supply the load. The second case is when the switch is turned off. This case is also called freewheeling, as can be seen in Fig. 2.3 where the inductor still has current and this current passed through the diode instead back to the inductor. This continues until the switch is turned on again and then the process repeats itself.

The duty cycle is a fraction of a switching period of when the switch is turned on

$$D = \frac{t_{on}}{T_{sw}} \tag{2.1}$$

where D is the duty cycle, t_{on} is the time when the switch is turned on, T_{sw} is the time period of the switching. Continuous conduction mode (CCM) is when the inductor current never reaches zero and is always conducting. This conduction mode

is considered in this work. Over one switching period in steady state the voltage over the inductor must be zero.

$$V_L = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_L(t)\, dt = \frac{1}{T_{sw}} \int_0^{t_{on}} (V_d - V_o)\, dt + \frac{1}{T_{sw}} \int_{t_{on}}^{T_{sw}} V_d\, dt = 0 \tag{2.2}$$

where V_L is the average inductor voltage, V_d is the input voltage, V_o is the load voltage and the last variable t_{off} which is the time of a period when the switch is turned off. Analysing (2.2) further it yields

$$(V_d - V_o)t_{on} + V_d t_{off} = 0 \tag{2.3}$$

Using (2.1) and (2.3) a simplified expression of the input, output voltage using the duty cycle

$$V_o = DV_d \tag{2.4}$$

this can be visualised by showing the inductor current and voltage over time.

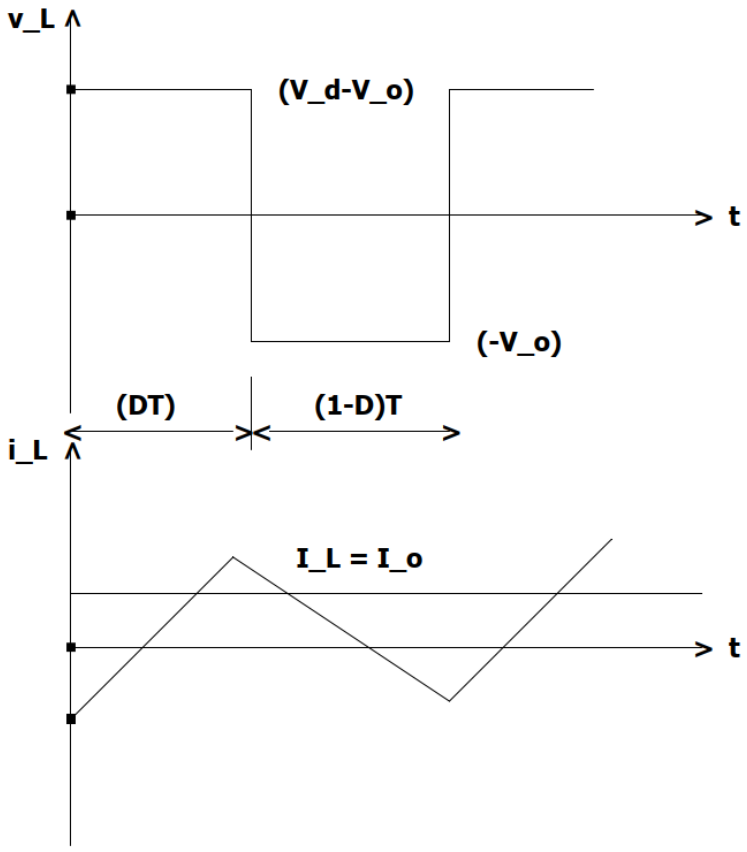

Figure 2.4: Buck converter inductor voltage and current for one period.

From Fig. 2.4, assuming no losses in the equation the power input and output should be equal.

$$P_{in} = V_d I_d = P_{out} = V_o I_o \tag{2.5}$$

where P_{out} is the output power, P_{in} is the input power and thus,

$$I_o = \frac{I_d}{D} \tag{2.6}$$

This gives a relation between the currents [1].

2.1.2 Boost converter

A boost converter takes low supply voltage and converters it to a higher output voltage, the basic boost converter has the following schematic,

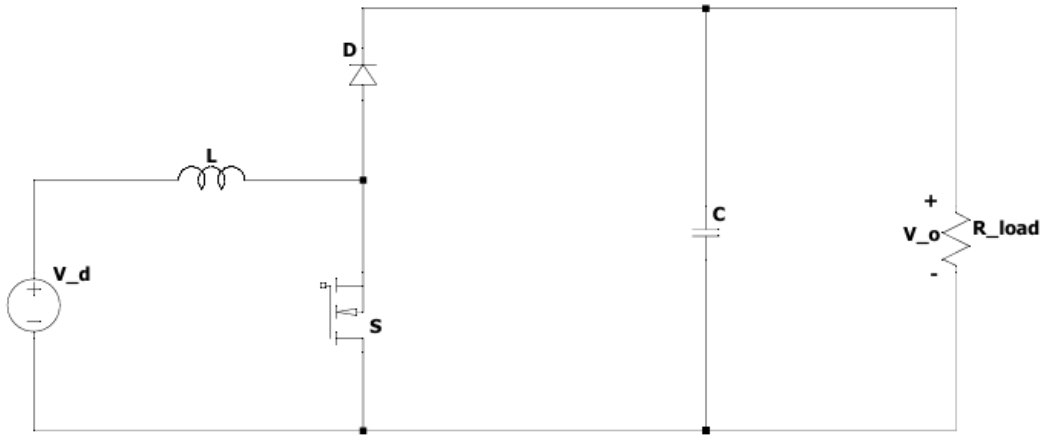

Figure 2.5: Boost converter.

where an inductor (L) is put in series with a voltage source (V_d), thereafter a diode (D) and a switch (S) are placed in next to the inductor. Thereafter a capacitor (C) in parallel with the load (R_{load}) where the voltage over the load is the output voltage (V_o). The capacitor voltage and output voltage are always equal or greater than the input voltage, this is due to the switching cycle of the switch. There are two equivalent circuits that are created when the switch is turned on and off. When the switch is turned on the inductor gets energized by the supply voltage.

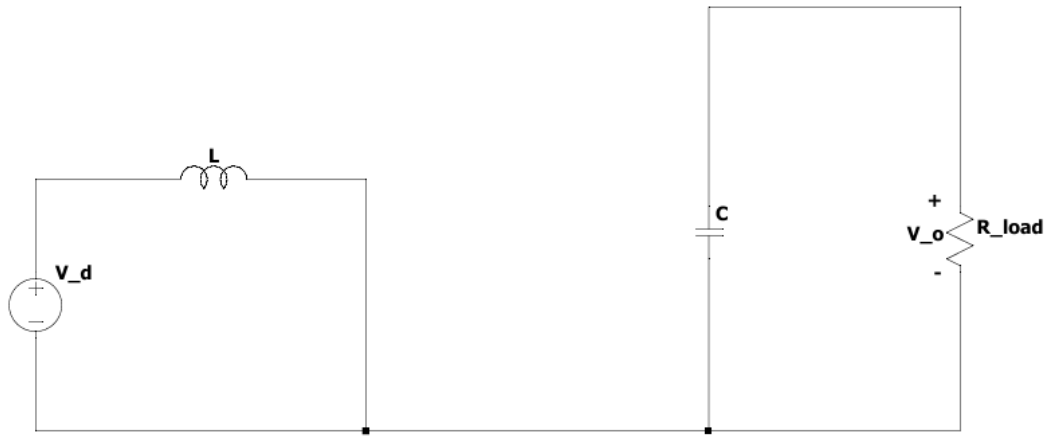

Figure 2.6: Boost converter when switch is turned on.

As seen in Fig. 2.6, the only way the output gets supplied is via the capacitor since the diode is blocking the other way. When the switch is turned off, the equivalent circuit in Fig. 2.7

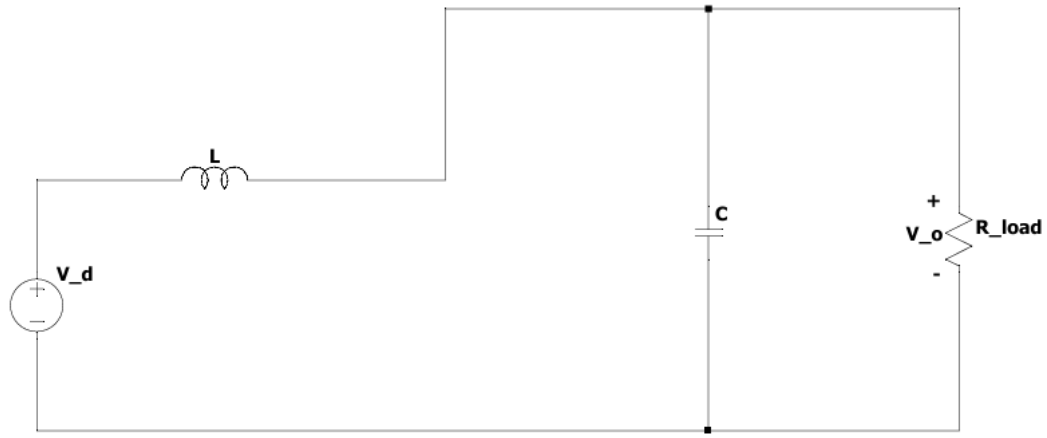

Figure 2.7: Boost converter when switch is turned off.

is used. Now the inductor de-energizes and the diode will conduct and the voltage over the inductor is added to the supply voltage. This means that the inductor and supply charges the capacitor and load. This happens over one switching cycle and these patterns repeats themselves. Using the equation of duty cycle from (2.1) and assuming CCM the equation for the voltage over the inductor for one switching period is also zero

$$V_L = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_L(t)\, dt = \frac{1}{T_{sw}} \int_0^{t_{on}} V_d\, dt + \frac{1}{T_{sw}} \int_{t_{on}}^{T_{sw}} (V_d - V_o)\, dt = 0 \qquad (2.7)$$

evaluating (2.7) which can be simplified to

$$V_d t_{on} + (V_d - V_o) t_{off} = 0 \tag{2.8}$$

This yields two plots that are inductor voltage and current plotted over time.

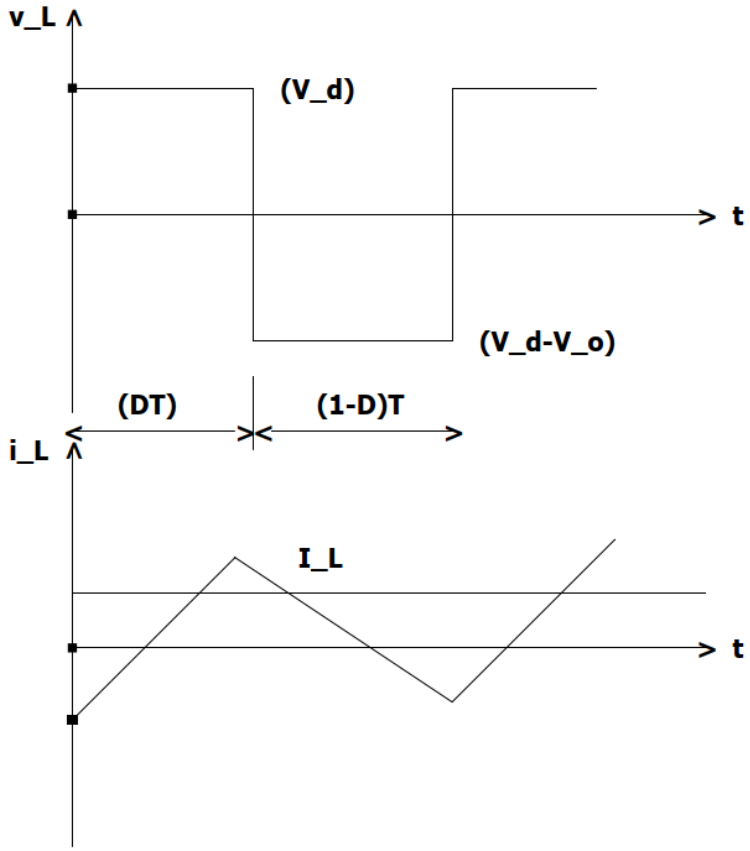

Figure 2.8: Boost converter inductor voltage and current for one period.

using (2.1) and (2.8) the relation between supply voltage and output voltage is

$$V_o = \frac{1}{1 - D} V_d \tag{2.9}$$

As seen in Fig. 2.8 if the two areas, 1 and 2 are the same. This is true if there are no losses and 2.5 is true if the current becomes,

$$I_o = (1 - D) I_d \tag{2.10}$$

In the ideal world, the voltage in (2.9) can be boosted infinitely if D is chosen to be as close to one as possible. In reality due to parasitic element and component restrictions there is a limit of how much it can be boosted [1].

2.1.3 Buck-Boost converter

The buck-boost converter takes a supply voltage and can either convert it to a higher or lower output voltage, the basic buck-boost converter has the following schematic,

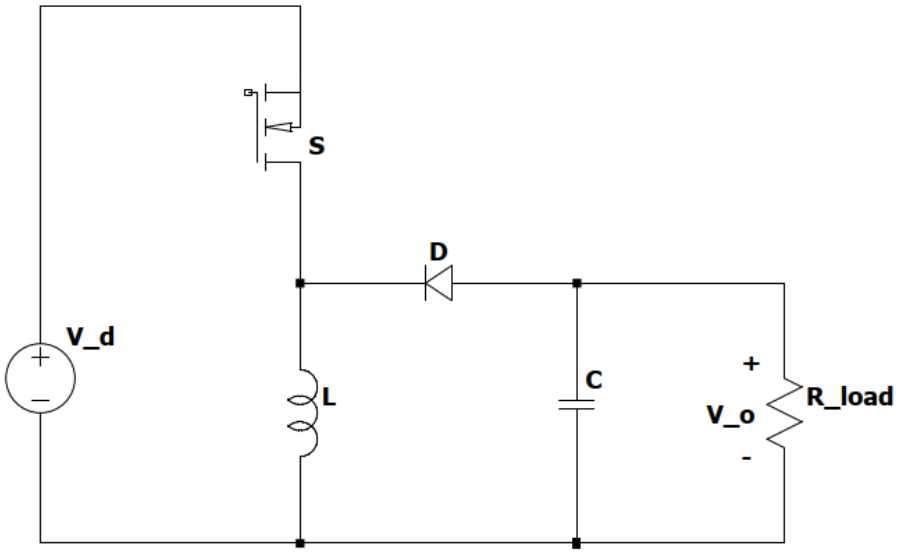

Figure 2.9: Buck-Boost converter.

where the supply voltage (V_d) lays in parallel with the switch (S). The switch branches out to a diode (D) that is faced against the input current and an inductor (L). In parallel with the switch and the inductor there is an output capacitor (C) and a load (R_{load}). There are two states in the buck-boost converter, when the switch is turned on and when the switch is turned off. The following schematic shows the equivalent circuit for when the buck-boost converter is turned on.

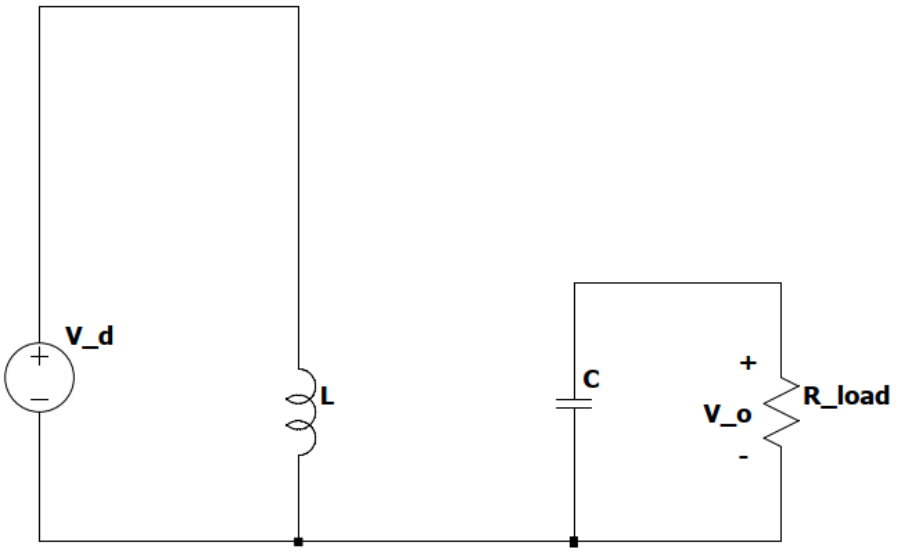

Figure 2.10: Buck-Boost when switch is turned on.

When the switch is on the supply energizes the inductor and the the diode blocks any current going through to the load, causing the load to be charged by the output

capacitor. When the switch is turned off, the following equivalent circuit can be used,

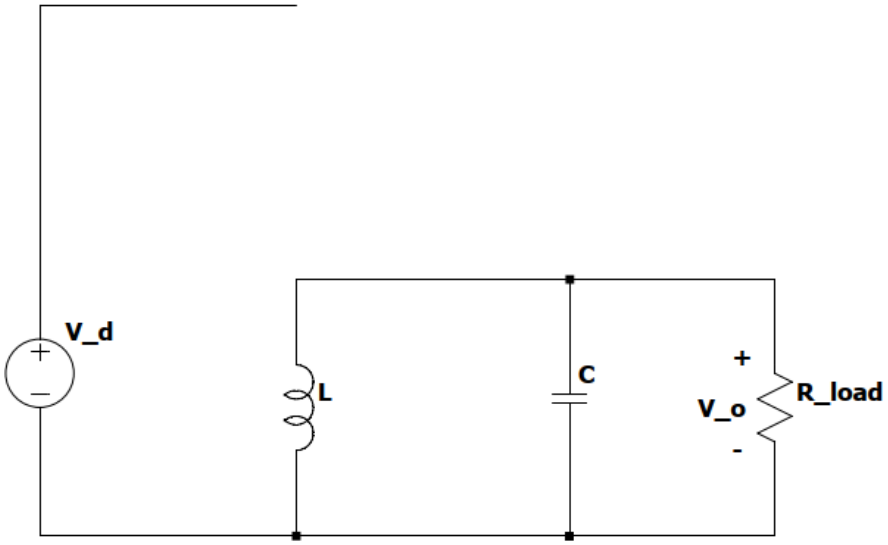

Figure 2.11: Buck-Boost when switch is turned off.

where the supply voltage is cut off from the rest of the circuit and the inductor de-energizes and the inductor current conducts and charges the capacitor and the load. The formula for the inductor voltage in CCM is expressed with an integral over one switching period that must be equal to zero,

$$V_L = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_L(t)\, dt = \frac{1}{T_{sw}} \int_0^{t_{on}} (V_d - V_o)\, dt + \frac{1}{T_{sw}} \int_{t_{on}}^{T_{sw}} (-V_o)\, dt = 0 \qquad (2.11)$$

using (2.11) the following relation is found

$$(V_d - V_o)t_{on} = (-V_o)t_{off} \qquad (2.12)$$

this yields two plots that show inductor current and voltage over one period.

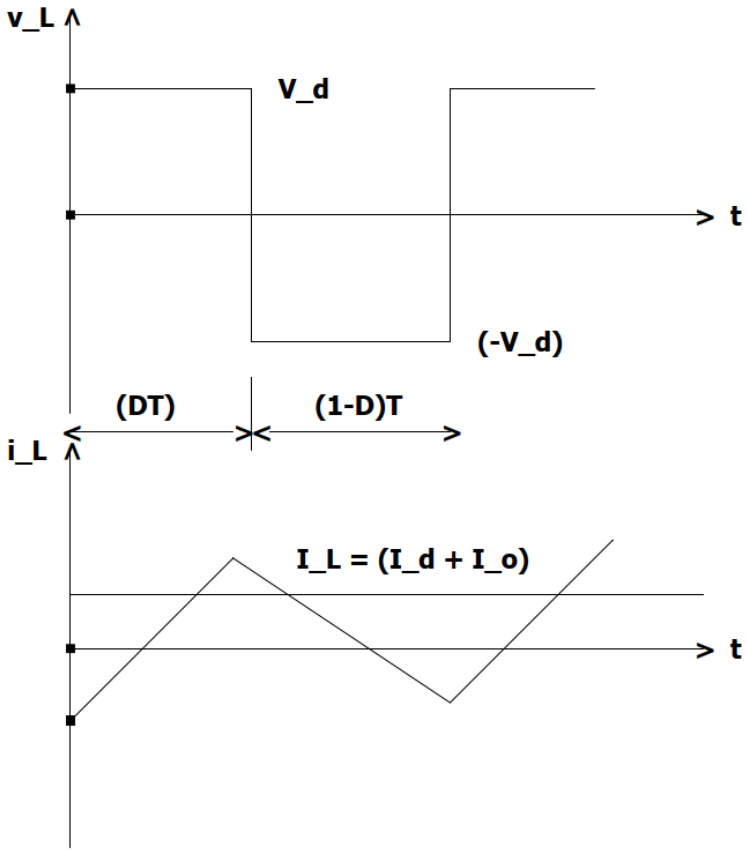

Figure 2.12: Buck-boost inductor voltage and current for one period.

using (2.1) and (2.12) they can be combined and the the relation between supply and output voltage is

$$V_o = \frac{D}{1-D} V_d \tag{2.13}$$

If the system is perfectly ideal and there are no losses, the two areas in Fig. 2.12 must be equal and 2.5 is true, a relation of the input and output current for the buck-boost converter can be extracted

$$I_o = \frac{1-D}{D} I_d \tag{2.14}$$

In a real world, the parasitic elements of the different components cause more losses and the equations above need to take in to account that [1].

2.2 Gallium-Nitride Transistor

For almost 60 years, the silicon Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been the cheapest to produce and has therefore dominated the market. In resent years, the use of GaN transistor grown. Over the last couple of years if has replaced the almost monopoly of the silicon power MOSFET. The differences of the GaN and the silicon transistors start with the molecular build

up, the GaN transistor is a wide bandgap semiconductor, with a higher bandgap the maximum electric field is higher. With a higher maximum electric field, the drift region becomes thinner and in theory the on-resistance should become smaller, giving the GaN transistors lesser conduction losses than it's silicon counter parts. The GaN transistor also switches significantly faster than the silicon transistor and that is due to its structure. There are four different layers inside, silicon substrate, buffer layers, GaN layer, and AlGaN layers, this is visualized in Fig.

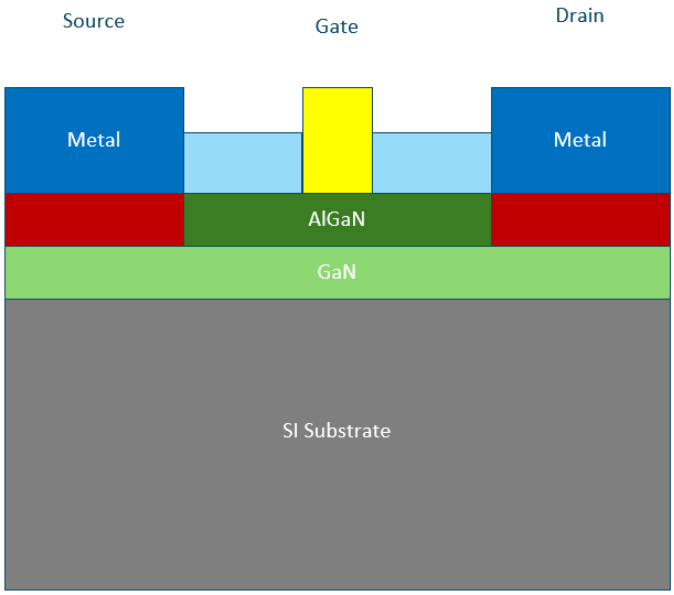

Figure 2.13: Structural layout GaN transistor.

The fact that AlGaN has higher polarization than GaN, meaning positive charges at the interface cause free electron to form at the AlGaN/GaN interface as shown in Fig 2.14.

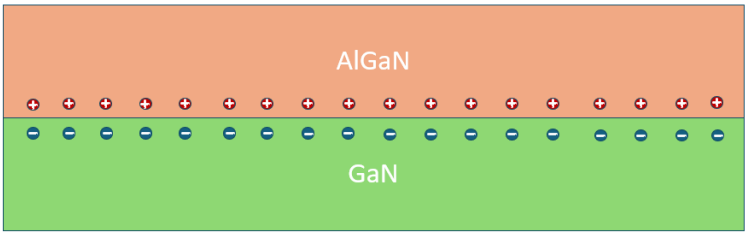

Figure 2.14: Polarization AlGaN and GaN interface.

The free electrons form a two dimension electron gas, that has a much higher electron mobility compared to electron in a Si structure. The higher electro mobility is the reason the GaN transistor switches significantly faster [2]. The GaN is also projected to be cheaper than the silicon MOSFET where 50% of the cost for a silicon MOSFET comes from the package [3].

2.3 Proportional-Integral Controller

The proportional-integral-derivative (PI) controller is a way to control different variables, such as temperatures, changes in current and voltage, humidity and everything that can be controlled. The PI controller has two parts, the proportional and the integral part that helps the controller regulate, and compensate when these variables change [4].

2.4 Regulation

There are two ways regulations can be done today, digital and analogue. Digital regulation samples a continuous signal at regular time steps to then be used in digital components that can be programmable. Programming the response has a benefit in flexibility but it also reduces the bandwidth it can operate in. At higher bandwidths, the sampling becomes too fast for the calculations required to regulate the signal, causing the system to fail to operate properly. Analogue regulation is when only electronic components use a continuos signal to determine how an output should respond to the changes from the input. It does not need any calculations when regulating meaning it can be operating at a higher bandwidth than digital regulation. But the analogue regulation is not as flexible as the digital one, where altering the code can change the programmed response [5].

2.4.1 Voltage mode regulation

In electronic regulation there are multiple ways to regulate, however current mode regulation and voltage mode regulation are the most common in DC-DC converters. The voltage mode regulation works in the following way, the output voltage is measured and is then compared to a reference signal. It is done with an operational amplifier than amplifies the error and generates a control voltage. The control voltage is compared with an voltage ramp in a comparator where the duty cycle is created. If the control signal is below the voltage ramp, the switch is turned off, if the voltage ramp is higher than the control signal the switch is turned on [6].

2.4.2 Current mode regulation

The current mode regulation measures the inductor current. This is then compared with a reference from an voltage error amplifier where it switches off when the sensed current is the same as the reference. This type of regulation uses a two-loop structure with an inner current loop and an outer voltage loop. The introduction of the inner current loop removes the inductor pole from the outer voltage loops transfer function making it more simple and easier to stabilize. This also means that it can use a higher bandwidth and have a fast transient response. If the duty cycle is above 50% there is a need for slope compensation due to the fact of sub-harmonics. The way slope compensation is done is by adding a stabilizing ramp to the signal to stabilize it and prevent sub-harmonics. There are also more subcategories in the current mode regulation. Peak current mode regulation is when the signal to turn

the switch on, occurs when a new cycle starts and when the reference value has been reached, it turns the switch off. Then there is valley-mode regulation and average-mode regulation [7].

2.4.3 Proportional

The proportional gain part in the PI controller is usually denoted as K_p. The proportional part is using the error to reduce the error. The error is determined between a set point (a reference) and a measured value. This means if the error is great the proportional output is great. Same reasoning for if the error is small, the proportional output is small. So, if K_p is large the controller will react with a larger output for an given error. The proportional part is great at reducing an error but, since it only can reduce an error and not use anything to regulate it back to the steady state value. Therefore it is usually combined with an integral part [4].

2.4.4 Integral

The integral gain part in the PI controller is usually denoted as K_i. The integral part is introduced to work to remove the error (offset) that the proportional part left and cannot by itself work away. The integral part is called that because it takes the area between the measured value and the set point overtime and sums it up and tries to remove the error. As long as there is a small error, the integral part will work to remove that error by adjusting the output of the controller. With a larger K_i the integral part becomes stronger which means it becomes faster at correcting the error, but the downside would be that it can become unsteady and can oscillate. If too low of K_i the problem would be that the response takes too long [4].

2.5 Component selection

With component selection there are certain criteria that needs to be satisfied. To select an inductor the inductance needs to be calculated,

$$v_L(t) = L\frac{di(t)}{dt} \tag{2.15}$$

where $v(t)$ is the voltage across the inductor, $i(t)$ is the current change over the inductor and L is the inductance. To decide the ripple for the inductance during steady state the following formula is used,

$$\Delta I_L = \frac{V_{supply}D}{Lf_s} \tag{2.16}$$

where D is the duty cycle, which in steady state is 50%. V_{supply} is the supply voltage and f_s is the switching frequency. For the energy consumption of the load and the energy supplied by the source,

$$E_{pulse} = P_{pulse}t_{on} = V_{out}I_{load}t_{on} \tag{2.17}$$

$$E_{supply} = V_{supply} I_{supply} t_{on} \tag{2.18}$$

the energy is based on I_{load} and I_{supply}, the load and supply current, V_{out} and V_{supply}, the output and supply voltage and duration of the pulse t_{on}. When selecting an energy storage to compensate for this loss the energy storage needs to be bigger than the energy consumed by the load. Therefore a capacitance needs to be scaled accordingly,

$$E_C = \frac{1}{2} C V_c^2 \tag{2.19}$$

where E is the energy for the capacitor, C is the capacitance and V_c is the capacitor voltage. To calculate the voltage drop that occurs in the capacitor,

$$\Delta V = \frac{I_C t_{on}}{C} \tag{2.20}$$

this formula is used to calculate the voltage drop to see if the capacitor can be recharged during t_{off}. To calculate the time to see if the capacitor can be recharged the energy lost needs to be calculated,

$$\Delta E_C = \frac{1}{2} C \left(V_c^2 - V_{c,a}^2 \right) \tag{2.21}$$

where V_c and $V_{c,a}$ are the capacitor voltages before and after the pulse. The time to recharge the capacitor is,

$$t_{charge} = \frac{\Delta E_C}{I_{L_{avg}} V_{supply}} \tag{2.22}$$

where the capacitor is charged via the average inductor current [1]. To decide the maximum temperature for both the capacitor and the inductor the data-sheet of each respective component have to be studied. Where the maximum temperature should be below 40°. The capacitor should also be able to handle above the nominal voltage due to overshoots that could occur if the regulation system is not fast enough. The inductor should also not be saturated, where the data-sheet will have that information.

3

Case set-up

3.1 System set-up

The half-bridge module is integrated in parallel to the load. The system is simplified to the schematic presented with measurement points in Fig. 3.1.

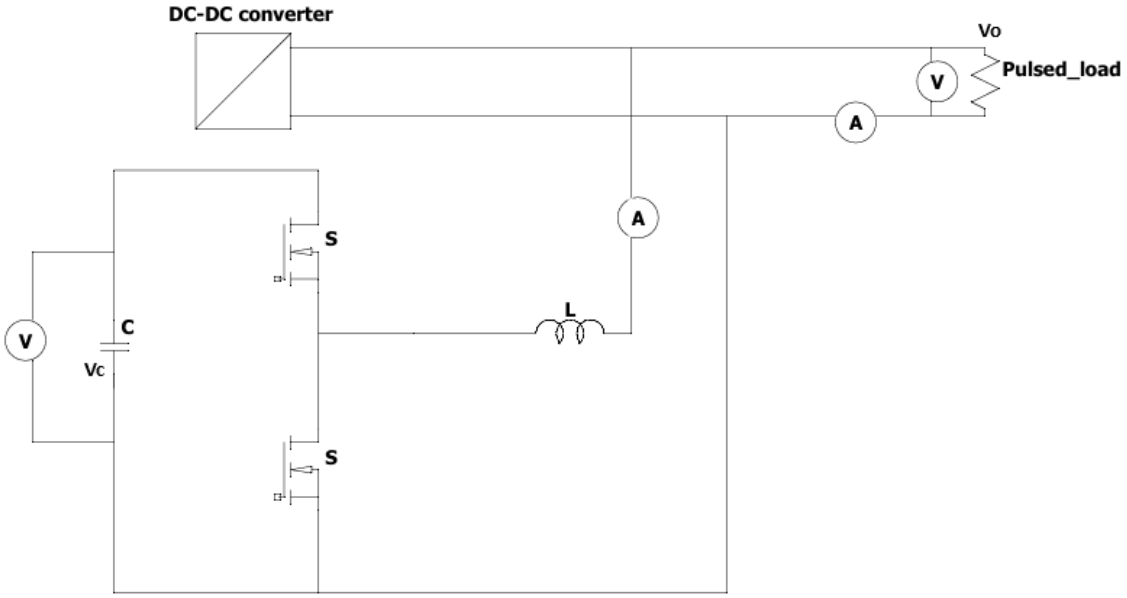

Figure 3.1: Simplified system with measurement points.

In Fig. 3.1 the voltage source is converted down and supplies the load. Then the APF compensates for the pulsed load using the capacitor bank.

3.2 Requirements and specifications

The different technical limitations used in this work had been set. They are based on similar electrical limitations of where the module would be placed in a real life application.

Table 3.1: Technical data/limitations from supervisors.

Description	Symbol	Value
Supply voltage	V_{supply}	28 V
Supply current	I_{supply}	9.8 A
Pulse duration	t_{on}	100 μs
Off duration	t_{off}	900 μs
Switching frequency	f_{sw}	1.2 MHz
Load current	I_{load}	40 A
Duty cycle	D	10 %

3.3 Placement of Active-Power Filter

The placement of the APF is crucial for the performance of the compensation. The filter can either be placed in series or in parallel (shunt) with the load. Placing the filter in parallel, it injects a current to compensate for the loss of current during pulse load. The series APF compensates with voltage, and its purpose is to stabilize the load voltage. Knowing this and applying it to this case, it was clear that the shunt APF filter should be used since a current injection was needed, due to a load of 40 A. The APF should therefore be placed in-between the source and load in parallel.

3.4 Selection of regulation

Two common regulation strategies are voltage regulation and current regulation. The choice of method depended on the behavior and requirements of the system.

3.4.1 Voltage sense regulation

In voltage sense regulation, the controller measures the selected voltages and adjusts the switching duty cycle to maintain a constant voltage level. Suitable voltages for measurement would be capacitor voltage inside the active filter and output voltage. The advantage is that it provides a simple control design with a direct regulation of the desired output voltage. It is suitable for designs where a stable voltage is the primary requirement. Disadvantages are that it has a slower dynamic response to rapid changes and does not limit current.

3.4.2 Current sense regulation

In current sense regulation, the controller measurers the current through the inductor of the active filter using a sensing resistor or current sensor. The switching action is then controlled based on and adjusted after the measured current. The advantages is that it provides a fast response to rapid changes and provides a current limit. Disadvantages are that it requires additional current sensing components and has a more complex control implementation.

3.4.3 Selected method

The system operates with a pulsed mode, where the capacitor voltage V_c recharges between pulses, while the output voltage V_o must be maintained during the pulse. During these pulses, the current can change rapidly due to the energy transfer from the capacitor through the active filter, providing stress to the components. Due to these specifications, current sense regulation is selected. Current regulation provides fast dynamic control and prevents excessive current peaks during the switching process. Therefore, current sense regulation offers better control and protection for the pulsed operation required in this system.

3.5 LTspice Schematic

In this chapter, the different sections of simulation will be broken down and explained in detail. The different part that will be broken down are, load, APF, current sensor CT425, reference control, pulse sensor, PI-regulator and drive circuit APF. Fig. 3.2 shows the different parts along with the simulation times and pulses. The pulses are 40 A high and lasts 100 μs for a period of 1 ms, which gives a duty cycle of 10%. Another thing to mention is that the triangle carrier wave, has a frequency of 1.2 MHz, that oscillates between 2 V and 3 V.

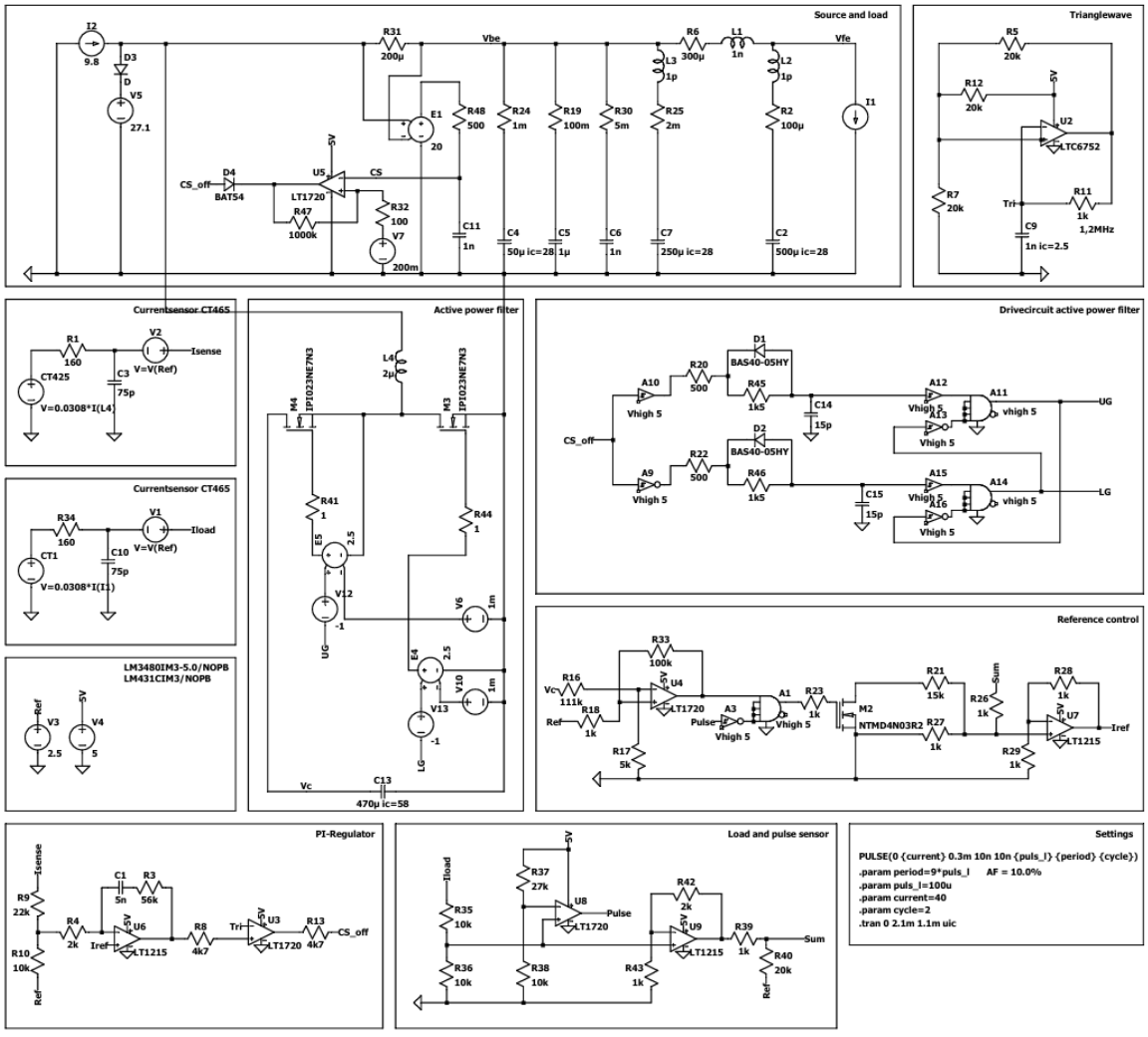

Figure 3.2: Full schematic in LTspice.

3.5.1 Supply and load

Fig. 3.2 shows the supply current and voltage as well as the load. The load is simulated with a 40 A amplitude and a duration of 100 μs with a duty cycle of 10%. The component between the different sources represent different contacts and cables with their approximate electrical properties. The supply voltage of 28 V,

with a current limited to 9.8 A together with the diode, simulates a current limited voltage source.

3.5.2 Active power filter

This section describes how the active power filter is created in LTspice. The two GaNFETs and everything that drives the gate in Fig. 3.2 is based on the half-bridge module LMG2100R026 and have been recreated in LTspice. C13 is the capacitor bank and L4 is the inductor.

3.5.3 Current sensor

This section describe how the current sensor was implemented in LTspice. In Fig. 3.2, the current sensor is a simplified behavioural model for the current sensor CT465. This was included since LTspice did not have this component in the library. It's designed to reproduce the real behaviour including it's non ideal parts. The sensor was modelled with a current controlled voltage source that measures 0.0308 V/A of the current through the measured component. This means that the sensor produce a voltage that is proportional to the measured current, with sensitivity of 30.8 mV/A. In our design, this device was used twice, both for measuring the current through the inductor connected to the active filter and for measuring the current from the pulsed load.

The resistor was included to represent an output impedance and the capacitor, which when connected to ground, models the limited bandwidth of the sensor. These two components together forms a first order low pass filter which reflects the response speed of the sensor. The voltage source at the output is set to 2.5 V, which was equal to the quiescent voltage output of the device.

3.5.4 Triangle wave and voltage references

A triangle wave is needed to mitigate the sub-harmonic oscillation. To generate a triangle wave at 1.2 MHz, 5 V is divided and connected to a comparator. The comparator generates a triangle wave that oscillates between 2 V and 3 V. This can be visualized in Fig 3.2. Two simulated references have been created for 2.5 V and 5 V, an internal system can be used and has been simulated but, with the actual references values created the simulation takes time. To reduce the simulation time, two voltage sources was implemented.

3.5.5 Load and pulse-sensor

In Fig. 3.2, the load is sensed via CT465 and divided down and compared with a 5 V reference. So when a pulse comes, the comparator LT1720 sends out a signal, *Pulse*. The sensed load is also sent in to LT1215 and the operational amplifier where the reference of 2.5 V is added to become the signal *Sum*. This is the load sense where the load could vary in amplitude and the reference system would adapt to it.

3.5.6 Reference control

The following section describes how the different references was handled via an analogue solution and how it was generated in LTspice. The reference control in Fig. 3.2 works in the following way. The capacitor bank voltage is compared with a reference voltage based on when the capacitor voltage reaches 58 V. The voltage is then compared in a comparator that sends out a signal into a logical AND-gate.

The signal is compared with the inverse of the pulse. This means that when V_c is not fully charged and there is not a pulse the logical AND-gate send out a gate signal that controls the MOSFET. When the MOSFET is turned in it sends the signal to ground sending out a very low I_{ref}. When the MOSFET is turned off, the Sum signal is added and forms the I_{ref} signal.

3.5.7 PI-regulator

The PI-regulator senses, regulates and creates the PWM signal used to operate the drive circuit. In Fig 3.2 the sensed inductor current comes in and is divided and compared with the 2.5 V reference. The signal in front of a voltage signal continues into the PI-part of the regulator where the values chosen now suits the circuit.

This may need to be adjusted when tested physically. The regulated signal was then compared as previously mentioned. The triangle wave bounces between 2 to 3 V. The signals are compared in the comparator mostly to counteract sub-harmonic oscillation which can occur when the duty cycle is greater than 50%. The output of this signal becomes the PWM signal that controls the half-bridge module's GaN-switches.

3.5.8 Drive circuit

The following section explain how the drive circuit operates the half-bridge using a PWM signal in LTspice. In Fig 3.2, the drive circuit is designed to convert a PWM input signal into two complementary gate drive signals to control the power stage of the half-bridge. The circuit adds delays (blanking time) to ensure safe switching operation by preventing simultaneous conduction on both switches in the half-bridge. The input PWM is applied to two parallel paths, one for the upper (UG) and one for lower (LG) gate signal. The UG signal is non-inverted and in phase with the PWM signal, while LG is inverted and is therefore 180° out of phase. Each signal is connected to an RC filter in combination with diodes. These filters adds propagation delays and shape the signal while the diodes provide a path for charging and discharging the capacitors, resulting in different turn on and turn off delays. The delayed and conditioned signals are then processed by logic gates that introduce a defined dead time, which ensures that both switches are never activated at the same time. The output signals UG and LG then operates each switch in the half-bridge, LMG2100R026VBNR.

3.6 KiCad Schematic and Layout

The circuit schematics and the layout are presented in Fig. 3.3 and 3.4. These was based on the simulations in LTspice and have from these, been constructed in KiCad.

3.6.1 KiCad schematic

In this schematic, all of the actual components, with their actual footprints, have been implemented and connected. The schematic does not include the half-bridge and inductor and capacitor bank, since those will already have been mounted on another existing test-card.

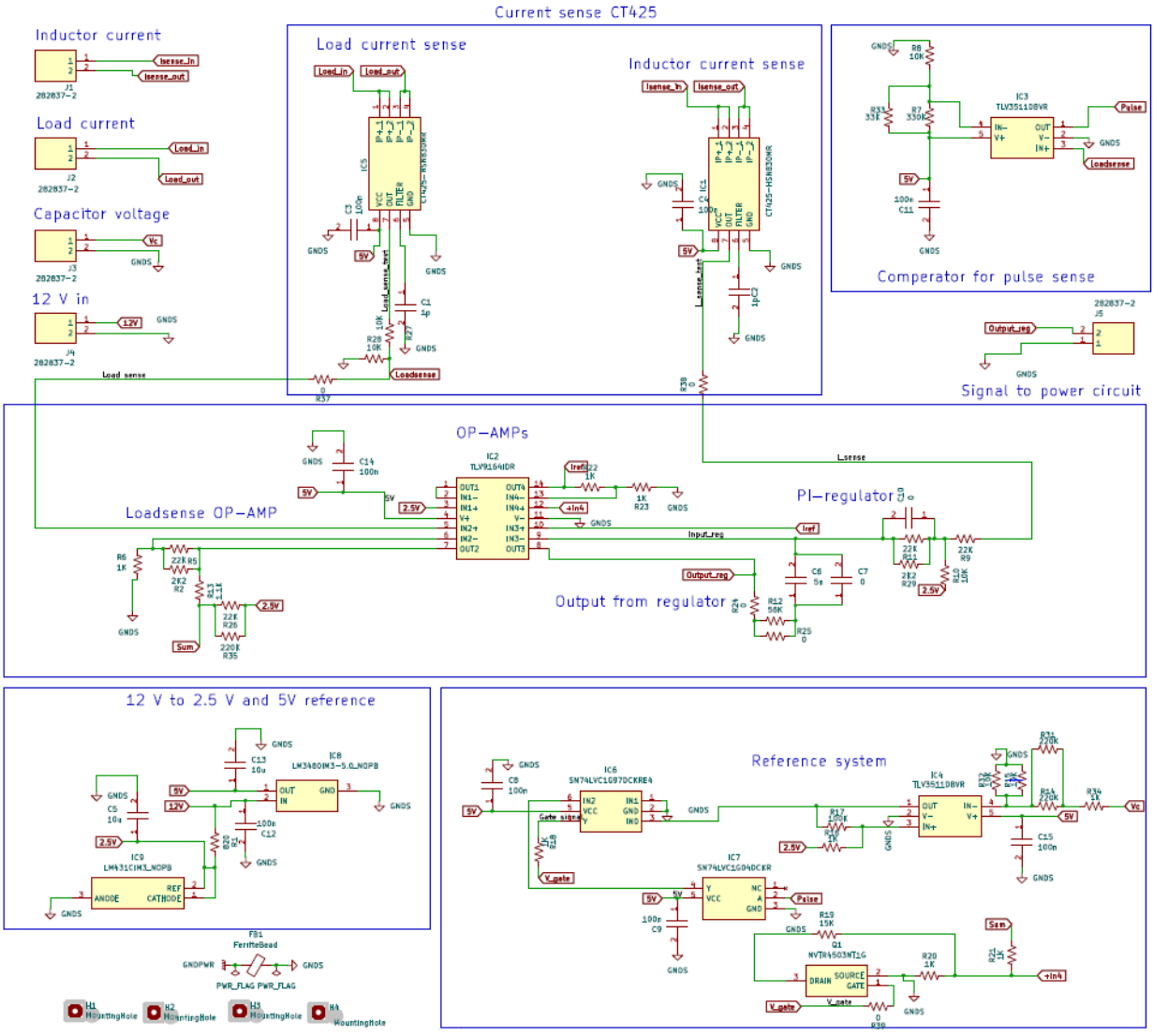

Figure 3.3: Full schematic in KiCad for PCB layout.

There are five different sections, current sense, comparator for pulse sense, the OP-AMPs, the reference maker and the reference system. Since this is a test card,

several 0 Ω have been implemented to investigate the impact of different resistances to, for instance optimize the feedback-loop.

3.6.2 Circuit layout

After the schematic had been created, the layout was constructed with the footprints of the components. This is a four-layer printed circuit board (PCB) with the first layer being signals, second being ground, third being 5 V reference to power the components and the final layer is a signal layer to avoid overlapping traces. The full layout is presented in Fig. 3.4.

In the layout there are some red squares around the board, and these are test points for easier access with a probe. The current sensors have been constructed with a large copper pad to help with the heat spreading. The pads have also been placed far from the regulation circuits since high currents creates noise and will cause disturbance.

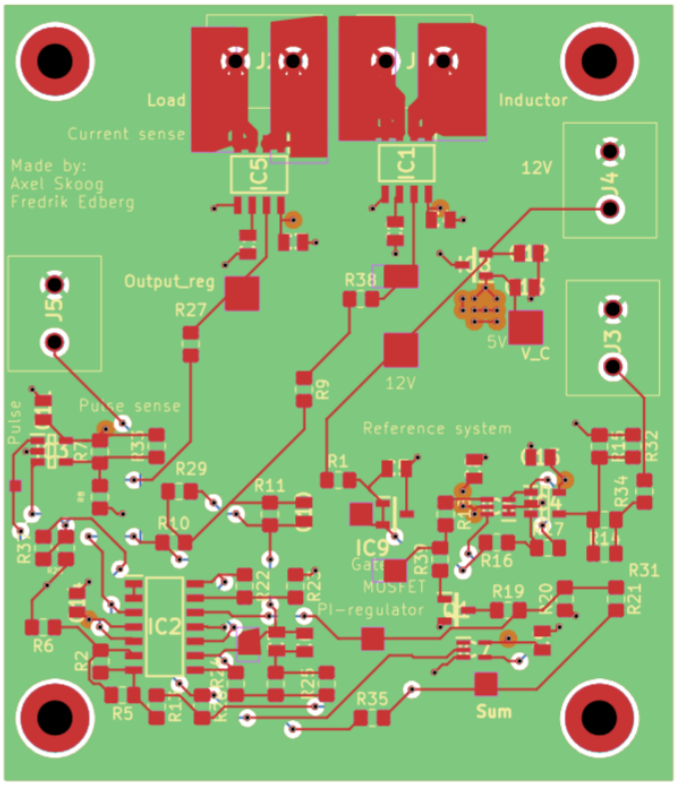

Figure 3.4: Full PCB layout in KiCad.

3.7 Assembly

The PCB was assembled using solder paste. A stencil was placed over the PCB and then the solder paste was smeared over the stencil. Using tweezers and the pick and place method, the components was placed on the PCB before going to the

soldering-oven. After the soldering-oven, the components was fixed to the PCB and the verification process could start. The final product is shown Fig. 3.5.

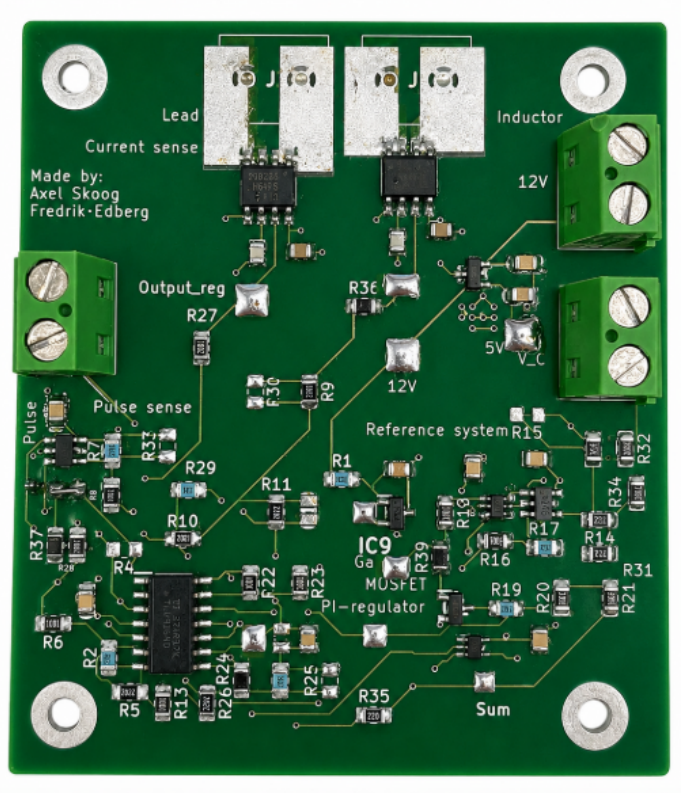

Figure 3.5: The assembled PCB.

3.8 Verification

The verification section describes the different steps taken after assembly to ensure that everything is in order.

3.8.1 Start-up

First of all, when everything was assembled there needed to be a visual check, to ensure that everything was soldered correctly so that no short-circuits had accidental been made. Then the power supply units (PSU) was connected and the PCB started. If there is some errors the integrated circuits (IC) are the first to fail and burn up. If that is not the case, it is critical to see that the regulation preforms as intended and softly charges the capacitor voltage. If a stable operation has been found then its time to apply the pulsed load.

3.8.2 Applying load

When the start-up tests was completed, it was time to apply the pulsed load. Since 40 A creates a substantial amount of power, to protect the circuit there was a ramp-up where a smaller load was tested first and then built up until it reached 40 A. The

PCB should be able to handle the loads and continuously send out 28 V during the load-pulses.

3.8.3 Thermal management

When the load had been applied, it is important to check the temperature of the components so that it does not exceed the thermal limit of 40° C, the only component allowed to reach higher temperatures without external cooling is the inductor. Therefore, a thermal camera was used to get a rough estimate of the temperature. High temperatures was likely to occur in the inductor during pulsating loads, which is then exposed to a high current.

Other component affected is the current sensors where the high current is measured and the half-bridge during switching. To be able to handle the increased current during pulsating loads, twisted parallel cables was used where the current is expected to be higher. This generates less heat than a single cable, as the current is distributed between them, while also minimizing electromagnetic interference.

3.9 Measurement Setup

This section will describe the measurement setup used to verify the practical part of this master thesis. The different components are then two power supply units, the power part of the APF, the controller part of the APF, and a pulsed load. This can be visualized in Fig. 3.6.

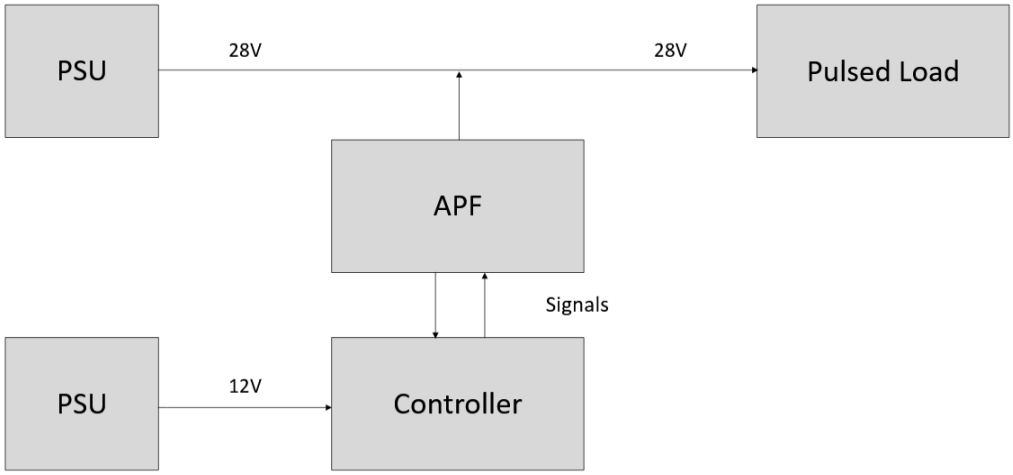

Figure 3.6: Simplified measurement set-up

Other than the main components there was voltage measurements and current measurements. To measure the voltage, several multimeters and probes was used along with a oscilloscope. To measure the current, a clamped current probe was used. Designed in the PCB there are several solder pads for easier access with a probe. There was also several 0 Ω resistors to optimize certain values, since real life components

differ from simulated ones. The current needs to be increased to at least 9.8 A for the switching circuit to activate, and when V_c reach its targeted value, the current will drop to approximately 0 A during steady state operation. The complete setup can be seen in Appendix A.

3.9.1 Method

Instead of designing a completely new PCB from scratch, the task was to integrate the control PCB with an already existing buck converter. On that buck converter certain components where removed. The buck converter shown in Fig. 3.7 reduced voltage from between 58 V-30 V to 28 V.

The four large capacitors attached to the buck converter provides a total capacitance of 16.8 mF and are charged and discharged to be able to handle the pulsating loads.

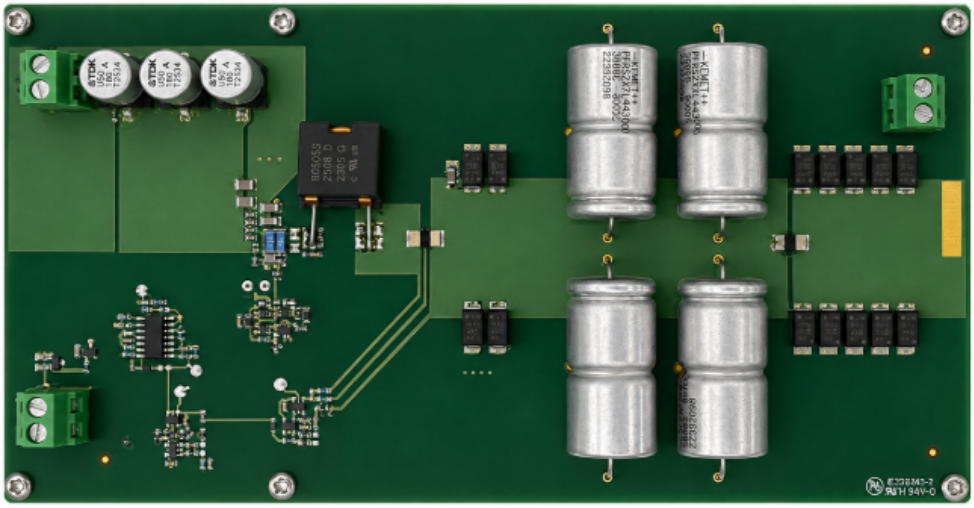

Figure 3.7: Buck converter.

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The removed components on the buck converter was the voltage regulation circuit, the inductor and the large capacitors. This removed the buck function completely and the remaining components represents "Source and load", "Drive circuit active power filter" and the half-bridge in "Active power filter" in Fig. 3.2. The APF was then integrated as shown in Fig. 3.8.

The purpose of the method used was to test if the proposed APF solution is functional and capable of maintaining the voltage V_o during pulsating loads. Through designing, construction, integration and testing, the thesis aims to verify that the design performs as intended during high switching operations.

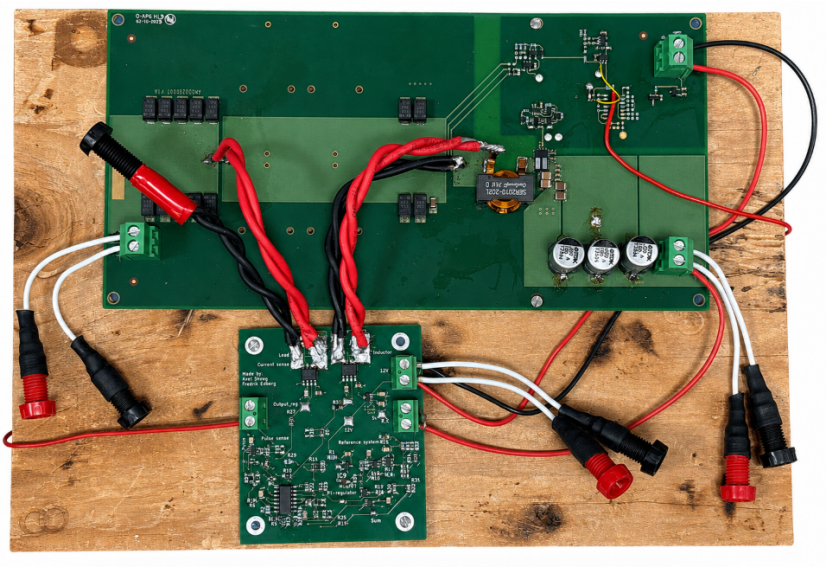

Figure 3.8: Integration of the APF onto the existing PCB.

The method used to verify each PCB was to operate each section on its own to verify that the voltages generated represented the values achieved during simulation. Afterwards several circuit sections was tested simultaneously to verify that they functioned together. Lastly each PCB was verified as a whole complete circuit. To verify that the integration between both PCB's works as intended, a step-up of both input voltage and pulsating load current was used. When it had been verified that the system operates as intended during steady state, the pulsating load was gradually increased in both duration and current amplitude.

3.10 Component selection

In this section the actual components that was selected is presented, including a description on why they have been chosen.

3.10.1 GaNFET

There are two GaNFETs that have been selected. One was for the power stage and was part of the half bridge. The other one was part of the reference system. For the power stage, a half-bridge module was selected beforehand as the project is based upon this module. The module in hand, LMG2100R026, is a half-bridge with two GaN switches and an internal driver circuit. It can handle high current bidirectionally, up to 55 A, and a drain-source voltage of 100 V. It is also capable to switch up to 10 MHz. For the other GaNFET in the reference system, a less powerful GaNFET was chosen since there is no need for high current, high voltage and high switching. Its main purpose was to turn on and off when certain criteria had been fulfilled in the reference control. Therefore the GaNFET used was NVTR4503NT1G, a logic-level n-channel GaNFET.

3.10.2 Capacitor storage

The capacitor in the active filter was used as the energy storage in the pulsed power system. It supplies the required energy during the pulse and is then recharged between pulses by the converter. During operation, the capacitor voltage V_c is charged to 58 V before a pulse occurs. When the pulse is triggered, energy stored in the capacitor is delivered to the load and the regulation maintains the output voltage V_o at 28 V. V_c decreases during the pulse and is then recharged before the next pulse. A large enough capacitance is required to ensure that the voltage drop over V_c during the pulse remains within acceptable limits. If the capacitance is too small, the output voltage V_o will drop during the pulses. Two main requirements are needed to determine the size of the capacitor, the energy required for the load during the pulse, and the maximum voltage drop allowed over V_c. Using (2.17) and (2.18), the energy consumed by the load is bound to be 0.112 J and the energy supplied by the source is 0.027 J. The energy that must be provided by the active filter was therefore.

$$E_{filter} = E_{pulse} - E_{supply} = 0.112 - 0.027 = 0.085\,\text{J} \tag{3.1}$$

Since I_{supply} still supplies current during the load. The actual current provided by the capacitor was less than I_{load}.

$$I_{filter} = I_{load} - I_{supply} = 40 - 9.8 = 30.2\,\text{A} \tag{3.2}$$

Using (2.20) with (3.2), and a maximum allowed voltage drop of 8 V over V_c during pulses, a minimum capacitance of 378 µF is required. Therefore, a standard capacitor value of 470 µF was selected to provide an additional margin. Using (2.19) with 470 µF, the total energy stored E_C is 0.8 J. This provides a stable range for the operation of the system. After the pulse, using (2.21) together with (3.1), the capacitor voltage after the pulse was calculated to 54.8 V. Resulting in a voltage drop of 3.2 V which is well within the allowed margin. With pulse duration t_{on} and duty cycle D, the time t_{off} equals 900 µs. Using (2.22), the time t_{charge} was calculated to 310 µs. Since the performance of capacitors is worse closer to rated voltages, standard practice is to operate within 50-80% of rated voltages. With a V_c value of 58 V the selected component has a rated voltage of 75 V. The capacitor selected was EEVFK1K471M from Panasonic. This capacitor fulfil the requirements regarding maximum temperature and maximum voltage, this information have been evaluated from its data-sheets. The overall large design margins used for the capacitor are selected to account for non-ideal component behaviour.

3.10.3 Inductor

The selection of the inductor was based on the inductance that was needed. The inductance for the inductor is based on (2.16). Where the duty cycle was 50%, the switching frequency f_s was 1.2 MHz, the supply voltage V_{supply} was 28 V and the inductance ripple Δi_L was 6 A. This yields

$$L = \frac{V_{supply} D}{f_s \Delta i_L} = \frac{28 \cdot \frac{1}{2}}{1.2 \cdot 10^6 \cdot 6} = 1.9\ \mu\text{H} \tag{3.3}$$

which means that the inductor selected must be larger or equal to 1.9 µH. The inductor should also be selected to handle over 40 A continuous current as well as to handle higher transients. Since this was a test-card, multiple inductors had been chosen from different manufacturers and also different composition, 78433290200 from Würth Electronics, which is a powder core inductor. SER2010-202MLD from Coilcraft that is a shielded inductor. The last inductor chosen was IHLP4040DZER2R0M11 from Vishay which also is an powder core inductor. All of these inductors should fulfil the temperature and saturation requirements, based upon data collected from their data-sheet. All of the inductors was tested and based upon generated heat and overall performance a choice was made of which to implement.

3.10.4 Operational Amplifiers

The TLV9164IDR from Texas Instruments is a rail to rail op-amp with a bandwidth of 11 MHz. The supply voltage between 2.7 V to 16 V gives a wide range of operation. The device is quad-channel, meaning it integrates four independent op-amps in one component, which saves PCB space and reduces the amount of total components in the design. Each channel features rail to rail capability and has a gain bandwidth of 11 MHz. It has a low power consumption with 2.4 mA per channel. The device is regarded as a stable general purpose op-amp with high precision in combination with high performance.

3.10.5 Comparator

The TLV3511DBVR from Texas Instruments is a high speed, single channel voltage comparator with rail to rail capability and supports a switching frequency up to 180 MHz, with a supply voltage between 2.7 V to 5 V. The comparator uses a push-pull output, which means that it can have both high and low output without requiring an external pull-up resistor, which means that there are fewer components used in total. The internal hysteresis of 2.3 mV helps prevent false trigger and improves stability. It maintains a low power consumption with 1.1 mA per channel. Additional features include a power-on-reset function, which ensures the output starts in a known state during startup.

3.10.6 Current sensor

The CT465-HSN865MR from Allegro MicroSystems is an isolated current sensor designed for accurate and fast current measurement. It's designed for measuring bidirectional AC and DC current up to ±65 A with a supply voltage between 4.7 V to 5.5 V. The device integrates a low resistance current carrying conductor which eliminates the need of shunt resistors, saving PCB space and a total reduction of components in the design. The sensor provide a linear analog voltage that is proportional to the sensed current with a total error between ±0.5% to ±1%. Combined with a bandwidth of 1 MHz and fast response time of 300 ns, the sensor can track rapid current changes. The device has an output between 0 V to 5.5 V and has a voltage output quiescent of 2.5 V which means that when the current value is 0 A, this device output is 2.5 V.

3.10.7 Voltage regulator

The design has two different regulated voltages, 2.5 V as a reference voltage and 5 V as a supply voltage for the comparators and op-amps. These two voltages was generated using two different components, LM431CIM3/NOPB and LM3480IM3-5.0/NOPB.

The LM3480IM3-5.0/NOPB from Texas Instruments is a fixed output linear voltage regulator designed to provide a stable 5 V output with an input up to 30 V. The device has a dropout voltage of 1.2 V during full load, requiring a minimum input voltage of 6.2 V. A 12 V supply available in the surrounding system environment is used as input to the device. To maintain stability, the device requires a minimum output capacitance of 0.1 µF.

The LM431CIM3/NOPB from Texas Instruments is a three-terminal adjustable shunt voltage regulator, meaning it controls voltage by sinking current. The device output can be set between 2.5 V to 36 V using two external resistors as a voltage divided network. But for 2.5 V, which is the internal reference, this is not required.

4
Analysis

4.1 Simulation

In this project, simulation has been a critical point in determining the design of the circuit and the construction of the printed circuit board. The results obtained from the simulation provide insight into system operation, stability, design decisions and validation of theoretical calculations. The simulation environment allows for variation of key parameters such as duty cycle and load conditions. Through this approach, a range of scenarios was evaluated in order to understand the sensitivity of the system to different design choices, such as change in duty cycle, capacitance, inductor values and load parameters. Different combinations of parameters were tested, to assess their impact on performance and stability. The simulation results presented use the initial conditions shown in Tab. 3.1. To show the differences, simulations have been performed without any filter, as well as with a passive power filter and with the active power filter.

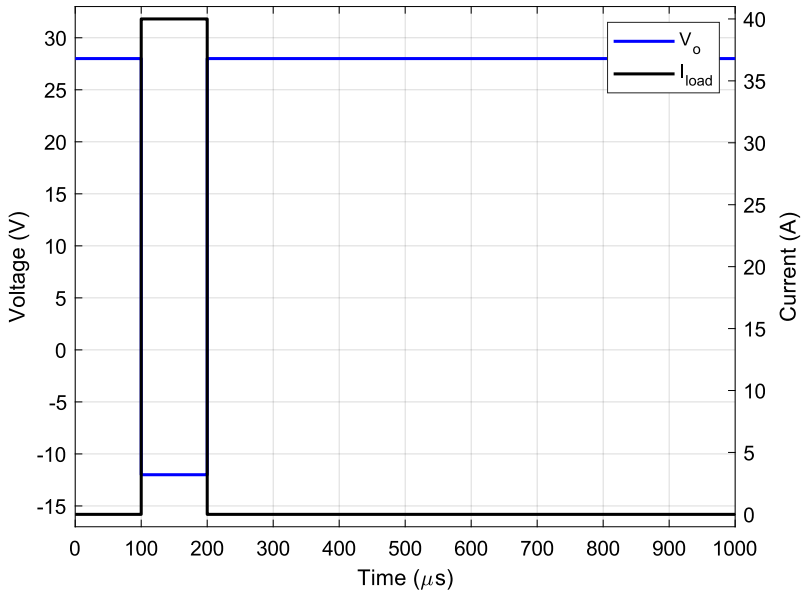

Figure 4.1: V_o with no filter installed.

With no filter installed, V_o immediately drops below 0 V during the pulse and return to 28 V afterwards. The mean power output during the pulse is 0 W (or negative?) and ideal is 1120 W.

4.1.1 Passive power filter

A passive power filter consisting of a capacitor has been connected in parallel with the load. The passive power filter is discharged when the pulse occurs and charged between the pulses.

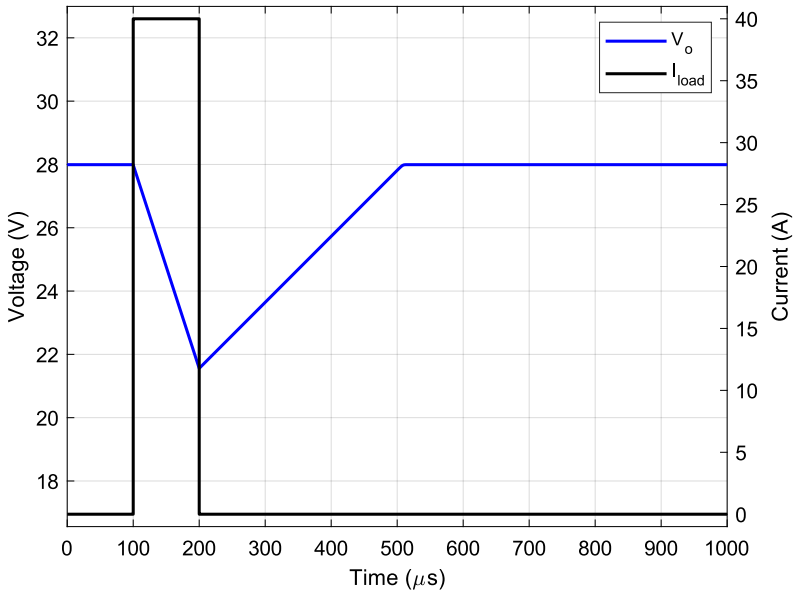

Figure 4.2: V_o with a 470 µF passive power filter installed.

Fig. 4.2 shows the behaviour of V_o when a 470 µF filter is used. V_o drops to 21.5 V during the pulse and then returns to 28 V afterwards. The mean voltage during the pulse is 24.75 V which results in an mean power output of 990 W.

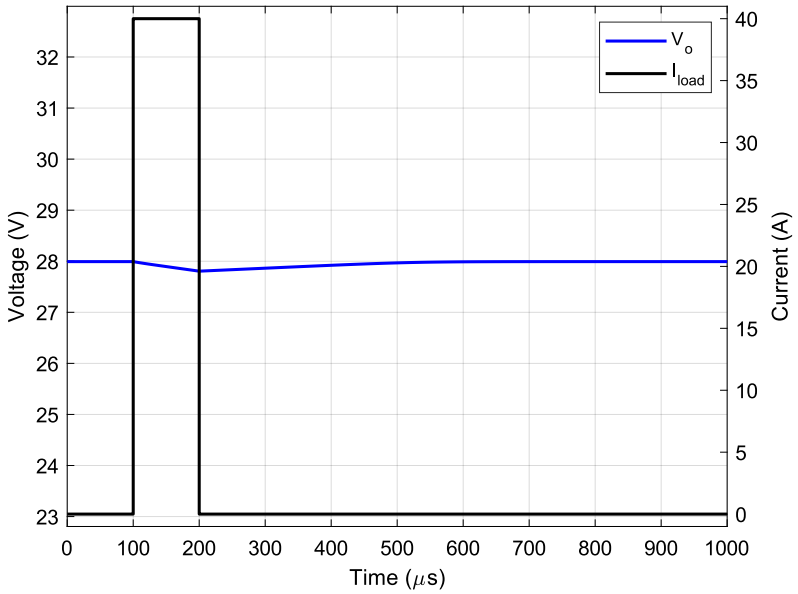

Figure 4.3: V_o with a 16.8 mF passive power filter installed.

To maintain a steady output voltage with a passive power filter, large capacitors needs to be used. Fig. 4.3 shows the behaviour of V_o when a 16.8 mF is used. The voltage drops to 27.8 V during the pulse which results in a mean output power of 1112 W. While this mean output power is acceptable, one or several capacitors are needed to achieve the results. Capacitors of 16.8 mF are large and takes up a lot of volume and weight. For radars, space and weight is of great importance and should be kept as minimal as possible. Therefore this solution is not optimum.

4.1.2 Active power filter

Simulation was done in LTspice using the components and values from the schematic shown in Fig. 3.2. In the theory section, the voltage is assumed to remain constant at 28 V during the pulse. In the simulation, the voltage during the pulse is monitored to validate this assumption. Ideally, it should remain close to 28 V with only small variations during pulses. By comparing the behaviour of the simulated voltage with the theoretical expectation of a stable value, the design can be confirmed.

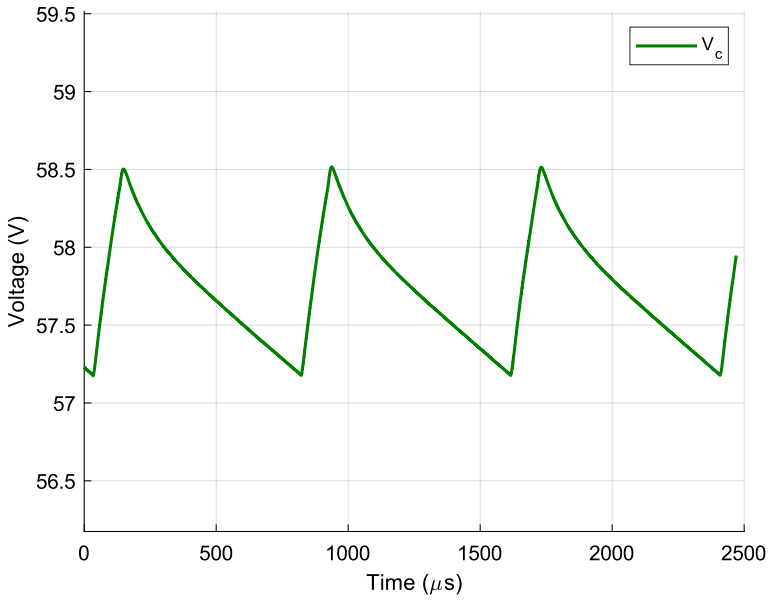

Figure 4.4: Voltage ripple when charging and discharging capacitor V_c without load.

The capacitor charges and discharges during no-load conditions in order to maintain a stable average V_c voltage. This behaviour is expected, as the capacitor acts as an energy buffer, supplying or absorbing small amounts of energy to balance the system and compensate for switching actions and internal losses. The average value of V_c is 57.85 V, with a ripple of ±0.65 V. This result is close to the design target of 58 V, indicating that the regulator and component values are correct. The small voltage ripple reflects periodic charging and discharging due to the converter switching, and its magnitude confirms that the voltage V_c remains well regulated.

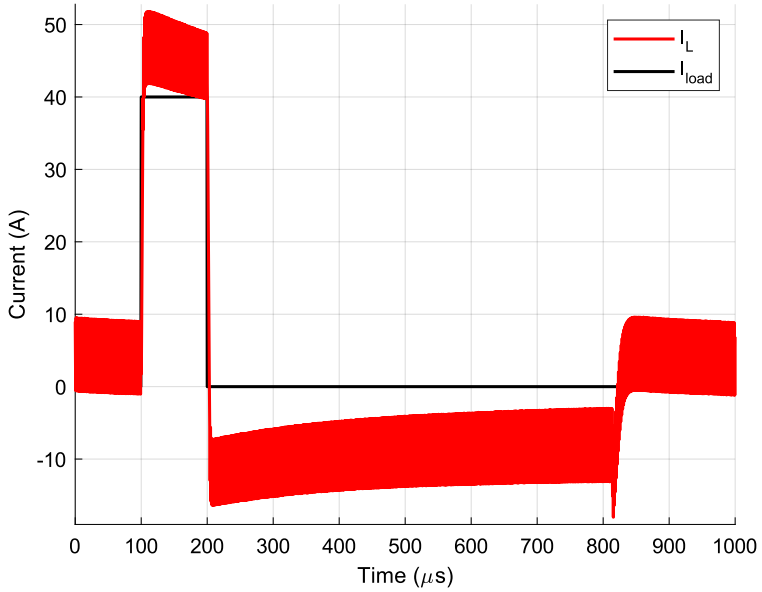

Figure 4.5: Inductor current i_L and load current i_{load} during one cycle.

During pulses, the load current i_{load} generates a need for power, which is provided by the active power filter when the capacitor in the active power filter is discharging. This generates a current i_L through the inductor, which maintains a steady voltage V_o to allow maximum power output. i_L oscillates at 0 A with a ripple of ± 3 A during no-load and when V_c is fully charged. When a pulse occurs, i_L rapidly increases and after the pulse it rapidly decreases. Positive current occurs during discharge, and a negative current occurs when the active power filter charges the capacitor.

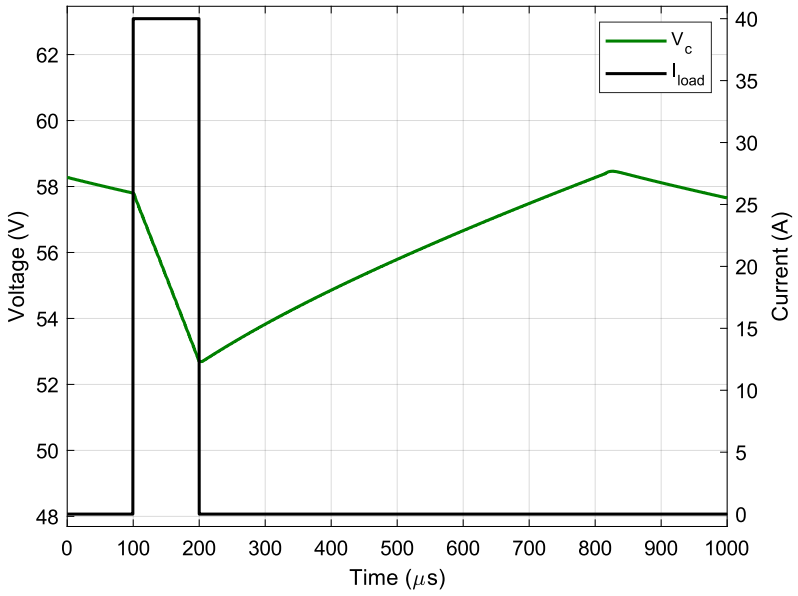

Figure 4.6: Capacitor voltage V_c and load current i_{load} during one cycle.

During pulses, capacitor voltage V_c discharges rapidly to maintain a steady voltage V_o. After the pulse, a controlled charge to return to 58 V begins. Once the value has been reached, an oscillation occurs to maintain the voltage between pulses. During the discharge in Fig. 4.6, the capacitor is discharged from 57.8 V to 52.7 V. According to Fig. 4.4, the value of V_c ripples during no load, and since the pulsed load can start anytime, the average value is calculated to 57.85 V and the voltage drop is approximate 5 V from the initial value during each pulse.

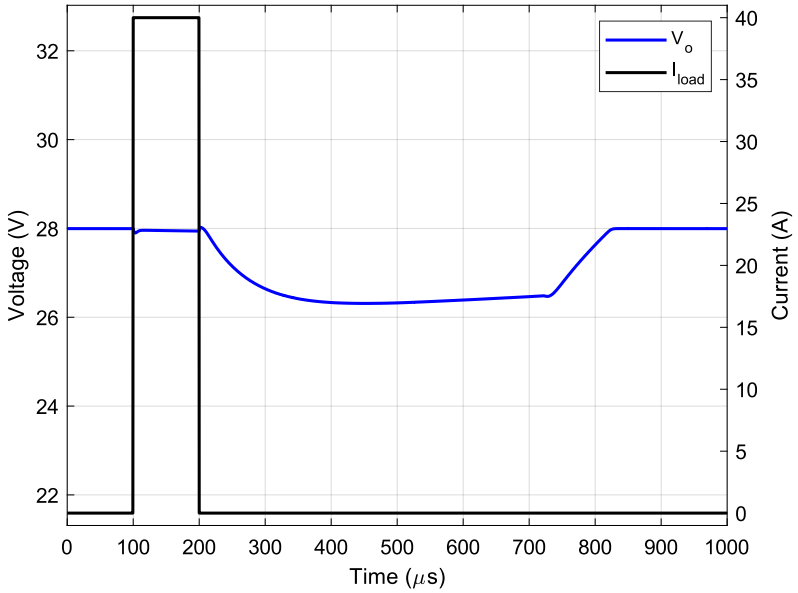

Figure 4.7: Output voltage V_o and load current i_{load} during one cycle.

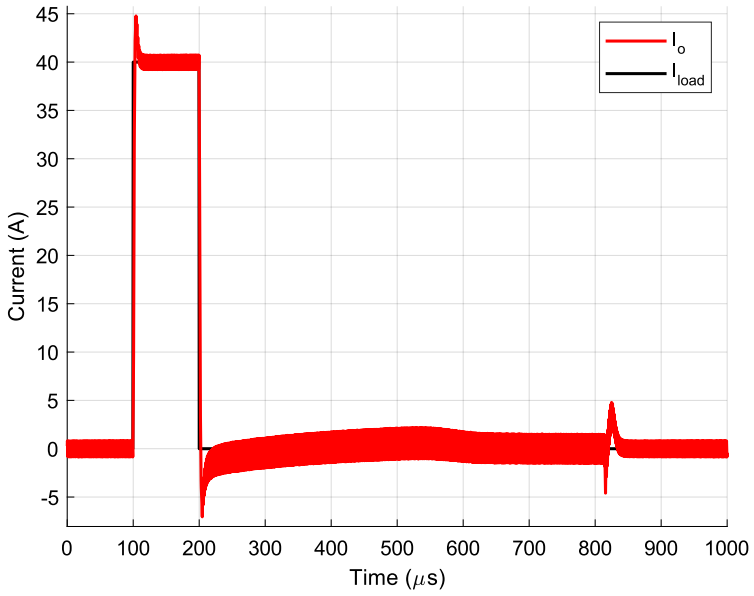

Figure 4.8: Output current I_o during one cycle.

The voltage at steady state is stable at 28 V, during pulses, the voltage experience a drop to 27.9 V before the capacitor can compensate up to 27.95 V. After the pulse, before the capacitor can react, an increase of voltage occurs up to 28.05 V. Afterwards, the output voltage droops to allow recharging of the capacitor voltage back to 58 V and once that condition has been reach, the output voltage return to 28 V before next pulse occurs. The output current I_o oscillates around 0 A during steady state and increase to 40 A with an initial overshoot during the pulse. After the pulse I_o decrease and continue to oscillate around 0 A. A small increase in current occurs when the output voltage returns to 28 V, as shown in Fig. 4.7. This gives a mean power output of 1118 W during the pulse.

To verify stability during simulation, a stability sensitivity analysis was done, were the parameters I_{load}, D, and t_{on} were each independently increased by 20% relative to their nominal (initial) values in order to evaluate the system's sensitivity to individual parameter variations. In addition, a combined case was tested in which all three parameters were simultaneously increased by 20%, representing a worst-case operating scenario. This approach ensures that the design remains robust under potential deviations in load conditions, duty cycle, and switching duration.

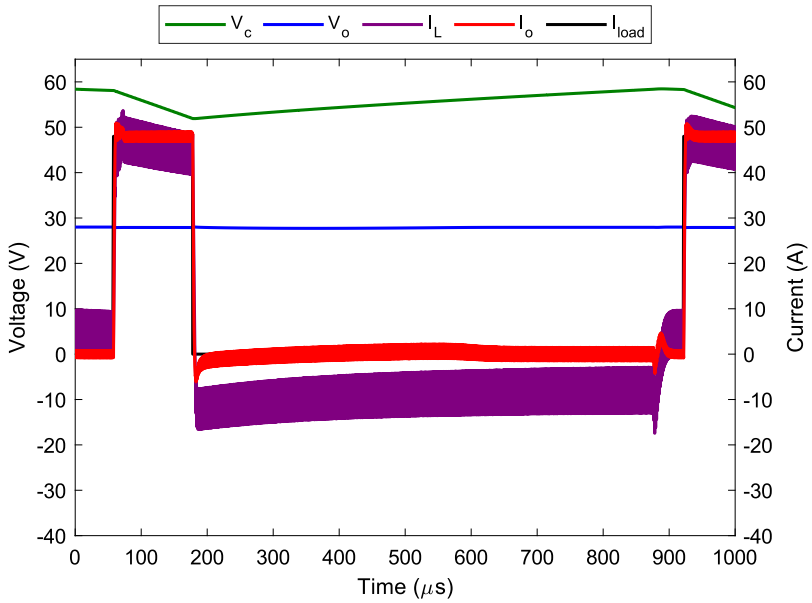

Figure 4.9: I_L, V_c, I_o and V_o with an 20% increase of I_{load}, D, and t_{on} during 1 ms.

Fig. 4.9 shows that the filter can operate with an increase of 20% load and maintain a mean output voltage of 27.92 V during the pulse. The results indicate that the design is stable and robust, as the system maintains its performance even after parameter variations and changes in operating conditions.

4.2 Measured results

When the board had been mounted, assembled and verified it was time for testing. During verification the powder core inductors became too warm. They registered over 130°C and was probably warmer since the heat-cameras max temperature was 130°C. Therefore, a decision was made to use the shielded inductor SER2010-202MLD from Coilcraft, which handled heat better and only reach a maximum temperature of 80°C. Below, two different sizes of capacitors was tested to see if it made any difference in performance. Before any load is applied a stable base case needs to be etablised. Fig. 4.10 shows how the regulation behaves without any load. In this case the APF is fed with 28 V and the PSU has limited current to 9.8 A.

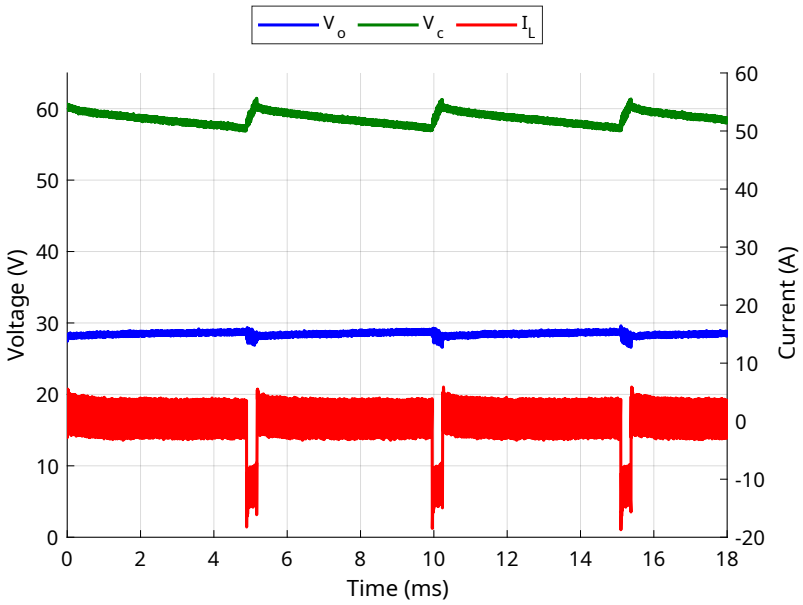

Figure 4.10: Capacitor voltage V_c, output voltage V_o and inductor current I_L without load.

In Fig. 4.10 the lines are not horizontal due to the capacitor voltage. Since the design goal was that it should regulate to around 58 V, and since everything is tuned to an exact voltage the regulation tends to overshoot to 60 V during start-up. This causes the control to slowly regulate down towards 58 V, and when it passes 58 V the capacitor voltage is regulated up. However, compared to Fig. 4.4 the regulation of V_c is significantly slower during no load condition. It does this with the current supply from the PSU and as can be seen in Fig. 4.10 the current spikes for a short moment to a mean value of around -9.8 A. The current increase also causes some small disturbances in the output voltage. The next step is to test how the control system handles a 40 A load. This is visualized in Fig. 4.11 where one 100 µs 40 A pulse is shown.

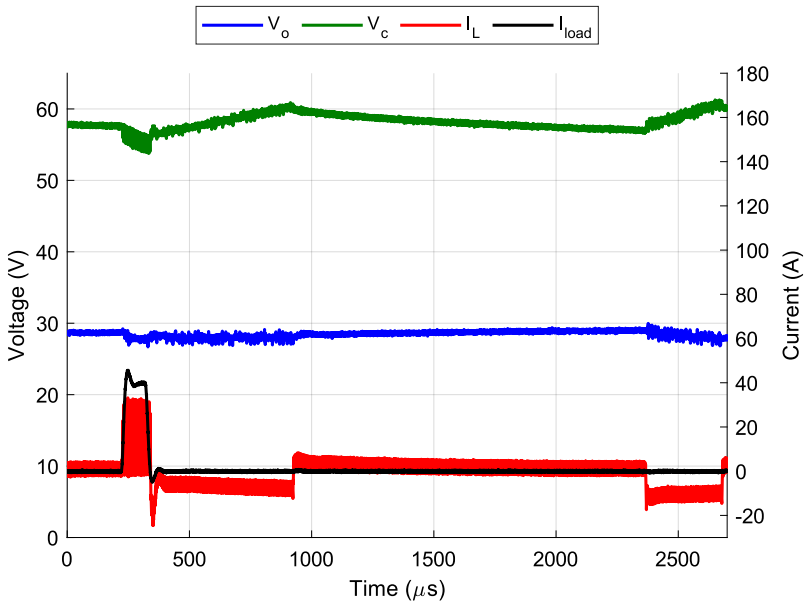

Figure 4.11: Capacitor voltage V_c, output voltage V_o and inductor current I_L during a single 40 A pulse.

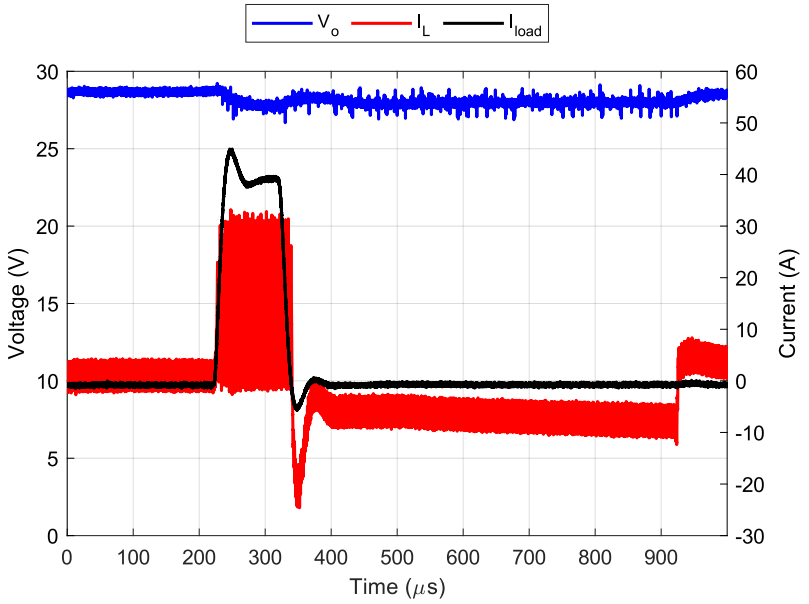

Figure 4.12: Capacitor voltage V_c, output voltage V_o and inductor current I_L during a single 40 A pulse zoomed in.

As seen in Fig. 4.11 and in Fig. 4.12 when the 40 A pulsed load comes the inductor current immediately increases to 30 A since the other 9.8 A is compensated by design from the PSU. When the pulsed load comes, the capacitor voltage decreases to compensate for the output voltage. Although the output voltage V_o drops to 27.1 V, giving a mean power output of 1084 W, during the pulse. The regulation still manages to keep it relative close to 28 V. When the load is finished the recharge process

begins. Between around 400 µs to 900 µs, the output voltage decreases together with the power unit's current supply to increase the capacitor voltage again to the goal value of 58 V. When the capacitor value has hit the target value, as seen in Fig. 4.11 at 900 µs, the output voltage and supply current goes back to 28 V and 0 A. After that the capacitor voltage tries to find the right value as previously explained regarding Fig. 4.10. To make sure that not everything was compensated with the power units current supply, a decision to measure the current over the supply cables was made. The results is visible in Fig. 4.13.

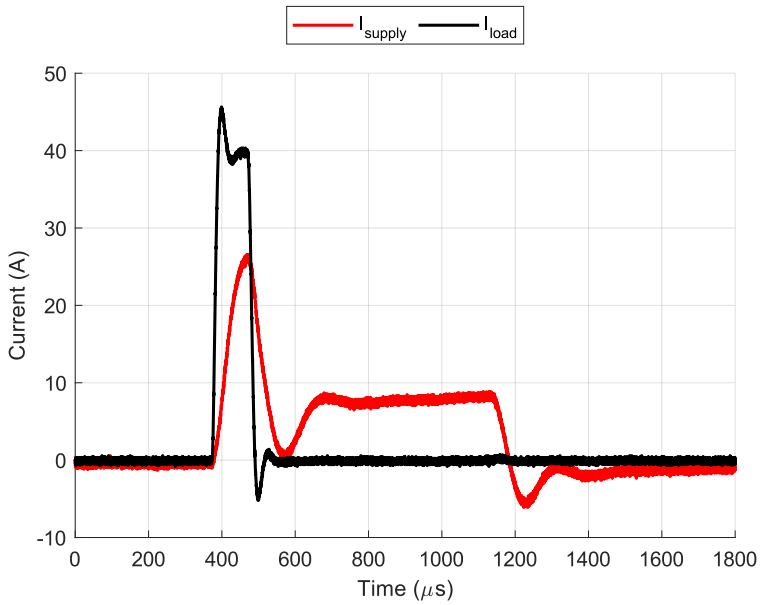

Figure 4.13: Supply current I_{supply} and load current I_{load} during single 40 A pulse.

When analysing Fig. 4.13 it becomes clear, even tough a current limit was set on the PSU, that the supply current during a pulse exceeds the 9.8 A current limit. This could be due to the fact that the PSU current limit could not handle fast pulsed loads and therefore will exceed the current limit. This does not means that every bit of compensation for pulsed loads comes from the PSU, because as seen in Fig. 4.11 the inductor current compensates before the supply current reaches over the limit of 9.8 A. As seen in Fig. 4.13 the current reaches to around 25 A, which means that the rest of the compensation is from the capacitor. After the pulse, from 600 µs to 1200 µs, the current is supplying 9.8 A to charge the capacitor bank up again. The following step is to test if the regulation and power compensation can handle two pulses with a duty cycle of 10 %, using the conditions given in Table. 3.1, this is visualised in Fig. 4.14.

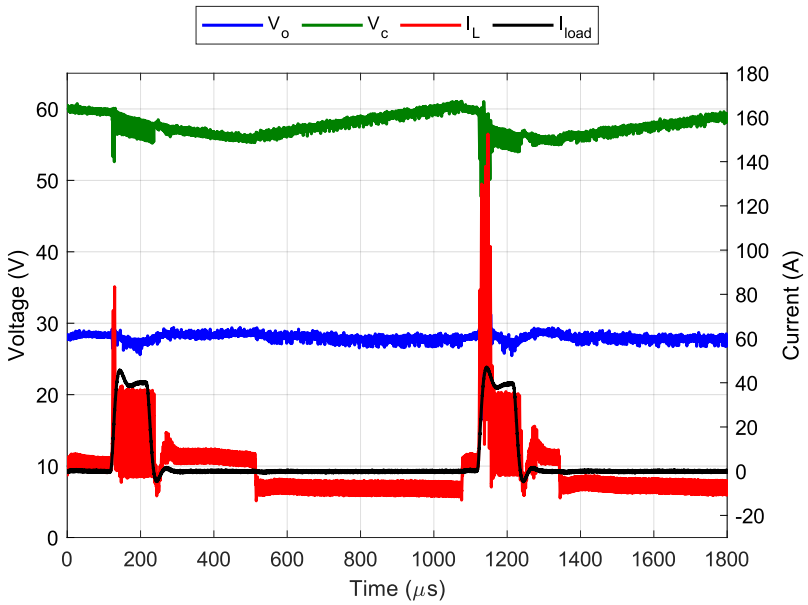

Figure 4.14: Capacitor voltage V_c, output voltage V_o and inductor current I_L during pulsating loads I_{load} with a duty cycle off 10 %.

When operating with with the conditions given in Table. 3.1, the APF is not able to correctly handle the pulsating loads. Although the value of V_c drops during the initial pulse, the transient on I_L causes the voltage drop on V_o to be less than expected, forcing V_c to drop less as well. Compared to the single pulse case, shown in Fig. 4.11, the drop in V_c is large enough to activate the recharge condition of the APF. Therefore, after the pulse, the inductor current changes direction immediately and starts to continue discharge until the targeted value for recharge is reached, causing the capacitor voltage to not start to restore directly after the pules has occurred. The result of this is that V_o never manage to recharge back to 28 V until the next pulse occurs again, resulting in an even bigger transient than during the previous pulse. The current sensors are only able to measure current up to 65 A. in Fig. 4.14, the second transient is well above this limit, with a peak of 145 A, causing the current sensors to hit the limits repeatedly.

Although the system still operates, trying to compensate for the pulsating load, the large transients will eventually cause damage to the circuit resulting in a complete breakdown of the system. Fig. 4.15 shows the measured output voltage V_o and load current I_{load} during a pulsating load with a duty cycle of 10 %. When the pulse occur, the output voltage experiences a voltage drop from 28 V to approximately 26.8 V, resulting in mean power output of 1072 W. After the pulse ends, the voltage gradually recovers toward its steady state value. Small oscillations and noise are visible during and after the transient, mainly caused by switching effects. Despite the noise, the output voltage remains relatively stable throughout the pulse duration, indicating that the APF is still capable of compensating for the pulsating load under these operating conditions.

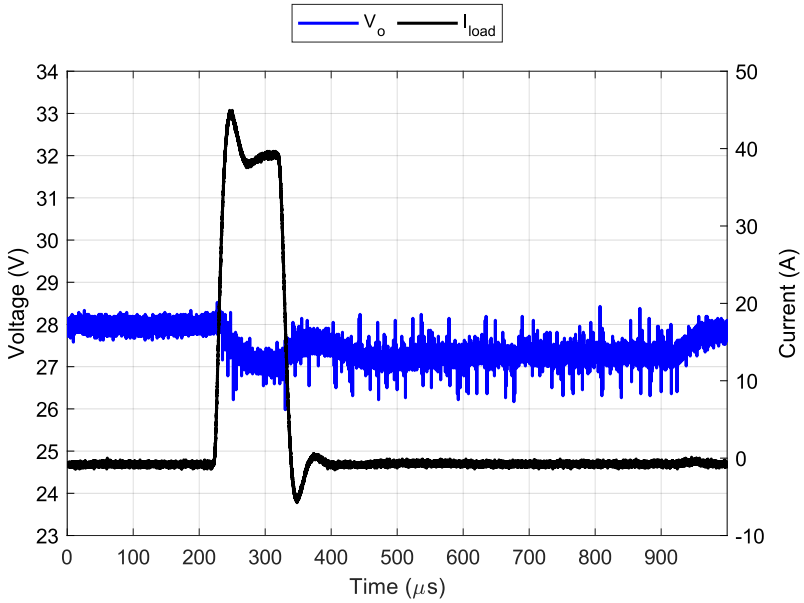

Figure 4.15: Output voltage V_o and load current I_{load} with a duty cycle of 10 %.

When the duty cycle was reduced to 9.1 %, the transients are no longer present. However, as seen in Fig. 4.16, the system still continues to discharges the voltage V_c after the pulse before the recharging begins. The voltage V_o manage to return to 28 V before the next pulse occurs and V_c is fully charged before the next pulse occurs. A small reduction in duty cycle removed the transients completely from the system during operation. During the pulse, the voltage drops to 27.1 V, resulting in a mean output voltage of 1084 W.

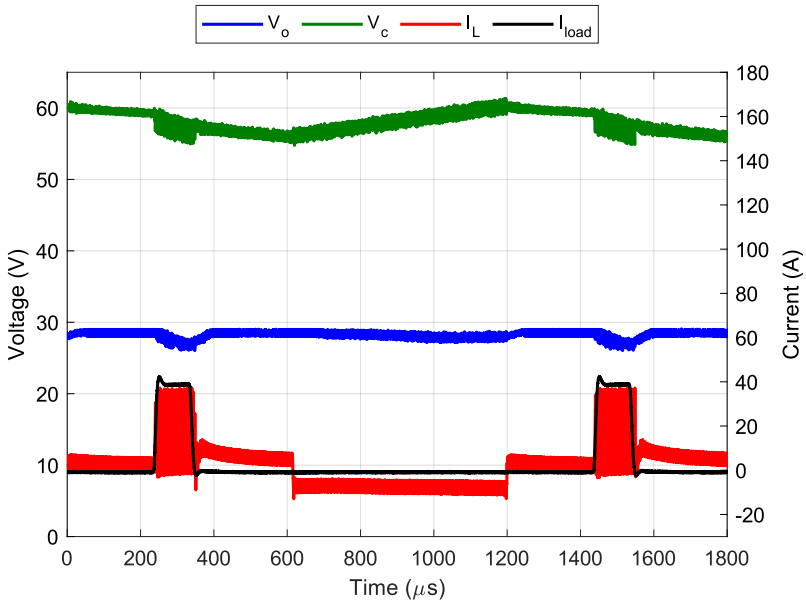

Figure 4.16: Output voltage V_o and load current I_{load} with a duty cycle of 9.1 %.

To be able to operate the APF as shown in the simulations, the duty cycle needed to be lowered to 5.00 %. The results shown in Fig. 4.17 indicates that an decrease of duty cycle results in a significantly more stable operation of the APF with the intended results. The large transient currents that occurred during the beginning of the pulsed load are no longer present and as a result, the capacitor voltage is able to recharge in a more controlled manner between the pulses.

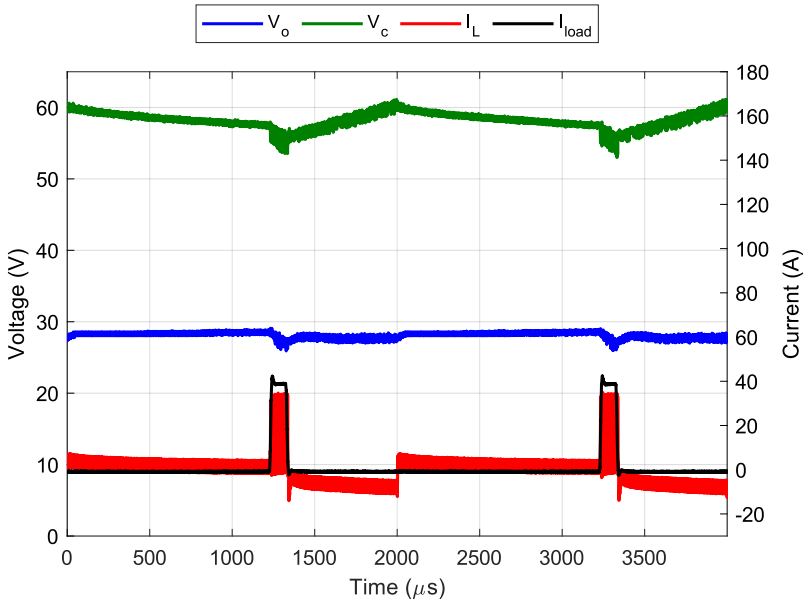

Figure 4.17: Capacitor voltage V_c, output voltage V_o and inductor current I_L during pulsating loads I_{load} with a duty cycle of 5.00 %.

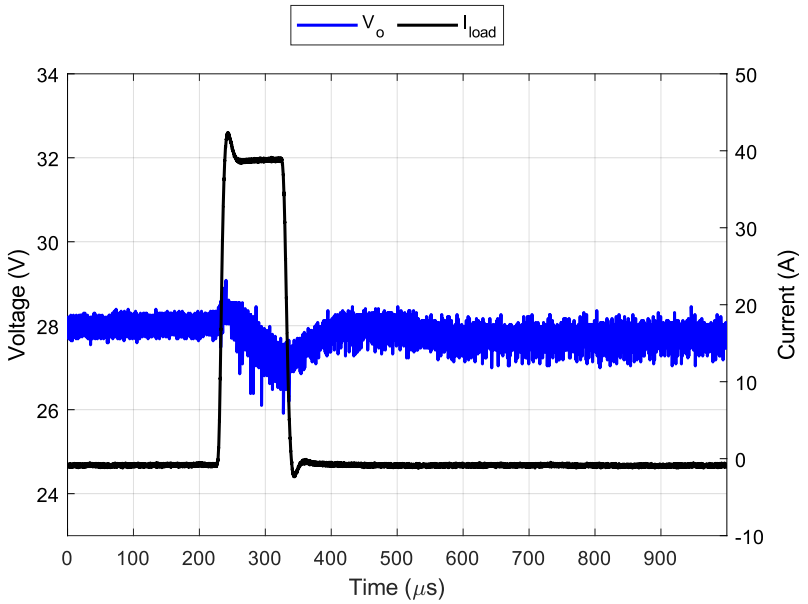

Figure 4.18: Output voltage V_o and load current I_{load} with a duty cycle of 5.00 %.

This allows the output voltage to fully recharge before the next pulse occurs and as shown in Fig. 4.18, it remain closer to its desired operating value during the pulsating load which results in a mean output power of 1084 W. Compared to the initial operating conditions, the APF no longer enters an unstable recharge behaviour where the capacitor voltage continues to decrease after the pulse. The reduced duty cycle also lowers the oscillations and switching related disturbances in the system, given a total ripple and noise is still present. Overall the response is more stable and closer to the intended design compared to when operating under the conditions in Table. 3.1. Both cases shown in Fig. 4.16 and Fig. 4.17 have the same output voltage during the pulses.

4.3 Thermal performance

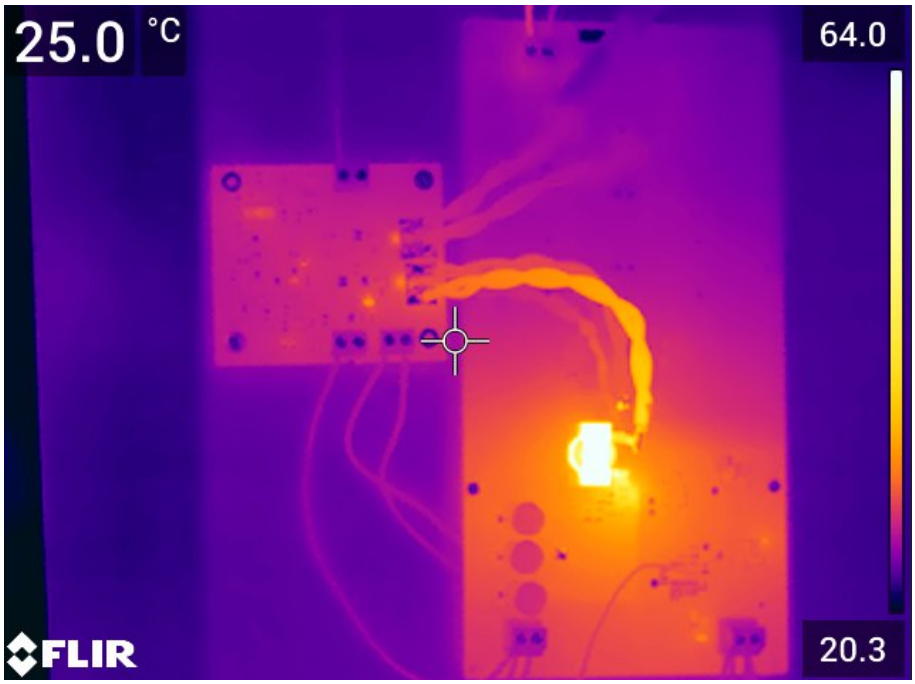

Figure 4.19: Thermal photo of the PCB using FLIR E76 Thermal camera during a duty cycle of 10 %.

During pulsating loads the temperature of the inductor reached around 64° depending on duty cycle, as shown in Fig. 4.19. A duty cycle closer to the target value of D shown in Table. 3.1, increased the temperature while lower duty cycle decreased the overall temperature of the inductor. The half-bridge located close to the inductor also experienced an increase in temperature, although to a lower value than the inductor. This indicates that switching and conduction losses provide additional thermal heating to the half-bridge. The thermal increase of the half-bridge does remain lower then the inductor, indicating that the inductor is the dominant heat generating component in the system during pulsating loads operation. The other components on the PCB stayed well below 40°, indicating that no excessive heating occurred in other parts of the circuit during operation.

5
Discussion

The results show that it is possible to construct and build an APF capable of handling 40 A pulsed loads. There are some notable differences between the simulation and the measured results. First of all the output voltage drops less in the simulation, to around 27.9 V while the measured output voltage drops to approximate 27.1 V. The reason behind this is the inductor current, in the simulation it ripples between 26 A and 30 A, this behaviour ensures that the output voltage is compensated with an appropriate amount of power. The measured inductor current ripples between 30 A and 0 A. When the signal is around 0 A, the output voltage is barley compensated with any power, which is the reason behind the extra drop in the measured output voltage. A reason for this could be an aggressive control loop, the PI-control loop settings are fixed at 56 kΩ and with an integration capacitor of 5 nF. This causes the ripple to shoot up and shoot down in an aggressive manor causing the ripple to oscillate between 30 A and 0 A. The aggressive PI-control could also be the reason for the high transients that occur in Fig. 4.14. There could also be another reason for the inductor ripple. The inductor saturates above 27 A, which causes the inductance to fall since the load pulses are 40 A. When the inductance is lowered, the current ramps up quicker and with the presence of an aggressive control loop, it could explain the results that were measured.

Another difference between simulation and measured results is the disturbances. The disturbances are non-excisting in the simulation while in the measured results they are across all signals. This is due to the fact that LTspice does not take into account electromagnetic interference (EMI) disturbances. Where there is a lot of power, there is a lot of EMI disturbances. Since this card is tested with a 40 A pulsed load, the EMI causes the already sensitive regulation to oscillate more in the measured results than in the simulated results.

There are some improvements to be made. During the verification process the problems started to arise. The voltage levels in the regulation are too close to each other and comparators trigger on a small change in voltage. An example of this is when changing a small resistor, R13, in the reference system from 1 kΩ, which caused the whole system to go from continuous operation to continuously charging the capacitor voltage, causing V_c to reach levels over 110 V. This eventually caused a flashover in the half-bridge module leading to breakdown. This was because there was always an input reference of 2.510 V to the PI-regulator. When changing R13 to 1.1 kΩ the voltage became 2.494 V and then the capacitor voltage regulated around 58 V. This small limit causes the whole regulation system to fail. This is also the

case with the PI-control loop. Optimizing the control loop with different values to improve regulation was tried, but this effort also failed due to the fact that every component is dependent on each other, in a symbiosis. Therefore the original values of the PI-control loop was kept due to time constraints. An improvement would be to design a isolated control loop where changing the values does not affect the rest of the regulation.

The APF used a dynamic limit for when V_c should start to recharge, instead of the predefined value that is used in the current design. By implementing a dynamic limit, the recharge condition could adapt depending on the conditions during operation. This would allow the APF to begin recharging earlier after a pulse has occurred even during demanding conditions. A dynamic limit could be based on the slope of the capacitor voltage V_c. Instead of only comparing V_c with the fixed limit, it could also be compared to how fast V_c is decreasing. Rapid decease does only occur during a pulse, which could be detected using a differentiator circuit and a comparator that would trigger the recharge condition if the negative slope would reach a chosen limit. Therefore allowing the recharge condition to be activated earlier, even if the fixed limit has not been reached, after a pulse has occurred.

When it comes to thermal management, the inductor gets hot. To solve this, a heat sink could be mounted underneath the two cards. When testing, the two PCB's was mounted on-top of a wooden board. which gives little thermal relief. If a heat sink was used instead, the thermal performance would improve. Another solution to help with thermal management would be to lower the switching frequency. The switching frequency at the moment is 1.2 MHz giving high switching losses and increasing the heat in the inductor. If the switching frequency was lowered to half, 600 kHz, the temperature of the inductor would decrease, due to lower switching losses. Another perk of lowering the switching frequency would be a possible improvement in the inductor ripple under the pulse. Since the heat becomes lower, it does not fully saturate, which could improve the inductor ripple, although lowering the switching frequency could also affect operation during pulsating loads.

From an environmental and sustainable perspective creating an analogue regulation PCB for an AESA radar does not have any clear impact on the environment. Though, some arguments can be made that replacing a PPF with an APF reduces capacitor volume and component size, this means an overall lower weight. In aviation weight is of critical importance since lowering weight will increasing fuel efficiency. The GaN transistors enable higher switching frequency, were smaller passive components can be used, therefore reducing the PCB size, leading to a more material efficient design.

6
Conclusion

The thesis involves the design, construction and verification of an analogue controlled APF for pulsating loads. The purpose of the work was to construct and analyse if it could maintain a stable output voltage V_o, during high current pulses. The results from both simulation and circuit implementation show that the analogue controlled APF is capable of compensating for pulsating loads and maintain V_o at the target value of 28 V during pulses. Compared to the passive power filter solution, the APF achieved improved voltage regulation while requiring smaller capacitors and reducing both volume and weight. This is important in applications such as radar systems where a small size and low weight are critical requirements.

The simulations showed that the capacitors voltage V_c remained stable at the target value of 58 V with some oscillations during steady state operation. During pulses, the APF supplied the required energy to the load while V_c decreased within the designed range before recharging between pulses. The selected method for regulation provided fast dynamic response during pulses.

During verification of the design, the constructed PCB and regulation system operated as intended. However, the target duty cycle of 10 % was not reached and the APF with the current design could only manage to operate safely without risking breakdown at 9.1 %. This shows that simulation and implementation differs, which is a valuable lesson for future work. But the verification did however prove that an APF is one of many solutions for handling high current pulsation loads. Although the APF managed to maintain V_o within it's allowed limits, several improvements can be made. The regulation system could be improved to handle transient responses and reduced voltage ripple during operation. A dynamic reference control for V_c, based on the slope of the V_c voltage, could improve recharge behaviour.

In conclusion, the thesis demonstrates that the APF is a viable solution for pulsating loads applications. The APF achieved stable operation, reduced the need of large passive components and showed that analogue control regulation, with improvements, can control fast GaNFET switching systems.

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Appendix 1

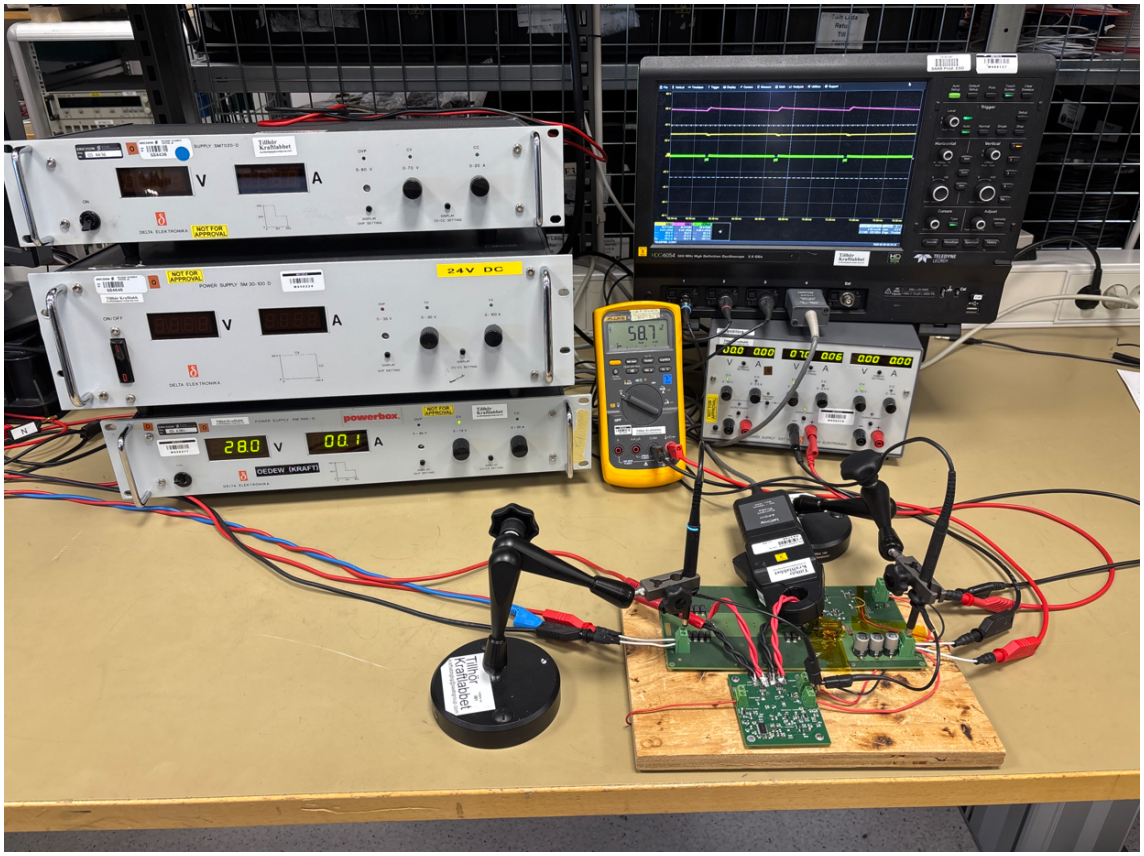

Figure A.1: Measurement set-up.

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