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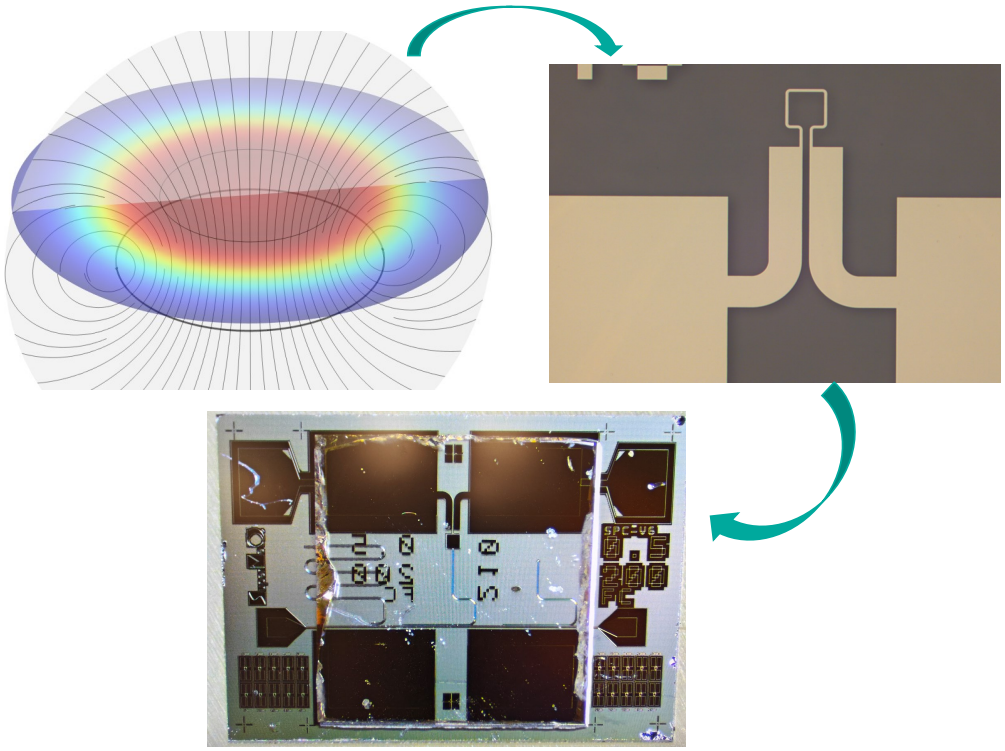

Superconducting flux transformers for the modulation of flux-tunable resonators

Master's thesis in Nanotechnology

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DEPARTMENT OF Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
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Cover: A cycle of the milestones of the thesis: a plot of the magnetic field distribution, a fabricated input coil, an assembled flip-chip.

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Abstract

Pushing the limits of quantum mechanics to larger objects is a goal of current research efforts. One approach to test the limits of quantum mechanics is to achieve quantum superposition with a macroscopic object on the order of micrometers. A possible experimental approach in this direction is given by coupling a magnetically levitated particle to a superconducting flux-tunable resonator. This system can allow us to sense the particle's motion and the flux-tunable resonator will act as the quantum sensor and the readout for the particle.
This system exploits flux coupling between the particle and the flux-tunable resonator. An approach of realizing this flux coupling is by implementing a flux transformer which is the main goal of this thesis. In this thesis we demonstrate a theoretical model to optimize the geometry of the flux transformer for maximum flux transfer efficiency. The theoretical analysis is verified with simulations on COMSOL Multiphysics. Then, a reliable fabrication recipe has been developed which had high yield of superconducting flux transformer and flip-chip devices. A novel flip-chip assembly technique was implemented with usage of Indium micro-spheres as superconducting interconnects. The thin-film of the materials used for the flux transformer and the flip-chip devices were characterized to demonstrate their superconductivity. Finally, a proof-of-principle for flip-chip based modulation of a flux-tunable resonator is demonstrated.

Keywords: flip-chip, superconductivity, nanofabrication, flux transformer, under-bump metallization.

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Karim Dakroury, Gothenburg, September 2024

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

FC	Flip-Chip
FTR	Flux-Tunable Resonator
PUL	Pick-Up Loop
TS	Transfer Stage
EBL	Electron Beam Lithography
SQUID	Superconducting Quantum Interference Device
AHC	Anti-Helmholtz Coil
UBM	Under-Bump Metallization

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Introduction

1.1 Background

Quantum sensing is a new field that would allow us to reach new realms in metrology. The idea of quantum sensing is the usage of quantum properties of a system in the measurement of a physical quantity. The quantum system is defined by quantized resolvable energy levels. A key characteristic of a quantum sensor is that its interaction with a physical quantity, such as a magnetic field, would lead to a change in the energy levels of the quantum system or a transition between levels [2]. In this thesis, the focus is on magnetic field sensing by implementing a superconducting flux transformer towards coupling a magnetically levitated particle to a superconducting flux-tunable resonator.

One of the highest precision magnetometers is the nitrogen-vacancy center (NV centers). NV centers are electronic spin defects in diamonds in which initialization and readout can be done optically. An ensemble of NV centers is predicted to have the sensitivity to measure magnetic fields $250\,\mathrm{aT}/\sqrt{\mathrm{Hz}}/\mathrm{cm}^{-3/2}$ [3] or gyroscopes with a precision of $1 \times 10^{-5}\,\mathrm{rad/s}/\sqrt{\mathrm{Hz}}/\mathrm{mm}^{3/2}$ [4, 5]. Although NV centers are promising, reaching this potential through actual devices is challenging. The two technical challenges are, first, the difficulty in efficiently detecting fluorescence for large NV ensembles [6, 7, 8]. Second, the coherence times of the spin are reduced 100 - 1000 times in high-density ensembles due to parasitic nitrogen spins that occur in high-density doping [9]. In contrast, superconducting circuits are scalable and easy to fabricate using standard nanofabrication processes. We utilize them specifically as superconducting flux-tunable resonators (FTR), which are a promising candidate as quantum sensors for magnetic fields [2, 10].

Superconducting resonators possess high intrinsic quality factors (Q_i), which allows them to be implemented in various applications such as superconducting quantum computing [11, 12], astronomical detectors [13, 14, 15] and spin resonance techniques [16, 17]. There are different approaches to implementing an FTR. An approach is to ground a superconducting resonator by shunting it through a DC superconducting quantum interference device (SQUID) [18, 19, 20, 21, 22, 23]. The DC SQUID consists of two Josephson junctions (JJs) that are in parallel in a superconducting loop. The nonlinear inductance of the JJs provides a large frequency tuning range and tuning speed [10]. An FTR can be tuned via magnetic flux. This tunability can be used for coupling an FTR to the motion of a magnetically levitated particle [24, 25].

The second system in our experiment is a magnetically levitated particle. Levitating a particle creates a highly isolated object, resulting in high mechanical quality factors and long coherence times. There exist several platforms for levitating particles; common approaches are optical and magnetic levitation. There are two main challenges with optical levitation, scattering, and absorption of photons, which lead to decoherence due to the increase in temperature [24]. Magnetic levitation exploits magnetostatic fields rather than photons, which overcomes these limitations, thereby making it a promising platform for ground-state cooling of massive particles on the order of micrometers. A micrometer-sized particle cooled to the ground state can then be used to explore the macroscopicity of quantum states through quantum superposition [26].

Quantum superposition of objects has been achieved in several experiments, such as the famous Young double-slit experiment. These experiments were performed using matter-wave interferometry [27, 28, 29]. The largest mass of the particle used in such experiments is about 10^4 amu [30]. Recently, an experiment using on-chip magnetic traps was proposed that can levitate objects $\geq 10^{13}$ amu [26]. The advantage of magnetic on-chip architecture is that it allows for an integrated coupling between the position of the center-of-mass of the levitated sphere and a superconducting circuit. This enables efficient coupling and makes it possible to cool the center of mass (COM) to the ground state [26].

It has been theoretically shown that a magnet levitated on top of a superconductor sheet in the absence of an external magnetic field can be used for ultra-sensitive force sensing with a sensitivity of $10^{-23}\ N/\sqrt{Hz}$ [31]. The proposed readout of this scheme is done using a superconducting quantum interference device (SQUID). The study shows that a smaller particle size (100 nm) results in higher force sensitivity, while a larger particle size (10 mm) gives higher acceleration sensitivity. Furthermore, it has been demonstrated that a magnetically trapped superconducting particle whose motion is controlled by a flux qubit in close proximity can be used as a gravimeter [32]. Thus, the application of such a system not only demonstrates quantum superposition in the macroscopic regime but can also be used for sensing in the quantum regime.

The third main component of the experiment is a superconducting flux transformer, which is the core of this thesis. The superconducting flux transformer plays a crucial role in transferring the flux generated from the particle's motion to the flux-tunable resonator. The question is how can we realize such a transformer with the highest possible flux efficiency. This flux transformer consists of a pick-up loop and either a single-winding or multi-winding input coil that transports the flux to the FTR. These flux transformers can be implemented in two ways: integrated on-chip (in-plane) or a flip-chip configuration (out-of-plane) in which the input coil patterned on a separate chip is assembled to the FTR chip via superconducting interconnects. The latter approach provides the possibility of multi-winding input coils, which increases flux efficiency. In addition, the fabrication process is simpler than that for in-plane flux transformers. Furthermore, it eliminates parasitic modes that are shown in the in-plane flux transformer configuration. Fig. 1.1 shows the three main components of the system and the respective fabricated devices for each part beneath it.

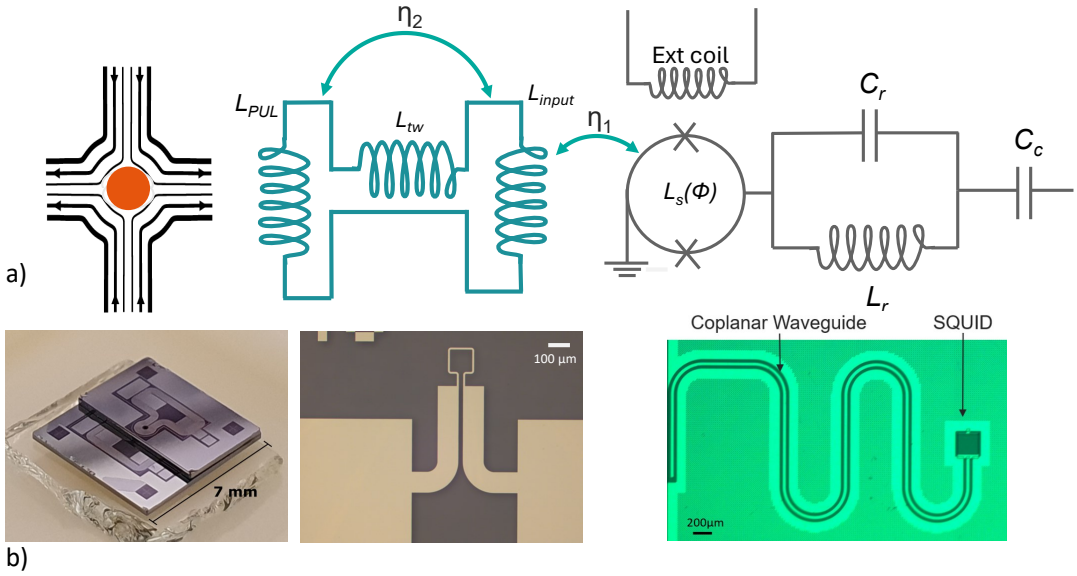


Figure 1.1: a) A schematic representation of the system: a particle trapped in a magnetic potential (left), flux transformer in blue with three inductances L_{pickup}, L_{tw} and L_{input}, the flux tunable resonator circuit in grey with a coplanar waveguide that ends with a SQUID terminated to ground. b) from left to right: a photo of the two-chip magnetic trap, an optical image of the input coil, and an optical image of the flux tunable resonator. η_2 denotes the flux transfer efficiency between the pick-up coil and the input coil, and η_1 denotes the flux transfer efficiency between the input coil and the SQUID.

1.2 State of the art

Experiments were done on flux coupling between a mechanical resonator system and a flux-tunable superconducting resonator. A very recent experiment was performed on coupling a superconducting magnetically levitated sphere of 6 µg to an FTR. In this experiment, the sphere is magnetically trapped using the bulk coil. This sphere is inductively coupled to an FTR via a flux transformer that has an efficiency of 10^{-3} from the pick-up loop (PUL) to the SQUID loop, and the achieved single-photon coupling strength is 0.7 mHz [25].

In this experiment, optimizing the geometry to increase the flux transfer efficiency is a challenge. As a result, we propose a flip-chip configuration implemented via In microsphere bonding as a part of the flux transformer. The superconducting flip-chip has been part of several experiments toward scalability and integration of quantum computing [33, 34, 35, 36] and quantum sensing [37, 38]. Indium microbumps have been widely used for superconducting flip-chips which are grown by electroplating [39, 40] or thermal evaporation [33, 34, 40, 41]. Indium microbumps require an advanced fabrication process and a high-precision flip-chip bonder to achieve a very tiny separation ($\leq$ 10 µm) and an almost uniform tilt ($\leq$ 100 µrad). Since we do not need this precision, we have developed a process in which there is no need for the fabrication of In microbumps; instead, we use In microspheres and a manual

flip-chip bonder.

Using the flip-chip technique implemented in this thesis, we predict an increase by one order of magnitude in flux transfer efficiency for a single-winding input coil and two orders of magnitude increase using multi-winding coils compared to the earlier work [25].

1.3 Thesis Goal & Objectives

The aim of this master thesis is to analyze and optimize the flux-transfer efficiency between a pick-up loop and FTR. This would pave the way for realization of coupling between a magnetically levitated superconducting microparticle and a flux-tunable resonator.

The objectives and main tasks involved in this thesis are:

- Design, simulation, and fabrication of an input coil:
  - Designing an input coil for optimum flux transport from the trap to the FTR.
  - Analyze the flux-transfer efficiency of the input coil.
  - Fabricating the flux transfer circuit.
- Developing a superconducting flip-chip interconnect:
  - Developing and realizing a fabrication recipe for the flux transformer.
  - Developing an assembly technique for flip-chips.
  - Characterization of thin-film materials used in the flux transformer.
  - Characterization of fabricated flip-chips.
- Design, analysis, and fabrication of multi-winding flux transformers:
  - Optimizing the design and enhancing the total flux transfer efficiency.
  - Developing a fabrication recipe for a multi-winding flux transformer.
- Demonstrate flip-chip based modulation of the flux tunable resonator.

2

Theory

2.1 Superconductivity

Superconductivity is a phenomenon that was discovered by Heike Kamerlingh Onnes in 1911 [42]. Superconductivity is a phase transition that occurs at a critical temperature (T_c) to a certain class of materials where two distinct properties are observed: the first is that its electrical resistance goes to zero, and the second is that it expels the magnetic field from the bulk. When cooled below their transition temperature, T_c, superconductors expel magnetic fields by inducing screening currents at the surface to cancel out the applied magnetic field. Thus, the field inside the bulk of the superconductor remains zero. As a result, superconductors are perfect diamagnets. This effect is known as the Meissner-Ochsenfeld effect (see Sec. 2.1.2), and the superconductor is said to be in the Meissner state provided that the applied magnetic field is below H_c and H_{c1} for type I and type II superconductors respectively (see Fig. 2.1).

2.1.1 Type I & II Superconductors

Superconductors can be classified as type I and type II. This distinction is primarily based on the response of the superconductor to an external magnetic field. A type I superconductor expels the magnetic field until a certain critical magnetic field (H_c) is reached, beyond which the superconductivity breaks and the material transitions into normal conducting phase. A type II superconductor has two critical magnetic fields: H_{c1} and H_{c2}. Below H_{c1}, a type II superconductor is in the Meissner state and, therefore, expels all external magnetic fields, similar to a type I superconductor. When the applied field is larger than H_{c1} but smaller than H_{c2}, a type II superconductor is in a mixed state where it exhibits flux vortices (known as Abrikosov vortices). At these vortices, magnetic flux penetrates the superconductor as a quantum of magnetic flux, thereby generating a normal current in the core of the flux vortex. These vortices are normal-conducting, whereas the rest of the bulk is superconducting. However, when the magnetic field exceeds H_{c2}, the superconductivity is fully broken, and the material transitions to its normal conducting phase. The way superconductors expel magnetic fields dictates the flow of current. For type I superconductors, the current flows only in a thin surface layer, while for type II, the current flows through the bulk.

Superconductors exhibit two main characteristic length scales: the London penetration depth (λ_L) and the coherence length (ξ). The London penetration depth

measures the depth of penetration of the magnetic field inside a superconductor (see Sec. 2.1.3). The coherence length in a superconductor is the minimum distance over which the material transitions from its fully superconducting state to its normal state. The ratio between these two parameters is used to classify the superconductor as type I if $\lambda_L/\xi < 1/\sqrt{2}$ or type II if $\lambda_L/\xi > 1/\sqrt{2}$.

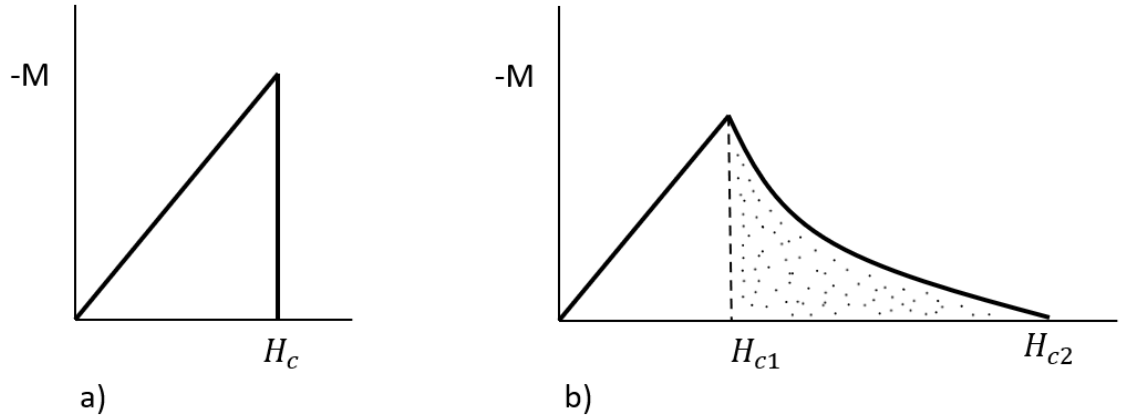


Figure 2.1: Magnetization (M) in a superconductor as a function of externally applied magnetic field (H). a) Type I superconductor induces M that is equal and opposite to H until it reaches H_c (Meissner state), beyond which M drops to zero, and the material transitions to a normal conductor. b) Type II superconductor exhibits Meissner state until H_{c1}, beyond which it enters a mixed state where flux gradually penetrates the bulk as vortices (shown as black dots). This reduces M until it reaches zero at H_{c2}, and the material becomes a normal conductor.

2.1.2 Meissner-Ochsenfeld Effect

The Meissner-Ochsenfeld effect is the phenomenon in which an applied magnetic field is expelled from the bulk of the superconductor ($B = 0$) [43]. A superconductor exhibiting such behavior is said to be in the Meissner state. This effect cannot be explained simply by treating a superconductor as a perfect electrical conductor, where the resistivity drops to zero ($\rho = 0$). This can be demonstrated using Ohm's law for a current-carrying ($\mathbf{j} \neq 0$) superconductor:

$$\mathbf{E} = \rho \mathbf{j}, \tag{2.1}$$

which implies $\mathbf{E} = 0$. Therefore, from the Maxwell-Faraday equation:

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} = 0. \tag{2.2}$$

Eq. 2.2 implies that for a perfect electrical conductor (PEC), $\mathbf{B}$ is a constant but not necessarily zero, which is observed in the Meissner effect. Therefore, a PEC cannot expel a magnetic field that is already present inside it, unlike a superconductor. Thus, the Meissner state is a fundamentally distinctive property of superconductors. As a result, superconductors deserve to be treated as a different class of materials

and explained with a distinct theory. Fig. 2.2 shows the behavior of superconductors and PEC when placed in a magnetic field, respectively.

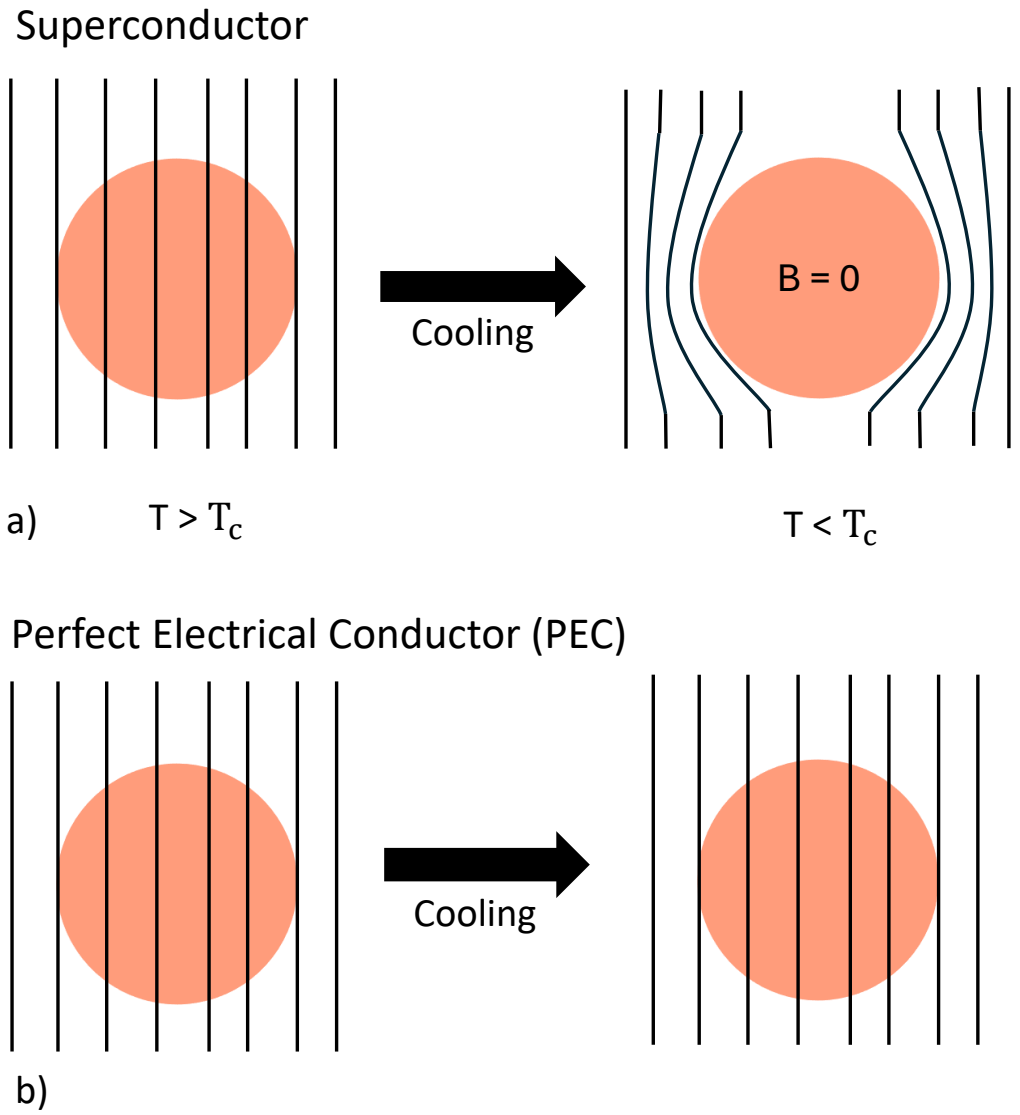


Figure 2.2: a)A type I superconductor below the transition temperature expels the applied magnetic field such that B = 0 inside the superconductor. b)A perfect electrical conductor (PEC) that allows magnetic flux density (B) to penetrate it.

2.1.3 The London Equations

These are two basic electrodynamic equations that describe the electric and magnetic fields inside a superconductor, which were proposed by Fritz and Heinz London in 1935 [44]. The first London equation describes the relation between the electric field, **E**, and the current density $\mathbf{J}_s$:

$$\mathbf{E} = \Lambda \frac{\partial \mathbf{J_s}}{\partial t} \tag{2.3}$$

where the London parameter Λ is defined as:

$$\Lambda = \frac{m}{n_s e^2} \tag{2.4}$$

where m is the mass of the superconducting electrons, n_s is the density of the superconducting electrons, e is the elementary charge.

Eq. 2.3 describes a state of perfect conductivity ($\rho = 0$) because even in the absence of an applied electric field ($\mathbf{E} = 0$), $\mathbf{J}_s$ remains constant unlike a normal conductor described by Ohm's law [45].
The second London equation describes the magnetic field, $\mathbf{B}$, with respect to the supercurrent density $\mathbf{J}_s$:

$$\mathbf{B} = -\Lambda(\nabla \times \mathbf{J_s}) \tag{2.5}$$

Now, applying Maxwell's equations:

$$\nabla \cdot \mathbf{B} = 0 \quad \text{and} \quad \nabla \times \mathbf{B} = \mu_0 \mathbf{J}_s, \tag{2.6}$$

we obtain:

$$\nabla^2 \mathbf{B} = \frac{1}{\lambda_L^2} \mathbf{B} \tag{2.7}$$

where $\lambda_L^2 = \Lambda/\mu_0$ is the London penetration depth defined in Sec. 2.1.1. Thus, from solving Eq. 2.7, we see that $\mathbf{B}$ decays exponentially from the surface of the superconductor and becomes zero inside the bulk, which explains the Meissner effect.

2.1.4 Two-fluid Model

The Two-fluid model is a phenomenological model of superconductors that was developed by Groter and Casimir. According to that model superconductors have two types of electrons: normal electrons and super-electrons. The normal electrons exhibit the same properties as electrons in metals while super-electrons have unusual and peculiar properties. Both electrons transport current, normal electrons are resistive while super-electrons have zero resistivity. The normal electrons transport heat while super-electrons are perfectly ordered and have no entropy as a result they have zero heat conductivity [46, 47].

As the critical temperature T_c is approached the density of the super-electrons n_s rise from zero given by:

$$n_s = n\left(1 - \left(\frac{T}{T_c}\right)^4\right) \tag{2.8}$$

where n is the total density of the carriers $n = n_s + n_n$.
While the density of normal electrons falls n_n see Fig. 2.3. The normal electrons and super-electrons conduct electricity in parallel thus the electrical conductivity is infinite below T_c while the thermal conductivity approches zero at $T = 0$ because all the electrons in the superconductor became super-electrons [46, 47].

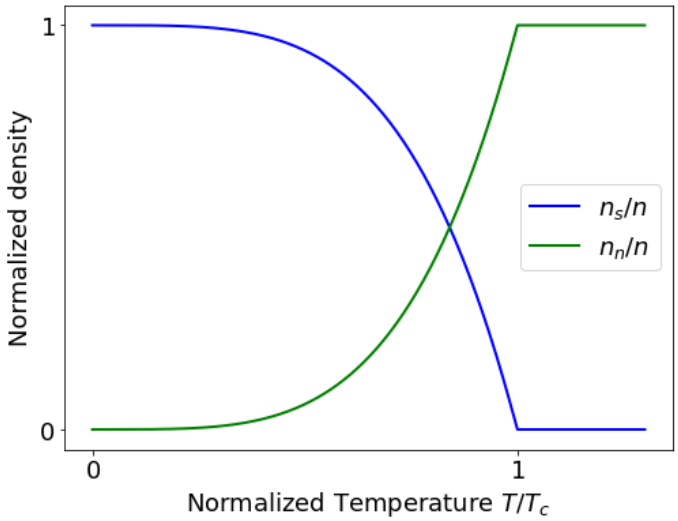


Figure 2.3: A plot of the two-fluid model that shows the temperature dependence of the super-electron density n_s and normal electron density n_n

2.1.5 Proximity Effect

The proximity effect occurs when a superconductor is in contact with a normal conducting metal. The proximity effect influences the transition temperature T_c of a superconducting system by effectively lowering it at the interface between the superconductor and the normal conducting metal. This occurs because the superconducting correlations leak into the normal metal. As a result, the superconductor's ability to maintain long-range order is weakened which reduces the overall transition temperature T_c of the system [48, 49].

2.2 Flux Calculation

This section explains the analytical equations used to calculate the magnetic field generated by a circular current-carrying loop and the magnetic flux passing through another circular loop that is placed nearby. This simple model will be used to analytically estimate the flux inside a SQUID loop generated by an input coil (see Sec. 2.3.3)

2.2.1 Biot Savart Law

The magnetic flux is defined as the number of magnetic field lines passing through a certain area. This can be described mathematically as the surface integral of the magnetic field vector ($\mathbf{B}$) over a surface ($\mathbf{S}$):

$$\Phi = \iint_S \mathbf{B} \cdot \mathbf{dS} \tag{2.9}$$

We consider a circular loop, called an input coil, which carries current $\mathbf{I}$ and generates a magnetic field $\mathbf{B}$. The center of this loop is at the origin of a cylindrical coordinate

system. Another circular loop, called SQUID, is placed at a position (r, θ, h). The assumptions made for this system are:

1. Both coils are treated as a one-dimensional circle (zero width and thickness),
2. No Josephson junctions or other elements are considered,
3. Superconductivity and Meissner effect are neglected.

A schematic of the system is shown in Fig. 2.4.

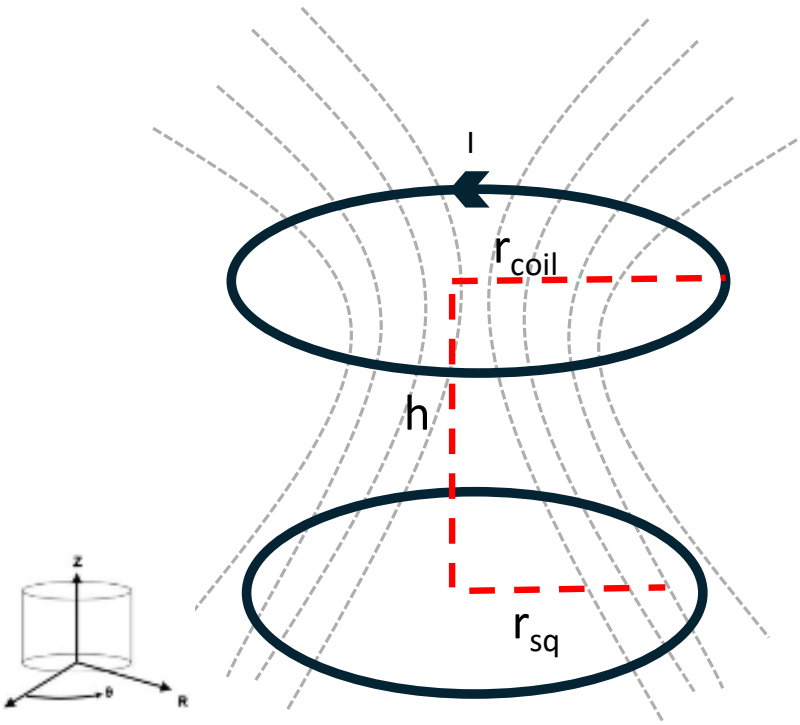


Figure 2.4: A schematic of the system where r_{coil} is the radius of the input coil, r_{sq} is the radius of the SQUID, and h is the axial separation between the two coils. The magnetic field (grey dotted lines) generated by the input coil partially passes through the SQUID.

A coil of radius r_{coil} carrying a current I generates a magnetic field that penetrates a SQUID of radius r_{sq}, where both coils are separated by a distance h. The generated field is given by:

$$B_z = B_0 \frac{1}{\pi\sqrt{Q}}[E(k)\frac{1-\alpha^2-\beta^2}{Q-4\alpha} + K(k)] \tag{2.10}$$

$$B_r = B_0 \frac{\gamma}{\pi\sqrt{Q}}[E(k)\frac{1+\alpha^2+\beta^2}{Q-4\alpha} - K(k)] \tag{2.11}$$

We use the following abbreviations:

$$\alpha = \frac{r_{sq}}{r_{coil}}, \beta = \frac{h}{r_{coil}}, \gamma = \frac{h}{r_{sq}} \tag{2.12}$$

$$Q = [(1+\alpha)^2 + \beta^2], \tag{2.13}$$

$$k = \sqrt{\frac{4\alpha}{Q}}, \tag{2.14}$$

$$B_0 = \frac{\mu_0 I}{2r_{coil}}. \tag{2.15}$$

The parameters used in the above equations are:

- B_0 is the magnetic field in the center of the coil
- I is the current flowing in the input coil.
- r_{coil} is the radius of the input coil.
- μ_0 is the permeability of free space.
- h is the distance in the axial direction from the center of the input coil to the center of the SQUID.
- r_{sq} is the distance in the radial direction from the center of the DC SQUID to the boundary of the circle.
- $K(k)$ is the complete elliptic integral function of the first kind.
- $E(k)$ is the complete elliptic integral function of the second kind.

The parameters α, β, and γ defined in Eq. 2.12 are unitless quantities defined by geometric parameters. The fields $\mathbf{B_z}$ and $\mathbf{B_r}$, obtained in Eq. 2.10 and Eq. 2.11, are the axial and radial magnetic field components, respectively. We neglect $\mathbf{B_r}$ since $\Phi = \mathbf{B_r} \cdot \mathbf{A} = 0$. Therefore, only the axial magnetic field component $\mathbf{B_z}$ contributes to the flux inside the DC SQUID. Thus, the total flux inside the SQUID will be the surface integral of $\mathbf{B_z}$ in the cylindrical coordinate system:

$$\Phi = \int_0^{2\pi} \int_0^{r_{sq}} \mathbf{B_z}\ r\ dr\ d\theta \tag{2.16}$$

Eq. 2.16 will be used in Sec. 4.1 to compute the flux transfer efficiency between the input coil and the SQUID.

2.3 Superconductivity Toolbox in Quantum Sensing

This section delves into the main components used towards quantum sensing with a levitated particle and utilizing superconducting devices. Firstly, the physics of a superconducting levitated particle, which acts as a mechanical resonator, will be explained. Then, superconducting coplanar waveguides (CPW), which are used as a microwave resonator, will be explained followed by flux-tunable resonators which are special superconducting microwave resonators terminated by a DC SQUID.

2.3.1 Levitated Particle

Diamagnetic materials oppose external magnetic fields. Diamagnets of magnetic susceptibility χ and volume V placed in a magnetic field $\mathbf{B}$, have the following energy assuming that they are a point particle [50]:

$$U = -\frac{\chi B^2 V}{2\mu_0} + m_p g z \tag{2.17}$$

where μ_0 is the permeability of free space, m_p is the mass of the particle, g is the gravitational acceleration, z is the position of the object.

For objects to levitate the magnetic force should be equal in magnitude and opposite in direction to the gravitational force:

$$\mathbf{B}\nabla\mathbf{B} = \mu_0 g \frac{\rho_p}{\chi}\hat{\mathbf{e}}_\mathbf{z} \tag{2.18}$$

where ρ_p is the density of the particle and $\hat{\mathbf{e}}_\mathbf{z}$ is the unit vector in the vertical direction.

Apart from the force balance criterion the levitation stability is another requirement that is equally important. It is fulfilled when:

$$\nabla^2 U = -\frac{\chi V}{2\mu_0}\nabla^2 B^2 > 0 \tag{2.19}$$

From Eq. 2.19 it is clear that only diamagnets satisfy this condition as they have $\chi < 0$. Superconductors fulfill this condition as they are perfect diamagnets with $\chi = -1$.

In this thesis the superconducting particle is levitated in an anti-Helmholtz coil configuration (AHC) which can be modeled as two coils that carry current I in opposite directions. These coils generate a magnetic field that creates a magnetic force on the sphere to levitate. The oscillation of the particle disturbs the magnetic field thus it changes the flux threaded in a pick-up loop (PUL) that is placed on top of the AHC.This change in flux induces a current inside the PUL. A figure of the AHC system is shown in Fig. 2.5.
Assuming $R \ll l$ and that the particle has a small displacement in the y-axis direction ϵ_y the flux threaded inside the PUL is given by [24]:

$$\Phi_{ext} = \frac{48 I \mu_0 \pi}{25\sqrt{5} l^2}\left[\frac{d R^5 r^2}{(d^2+r^2)^{\frac{5}{2}}} + \epsilon_y\left(\frac{R^5 r^2(-4d^2+r^2)}{(d^2+r^2)^{\frac{7}{2}}} - \frac{R^3 r^2}{(d^2+r^2)^{\frac{3}{2}}}\right)\right] \tag{2.20}$$

Then the change of the flux as function of the particle's position is given by [24]:

$$\Phi'_{ext} = \frac{\partial \Phi_{ext}}{\partial \epsilon_y} \simeq \frac{-48 I \mu_0 \pi R^3 r^2}{25\sqrt{5} l^2 (d^2+r^2)^{\frac{3}{2}}} \tag{2.21}$$

In Eq. 2.21 we neglect the term proportional to R^5 as it is very small. From Eq. 2.21 one can obtain the induced current inside the PUL with respect to the particle's position provided that the inductance of the PUL is known.

2.3.2 Coplanar Waveguides (CPW)

A coplanar waveguide (CPW) is a microwave transmission line consisting of a central conductor of width w and a ground plane on either side of the central conductor separated by a gap s; see Fig. 2.6. A CPW can be used as a microwave resonator with

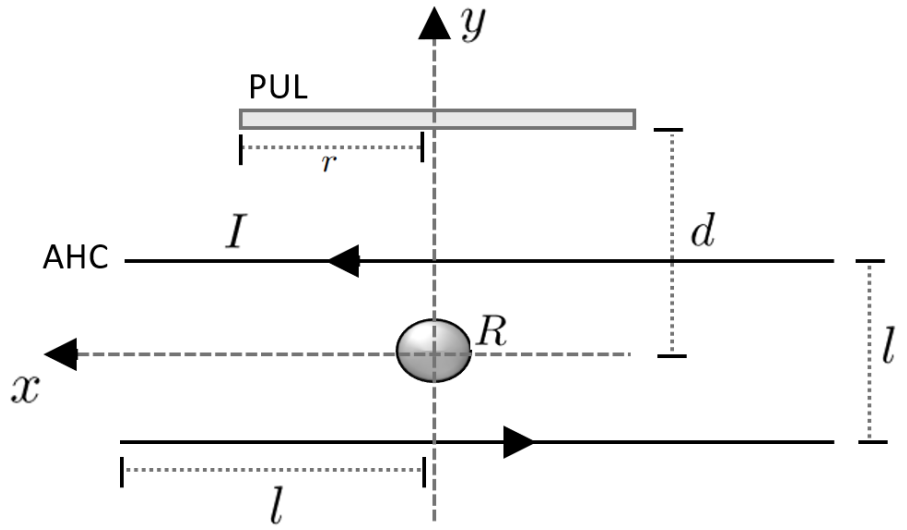


Figure 2.5: A cross-section of an AHC system that shows a superconducting levitated particle of radius R. Two black lines are the two coils carrying current I in opposite directions. The separation between the coils is denoted by l and the distance d is the distance between the particle and the PUL.

appropriate boundary conditions such that it absorbs energy at a certain resonance frequency (ω_0). A CPW can be either a half-wave or a quarter-wave resonator. A half-wave resonator is terminated with an open circuit of the resonator such that there are nodes on both ends of the resonator. while a quarter-wave resonator is terminated by a grounded short circuit such that it has a node at the ground terminal and an anti-node at the coupling capacitor.

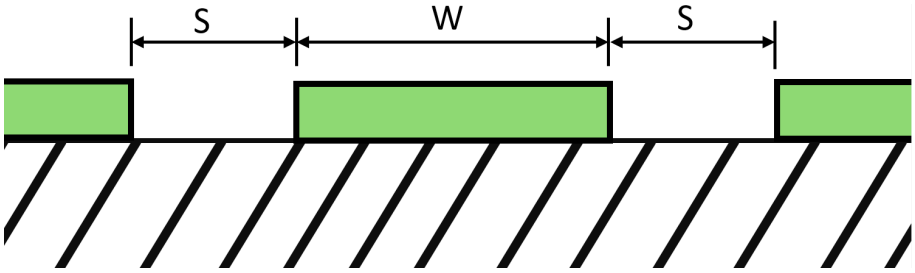


Figure 2.6: Cross-section of a CPW. A central conductor of width w which is separated by a gap s from the two ground planes on both sides. The substrate is illustrated in black stripes and the superconducting material in green.

From transmission line theory, a coplanar waveguide can be modeled as an LC circuit, which has an inductance per unit length (L_l) and capacitance per unit length (C_l). From [51, 52]:

$$L_l = \frac{\mu_0}{4}\frac{K(k_0')}{K(k_0)}, \tag{2.22}$$

$$C_l = 4\epsilon_0\epsilon_{eff}\frac{K(k_0)}{K(k_0')}, \tag{2.23}$$

where K denotes the complete elliptic integral of the first kind with the arguments k_0 and k_0':

$$k_0 = \frac{w}{w + 2s}, \tag{2.24}$$

$$k_0' = \sqrt{1 - k_0^2}. \tag{2.25}$$

The total inductance and capacitance of the CPW is given by [53, 54]:

$$L = \frac{8L_l l}{\pi^2} \tag{2.26}$$

$$C = \frac{C_l l}{2} \tag{2.27}$$

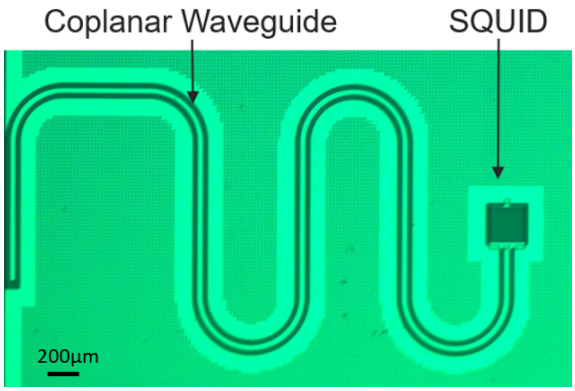
where l is the length of the CPW.

The total inductance and capacitance determine the resonance frequency (ω_0) which is given by [55]:

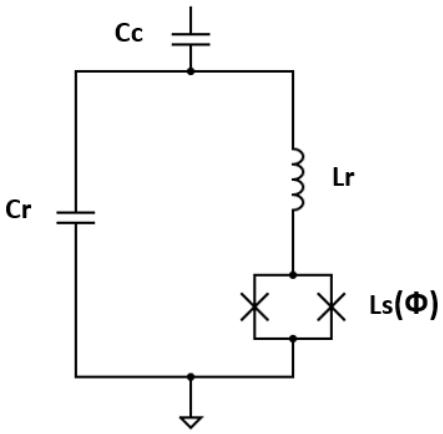
$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.28}$$

2.3.3 Flux Tunable Resonator (FTR)

A flux tunable resonator in this work is a superconducting quarter-wave CPW resonator that is terminated with a DC SQUID in series to ground [18]. A DC SQUID consists of two Josephson junctions in a superconducting loop and acts as a nonlinear flux-tunable inductor. The length of the CPW and the Josephson junctions determine the resonance frequency of the resonator and the flux sensitivity of the DC SQUID determines the shift in the resonance frequency as a result of the change in the inductance of the SQUID, thus a change in the total inductance.



(a) Image of an FTR with a CPW & a DC SQUID.



(b) A circuit representation of an FTR.

Figure 2.7: a) shows a fabricated FTR and b) shows a circuit diagram for an FTR.

The inductance of a Josephson junction is tunable via flux:

$$L_j(\Phi) = \frac{\Phi_0}{2\pi I_c \cos(\frac{\pi\Phi}{\Phi_0})} \tag{2.29}$$

where Φ_0 is a quantum of magnetic flux, I_c is the critical current. A DC SQUID has two Josephson junctions in parallel, therefore the inductance of the SQUID is:

$$L_s = L_j/2 \tag{2.30}$$

Thus, the resonance frequency of the FTR is tunable via flux:

$$\omega_0(\Phi) = \frac{1}{\sqrt{(L_r + L_s(\Phi) + L_{geo})C_r}} \tag{2.31}$$

where L_r is the total inductance of the CPW, L_{geo} is the geometric inductance of the SQUID loop, C_r is the total capacitance of the CPW.

The FTR's eigenfrequency ω_c can be determined by solving the following transcendental equation [56, 57, 58]:

$$\frac{\pi\omega_c}{2\omega_0} \tan \frac{\pi\omega_c}{2\omega_0} = \frac{(2\pi)^2}{\Phi_0^2} L_r E_s(\Phi_{ext}) \tag{2.32}$$

where E_s is the flux dependent energy of a DC-SQUID given by:

$$E_s(\Phi_{ext}) = \frac{\Phi_0^2}{(2\pi)^2} \frac{1}{L_s(\Phi_{ext}) + L_{geo}/4} \tag{2.33}$$

A Laurent expansion of the left-hand side (L.H.S) of Eq. 2.32 for $\omega_c/\omega_0 \approx 1$:

$$\frac{\pi\omega_c}{2\omega_0} \tan \frac{\pi\omega_c}{2\omega_0} \approx -\frac{1}{\frac{\omega_c}{\omega_0} - 1} - 1 + \mathcal{O}\left(\frac{\omega_c}{\omega_0} - 1\right) \tag{2.34}$$

Substituting Eq. 2.34 in L.H.S of Eq. 2.32, neglecting higher order terms and solving for ω_c gives:

$$\omega_c(\Phi_{ext}) = \omega_0 \left(\frac{L_r}{L_r + L_s(\Phi_{ext}) + L_{geo}/4} \right) \tag{2.35}$$

Eq. 2.35 describes the change in resonance frequency of a flux tunable resonator as a function of the applied external flux. By comparing Eq. 2.35 to Eq. 2.31 we see that the $L_s(\Phi_{ext})$ is the term that causes the modulation of the resonance frequency of the FTR.

3

Methods

This chapter discusses the methods used in this thesis. First, the microfabrication process of thin films will be introduced, which gives a detailed overview of different fabrication techniques. Second, we will describe the bonding technique that we developed in-house to bond superconducting flip-chips. Finally, the experimental setup will be explained, including how the samples were assembled and characterized for the characterization of thin films and modulation of flux-tunable resonators.

3.1 Microfabrication

This section details the fabrication process used to fabricate the devices mentioned in this thesis. These processes were developed to fabricate superconducting thin films with patterned input coil and under-bump metallization (UBM) pads. These structures were designed to develop superconducting flip-chip (FC) devices as a part of a flux-transfer circuit. The thin film material used to fabricate the UBM and the coil was either Nb or NbN. Both materials were fabricated with and without an Au passivation layer deposited in the same vacuum. A silicon substrate is used for the bottom chip and sapphire substrate for the top chip because its transparency allows for alignment in transfer stage-based flip-chip bonding (see Sec. 3.2). Fig. 3.1 shows The full material stack used for the superconducting flip chip (FC).

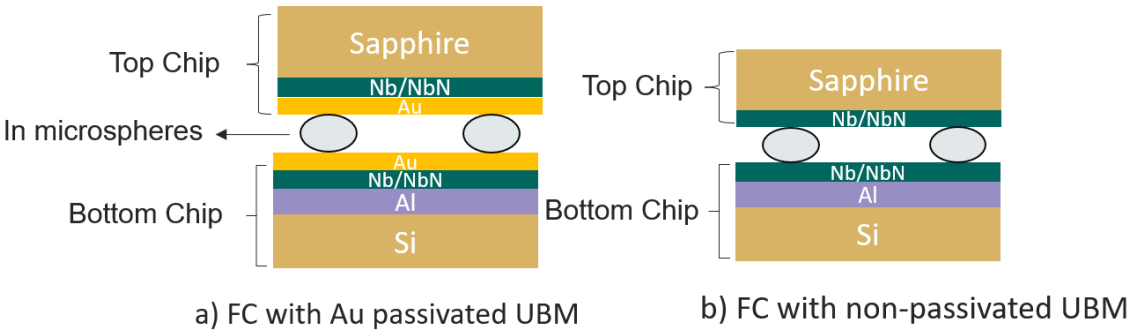


Figure 3.1: The FC consists of two chips, top and bottom, with In microspheres sandwiched in between. Top chips are fabricated on sapphire substrates, while bottom chips are fabricated on Si substrates. The bottom chip consists of Al for the wiring layer, Nb or NbN for UBM, and Au for passivation. Top chip consists of Nb or NbN for patterning coils and Au layer for passivation.

3.1.1 Etching Process

Etching is a well-established fabrication technique that consists of two main forms: dry etching and wet etching. Dry etching is a process that involves gas reactants to etch certain materials. Wet etching is a process that involves liquid chemicals for etching. In the etching process, the material is first deposited and then patterned with a resist mask using lithography tools. This is followed by removal of the deposited material from the undesired regions by etching. Fig. 3.2 shows the steps involved in a general etching process.

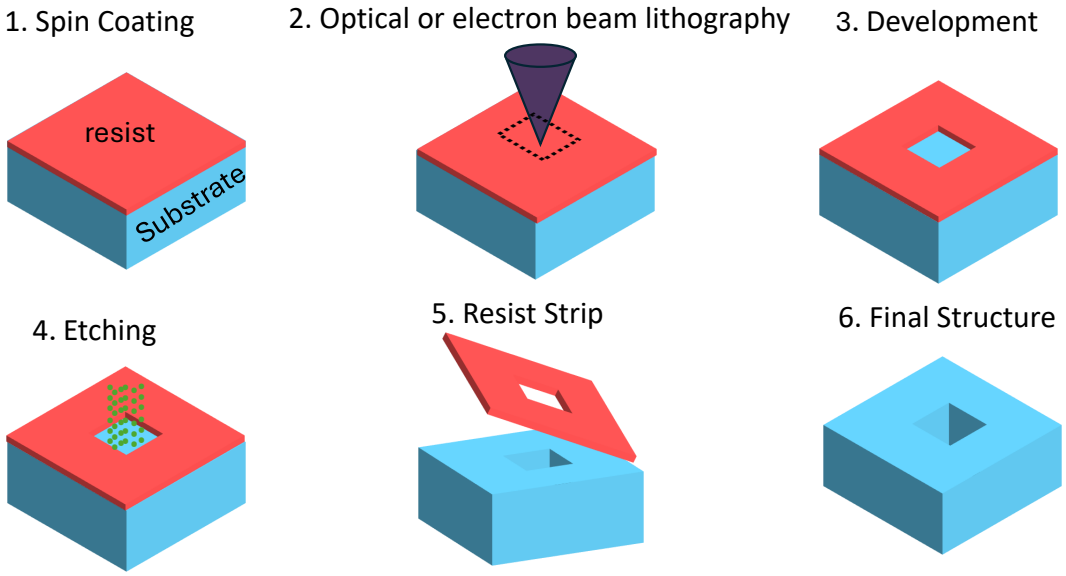


Figure 3.2: Schematic of a generic etching process.

A dry etching-based fabrication process was used to fabricate the UBM on the bottom chip and the input coil on the top chip. We used xenon difluoride gas (XeF_2) as an etchant for Nb and NbN. XeF_2 is a typical etchant for Si, Ge and Mo. However, XeF_2 has also been shown to etch Nb [59] and NbN [60].

In this process, Nb was sputtered by a DC magnetron in a vacuum chamber. The next step was to spin coat the resist S1813. This is followed by optical lithography, which was performed using a UV laser writer. Then, the development is carried out by immersing the chips in MF-319. The chips were then placed in a Memstar XeF_2 dry-release etch. Finally, the resist is removed using remover 1165. Fig. 3.3 shows a step-by-step for the etching process. For the detailed fabrication parameters see App. A.

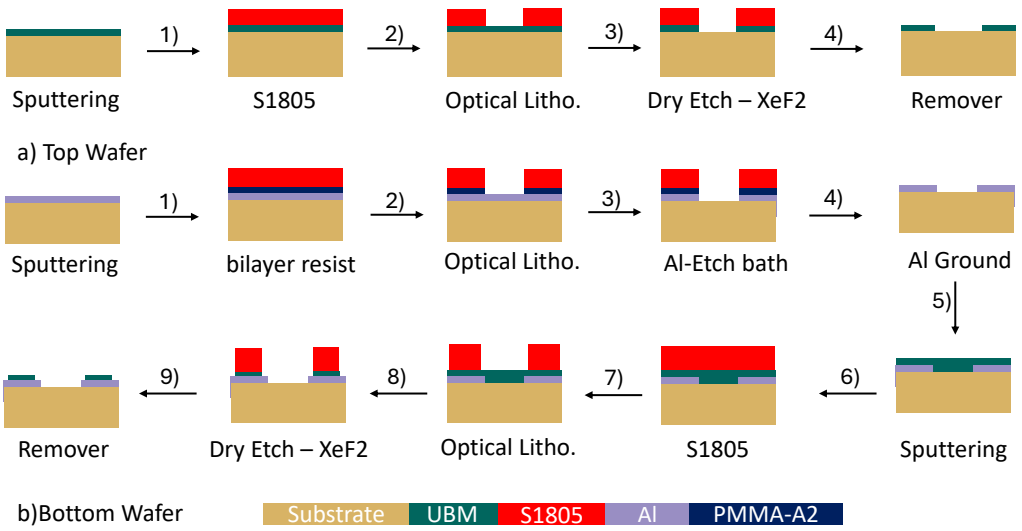


Figure 3.3: Schematic of the etching process.

3.1.2 Lift-off Process

The lift-off process is a fabrication technique that is widely used in patterning thin films using photo-resist as a sacrificial layer. In the lift-off process, the resist mask is patterned before the thin film is deposited. After deposition, the resist (sacrificial layer) is lifted off by dissolving it in a solvent, leaving only the metal deposited in the desired regions. The main advantage of lift-off is that it can be used with materials that are hard to etch. In addition, liftoff prevents damage to other layers of the chip, which are susceptible to etching. Fig. 3.4 shows the steps involved in a general lift-off process.

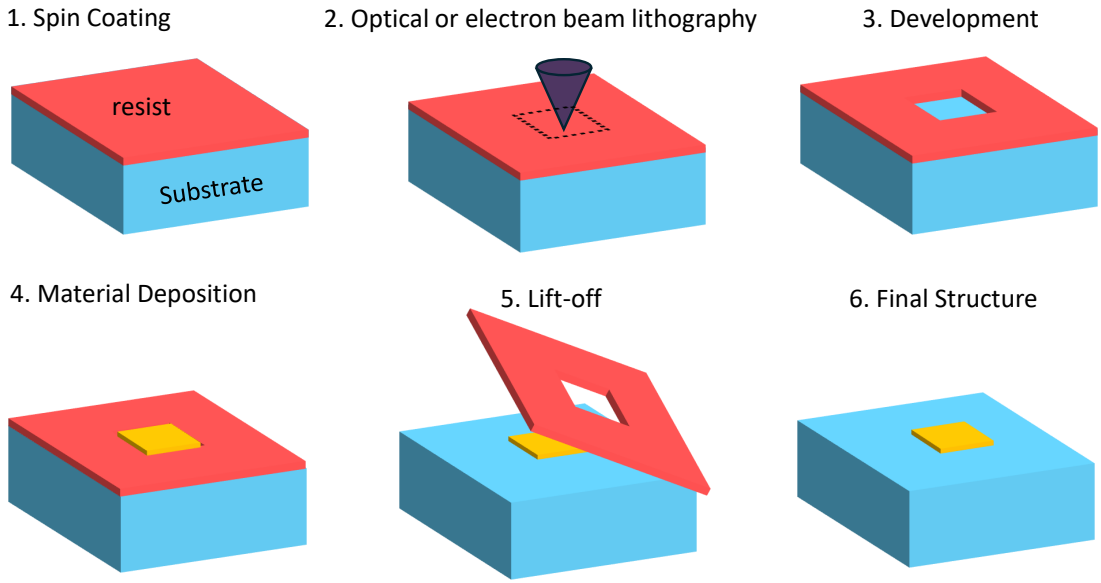


Figure 3.4: Schematic of a generic liftoff process.

3.1.2.1 Liftoff using e-beam lithography

Two wafers are patterned independently on two different substrates, silicon and sapphire, using electron beam lithography (EBL).

The top chip is patterned on a sapphire wafer. First, a bilayer EBL resist, EL6 (µm) & PMMA-A6 (µm), is spin-coated. The EL6 resist provides an undercut that is necessary for the lift-off process and also prevents sidewall deposition. Since sapphire is transparent and insulating, a thin layer of chromium (Cr) is deposited on top of the resist by thermal evaporation. This eases alignment on the EBL cassette and prevents charge accumulation. The UBM and coil are then patterned using EBL, followed by etching the Cr layer using a Cr etchant and developing in MIBK:IPA. The wafer is descummed in O_2 plasma to ensure the removal of any residual resist. The deposition process takes place using a DC magnetron. Reactive sputtering is performed by flowing N_2 gas inside the chamber to deposit NbN. The Au capping layer is then deposited on top of the UBM for devices with passivation. Finally, remover 1165 is used to lift off the resist accompanied by a low-power ultrasonic cleaning of the wafer.

The bottom chip is patterned on a silicon wafer. Firstly, the Al wiring layer is sputtered, followed by spin coating of the S1805 resist, patterning with optical lithography, and development using MF-319. This wiring layer contains the pads for wirebonding. After development, the wafer is treated in O_2 plasma to remove resist residue. Later, the wafer is soaked in an Al etch bath to pattern the wiring layer. Wafer cleaning is performed before patterning the UBM layer. The rest of the steps are exactly the same as the top chip, except that there is no need for deposition of Cr because silicon is not transparent. In addition, ion milling is performed prior to sputtering the UBM to strip off the native oxide of the Al to make galvanic contact between the two layers. Fig. 3.5 a step-by-step schematic of the lift-off process.

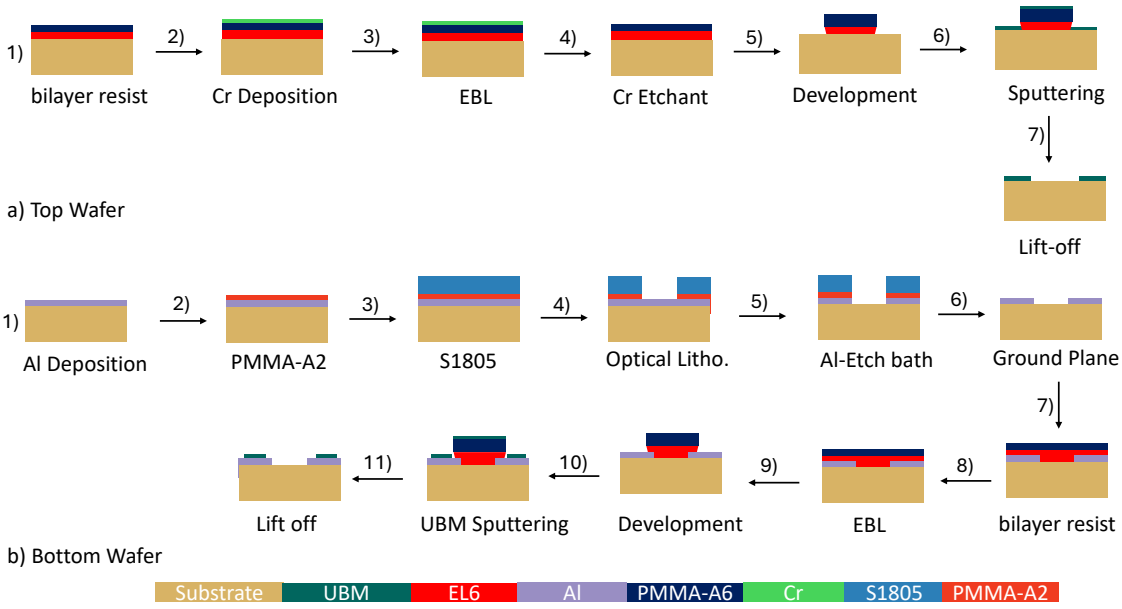


Figure 3.5: Schematic of the EBL Lift-off process.

This process requires the additional step required for Cr deposition on the top chip and etching as well as long exposure time in the EBL. As a result, a new process was developed using optical lithography to simplify the process and reduce the fabrication time. For the detailed fabrication parameters see App. A.

3.1.2.2 Liftoff using optical lithography

Two wafers are independently patterned on two different substrates, silicon and sapphire, using optical lithography.

The top sapphire wafer is spin-coated by a bilayer resist consisting of lift-off resist LOR 3A & SPR 220. The LOR 3A creates an undercut responsible for lifting off the resist. After that, optical lithography is performed using a UV laser writer. The wafer is developed in MF-24A. After development, the wafer is flood-exposed using a UV lamp. This is a important step because it prevents bubbling of the resist due to trapped nitrogen during UBM deposition. Then, the wafer is descummed in O_2 plasma. The deposition of the UBM layer is performed in a DC magnetron sputtering tool as discussed above. Finally, the lift-off is done using remover 1165, followed by ultrasonic cleaning.

The bottom chip wiring layer is patterned using the same process mentioned in Sec. 3.1.2.1 steps (1-6). This is followed by the same process of the top chip for patterning the UBM. Fig. 3.6 is a step-by-step schematic of the process.

This process has a higher yield than the other two processes and is also fast because it has fewer steps and a very short lithography time. For detailed fabrication parameters, refer to App. A.

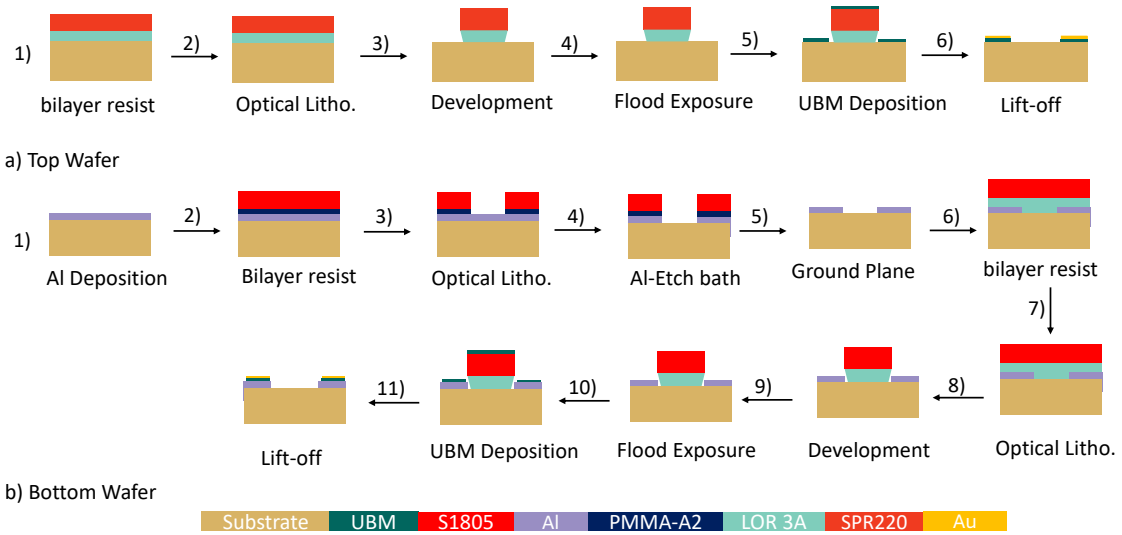


Figure 3.6: Schematic of the Lift-off process.

3.1.3 Multilayer Process

The multilayer process was developed to create a superconducting connection with a cross-over using an insulating layer between the two conducting layers. The material used for the conducting layers is NbN, and that for the insulating layer is SiO_2. In this process, three film layers need to be patterned. The first layer is 50 nm of NbN. The first layer is patterned using the LOR-3A & SPR 220 lift-off process Sec. 3.1.2.2. The second layer of SiO_2 was patterned using the same lift-off process Sec. 3.1.2.2. Here, a 75 nm SiO_2 is deposited on top of the NbN using plasma-enhanced chemical vapor deposition (PECVD). Finally, the third layer of 90 nm NbN is patterned using the same lift-off process Sec. 3.1.2.2. Fig. 3.7 shows the major steps in the multilayer fabrication process of the three layers NbN-SiO_2-NbN.

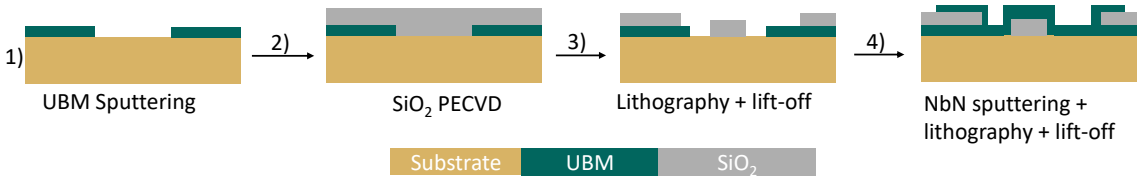


Figure 3.7: Schematic of the Multilayer fabrication process.

3.2 Flip Chip Assembly

This section is an overview of the technique developed to bond flip chips. We use indium microspheres [61] to form superconducting interconnects between two chips by applying a flip-chip bonding technique that we developed. The bonding is done using a homemade transfer stage as well as a manual flip-chip bonder for comparison. The design of the top and bottom chips is shown in Fig. 3.8. The top chip consists of an input coil, and the bottom chip consists of the wiring layer, which is Al, and the UBM. The essential criterion for a successful flip-chip bond is to have a mechanically sturdy and fully superconducting connection between the two chips. In addition, vertical separation, lateral misalignment, and tilt between the two chips must be as small as possible.

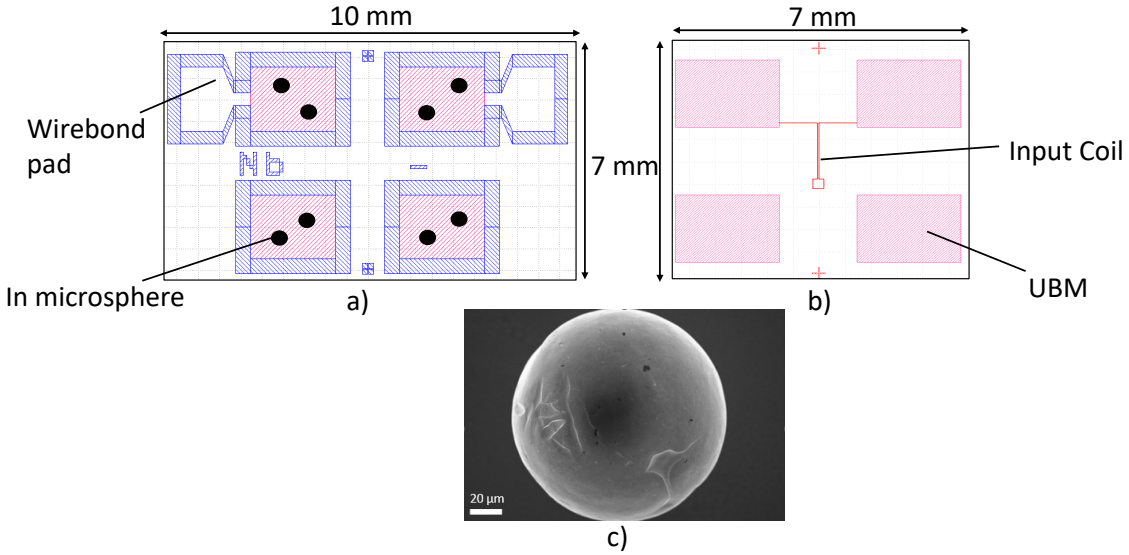


Figure 3.8: (a) CAD design of the bottom chip with In microspheres (solid black) placed manually on the UBM pads, and Al pads for wirebonding. (b) CAD design of the top chip with input coil and the UBM pads patterned on the same layer. The UBM material on both chips is either Nb or NbN, which can also be passivated with Au. c) An SEM image of a 300 μm diameter In microsphere.

3.2.1 Bonding with transfer stage

The transfer stage bonder is built using an XYZ micromanipulator stage that is primarily used to transfer 2D materials [62]. It consists of two micromanipulators, a camera-equipped microscope, a vacuum, and a heat source on the bottom surface.

Firstly, the bottom chip is held in-place by vacuum while the top chip is stuck to a metal plate using polydimethylsiloxane (PDMS) tape. Then, the In particles are placed on the pads of the bottom chip. Two micromanipulators are used to translate the chips in the lateral directions. A microscope is used to align both chips on top of each other. The transparent sapphire top chip allows for direct vertical alignment of the two chips. Once alignment is achieved, a heater is used to heat the bottom chip to 110 °C which is below the melting point of In at 156 °C [63]. This softens the In particles, allowing them to deform when pressed. Finally, the top chip is pressed down on the bottom chip with an uncalibrated force using the z-translation of the micromanipulator until both chips are perfectly in focus, indicating their vertical proximity.

The transfer stage's advantage is that it is a simple process and allows for continuous monitoring and correcting the alignment while bonding. The drawbacks are that the force applied is uncalibrated, and the top chip needs to be transparent for alignment.

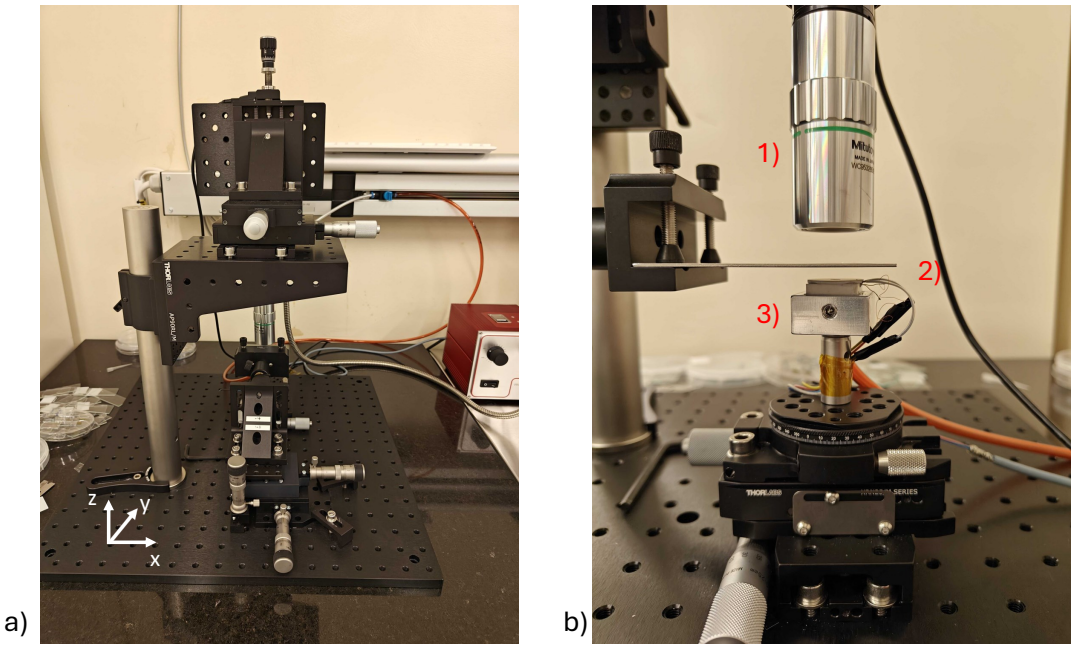


Figure 3.9: a) A photo of the transfer stage b) The three main components of the transfer stage: 1) a microscope for alignment, 2) a micro-manipulator with a plate with PDMS tape to hold the top chip, 3) a micromanipulator with a plate with vacuum to hold the bottom chip.

3.2.2 Bonding with flip-chip bonder

The flip-chip bonder is a commercial tool designed for bonding flip-chips and is commonly used in the industry for the 3D packaging of chips. The flip-chip bonder used in this thesis is a manual flip-chip bonder from the FINEPLACER 96 model 'Lambda'. It consists of three micromanipulators, a microscope, a beam splitter, two independent heat sources, vacuum lines for the top and bottom surfaces, and a lever with a pre-calibrated force.

First, the bottom chip is placed on the bottom plate, which is held by Kapton tape in addition to the vacuum. The top chip is then picked up using a pick-up tool that has a vacuum to hold the top chip. Finally, the In microspheres are placed on the bottom pads. After that, alignment is performed using two micromanipulators in the x-y coordinates and a third one for the rotation correction. The microscope and the beam splitter are used to align both chips using alignment markers. Finally, the top chip is pressed against the bottom chip using a lever that can be adjusted to a calibrated force ranging from 0 N to 100 N. The forces applied for the flip-chips in this thesis were 50 N and 65 N, which correspond to the pressure of 60 MPa and 80 MPa, respectively. These forces were applied on the basis of trial and error with the goal of achieving the lowest chip separation.

The advantage of the flip-chip bonder is that heat can be applied separately to the top and bottom chips with two independent heat sources. In addition, the force is calibrated and controlled by the lever.

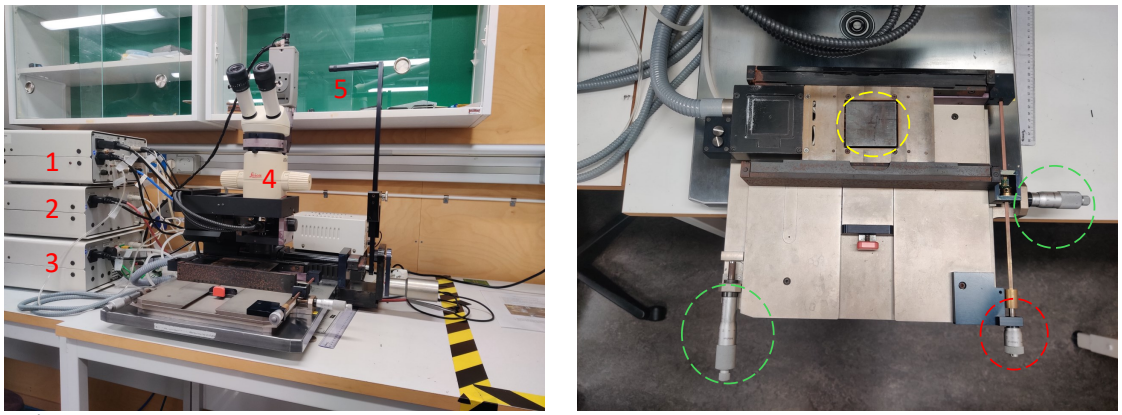


Figure 3.10: a) A photo of the FC bonder where label 1 and 2 are the heat sources for the pick-up tool and the bottom plate, label 3 is the vacuum for the bottom plate, 4 is the microscope for alignment, 5 is the calibrated lever. b) A photo of the stage, the green circles indicate the x-y micro-manipulators, red circle is the vertical control for the focus of the microscope and the yellow circle points to the plate where the bottom chip is held with vacuum.

3.3 Characterization Setup

The characterization of thin films, flip chips, and flux-tunable resonators is performed inside a BlueFors LD250 dilution refrigerator. This section describes the experimental setup, provides an overview of the instruments used, and describes the characterization techniques used to measure the devices.

3.3.1 Thin-film and Flip-chip Characterization

The flip-chip samples are placed on the mixing plate (MXC) inside the refrigerator, which operates at a base temperature of 75 mK, where the superconducting connection of the flip-chip will be characterized. The characterization is performed with a four-wire measurement on the flip-chip devices to measure the critical current (I_c) and the critical temperature (T_c) of the samples. A four-wire measurement is an accurate way to measure the resistance of a device-under-test (DUT) by eliminating the contact resistance. This measurement is performed with an independent current source and a voltmeter, see Fig. 3.11 . A Keithley 2450 SourceMeter is used as the current source to send a bias current across the DUT, while an R&S HMC8012 digital multimeter is used as the voltmeter to measure the voltage drop across the DUT. In contrast, in a two-wire measurement, one cannot eliminate the contact resistance, as the same device is used to send the bias current and measure the voltage.Thus, a four-wire measurement is required for the characterization of a DUT that has a resistance much lower than that of the measurement lines, which is the case for superconducting thin films. However, we also measured the two-wire voltage using the Keithley 2450 SourceMeter as an additional measurement parameter. The current

source has a voltage compliance of 1 V, and each voltage measurement is taken with 4 s of hold time to reduce measurement noise.

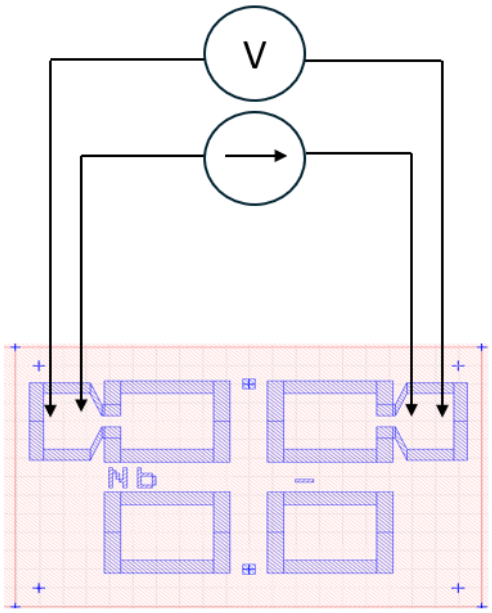


Figure 3.11: A schematic of a 4-wire measurement. An independent current source sends a constant current while monitoring the voltage via a voltmeter.

Fig. 3.12 shows a schematic of the experimental setup. The flip chip (FC) is glued to a Cu sample holder using cryogenic-compatible glue (BF-6). The sample holder consists of four Nb pads, one for each terminal of the four-wire measurement. Each Al pad on the bottom chip is wire bonded to two Nb pads on the sample holder, one for a voltage terminal and one for a current terminal. Each Nb pad is wire-bonded using four Al wires of 25 µm diameter ($I_c \sim 85$ mA) such that the critical current measurements are not limited by the wirebonds. The FC sample holder is then screwed onto the MXC plate. Then a superconducting niobium-titanium (NbTi) wire is screwed with titanium screws to each Nb pad of the sample holder. The other end of the NbTi wires are soldered to the Cu DC pins of a 24-pin micro-D sub-miniature connector at the 4K plate. Thus, all electrical connections below the 4K plate are fully superconducting. The Cu DC lines terminate at the top flange of the refrigerator as a Fischer connector that is connected to a QDevil DC breakout box using a shielded Fischer cable. On the DC breakout box, connections are made to the current source and the voltmeter using banana cables. The MXC plate also has a RuOx temperature sensor to monitor the temperature near the sample and a heater to vary the temperature of the sample.

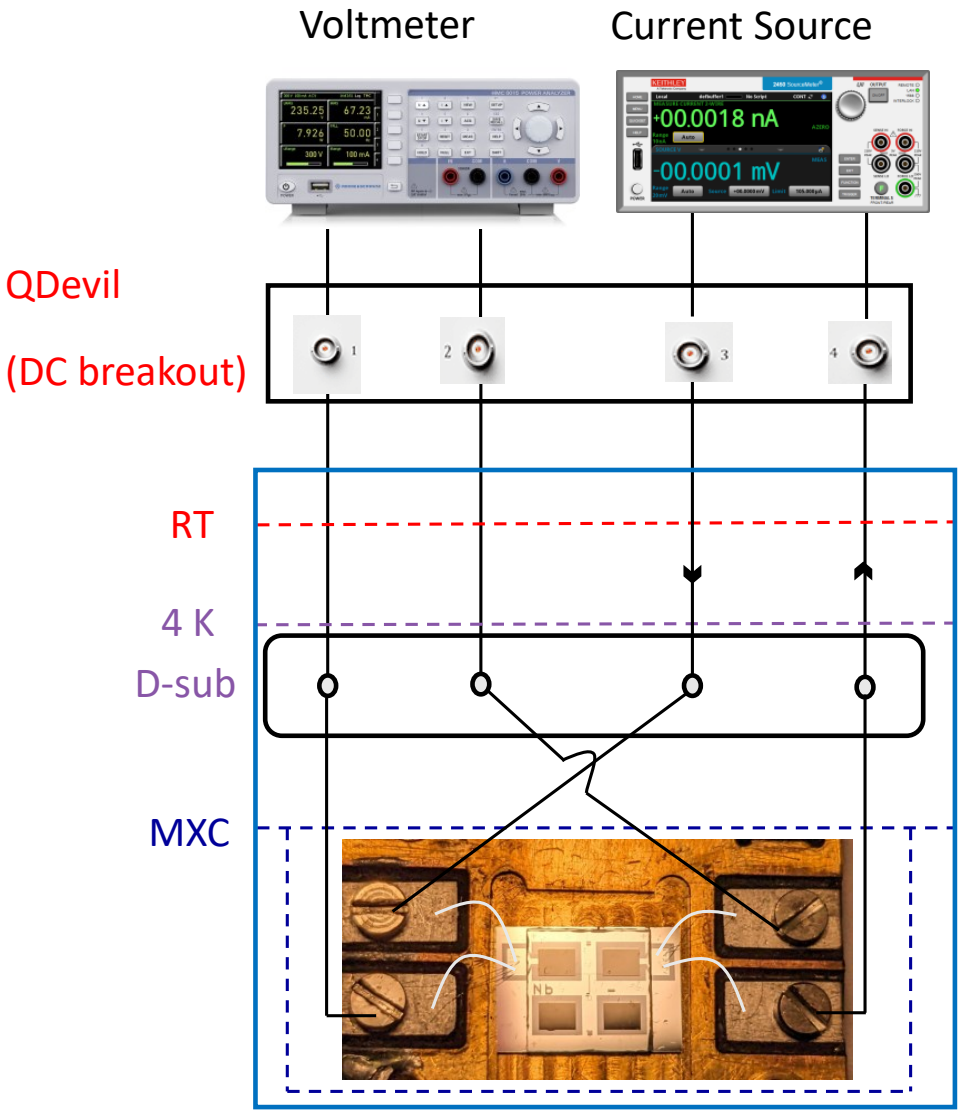


Figure 3.12: A schematic of the experimental setup: blue box represents the dilution refrigerator, voltage is measured across ports 1-2, and bias current is sent through ports 3-4. Connections from DC breakout to the 4K stage are normal conducting, while those below the 4K stage are with NbTi wires. The Nb pads interface the NbTi wires and the wirebonds to the chip.

3.3.2 Flux-tunable resonator measurement setup

The FTRs are fabricated on a 5×7 mm silicon chip. An Aluminum ground plane is deposited in which CPW resonator is patterned via etching process. Then, Josephson junctions of the DC SQUID are patterned using EBL via a lift-off process. The junctions are deposited in a Plassys tool using the shadow evaporation method. After that the chip is assembled using a flip-chip bonder in which the input coil (top chip) is bonded to the bottom chip via In microspheres, see Sec. 3.2.2. Next, the flip-chip is glued to a Cu sample holder and wire-bonded with Al wire-bonds.

Finally, the sample holder is screwed on a U-shaped copper support that is mounted on and thermalized to the MXC plate of the dilution refrigerator.

The characterization of the flux-tunable resonator (FTR) is carried out by measuring the transmission (S_{21}) parameter. Fig. 3.13 shows a schematic and photos of the experimental setup. Two RF ports with SMA connectors on the sample holder are connected to the vector network analyzer (VNA). Two DC ports with insulated aluminum pins that are soldered with twisted NbTi wires are connected to the external bias coil and a Keithley current source. Another two RF ports are connected to the input coil and a Keithley current source. The FTRs are capacitively coupled to a feedline that is wire-bonded to the input and output SMA ports of the sample holder. The sample holder is shielded with multiple magnetic shields at different stages of the refrigerator to minimize flux noise in the FTRs. The input and output SMA ports are connected to the refrigerator's RF lines 1 and 8, respectively, using non-magnetic cryogenic SMA cables. The downline (RF line 1) has attenuators at each stage to reduce thermal noise in the signal. The upline (RF line 8) has two room-temperature low-noise amplifiers (LNA) (G$\sim$26 dB each) connected to the top flange of the refrigerator, a HEMT-LNA (G$\sim$40 dB) connected at the 4K stage, and two circulators on the MXC stage acting as isolators ($\sim$42 dB each). The S_{21} parameter is obtained by frequency sweeping of the drive microwave tone at the input port and measuring at the output port using a VNA.

The FTR modulation is done by driving a current in an input coil that is patterned on a separate chip (see Fig. 3.8) which is flip-chip bonded to the FTR chip. The input coil is used to modulate the resonance frequency of the FTR by threading magnetic flux into the SQUID loop of the FTR (see Sec. 2.3.3). In addition, an external bias coil, made by winding $\sim$1000 turns of a NbTi wire, is glued to the sample holder. This coil is used to bias the FTR frequency at the operating point with the desired modulation slope (see Sec. 2.3.3).

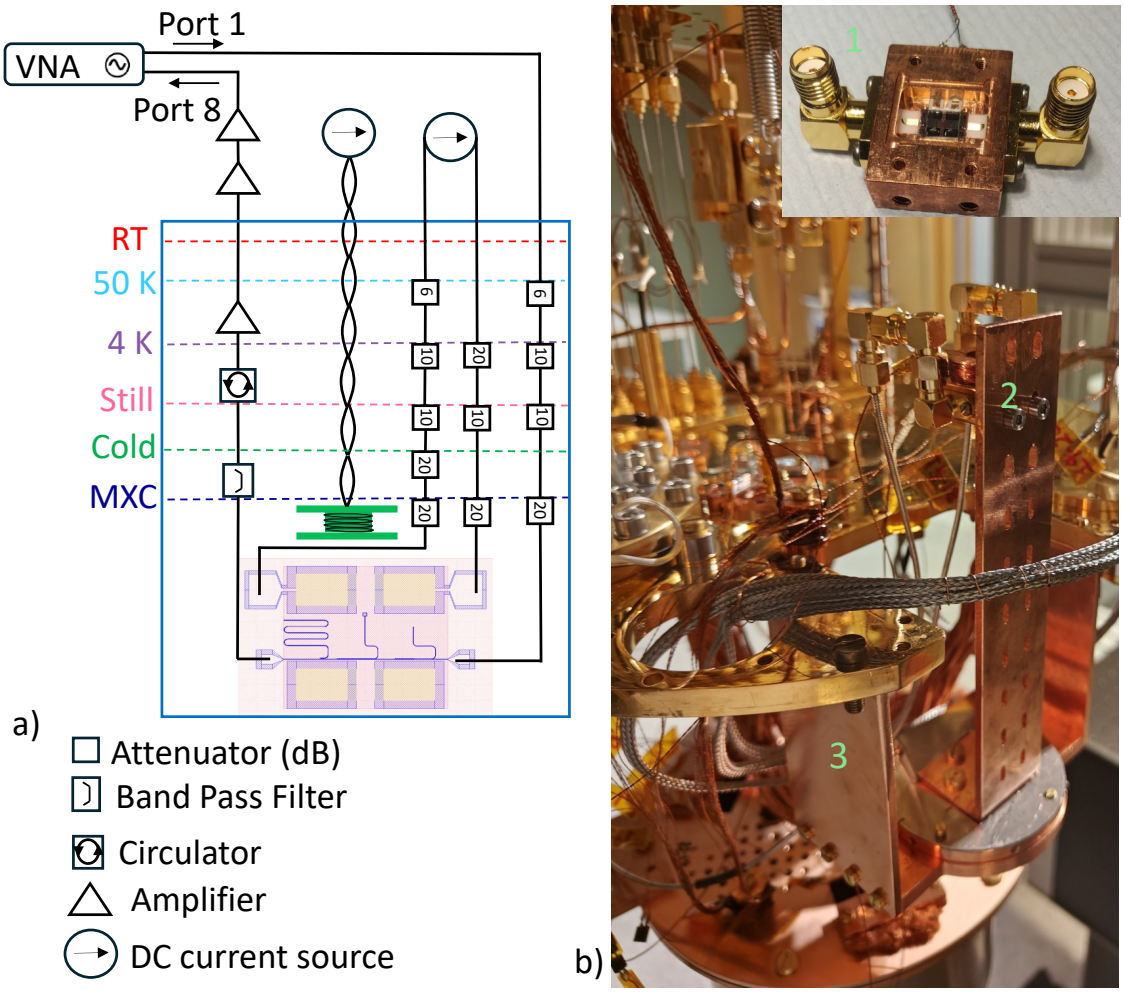


Figure 3.13: a) A schematic of the experimental setup for FTR characterization. The FTR is inductively coupled to an input coil via flip-chip bonding. Port 1 and 8 are the down and up lines, respectively, connected to a VNA. Two independent current sources are used to generate magnetic flux in the input coil and the external bias coil. b) A photo of the experimental setup with the FTR sample holder screwed using Ti screws to an L-shaped Cu holder (label 2) that is mounted on a U-shaped Cu assembly (label 3). An inset photo on the top right shows the FTR sample holder with SMA connectors and a wire-bonded flip chip (label 1).

4

Results

This chapter presents the main results obtained in this thesis. First, results for optimizing the geometry to enhance the flux-transfer efficiency are discussed using both analytical and simulation methods. Second, the results of the design, fabrication, and bonding of the flip-chip devices are shown. Lastly, the superconducting and normal-state properties of the flip-chip devices are characterized.

4.1 Flux Transfer Efficiency

One of the goals of this thesis was to design an input coil to optimize the flux transfer from the PUL to the SQUID loop of the FTR. To this end, we first define the flux-transfer efficiency between the input coil and the SQUID. This efficiency is denoted by η_1 (see Fig. 4.1). These results will be shown for both single-winding and multi-winding coils. In addition, the flux transfer efficiency between the PUL and the input coil is analyzed, which is denoted by η_2. The total efficiency, η, is given by the product of η_1 and η_2. Fig. 4.1 shows a schematic of the flux coupling between the magnetically trapped particle and the flux-tunable resonator.

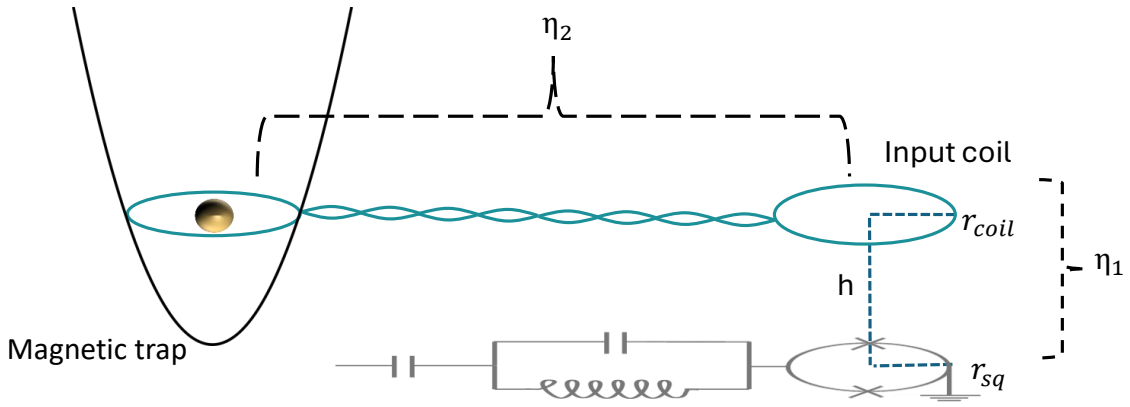


Figure 4.1: Flux coupling schematic: a superconducting particle trapped in the two-chip magnetic trap changes the flux inside the PUL (red coil). This flux is transferred to the input coil via twisted cables (green color). The current in the input coil generates a flux that is captured by the SQUID loop of the FTR. The PUL, twisted cables and the input coil form the closed loop flux transfer circuit.

The flux transfer efficiency η_1 is defined as the ratio of the flux within the SQUID loop and the flux generated by the input coil:

$$\eta_1 = \frac{\Phi_{sq}}{\Phi_{input}} \tag{4.1}$$

where Φ_{sq} is the flux threaded inside the SQUID loop and Φ_{input} is the flux generated by the input coil. The efficiency of η_2 is defined as the ratio between the flux inside the input coil to the flux captured by the PUL.

$$\eta_2 = \frac{\Phi_{input}}{\Phi_{PUL}} \tag{4.2}$$

From the circuit diagram in Fig. 4.1, the flux in the PUL varies due to the motion of the particle, which induces a current (I_p) in the flux transfer circuit. The magnitude of the induced current is given by the total inductance of the flux transfer circuit.

$$\Phi_{PUL} = I_p(L_{input} + L_{tw} + L_{PUL}) \tag{4.3}$$

where L_{input}, L_{tw}, and L_{PUL} are the geometric inductances of the input coil, twisted cables, and the PUL coil, respectively. The flux generated by the input coil is the current induced by the motion of the particle times the inductance of the input coil.

$$\Phi_{input} = I_p L_{input} \tag{4.4}$$

Thus, η_2 can be expressed as:

$$\eta_2 = \frac{L_{input}}{L_{input} + L_{tw} + L_{PUL}} \tag{4.5}$$

From Eq. 4.1 and Eq. 4.5 the total efficiency is given by:

$$\eta = \eta_1 \cdot \eta_2 = \frac{\Phi_{sq}}{\Phi_{input}} \cdot \frac{L_{input}}{L_{input} + L_{tw} + L_{PUL}} \tag{4.6}$$

4.1.1 Single-winding coils

The first result is for η_1 with a parametric sweep of the axial separation, h, between the input coil that carries 100 µA of current and the SQUID loop for different ratios of r_{coil} and r_{sq} (see Fig. 4.1).
Fig. 4.2 shows that if $r_{coil} = r_{sq}$ with $h = 0$ the efficiency is 100%. This is expected since the coils perfectly overlap, and therefore, no flux is lost. However, the efficiency drops drastically with a slight increase in h. Furthermore, for a larger chip separation, it is advantageous to have r_{sq} slightly larger than r_{coil}. Our flip-chips have a separation in the range of 20 µm to 50 µm (Sec. 3.2.2), for which maximum efficiency is obtained if $r_{coil} = r_{sq}$.

The ratio between r_{coil} and r_{sq} can be optimized, provided that h remains constant, which is reasonable since h is set by the force applied with the flip-chip bonder; see Sec. 3.2.2. From the devices assembled by both the flip-chip bonder and the transfer stage, we know that the chip separation ranges from 20 µm to 50 µm, and therefore the plot in Fig. 4.3 is shown for these h values.

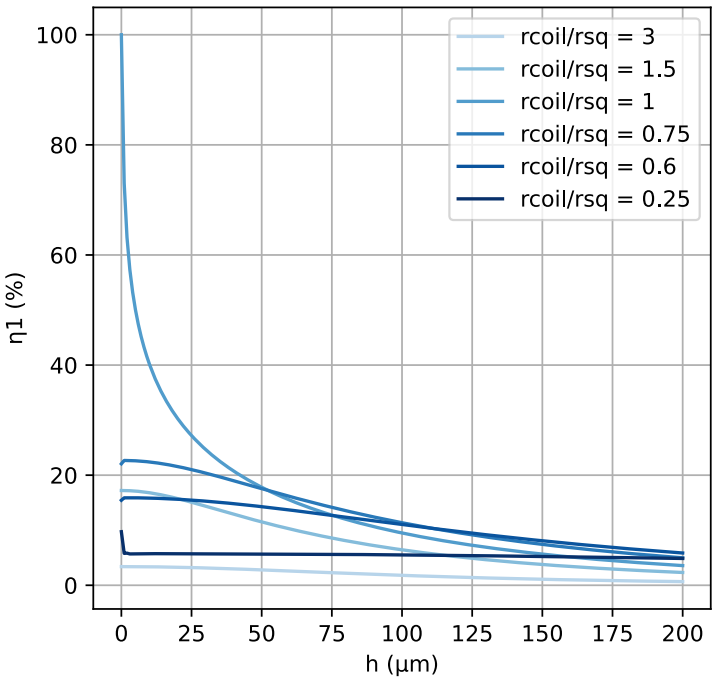


Figure 4.2: Plot for the efficiency η_1 against the chip separation h for different ratio r_{coil}/r_{sq}.

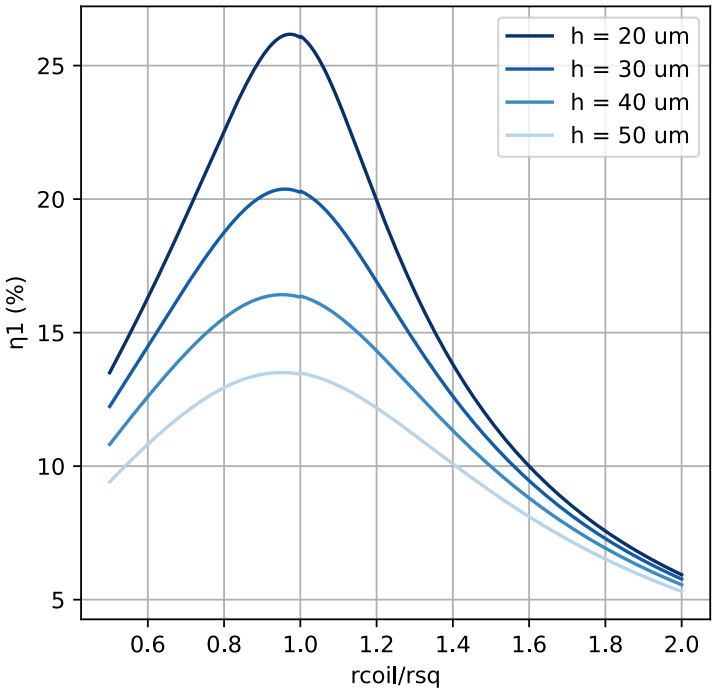


Figure 4.3: Plot for efficiency η_1 against the ratio of r_{coil} to r_{sq} for different chip separations h.

From Fig. 4.3, we deduce that r_{coil} and r_{sq} should be almost equal for chip separations achieved in this thesis. Also, as expected, the smaller the chip separation, the higher

the efficiency, the highest efficiency achieved is $\eta_1 \approx 26\%$ for $h = 20\,\mu m$.

The analytical results were then corroborated with numerical simulations performed using COMSOL Multiphysics. The 3D model consists of an input coil which is a wire of thickness 1 µm and a spherical simulation region of 300 µm radius with air as a medium. The input coil is defined with a very high conductivity σ, which effectively renders it lossless, similar to a superconductor. A circular area is defined in the xy plane with radius r_{sq} and at an axial separation h from the input coil. This geometry is used to calculate the flux captured by the SQUID loop. Fig. 4.4 shows the model used in the COMSOL simulation along with the simulation region. The simulation configuration is as follows:

- The input coil conductivity $\sigma = 10^{10}\,S/m$ to behave as a perfect conductor.
- The relative permittivity of the input coil $\epsilon_r = 1$.
- The relative permeability of the input coil $\mu_r = 10^{-4}$ to behave as a diamagnet.
- Superconductivity, Meissner effect, and Josephson junctions are neglected.
- The input coil is a circle in geometry with a 1 µm width in the x-direction and zero dimensions in the y, z directions respectively.
- A bias current of 100 µA was assigned to the input coil.

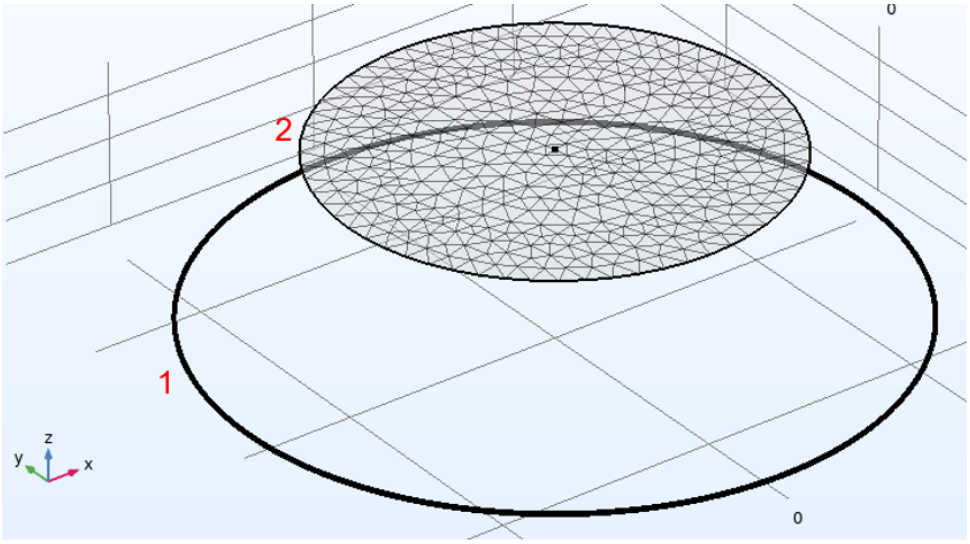


Figure 4.4: COMSOL model of (1) a 1 µm wide input coil and (2) a SQUID loop shown as a circular geometry. The input coil carries a current that generates a magnetic field. This field passes through the SQUID loop. The system is enclosed in a sphere (not shown for clarity) with air as the medium, which defines the simulation region.

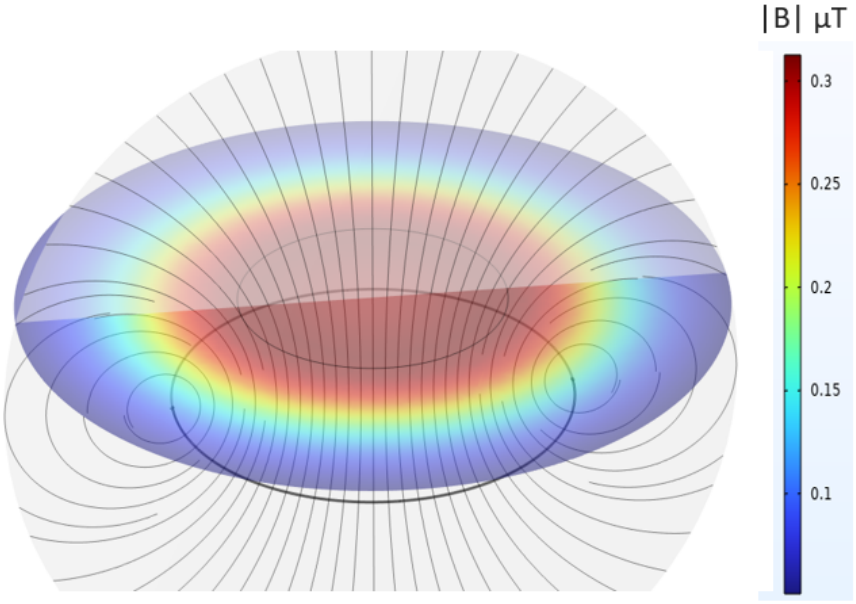


Figure 4.5: A color plot of the magnetic flux density.

Fig. 4.5 shows the color plot of magnetic field intensity. The magnetic field passes through the SQUID geometry, which contributes to the flux inside the SQUID. The highest magnetic flux density is in the center, and it decreases along the radial direction.

The current in the input coil generates a magnetic field that can be calculated from the Biot-Savart law, see Sec. 2.2.1. The relation between the magnetic field and the magnetic vector potential $\mathbf{A}$ is given by $\mathbf{B} = \nabla \times \mathbf{A}$. This magnetic vector potential is used to compute the flux inside the input coil as well as the SQUID loop by taking the line integral of $\mathbf{A}$ around the desired area by applying Stoke's Theorem:

$$\Phi = \iint_S \mathbf{B} \cdot \mathbf{dS} = \iint_S \nabla \times \mathbf{A} \cdot \mathbf{dS} = \oint \mathbf{A}.dl \tag{4.7}$$

In order to obtain the flux results from the COMSOL simulation, we do a parametric sweep on various height separations between the input coil and the SQUID geometry. The current I and the ratio r_{coil}/r_{sq} in the simulation model are the same as in the analytical model. The results obtained from the analytical and simulation models are then plotted together for comparison; see Fig. 4.6.

Fig. 4.6 shows analytical results to be in good agreement with the simulation results for all chip separations. This implies that our analytical model is reliable for estimating flux efficiencies for a given geometry.

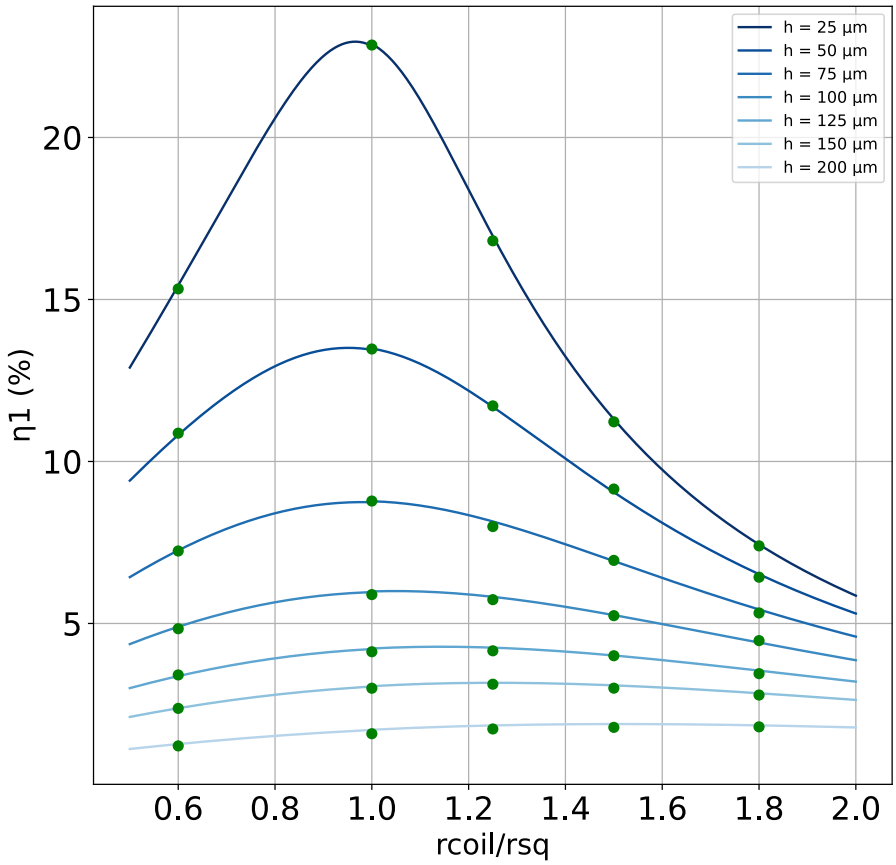


Figure 4.6: flux transfer efficiency η_1 between the SQUID loop and the input coil as a function of the ratio r_{coil}/r_{sq}. The curves are the analytical solutions, while the dots are the COMSOL results obtained for different axial separations h and a bias current of 100 µA.

4.1.2 Multi-winding coils

To maximize total efficiency η, we need to maximize both efficiencies η_1 and η_2, respectively. From Eq. 4.5, the input coil inductance L_{input} should be maximized. This can be achieved with a multi-winding input coil since the inductance increases with the number of turns.

The input coil is a spiral with an inner diameter d of 50 µm, 3 µm width w and 5 µm gap between turns g, see Fig. 4.7. The radius of the SQUID (r_{sq}) is 100 µm. The chip separation is taken as 20 µm and 50 µm based on the minimum and maximum achievable flip-chip separation, respectively. Finally, L_{tw} & L_{PUL} are taken as 12 nH and 0.72 nH respectively. These values are obtained for a levitation experiment that was performed in our lab [64].

The inductance of the input coil L_{input} is estimated as [65]:

$$L_{input} = \mu_0 d[ln(\frac{8d}{w}) - 2] \tag{4.8}$$

where d and $2w$ are the diameter and width of the input coil, respectively. For each

turn a new diameter d is computed to calculate the respective inductance, then the sum of these inductances is the total inductance of the multi-winding coil.

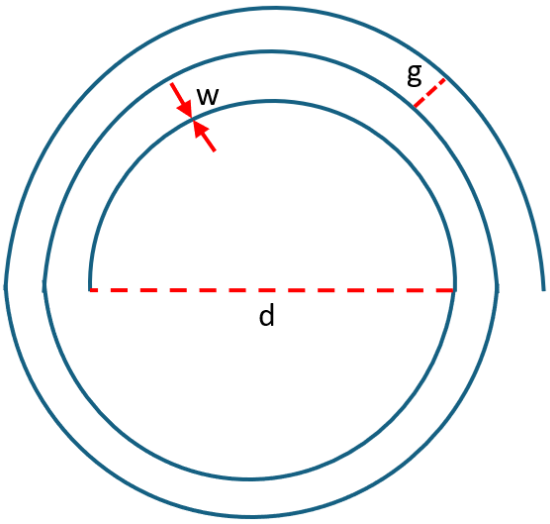


Figure 4.7: Spiral multi-winding coil showing the inner diameter d, width w and gap g between the turns.

Fig. 4.8a shows that we can achieve a total efficiency of 12% for a 100 µm SQUID loop with a chip separation of 20 µm by designing a multi-winding coil with approximately 20 turns ($N = 20$). This increase in efficiency is one order of magnitude compared to the single-turn coil ($N = 1$), where the efficiency is ≈ 1 %.

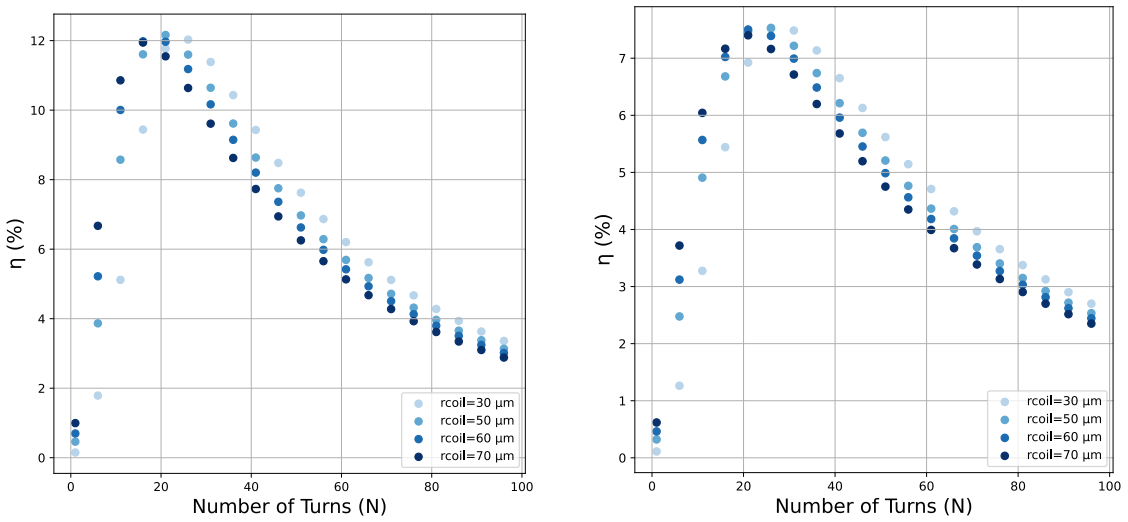
Fig. 4.8b shows that we can achieve a total efficiency of 7.5% with a chip separation of 50 µm by designing a multi-winding coil with approximately 20 turns ($N = 20$). This increase in efficiency is also remarkable compared to a single-winding coil ($N = 1$) that has 1 % efficiency.

4.2 Flip-chip Devices

This section describes the results obtained for the flip-chip devices. Firstly, the design and fabrication results are presented. Secondly, the height and tilt results of the flip-chip assembly are presented using both the transfer stage and the flip-chip bonder for comparison. Lastly, the superconducting characterization of the UBM thin films, as well as that of the flip chips, is shown in which the following parameters are measured:transition temperature T_c, the critical current I_c, I_c vs T.

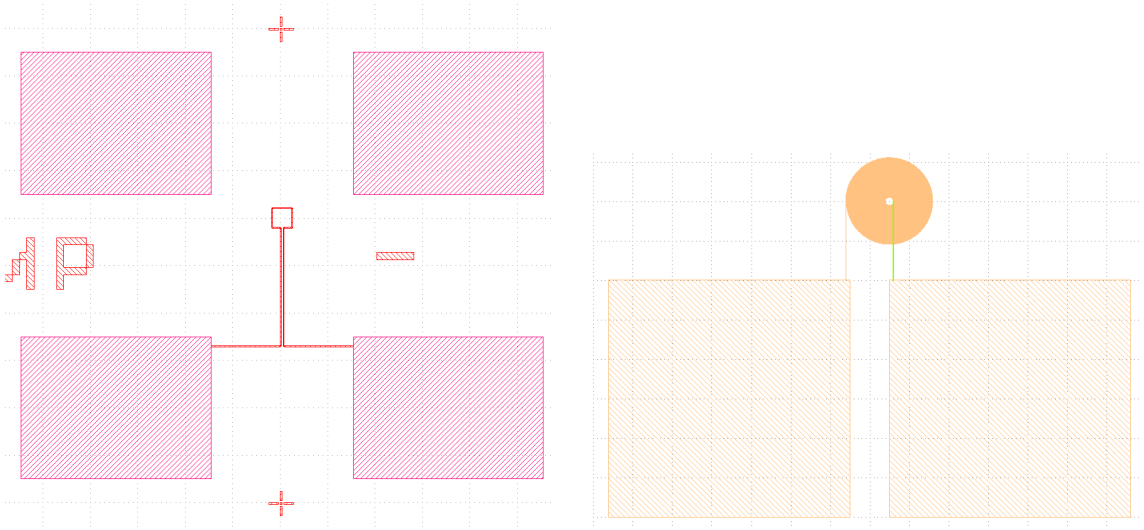
4.2.1 Design & Fabrication

The design of the top chip consists of a bottom pad and an input coil patterned on the UBM layer. The input coil can be single-winding or multi-winding. The designs for single-winding and multi-winding coils are shown in Fig. 4.9a and Fig. 4.9b, respectively.



(a) **(b)**

Figure 4.8: Total flux-transfer efficiency as a function of the number of turns in the multi-winding input coil plotted for different coil radii. a) shows the scenario for a chip separation of 20 µm, and b) shows the scenario for a chip separation of 50 µm.



(a) **(b)**

Figure 4.9: Layout of a) a single-winding coil of width 10 µm and diameter 100 µm, and b) a multi-winding coil with 40 turns with a width of 5 µm, a gap of 5 µm and inner diameter of 50 µm.

4.2.1.1 Etching fabrication results

The fabrication results for the etching process described in Sec. 3.1.1 are shown and discussed below.

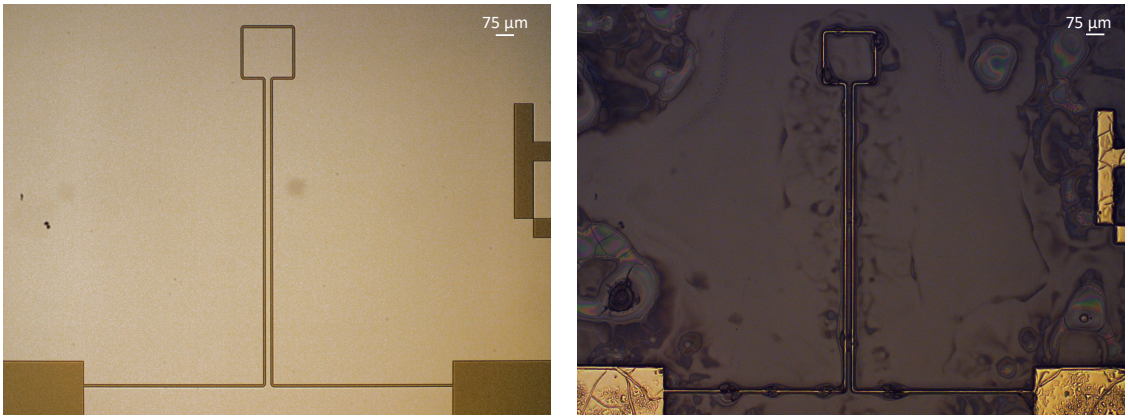


Figure 4.10: Optical images of a) a patterned input coil before etching, and b) after XeF_2 etching with marks around the input coil region where the resist deteriorated, possibly due to unintended reaction or partial etching by XeF_2.

This process was performed on several devices. However, the process failed because the resist did not survive during dry etching, probably due to chemical interaction or etching by XeF_2. As a result, a new process had to be developed using lift-off. It is worth mentioning that a dry etching process using NF_3 was also developed in parallel, which gave good results but is not part of this thesis.

4.2.1.2 Lift-off fabrication results

The fabrication results of the input coil and the UBM using the liftoff process (Sec. 3.1.2.2) are shown below in Fig. 4.11:

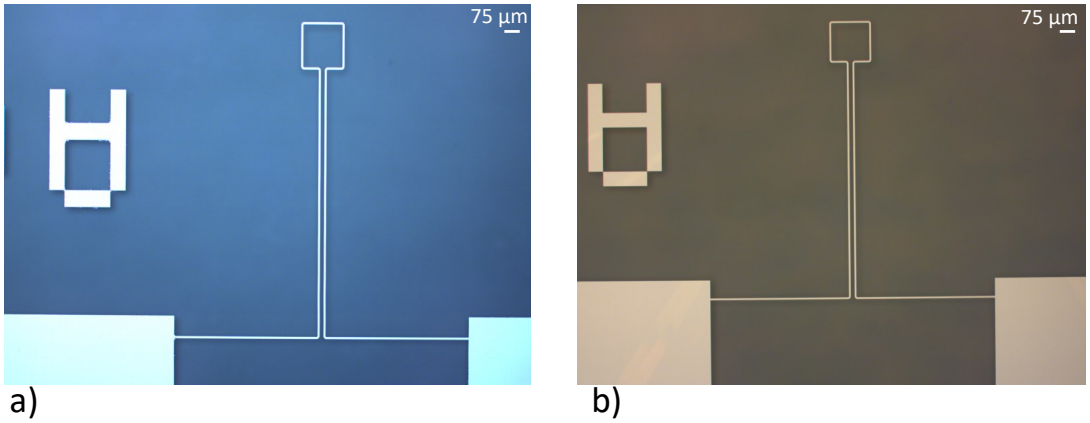


Figure 4.11: Optical images of a) a NbN /Au input coil made of 50 nm NbN and 5 nm Au on top of it for passivation, and b) a 50 nm NbN input coil.

As shown in Fig. 4.11, this process gave much better results compared to the etching process and a higher yield of working devices.

4.2.1.3 Multiwinding fabrication results

The fabrication results for the multi-winding input coil are shown in Fig. 4.12 and Fig. 4.13. The multi-winding fabrication was successful in which the three fabrication layers are well-defined. The NbN spiral coil is patterned, then, SiO_2 bridge is deposited to prevent any shorts. Finally, a NbN crossover is deposited to create a galvanic contact between the pad and the coil.

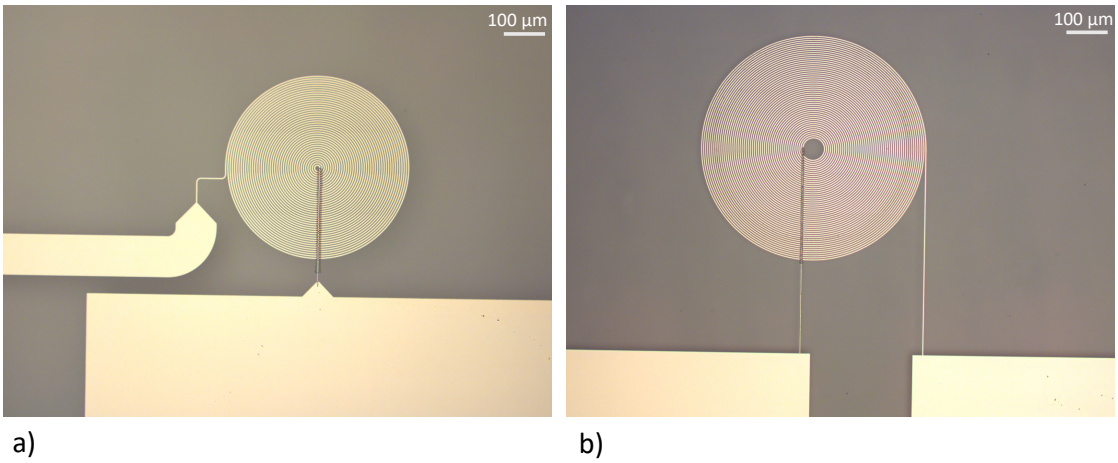


Figure 4.12: Optical images of multi-winding coils with $NbN/SiO_2/NbN$ multilayered stack with a) 38 number of turns and 50 µm inner diameter, b) 40 number of turns and 100 µm inner diameter.

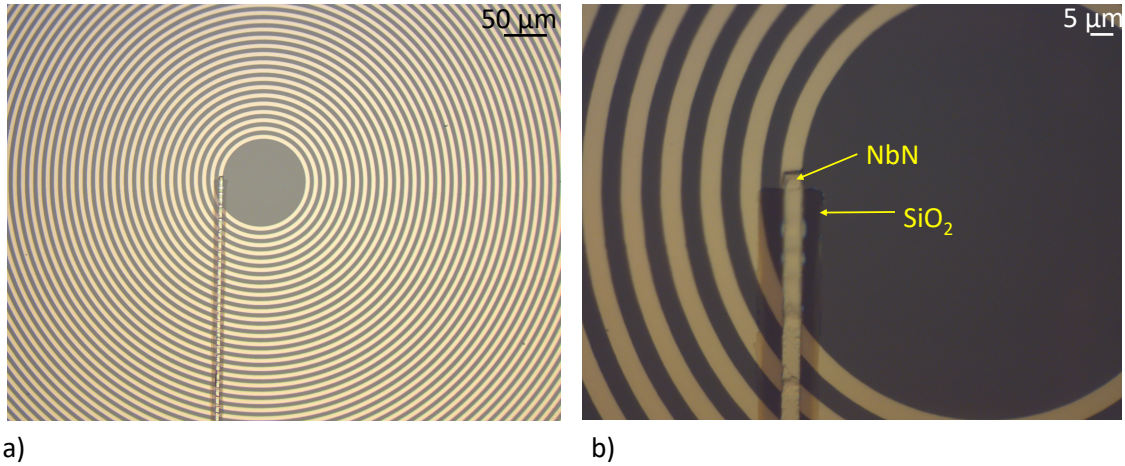


Figure 4.13: Optical images a) the separation between the turns of the coil which indicates successful lift-off, b) shows the 75 nm SiO_2 bridge and 90 nm NbN crossover that makes the galvanic contact to the spiral coil.

4.2.1.4 Surface Profilometry

Profilometry is a thin film characterization method that extracts the surface profile, which can be used to determine the surface roughness and film thickness. The Tencor AS500 surface profiler, which has a tolerance of ±2 nm, was used to determine the film thickness of the NbN UBM to verify the sputtering rate. The thickness of the NbN film that was characterized using the profiler showed a thickness of 53.4 nm, which was in agreement with the calibrated deposition rate of the sputtering tool. Fig. 4.14 shows the profilometry performed for a NbN/Au input coil chip.

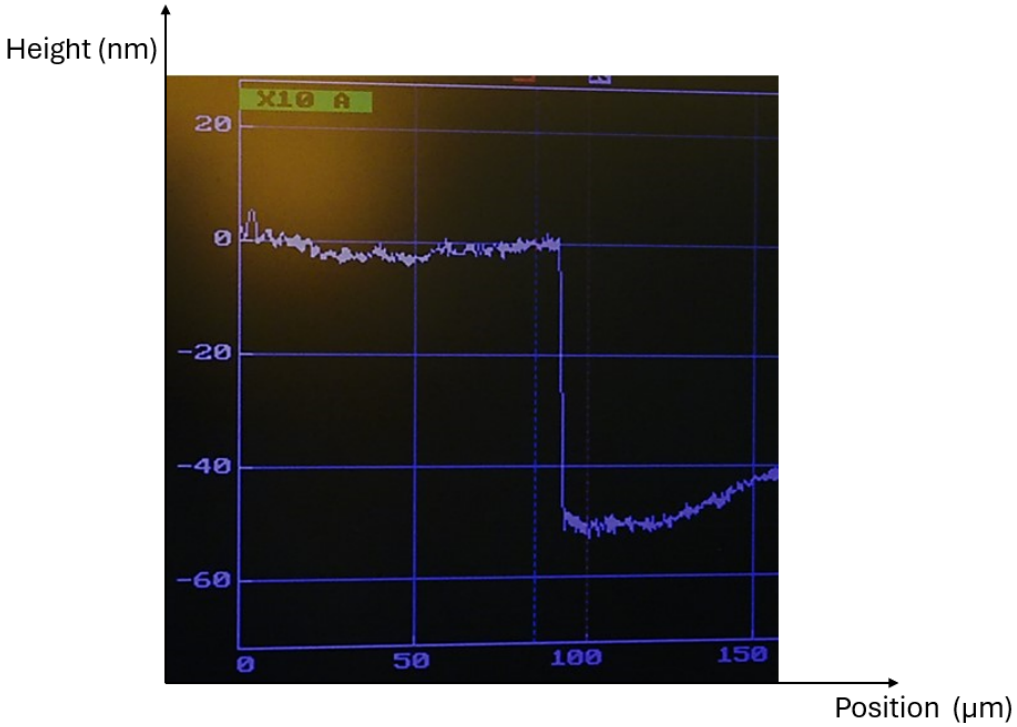


Figure 4.14: The figure shows the film thickness of the NbN/Au film, which is expected to be 55 nm. The measured film thickness is 53.4 nm while the surface profiler has a tolerance of ±2 nm.

4.2.2 Flip-chip Assembly

The flip-chip assembly was performed using a transfer stage and a manual flip-chip bonder (see Sec. 3.2.1 and Sec. 3.2.2). In this section, the alignment, chip separation, and tilt are compared.
The misalignments obtained from the transfer stage and the flip-chip bonder are very close to each other. The alignment error in the transfer stage is ± 5 µm while the alignment error in the flip-chip bonder is ± 3 µm. The alignments achieved with both methods are shown in Fig. 4.15.
The chip separation (h) was measured using a height gauge. In this measurement, the four corners and the center of the top chip are measured with respect to the top surface of the bottom chip. Then, the thickness of the top chip, which is 450 µm,

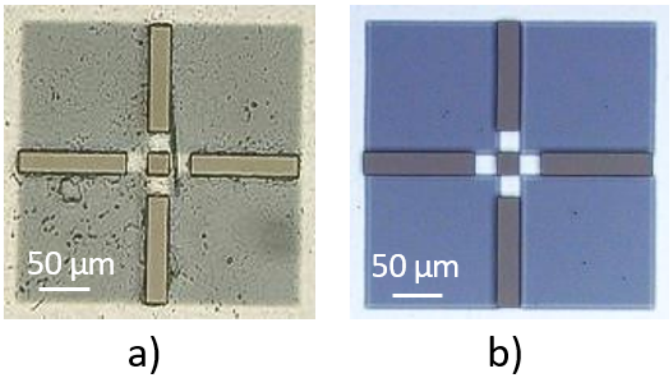


Figure 4.15: Optical images of alignment achieved with a) the transfer stage and b) the flip-chip bonder. The alignment of the top chip is a cross that is aligned between the four boxes on the bottom chip.

is deducted from the measured height. Using the chip separations obtained, the tilt (θ) is calculated between two opposite points. Fig. 4.16 shows the difference in separation before and after FC bonding. Tab. 4.1 shows the range of h and θ obtained for both the transfer stage and the flip-chip bonder.

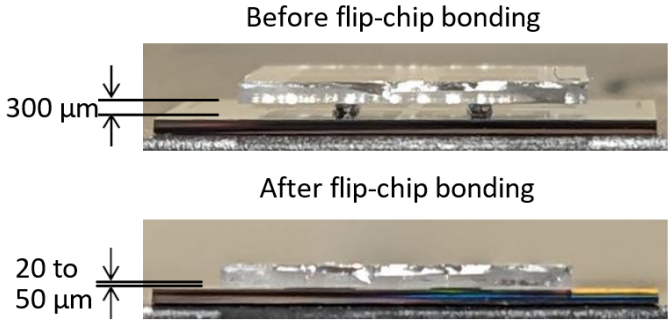


Figure 4.16: A side-image of a flip-chip showing the separation before and after flip-chip bonding.

Property	Transfer stage	FC bonder (50 N)	FC bonder (65 N)
h (µm)	40-50	35	20
θ (mrad)	2 – 2.5	2 – 3	2 – 3

Table 4.1: Comparison of flip-chip bonding performance using the transfer stage versus the flip-chip bonder

4.2.3 Superconducting flip-chip characterization

The characterization of the flip chips was performed using a 4-wire measurement as explained in Sec. 3.3.1. This section summarizes the main results for measuring the

following parameters for the UBM: T_c, I_c, I_c vs T. First, the characterization results of the UBM thin film are explained. Second, the characterization results of the FCs are analyzed and compared with those of the UBM thin films with and without the Au passivation layer.
The measurements to determine each superconducting parameter of the sample (thin film and flip chip) are performed as follows:

1. T_c measurement: the T_c of the sample is measured by first increasing the MXC plate temperature to 14 K using the MXC heater. At this point, the four-wire resistance measurement is started. Then, the fridge is cooled down to 5 K while continuously monitoring the four-wire resistance. During the temperature sweep, a sharp drop in the four-wire resistance is observed at a certain temperature.
2. I_c measurement: the I_c of the sample is measured by increasing the current in steps of 0.5 mA. The step size is reduced to 0.1 mA when approaching the expected I_c. The measurement is continued until the four-wire voltage increases sharply and exceeds 0.1 V, which defines I_c of the sample at the measured temperature. A corresponding rise in the MXC temperature accompanies the sharp increase in voltage. This is another indicator that the sample has transitioned to the normal-conducting state, which causes Joule heating.
3. I_c versus T measurement: in this measurement, the I_c of the sample is measured at each temperature starting from the base temperature of the MXC. After each I_c measurement, the MXC temperature is increased to a certain temperature using the MXC heater, and a new I_c measurement is performed.

4.2.3.1 UBM thin film characterization

Fig. 4.17 a) shows the resistance (R) of the thin films as a function of temperature (T). The UBM thin film was characterized on separate chips patterned with a coil that is 4720 µm long and 10 µm wide with a film thickness of 50 nm (See Fig. 4.11). The UBM thin film is then characterized to obtain T_c, and I_c as a function of T. T_c measurement is done by monitoring the resistance R using a 4-wire measurement in which the bias current (I_b) is fixed to 10 µA. The non-passivated UBM NbN and Nb has T_c of 10.4 K and 8 K respectively, see Fig. 4.17. The T_c of NbN and Nb agree well with the literature [66, 67], see Tab. 4.2. The passivated UBM contains 5 nm Au on top of the UBM in which the T_c of NbN/Au and Nb/Au is 9.8 K and 7.7 K respectively. The passivated UBMs exhibit lower T_c than their non-passivated counterparts. This is due to the proximity effect, which is a result of the Au capping layer [68, 69, 70].
The characterization of I_c vs T was performed by increasing the current in intervals of 0.1 µA at a certain temperature. The current at which the measured voltage increases sharply by a factor of 10 is defined as I_c. The obtained T_c is in agreement with T_c obtained from the resistance transition in Fig. 4.17 a). The results are shown in Fig. 4.17 b), which is fitted to the two-fluid model [45] given by Eq. 4.9:

$$I_c = I_{c0}\left(1 - t^4\right). \tag{4.9}$$

where $t = T/T_c$

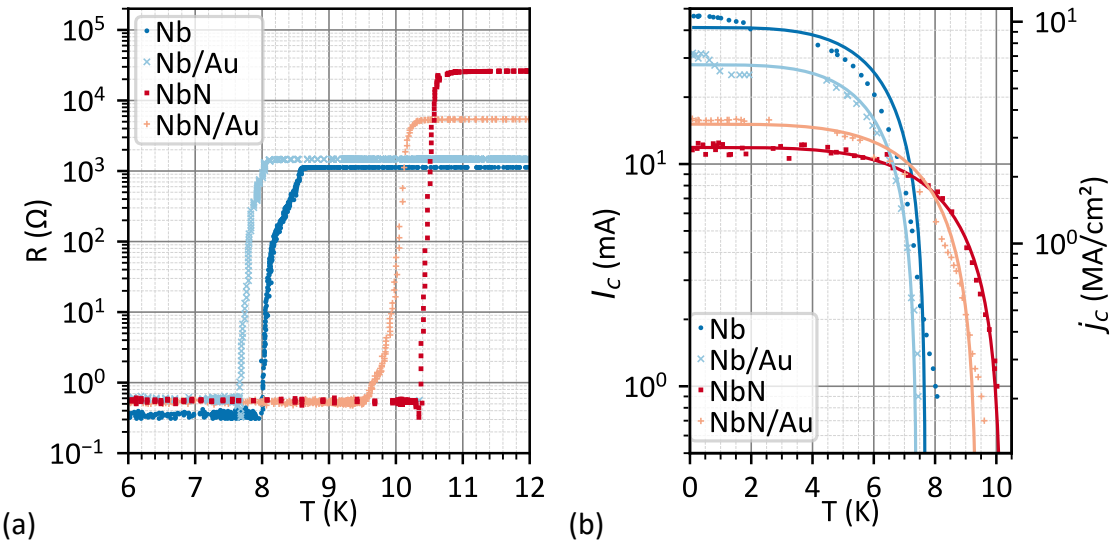


Figure 4.17: Characterization of superconducting thin films. a) Resistance as a function of temperature at 10 µA bias current. The resistance offset below T_c is due to the voltage systematic error of the voltmeter, which is 7 µV with 10 µA bias current which yeilds a resistance offset of 0.7 Ω. (b) Critical current and critical current density as a function of temperature. The solid line is a fit according to Eq. 4.9.

The critical current density j_c of the thin films is obtained at the base temperature of the dilution refrigerator ($\approx$ 100 mK). The j_c for Nb and NbN is 9.26 MA cm^{-2} and 2.5 MA cm^{-2} respectively. On the other hand, j_c for Nb/Au and NbN/Au is 6.3 MA cm^{-2} and 3.2 MA cm^{-2}, respectively. For comparison with the literature, see Tab. 4.2 [1]:

Thin film material [thickness]	j_c (MA/cm^2)		T_c (K)	
	Exp.	Lit.	Exp.	Lit.
Nb[50 nm]	9.3	4 [71]	8.0	8.1 [71]
Nb[50 nm] / Au[5 nm]	6.3	-	7.7	7.3 [70]
NbN[50 nm]	2.5	2.5 [69]	10.4	10.6 [66]
NbN[50 nm] / Au[5 nm]	3.2	-	9.9	10.2 [72]

Table 4.2: Superconducting properties of the UBM layers patterned on a sapphire substrate. The literature values are taken from works that use similar deposition techniques and film thicknesses [1].

4.2.3.2 Flip chip Characterization

The flip-chip devices were characterized for the four combinations of UBM materials, see Tab. 4.2. The flip chips using NbN, NbN/Au, and Nb/Au as UBM exhibit full

superconductivity at the base temperature (millikelvin). However, the Nb-based flip chip showed resistance at the base temperature due to the presence of a native oxide layer on top of Nb. As a result, we show the results of the other three UBM devices. Similar to thin film UBM characterization, a 4-wire measurement was performed in which the bias current is 100 µA. The bias current is higher than the one used for UBM characterization in order to resolve the superconducting transition of Al. In addition, a critical current measurement was performed for different temperatures. Fig. 4.18 shows R vs T and I_c vs T plots [1].

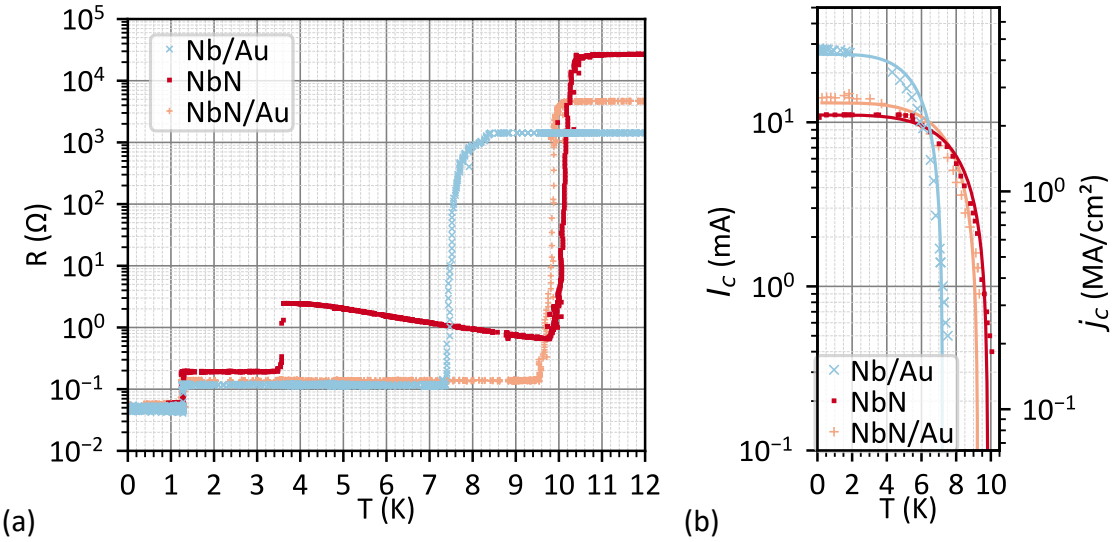


Figure 4.18: Characterization of superconducting flip-chips. a) Resistance vs temperature at 100 µA bias current. b) Critical current and critical current density as a function of temperature.

Fig. 4.18 a) shows the resistance dependence on temperature of the superconducting flip-chip devices. The sharp transitions in resistance are due to the phase transition of a certain material in the flip-chip stack. The three UBMs exhibit very close transition temperatures T_c to the ones obtained from the UBM thin-film characterization. The flip-chip devices have slightly smaller T_c, which is because of the proximity effect from the Al layer below the UBM [73]. For all the flip-chip devices, the final transition is observed at 1.25 K, which corresponds to the transition temperature of Al. The transition of In is not observed because the estimated room temperature resistance is in the order of nΩ. For NbN flip-chip device, there is an intermediate transition between the NbN and Al. This transition occurs at 3.5 K, which is at the critical temperature of In. This is observed due to a native oxide layer formed on top of the NbN due to air exposure, which forms NbN/NbO_x/In interface. Above the T_c of In, this interface forms a superconductor-insulator-normal conductor interface that is resistive. However, below the T_c of In, this interface forms a superconductor-insulator-superconductor Josephson junction [74] where the current tunnels through the oxide barrier, and thus a drop in resistance is observed.

Fig. 4.18 b) shows I_c vs T plot for the flip chip devices. The measurement was done using the same procedure as that for the thin-film UBM characterization. The j_c is

defined by the critical feature size in the UBM test structure. The I_c as a function of temperature follows the two-fluid model equation (see Eq. 4.9). The I_c values obtained for the flip-chip devices matches the values of I_c values from the UBM thin film characterization which implies that the UBM structure is the bottleneck of the flip-chip devices that dictates the I_c of the flip-chip and not the In interconnect.

4.3 Flip-chip based FTR Modulation

In this section, we show a proof-of-principle for flip-chip-based modulation of an FTR where the input coil on the top chip threads a magnetic flux inside the SQUID loop of the FTR. This flux biasing will cause a shift in the resonance frequency and thereby modulate the FTR (see Sec. 2.3.3).

4.3.1 Frequency Modulation via external bias coil

The modulation of the FTR can be driven by an external bias coil (see Fig. 3.13 (a)). The DC current flowing through the external bias coil generates a flux that threads the SQUID, thus modulating the FTR.

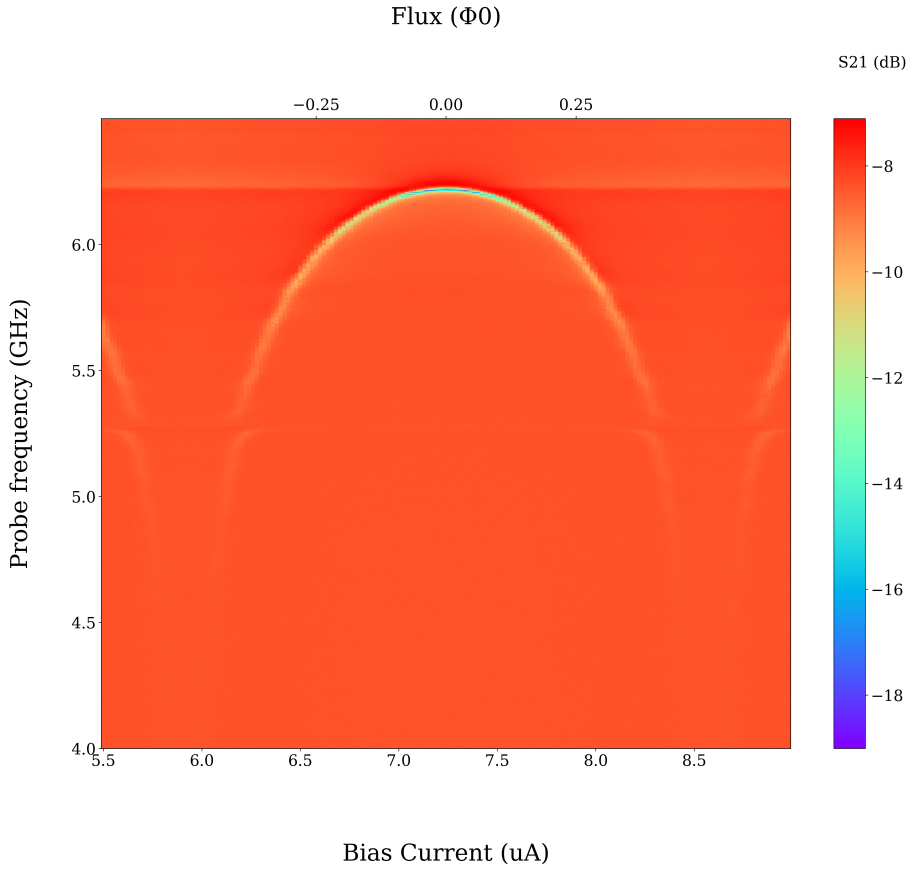


Figure 4.19: Modulation of the FTR via applied flux from the external bias coil.

Fig. 4.19 is a color plot that shows the S_{21} amplitude as a function of probe frequency applied to the feedline via the VNA and the bias current I applied to the external

coil. The plot shows a deep dip of −14 dB at a resonance frequency of 6.22 GHz. The current needed for a full modulation is ≈ 3 µA.

4.3.2 Frequency Modulation via flip chip coil

An integrated approach to modulate the FTR is via the patterned input coil in a flip-chip configuration. Similar to the modulation of the external bias coil, a DC current flows in the input coil to thread flux inside the SQUID.

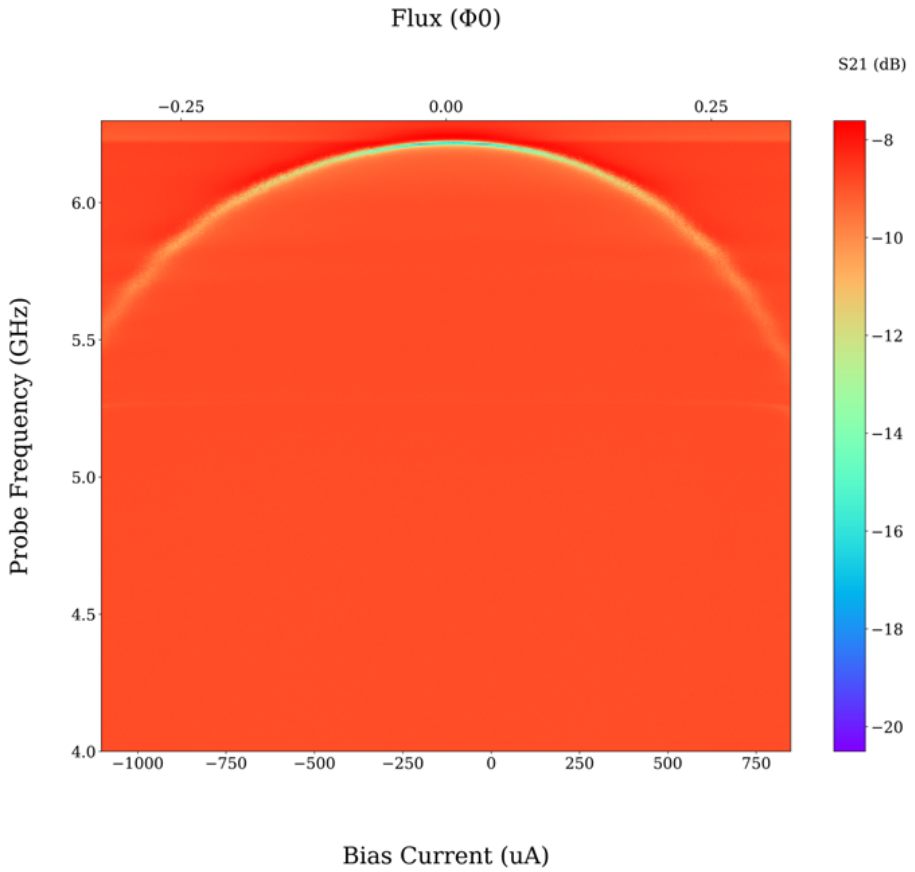


Figure 4.20: Modulation of the FTR via applied flux from the input coil.

Fig. 4.20 shows that the FTR is modulated via the input coil and exhibits a resonance frequency of 6.22 GHz. The input coil is connected to the RF lines to attenuate the thermal noise at every stage of the fridge to that of the stage temperature. The current needed for Φ_0 is ≈ 1.6 mA. Analytically, we estimate that Φ_0 requires tens of µA. We attribute this discrepancy to the attenuation used in the RF lines connected to the input coil (See Fig. 3.13).

5

Conclusion & Outlook

In this thesis, I have successfully developed an analytical model to estimate the flux transfer between the pickup loop of the magnetic trap and the SQUID loop of the flux-tunable resonator. The flux transfer is based on the use of single-winding as well as multi-winding input coils. Simulations were performed to verify the analytical results using COMSOL Multiphysics. The analytical and simulation results were in very good agreement. Although the flux transfer efficiency for the single-winding coil is 1%, the multi-winding approach increases the efficiency to 12%. Then, a reliable fabrication recipe for flux transformers was developed that obtained a high yield of working devices. A superconducting flip-chip interconnect was demonstrated and characterized using Nb and NbN under-bump metallization with and without Au passivation. These devices can transport tens of mA of supercurrent, which is sufficient to modulate the flux-tunable resonators. The critical current of these superconducting flip-chips has been limited by the under-bump metallization layer, which implies that the In microspheres used as interconnects are not the bottleneck of the critical current. This was verified by independently characterizing the under-bump thin film, and the critical current matches the one obtained from the flip-chips. Finally, the measured transition temperature (T_c) and the critical current (I_c) for the thin films agree with the values reported in the literature, which indicate the high quality of the thin films.

The outlook will mainly be to develop a more robust fabrication recipe for multi-winding coils. These multi-winding coils can be implemented on both sides of the experiment: the magnetic trap and the input coil of the flux transformer. In the magnetic trap, the multi-winding coils will provide a higher magnetic field gradient, which would increase the lift force on the particle if the chip trap is implemented in a flip-chip configuration. For the flux transformer, the multi-winding coil would increase the flux transfer efficiency by one order of magnitude. In addition, AlN can be a better insulation layer in the multilayered stack than SiO_2 used in this work. AlN has good wettability with NbN [75, 76]. These next steps would give a forward leap for the experiment that would allow it to achieve coupling between the particle and the flux-tunable resonator with an unprecedented record for the coupling strength.

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A

Appendix 1

A.1 SPR 220 Lift-off Process

The process development for optically patterning bottom pads and input coil with LOR-3A & SPR 220 bilayer resist stack.

1. Spin coating & Pre-bake
   - Spin coat LOR-3A 2000rpm, 1000/s2, 1 min
   - Bake hotplate 5min, 180 °C
   - cool cold plate 20s
   - Spin coat SPR 220 3.0 3000rpm, 1500/s2, 1 min
   - Bake hotplate 90s, 115 °C
   - cool cold plate 20s
2. Lithography & Development
   - Expose MLA Dose = 220, defocus = +2
   - Development 1 min MF-24A
   - Flood Exposure using UV light
   - Ashing 30s, 40W, #422
3. NbN deposition DCA metal
   - Ar ion milling 50s
   - Deposit 50 nm of NbN
4. Lift-off Procedure
   - Warm 1165 on a hotplate 80 °C
   - Immerse the wafer for 8h
   - Warm 1165 on a hotplate 80 °C
   - Fresh 1165 and ultrasonic (40, sweep mode, 35 KHz)
   - Fresh acetone and ultrasonic (40, sweep mode, 35 KHz)
   - Fresh IPA and ultrasonic (40, sweep mode, 35 KHz)
   - N_2 blow dry

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