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Impedance Modelling of DC-DC Converters

Master's Thesis in Electric Power Engineering

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Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2021

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Abstract

The DC-DC converters, known as the dc voltage regulator, are widely applied to several power supply applications. Among these applications, in this thesis work, the research is conducted on the dc part of a typical telecom power system at Ericsson, where the circuit mainly includes the front-end converters and PWM dc-dc converters. In a telecom system, especially in the 5G telecom system with cutting-edge technology, some critical performances, known as the high stability and anti-interference capability of the power supply, are required to guarantee a reliable telecom signal transmission. Moreover, it is known that the input and output impedance of these converters are tied up with the stability and anti-interference capability of the system. To meet these requirements, the dynamic research, mainly referring to the impedance modelling analysis, needs to be conducted on these converters.

According to the control schemes of converters, the thesis work is mainly distributed into two parts: the LLC resonant converter with voltage mode (VM) control and PWM dc-dc converters with peak current mode (PCM) control. For the LLC resonant converter, the extended describing function method is mainly employed to derive and establish the small-signal model. Moreover, the application of the VM control simplifies the closed-loop small-signal model establishment. For the PWM dc-dc converter, the circuiting averaging is an efficiency method to derive the small-signal model. The PCM control in this converter, as the popular control scheme, consists of two loops: inner current loop and outer voltage loop.

In general, the research process of these two converters is formed almost in the same way. To be specific, the physical meanings behind the small-signal impedance models are illustrated, and used to explain the relationship between the Bode plots and equivalent circuits. Furthermore, the comparisons and mutual verification of analytical results from the mathematical model and the simulation results from the simulation model, as the principle line, run through the whole study. Eventually, the verified mathematical model and simulation model can serve as a tool to improve the performance of stability and anti-interference capability in the power system.

LLC resonant converter, PWM converter, PCM control, VM control, Small-signal model

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Last but not the least, we would like to thank our families for their love, caring and support. We extremely appreciate what they have dedicated and sacrificed for our education.

Ke Zhang, Kunyang Huang, Gothenburg, 05 2021

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1

Introduction

1.1 Research Background

In recent years, the fifth-generation (5G) cellular networks have played an increasingly significant role in telecommunication technology. The features of widespread connectivity, remarkably low latency and high-speed data transfer contribute to a better cellular network service for human beings [1]. Furthermore, this cutting-edge technology requires a high reliable 5G power system for providing power with fewer losses, less size and cost. To meet these requirements, there has been a series of well-designed power electronic circuits implemented in the 5G power system at Ericsson, and one system architecture basically is composed of a power factor correction (PFC) AC-DC converter, a front-end DC-DC converter and an isolated full-bridge DC-DC buck converter.

Specifically, in the part of the AC-DC converter, the application of a PFC not only realizes the established function but also aims to reduce the input current harmonics and gain power factor close to unity [2]. Furthermore, among many types of the front-end DC-DC converters, a LLC resonant converter, with a half-bridge topology, is commonly used in modern power electronic circuits. Compared with series resonant converters (SRCs) and parallel resonant converters(PRCs), the LLC resonant converter performs with a lower level of electro-magnetic Interference (EMI) and fewer power losses at a higher switching frequency [3]. Likewise, the isolated full-bridge DC-DC buck converter has gained widespread popularity in high-frequency switch-model applications. Moreover, for the purpose of voltage scaling and electrical isolation, a transformer, in general, is adopted in this circuit [4].

However, losses and disturbances still exist in the 5G power system, even though the main circuit has been designed under a deliberate consideration. Especially, once a perturbation signal occurs in the circuit, the input and output impedance of converters may intensify this perturbation and eventually have an negative effects on the entire power system [5]. The telecommunication signal may be affected and transformed with a low quality. In order to avoid or minimize the occurrence of this severe situation, the relevant research needs to be conducted on the anti-interference capability and stability of the power system. The small-signal modelling, as a feasible and efficiency mathematical method, has been widely adopted to analyse the aforesaid academic problem in the power system.

1.2 Purpose

In this thesis work, we intend to analyse impedance modelling of DC-DC converters in a typical telecom power system. To this aim, the small-signal modelling methodology is initially performed to construct the small-signal model of these converters. Then, fundamental small-signal transfer functions of these models are derived, and the deep physical significance of these transfer functions in the Bode plot is investigated. Meanwhile, correspondent simulation models, as the priority among priorities, are established on the platform of Simulink in Matlab. Furthermore, simulation outcomes mainly contain bode plots of aforementioned transfer functions, which can be verified by the theoretical analysis of the small-signal model. Eventually, the verified simulation model will be utilised as a tool to refine the anti-interference capability and stability of the power system, by optimizing the operating zones or tuning the parameters such as resistance, capacitance and inductance in the system.

2

Theory

2.1 Introduction of the LLC Resonant Converter

2.1.1 Working Principle

The LLC circuit topology illustrated in Figure 2.1, one of the most widely adopted front-end DC-DC converters, is characterised by two resonant frequencies. Accordingly, the LLC circuit has two working scenario. When the magnetizing inductor L_m is excluded from the resonant tank, the resonant frequency is derived and shown as (2.1). On the contrary, when L_m is involved in the resonant tank, the resonant frequency is shown at (2.2) [6].

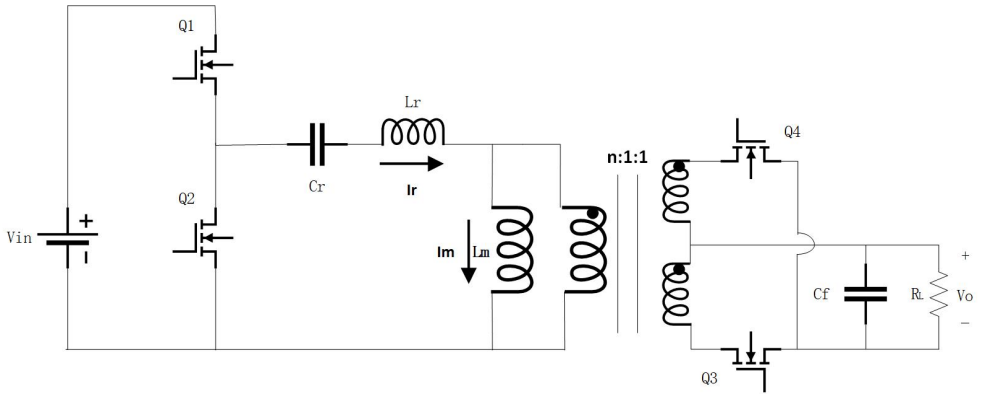


Figure 2.1: The schematic of the LLC resonant converter

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.1}$$

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2.2}$$

The operating principle of the LLC resonant converter is classified to three conditions in terms of the relation between the resonant frequency F_0 and switching frequency F_s. As shown in Figure 2.2, when F_s>F_0, the magnetizing inductance L_m is either clamped by $+V_{in}$ or $-V_{in}$ in terms of the switch status, and therefore have no effect on the resonance. Meanwhile, under this condition, the secondary-side Mosfets conduct continuously so that the LLC circuit operates in continuous conduction mode (CCM). Furthermore, the current at the resonant tank flows with a sharp

variation. Particularly, when the switching frequency is very high, the current at the resonant tank grows and reaches a high peak value, where a intensive current stress is induced in the circuit.

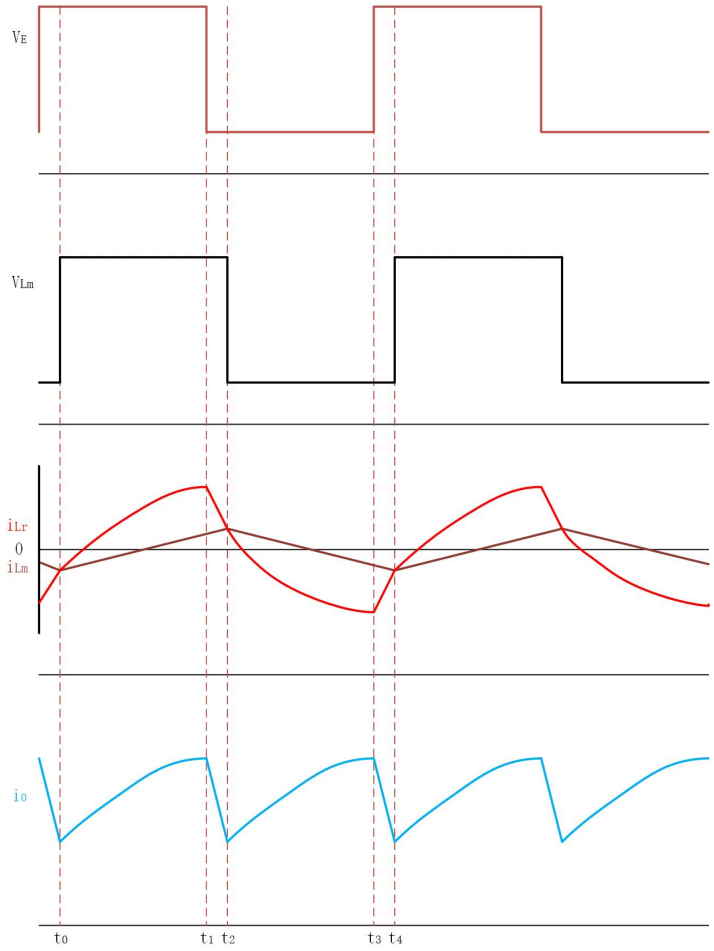


Figure 2.2: Waveform of the LLC circuit for $F_s > F_0$

When $F_s = F_0$, the LLC circuit operates in the boundary conduction mode (BCM), and the operating waveform is shown in Figure 2.3. When this circuit operates at the resonant frequency, the resonant current is perfectly sinusoidal with the lowest harmonic distortion and the best electro magnetic compatibility (EMC) performance. Meanwhile, the secondary side current flows in BCM, with neither a sharp drop in current nor a dead zone where the current is zero. Also, the voltage gain keeps unity and the LLC transfer function is insensitive to load variations. The output current can be approximated as a full-wave rectification and the switching losses are close to zero. In addition, when $F_s < F_0$, the LLC circuit operates in the discontinuous conduction mode (DCM) as shown at Figure 2.4.

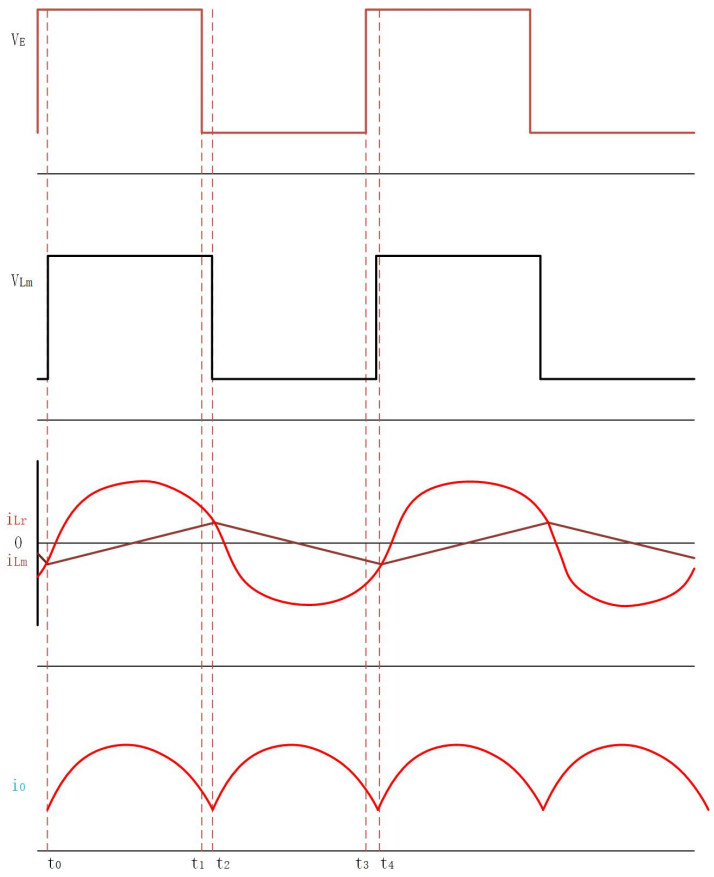


Figure 2.3: Waveform of the LLC circuit for F_s=F_0

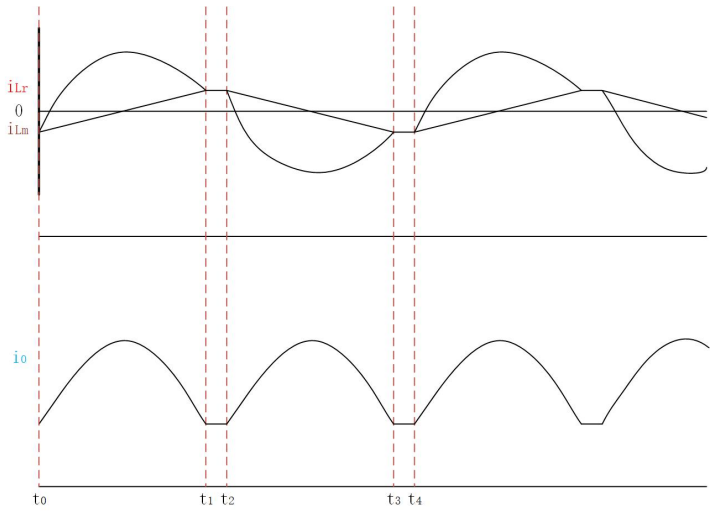


Figure 2.4: Waveforms of the LLC circuit for F_s<F_0

Figure 2.5 illustrates sub-circuits of the LLC resonant converter at each operating status. It is clearly seen from Figure 2.5 that the structure of the resonant tank changes at different time periods. During the time periods [t_0,t_1] and [t_2,t_3], L_m acts exactly in the same manner as the previous scenario when F_s>F_0, which is either clamped by $+V_{in}$ or $-V_{in}$ without participating in the resonance. In the periods

$[t_1,t_2]$ and $[t_3,t_4]$, L_m takes part in the resonant tank that consists of C_r and L_m in series with L_r. Simultaneously, the load at the second side is decoupled from the resonant tank. Based on illustrations above, it is found that the LLC resonant converter operates with two resonant frequencies at one switching cycle.

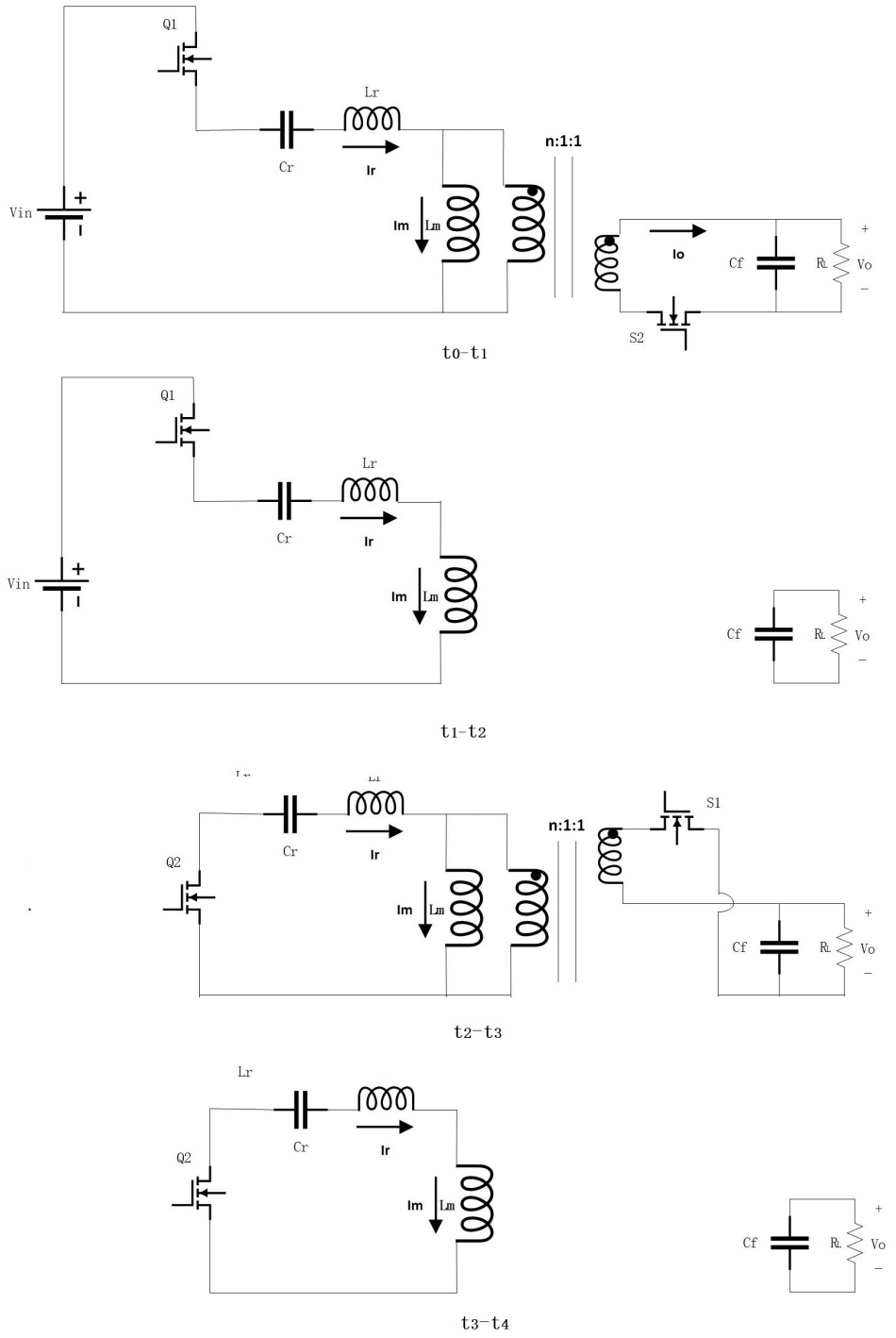


Figure 2.5: Sub-circuits of the LLC circuit for F_s<F_0

2.1.2 Simulation Model Establishment

The simulation model of the LLC circuit is implemented in the Simulink, where theoretical results illustrated in section above can be identified. The scheme of the circuit simulation is shown at Appendix A.1, and all the parameters of the LLC converter are shown at Table 2.1, where the parasitic parameters, equivalent series resistance (esr) of inductors and capacitors, are taken into consideration.

Table 2.1: Parameters of the LLC resonant converter

Parameter lists			
LLC converter	Symbol	Parameter	Value
	V_g	Input DC voltage	400 V
	V_o	Output DC voltage	56 V
	L_r	Resonant inductance	62 μH
	L_m	Magnetizing inductance	268 μH
	C_r	Resonant capacitance	9.4 nF
	C_f	Output capacitance	2000 μF
	R_{esr}	Equivalent series resistance	1 mΩ
	P_o	Output power	1000 W

2.2 Introduction of the PWM DC-DC Converter

2.2.1 Working Principle

The dc-dc converters, aiming to convert the unregulated dc input into a controlled dc output, are widely employed in diverse power electronic systems. According to the topological structures, the dc-dc converters are mainly classified to three basic converters known as the step-down (buck) converter, step-up (boost) converter and step-down/step-up (buck/boost) converter. In addition, for safety issues, an electrical isolation transformer is widely used in these converters, which derivatives several different typologies. Among them, the isolated full-bridge converter is known as a popular application. For the purpose of controlling the dc output at the desired level, the pulse-width modulation (PWM), as one of the most widely-used method, is normally applied to the dc-dc converters [7].

In this thesis work, the boost converter and isolated full-bridge dc-dc buck converter are implemented in the dc part of the 5G telecom power system. To be specific, the boost converter that serves as the preceding stage is used to prevent the input voltage to the isolated full-bridge converter from being under the requirement range. Therefore, in a general way, only the post-stage, the isolated full-bridge converter serves in the system. The topology of the PWM boost dc-dc converter is simplified to the structure illustrated in Figure 2.6. It is observed that the peak current mode (PCM) control is implemented in the system, which will be discussed in detail in the further chapter.

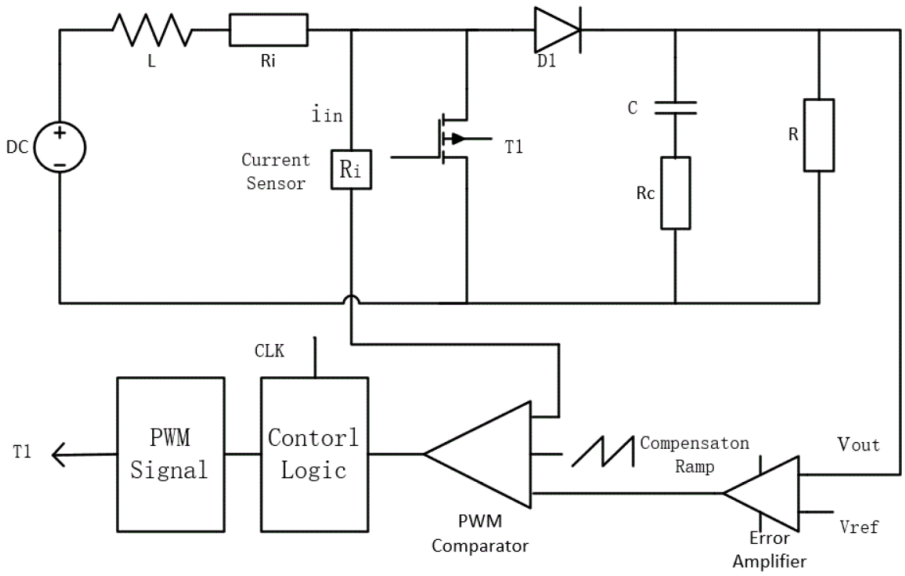
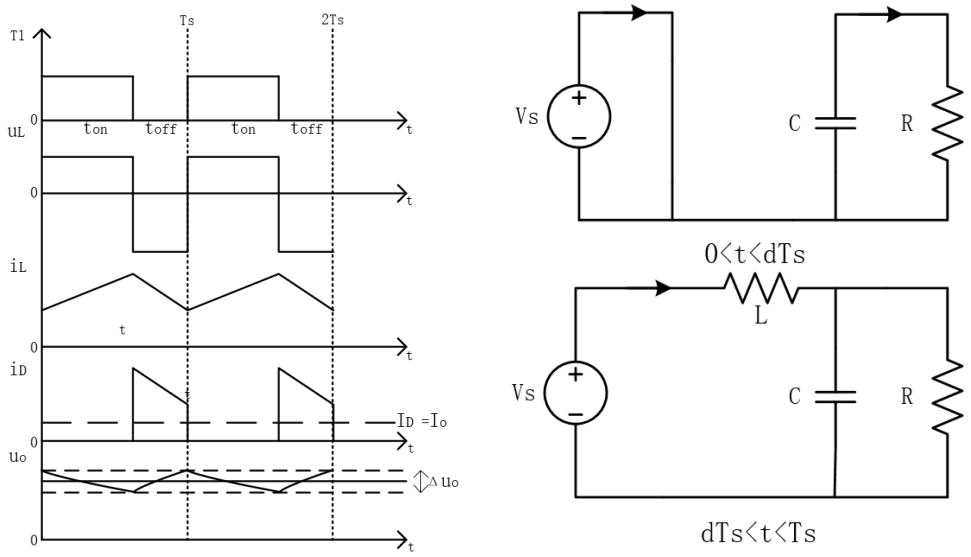


Figure 2.6: Schematic diagram of the PWM boost converter

The boost converter, as the name implies, generates a higher dc output voltage than the dc input voltage. Figure 2.7a shows the steady-state waveforms for the boost converter when considering the continuous-conduction model (CCM) with $i_L(t) > 0$.



(a) **(b)**

Figure 2.7: (a).Waveform of the PWM boost converter (b).Sub-circuits of the PWM boost converter

During the on-time period, the switch is on and then the diode is reverse biased, where the output voltage is isolated. During the off-time period, the switch is off and then the current flows through the diode, where the energy is transferred from

the input stage to the output stage. Furthermore, Figure 2.7b shows the sub-circuit of the PWM pre-boost converter over one period. When considering the integral of inductor voltage over the entire period is zero, the ratio of the input and output voltage is derived as

$$\begin{aligned} V_{in}t_{on} + (V_{in} - V_o)t_{off} &= 0 \\ \frac{V_o}{V_{in}} = \frac{T_s}{t_{off}} &= \frac{1}{1-D}, \end{aligned} \tag{2.3}$$

where D is the duty ratio [7].

The topology of the isolated full-bridge dc-dc buck converter is simplified to the structure illustrated in Figure 2.8, where the PCM serves as the controller as well. This converter, as the name implies, generates the dc output voltage smaller than the dc input voltage. As shown in Figure 2.8, the isolated full-bridge dc-dc buck converter includes two legs, each leg is implemented with two switches and anti-parallel diodes which are replaced by the Mosfet in the circuit. Typically, there are two PWM switching strategies applied in full-bridge converters, one is the bipolar voltage switching and the other is the unipolar voltage switching. In order to avoid the magnetic saturation of the isolated transformer, in this system, a bipolar voltage switching is taken into consideration [8].

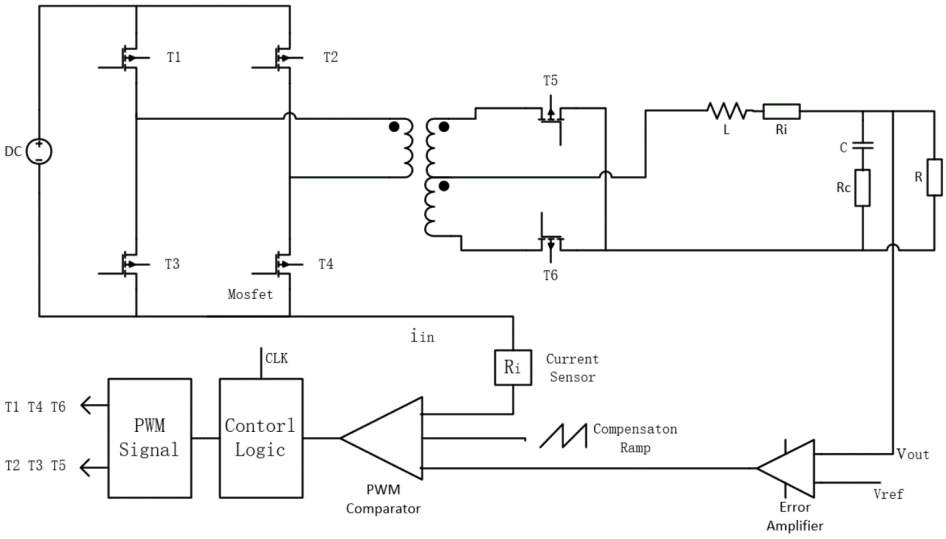
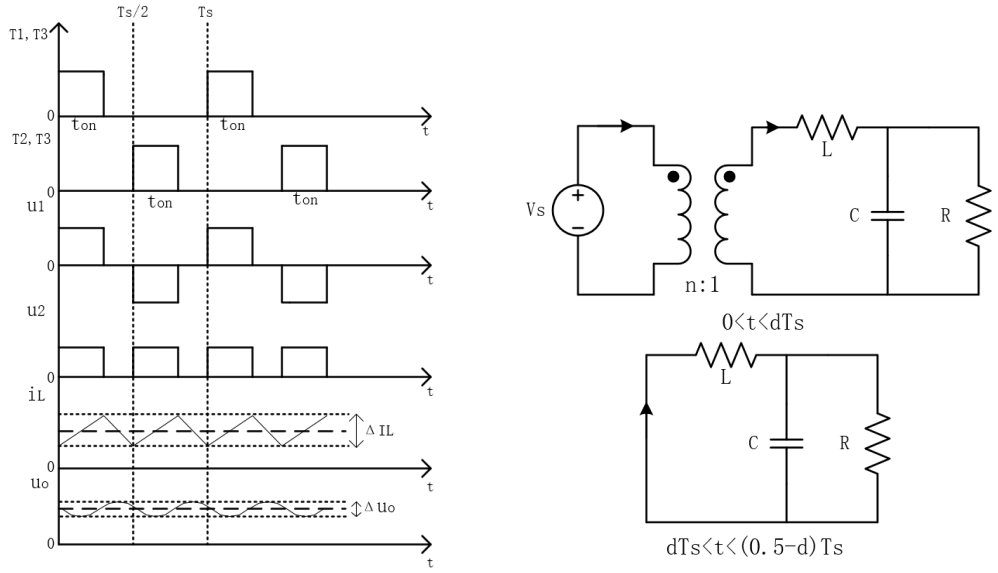


Figure 2.8: Schematic diagram of the PWM isolated full-bridge dc-dc buck converter

Figure 2.9a illustrates the steady-state waveforms for the PWM isolated full-bridge dc-dc buck converter in CCM. There are two switch groups T_1, T_4 and T_2, T_3, each group switches on or off synchronously and the phase degree between the two groups is 180°. This control strategy drives the secondary side voltage V_2 to form a periodic square wave, which eventually leads to the acquirement of the desired dc output voltage.



(a) **(b)**

Figure 2.9: (a).Waveform of the PWM isolated full-bridge dc-dc buck converter (b).Sub-circuit of the PWM isolated full-bridge dc-dc buck converter

Figure 2.9b shows the sub-circuit for half of a period. By considering that the integral of the inductor voltage is zero over half of the period, the relationship between the input and output voltage is derived as

$$\begin{aligned} (\frac{V_{in}}{n} - V_o)t_{on} &= V_o t_{off} \\ \frac{V_o}{V_{in}} &= \frac{t_{on}}{0.5nTs} = \frac{2D}{n}. \end{aligned} \tag{2.4}$$

2.2.2 Simulation Model Establishment

In order to evaluate the performance of these two converters, simulation models are constructed on the platform of Simulink in Matlab. Appendix A.2 and Appendix A.3 show the simulation diagram of the PWM isolated full-bridge buck dc-dc and the PWM pre-boost converter respectively, and all parameters are defined in terms of Table 2.2, where the parasitic parameters of the inductance and capacitance known as equivalent Series Resistance R_{esr} are taken into consideration, and all R_{esr} are simplified to be equivalent.

Table 2.2: Parameters for these two PWM converters

Parameter lists			
Pre-boost converter	Symbol	Parameter	Values
	V_s	Input DC voltage	36 V-42 V
	V_o	Output DC voltage	42 V
	L	Inductance	6.6 μH
	C	Capacitance	2040 nF
	R_{esr}	Equivalent series resistance	1 mΩ
	P_o	Output power	1000 W
Full-bridge buck converter	Symbol	Parameter	Values
	V_s	Input DC voltage	42 V-56 V
	V_o	Output DC voltage	17 V-32 V
	L	Inductance	4.7 μH
	C	Capacitance	200 μF
	R_{esr}	Equivalent series resistance	1 mΩ
	P_o	Output power	1000 W

The duty ratio is calculated by selecting the specific input and output voltage values from their ranges. Here, under the typical condition of $V_s = 56[V]$ and $V_o = 42[V]$, the simulation results is illustrated in Figure 2.10, where the output voltage rises with some oscillation and eventually stabilizes at the desire voltage level. Thus, the accuracy and functionality of the simulation model are proven.

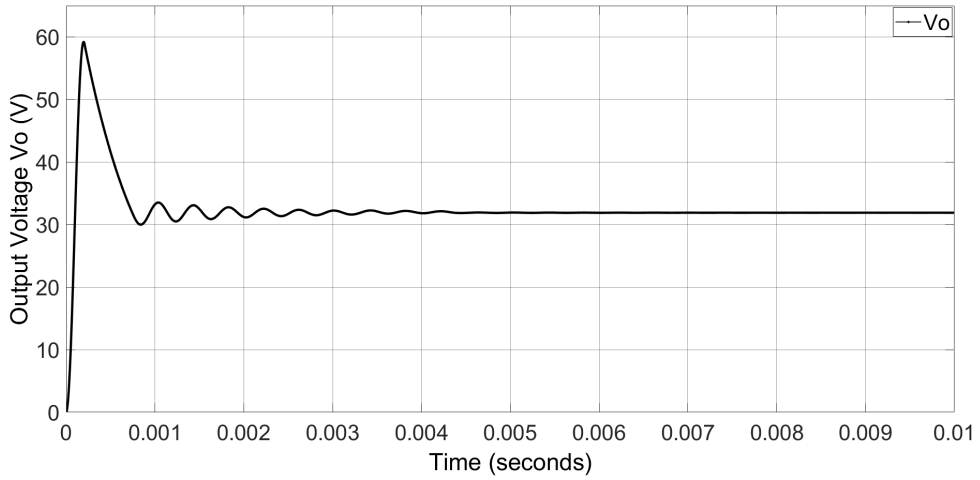


Figure 2.10: Dynamic performance of the PWM full-bridge buck converter

Likewise, the simulation model of the boost converter is shown in Appendix A.3. With the condition $V_s = 36[V]$ and $V_o = 42[V]$, the dynamic performance of the output voltage is illustrated in Figure 2.11.

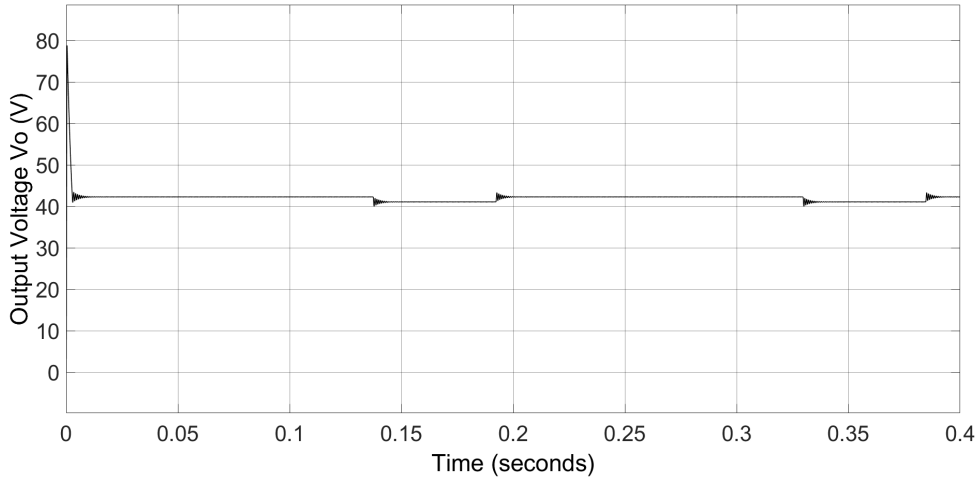


Figure 2.11: Dynamic performance of the PWM boost converter

As shown in Figure 2.10 and Figure 2.11 above, there are some oscillations in the output voltage. Thus, it is significant to apply the control system in the circuit.

3

Power Stage Small-Signal Modelling

3.1 Modelling of the LLC Resonant Converter

3.1.1 Extended Describing Function Method

3.1.1.1 Introduction to Extended Describing Function

The extended describing function (EDF) method is the main approach to investigate the small-signal LLC resonant circuit model [9]. Based on the principle of the LLC resonant converter, the nonlinear state equations can be written as

$$\dot{x} = Ax + Bu \tag{3.1}$$
$$y = Cx + Du \tag{3.2}$$

where $\dot{x}$ is the state vector, u is the input vector and y is the output variables.

By imposing the extended describing function concept, the nonlinear terms can be approximately substituted either by the fundamental harmonic elements or dc components. Therefore, the linear state equations can be derived by making the Fourier expansions of these terms.

Due to the harmonic balance, a nonlinear large-signal model of the LLC resonant converter power stage is determined. The inputs of this large-signal model equation set are varying slowly with the switching frequency. Thus, the steady-state solution is provided for a given operating point. Besides, the state equations of this small-signal model are established when there is a perturbation around the operating point.

3.1.1.2 Derivation of Nonlinear State Equation

A quasi-square wave voltage v_{AB}, generated by the active half-bridge circuit, is applied to the resonant tank of the LLC resonant circuit, as shown in Figure 3.1. The primary and secondary sides of the transformer are equivalent to the controlled voltage source and controlled current source respectively in Figure 3.1. The voltage at the primary side of the transformer is approximately described as $sgn(i_{Lr} - i_{Lm})$.

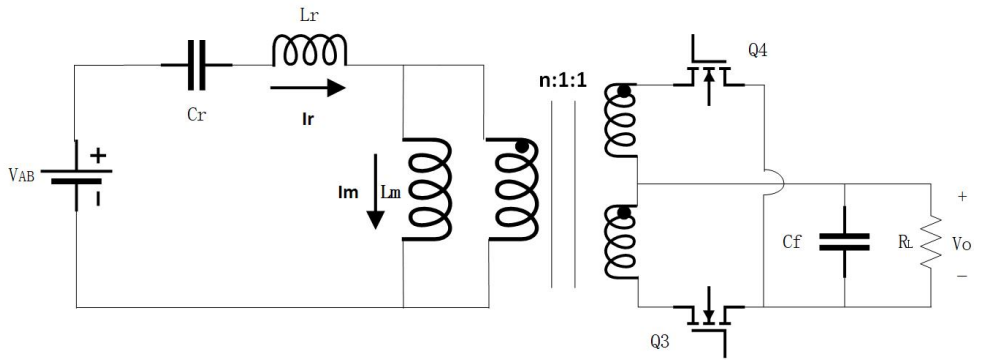


Figure 3.1: Equivalent circuit of the LLC resonant converter

According to the Kirchhoff's Circuit Laws(KCL), the state equations can be listed as

$$\begin{cases} v_{AB} = L_r \frac{di_{L_r}}{dt} + L_m \frac{di_{L_m}}{dt} + V_{C_r} \\ L_m \frac{di_{L_m}}{dt} = sgn(i_{L_r} - i_{L_m}) V_o n \\ i_{L_r} = C_r \frac{dv_{C_r}}{dt} \\ |i_{L_r} - i_{L_m}| \, n = C_o \frac{dv_{C_o}}{dt} + \frac{v_{C_o}}{R_L} \end{cases} . \tag{3.3}$$

3.1.1.3 Harmonic Approximation

The current and voltage waveforms of the LLC circuit tank can be estimated as a sinusoidal when the circuit operates at the steady state. Therefore, the resonant current i_r, voltage v_{cr} and the magnetizing circuit i_m at the primary side resonant tank are approximated to fundamental harmonics that are derived by the Fourier series,

$$\begin{cases} i_{L_r}(t) = i_{L_{rs}}(t) sin(w_s)t + i_{L_{rc}}(t) cos(w_s)t \\ v_{C_r}(t) = v_{C_{rs}}(t) sin(w_s)t + v_{C_{rc}}(t) cos(w_s)t \\ i_{L_m}(t) = i_{L_{ms}}(t) sin(w_s)t + i_{L_{mc}}(t) cos(w_s)t \\ \frac{di_{L_r}}{dt} = (\frac{di_{L_{rs}}}{dt} - w_s i_{L_{rc}}) sinw_s t + (\frac{di_{L_{rc}}}{dt} + w_s i_{L_{rs}}) cosw_s t \\ \frac{di_{L_m}}{dt} = (\frac{di_{L_{ms}}}{dt} - w_s i_{L_{mc}}) sinw_s t + (\frac{di_{L_{mc}}}{dt} + w_s i_{L_{ms}}) cosw_s t \\ \frac{dv_{C_r}}{dt} = (\frac{dv_{C_{rs}}}{dt} - w_s v_{C_{rc}}) sinw_s t + (\frac{dv_{C_{rc}}}{dt} + w_s v_{C_{rs}}) cosw_s t \end{cases} . \tag{3.4}$$

3.1.1.4 Applying Extended Describing Function

The EDF method is an effective approach that turns nonlinear functions into linear patterns by only adopting the fundamental terms of the nonlinear system. Referring to the LLC circuit, the nonlinear components in (3.3) can be described by the Fourier functions in (3.5),

$$\begin{cases} V_{AB} = f_1(v_g) sin(w_s)t \\ sgn(i_{Lr} - i_{Lm}) \cdot v_0 \cdot n = f_2(i_{Lrs} - i_{Lms}, v_{C0}) sin(w_s)t + f_3(i_{Lrc} - i_{Lmc}, v_{C0}) cos(w_s)t \\ |i_{Lr} - i_{Lm}| = f_4(i_{Lrs} - i_{Lms}, i_{Lrc} - i_{Lmc}) \end{cases} . \tag{3.5}$$

$f_1(v_g)$, $f_2(iLrs - i_{Lms}, v_{C0})$, $f_3(i_{Lrc} - i_{Lmc}, v_{C0}$ and $f_4(i_{Lrs} - i_{Lms}, i_{Lrc} - i_{Lmc})$ are the

functions of the EDF method shown in (3.6),

$$\begin{cases} f_1(v_g) = \frac{2}{\pi} \cdot v_g \\ f_2(i_{Lrs} - i_{Lms}, v_{C0}) = \frac{4}{\pi} \frac{iLrs - i_{Lms}}{i_p} \cdot v_{C0} \cdot n \\ f_3(i_{Lrc} - i_{Lmc}, v_{C0}) = \frac{4}{\pi} \frac{iLrc - i_{Lmc}}{i_p} \cdot v_{C0} \cdot n \\ f_4(i_{Lrs} - i_{Lms}, i_{Lrc} - i_{Lmc}) = \frac{2}{\pi} \cdot i_p \\ i_p = \sqrt{(i_{Lrs} - i_{Lms})^2 + (i_{Lrc} - i_{Lmc)^2}} \end{cases} . \tag{3.6}$$

3.1.1.5 Harmonic Balance

Harmonic balance is a powerful frequency domain solution to acquire the steady-state results of the nonlinear differential equations. Therefore, the harmonic balance method is frequently applied to solve the LLC resonant circuit. By substituting (3.4), (3.5) and (3.6) into (3.3), it gives

$$\begin{cases} L_r \cdot (\frac{di_{Lrs}}{dt} - \omega_s i_{Lrc}) + v_{Crs} + L_m \cdot (\frac{di_{Lms}}{dt} - \omega_s i_{Lmc}) = \frac{2}{\pi} \cdot v_g \\ L_r \cdot (\frac{di_{Lrc}}{dt} + \omega_s i_{Lrs}) + v_{Crc} + L_m \cdot (\frac{di_{Lmc}}{dt} + \omega_s i_{Lms}) = 0 \\ L_m \cdot (\frac{di_{Lms}}{dt} - \omega_s i_{Lmc}) = \frac{4}{\pi} \frac{i_{Lrs} - i_{Lms}}{i_p} \cdot v_0 \cdot n \\ L_m \cdot (\frac{di_{Lmc}}{dt} + \omega_s i_{Lms}) = \frac{4}{\pi} \frac{i_{Lrc} - i_{Lmc}}{i_p} \cdot v_0 \cdot n \\ C_r \cdot (\frac{v_{Crs}}{dt} - \omega v_{Crc}) = i_{Lrs} \\ C_r \cdot (\frac{v_{Crc}}{dt} + \omega v_{Crs}) = i_{Lrc} \\ C_f \frac{dv_{cf}}{dt} + \frac{v_{cf}}{R_L} = \frac{2}{\pi} \cdot i_p \cdot n \end{cases} . \tag{3.7}$$

3.1.1.6 Obtaining Steady-State Point

Once the circuit reaches the steady-state point, the differential terms of the variables in (3.7) that are unchangeable with time are all fixed to zero. These equations are rewritten as

$$\begin{cases} -L_r \Omega_s I_{Lrc} + V_{Crs} - L_m \Omega_s I_{Lmc} = \frac{2}{\pi} V_g \\ L_r \Omega_s \\ I_{Lrs} + v_{Crc} + L_m \Omega_s I_{Lms} = 0 \\ L_m - \Omega_s I_{Lmc}) = \frac{4}{pi} \frac{I_{Lrs} - I_{Lms}}{I_p} v_0 n \\ L_m \Omega_s I_{Lms} = \frac{4}{\pi} \frac{I_{Lrc} - I_{Lmc}}{I_p} V_0 n \\ -\Omega C_r V_{Crc} = I_{Lrs} \\ \Omega C_r V_{Crs} = I_{Lrc} \\ \frac{V_{cf}}{R_L} = \frac{2}{\pi} I_p n \\ I_p = \sqrt{(I_{Lrs} - I_{Lms})^2 + (I_{Lrc} - I_{Lmc)^2}} \end{cases} . \tag{3.8}$$

According to the given parameters of V_g, R_L and Ω_s, the conversion ratio of the voltage at steady state is found as

$$M = \frac{2nV_o}{V_g} = \left| \frac{j\omega_n L_n}{j\omega_n (L_n + 1 + \frac{1}{\omega_n^2}) + \frac{\pi^2}{8} Q (1 - \omega_n^2) L_n} \right|, \tag{3.9}$$

where $\omega_n = \frac{\Omega_s}{\Omega_o} = \frac{F_s}{F_o}$, $L_n = \frac{L_m}{L_r}$, $Q = \frac{\sqrt{L_r / C_r}}{n^2 \cdot R_L}$.

3.1.1.7 Perturbation and Linearization of Harmonic Balance Equations

It is assumed that the variables have two components including a constant DC part and an AC element as a small signal. The perturbed variables are illustrated at (3.10), it gives

$$\begin{cases} v_g = V_g + \hat{v_g} \\ \omega_s = \Omega_s + \hat{\omega_s} \\ i_{Lrs} = I_{Lrs} + \hat{i_{Lrs}} \\ i_{Lrc} = I_{Lrc} + \hat{i_{Lrc}} \\ i_{Lms} = I_{Lms} + \hat{i_{Lms}} \\ i_{Lmc} = I_{Lmc} + \hat{i_{Lmc}} \\ v_{Crs} = V_{Crs} + \hat{v_{Crs}} \\ v_{Crc} = V_{Crc} + \hat{v_{Crc}} \\ v_{Co} = V_{Co} + \hat{v_{Co}} \end{cases} . \tag{3.10}$$

By submitting the variables at (3.10) to (3.7), the non-linear state equations array is derived as

$$\begin{cases} K \cdot \frac{d\hat{x(t)}}{dt} = A\hat{x(t)} + B\hat{u(t)} \\ \hat{y(t)} = C\hat{x(t)} \end{cases} . \tag{3.11}$$

3.1.2 Equivalent Circuit of the LLC Resonant Converter

3.1.2.1 Simplified Resonant Tank

Based on the EDF method, the small-signal model of the inductance and capacitance in the resonant tank are shown in Figure 3.2 and Figure 3.3 respectively. The inductor model has two parts including the complex component caused by the effect of the switching frequency and the perturbed voltage source. The capacitor contains a complex impedance and a current source which are induced by the switching frequency [10].

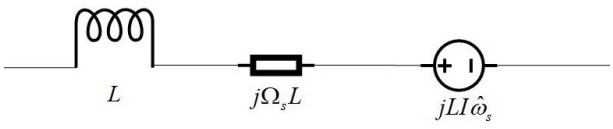


Figure 3.2: Small-signal model of inductance

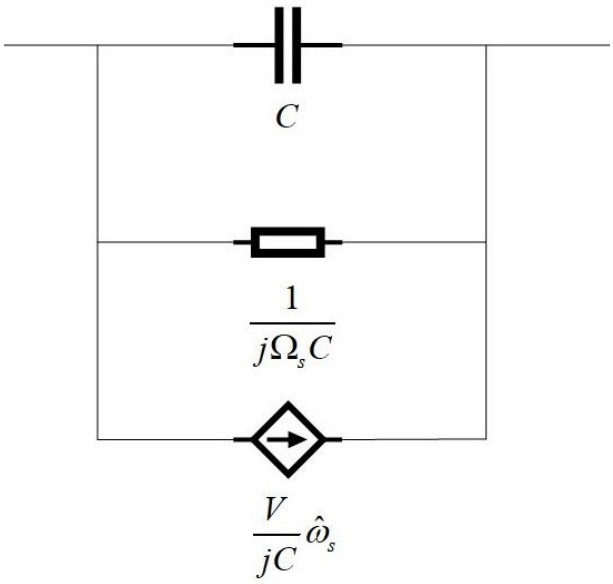


Figure 3.3: Small-signal model of capacitance

In order to simplify the resonant tank further, it is vital to inspect the complex shunt and controlled current source. Firstly, under the condition of $\hat{\omega} = 0$, the current source is removed from this model, as shown at Figure 3.4. The model of this case ends up as

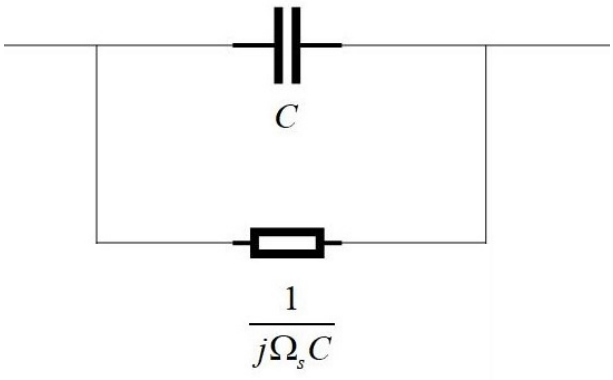


Figure 3.4: Simplified small-signal model of capacitance

$$\frac{\hat{v}}{\hat{i}} = \frac{1}{sC + j\Omega_s C} = \frac{\frac{-s}{j\Omega_s} + 1}{j\Omega_s C(1 + \frac{s^2}{\Omega^2})}. \tag{3.12}$$

As the modulation frequency is much lower than the switching frequency, the second term of the denominator is much smaller than one, and therefore can be neglected. The mathematical analysis is simplified further to the following

$$\frac{\hat{v}}{\hat{i}} \approx \frac{\frac{-s}{j\Omega_s} + 1}{j\Omega_s C} = \frac{s}{\Omega_s^2 C} + \frac{1}{j\Omega_s C}. \tag{3.13}$$

By using (3.13), the original model can be replaced by an inductor and an impedance in series.

It is found that the similar rule is also suitable for the general case that is illustrated in Figure 3.5. By applying the Thevenin's Theorem, the final model is further simplified as Figure 3.6 shown [10].

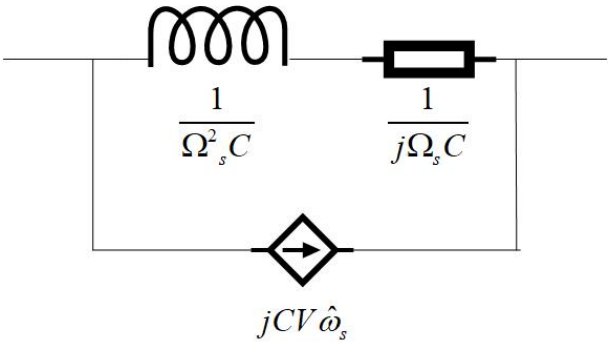


Figure 3.5: Equivalent capacitance model in case of $\omega_m \ll \Omega_s$

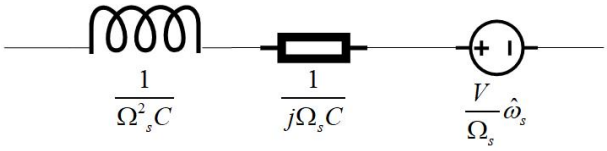


Figure 3.6: Simplified equivalent capacitance model by the Thevenin's Theorem

3.1.2.2 Equivalent Circuit Model of LLC with $F_s \geqq F_o$

By applying the small-signal modelling method illustrated above, the equivalent circuit is derived and presented in Figure 3.7. L_{eq} and X_{eq} in the equivalent circuit is shown at (3.14) based on the simplification of the resonant tank [10].

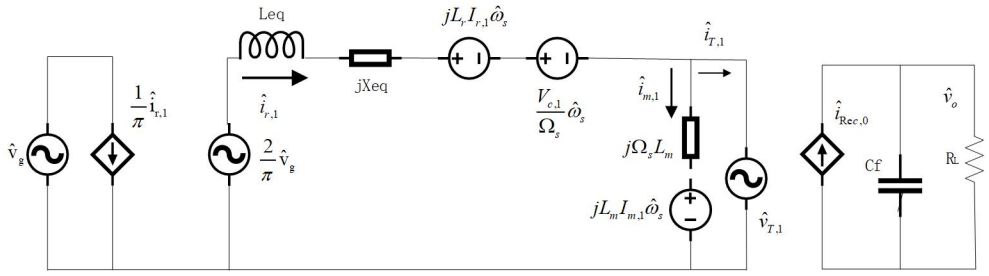


Figure 3.7: Small-signal model of LLC circuit for $F_s \geq F_o$ with simplified resonant tank

$$\begin{cases} L_{eq} = L_r + \frac{1}{C_r \Omega_s^2} = L_r(1 + \frac{\Omega_o^2}{\Omega_s^2}) \\ X_{eq} = \Omega_s L_r - \frac{1}{\Omega_s C_r} \end{cases} . \tag{3.14}$$

According to the Extended Describing Function method, separating the equivalent circuit into sine and cosine part is a suitable methodology to tackle the transfer function. The circuit model that has two separated parts is shown at Figure 3.8, and G_s, G_c, R_s, R_c, k_{rs}, k_{rc}, k_s and k_c are expressed as (3.15) shows,

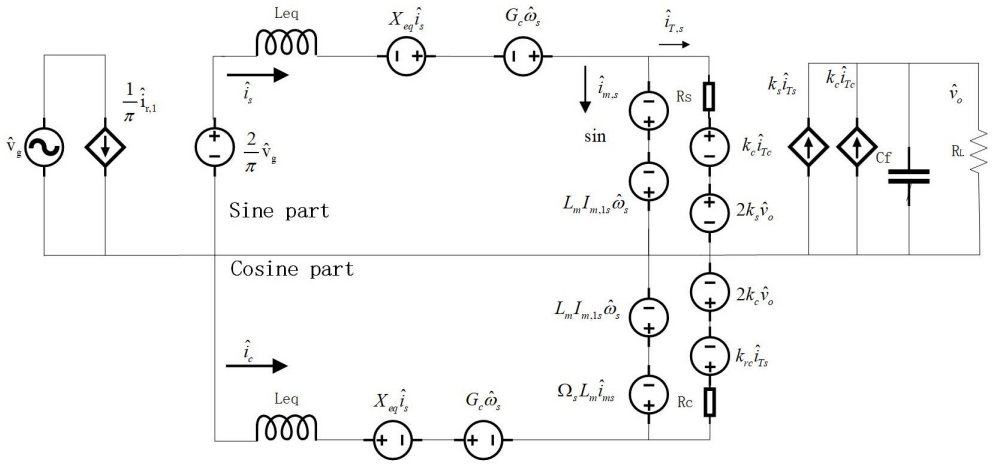


Figure 3.8: Sine and cosine equivalent circuit model of LLC converter for $F_s \geq F_o$

$$\begin{cases} G_s = L_rIr,1c + \frac{V_{c,1s}}{\Omega_s} \\ G_c = L_rIr,1s - \frac{V_{c,1c}}{\Omega_s} \\ R_s = \frac{4n}{\pi}\frac{V_o}{\sqrt{I_{T,1s}^2+I_{T,1c}^2}}\frac{I_{T,1c}^2}{I_{T,1s}^2+I_{T,1c}^2} \\ R_c = \frac{4n}{\pi}\frac{V_o}{\sqrt{I_{T,1s}^2+I_{T,1c}^2}}\frac{I_{T,1s}^2}{I_{T,1s}^2+I_{T,1c}^2} \\ k_{rs} = k_{rc} = -\frac{4n}{\pi}\frac{V_o}{\sqrt{I_{T,1s}^2+I_{T,1c}^2}}\frac{I_{T,1s}I_{T,1c}}{I_{T,1s}^2+I_{T,1c}^2} \\ k_s = \frac{2n}{\pi}\frac{I_{T,1s}}{\sqrt{I_{T,1s}^2+I_{T,1c}^2}} \\ k_c = \frac{2n}{\pi}\frac{I_{T,1c}}{\sqrt{I_{T,1s}^2+I_{T,1c}^2}} \end{cases}, \tag{3.15}$$

where $I_{r,1s}$, $I_{r,1c}$, $V_{c,1s}$, $V_{c,1c}$, $I_{T,1s}$ and $I_{T,1c}$ are derived from the steady state equivalent circuit model. Besides, it is feasible to apply the superposition theorem to derive an uncoupled equivalent circuit model shown at Figure 3.9.

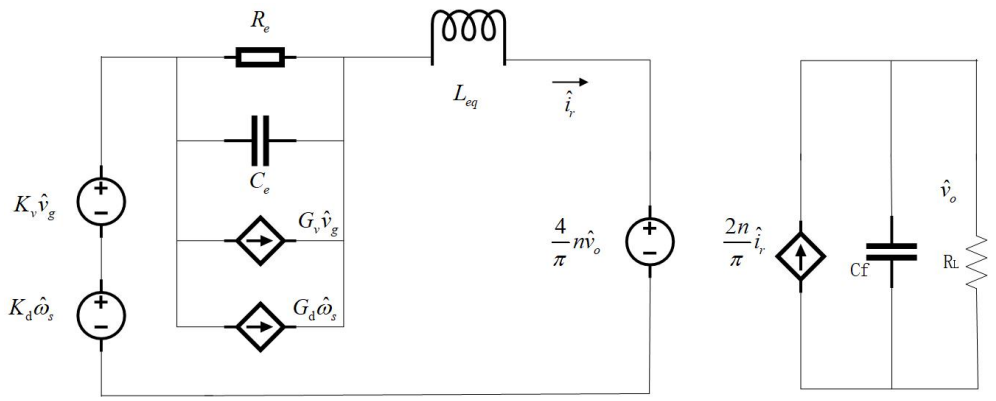


Figure 3.9: Small-signal model of LLC circuit for $F_s \geq F_o$ by superposition theorem

All the parameters are shown at (3.16),

$$\begin{cases} L_{eq} = L_r + \frac{1}{C_r \Omega_s^2} = L_r(1 + \frac{\Omega_o^2}{\Omega_s^2}) \\ C_e = \frac{1}{L_{eq}(\Omega_s - \Omega_o)^2} \\ R_e = \frac{L_{eq}|X_{eq}|(\Omega_s - \Omega_o)}{R_{eq}} \\ G_d = \frac{2V_g L_n}{\pi \omega_o R_e} \left(\frac{\frac{1}{\omega_n(\frac{\pi^2}{8}QL_n)^2)(\frac{1}{\omega_n^2} - \omega_n^2) - (L_n + 1 - \frac{1}{\omega_n^2})\frac{2}{\omega_n^3}}}{\sqrt{(L_n + 1 - \frac{1}{\omega_n^2})^2 + ((\frac{1}{\omega_n} - \omega_n)\frac{\pi^2}{8}QL_n)^2}^3} + \frac{2}{L_n^2} \right) \\ K_d = -\frac{4V_g}{\pi \omega_o L_n} \\ G_v = \frac{X_{eq}}{\pi \sqrt{R_{eq}^2 + X_{eq}^2}} \\ K_v = \frac{4V_g L_n \omega_n}{\pi^2 R_{eq}} \frac{L_n + 1 - \frac{1}{\omega_n^2}}{\sqrt{(L_n + 1 - \frac{1}{\omega_n^2})^2 + ((\frac{1}{\omega_n} - \omega_n)\frac{\pi^2}{8}QL_n)^2}} \end{cases} . \tag{3.16}$$

3.1.2.3 Equivalent Circuit Model of LLC with $F_s < F_o$

As mentioned in Chapter 2.1.1, the magnetizing inductance is excluded from the resonance during [t_0,t_1] and [t_2,t_3], while being coupled with the resonant tank over the time of [t_1,t_2] and [t_3,t_4]. The time span of [t_0,t_1] is exactly the resonant period T_o. The equivalent inductance modeled in the equivalent circuit with respect to the ratio between $\frac{T_o}{T_s}$ and $\frac{T_s - T_o}{T_s}$ is derived as

$$L_{r'} = L_r + L_m \frac{F_o - F_s}{F_o}. \tag{3.17}$$

The equivalent circuit, shown at Figure 3.10 with simplified resonant tank, is formulated in the similar methodology as the previous case [10].

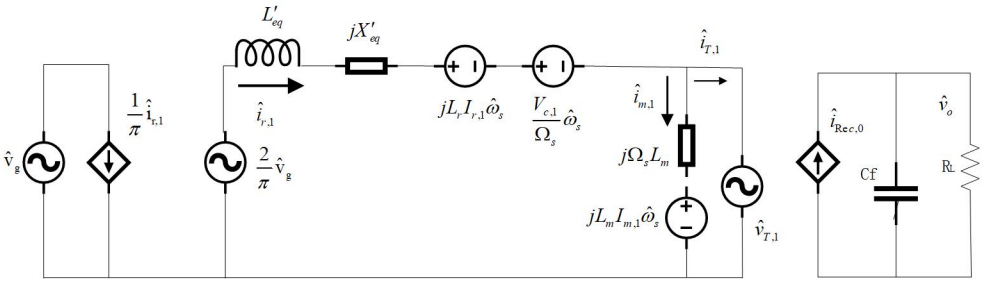


Figure 3.10: Small-signal model of LLC circuit for $F_s < F_o$ with simplified resonant tank

$$\begin{cases} L'_{eq} = L_r(1 + \frac{1}{\Omega_n^2}) + L_m(1 - \Omega_n) \\ X'_{eq} = \Omega_s(L_r + L_m(1 - \Omega_n)) - \frac{1}{\Omega_s C_r} \end{cases} . \tag{3.18}$$

As Section 3.1.2.2 mentioned, the equivalent circuit is separated into sine and cosine components as Figure 3.11 shows.

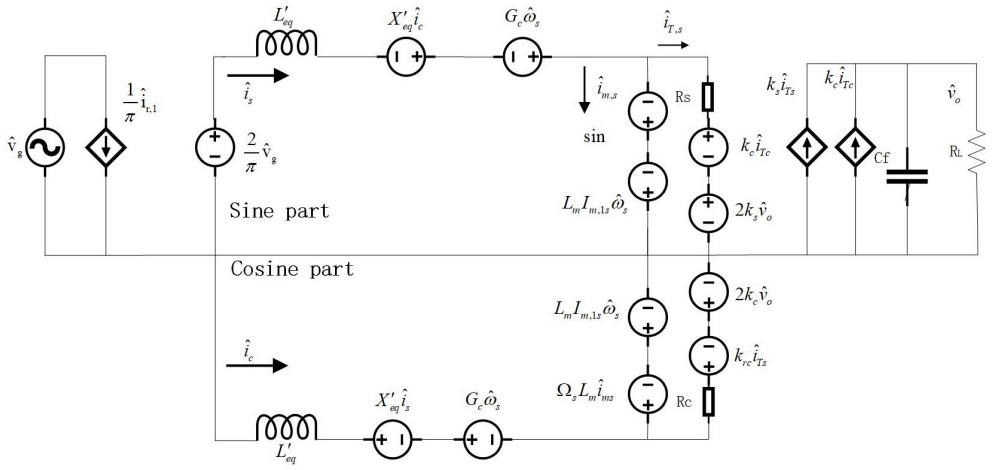


Figure 3.11: Sine and cosine equivalent circuit model of LLC converter for $F_s < F_o$

By applying the superposition theorem, the non-coupled circuit is reconstructed in Figure 3.12, which is more convenient to derive transfer functions in further study [10].

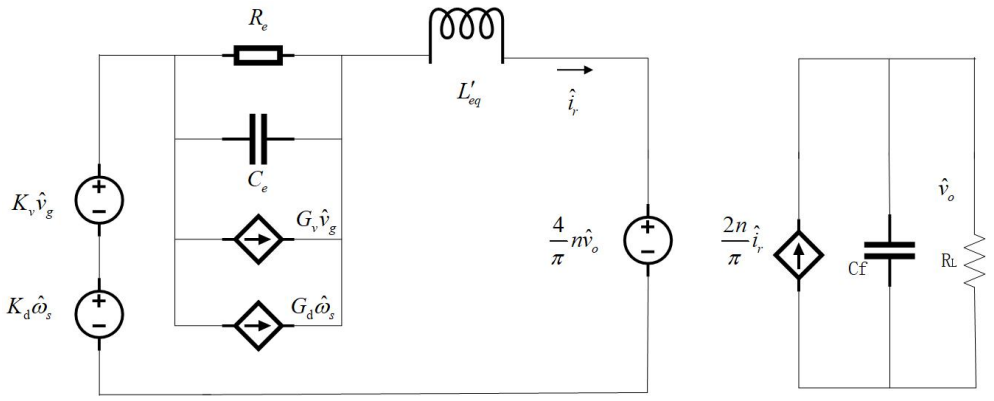


Figure 3.12: Small-signal model of LLC circuit for $F_s < F_o$ by superposition theorem

3.1.3 Power Stage Transfer Function Expressions

The power stage transfer functions derived from Figure 3.9 and Figure 3.12 are listed in Table 3.1 and Table 3.2 respectively, where Z_o is the load current to output (output impedance) transfer function [10].

Table 3.1: Output impedance transfer function for $F_s \geq F_o$

$$\begin{cases} \frac{\hat{v}_o(s)}{\hat{\omega}_s(s)} = G_{DC}\frac{X_{eq}^2+R_{eq}^2}{(s^2L_{eq}^2+sL_{eq}R_{eq}+X_{eq}^2)(1+R_LC_fs)+R_{eq}(sL_{eq}+R_{eq})} \\ G_{DC} = \frac{V_g}{2n}\frac{L_n}{\omega_n\omega_o}\frac{(\frac{1}{\omega_n^2}-\omega_n^2)(\frac{\pi^2}{8}QL_n)^2-\frac{2}{\omega_n^2}(L_n+1-\frac{1}{\omega_n^2})}{\sqrt{(L_n+1-\frac{1}{\omega_n^2})^2+((\frac{1}{\omega_n}-\omega_n)\frac{\pi^2}{8}QL_n)^2}^3} \\ L_{eq} = (1+\frac{\Omega_o^2}{\Omega_s^2})L_r, R_{eq} = \frac{8}{\pi^2}n^2R_L, \\ X_{eq} = \Omega_sL_r - \frac{1}{\Omega_sL_r}, Q = \frac{\sqrt{L_r/C_r}}{n^2R_L}, L_n = \frac{L_m}{L_r} \end{cases} \quad (3.19)$$

$$\begin{cases} \frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{1}{2n}M\frac{X_{eq}^2+R_{eq}^2+L_{eq}R_{eq}s}{(s^2L_{eq}^2+sL_{eq}R_{eq})(1+R_LC_fs)+R_{eq}(sL_{eq}+R_{eq})} \\ M = \left|\frac{j\omega_nL_n}{j\omega_n(L_n+1+\frac{1}{\omega_n^2})+\frac{\pi^2}{8}Q(1-\omega_n^2)L_n}\right| \end{cases} \quad (3.20)$$

$$Z_o(s) = R_L\frac{s^2L_{eq}^2+sL_{eq}R_{eq}+X_{eq}^2}{(s^2L_{eq}^2+sL_{eq}R_{eq}+X_{eq}^2)(1+R_LC_fs)+R_{eq}(sL_{eq}+R_{eq})} \quad (3.21)$$

Table 3.2: Output impedance transfer function for $F_s < F_o$

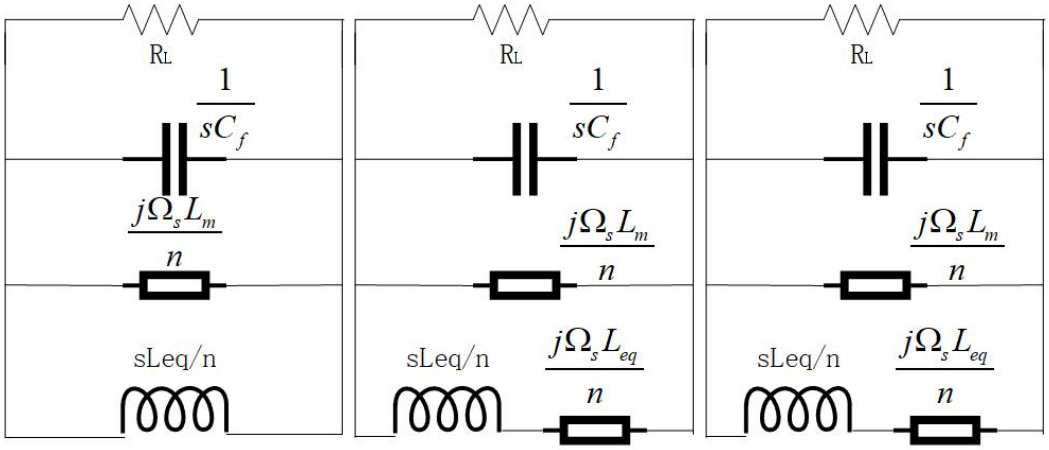
$$\begin{cases} \frac{\hat{v}_o(s)}{\hat{\omega}_s(s)} = G_{DC}\frac{X_{eq}'^2+R_{eq}^2}{(s^2L_{eq}^2+sL_{eq}'R_{eq}+X_{eq}'^2)(1+R_LC_fs)+R_{eq}(sL_{eq}'+R_{eq})} \\ G_{DC} = \frac{V_g}{2n}\frac{L_n}{\omega_n\omega_o}\frac{(\frac{1}{\omega_n^2}-\omega_n^2)(\frac{\pi^2}{8}QL_n)^2-\frac{2}{\omega_n^2}(L_n+1-\frac{1}{\omega_n^2})}{\sqrt{(L_n+1-\frac{1}{\omega_n^2})^2+((\frac{1}{\omega_n}-\omega_n)\frac{\pi^2}{8}QL_n)^2}^3} \\ L_{eq}' = L_r(1+\frac{1}{\Omega_n^2})+L_m(1-\Omega_n), \\ X_{eq}' = \Omega_s(L_r+L_m(1-\Omega_n))-\frac{1}{\Omega_sC_r}, R_{eq} = \frac{8}{\pi^2}n^2R_L \end{cases} \quad (3.22)$$

$$\begin{cases} \frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{1}{2n}M\frac{X_{eq}'^2+R_{eq}^2+L_{eq}'R_{eq}s}{(s^2L_{eq}'^2+sL_{eq}'R_{eq})(1+R_LC_fs)+R_{eq}(sL_{eq}'+R_{eq})} \\ M = \left|\frac{j\omega_nL_n}{j\omega_n(L_n+1+\frac{1}{\omega_n^2})+\frac{\pi^2}{8}Q(1-\omega_n^2)L_n}\right| \end{cases} \quad (3.23)$$

$$Z_o(s) = R_L\frac{s^2L_{eq}'^2+sL_{eq}'R_{eq}+X_{eq}'^2}{(s^2L_{eq}'^2+sL_{eq}'R_{eq}+X_{eq}'^2)(1+R_LC_fs)+R_{eq}(sL_{eq}'+R_{eq}')} \quad (3.24)$$

3.1.4 Bode Plot Representations and Physical Meanings of Power Stage Transfer Functions

In order to analyse the physical meanings behind power stage transfer functions, the bode plots of transfer functions and correspondent equivalent circuits need to be studied. Especially, among these transfer functions, the output impedance, as an essential link to the post-stage (PWM converters) analysis, is mainly illustrated in this section. Figure 3.13 diagrams the equivalent circuit of the output impedance under there different conditions of $F_s = F_o$, $F_s > F_o$ and $F_s < F_o$, and the relevant Bode plots of the output impedance transfer functions are shown in Figure 3.14.

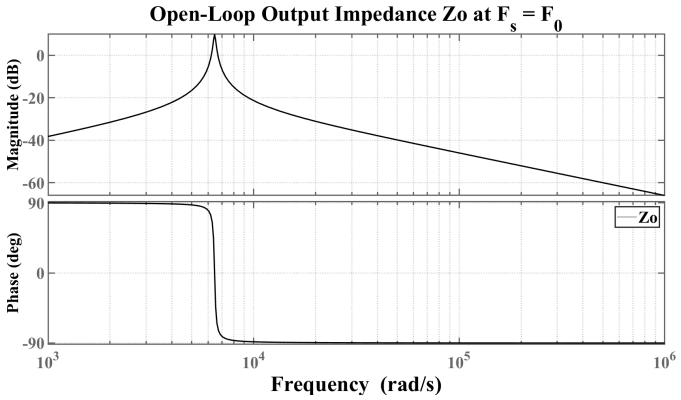


(a) **(b)** **(c)**

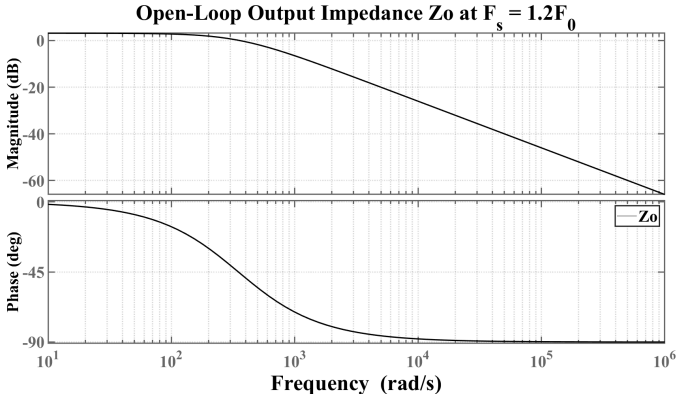
Figure 3.13: Equivalent circuit of output impedance at $F_s = F_o$, $F_s > F_o$ and $F_s < F_o$

In Figure 3.13a, under the condition of $F_s = F_o$, the equivalent circuit, with four components in parallel, is characterised with the parallel resonance, and there is a resonant frequency point where their two reactive components $\frac{1}{sC_f}$ and $\frac{sL_{eq}}{n}$ cancel each other. At the resonance frequency, the parallel LC circuit acts like an open circuit with the current flowing through R_L and $\frac{j\Omega_s Lm}{n}$, where the total impedance reaches the maximum value. Below the resonant frequency, the circuit acts like an inductive circuit, whereas the circuit behaves as a capactive circuit when the frequency exceeds the resonant point. Meanwhile, the illustration above can be verified by the Bode plot of the output impedance as shown in Figure 3.14a, where the Amplitude-Frequency curve shows the typical characteristics of the parallel resonant circuit.

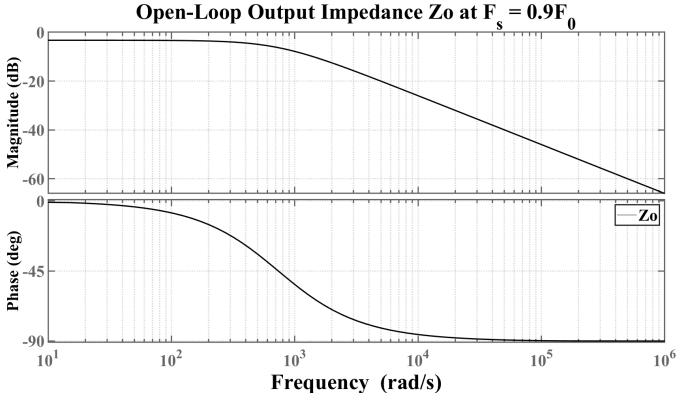
The equivalent circuit of other two cases of $F_s > F_o$ and $F_s < F_o$ are shown in Figure 3.14b and Figure 3.14c. It is found that these two equivalent circuits are established with the same topology, where an additional inductive element $\frac{j\Omega_s L_{eq}}{n}$ is connected in series with the inductance $\frac{sL_{eq}}{n}$. Owing to the fact that the inductive components predominate in the equivalent circuit, the total impedance in the equivalent circuit is predominately characterised by the capacitance along the frequency domain according to the property of the parallel resonant circuit. This phenomenon is verified by the Bode plot of the output impedance transfer function shown in Figure 3.14b and Figure 3.14c, where the phase angle decreases from $0°$ to $-90°$ with the frequency increase.



(a)



(b)

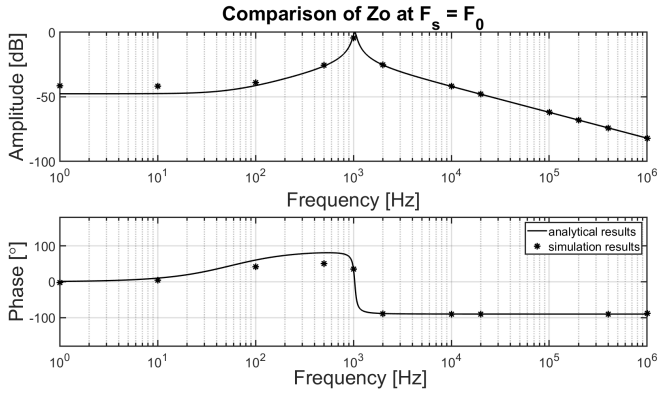


(c)

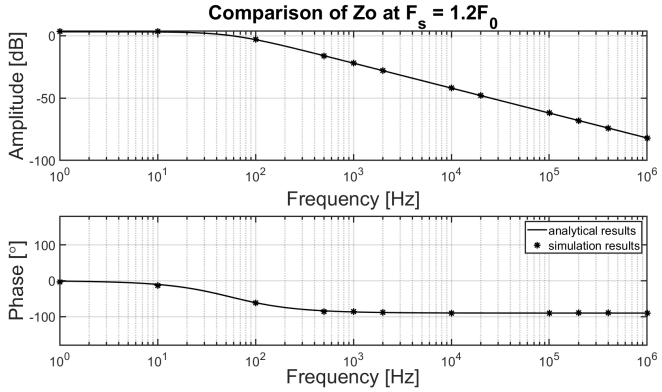
Figure 3.14: Bode plot of output impedance transfer functions at $F_s = F_o$, $F_s \geq F_o$ and $F_s < F_o$

3.1.5 Analytical Transfer Functions Verification

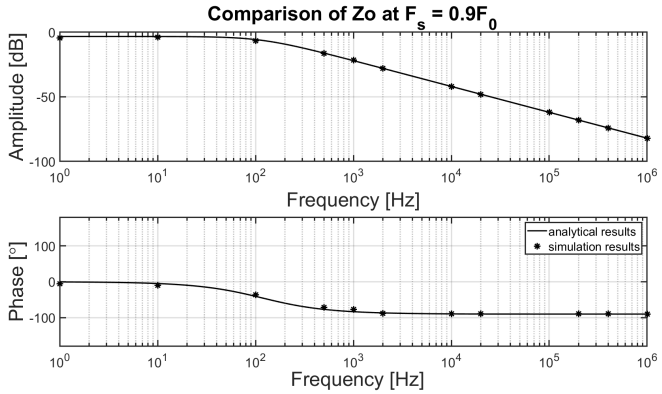
The main purpose of the simulation model is to verify the small-signal transfer function, especially for the small-signal output impedance Z_o of the LLC circuit. There are certain adjustments to the original simulation model established in Appendix A.1. To be specific, when conducting the research on the output impedance, the addition sinusoidal waveform current source with a certain frequency is implemented in the circuit to constitute the artificial ac disturbance $\hat{i}_o$ as shown in Appendix A.4.



(a)



(b)



(c)

Figure 3.15: Simulation verification of output impedance transfer functions for $F_s = 1.2F_o$, $F_s = F_o$ and $F_s = 0.9F_o$

Under the influence of this perturbance, the ac disturbance $\hat{v}_o$ is involved in the output voltage, and this ac signal can be collected by comparing with the ideal output voltage. The collected data of the ac signals $\hat{i}_o$ and $\hat{v}_o$ is processed by using the Fourier Analysis, and the result shows the output impedance at a certain frequency. Furthermore, by modifying the frequency of the ac current source, an array of small-signal output impedance values, coordinating with frequency, is calculated. These data can be drawn as a Bode Plot, and then compared with the Bode Plot of the analytical small-signal impedance.

Figure 3.15 shows the simulation verification of the control to the output voltage (output impedance) transfer function for three cases of $F_s = 1.2F_o$, $F_s = F_o$ and $F_s = 0.9F_o$. In all above three scenarios, simulation results match quite well with analytical results, but there are still some errors occurring between the analytical results and simulation results, especially at the high frequency.

3.2 Modelling of the PWM DC-DC Converter

3.2.1 State Space Averaging Method

In PWM dc-dc converters, with nonlinear and time-variant characteristics, the configuration of the power stage continuously changes with time and influences the switch condition. Moreover, there is a nonlinear relation between the input and output variables in the PWM process which serves as the switch drive signal generator. In order to analyze the dynamic characteristics of this nonlinear and time-varying system, there are three steps normally applied to the power stage as illustrated in Figure 3.16, including Averaging, Linearization and S-Domain Conversion. Eventually, a complete small-signal model for PWM converter can be established [11].

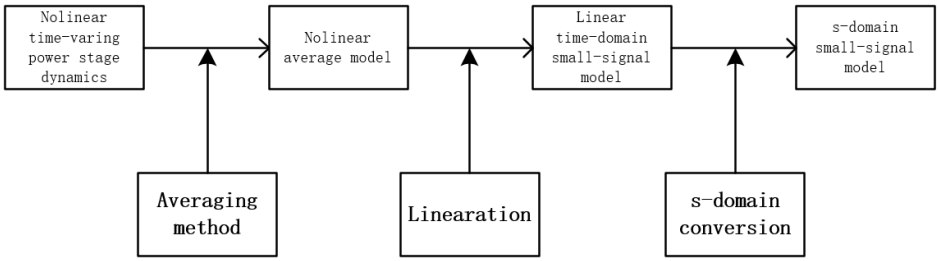


Figure 3.16: Flow chart of the small-signal modelling

The method of averaging is initially employed to the PWM dc-to-dc converter, which aims to remove the time-varying characteristic. The state space averaging, as one of the proper methods developed for PWM dc-to-dc converters, can form the state-space equation of the power stage. Thus, the time-averaged dynamics of the power stage can be concluded by the formed state-space equation.

In the approach of state-space averaging, combined with the switching function which consists of time-dependent variables, the power stage dynamics is initially described by a switched state-space model. Particularly, the power stage dynamics during the on-time period is described as

$$\begin{aligned} \frac{dx(t)}{dt} &= A_{on}x(t) + B_{on}v_{in}(t) \\ v_o(t) &= C_{on}x(t), \end{aligned} \tag{3.25}$$

where x is the state vector that contains independent state variables including the inductor current and capacitor voltage, v_{in} and v_o refer to the input voltage and output voltage separately, and the coefficient matrices include A_{on}, B_{on} and C_{on}. Likewise, the power stage dynamics of the off-time period can be express as

$$\begin{aligned} \frac{dx(t)}{dt} &= A_{off}x(t) + B_{off}v_{in}(t) \\ v_o(t) &= C_{off}x(t). \end{aligned} \tag{3.26}$$

By combining the two equations discussed above, it becomes

$$\begin{aligned} \frac{dx(t)}{dt} &= (q(t)A_{on} + (1-q(t))A_{off})x(t) \\ &\quad + (q(t)B_{on} + (1-q(t))B_{off})v_{in}(t) \\ v_o(t) &= (q(t)C_{on} + (1-q(t))C_{off})x(t). \end{aligned} \tag{3.27}$$

Equation (3.27) is known as the switched state-space model, and $q(t)$ that represents the switch function is expressed as

$$\begin{aligned} q(t) &= 1 \qquad 0 < t < dTs, \\ q(t) &= 0 \qquad dTs < t < Ts. \end{aligned} \tag{3.28}$$

Since the switch function $q(t)$ emerges the characteristic of time-variance, the averaging process is applied to the switching function

$$d(t) = \frac{1}{T_s}\int_{t-T_s}^{T_s} q(t)dt. \tag{3.29}$$

where $d(t)$ is known as the continuous duty ratio. Next, the average process is performed on (3.27), it becomes

$$\begin{aligned} \frac{d\overline{x}(t)}{dt} &= \overline{(q(t)A_{on} + (1-q(t))A_{off})x(t)} \\ &\quad + \overline{(q(t)B_{on} + (1-q(t))B_{off})v_{in}(t)} \\ \overline{v}_o(t) &= \overline{(q(t)C_{on} + (1-q(t))C_{off})x(t)}. \end{aligned} \tag{3.30}$$

Then, (3.30) is rearranged as

$$\begin{aligned} \frac{d\overline{x}(t)}{dt} &= (d(t)A_{on} + (1-d(t))A_{off})\overline{x}(t) \\ &\quad + (q(t)B_{on} + (1-d(t))B_{off})\overline{v}_{in}(t) \\ \overline{v}_o(t) &= (d(t)C_{on} + (1-d(t))C_{off})\overline{x}(t), \end{aligned} \tag{3.31}$$

which is known as the averaged state-space model. In order to apply this model to the PWM full-bridge dc-dc converter, the state vector x is defined as $[i_L V_s]^T$. Combined with the sub-circuit diagram of the full-bridge converter illustrated in Figure 2.9b, the averaged state-space model is derived as

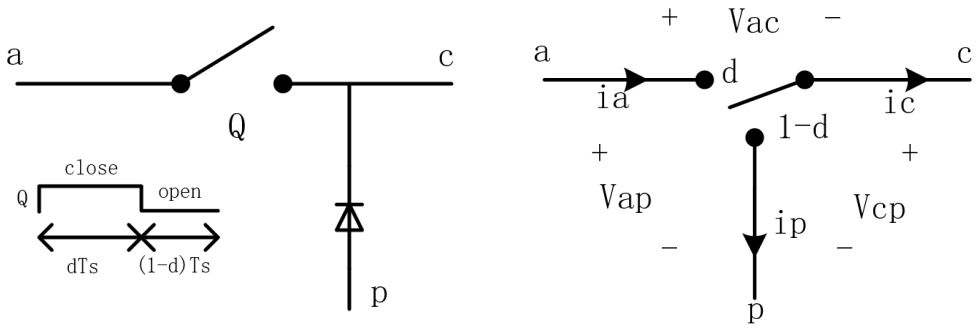
$$\begin{aligned}\frac{d\overline{x}(t)}{dt} &= (d(t)\begin{bmatrix}0 & -\frac{1}{L}\\ \frac{1}{C} & -\frac{1}{CR}\end{bmatrix} + (1-d(t))\begin{bmatrix}0 & -\frac{1}{L}\\ \frac{1}{C} & -\frac{1}{CR}\end{bmatrix})\overline{x}(t)\\ &\quad + (q(t)\begin{bmatrix}\frac{1}{nL}\\ 0\end{bmatrix} + (1-d(t))\begin{bmatrix}0\\ 0\end{bmatrix})\overline{v}_{in}(t)\\ \overline{v}_o(t) &= (d(t)\begin{bmatrix}0 & 1\end{bmatrix} + (1-d(t))\begin{bmatrix}0 & 1\end{bmatrix})\overline{x}(t),\end{aligned} \tag{3.32}$$

Likewise, in terms of the subcircuit of the boost converter in Figure 2.7b, the average state-space model is expressed as

$$\begin{aligned}\frac{d\overline{x}(t)}{dt} &= (d(t)\begin{bmatrix}0 & 0\\ 0 & -\frac{1}{CR}\end{bmatrix} + (1-d(t))\begin{bmatrix}0 & -\frac{1}{L}\\ \frac{1}{C} & -\frac{1}{CR}\end{bmatrix})\overline{x}(t)\\ &\quad + (q(t)\begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix} + (1-d(t))\begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix})\overline{v}_{in}(t)\\ \overline{v}_o(t) &= (d(t)\begin{bmatrix}0 & 1\end{bmatrix} + (1-d(t))\begin{bmatrix}0 & 1\end{bmatrix})\overline{x}(t).\end{aligned} \tag{3.33}$$

3.2.2 Circuit Averaging Method

The circuit averaging method uses the circuit variables with time-averaged behaviour to establish an average model of the power stage. In circuit averaging, the circuit variables are averaged directly and correlated with power stage component, and then the averaged circuit equation can be formed. An averaged circuit model can be developed to correspond with the equation and eventually replace the original circuit [11]. Specifically, the PWM switch as an individual circuit component in a buck converter shown in Figure 3.17a can be transferred to Figure 3.17b,



(a) **(b)**

Figure 3.17: (a).Switch operation under PWM principle (b).Circuit representation for PWM switch

and it is described as

$$\begin{aligned}V_{cp}(t) &= V_{ap}(t)q(t)\\ i_a(t) &= i_c(t)q(t),\end{aligned} \tag{3.34}$$

where $q(t)$ represents the switch function as referred before. By taking the local average, (3.34) is approximately derived as

$$\begin{aligned} \overline{v}_{cp}(t) &= \overline{v_{ap}(t)q(t)} \approx \overline{v}_{ap}(t)\overline{q}(t) \\ \bar{i}_a(t) &= \overline{i_c(t)q(t)} \approx \bar{i}_c(t)\overline{q}(t). \end{aligned} \tag{3.35}$$

The continuous duty ratio $d(t)$ is expressed as

$$d(t) = \frac{1}{T_s}\int_{t-T_s}^{T_s} q(t)dt. \tag{3.36}$$

Thus, (3.35) is rewritten as

$$\begin{aligned} \overline{v}_{cp}(t) &= \overline{v}_{ap}(t)d(t) \\ \bar{i}_a(t) &= \bar{i}_c(t)d(t). \end{aligned} \tag{3.37}$$

As shown in Figure 3.18a, the average equation above can be described as an averaged model which contains an ideal two-winding transformer with a turn ratio $d(t)$. For processing the small-signal model of the PWM switch, the ac components are taken into consideration. Therefore, (3.37) of the averaged PWM switch is further developed as

$$\begin{aligned} V_{cp} + \hat{v}_{cp}(t) &= (D + \hat{d}(t))(V_{ap} + \hat{v}_{ap}(t) \\ &= DV_{ap} + \hat{d}(t)V_{ap} + D\hat{v}_{ap}(t) + \hat{d}(t)\hat{v}_{ap}(t), \end{aligned} \tag{3.38}$$

$$\begin{aligned} I_a + \hat{i}_a(t) &= (D + \hat{d}(t))(I_c + \hat{i}_c(t) \\ &= DI_c + \hat{d}(t)I_c + D\hat{i}_c(t) + \hat{d}(t)\hat{i}_c(t), \end{aligned} \tag{3.39}$$

where the uppercase variables are dc component and variables with up script are ac small-signal components. By extracting the ac components in (3.35) and (3.37), the small-signal equation is described as

$$\begin{aligned} \hat{v}_{cp}(t) &= V_{ap}\hat{d}(t) + D\hat{v}_{ap}(t) \\ \hat{i}_a(t) &= I_c\hat{d}(t) + D\hat{i}_c(t), \end{aligned} \tag{3.40}$$

where the dc and ac components are linearly combined to express the left-side ac components. The equations above represent the small-signal model of the PWM switch and can be expressed as the equivalent circuit as shown in Figure 3.18b, where the linear time-invariant characteristic is formed.

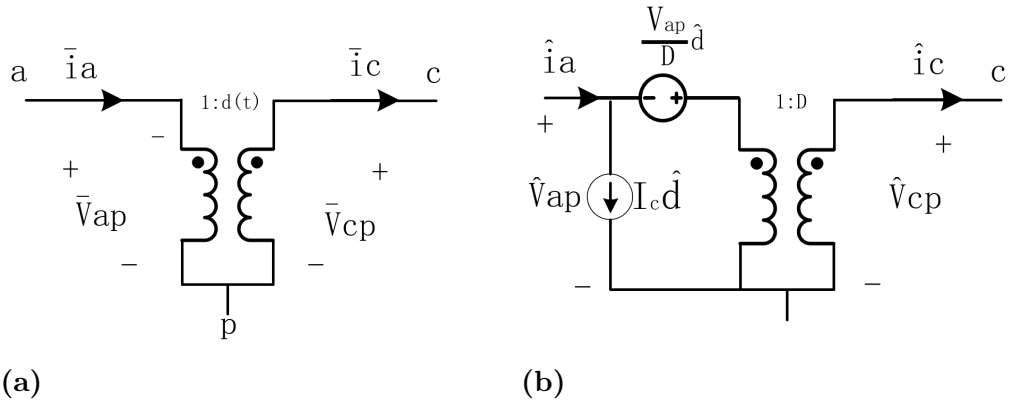


Figure 3.18: (a).Average model of the PWM switch (b).Small-signal model of the PWM switch

When applying this small-signal model of the PWM switch to the buck converter and employing small-signal source $\hat{v}_s$ as the input signal, the complete time-domain small-signal model is established as shown in Figure 3.19.

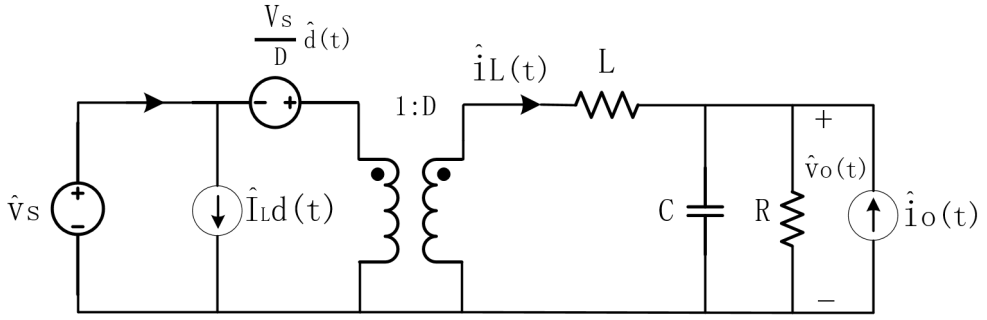


Figure 3.19: Average model of PWM buck converter

Then, by applying the Laplace Transform to this time-domain small-signal model, the s-domain small-signal model is derived and illustrated in Figure 3.20.

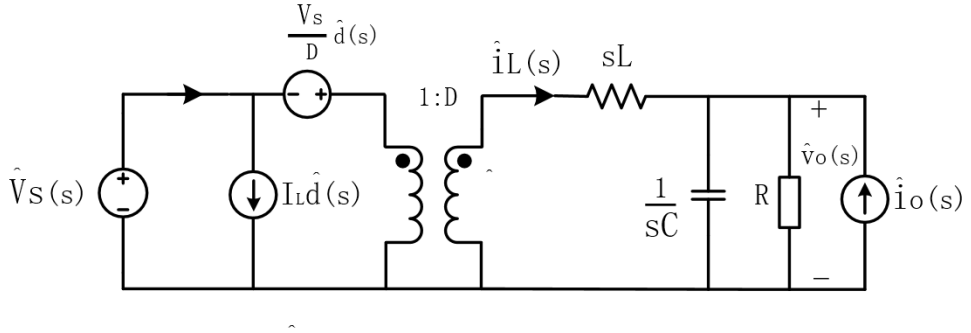


Figure 3.20: Small-signal model of PWM buck converter

Furthermore, by considering the dc-dc converters implemented in this thesis work, the isolated full-bridge dc-dc buck converter is simplified to the combination of

original buck converters and a transformer. Therefore, the s-domain small-signal of the isolated full-bridge buck converter is established in Figure 3.21, where the equivalent series resistance R_l and R_c are involved. Its application provides the foundation for deriving the small-signal transfer function in next section.

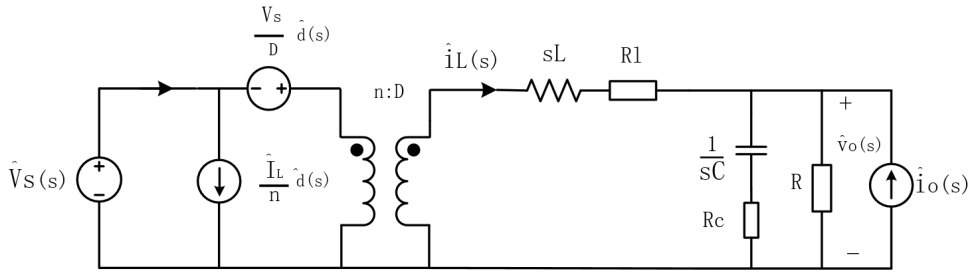


Figure 3.21: Small-signal model of PWM isolated full-bridge dc-dc buck converter

As same as the process illustrated above, with the condition $V_{ap} = -V_o$ and $I_c = -I_L$, the small-signal equation for the PWM process of the boost converter is expressed as

$$\begin{aligned} \hat{v}_{cp}(t) &= V_{ap}\hat{d}(t) + D\hat{v}_{ap}(t) = -V_o\hat{d}(t) + D\hat{v}_{ap}(t) \\ \hat{i}_a(t) &= I_c\hat{d}(t) + D\hat{i}_c(t) = -I_L\hat{d}(t) + D\hat{i}_c(t). \end{aligned} \tag{3.41}$$

Therefore, by modifying the direction of relevant voltages or currents, the s-domain model of the boost converter is shown in Figure 3.22. In order to facilitate the further analysis, the small-signal model is refined as shown in Figure 3.23.

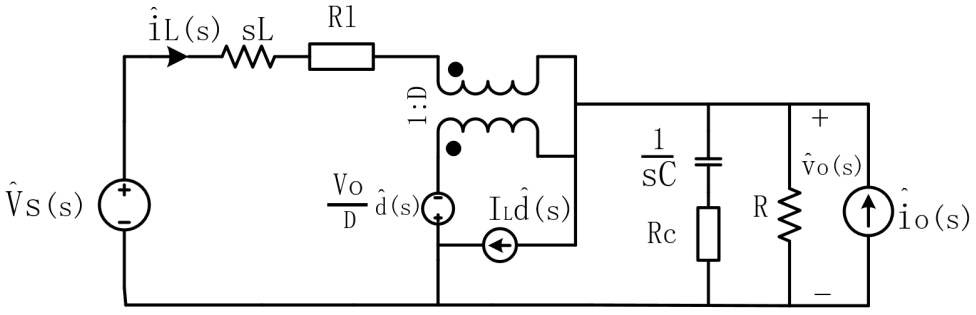


Figure 3.22: Small-signal model of PWM boost converter

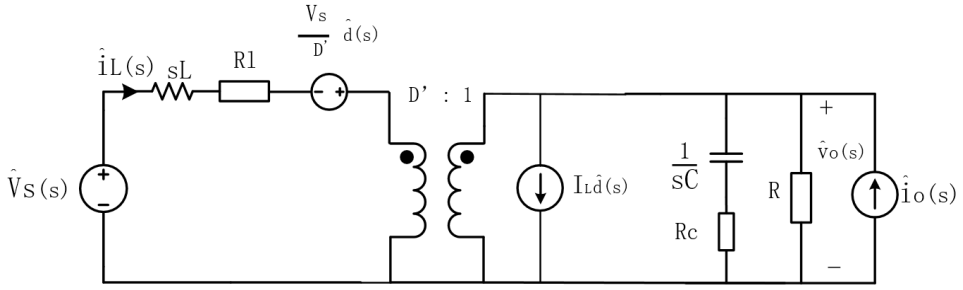


Figure 3.23: Refined small-signal model of PWM boost converter

3.2.3 Power Stage Transfer Function Expressions

The power stage transfer function of PWM converters, as the essential part for analysing the interaction for converters, can be derived by the s-domain small-signal model. For instance, in Figure 3.21, with the series equivalent resistance considered in the full-bridge buck converter, with the condition $\hat{d}(s) = \hat{i}_o(s) = 0$, the input-to-output transfer function is yield as

$$G_{vs} = \frac{\hat{v}_o(s)}{\hat{v}_s(s)} = K_{vs}\frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}, \tag{3.42}$$

and parameters are defined as

$$\begin{aligned} \omega_o &= \sqrt{\frac{1}{LC}\frac{R+R_l}{R+R_c}} \approx \frac{1}{\sqrt{LC}} \\ K_{vs} &= \frac{D}{1+\frac{R_l}{R}} \approx D \quad \omega_{esr} = \frac{1}{CR_c} \\ Q &= \frac{1}{\omega_o}\frac{R+R_l}{L+C(R_lR_c+R_lR+R_cR)} \approx R\sqrt{\frac{C}{L}}, \end{aligned} \tag{3.43}$$

where ω_{esr} is the esr zero frequency originating from the series equivalent resistance, ω_o is the doule pole frequency, and Q is the damping ratio. Likewise, with the condition $\hat{v}_s(s) = \hat{i}_o(s) = 0$, the duty ratio to output transfer function is derived as

$$\begin{aligned} G_{vd} &= \frac{\hat{v}_o(s)}{\hat{d}(s)} = K_{vd}\frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \\ K_{vd} &= \frac{V_s}{1+\frac{R_l}{R}} \approx V_s. \end{aligned} \tag{3.44}$$

The load current-to-output transfer function is yielded as

$$\begin{aligned} Z_{out} &= \frac{\hat{v}_o(s)}{\hat{i}_o(s)} = R \parallel R_l\frac{(1+\frac{s}{\omega_z})(1+\frac{s}{\omega_{esr}})}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \\ \omega_z &= \frac{R_l}{L}, \end{aligned} \tag{3.45}$$

with the condition $\hat{v_s}(s) = \hat{d}(s) = 0$. In (3.45), another zero frequency ω_z occurs which originates from the esr of inductor. The three transfer functions above are derived from the PWM dc-dc buck converter. Moreover, the transfer functions for another PWM dc-dc converter, the boost converter implemented in the 5G power system, also needs to be formulated in the same way. The input-to-output transfer function for the boost converter is yielded from Figure 3.23,

$$\begin{aligned} G_{vs} &= \frac{\hat{v_o}(s)}{\hat{v_s}(s)} = K_{vs}\frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \\ K_{vs} &= \frac{1}{(D')(1+\frac{R_l}{RD'})} \approx \frac{1}{D'} \quad \omega_{esr} = \frac{1}{CR_c} \quad D' = 1-D \\ \omega_o &= \sqrt{\frac{1}{LC}\frac{RD^{12}+R_l}{R+R_c}} \approx \frac{D'}{\sqrt{LC}} \\ Q &= \frac{1}{\omega_o}\frac{RD'^2+R_l}{L+C(R_lR_c+R_lR+R_cRD'^2)} \approx RD'\sqrt{\frac{C}{L}}. \end{aligned} \tag{3.46}$$

The duty ratio-to-output transfer function for the boost converter is derived as

$$\begin{aligned} G_{vd} &= \frac{\hat{v_o}(s)}{\hat{d}(s)} = K_{vd}\frac{(1-\frac{s}{\omega_{rhp}})(1+\frac{s}{\omega_{esr}})}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \\ K_{vd} &= \frac{V_s}{D'}\frac{1-\frac{R_l}{RD'^2}}{1+\frac{R_l}{RD'^2}} \approx \frac{V_s}{D'^2} \\ \omega_{rhp} &= \frac{D'^2R}{L}(1-\frac{R_l}{RD'^2}) \approx \frac{D'^2R}{L}, \end{aligned} \tag{3.47}$$

where ω_{rhp} is the particular term in the transfer function of the boost converter, and known as the right-half plane(RHP) zero. This single zero emerges in the right-hand side of s-plane and moves around in terms of the duty ratio. The load current to output transfer function is formulated as

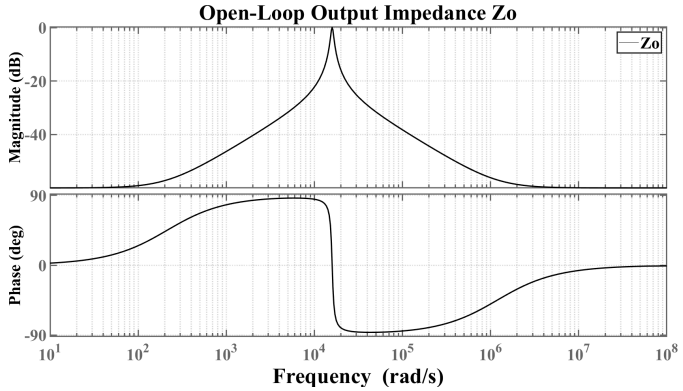
$$\begin{aligned} Z_o &= \frac{\hat{v_o}(s)}{\hat{i_o}(s)} = K_p\frac{(1+\frac{s}{\omega_z})(1+\frac{s}{\omega_{esr}})}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \\ \omega_z &= \frac{R_l}{L} \quad K_p = R \parallel \frac{R_l}{D'^2} \approx \frac{R_l}{D'^2}. \end{aligned} \tag{3.48}$$

Except the three main transfer functions of PWM dc-dc converters, there are also some other equations that will be utilized to evaluate the transfer functions for closed-loop PWM dc-dc converters. In Table 3.3, the input-to-inductor current G_{is}, duty ratio-to-inductor current G_{id}, load current-to-inductor current Z_q are included [11].

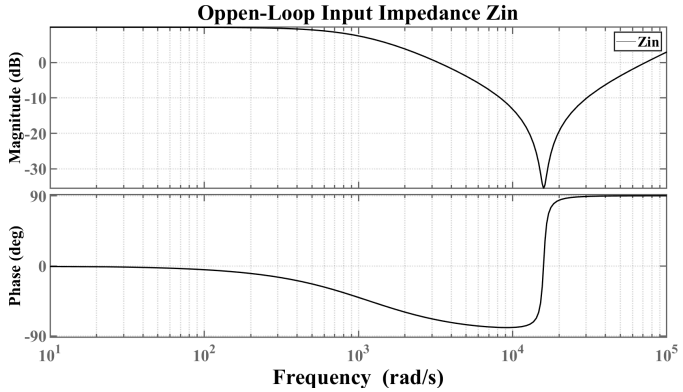
Table 3.3: Open-loop transfer functions of PWM converters

Transfer Function		
$G_{is} = \frac{\hat{i}_L}{\hat{v}_s} = K_{is}\frac{1+\frac{s}{\omega_{is}}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}$	$G_{id} = \frac{\hat{i}_L}{\hat{d}} = K_{id}\frac{1+\frac{s}{\omega_{id}}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}$	$Z_q = \frac{\hat{i}_L}{\hat{i}_o} = K_q\frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}$
Parameter	Full-Bridge Buck Converter	Boost Converter
K_{is}	D/R/n	$1/(1\text{-D})^2/R$
K_{id}	$V_s/R/n$	$2V_s/(1-D)^3/R$
K_q	-1	-1/(1-D)
ω_{is}	1/(CR)	1/(CR)
ω_{id}	1/(CR)	2/(CR)

3.2.4 Bode Plot Representations and Physical Meanings of Power Stage Transfer Functions



(a)



(b)

Figure 3.24: (a).Open-loop output impedance bode plot of the PWM full-bridge buck converter (b).Open-loop input impedance bode plot of the PWM full-bridge buck converter

Figure 3.24a diagrams the Bode plot of the output impedance of the PWM full-bridge dc-dc converter. It can be seen that the output impedance has the following

characteristics: The amplitude of the output impedance is constant at low and high frequency; the impedance initially increases to the maximum value at the LC resonant frequency ω_o, and then gradually decreases. These amplitude-frequency characteristics reveal that the output impedance has different suppression capabilities for load disturbances at different frequencies. When $\omega < \omega_o$, this suppression capability becomes worse with the increase of frequency. In contrast, this capability grows better with the increasing frequency when $\omega > \omega_o$.

Meanwhile, Figure 3.25a illustrates the equivalent circuit of the output impedance, which is reconstructed from Figure 3.21 with the condition of $\hat{v_s}(s) = \hat{d}(s) = 0$. This equivalent circuit model consists of three branches, the inductor, capacitor and resistor in parallel, which apparently has the characteristics of a typical RLC resonant circuit. When $f \to 0$, the output impedance is derived as

$$Z_o = (j\omega L + R_l) \parallel (\frac{1}{j\omega C} + R_c) \parallel R \approx R_l \parallel R \approx R_l, \tag{3.49}$$

which reveals that the output impedance is dominated by the R_l of the inductor at low frequency. In contrast, when $f \to \infty$, it becomes

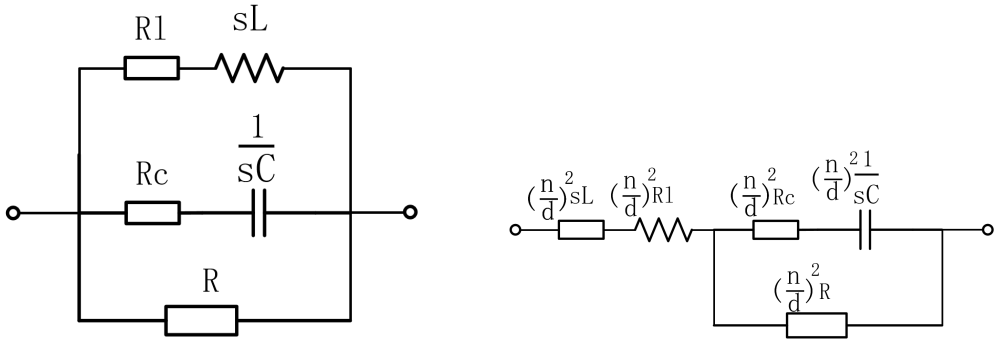
$$Z_o = (j\omega L + R_l) \parallel (\frac{1}{j\omega C} + R_c) \parallel R \approx R_c \parallel R \approx R_c \tag{3.50}$$

where the output impedance performs the property of the R_{lc} of the capacitor. When it approaches the parallel resonant frequency $f = \frac{1}{\sqrt{LC}} Hz$, the output impedance is reformulated as

$$\begin{aligned} Z_o &= (j\omega L + R_l) \parallel (\frac{1}{j\omega C} + R_c) \parallel R \\ &\approx j\omega L \parallel \frac{1}{j\omega C} \parallel R \\ &\approx \infty \parallel R \approx R \end{aligned} \tag{3.51}$$

where branches including the capacitor and inductor offset each other and only output resistor R remains. Therefore, by comparing this equivalent circuit model with the bode plot representation, it is concluded that the performance of the output impedance equivalent circuit along the frequency domain behaves in the same way as the Bode plot.

Figure 3.24b illustrates the bode plot representing the small-signal transfer function of the input impedance in PWM full-bridge dc-dc buck converters. The input impedance has the following characteristics: the amplitude is constant at low frequency and slightly drops at a certain frequency, and then linearly increases.



(a) **(b)**

Figure 3.25: (a).Equivalent circuit of the open-loop output impedance for PWM full-bridge buck converter (b).Equivalent circuit of the open-loop input impedance for PWM full-bridge buck converter

As same as the analysis of the output impedance, in general, the input impedance has a better load ability at the low frequency compared to the situation at a higher frequency. The equivalent circuit for the input impedance derived from Figure 3.21 is shown in Figure 3.25b by noting that the R_{esr} is considered, where a capacitor and a resistor connected in parallel and then in series with an inductor. When $f \to 0$, the input impedance is derived as

$$\begin{aligned} Z_{in} &= (\frac{n}{d})^2\{(j\omega L + R_l) + [(\frac{1}{j\omega C} + R_c) \parallel R]\} \\ &\approx (\frac{n}{d})^2(R_l + R) \approx (\frac{n}{d})^2 R, \end{aligned} \tag{3.52}$$

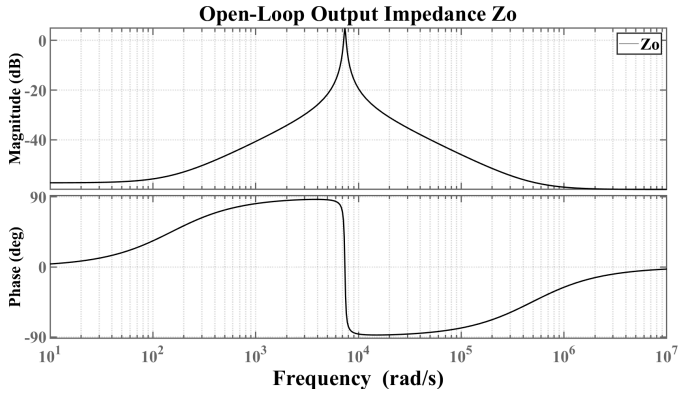
where the resistor R dominates the input impedance at the low frequency. On the contrary, when $f \to \infty$, it becomes,

$$\begin{aligned} Z_{in} &= (\frac{n}{d})^2\{(j\omega L + R_l) + [(\frac{1}{j\omega C} + R_c) \parallel R]\} \\ &\approx (\frac{n}{d})^2(j\omega L + R_c) \approx j(\frac{n}{d})^2 \omega L, \end{aligned} \tag{3.53}$$

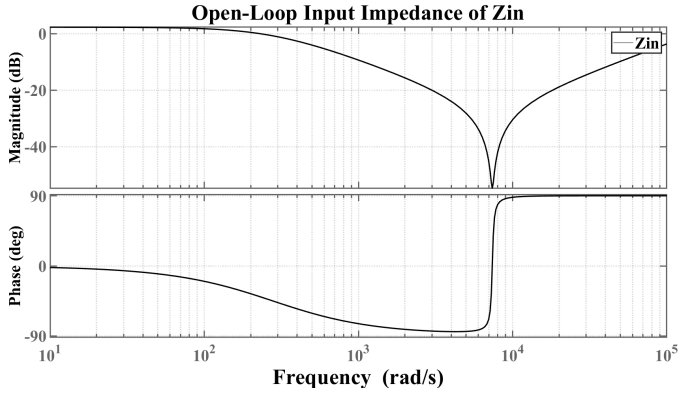
where the impedance is characteristic with the inductive property at the high frequency. When it approaches the parallel resonant frequency $f = \frac{1}{\sqrt{LC}} Hz$, the input impedance is rearranged as

$$\begin{aligned} Z_{in} &= (\frac{n}{d})^2\{(j\omega L + R_l) + [(\frac{1}{j\omega C} + R_c) \parallel R]\} \\ &\approx (\frac{n}{d})^2(j\omega L + \frac{1}{j\omega C} \parallel R) \\ &= (\frac{n}{d})^2 \frac{\frac{j\omega L}{R}}{\frac{1}{R} + j\omega C}, \end{aligned} \tag{3.54}$$

where the value is approximately identical to the amplitude at the same frequency in the Bode Plot.

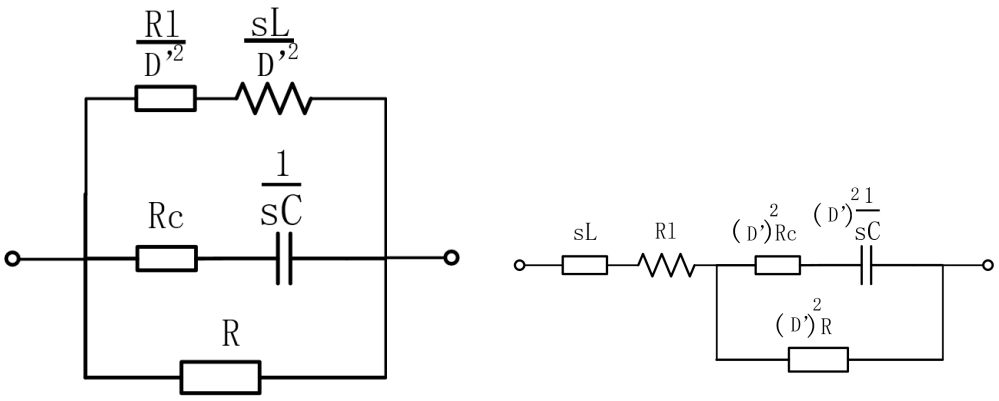


(a)



(b)

Figure 3.26: (a).Open-loop output impedance bode plot of the PWM boost converter (b).Open-loop input impedance bode plot of the PWM boost converter



(a) **(b)**

Figure 3.27: (a).Equivalent circuit of the open-loop output impedance for boost converter (b).Equivalent circuit of the open-loop input impedance for boost converter

Similarly, the dynamic analysis is processed on the PWM boost converter. Figure

3.26 shows the Bode plots of the small-signal input and output impedance transfer functions respectively. In these two diagrams, the dynamics of the input and output impedance has the same performance as the full-bridge buck converter's. Figure 3.27 shows the equivalent circuit of the input and output impedance, where the resonant frequency f_0 is defined as $D'\frac{1}{\sqrt{LC}}$ and D' is the duty ratio of the off-time period. Table 3.4 shows the calculated input and output impedance amplitudes at three different conditions as aforesaid, which are corresponding with their Bode plots.

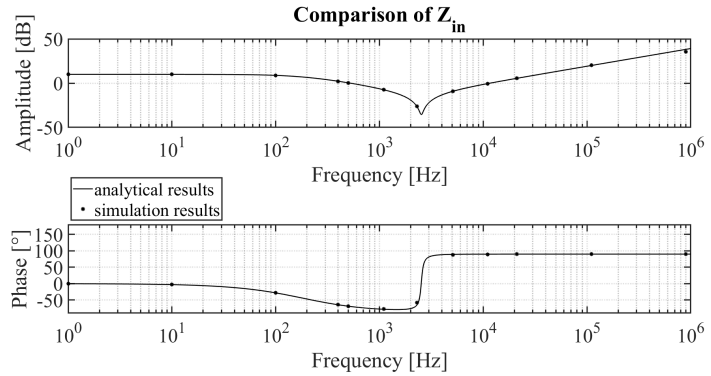
Table 3.4: Calculated input and output impedance of boost converters

	$f \to 0$	$f = D'\frac{1}{\sqrt{LC}}$	$f \to \infty$
$\lvert Z_o \rvert$	$\frac{R_l}{D'^2}$	R_c	R
$\lvert Z_{in} \rvert$	$D'^2 R$	ωL	$\lvert \frac{\frac{j\omega L}{R} - (1-D'^2)}{\frac{1}{R} + j\omega C} \rvert$

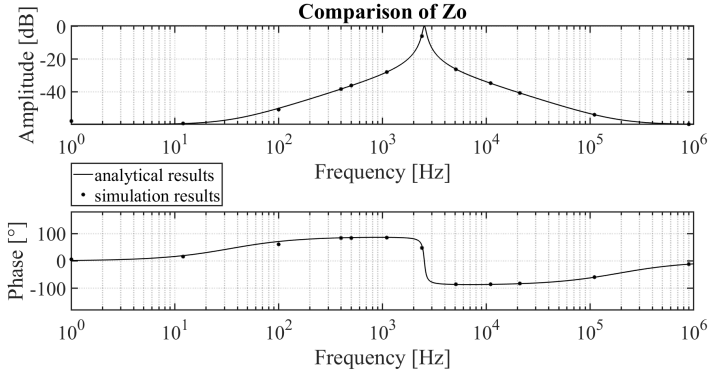
In general, the Bode plot representations and the physical meanings of the input and output impedance verify each other. Meanwhile, the amplitudes of the output and input impedance reflect the anti-interference ability and load ability of the open-loop system. The power stage transfer functions analysis in this section will establish a solid foundation on the closed-loop transfers function analysis.

3.2.5 Analytical Transfer Functions Verification

Figure 3.28 and Figure 3.29 illustrate the Bode plot comparison of simulation results and analytical transfer functions for the two PWM converters respectively, where the solid line represents the analytical results, and the scattered points are originated from the simulation model. As can been seen, most of the scattered dots are overlapped with the analytical transfer function bode plots except some unexpected errors existing somewhere. Therefore, it is concluded that the analytical transfer function and simulation model are verified with each other.

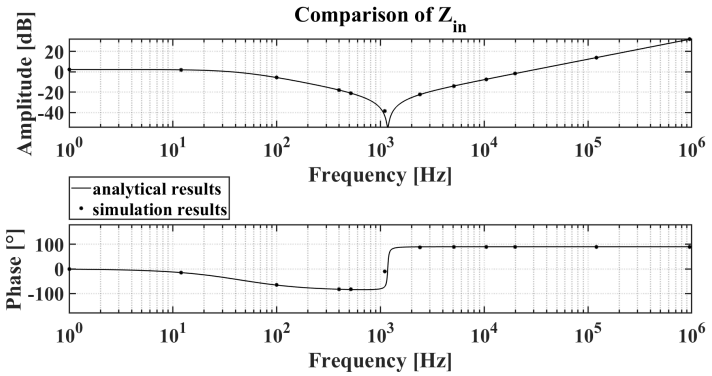


(a)

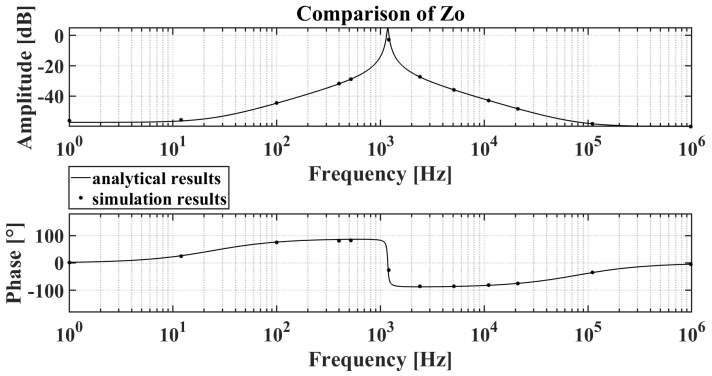


(b)

Figure 3.28: (a).Comparison of the open-loop input impedance for PWM full-bridge buck converter (b).Comparison of the open-loop output impedance for PWM full-bridge buck converter



(a)



(b)

Figure 3.29: (a).Comparison of the open-loop input impedance for PWM boost converter (b).Comparison of the open-loop output impedance for PWM boost converter

4

Closed-Loop Small-Signal Modelling

4.1 Modelling of Voltage Mode Controlled LLC Resonant Converter

4.1.1 Principle of Voltage Mode Control

The voltage mode (VM) control that uses the output voltage as the only feedback signal has been widely applied in power electronic converters [11]. In the LLC resonant circuit, this control scheme is implemented. The method of asymptotic analysis is introduced when designing the voltage feedback loop of the LLC resonant circuit.

Firstly, it can be seen from the properties of the LLC resonant circuit that the phase angle at the DC side is 180 degree rather than 0 degree under the situation of a PWM converter. From the perspective of the (VM) control, it means that the LLC circuit acts as an inverter. Therefore, the output voltage will drop when the control voltage increase. Owing to working under zero voltage switch condition, the output voltage is about to have a turn-down as the switching frequency increases. From the perspective of the voltage-controlled mode, the increase of its input voltage results in a boost of the frequency. On the contrary, the voltage-controlled compensator of the PWM converter displays an alternative pattern. As the control voltage increases, the duty cycle increases, thus increasing the output voltage. As a result of this characteristic, the compensator of the PWM converter has a negative feedback while a positive compensator is equipped with the LLC resonant converter as Figure 4.1 shows.

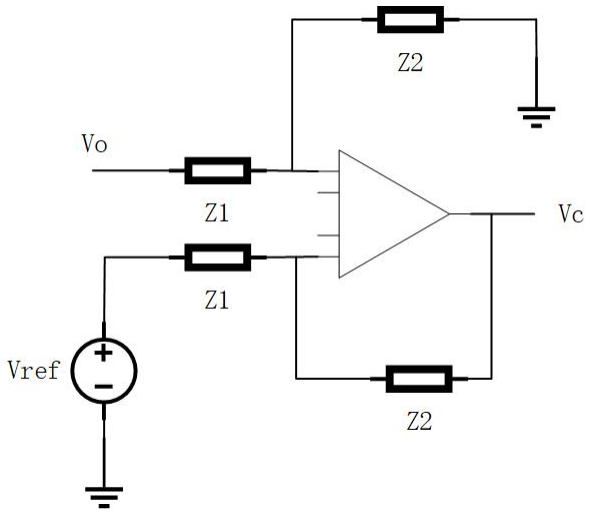


Figure 4.1: Compensator structures of LLC resonant converter

Figure 4.2 shows the block diagram representation of the voltage mode controlled LLC resonant converter, where F_v is the feedback compensator and F_m is the voltage-to-frequency modulator. The expected structure of the voltage feedback compensation is determined as

$$\begin{aligned} F_v(s) &= \frac{Z_2(s)}{Z_1(s)} = \frac{K_v}{s}\frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \\ K_v &= \frac{1}{R_1(C_2+C_3)} \\ \omega_{z1} &= \frac{1}{R_3C_2} \\ \omega_{z2} &= \frac{1}{(R_1+R_2)C_1} \\ \omega_{p1} &= \frac{1}{R_1C_1} \\ \omega_{p2} &= \frac{1}{R_3\frac{C_2C_3}{C_2+C_3}}. \end{aligned} \tag{4.1}$$

Due to neglecting the esr of the inductance and capacitance, ω_{p1} and ω_{p2} are both completely ignored.

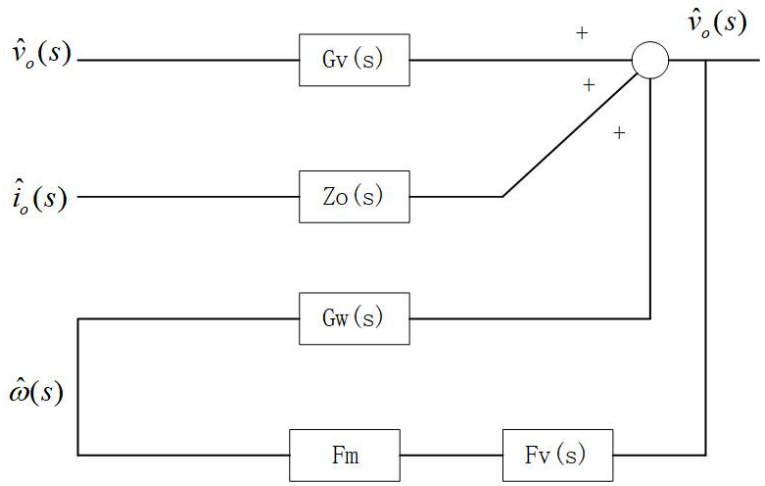


Figure 4.2: Small-signal block diagram of the LLC resonant converter

4.1.2 Closed-Loop Transfer Function Expressions

According to the block diagram in Figure 4.2, the voltage loop gain T is expressed as

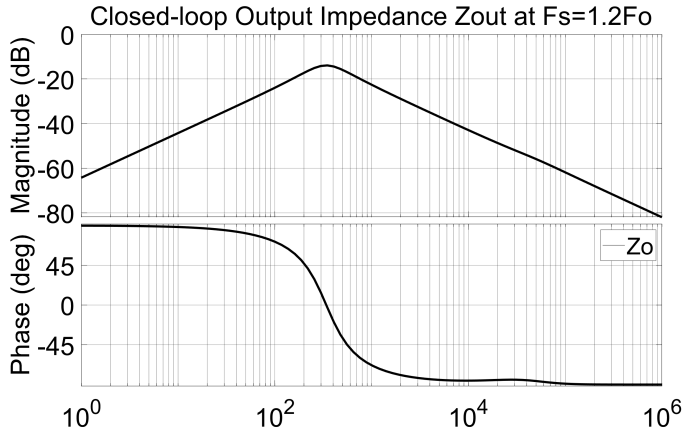
$$T_v(s) = \frac{\hat{v_o}(s)}{\hat{d}(s)} \frac{\hat{v_{con}}(s)}{\hat{v_o}(s)} \frac{\hat{d}(s)}{\hat{v_{con}}(s)} = G_{vd}(s)F_v(s). \tag{4.2}$$

The closed loop of the transfer functions including the control-to-output, input-to-output voltage and Z_{out} are identified as

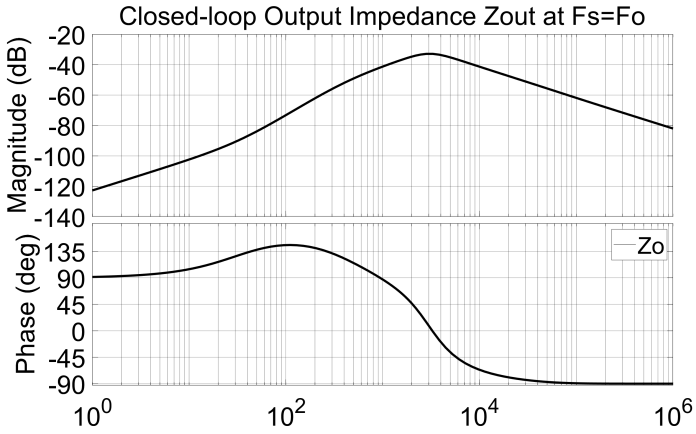
$$\begin{aligned} Aw &= \frac{Gw}{1+Tm} \\ Av &= \frac{Gv}{1+Tm} \\ Zout &= \frac{Zo}{1+Tm}. \end{aligned} \tag{4.3}$$

4.1.3 Bode Plot Representations and Physical Meanings of Closed-Loop Transfer Functions

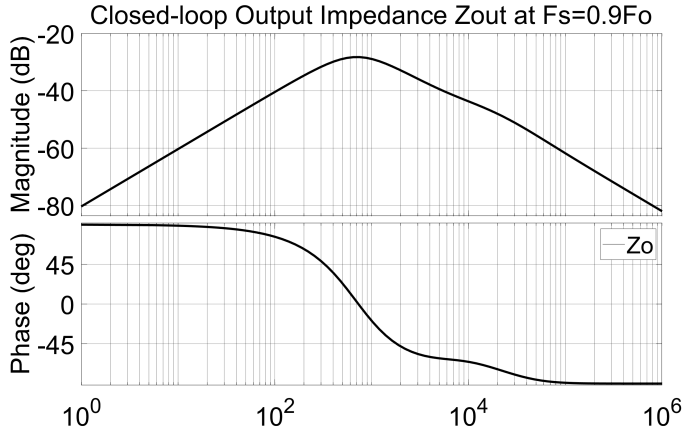
Figure 4.3 shows the Bode plot of the closed-loop output impedance for the LLC resonant converter.



(a)



(b)

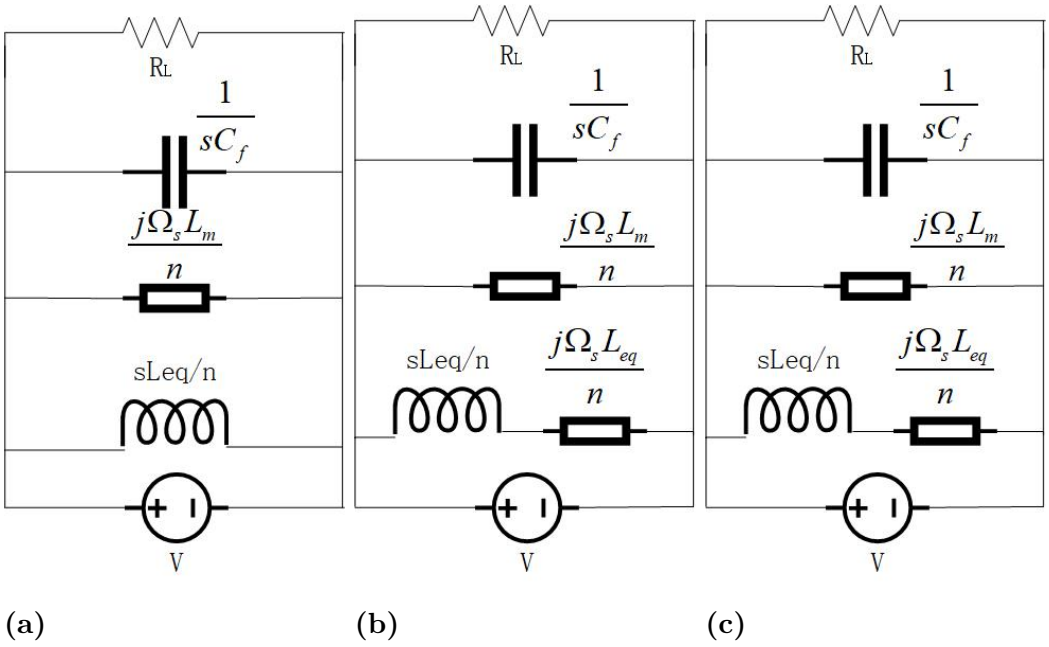


(c)

Figure 4.3: Analytic results of the closed-loop output impedance for three cases of $F_s = 1.2F_o$, $F_s = F_o$ and $F_s = 0.9F_o$

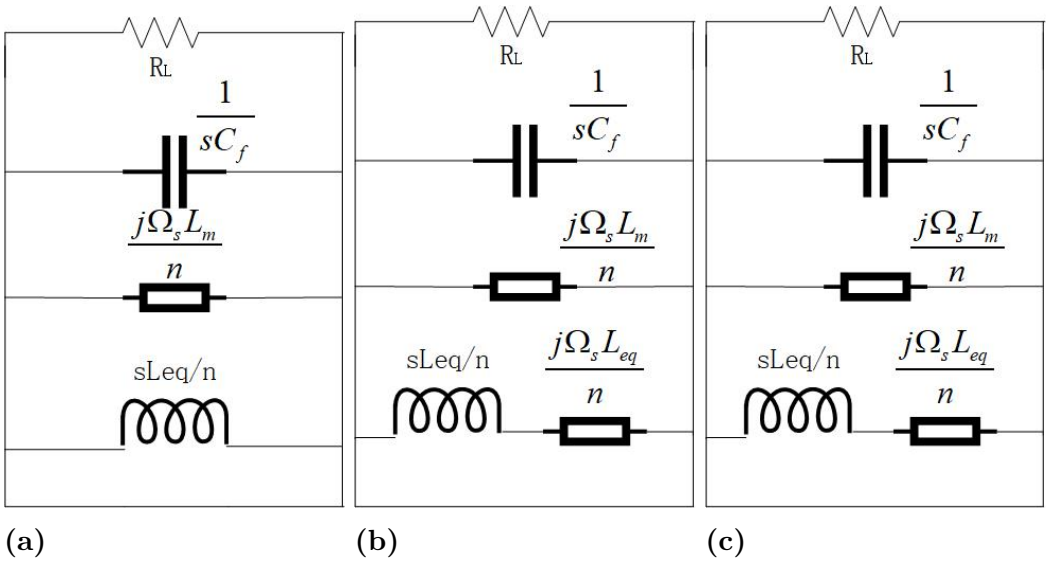
At the area of low frequency, in Figure 4.3, the voltage loop can be replaced with a voltage source in the output impedance equivalent circuit shown in Figure 4.4. Therefore, the equivalent circuit of the output impedance at the low frequency is refined in Figure 4.5, where the voltage source is short-circuit based on the Thevenin's

Theorem. In contrast to this, the voltage source is open-circuit, when the frequency reaches the high area, which causes the closed-loop output impedance to follow the open-loop output impedance.



(a) **(b)** **(c)**

Figure 4.4: Equivalent circuit of closed-loop output impedance at $F_s = F_o$, $F_s \geq F_o$ and $F_s < F_o$



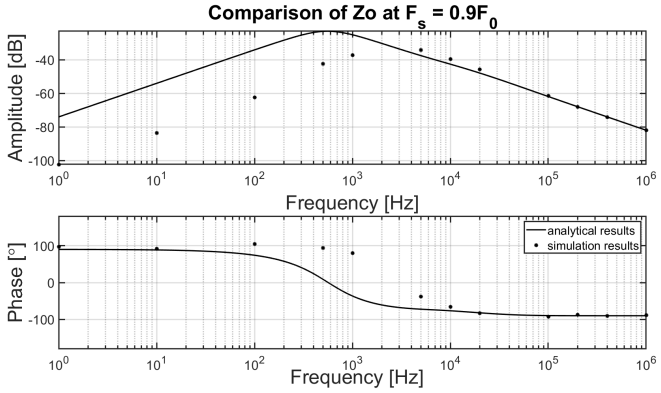
(a) **(b)** **(c)**

Figure 4.5: Refined equivalent circuit of closed-loop output impedance at $F_s = F_o$, $F_s \geq F_o$ and $F_s < F_o$ at low frequencies

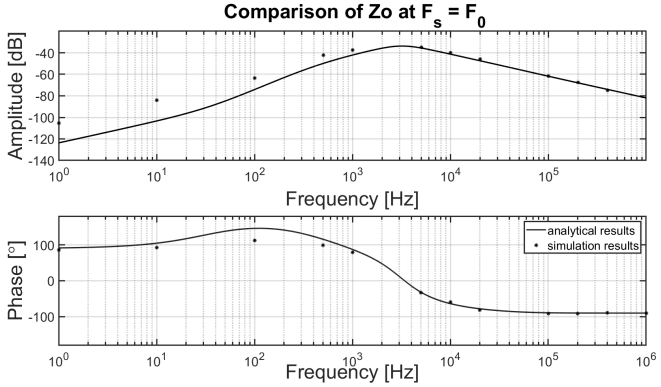
4.1.4 Analytical Transfer Functions Verification

In this section, the comparisons between analytical results and simulation results for the closed-loop output impedance are diagrammed in terms of three operating

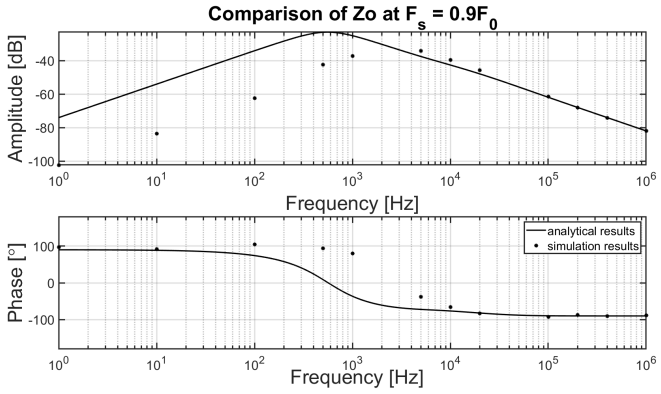
conditions of $F_s = 1.2F_o$, $F_s = F_o$ and $F_s = 0.9F_o$. By applying the same method as mentioned in Section 3.1.5 and combining with the modelling theory of the VM control, simulation models are constructed in Appendix A.7. Figure 4.6 illustrates bode plot comparisons of simulation results and analytical transfer functions for the closed-loop output impedance, where the solid line represents the analytical results, and scattered points originate from the simulation model.



(a)



(b)

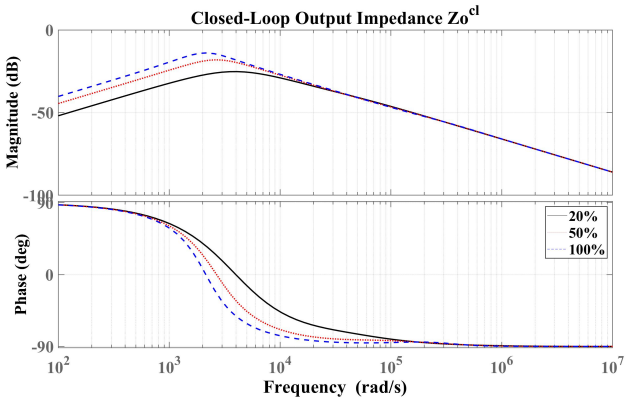


(c)

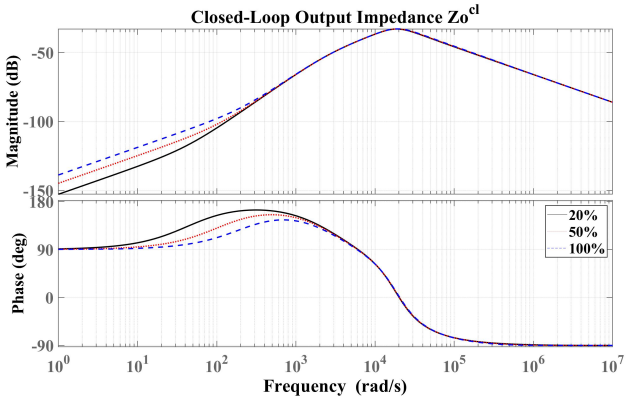
Figure 4.6: Comparison of the closed-loop output impedance for three cases of $F_s = 1.2F_o$, $F_s = F_o$ and $F_s = 0.9F_o$

4.1.5 Boundary Condition Analysis

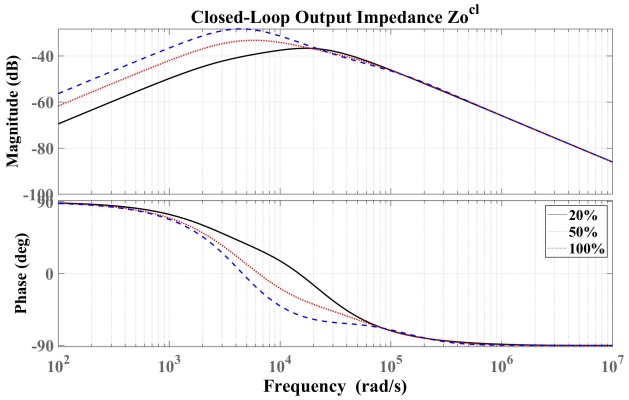
This section investigates the properties of the output impedance for the LLC resonant converter under various ranges of loads. Under the rated voltage level, Figure 4.7 shows bode plots of the closed-loop output impedance when the circuit performs with the full-load P_o, the half-load 50%P_o and light-load 20%P_o.



(a)



(b)



(c)

Figure 4.7: Closed-loop output impedance under the condition of 100%, 50%,20% P_o for three cases of $F_s = 1.2F_o$, $F_s = F_o$ and $F_s = 0.9F_o$

It is concluded from Figure 4.7 that different loads have effects on the LLC resonant

converter in the low-frequency area, since Z_o at the output side depends on the R_L, which can be expressed as

$$R_L = \frac{{V_o}^2}{P_o}. \tag{4.4}$$

With the drop of the output power P_o, the output resistance increases which induces the raise of Z_o. This phenomenon can be explained by (4.3), where Z_o at low frequencies has a positive correlation with output resistance R_L.

4.2 Modelling of Peak Current Mode Controlled PWM DC-DC converter

4.2.1 Principle of Peak Current Mode Control

In the 5G power system, current mode control is employed in some topologies of PWM dc-dc converters. Current control mode refers to that both output voltage and inductor current signals are involved as the feedback signal to generate the PWM switch drive signal for PWM dc-to-dc converters. There are various ways to implement the current mode control in terms of a current sensing method or sensed current usage. Peak current mode (PCM) control, regarded as the most popular method, applies the peak value of the inductor current as control variables. These control variables are combined with control references derived from the voltage feedback circuit to form the PWM switch drive signal [11].

Figure 4.8 illustrates the schematic of the isolated full-bridge dc-dc buck converter with the PCM control, where the PWM generator is formed by the ramp signal V_I and the control signal V_{con}. Specifically, at the beginning of each working period, the switch is turned on and then turned off when the signal V_I climbs up to the signal V_{con}. The voltage compensator consisting of impedances Z_1, Z_2 and an amplifier are implemented to regulate the output voltage to a reference value V_{ref}, and the output signal V_{con} from the compensator is synchronously modified to produce the necessary duty ratio for regulating the output voltage.

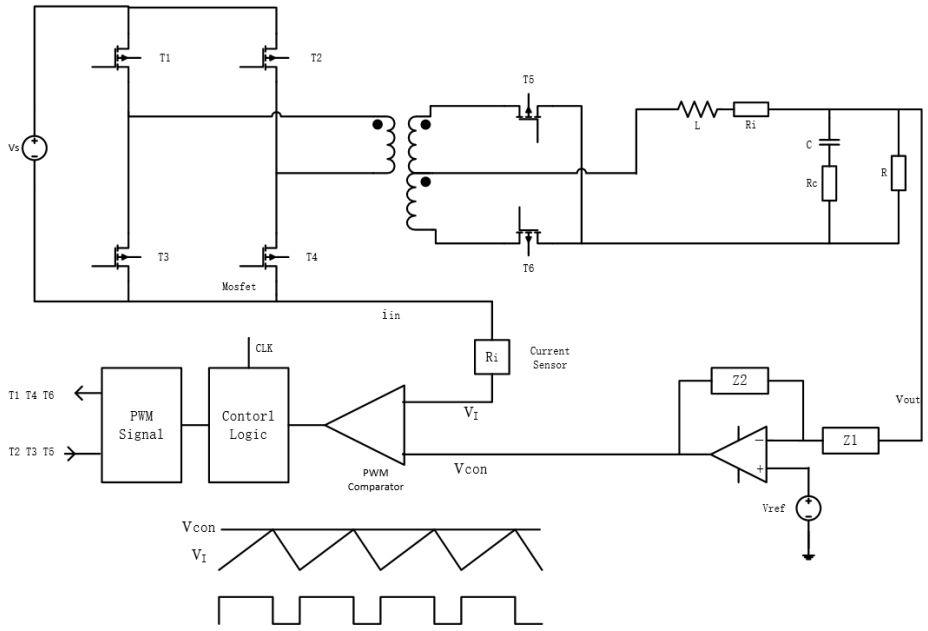


Figure 4.8: Control scheme and waveform of peak current mdoel control

In order to generate the PWM waveform, a time-varying piecewise linear waveform is required. Specifically, the triangular waveform, as one of the aforementioned waveforms, can be applied to the PWM process. In all PWM converters, the inductor current that increases and then decreases regularly in the power stage can be regarded as a prepared triangular waveform. In PCM control, this current is sensed by the current sensing network (CSN) and transformed to the voltage signal V_1 as shown in Figure 4.8, which mainly aims to avoid the overcurrent condition and reduce the Ohmic losses. The sensed voltage signal is then compared with the control signal V_{con} to generate the PWM waveform.

However, the peak current mode control has one critical problem when the duty ratio is above 0.5. As shown in Figure 4.9, the solid line V_I and dash line V_I' represents the original sensed voltage signal and the perturbed sensed voltage signal respectively. The error between V_I and V_I' converges gradually and eventually vanishes when the duty ratio is smaller than 0.5, whereas this error diverges regularly on the basis of the double operating period $2T_s$ when the duty ratio is larger than 0.5. Since the nonlinear oscillation caused by the error occurs at the half of the switching frequency $1/2f_s$, this problem is called the sub-harmonic oscillation [11].

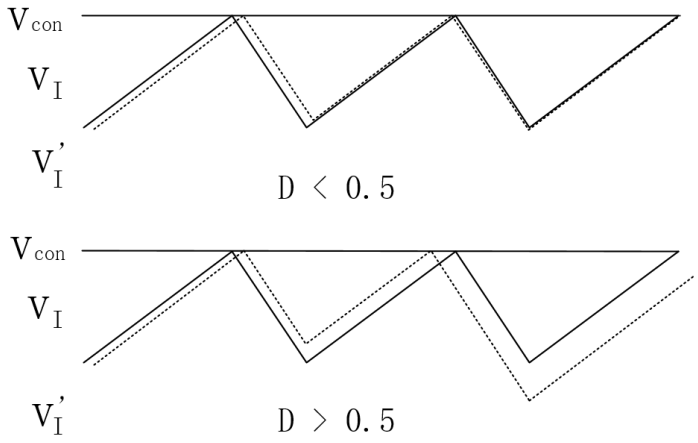


Figure 4.9: Current feedback signal disturbance

For overcoming the aforesaid obstacle, a simple and efficient way is to employ a ramp signal. As shown in Figure 4.10, when the duty ratio exceeds 0.5, the sensed voltage signal V_1 is added with a compensation ramp signal V_{ramp}, and the summed signal is compared against V_{con}. In contrast to the case without compensation ramp, the error successively narrows and finally disappears. Therefore, with the assistance of the compensation ramp, in PCM control, the PWM converter can operate stably with the duty ratio range from 0 to 1.

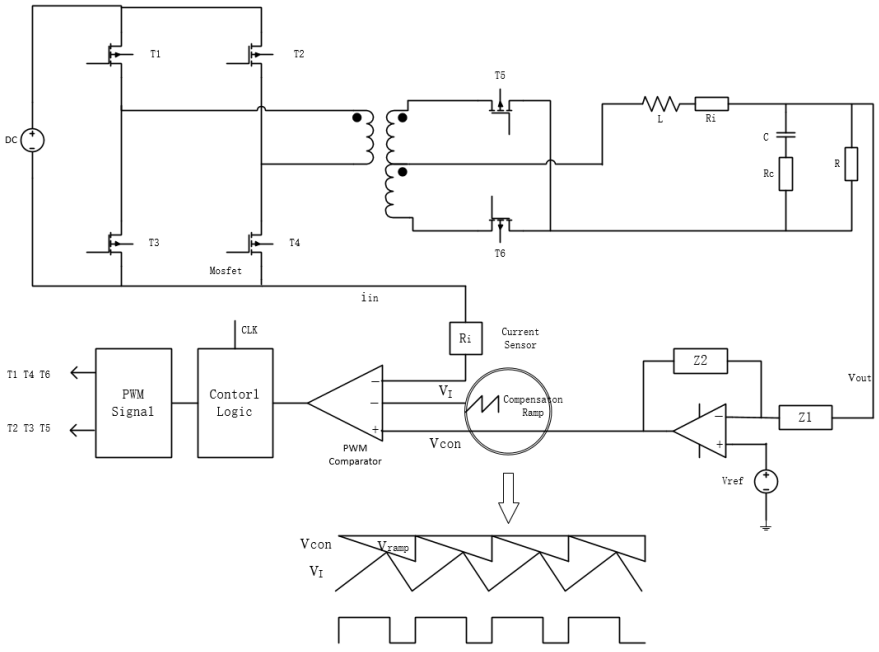


Figure 4.10: Refined control scheme and waveform of peak current model control

Figure 4.11 is the small-signal model block diagram representation for peak current mode controlled PWM converters, where the model of the power stage part can

be established in terms of the previous discussion. There are two feedback loops involved in the system, including one current close-loop derived from the inductor current i_L, and the other voltage close-loop coming from output voltage v_o.

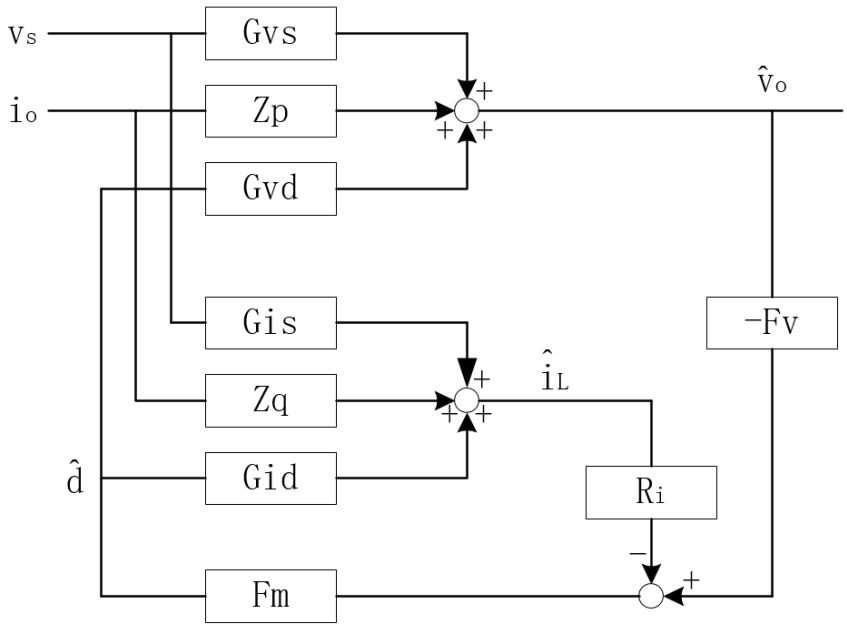


Figure 4.11: Block diagram representation for peak current mode controlled PWM converter

The gain block F_v represents the voltage feedback compensation, which can be expressed as

$$\begin{aligned} F_v(s) &= \frac{Z_2(s)}{Z_1(s)} = \frac{K_v}{1+\frac{s}{\omega_{zc}}} \\ K_v &= \frac{1}{R_1(C_2+C_3)} \\ \omega_{zc} &= \frac{1}{R_2C_2} \\ w_{pc} &= \frac{1}{R_2\frac{C_2C_3}{C_2+C_3}}. \end{aligned} \tag{4.5}$$

The CSN gain R_f serves as the current sensing network, and the modulator gain F_m represents the PWM block. For analyzing and formulating the modulator gain equation, the waveform structure of the PWM comparator is shown in Figure 4.12.

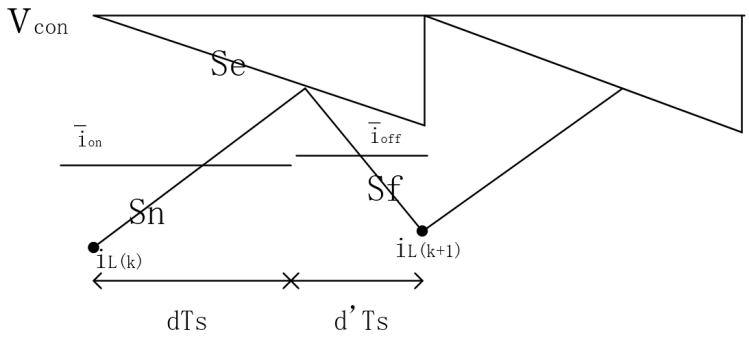


Figure 4.12: Peak current model control waveforms

By assuming that the sensed voltage waveform v_I increase periodically, the voltage $v_I(k+1)$ is larger than $v_I(k)$, where k represents the k^{th} period. When considering the CSN gain equals to 1, the magnitude of sensed current i_L equals to v_I. The follow equation can be derived from Figure 4.12.

$$\begin{aligned} \overline{v_I}_{on}(t) &= \bar{i}_{on}(t) = v_{con} - S_e dT_s - \frac{1}{2} S_n dT_s \\ \overline{v_I}_{off}(t) &= \bar{i}_{off}(t) = v_{con} - S_e dT_s - \frac{1}{2} S_f (1-d) T_s, \end{aligned} \tag{4.6}$$

where the voltage $\overline{v_I}_{on}$ and $\overline{v_I}_{off}$ are the average values during the on-time and off-time period separately. The values S_n and S_e represent the on-time and off-time slopes respectively. When assuming that the sensed voltage varies slowly, the voltage $\overline{v_I}_{on}$ is approximately equal to $\overline{v_I}_{off}$, and then the equation can be derived as

$$S_n dT_s = S_f (1-d) T_s. \tag{4.7}$$

By rearranging the equation above, it becomes

$$(S_n + S_f) d = S_f \tag{4.8}$$

Furthermore, when the voltage $\overline{v_1}_{off}$ is approximately considered as the averaged sensed voltage V_1, the equation can be rearranged as

$$\overline{v_I}_{off}(t) = V_I(t) = v_{con} - S_e dT_s - \frac{1}{2}(S_n + S_f) d(1-d) T_s. \tag{4.9}$$

By applying the linearization process to (4.9), it becomes

$$\begin{aligned} V_1 + \hat{v_1} = (V_{con} + \hat{v_{con}}) - S_e (D + \hat{d}) T_s \\ - \frac{1}{2}(S_n + S_f)(D + \hat{d})(1 - (D + \hat{d})) T_s. \end{aligned} \tag{4.10}$$

Then, the ac terms can be extracted, and the final expression is derived as

$$F_m = \frac{\hat{d}}{\hat{v_{con}} - \hat{v_1}} = \frac{2}{(S_n - S_f + 2S_e) T_s}. \tag{4.11}$$

The block diagram representation and all parameters derived and illustrated above will be applied for developing the closed-loop transfer function. In short, the PCM control consists of two control loops, and the outer voltage loop controls the inner current loop. This inner current loop takes charge of the dynamic variations of the inductor current waveform, which reveals that the inner current loop can be regarded as a current source when the system is steady-state. Thus, the inductor connected in series with the current source can be neglected, and the LRC second-order system is simplified to a first-order system with RC. Meanwhile, the outer voltage loop which controls the output voltage can be identical to a voltage source. The discussion above will be applied to analyze the small-signal closed-loop impedance.

4.2.2 Closed-Loop Transfer Function Expressions

Referring to the block diagram in Figure 4.11, the current loop T_i, as the negative feedback loop, is expressed as

$$T_i(s) = -\frac{\hat{i_L}(s)}{\hat{d}(s)}\frac{\hat{v_1}(s)}{\hat{i_L}(s)}\frac{\hat{d}(s)}{\hat{v_1}(s)} = G_{id}(s)R_fF_m \tag{4.12}$$

Likewise, the voltage feedback loop T_v is derived as

$$T_v(s) = -\frac{\hat{v_o}(s)}{\hat{d}(s)}\frac{\hat{v_{con}}(s)}{\hat{v_o}(s)}\frac{\hat{d}(s)}{\hat{v_{con}}(s)} = G_{vd}(s)F_v(s)F_m. \tag{4.13}$$

Then, by applying the Mason's gain formula to Figure 4.11, the output impedance is expressed as

$$Z_o(s) = \frac{Z_{out}(1+T_i) - Z_qR_fF_mG_vd}{1+T_i+T_v} \tag{4.14}$$

Furthermore, the relation between ac input current and ac inductor current is formulated as

$$\hat{i_{in}} = j(s)\hat{d} + M(d)\hat{i_L} \tag{4.15}$$

where $M(d)$ and $j(s)$ are the model parameters for PWM converters shown in Table 4.1 [12].

Table 4.1: Parameters for full-bridge buck converters and boost converters

	Full-bridge Buck Converter	Boost Converter
M(d)	$\frac{d}{n}$	$\frac{1}{1-d}$
j(s)	$\frac{V_o}{nR}$	$\frac{V_o}{(1-D)^2R}$

Therefore, Figure 4.11 is reconstructed to be illustrated in Figure 4.13, with blocks related to the ac input current signal $\hat{i_s}$ added.

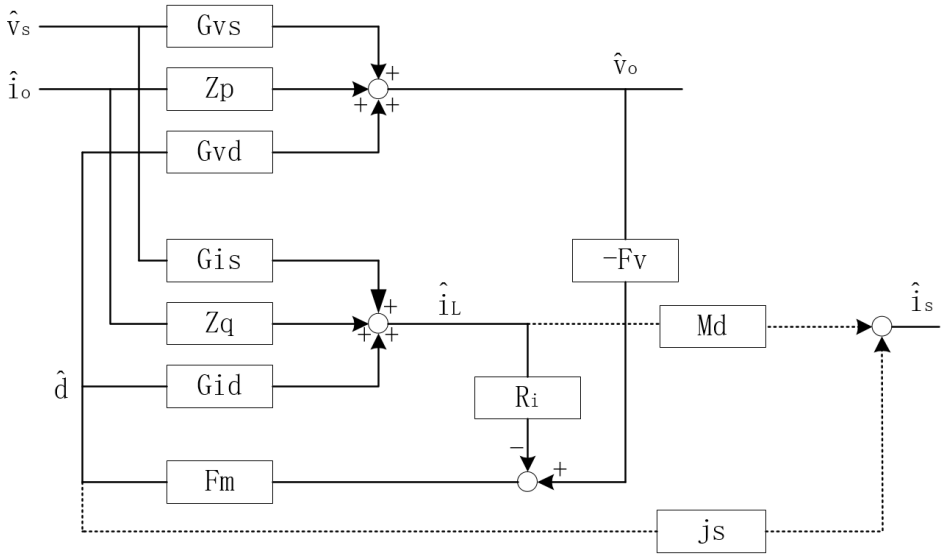


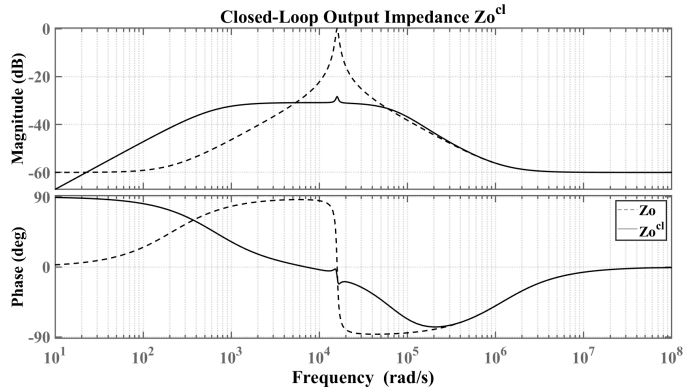
Figure 4.13: Modified block diagram representation for peak current model controlled PWM converters

The input impedance Z_{in} is derived in the same rule as that of input impedance Z_o, and it becomes

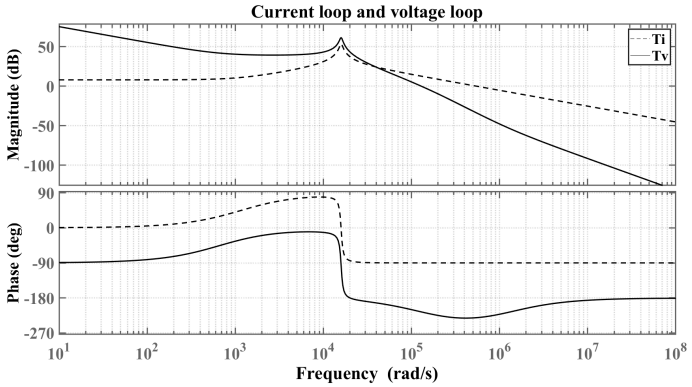
$$Z_{in}(s) = \frac{1 + T_i + T_v}{G_{is}M(d) + G_{vs}F_vF_mj(s) - G_{is}A_fF_mj(s)}. \tag{4.16}$$

4.2.3 Bode Plot Representations and Physical Meanings of Closed-Loop Transfer Functions

Figure 4.14a shows the Bode plot of the closed-loop output impedance for PWM isolated full-bridge dc-dc buck converter, and the open-loop output impedance that serves as the reference is involved as well.

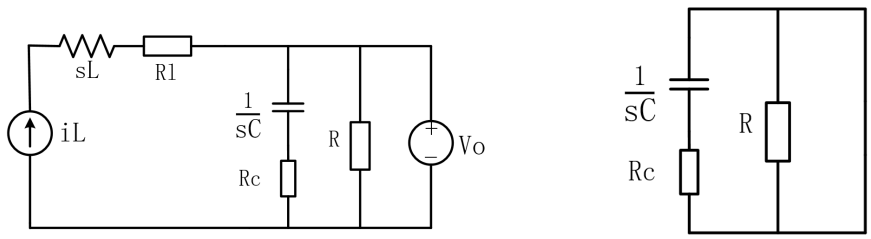


(a)



(b)

Figure 4.14: (a).Closed-loop output impedance for PWM isolated full-bridge dc-dc buck converter (b)Outer voltage loop and inner current loop



(a) **(b)**

Figure 4.15: (a).Equivalent circuit of closed-loop output impedance at low frequencies (b).Refined equivalent circuit of closed-loop output impedance at low frequencies

At the low frequency, in Figure 4.14b, the voltage loop gain and current loop gain reflect the performance of the system steady-state error. When the frequency reaches zero, the magnitude of the voltage gain approaches infinity. Therefore, the output voltage is controlled to a constant value, and then the voltage loop can be replaced with a voltage source in the output impedance equivalent circuit shown in Figure 4.15a. Meanwhile, the inductor current waveform controlled by the current loop has few variations due to the steady output voltage, which implies that the current loop

can be substituted with a current source. Thus, the equivalent circuit of the output impedance at the low frequency is refined in Figure 4.15b, where the voltage source is short circuit and the current source is an open circuit, based on the Thevenin's Theorem.

According to the equivalent circuit at low frequency, the magnitude of the output impedance is equal to zero. At the high frequency, T_i and T_v approximately reach zero, which reveals that the controller has few effects on the power stage. Thus, the closed-loop output impedance ${Z_o}^{cl}$ simply follows the open-loop output impedance Z_o as shown in Figure 4.14a.

The closed-loop input impedance ${Z_{in}}^{cl}$ analysis is initiated in Figure 4.16. As same as the output impedance analysis above, the open-loop input impedance is included.

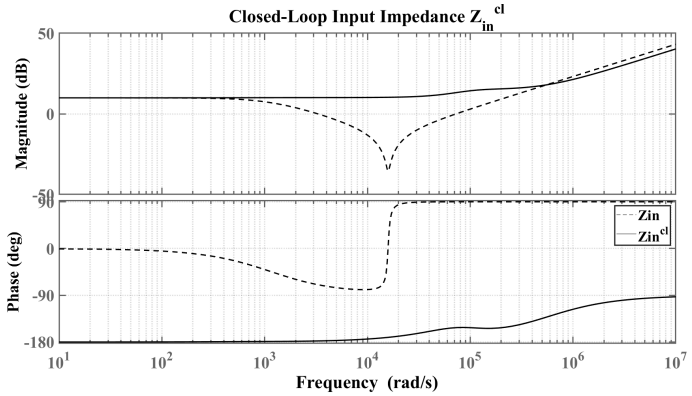


Figure 4.16: Closed-loop input impedance for PWM full-bridge buck converter

At the low-frequency domain, ${Z_{in}}^{cl}$ is characteristic with the negative resistance, where the amplitude of ${Z_{in}}^{cl}$ is constant and the phase angle is -180 . For analyzing this phenomenon, assuming the efficiency of the converter is 100 %, the output power is expressed as

$$P_o = V_{in} I_{in} \tag{4.17}$$

where V_{in} and I_{in} are the input voltage and current respectively. By adding the ac disturbance, it becomes

$$P_o + \hat{p_o} = (V_{in} + \hat{v_{in}})(I_{in} + \hat{i_{in}}). \tag{4.18}$$

The output power is approximately constant due to the implementation of the controller. Thus, the output power ac disturbance is neglected, and it becomes

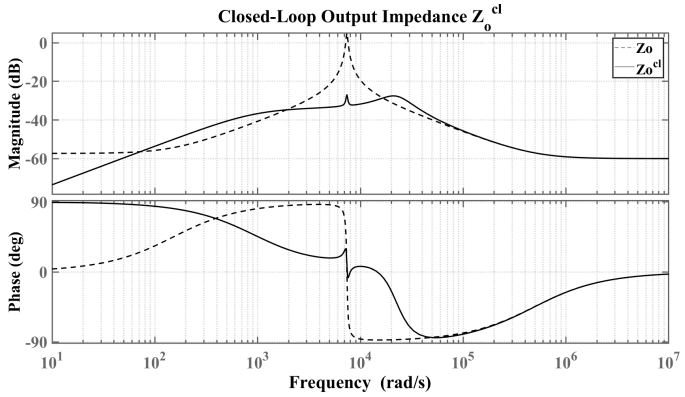
$$\begin{aligned} P_o &= V_{in} I_{in} + \hat{v_{in}} I_{in} + V_{in} \hat{i_{in}} + \hat{v_{in}} \hat{i_{in}} \\ &\approx V_{in} I_{in} + \hat{v_{in}} I_{in} + V_{in} \hat{i_{in}}. \end{aligned} \tag{4.19}$$

Therefore, the input impedance ${Z_{in}}^{cl}$ is derived as

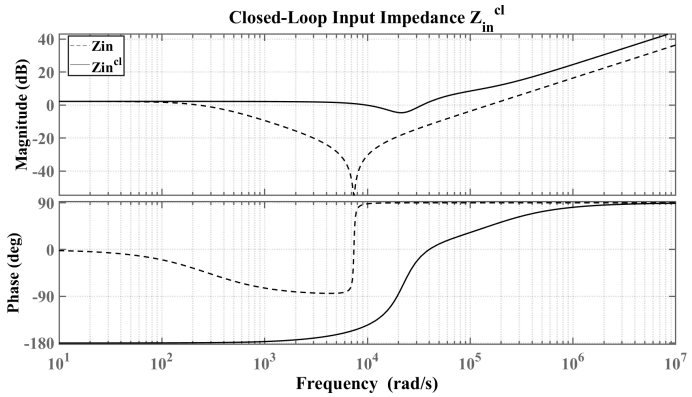
$${Z_{in}}^{cl} = \frac{\hat{v_{in}}}{\hat{i_{in}}} = -\frac{V_{in}}{I_{in}} = -\frac{{V_{in}}^2}{P_o} = -(\frac{n}{d})^2 R \tag{4.20}$$

Therefore, at low frequencies, Z_{in} overlaps ${Z_{in}}^{cl}$ with the same amplitude of $(\frac{n}{d})^2 R$. At high frequencies, the controller barely impacts on the power stage. It is expected that ${Z_{in}}^{cl}$ follows Z_{in}, but there is still some error between Z_{in} and ${Z_o}^{cl}$.

Figure 4.17 shows Bode plots of the closed-loop input and output impedance for PWM boost converter respectively, and these two impedances can be analysed in the same manner as the PWM isolated full-bridge dc-dc buck converter.



(a)



(b)

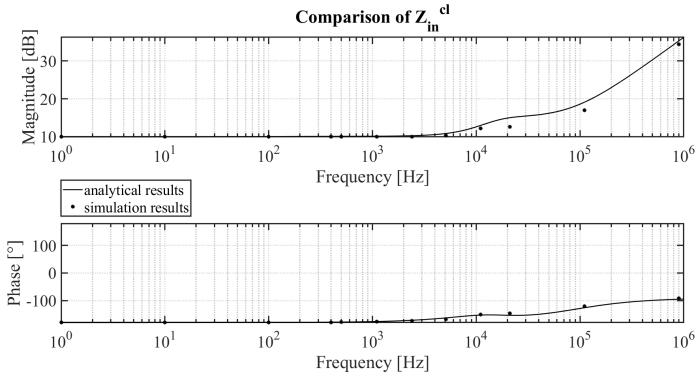
Figure 4.17: Closed-loop output and input impedance for PWM boost converter

To conclude, from the perspective of output impedance, the peak current control model improves the anti-interference ability of the system, and the impedance amplitude that closes to zero at low frequency reduces the power losses in the system. In the analysis of the input impedance, the peak current control mode brings the negative resistance property of the input impedance at low frequencies and improves the load-ability of the system when pre-stage is taken into consideration.

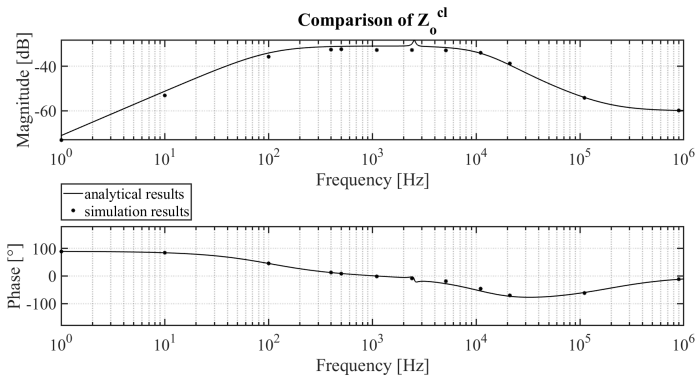
4.2.4 Analytical Transfer Functions Verification

This section expounds the comparison between analytical results and simulation results for the closed-loop input and output impedance. By applying the same method as mentioned in Section 3.1.5 and combining with the modelling theory of the peak

current mode control, simulation models are constructed in Appendix A.8 and Appendix A.9. Figure 4.18 and Figure 4.19 illustrate the Bode plot comparison of the simulation results and analytical transfer functions for the two PWM converters, where the solid line represents the analytical results, and the scattered points originates from the simulation model. Although there are still some errors between the analytical results and simulation results at some frequencies band, the overall trend is consistent. Thus, the simulation model and the derived transfer function, to some degree, are required to be improved.

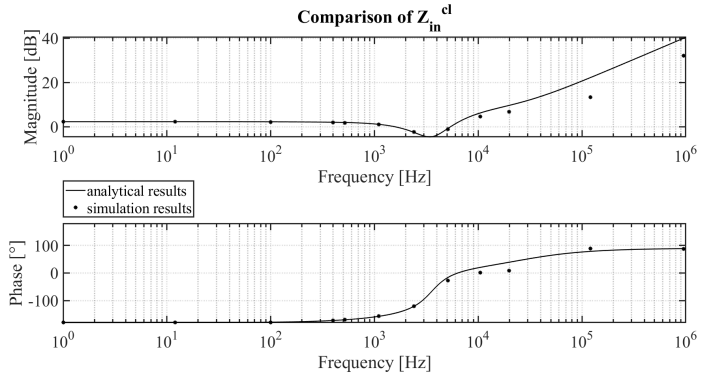


(a)

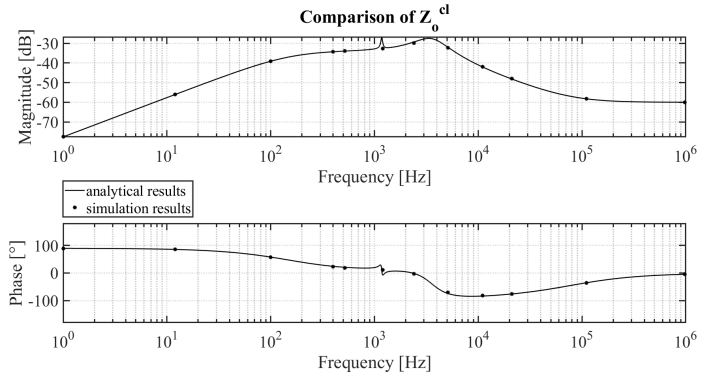


(b)

Figure 4.18: (a).Comparison of the closed-loop input impedance for PWM full-bridge buck converter (b).Comparison of the closed-loop output impedance for PWM full-bridge buck converter



(a)

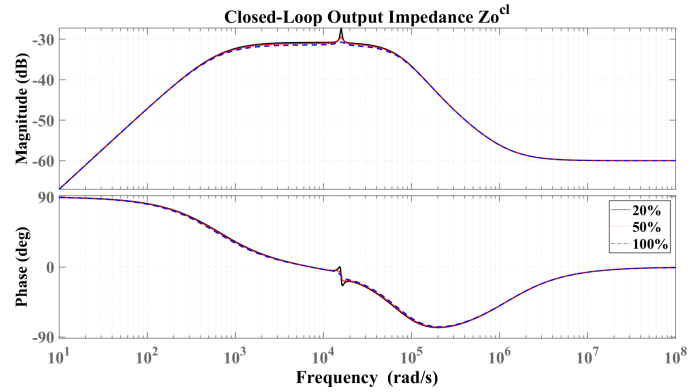


(b)

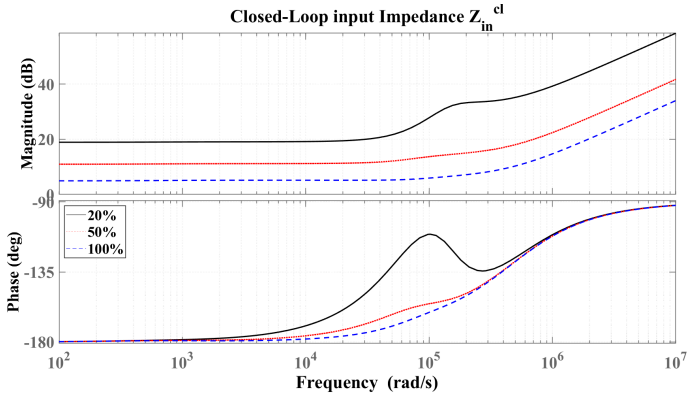
Figure 4.19: (a).Comparison of the closed-loop input impedance for PWM boost converter (b).Comparison of the closed-loop output impedance for PWM boost converter

4.2.5 Boundary Condition Analysis

This section explores the performance of the input and output impedance for PWM converters under the boundary condition, where possible combinations of the input voltage, output voltage and output power are formed in terms of their ranges. Under the condition of $V_{in} = 32[V]$ and $V_o = 17V$, Figure 4.20 illustrates Bode plots of the closed-loop input and output impedance when the full-load P_o, the half-load $50\%P_o$ and light-load $20\%P_o$ are taken into consideration.



(a)



(b)

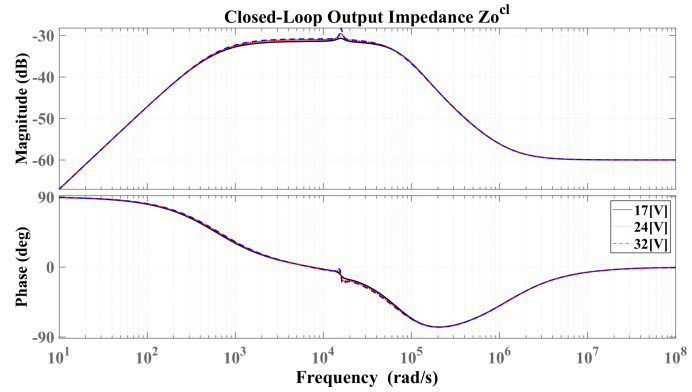
Figure 4.20: (a).Closed-loop output impedance under the condition of 20%, 50%, 100% P_o (b).Closed-loop input impedance under the condition of 20%, 50%, 100% P_o

In Figure 4.20a, it is clear that Z_o has few variations along with the frequency domain except the parallel resonant point nearby, since Z_o at the parallel resonant depends on the output resistance R, which can be expressed as

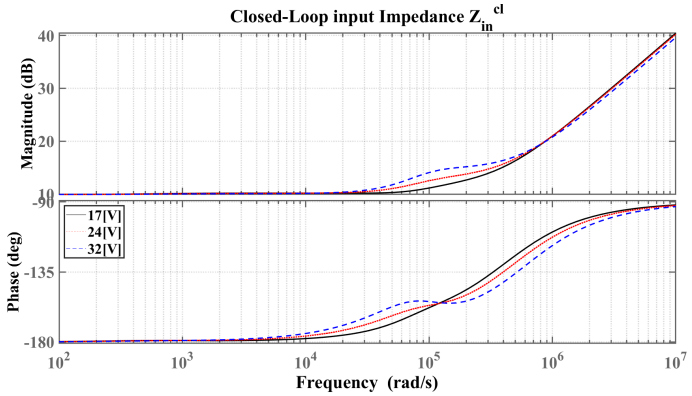
$$R = \frac{{V_o}^2}{P_o}. \tag{4.21}$$

With the decline of the output power P_o, the output resistance increases which leads to a rising Z_o in the region of the parallel resonant point. Inversely, in Figure 4.20b, the input impedance at low frequencies has a dramatics influence from the varying of output power. This phenomenon can be explained by (4.20), where Z_{in} at low frequencies has a strong positive correlation with the output resistance R.

Under the condition of $P_o = 1000[W]$ and $V_{in} = 56[V]$, Figure 4.21 shows the bode plot of the input and output impedance when the output voltage equals to 17[V], 24[V] and 32[V].



(a)



(b)

Figure 4.21: (a).Closed-loop output impedance under the output voltage condition of 17[V], 24[V] and 32[V] (b).Closed-loop input impedance under the output voltage condition of 17[V], 24[V] and 32[V]

Similarly, the output impedance is slightly affected by the variation of the output voltage. Meanwhile, the input impedance at low frequencies remains unchanged. For analysing this phenomenon, the input impedance at low frequencies is derived as

$$Z_{in} = \frac{n^2}{d} R = \frac{n^2}{d} \frac{V_o^2}{P_o} = \frac{V_{in}^2}{P_o} \tag{4.22}$$

Since the V_{in} and P_o are selected to be constant, the input impedance at low frequencies is the same value.

To conclude, the boundary condition analysis illustrated above reveals that the small-signal input and output impedances are inextricably linked to the variation of load demands such as output power, output voltage and so on. Specifically, compared with the performance of the output impedance, the input impedance is dramatically affect by the varying of conditions. Thus, it is critical to take the load demands range into consideration when designing the circuit in the power system.

5

Conclusion

Front-end converters and PWM dc-dc converters are widely adopted in the power system for telecom applications. Specifically, in this thesis work, the LLC resonant converter, the PWM isolated full-bridge dc-dc buck converter and boost converter, as typical topologies, are mounted in a telecom power system. In order to guarantee the stability and anti-interference capability of this power system, some researches have been conducted on the principles, mathematical models and simulation models of these converters.

Initially, operation principles of these converters are investigated in Chapter 2, and correspondent simulation models are established to verify these theories. Next, the small-signal modelling, as the fundamental and core mathematical method, is applied to these converters. These completed small-signal models are sequentially utilized to derive small-signal transfer functions such as the input impedance and output impedance. Furthermore, bode plots of these transfer functions are drawn to intuitively analyze the stability of the system, and the simulation model is designed and then verified by the mathematical model, both of which establish a solid foundation for further research.

The main research is conducted in Chapter4, where the small-signal modelling of these converters with closed-loop control is studied. Specifically, the LLC resonant converter and PWM converters are employed with different control schemes, VM control and PCM control respectively. By applying the asymptotic analysis method, the closed loop can be designed and the relevant parameters can be derived. As same as for the above-mentioned process, final bode plots of closed-loop small-signal transfer functions are diagrammed, and the physical meanings behind them are illustrated. Based on the aforesaid study and combined with the self-defined boundary condition analysis, it is founded that components such as inductance, capacitance and resistance in the circuit are closely bound up with the stability and anti-interference capability of the power system. Moreover, compared with the power system with open-loop control, the involvement of the controller improves the performance of the system in terms of the two properties mentioned above. Thus, it is essential to study and establish the small-signal model to select proper circuit topologies and control strategies of the system. Also, the proper values of these components in the circuit can be estimated.

However, there are still some limitations in this thesis work. For simplifying the process of the closed-loop transfer functions derivation of the LLC resonant converter,

only the simple voltage mode control is applied to the LLC resonant converter in this thesis work. Besides, the entire study of this thesis work mainly focuses on the small-signal modelling of the converters individually. Thus, the results are restricted to the single converter but not the power system. In order to further improve the study, the small-signal modelling of the entire power system needs to be established. Moreover, the experimental part needs to be added to improve the reliability of the research, and the shifting load demands of the 5G power system need to be taken into consideration as well.

In addition, it is essential for us to consider the ethics and sustainability in this thesis work. From the perspective of professionals, the outcomes of this thesis work can serve as a learning tool for engineers to learn about or go over the small-signal modelling method and get the link between impedance and stability of the system. We have put an effort in checking the parameters used so that they are as correct as possible, furthermore, we have displayed the results as the models have predicted also when the results were not exact, this means that someone else can take the prerequisites and descriptions in this report, redo the work, get the same results, and even update these models to get more accurate results. From the perspective of companies, it is more economical and efficient to design and update the hardware circuit in simulation models compared to produce samples in reality. However, the reliability and functionality of these models need to be further examined by the company, and there are still some gaps between the virtual model and the real circuit. Thus, it is still possible for the company to invest human and material resources to verify these models to be practical. From the perspective of individuals, it is known that these models might be used to improve the 5G power system, and then boost the stability of the telecom signal transmission. It is critical for us to communicate with others with a more stable telecom signal transmission, in which case our living standards are indirectly improved. Besides, this thesis work accords with the concept of sustainable development since all works are done in virtuality without wasting materials to produce hardware circuits in reality.

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A
Appendix

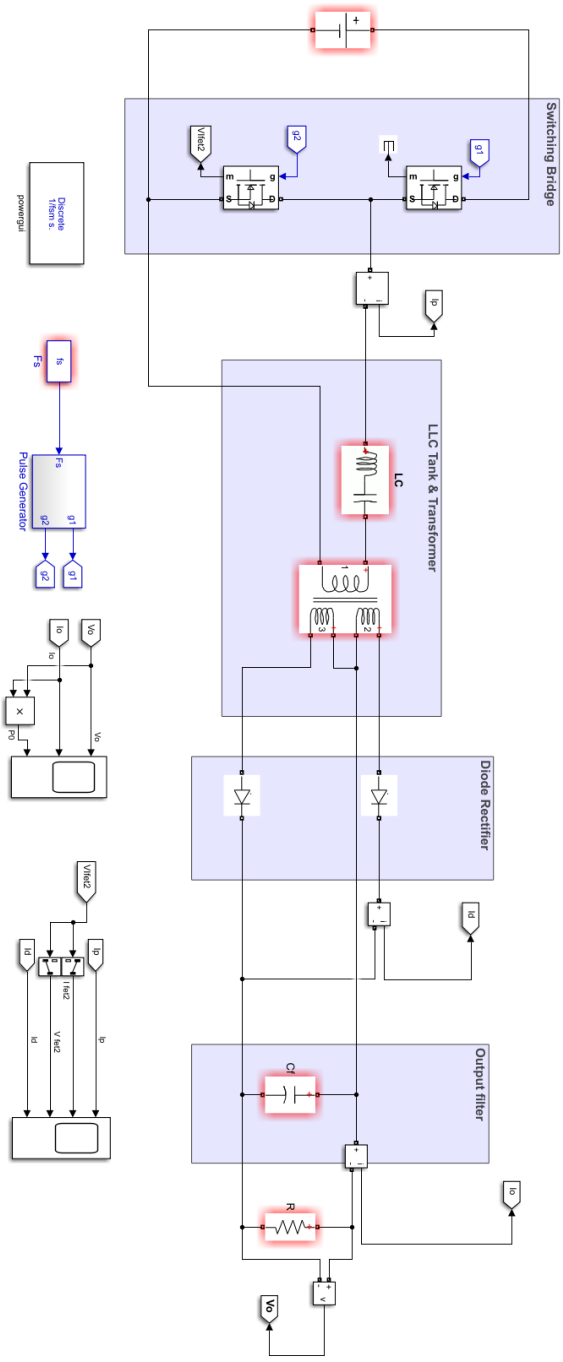

Figure A.1: Simulation model of the LLC resonant converter II

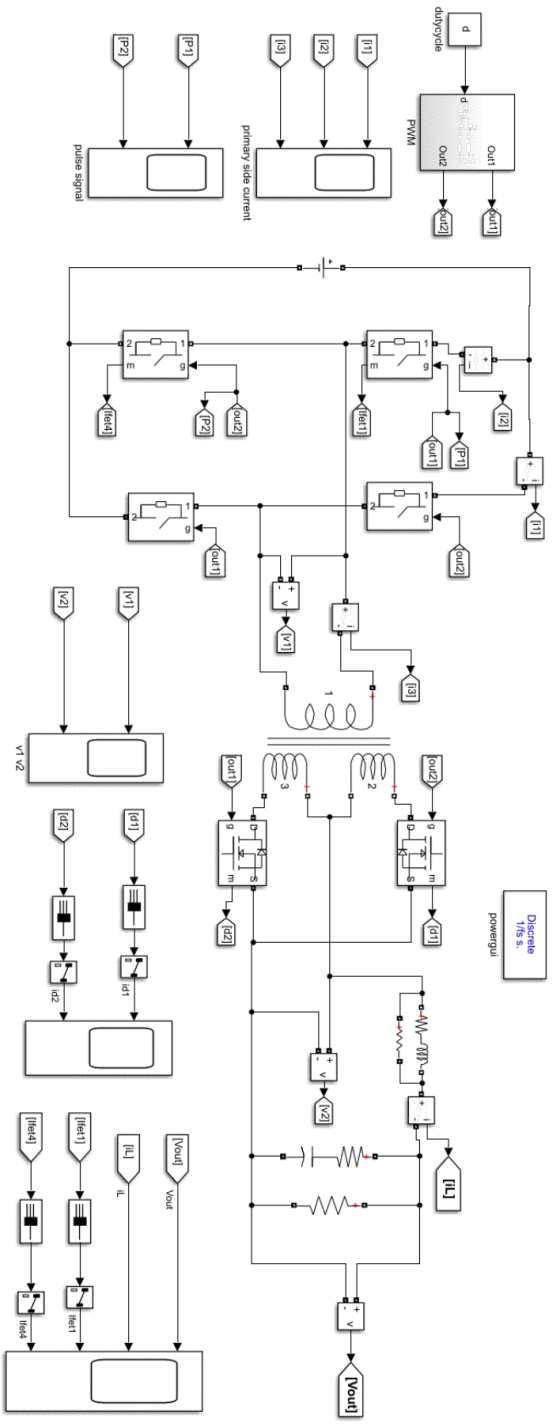

Figure A.2: Simulation model of the PWM full-bridge buck converter

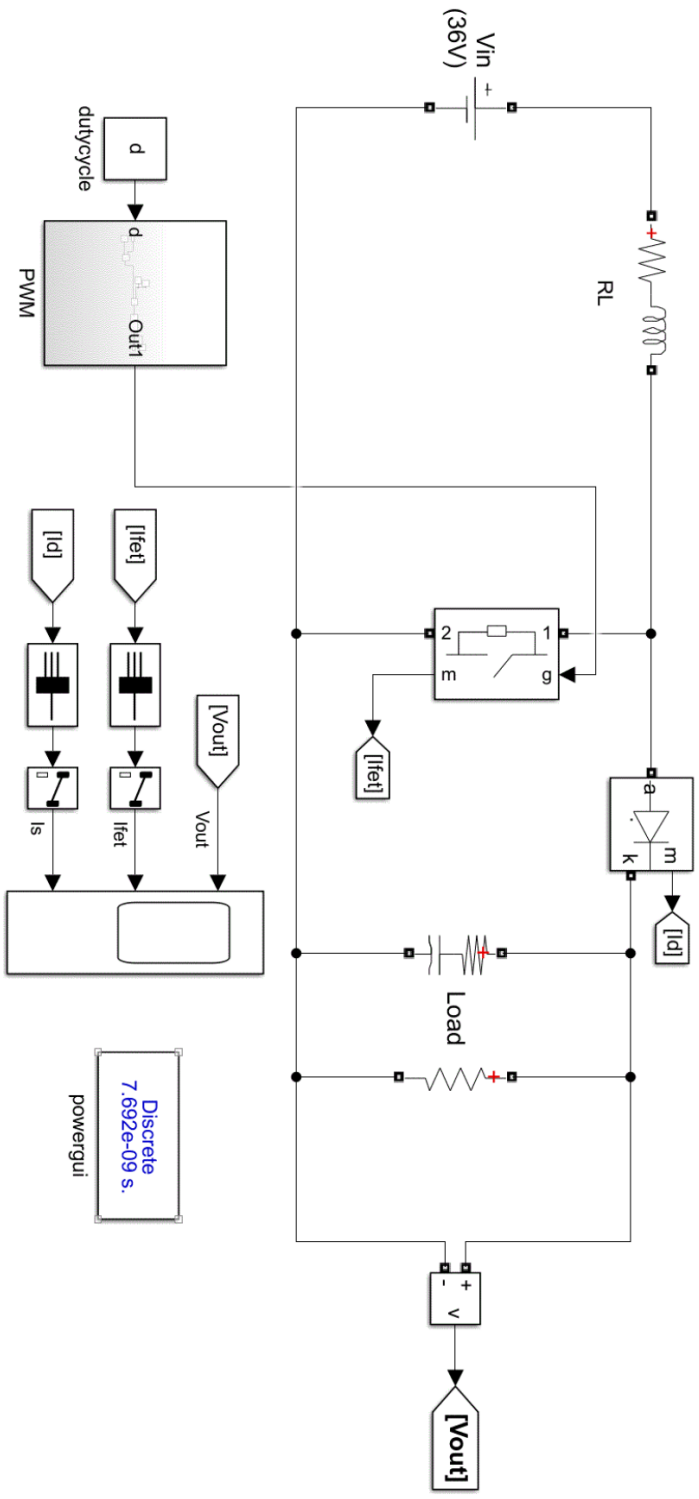

Figure A.3: Simulation model of the PWM boost converter

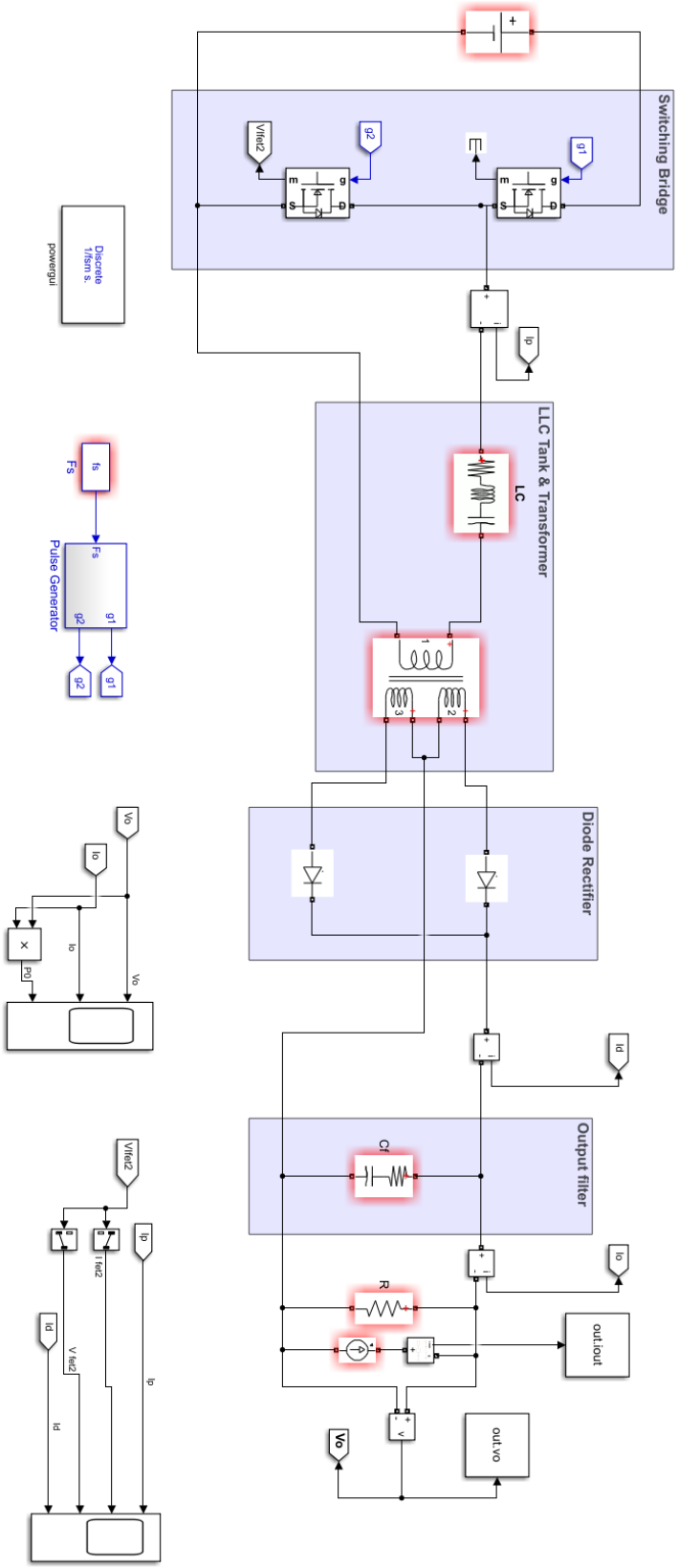

Figure A.4: Simulation model of the LLC resonant converter for output impedance analysis

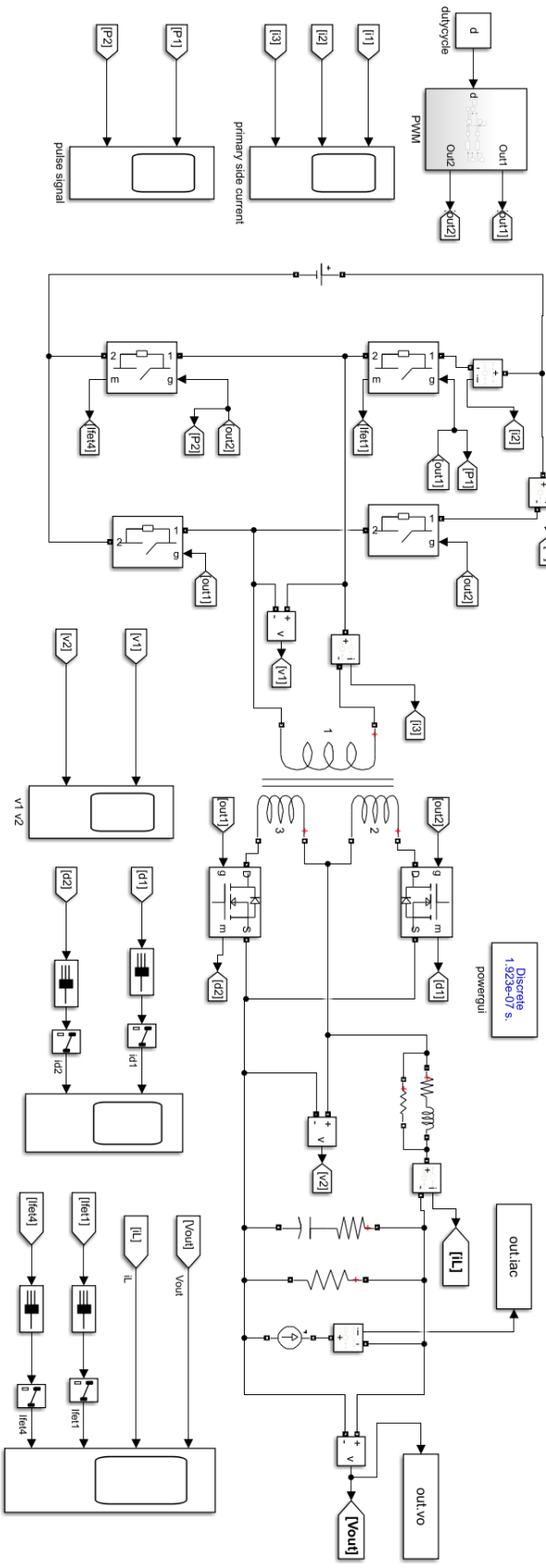

Figure A.5: Simulation model of the PWM full-bridge buck converter for output impedance analysis

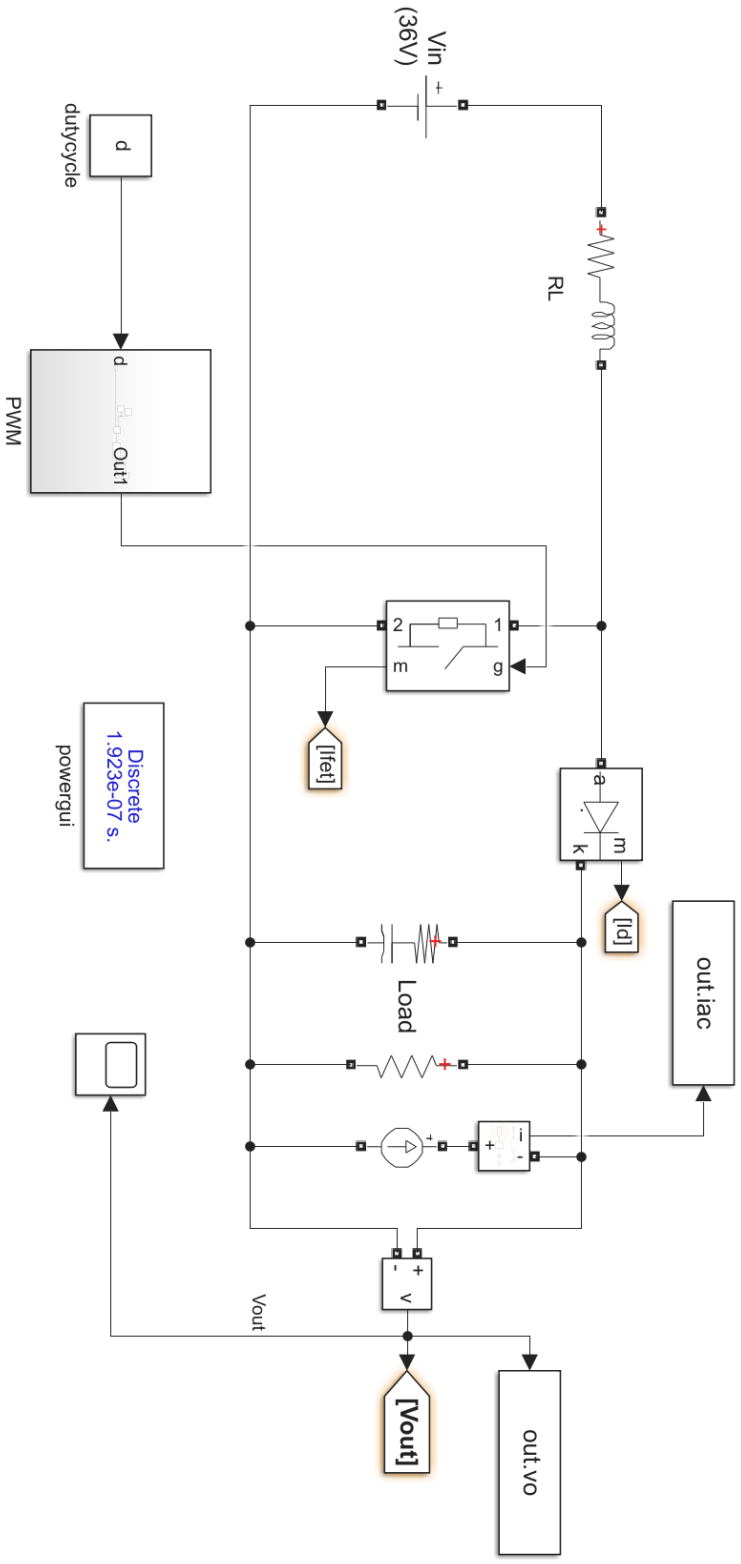

Figure A.6: Simulation model of the PWM boost converter for output impedance analysis

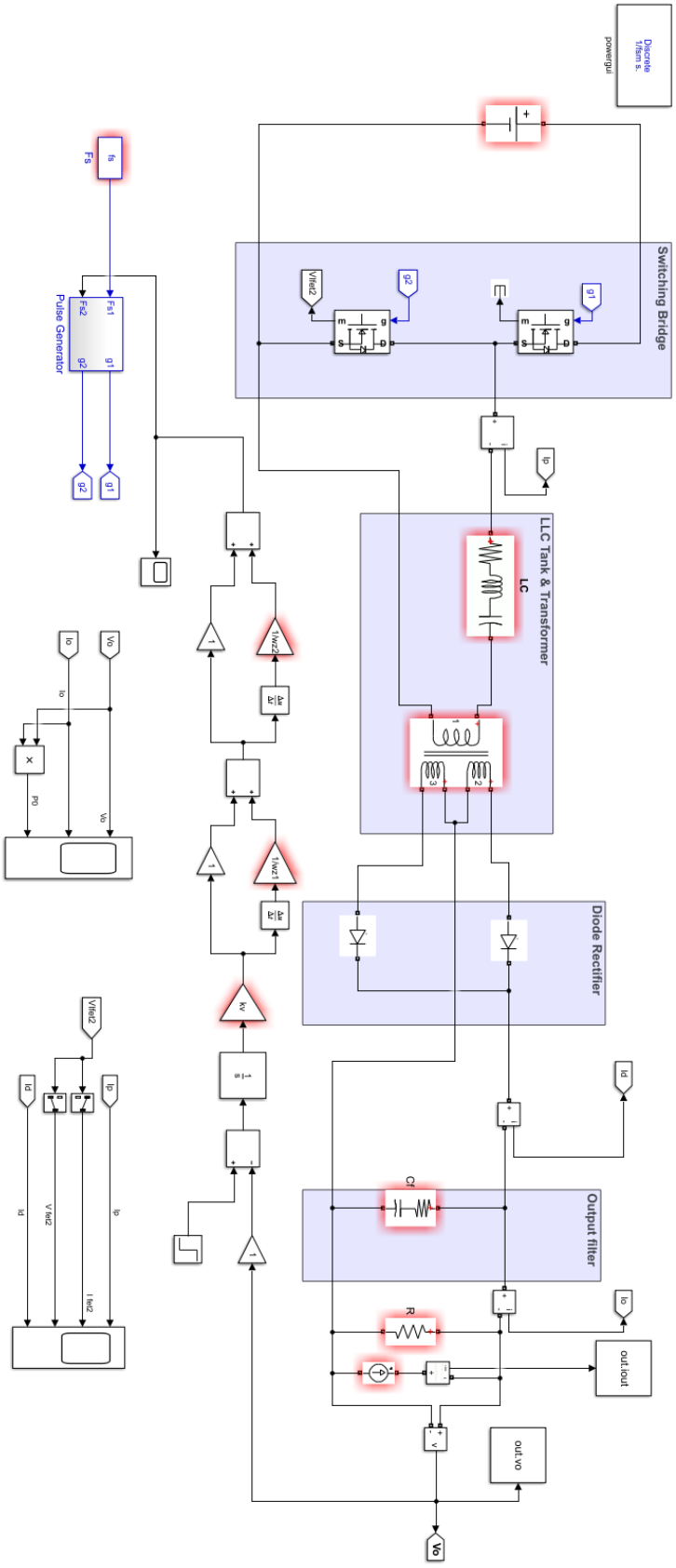

Figure A.7: Simulation model of the voltage mode controlled LLC resonant converter for output impedance analysis

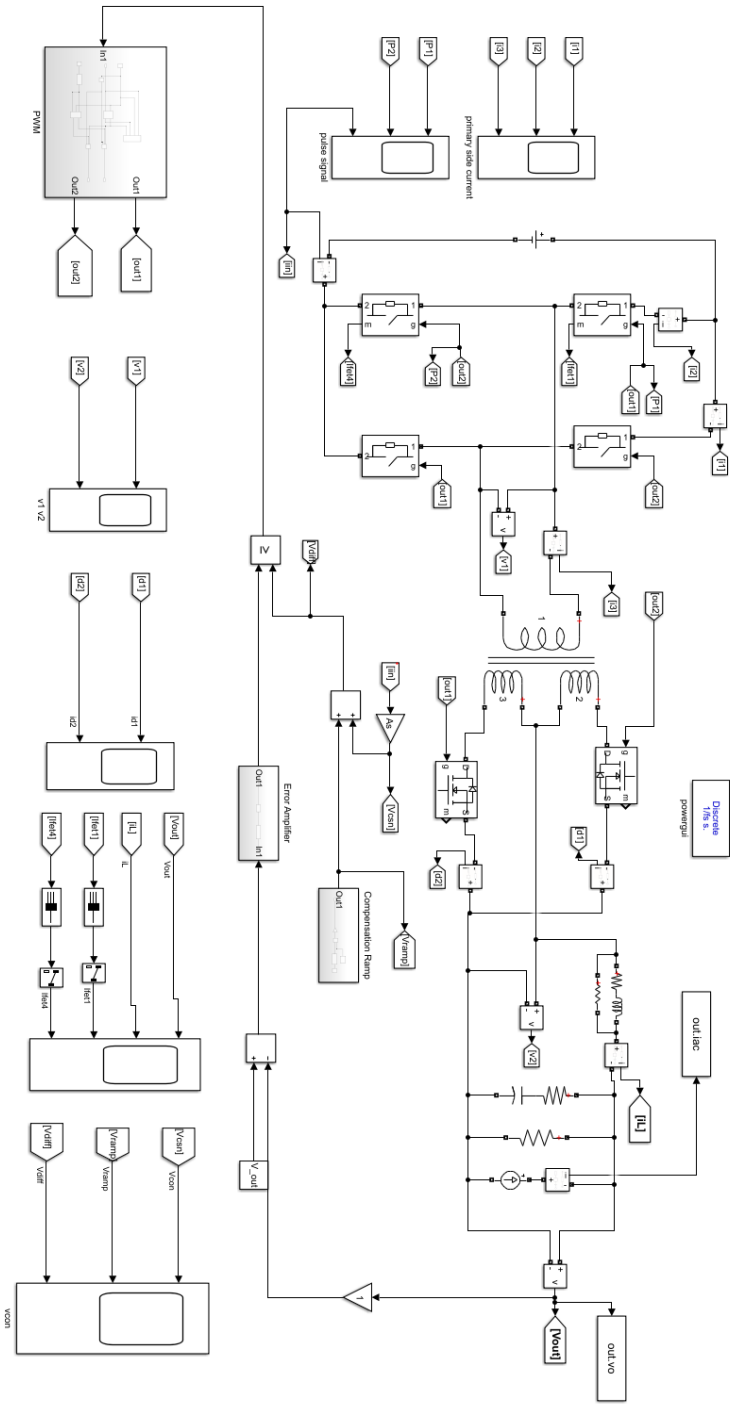

Figure A.8: Simulation model of the peak current mode controlled PWM full-bridge buck converter for output impedance analysis

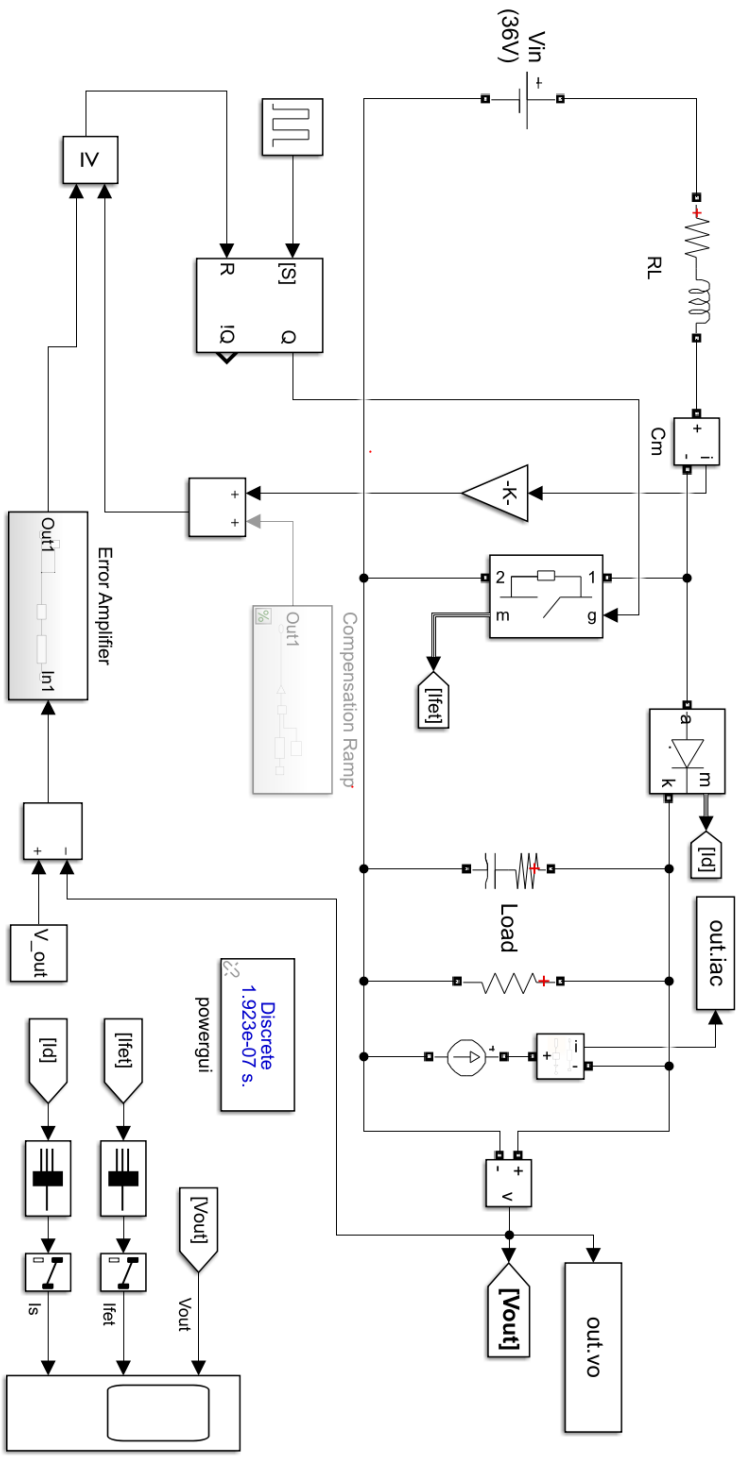

Figure A.9: Simulation model of the peak current mode controlled PWM boost converter for output impedance analysis