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Thermal Simulations of a System-in-Package for Space Applications

Master's thesis in Embedded Electronic System Design

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Gothenburg, Sweden 2025

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Master's Thesis 2025
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Typeset in LaTeX
Gothenburg, Sweden 2025

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Abstract

Frontgrade Gaisler AB is investigating a System-in-Package (SIP) based on their radiation hardened, fault-tolerant, octa-core, SPARC LEON and RISC-V microprocessor (GR765) together with DDR4 memories. The SIP aims to provide reliable, high performance processing in a small package form factor for space applications. The packaging of processor and memories together increases the demands on the package for proper thermal management. This task is further complicated by the harsh space environment, which needs special considerations during the design process. This work supports the developments of the GR765 SIP through thermal simulations using computational fluid dynamics (CFD). Example models of the SIP were built and simulated using ANSYS Icepak to determine where in the package hot spots occurred, how heat transferred through different parts of the package, and how different packaging methods and materials impacted the results.

The simulations of the thesis featured six different models. The first three models centered around finding an appropriate level of detail, which should give accurate results while not becoming too computationally intensive. These models also showed the impact which simplifications like ideal contact resistances and homogeneous heat generation had on temperature calculations. Model I, featuring both simplifications, had a peak temperature of 43°C lower than Model III which featured contact resistances and uneven heat generation. The following two models focused on lowering the package temperatures to fit a thermal target of 125°C at an ambient temperature of 55°C. The results of these simulations showed that swapping a plastic overmold for a metal lid could increase the peak temperatures of the package. With a dedicated heat sink the peak temperatures were within the thermal target at 99°C with 55°C as the ambient temperature. The last model explored memory stacking using film over wire (FOW). In these simulations, the stacked dies struggled with thermal management resulting in a peak temperature of 151°C in the memories at an ambient temperature of only 20°C. The combined results suggest that simplifications can have a large impact on the results, a dedicated heat sink is needed for the design, and additional thermal management methods are needed if die stacking is to be used in this kind of SIP.

Keywords: System-in-Package, heat transfer, electronics packaging, thermal simulation, Finite Volume Method

Acknowledgements

I'd like to start by thanking my family. You've followed me through all the ups and downs of my education, constantly offering advice and support. For this I am very grateful. The same goes for my friends, old and new, who were always curious of what progress I was making and kept me motivated when I struggled on my own.

Special thanks to my supervisors at Chalmers Technical University, Prof. Johan Liu and Lic. Markus Enmark. This thesis would not have been possible without your experienced insights and discussions. Thank you as well to Dr. Torbjörn M. J. Nilsson who provided lots of useful technical expertise during my simulations. And of course my examiner, Prof. Per Larsson-Edefors, thank you for your contributions in the early and late stages of my thesis project.

Finally, many thanks to Dr. Francisco Hernandez, M.Sc. Peter Sinander, and everyone else at Frontgrade Gaisler AB who contributed to my thesis. Either through insightful discussions of related topics, or through making me feel welcome to participate in their office activities. I hope to meet you all again in the future!

Erik Bolminger, Gothenburg, September 2025

Contents

1

Introduction

With developments in the area of semiconductor processing slowing down, designers and manufacturers have to look for other solutions for increased performance. Advanced packaging techniques allow for the combination of multiple chips in the same package, called a multi-chip module. Creating a package with chips designed to work together elevates the multi-chip module to a system in package (SIP). Compared to traditional packaging, the primary benefits of using SIPs are the shorter interconnects, which result in increased performance, and a compact form factor [1].The modular design also allows for combination of different semiconductor processes not possible with a monolithic design. Generally, SIPs are also easier for customers to use, as the development, integration, and quality assessment are all handled by the SIP manufacturer.

One form of SIP is the combination of a processor together with its memories. Frontgrade Gaisler AB (Gaisler) is investigating a SIP centered around the GR765, a radiation hardened, fault-tolerant, octa-core, SPARC LEON and RISC-V microprocessor targeted at space applications. The SIP could contain up to 12 DDR4 memory dies in the same package. The amount of dies placed in close proximity to one another does however introduce new design challenges.

Increasing the number of active dies will increase the temperatures of the package which could have large consequences. A package's inability to dissipate the heat generated by the dies leads to performance losses or in extreme cases even failure [2]. Component failure is especially devastating for space applications where maintenance is in most cases impossible. This thesis aims to provide a thermal management perspective on the SIP design process.

During SIP development, much time and resources could be spent trying to validate the design by testing unfinished products. In order to gain a fundamental understanding of the design before manufacturing, computational analyses are useful tools in an engineer's arsenal. This thesis uses computational fluid dynamics (CFD) to perform thermal simulations of some example SIP designs.

1.1 Purpose and Goal

The purpose of this project is to assist Gaisler's investigation into the GR765 SIP through exploring suitable package designs from a thermal perspective. The report aims to give a good understanding on the issue of thermal management and to

provide an overview of some existing solutions to these issues. The insights gained from the project provide the team with the necessary knowledge to engage in thermal management discussions both internally and with their suppliers. The results could also hint towards what kinds of designs are viable, and what methods should be avoided during potential future development of a GR765 SIP.

The goals of the project are to study and present the underlying theory on heat transfer in a space environment and explore SIP manufacturing techniques and materials from a thermal management perspective. The knowledge gained from the study together with Gaisler's theoretical data for the microprocessor acts as the ground works for a series of CAD models. Through thermal simulation of these models, the project aims to build knowledge of the thermal impact of different SIP designs and layouts. The models may be revised with thermal management techniques if they are deemed necessary to remain within temperature constraints.

1.2 Thesis Outline

Following the introduction, chapter 2 presents some necessary technical background. This includes knowledge of thermodynamics, SIP packaging techniques and materials, and a presentation of the simulation software. Any methodology used to plan, research and perform the work is presented in chapter 3. The design of the different simulation models is presented and motivated in chapter 4. The simulation results are shown in chapter 5, and discussed in chapter 6. Lastly, chapter 7 concludes the thesis and presents some possibilities for expansion through future works.

2

Technical Background

The following chapter presents technical background and theory needed to follow the thesis work. The chapter begins with fundamental understandings of heat transfer with the additional consideration of a space vehicle. Then, some microelectronics packaging techniques are introduced with the perspective of thermal management. The chapter finishes by describing the underlying theory of computational fluid dynamics using the finite volume method, along with other features of the ANSYS Icepak (Icepak) simulation software. The background provided in this chapter is used as a basis for the design choices made later in the thesis.

2.1 Heat

On a microscopic level, every molecule has some amount of kinetic energy. Observing a group of molecules, their average kinetic energy can be measured in terms of temperature. The more kinetic energy a group of molecules have, the higher their temperature. Thermodynamics is the science of how the energy and temperature of objects change in respect to their surroundings. The movement of these energies is referred to as heat.

In a given object heat can be either lost or gained, resulting in a change of temperature. Different materials have different sensitivities to this sort of temperature change. The amount of energy needed to force a specified change in temperature onto a certain mass of a material is known as the materials specific heat capacity. The higher the specific heat capacity, the more energy the object can absorb before showing an increase in temperature.

2.1.1 Heat Transfer

Heat transfer is part of the thermodynamic process where heat flows from an object of higher temperature to an object of lower temperature. The rate of transfer is dependent on the temperature difference between the objects and how susceptible the objects are to heat change. Heat transfer happen through three different processes: conduction, convection, and radiation.

Conduction

Conduction is the primary way of heat transfer inside of- and in between solids, and happen when heat is transferred through contact. The heat flow can be calculated

by Fourier's law, shown in differential form in equation 2.1.

$$\mathbf{q} = -k\nabla T \tag{2.1}$$

Here $\mathbf{q}$ is the heat flux density (W/m^2), k is the thermal conductivity (W/mK), and ∇T is the temperature gradient (K/m). The equation shows how heat flows from higher temperature towards lower temperature, at a rate either dampened or amplified by the thermal conductivity. Choosing materials with appropriate thermal conductivities is an important part of thermal management in an electronics package.

Thermal resistivity is the inverse of thermal conductivity. When multiplied by the distance heat travels through a material with a certain resistivity, and divided by the contact area, the objects thermal resistance is gained.

$$\theta = \frac{l}{kA} \tag{2.2}$$

Here θ is the thermal resistance (K/W), l is the distance which the heat is transferred, k is the thermal conductivity, and A is the contact area. When transferring between different objects, the contact resistance needs to be taken into account as well. The contact resistance arises from the microscopic imperfections in otherwise flat materials. The roughness of the surfaces creates small air pockets between the objects, lowering the true contact area. Zandén et al. have shown that increased roughness leads to increased contact resistances, which correlates with the area dependency in equation 2.2. Pressing together the surfaces with higher pressure will reduce the contact resistances due to the increased contact area despite surface roughness [3].

Convection

Heat transfer between the surface of an object to a moving fluid is called convection. A fluid can be either a gas or a liquid. The convection can be caused naturally, for example movement caused by temperature dependent density changes. Convection can also be forced, when the movement is produced by external inputs. A fan can be used to move gasses, and liquids can be moved through a closed loop with a pump.

Radiation

Radiation refers to the process of heat transfer from an object in the form of electromagnetic waves. Any object with a temperature higher than absolute zero radiates some degree of heat. The heat transfer from an object through radiation is defined by Stefan Boltzmann's law, shown in equation 2.3

$$P = A\epsilon\sigma T^4 \tag{2.3}$$

Here P is the radiated heat (W), A is the object's surface area (m^2), ϵ is the emissivity (unit-less), σ is the Stefan-Boltzmann constant (W/m^{2}T^4), and T is the temperature (K). Emissivity is a measurement of how efficiently a surface is able to transfer

heat through radiation. It is used as a ratio ranging from 0 to 1, with 1 being perfectly efficient radiation of heat. The equation is otherwise highly temperature dependent, but surface area is also of importance.

Heat Transfer in Space

Consider a vehicle in the vacuum of space. The absence of fluid in the vacuum makes convection impossible. The vacuum also removes any medium for conduction, meaning the only remaining process for heat to transfer to and from the vehicle is radiation. The possible thermal processes affecting the vehicle can be reduced and simplified to the following:

1. Absorption of heat from external radiation
2. Generation of heat through electrical currents
3. Conduction of heat from one part of the vehicle to another
4. Radiation of heat into space

Processes 1 and 2 increase the temperature of the vehicle, and temperature is reduced by process 4. If the vehicle is to achieve thermal equilibrium, i.e. stable temperatures, the heat radiated from the vehicle has to be equal to the heat gained from absorption and heat generated by electronics.

Examining an individual component show some different behaviors. The surface area of the individual component is small in relation to the vehicle, meaning the radiation from a single component will likely be low in comparison to the larger vehicle. Instead, the generated heat first has to be conducted away from the component towards the surrounding vehicle, which in turn is able to more efficiently radiate the excess heat into space. The thermal design of the component should therefore focus on increasing the conduction from the heat generating circuitry to the vehicle.

2.1.2 Thermal Path

With conduction as the primary form of heat transfer at the component level, it is important to consider the possible ways for heat to conduct through the package. Figure 2.1 shows cross sections of two packages with different interconnects. The thermal paths, the different ways heat can transfer from the die to the printed wiring board (PWB), are marked with red arrows in each figure. Guo et al. stated that when the top side of the die is covered by a thermally insulating material, a majority of the heat generated will transfer downward through the package substrate [4].

The thermal paths can be presented in the form of an equivalent thermal circuit. These circuits enable analysis of the possible paths of conduction by representing the materials along each path as a thermal resistance between points. Figure 2.2 displays equivalent thermal circuit for the thermal paths from figure 2.1. The circuit shows sequential parts of the path as resistors in series, and alternate paths as resistors in parallel. Each material the heat passes through appears as a resistance according to equation 2.2. Contact resistances at surface interfaces are also included. A well extrapolated equivalent circuit should give an overview of all important aspects of the thermal path, highlighting targets for thermal optimization.

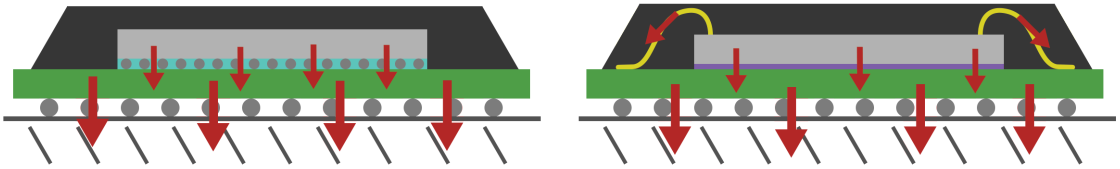


Figure 2.1: Thermal path in two types of packages. The left package contains a flip chipped silicon die, and heat moves downwards through the microbumps and underfill. The right package contains a wire bonded silicon die, and heat moves downwards through the adhesive and also through the bond wires.

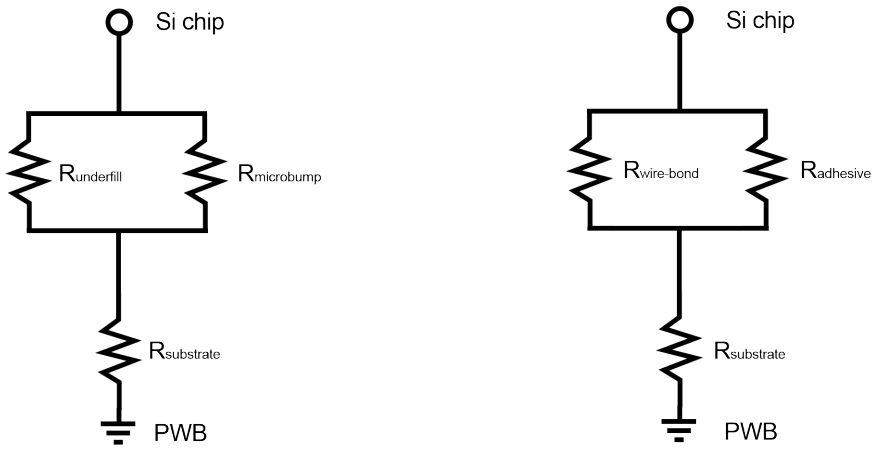


Figure 2.2: Equivalent thermal circuits of the two example packages shown in Figure 2.1

2.1.3 Thermal Uniformity

The placement of heat generating circuitry plays a role in the maximum temperature inside of the package. Rangarajan et al. showed that having multiple heat generating components close to one another makes the temperatures of each die higher than if they were more spread out [5]. On the die itself it is also helpful to separate the active circuitry, which was showed by Medina et al. Their work has the same processor perform the same task multiple times while using different cores. When the activity is spread out the peak temperature is lower compared to assigning the task to cores in close proximity [6].

Die placement on the substrate is also important. Having a more uniform temperature throughout the substrate allows for better transfer of heat from the die. Placing the die in the middle of a substrate allows heat to flow in all directions of the substrate. A die placed in the corner of a substrate will yield a higher temperature in the substrate, and due to the temperature dependency of conduction, lower the flow of heat from the die itself [5].

2.2 SIP Manufacturing

The purpose of electronics packaging is to provide the ICs with electrical interconnects, mechanical stability, and protection from their environment. The SIP takes it even further by incorporating multiple chips into a compact form factor. Considering our pre-existing knowledge of the GR765 microprocessor, this work will focus on the thermal aspects of available manufacturing techniques and thermal modeling of a ball grid array (BGA) package. The BGA is based on a substrate with an array of solder balls on its underside allowing for a large number of interconnects. Figure 2.3 showcases a couple of examples of BGAs to give an idea of the package structure.

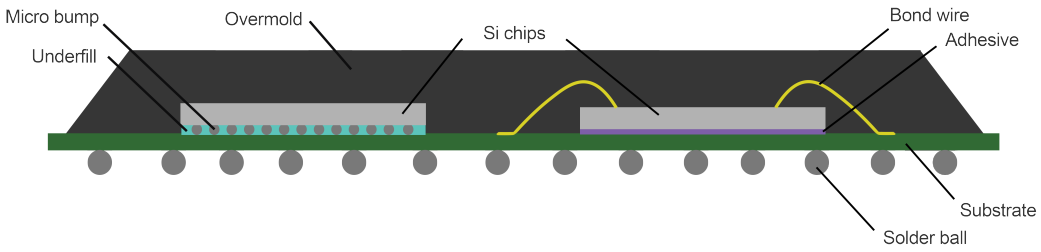


Figure 2.3: An example of a BGA package featuring both a flip chip and a wire bonded chip. The package is encapsulated by a plastic overmold.

There are many approaches to manufacturing a BGA. This section aims to present the key components of the package type, considerations to keep in mind when design-

ing a BGA, as well as some commonly used materials. Some of the more advanced techniques showcased in the section are usually not necessary for package manufacturing, but instead focus on improving upon the existing techniques in order to fit more chips in a smaller form factor.

2.2.1 Circuit Boards

In order to use the IC it needs to be connected to the remaining system. This is done through a circuit board. While there are different levels of circuit boards they all serve the same three general purposes: provide their components with mechanical stability, electrical connection, and if necessary help with thermal management.

The largest circuit board in the system will likely be a printed wiring board (PWB). Consisting of multiple layers of metal wiring and insulators, the PWB forms larger scale connections between components, including power supply and ground connections. On the component level a smaller form of circuit board, called a substrate, is needed. A substrate is conceptually the same as a PWB, but with finer signal routing and a shorter distances between interconnects, also known as the interconnect pitch. The smaller substrate allows for connection of one or more dice on one side and the PWB on the other. Cases with high interconnect requirements in terms of electrical performance can consider using an interposer. This third level of circuit board forms connections between different dice and between the die and substrate. The interposer increases the quality of the interconnects by for example reducing interconnect lengths or increasing I/O density.

Vias

The layered structure of the circuit boards allows for signal routing to utilize multiple times the surface area of the actual board. To make full use of the many layers a method of carrying the signal from one layer to another is needed. This is done through a via. Vias are holes in the insulation layers that get covered in metal, allowing for signals to transfer between signal layers. Some classifications of vias include through hole vias which pass through the entire board, blind vias that are only visible from one side, and buried vias which exist in between laminates and can not be seen from either side. The types of vias can be seen in figure 2.4.

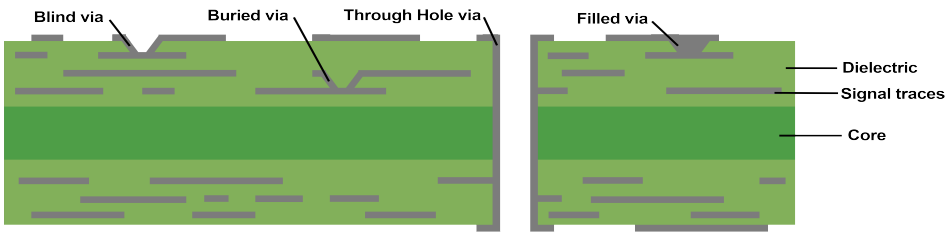


Figure 2.4: A showcase of different kinds of via structures in an organic circuit board.

Vias in Organic Circuit Boards: Large via structures like through hole vias are commonly formed by mechanical drilling through the circuit board. The smaller microvias, which intend only to connect internal layers together use laser drilling instead. After forming the hole, the via is plated with a metal, usually copper, to form the electrical connection. The plating can be extended to fill the entire hole, called a filled via, for better electrical and thermal performance [7].

Through Silicon Vias (TSVs): Three approaches exist for manufacturing TSVs: via-first, via-middle, and via-last. These names refer to when in the semiconductor manufacturing process the via is formed, relative to IC patterning and metalization of the connective pads on the IC. Manufacturing with the via-last approach is most common [7]. TSVs can be formed using for example the Bosch method, alternating etching and passivation steps to make the via itself, and then filled with metal by electroplating [8].

Even with all I/O needs met, use of additional vias can still be beneficial. Thermal vias are redundant vias which serve no electrical purpose, but are used to increase the metal concentration of the circuit board. The presence of more metal increases the thermal conductivity, transferring the heat faster through the board and away from heat generating components [9]. The placement of the thermal vias in comparison to the components has little effect on the temperature [10]. Baker et al. compared different methods of increasing thermal conductivity through a PWB. The study showed that thermal vias was a more effective way of increasing thermal conductivity from the die when compared to using a metal core in the substrate [11].

Substrates

The substrate's role in a package is to connect all of the package components together and form their connection to the PWB. The connection type to the PWB is what defines the package type. The package type considered in this work is a BGA package. The substrate consists of a core for increased stability, metal for signal traces and a dielectric or ceramic material for insulation. The position of the substrate in between the heat generating dice and the PWB means the substrate is a critical part of the thermal path.

An organic substrate is formed around a core made from woven glass fibers coated in a mixture of resin and additives. The additives could for example be hardeners, catalyzing materials or flame retardant materials. Through vias are formed and plated before additional layers are applied. The layered structure is made through a repeating process of metalization, patterning resist, etching, dielectric layering and microvia drilling. Organic substrates can be formed in large sheets and later diced into individual substrates, which makes them inexpensive to produce in large volumes. This low cost production has driven the organic substrate to be the most common type found today [7]. Due to the high contrast in thermal conductivity between the dielectrics and metals in the organic substrate, the thermal conductivity is often classified as in-plane or cross-plane. The metal layers give a high thermal conductivity in-plane while metal vias are needed to increase the cross-plane thermal conductivity.

For packages requiring a higher thermal conductivity, a ceramic package should be considered. Manufacturing ceramic packages starts with a ceramic powder carried in a solvent. The solvent is used to help cast the ceramic into the substrate shape. Vias and signal traces for each individual layer are performed before lamination. For the ceramic to take change from powdered form to bulk ceramic, the substrate needs to undergo a process called sintering. The process is performed at high temperatures, and when all laminates are treated together it is referred to as co-firing. Depending on the ceramic material the temperature will be either around 850°C (low temperature co-fired ceramic, LTCC), or at 1500-1800°C (high-temperature co-fired ceramic, HTCC). The sintering temperature will also have to be considered when choosing the metal used for signal tracing and vias [7].

Silicon Interposers

Packages with high requirements on electrical performance can implement a silicon interposer. The interposer aims to shorten the interconnects and through fine pitch implementation increase I/O density. An interposer's main purpose is to run signal traces, but passive components can be built in as well. The key technology to process the silicon wafer into a usable interposer is the TSV. The use of TSVs opens the possibility for designs known as higher dimensional ICs. Devices using TSVs in a silicon interposer are referred to as a 2.5D IC, while use of TSVs through active silicon is called 3D ICs. Other types of higher dimensional ICs exist, but 2.5D and 3D are the most common implementations. The primary downside of using an interposer is the cost increase due to the additional material and processing of silicon [12].

2.2.2 Interconnects

The main goal of the interconnects is to get power and data signals to the ICs on the semiconductor die. The interconnects form onto a so called bonding pad on the die. The bonding pad is a opening in the outer insulation layer on the semiconductor, plated with metal to achieve good contact with other metals. Even though the main purpose of the interconnects is to carry electrical signals, the metal is also a good conductor of heat. This aids thermals by providing a low resistance thermal path from die to substrate.

Wire Bonding

The use of wire bonding to connect ICs is the first well established interconnection technology. Two versions of wire bonding exist, namely ball bonding and wedge bonding. The process of forming a ball bond is briefly described below.

The IC die with its bonding pads facing upwards is mounted on the board using either solder or an adhesive. A nozzle fed with a gold or gold alloy wire has been prepared with a ball on the end. The ball is welded to the IC bonding pad using ultrasonic vibrations. With the weld formed, the nozzle extrudes more wire while moving down towards the board's bonding pad. When fastening the bond to the

board enough wire is left to form the gold ball for the next bond [7]. The resulting interconnect is a wire arching from the die to the board.

The wire bonds are formed sequentially making the process slower than other interconnect alternatives. As all wires are required to leave the die along the sides, the possible number of I/Os are limited by the circumference of the die. Use of long bond wires also introduce impedances which affect electrical performance. The benefits of wire bonds are their reliability and cost effectiveness when producing a small number of components [7].

Flip Chip

Flip chip interconnect technology was developed as a way to form higher I/O applications or applications with higher electrical performance requirements. The shorter interconnects compared to wire bonds also bring increased electrical performance. The process of flip chipping is described in the this section.

Before the interconnect can be formed, both the IC and the substrate need to go through preparationary steps. The die is covered in a layer of passivation which insulates the circuitry and protects from oxidation. The bonding pads are prepared using under-bump metalization (UBM). The UBM overlaps the passivation layer, protecting the pad from corrosion while still allowing to conduct the electrical signal. A wetting layer is part of the UBM to help the solder adhere to the pad easier and form a cleaner connection. A similar process is done to the substrate, with a solder mask to insulate the circuitry and surface metallurgy performing similar functions as the UBM.

When all components are ready, the process starts with microbumps (solder bumps) getting attached to the UBM on the die. The solder material for consumer electronics usually consists of an alloy of tin, silver and copper (SAC) while the aerospace industry still allows lead based solders, like PbSn. When bumped, the die is flipped and aligned with the pads on the substrate. The die and substrate are heated, reflowing the solder bumps until the interconnects are formed [7].

Aligning the solder bumps on a die with the bond pads on the substrate is a difficult part of the packaging process of flip chips. When reflowing the solder bumps, the capillary forces in the solder along with the surface tension helps align the die correctly to the pads below [13]. With a higher number of solder bumps the total forces are greater, further assisting the alignment. With low I/O density the alignment becomes harder and makes for a more complicated packaging process.

To assist the interconnect stability, the additional process of underfilling may be used. Underfill is a polymer applied below the die in between the microbumps. Its purpose is to help redistribute mechanical stresses throughout the connection. The underfill is very helpful when flip chipping on organic substrates, but for ceramic or silicon boards with coefficient of thermal expansion (CTE) similar to silicon it is not always necessary. While the underfill material conducts heat better than air, the impact of a high thermally conductive underfill is reduced when the flip chip features a small pitch [14].

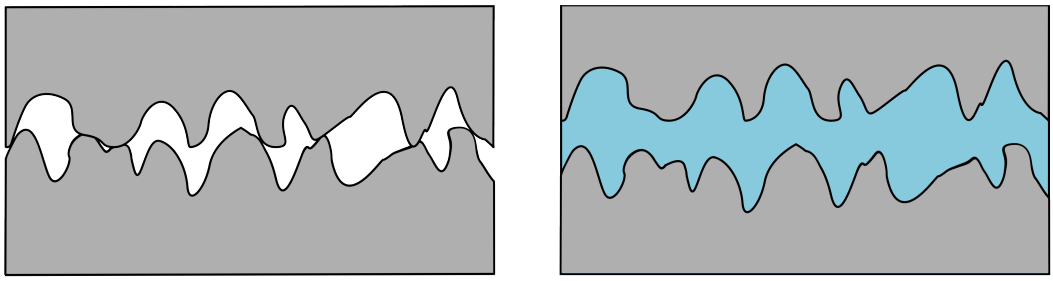


Figure 2.5: Surface roughness create cavities at material interfaces. The cavities can be filled through use of a TIM.

Tin Whiskers

Solder used for electronics packaging today are commonly lead free alternatives. Instead of lead, high amounts of tin is used for solder. This introduces the risk for building tin whiskers. A tin whisker is a stress relief mechanism seen in alloys with high tin concentration. When put under stress, the metal induces tin crystal growth. During continuous stress the crystal may grow several millimeters long. Should the whisker make contact with another interconnect an electrical short is formed, potentially making the entire component faulty. The probability of tin whiskers forming may be increased in space due to the low gravity and pressure [15].

Due to the risk of tin whiskers shorting components, the aerospace industry is one of few industries that still use lead based solders. The possibilities of tin whiskers for flip chip applications can be reduced by using a good underfill. Shan et al. studied tin whisker growth and corrosion of microbumps in components stored over a six month period. Use of an epoxy underfill was shown to significantly reduce the possibilities of tin whiskers forming compared to using no underfill or other underfill alternatives like polyurethane [16].

2.2.3 TIMs and Adhesives

Thermal interface materials (TIMs) are used to reduce contact resistances over surface interfaces. Surface roughness of the materials create microscopic air pockets between them. Considering the thermal resistance seen in equation 2.2, these air pockets effectively reduce the area of contact, increasing the resistance across the interface. The TIM aims to fill the pockets, increasing the contact area and thereby reducing thermal resistance. Figure 2.5 shows how the TIM fills air gaps between two surfaces.

Even though use of a TIM increases the number of interfaces, and thereby the number of contact resistances, the total thermal resistance is reduced. This is due to the better contact area on both interfaces as well as the thermal conductivity of the TIM which is usually magnitudes better than that of air. The bond line thickness (BLT) also plays in important role as the average distance the heat needs to traverse through the TIM. The impact of a thin BLT has been shown to have

similar importance to thermal performance as the material selection [17]. To keep the thermal resistance low, the BLT is aimed to be as thin as possible while still effectively filling the gaps between surfaces.

Due to application issues, voids can be formed or the TIM can experience shrinkage. The reduced contact area will then reduce the effectiveness of the TIM. Experiments of Li et al. produced increased thermal resistance when contact area was reduced [18]. In a similar study, Yan et al. showed how lower contact area could increase junction temperatures [19]. Additionally, proper coverage of the TIM is more important closer to the heat generating component [20].

The most common TIMs consist of a polymer together with filler particles. These filler particles are made from highly thermally conductive materials that form a good thermal path through the TIM. The final thermal conductivity of the material is impacted by the filler type, size, amount and if any surface treatment has been performed [21]. The polymer essentially serves as a carrier to put the fillers in position and keep them in place during operation. The TIM will have very different characteristics dependent on the polymer used [22].

A very useful version of TIM is the thermally conductive adhesive. An epoxy resin with conductive fillers can both aid with mechanical fastening and stability as well as thermal management. The choice of epoxy and filler will depend on the package requirements. An important consideration, however, is if the adhesive is allowed to be electrically conductive or not. In general, the fillers with the best thermal conductivities are also electrically conductive. For some applications this may not be an issue, but for others it may increase the risk of electrical shorts in the package.

2.2.4 Encapsulation

The semiconductor die is a very sensitive component. The package encapsulation protects the delicate ICs from the environmental disturbances such as radiation, dust particles or corrosive elements. Depending on the form of encapsulation it can also act as a heat spreader. This greatly helps with the dissipation of heat generated inside the package.

Molded plastics

The main benefit of using a molded plastic for encapsulation is the production cost. It is reliable enough for many of the semiconductor applications today. Yet, the materials are cheap and many components can be manufactured in parallel. For simpler components that do not generate a lot of heat, the plastic encapsulation is sufficient for thermal management despite the low thermal conductivity.

The most common method of manufacturing plastic molds is transfer molding. The mold is formed to hold the IC and substrate in place with a cavity to form the encapsulation. An epoxy compound is placed in a transfer pot beside the mold and heated until reaching the desired viscosity. By increasing the pressure in the transfer pot, the epoxy is pushed through a runner to fill the mold around the IC. The air occupying the mold escapes through vents in the mold. In large scale production

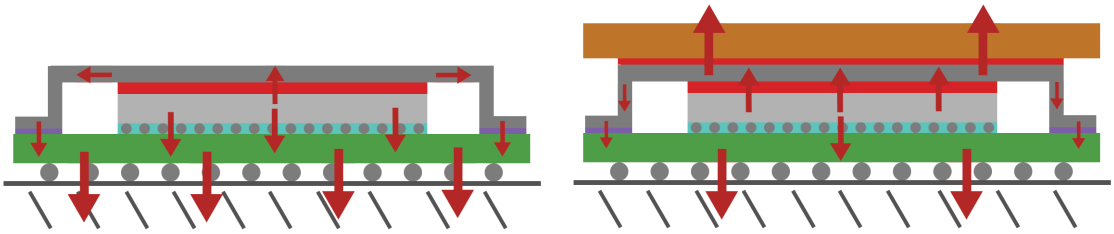


Figure 2.6: Two examples of thermal paths for a lidded package. The left package dissipates heat through the substrate. The right package dissipates some heat through the substrate but also through a dedicated heat sink on top of the lid.

a single mold can hold many components each with their own runner connected to the transfer pot allowing to form multiple encapsulations at a time. When the mold has been filled pressure is increased further to minimize voids in the epoxy. The pressure stays high until the compound has cured. The newly formed packages are removed, the mold is cleaned of residue and is then ready for the next batch.

The plastics used for encapsulation have poor thermal properties for electronics packaging. The CTE does not match the CTE of silicon, and thermal conductivity is low, trapping heat with the die. To resolve these issues fillers are mixed in with the compound. The fillers can be made form many different materials, but a common choice is silica, SiO_2, because it is electrically insulating. Using different sizes of filler particles allows for higher ratio of filler, further improving the thermal conductivity of the mold. At a filler ratio of 90% by weight, thermal conductivities of 3.05-3.62 W/mK were achieved [23]. Adding fillers could alter other properties of the epoxy, which may change the demands of the manufacturing process.

Metal lids

Devices made for difficult environments such as those in the aerospace industry may need a more reliable package. Using a metal lid instead of plastic overmolds results in increased stability, lower absorption of water and corrosive substances, and better thermal conductivity from the die. Through use of a TIM, the die can be connected to the metal lid, forming alternate thermal paths for heat to dissipate through. The higher thermal conductivity of metal compared to plastic encapsulations increase the viability of placing a heat sink on top of the package. The additional heat sink would reduce the amount of heat that needs to pass through the substrate. The thermal path of a lidded BGA with and without heat sink is shown in figure 2.6.

The lidded packages comes in hermetically sealed and non-hermetically sealed variants. Hermetical sealing is used to create highly reliable packages that do not allow any moisture or gasses to leave nor enter the package cavity. A hermetic seal can not be achieved with organic materials in either substrate or lid adhesive. A ceramic substrate is required, and the lid has to be fastened through a glass seal, soldering

or welding [7].

The lid itself can be made from many different metals and alloys. Commonly used are copper, aluminum, Alloy 42 (nickel-iron alloy), and Kovar (nickel-iron-cobalt alloy). If the lid is to be fastened by soldering, the solder used should have a high enough melting point to stay solid during the soldering of the BGA to the PWB.

2.2.5 Reducing Package Formfactor

One of the main purposes of pairing silicon dice into a SIP is to achieve a smaller form factor. After exhausting the traditional packaging techniques more intricate methods are required to further reduce package size. The following section describes a few techniques to minimize the area occupied by the dice, leaving room for other components in the package or allowing for a smaller package all together.

Dual Sided Die Mounting

A simple way to increase silicon density of a package is to utilize more of the available substrate. Commonly, the die would be confined to the top side of the substrate. Through double sided molding, a package can be made with dice and plastic overmold on both sides. A sufficient stand off height is required to form good interconnects despite the additional thickness of the package [24]. With dice on the underside of the substrate, I/O possibilities become limited. Therefore, this technology is best applied for packages with lower I/O requirements, but with high processing needs.

Panel Level Embedded Dice

Traditional SIP packaging connects the dice on top of a substrate, which in turn forms the package. Panel level embedding refers to a process that encapsulates one or more dice into the substrate itself. The technology utilizes copper pillars and polymers to form a substrate frame where a die can be inserted. The frame is limited to a 10 $\times$ 10 mm area and a depth of 400 μm. The die is placed into the frame with an adhesive tape, and then fastened to the substrate with build-up film. The adhesive film is then removed, exposing the die's bonding pads. The interconnects are formed simultaneously as the substrate signal traces. Additional substrate layers may then be added as needed.

For better thermal management, additional copper plating can be used as a heat spreader on the backside of the die. Thermal vias connected to the heat spreader aid the heat dissipation through any additional substrate layers. When researching panel level embedding of a power converter module, the embedded die showed lower temperatures compared to traditional packaging methods [25].

Die Stacking Using TSVs

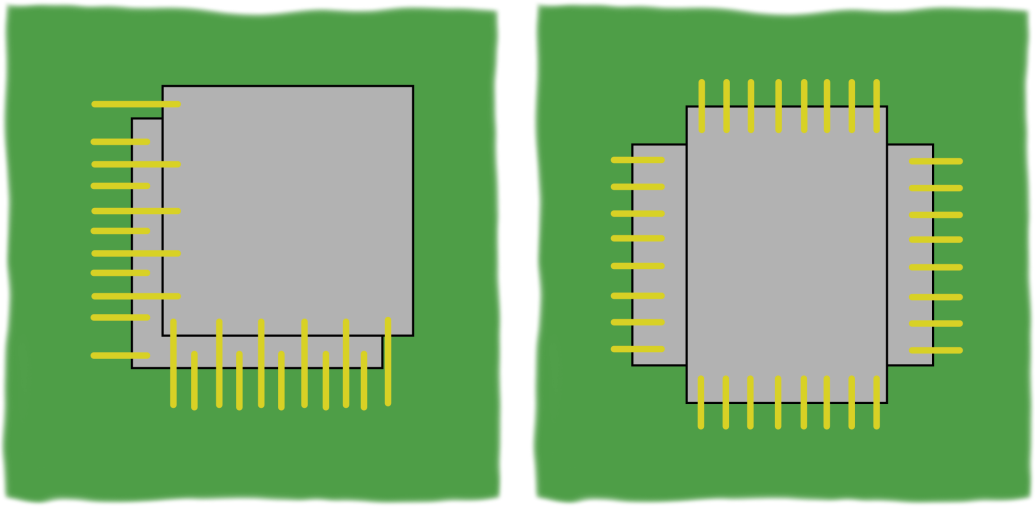
Applying the technology of TSVs on IC dice allows for die stacking and connecting the signals through other active ICs. Use of multiple layers of active ICs is referred to as 3D packaging. This process enables compact designs with many dice

occupying a small area as well as improves the electrical performance by means of shorter interconnects. The signals from one die are aligned to the TSVs of another through redistribution layers. The dice are then soldered together with microbumps similarly to flip chip. All interconnects eventually pass through the bottom die with high routing density. The high routing requirements is often handled by using an interposer to scale the connections to the substrate [7].

The temperatures in a 3D implementation will be higher than if the dice were laid out side by side. The thermal path of the stack forces heat from one die to travel through another to reach a heat sink. This hinders 3D stacking to be a viable option for multiple high performance dice. More commonly, 3D implementations are used to decrease the footprint of memories.

Die Stacking Using Wire Bonds

Stacking of wire bonded dice is also possible. Even if the dice are of the same size, they can be placed with an offset to expose bonding pads at the edge of the die. If the dice have different width than length with bonding pads along the shorter edges, their orientation can be alternated before placement to expose the pads. These methods are showcased in Figure 2.7.



(a) Stacking of wire bonded dice using offset.

(b) Stacking of wire bonded dice using alternating orientation.

Figure 2.7: Two methods of stacking wire bonded dice with bonding pads along the edges of the dice.

If the bond pads can not be exposed through use of either of the previously mentioned techniques, film over wire (FOW) can be utilized to achieve stacked wire bonded dice. FOW uses a non-conductive adhesive film to attach the top die and bottom die, with the bonding wires absorbed into the adhesive film.

To manufacture a FOW stack, the adhesive film is attached to the wafer before it is cut into separate dice. The first die of the stack is attached and wire bonded traditionally. The following dice contain the adhesive film, and are placed on top of

the already wire bonded die. The existing wire bonds cut through the adhesive film embedding themselves within. The newly added die can then be wire bonded. The result is a fully wire bonded die stack with the same footprint as a single die [26].

Choosing materials for FOW is crucial. The adhesive film can not be electrically conductive due to the direct contact with bond wires. Additionally, the adhesive should be soft enough to not deform the wire bonds during placement. Chung et al. showed that FOW can potentially be much gentler on the wire bonds compared to other methods using die attach film [27].

2.3 Simulation and model

The software used for this project is Icepak from Ansys Inc.. This particular program fit the thesis well since it could handle all of the steps needed for the project. This includes simple CAD modeling, mesh generation, simulation and post-processing. The following section outlines the underlying theory, modeling options, quality control and post processing of the simulation[28].

The way heat dissipates from a source towards its surroundings often behaves similarly to fluid movements. This behavior allows modeling heat flow using computational fluid dynamics (CFD) simulations. For simulating thermal conduction, Icepak utilizes the ANSYS Fluent solver to find a solution to the energy conservation equation given in equation 2.4

$$\frac{\partial}{\partial t}(\rho h) = \nabla \cdot (k * \nabla T) + S_h \tag{2.4}$$

The left side of the equation represents the rate of change for energy in a set volume. The right hand side is the heat flux density based on Fourier's law from equation 2.1. The source term S_h is the addition of the heat generated inside the volume itself. The sensible enthalpy h is dependent on the specific heat capacity of the material as well as current and ambient temperatures according to equation 2.5.

$$h = \int_{T_{\text{amb}}}^{T} c_p \, dT \tag{2.5}$$

When density and specific heat capacity remain constant across temperature and time the only way to balance the left hand side is through a change in temperature. To create boundary conditions for the energy conservation equation, the user can either define a heat flux in or out of the system, or adjust the source term for particular volumes.

2.3.1 Finite Volume Method

Solving a large number of differential equations gets computationally intensive. Through a process called discretization the differential equations of CFD can be reduced to linear algebraic equations (LAEs) which are much simpler to solve in large quantities. One approach to discretization is the finite volume method (FVM) [29].

FVM begins by dividing the space into a grid of smaller increments called control volumes (CVs). The temperature at the center point P of a CV is decided by its internal energy. By integrating the energy conservation equation from equation 2.4 over the CV and applying Gauss' divergence theorem, the discrete equation for the temperature at P is given as equation 2.6.

$$a_P T_P = \sum_{nb} (a_{nb} T_{nb}) + S_P \tag{2.6}$$

The suffix nb represents the neighboring CVs. The temperature at P can be seen as dependent on the temperature of the neighboring CV center points added to the heat generated inside the CV itself. The constants $a_{p/nb}$ are the coefficients of the LAE for each respective CV. Subtracting each side by $a_p T_p$ and generating the same equation for every CV results in an equation system. Equation 2.7 shows the equation system expressed in matrix form.

$$\begin{bmatrix} a_{11} & a_{12} & ... & a_{1n} \\ a_{21} & a_{22} & ... & a_{2n} \\ \vdots & & & \\ a_{n1} & a_{n2} & ... & a_{nn} \end{bmatrix} * \begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_n \end{bmatrix} + \begin{bmatrix} S_1 \\ S_2 \\ \vdots \\ S_n \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{2.7}$$

The equation system contains one temperature T at the center of every CV in the grid. For energy conservation to be satisfied the CFD solver has to find the temperature for all CVs to satisfy the equation system.

Residuals and Convergence

If the solver finds the temperatures resulting in all LAEs being equal to zero, the solution is said to be fully converged. Before reaching convergence, the LAEs output non-zero results called residuals. The presence of residuals means that energy conservation is not being satisfied. They are errors caused by poor approximations of the temperatures by the solver. Based on the formulation of equation 2.7, the residuals r would be given by

$$\begin{bmatrix} a_{11} & a_{12} & ... & a_{1n} \\ a_{21} & a_{22} & ... & a_{2n} \\ \vdots & & & \\ a_{n1} & a_{n2} & ... & a_{nn} \end{bmatrix} * \begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_n \end{bmatrix} + \begin{bmatrix} S_1 \\ S_2 \\ \vdots \\ S_n \end{bmatrix} = \begin{bmatrix} r_1 \\ r_2 \\ \vdots \\ r_n \end{bmatrix} \tag{2.8}$$

Despite the lower computational requirements of LAEs, a FVM grid can contain millions of elements that all need to be balanced to reach convergence. For large simulations this leads to valuable computational time spent to marginally increase the accuracy of the solution. Through the residuals the user may define an acceptable margin of error. When residuals are small enough to be within the margin the solutions is deemed to be sufficiently converged and the solver can move on to the next timestep.

Simply relying on the size of the residual to judge convergence could be misleading. Comparing two simulations with high and low respective energy inputs, the same magnitude of residual may produce significantly deviating results for the low energy simulation, while the high energy simulation could be considered to be converged. In order to equalize the convergence criteria the residuals are processed through scaling. In Icepak, the residuals are scaled according to equation 2.9

$$R^{\varphi} = \frac{\sum_{grid} |r_P|}{\sum_{grid} |a_P T_P|} \tag{2.9}$$

The sum of the residuals from all CVs in the grid is divided by sum of the temperatures of all CVs multiplied by their respective LAE coefficient. In other words, the total error is divided by the total energy in the entire grid [30].

2.3.2 Model building

Icepak provides a CAD tool to generate a model for simulation. This section aims to provide an overview of the possibilities for creating geometries in Icepak as well as what parameters are needed by the program in order to perform the thermal simulation.

Geometry Definition

The modeling process begins by defining the spacial boundaries of the simulation, inside of which the model will be placed. The defined space is referred to as the cabinet. All of the volume in the cabinet that are not occupied by a defined geometry at the time of simulation start will be filled with a "default fluid". Icepak sets this default fluid to air, but it can be changed by the user to something else.

Simple geometries, called blocks, can be added to the model by defining start- and end-points in the coordinate system. Possible shapes of "blocks" are rectangular prisms, cylinders, and spheroids. If more complex geometries are desired, existing CAD files can also be imported. The thermal properties of the geometries are chosen through selection of a material to inhabit the geometry. The selection can be either a solid material or a fluid material. Surface conditions related to flow and radiation are chosen through a surface material. Finally, the heat generated throughout the geometry is defined either by selecting a wattage or through setting a fixed temperature at a surface or in a volume.

Object Priority

If two or more objects have intersecting surfaces or volumes, the software uses a number named object priority to decide which block will inhabit the intersecting areas. The larger the number, the higher priority the block has. A simple example of how to use object priority to control the model is shown in figure 2.8.

Object priority works the same way for 2D objects, meaning a plate can be intersected by another plate and Icepak will use priority to find which conditions will

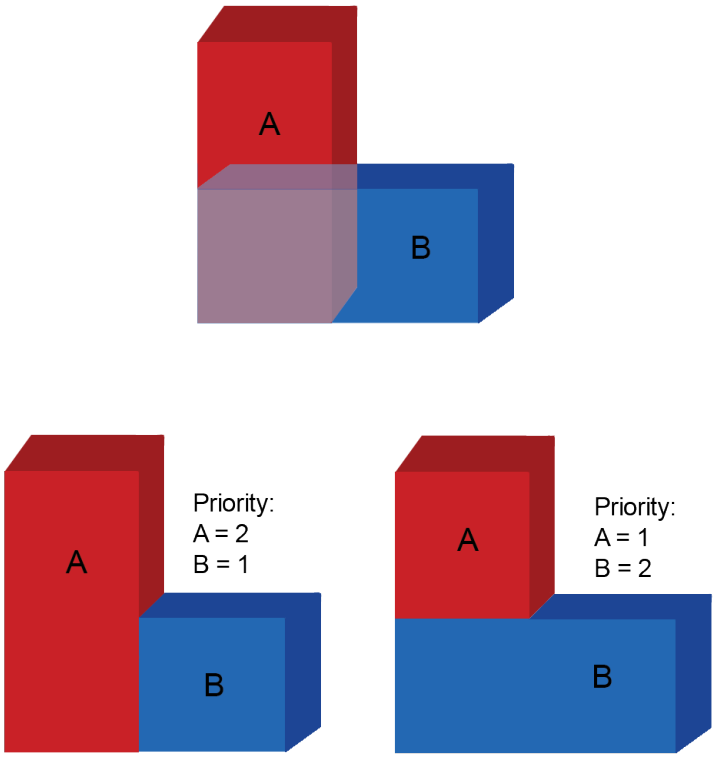


Figure 2.8: An example showing how mesh priority is used to decide material properties of overlapping geometries in Icepak.

apply in the area. 2D objects do however take priority over 3D objects, meaning all contact resistances or heat sources are applied before generating any other blocks.

Material Properties

Icepack provides a stock materials library. The library contains many examples of common materials used in electronics packaging. Users are also able to customize a material by modifying the existing materials or by defining a completely new material. To define a solid material in Icepak, the following properties are needed:

- Density (kg/m^3)
- Specific heat capacity (J/kgK)
- Thermal conductivity (W/mK)

These properties are all needed to solve for energy conservation in equation 2.4.

The simplest definition format handles all properties as constants. To create a more realistic model, properties can be defined to instead be changing dependent on the temperature. This could be done either as a single linear function, a piecewise linear function, or a piecewise constant function. The user defining such a function should consider not only what material they are making but also what temperature range the simulation is expected to span.

Additionally, thermal conductivity may not be equal in all directions of a material. A material can be defined to have an orthotropic thermal conduction, meaning that the thermal conductivity is scaled by a different factor for each axis of the coordinate system.

2.3.3 Meshing

The geometries defined in previous steps are split up into smaller CVs through a process called meshing. During meshing, all shapes are approximated by a discrete number of simpler volumes. Icepak recommends the use of their included unstructured, hex-dominant meshing tool. The cells generated by this type of mesher takes on two shapes, either a rectangular prism or a pyramid. The size of the average CV indicates if the mesh is fine or coarse. A fine mesh can be used to better approximate the geometries and generate smoother transitions between volumes. The finer mesh does however require more computations, increasing simulation runtime. A good mesh should therefore be just fine enough to accurately represent the geometries at the required level of detail, but coarse enough to reduce computational efforts.

To help the tool create a good mesh, the user can define some parameters. Many of the default settings are good enough, but sometimes extra attention is needed at the model extremes. This means limiting the maximum size of the cells in each respective direction, as well as defining the minimum gap the mesher needs to handle. By limiting the maximum size the user is able to enforce a certain level of detail in an area. The minimum gap is required as the mesher could otherwise optimize small spaces too much, making the solver consider the gaps as solid surfaces and thus not calculating any flow through the gaps.

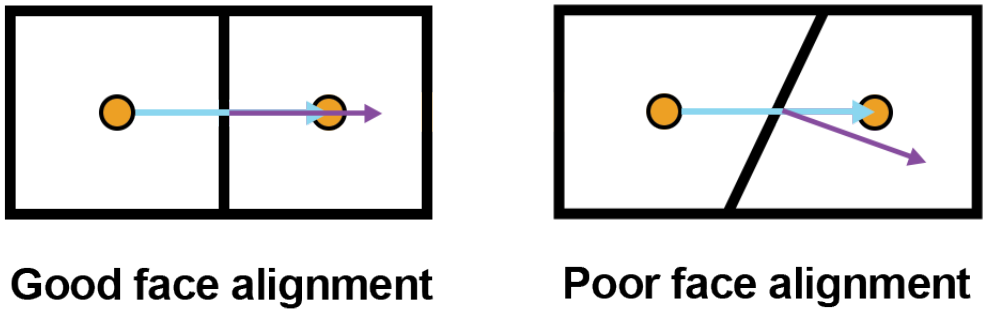


Figure 2.9: Examples of mesh cells with good face alignment compared with mesh cells with poor face alignment.

Mesh Quality

Generating a quality mesh is a crucial step in performing a good simulation. According to a lecture from ANSYS Introduction to Icepak [31], the quality of the mesh can be measured by evaluating three factors of each individual CV:

- Volume
- Face alignment
- Skewness

The simplest factor to determine is volume. The only real criteria is that no CV has a negative volume, as this would indicate a large deformation of surrounding CVs. Smaller issues can arise from adjacent CVs having a large difference in volume.

Face alignment refers to the orientation of the CVs surrounding surfaces compared to the position of adjacent CVs. The face alignment is found by calculating the angle between a vector from one CV center to another and the normal of the surface connecting the two CVs. Figure 2.9 shows an example of high quality face alignment compared to poor quality face alignment. The face alignment quality is normalized, with 0 meaning very poor quality and 1 meaning excellent quality.

Lastly, skewness refers to general deformity of a CV. The target shapes are either rectangular prisms or pyramids, and the deviance from these shapes are measured by comparing angles of the surfaces and length of the sides. Figure 2.10 shows an example of high quality skewness compared to poor quality skewness. Again, the skewness is normalized, with 0 meaning poor quality and 1 meaning excellent quality.

2.3.4 Steady-State or Transient Simulation

Icepak allows for the thermal analysis to be performed in either steady state or transient mode. The difference between the two is how the solver handles time.

For steady state solutions the solver evaluates the temperatures when the system has reached thermal equilibrium. For a linear steady state solution, all model parameters

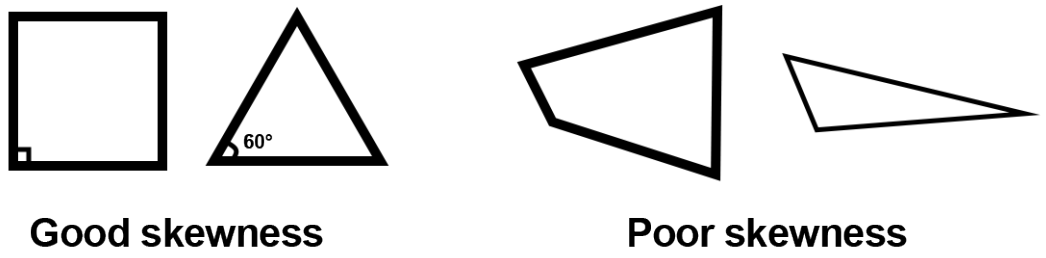


Figure 2.10: Examples of mesh cells with good skewness compared with mesh cells with poor skewness.

are to remain constant through the entire analysis. A non-linear solution could have interdependent parameters, for example a thermal conductivity or specific heat capacity that is dependent on the temperature of the material. Most importantly, no parameters should change dependent on the time passed. A steady state solution only needs to converge once, and will require much less computational resources than a transient solution would.

If, however, some parameter were dependent on time, i.e. a heat source changing as a one time event, or alternating in a cyclical pattern, transient simulation would be required. A transient solution also allows to observe how temperature changes and transfers from initial conditions throughout time, compared to the steady state. Additionally, when no more time dependent changes are made the transient solution would approach steady state as time continues towards infinity.

Other than the convergence criteria, the transient solution requires the user to define some additional parameters, namely start- and end-times, timestep and iterations per timestep. The start- and end-times defines the time window observed by the solution. The timestep tells the simulation what accuracy is needed in respect to time based events. With time dependent changes in the model the timestep should be selected very carefully, but when going for steady state it has less importance. Iterations per timestep sets a limit to how many iterations the solver is allowed to run before being required to abandon further attempts at convergence for this timestep and move on to the next.

Finding appropriate time limits and timestep is key for a high quality transient simulation. The timestep should be small enough to capture the necessary amount of detail in the solution. This detail could refer to the periodic rise and fall of temperatures or the temperature gradient changing through small objects. On the other hand, more computational resources are required for a smaller timestep, as more equations need to be solved in order to reach the simulation end-time. When looking for thermal equilibrium through transient simulation, the end-time should be large enough to allow the system to reach steady state. The timestep can also be large, assuming the intricate developments in individual objects are not of interest.

2.3.5 Post Processing

Since we are only interested in temperature, the post processing alternatives in Icepak are sufficient for our case. The temperature can be examined in a few different ways. This work makes use of the following three: History plot, a graph of the temperature at a certain point over time, Variance plot, a graph showing the temperature along a line through space, and finally Plane cut and Object face, which shows a temperature gradient either as a cross section along one of the axis, or at the surfaces of a select object in the model.

3

Methods

This chapter presents the methodology used for gathering information needed to produce well motivated designs. The chapter also describes two methods used to estimate material properties when the data could not be found elsewhere. The process used to produce and iterate simulation models is also explained.

3.1 Literature Study

The many interdependent aspects of SIP design makes it difficult to practically try out all combinations of materials and technologies. Therefore, a literature study was employed to find suitable technologies and research their applications. Most importantly, sometimes one technology is reliant on others in order to function. On the other hand, a certain technology could limit the choices later down the line. Understanding the technology dependencies and the possible mutual exclusions is key to making thorough design choices.

The study consisted of academic papers, industrial publications and datasheets. The main sources for the literature were the Chalmers Library, their associated databases, and Gaisler and their suppliers.

Additionally, the documentation of Icepak as well as some online provided lectures gave good insights into the model and meshing setup as well as simulation settings for the projects use case.

3.2 Material Property Approximation

Not all material properties needed for simulation were readily available. For many materials, a combination of product data sheets and academic papers was used to fully define the material. For certain composites, however, even these methods fell short. These cases required an approximation from the primary materials used in the composite materials.

The density of a compound can be found through the densities of its parts if the ratio between the two materials is known. With a known weight ratio this is done through the following equation.

$$\rho_c = \frac{\rho_1 \rho_2}{w\rho_2 + (1-w)\rho_1} \tag{3.1}$$

Here ρ_c is the density of the compound, ρ_1 the density of material 1, ρ_2 the density of material 2, and w is the weight percentage of material 1.

Specific heat capacity is more complicated, and no regularly used equation could be found. Therefore, the compound used the values of its materials weighted by their respective percentages. The weighting was done according to the following equation

$$c_{pc} = wc_{p1} + (1 - w)c_{p2} \tag{3.2}$$

Here c_{pc} is the specific heat capacity of the compound, w is the weight percentage of material 1, c_{p1} is the specific heat capacity of material 1, and c_{p2} is the specific heat capacity of material 2.

In the few cases where no good sources could be found, the data selections were guided by the engineering intuition and experience of my supervisors and the technical advisors they put me in contact with. This was done instead of conducting further research due to the constraints placed on the thesis work, and could be grounds for further studies.

3.3 Iterative Model Design Process

Generation of models for simulation was done through an iterative design process. The strengths of this methodology lies in the fast feedback of new data into the next generation of the design. The iterative process also allows to identify the impact of individual design changes.

The work begun with gathering knowledge about packaging technologies used in the industry or under development. With the acquired knowledge, a suggested design can be made. The design then is used to perform a simulation. The output is put under analysis where the results are evaluated to find potential issues. If the design itself is causing problems it's an indication that more research is needed. If the issue is deemed to be caused by something other than the model geometries or material definition, the same model can be used again while changing either boundary conditions or external simulation settings. When no issues are found during analysis, the output can be considered a valid result and post-processed. A flowchart of the iterative design and simulation process is depicted in figure 3.1.

The iterative process was used to first find simulation settings and check material properties that made for a good representation of a real SIP. The space environment and the boundary conditions of the model also had to be considered. Then, the iterative process focused on improving the accuracy of the model by removing some initial simplifications, and finally designing for better thermal management.

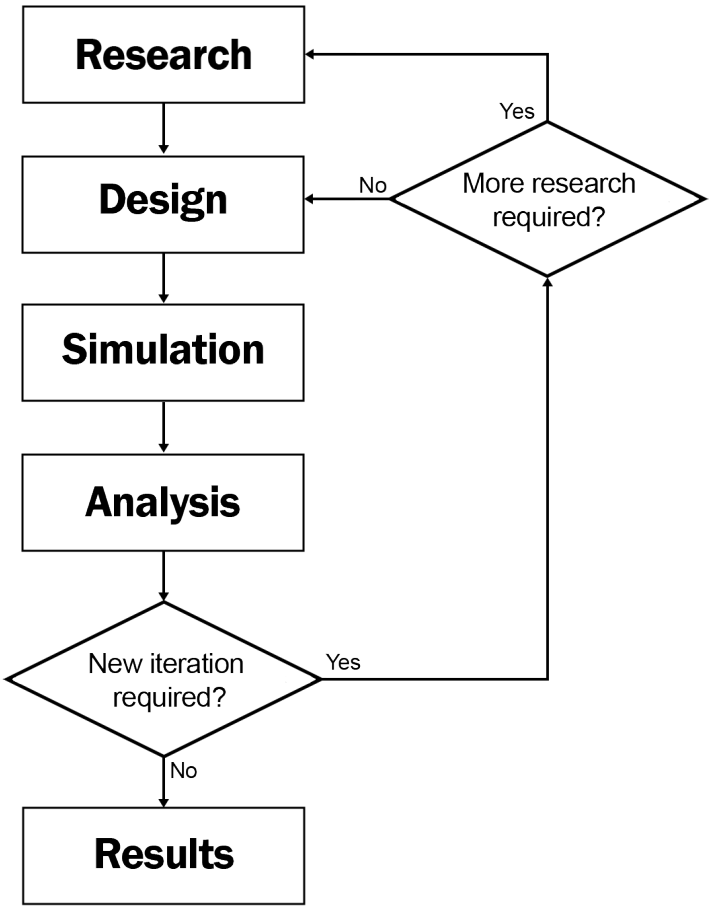


Figure 3.1: A flowchart depicting the iterative process used for model generation.

4

Design

This chapter describes the design and production of the simulation models used for the thesis work. Motivations are presented for technologies, material choices, and other design aspects. The simulation environment in regards to defining boundary conditions as well as transient settings are presented. The models were built one after the other based on the simulation results of the previous iteration, which are presented in the following chapter. The new iteration aims to produce a more accurate representation of the SIP and reaching the thermal targets defined by Gaisler.

4.1 Setup and Baseline

Before producing the first model, some design choices had to be made regarding technologies and materials. This section aims to motivate the different selections made to represent key components. Said components were then combined into the first GR765 SIP model. which acted as a baseline for future models.

4.1.1 Material Selection

To best replicate the materials used for packaging the SIP, the primary way of acquiring material data was through Gaisler and their suppliers. For some components of the SIP, not all the necessary material properties could be found through the same source. For these cases, additional data sheets and papers were researched to complete the material definition. For some materials in the model, the use of Icepak's included library was deemed sufficient for the application. The following section motivates the decision making surrounding some key model components.

Circuit Boards

The material properties of a circuit board will vary greatly dependent on the implementation. For organic boards, the properties rely heavily on the metal concentration. The number of metal layers as well as the vias will all change the board properties. Icepak is able to model the individual layers of the board, making for a very representative simulation. However, the substrate of the package was not designed at the time, and the PWB used to mount the SIP would be designed by the customer. Therefore, little is known about the metal concentration of the circuit

boards involved in the simulation. A representative material is needed to account for both metal and dielectrics of the circuit boards.

Such a material can be found in Icepak's included library. This material does however feature isotropic thermal conductivity. As stated in section 2.2.1, an organic substrate often has different in-plane and cross-plane thermal conductivities. To achieve this, the existing substrate material from Icepak was modified with orthotropic thermal conductivities based on articles.

Solders

Two kinds of solders were prepared for the model: one lead based to lower risk of tin whiskers, and one lead free. The lead based solder used was Sn63Pb37, a tin-lead alloy with 63% tin and 37% lead. For the lead free solder, SAC305 was used instead. The SAC305 alloy consists of 96.5% tin, 3% silver, and 0.5% copper.

Adhesives

Both electrically conductive and non-conductive adhesives were prepared for use in the model. The conductive adhesive Ablestik JM7000 was recommended by a supplier and the non-conductive Ablestik ATB F100E adhesive film was found when researching options for FOW.

The only needed material property listed in the datasheet for JM7000 adhesive was the thermal conductivity. The remaining material properties were calculated based on the available datasheet and an estimation of the filler content of the JM7000 adhesive.

Similarly, the non conductive ATB F100E adhesive gathered properties from multiple data sheets and from calculations based on an estimation of the filler content.

TIMs

Connecting the back side of the GR765 to a metal lid requires an interface material. For this purpose, a graphene based thermal pad was chosen due to the ability to effectively conduct heat over the relatively large gap between the chip and lid. The pad chosen was the GT90PRO from Smart High Tech. The same example pad was used to connect the top of the lid to an external heat sink. The pad was chosen due to the longevity of the pad as well as increased thermal conductivity in comparison with thermally conductive adhesives.

Complete list of material properties

Through the previously stated estimations all needed materials could be defined. Table 4.1 shows the properties used for all materials used to build the models. Properties dependent on temperature and calculated values have been marked respectively.

Table 4.1: Physical properties of the materials and compounds used to create the models.

Component	Material	Density (kg/m^3)	Specific heat capacity (J/kgK)	Thermal conductivity (W/mK)
Semiconductor	Silicon	2330	750*	148
Solder	SAC305	7490[32]	232[33]	58.7[32]
Underfill	Epoxy	1210	1172	0.8
Adhesive	Ablestik JM7000	3870**	410**	1.1[34]
Adhesive	Ablestik ATB F100E	1100[35]	1100**	0.57[36]
Substrate	Metal-dielectric laminate	1900	795	[x y z] [15 3 15][18][37]
Solder	Sn63Pb37	8400[38]	150[38]	50[38]
Overmold	Silica filled epoxy	18	1004	0.63
Thermal pad	SHT GT90PRO	520[39]	740[39]	90[39]
Metal lid	Kovar	8360[40]	460.5[40]	17[40]
Enclosed gas	Nitrogen	1.25	1040.67	0.028*
Cold plate	Copper	8933	380*	387.6

* Average value between 0°C and 150°C.
** Calculated values based on material estimations.

4.1.2 Simulation Environment

The environment of space introduces some unique constraints on the thermal management that would not be present on Earth. The largest difference is the vacuum surrounding the package, unable to remove heat through either conduction or convection. The heat dissipated by radiation would be small, and by request of Gaisler was completely omitted from the simulations. This leaves only conduction through the package itself, and puts a large emphasis on the configuration of the heat sinks. Even one poorly defined aspect of this environment could effect the results of the simulation. The best implementations found are presented in the following section.

Thermal simulation of vacuum

To get a good understanding of the component's behavior in space, the model needs to be adapted to these conditions. Methods for performing thermal simulation of a vacuum environment in Icepak are explained by ANSYS in an online presentation [41]. The presentation features two approaches based on implementing a custom fluid material with similar thermal properties to vacuum. The fluid material approximates a vacuum through the following features:

- High density ($1 \cdot 10^3$ kg/m^3)
- Very high specific heat capacity ($1 \cdot 10^6$ J/kgK)
- Very low thermal conductivity ($1 \cdot 10^{-6}$ W/mK)

The high density and specific heat ensures that a very large amount of heat would have to be added for the material to change temperature, and the low thermal conductivity limits the rate of which heat can be added to the material. The low

conductivity together with exclusion of convection also means that all heat absorbed by the vacuum will stay close to the surface of the heat source. The result is a fluid that will taper off in temperature and quickly return to ambient temperature, even when in contact with very high temperature objects.

When looking for maximum temperatures and heat propagation in a package without any time dependent changes, a steady state solution would usually be enough. However, with this definition of a vacuum the surrounding fluid would be able to absorb a large amount of heat due to the high density and heat capacity. A steady state solution would calculate the values as if the vacuum had absorbed a lot of heat. This does not align with the isolating properties of vacuum that we want to achieve during simulation.

By instead performing a transient simulation, the low thermal conductivity ensures that the custom vacuum material does not absorb a significant amount of heat as the simulation reaches a steady state. This method takes longer to simulate, but generates a better representation of the temperatures in the SIP as less heat is transferred to the surrounding vacuum, more accurately reflecting a real vacuum environment.

Heat sink design

To achieve thermal equilibrium, a boundary condition is needed to remove heat from the system. These conditions should be implemented in a manner that reflects the real thermal paths from the dice towards the larger space vehicle.

As was stated in section 2.1.2, for plastic packages most of the heat will dissipate downwards through the PWB. For metal packages with a cold plate on top, a majority of the heat will instead travel through a TIM and the lid towards the top heat sink. The boundary condition was set through a heat transfer coefficient on the bottom surface of the PWB and top surface of the cold plate.

The heat transfer coefficient will remove heat based on the temperature difference between the surface and ambient temperature, adjusted for area of the surface. The value was set as a constant with respect to both time and temperature. The assumption is that the heat sinks in form of PWB and cold plate are connected to the space vehicle in such a manner that the heat sink takes on ambient temperature. The only limitation to the heat transfer between our simulated system and the space vehicle is thermal contact resistance.

Transient simulation setup

Configuration of the transient settings needs to find the balance between detailed simulation and simulation runtime. The timestep and total simulation time decide what information can be extracted from a simulation. Choosing too small of a timestep or too long simulation time would instead lead to the simulation taking too long to finish.

Initial testing showed that thermal equilibrium was reached in approximately 250 seconds of simulated time. The temperatures increased quickly at first, but slowed

down drastically after around 200 seconds. This behavior indicated that the early states of the simulation would require a smaller timestep to fully reflect the quick changes. After around 200 seconds, the timestep could be increased to reduce the simulation runtime.

The time it takes to reach thermal equilibrium could vary between different models. Increasing the total simulation time ensures that the simulation achieves equilibrium before the simulation end. The total simulation time was decided to be 800 seconds.

4.1.3 Model I: Baseline

The baseline model aims to provide a reference point for future iterations. The model is meant to represent the simplest possible SIP from a manufacturing standpoint. The baseline will also feature some simplifications aimed at lowering simulation runtime.

This section aims to describe how the different components were generated, and how they were grouped for easy use in the models. The same components described here will be reused in future models.

GR765

The GR765 component was created as an assembly of the silicon die, microbumps and underfill. The die was assumed to have dimensions of 12.5 x 12.5 x 0.5 mm. The die was also assumed to generate a total of 14 Watts of heat, which for the base component is set to be uniformly generated throughout the entire silicon die volume.

The GR765 was assumed to have approximately 2000 I/O connections. Using flip chip, an array of 45 x 45 microbumps yields a total of 2025 I/O. The pitch was assumed to be 200 μm. Gaisler provided data on flip chip process using SAC305 lead free solder. This included the dimensions of the microbumps at a diameter of 100 μm and stand off height of 75 μm. Use of a lead free solder for this application was deemed acceptable, as the underfill protects from potential tin whiskers forming and shorting the interconnects. The microbumps were modeled as cylinders, as this is the approximate shape a bump would form after reflow.

The space in between the microbumps is occupied by an underfill material. The underfill covers the entire underside of the die all the way out to the edge. The underfill was implemented as a single block with low mesh priority. The microbumps would be formed first and then the underfill takes up the remaining volume. The material of the underfill was taken from ANSYS standard library. The material is meant to represent an epoxy filled with thermally conductive silica spheres. The existing material was deemed to be a good representation of commonly available materials.

DDR4 Dice

Each DDR4 component was designed as an assembly of the silicon die, and an adhesive. The dimensions of the memory dice was obtained from a datasheet of an

Table 4.2: Thicknesses of different substrate layer types

Layer type	Thickness (μm)
Core	400
First metal	15
Dielectric	30
Second metal	10
Surface insulator	15

exesting memory provided by one of Gaisler's suppliers. The bond pad locations on this particular memory make flip chip interconnects difficult due to alignment issues. This means the memory dice need to be wire bonded.

A conductive adhesive was chosen to fasten the memory dice. Gaisler provided a datasheet of an example adhesive. According to the datasheet, the adhesive should be applied to form a BLT of 25 μm, which was used for the model [34]. The area of the adhesive was made to cover the entire memory die.

The wire bonds intended to connect the memory dice to the substrate were omitted from the model due to complexity. The small shapes required a very fine mesh, which increased simulation runtime to unreasonable lengths for the resources of this thesis.

Substrate

The substrate component was created as an assembly of the circuit board itself and the solder balls of the BGA. The substrate area of 45 x 45 mm^2 was given through one of Gaisler's suppliers. The substrate thickness was found through existing data from suppliers regarding the thickness of signal and dielectric layers, paired with an estimation about how many layers the SIP is expected to have. The thickness of the different kinds of substrate layers are found in table 4.2.

The design is estimated to feature nine layers when including the core. This yields a substrate with one core layer, four metal layers - two first and two second metal, two dielectric layers and two surface insulation layers. The thickness of the substrate is 540 μm according to equation 4.1.

$$400 + 2 \cdot 30 + 2 \cdot 10 + 4 \cdot 15 = 540 \tag{4.1}$$

The example substrate from the supplier was a BGA with 42 rows and 42 columns with a pitch of 1 mm. The solder balls were made to be out of a PbSn solder. Gaisler provided an example of solder balls used by their supplier, which were 0.4 mm in diameter. According to a packaging guide by Intel [42], the combination of 1 mm pitch with 0.4 mm ball diameters should result in a stand off height of 0.3 mm. The solder balls were modeled as cylinders, as they were for the microbumps.

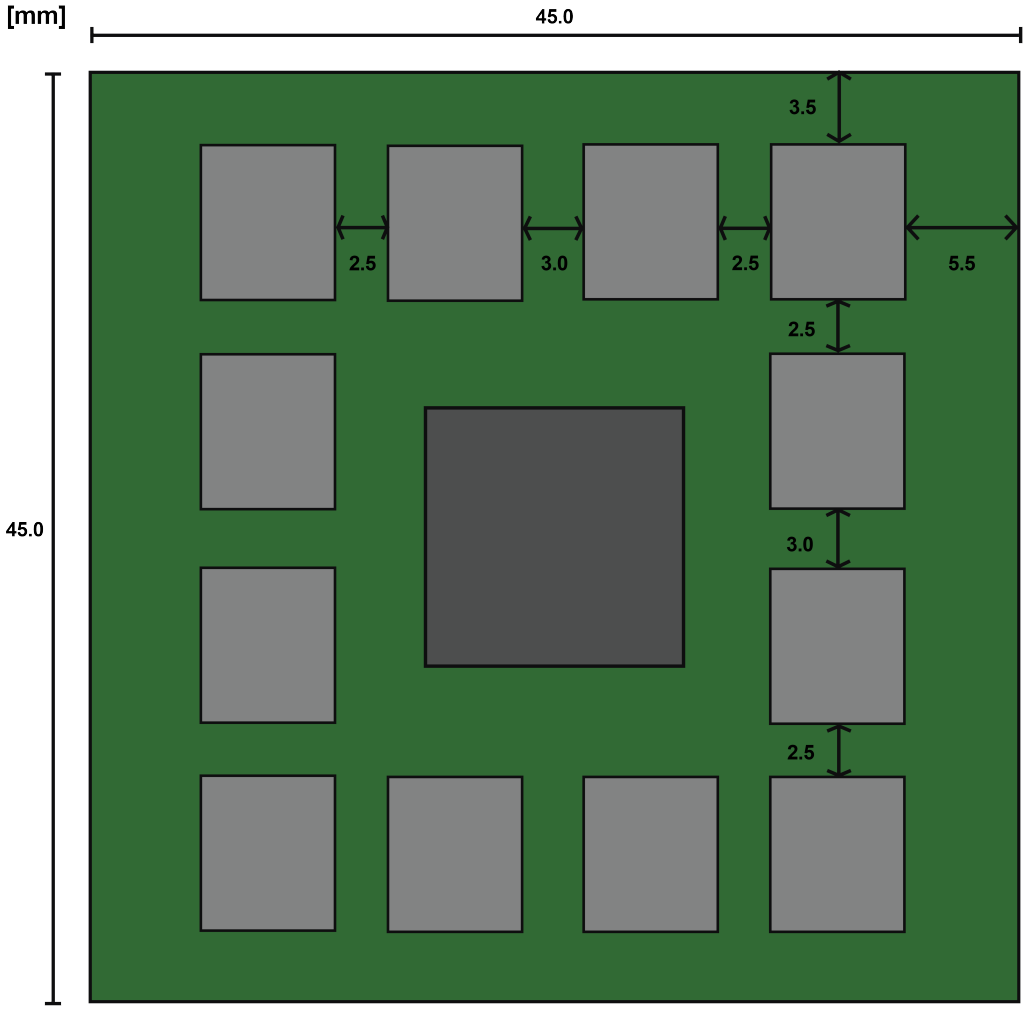


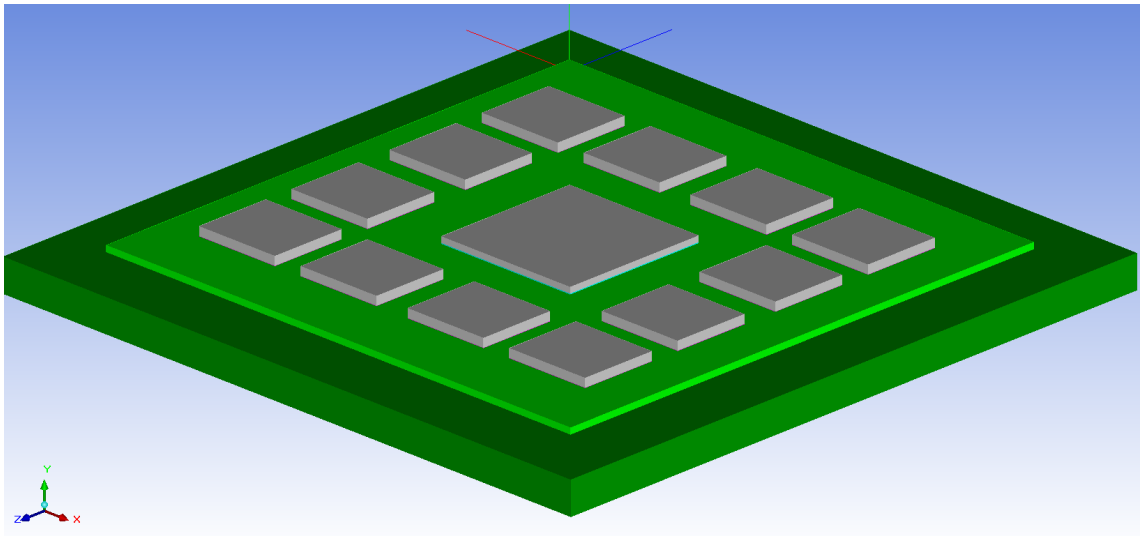
Figure 4.1: A top view of the GR765 and DDR4 dice placements on the package substrate.

Model Assembly

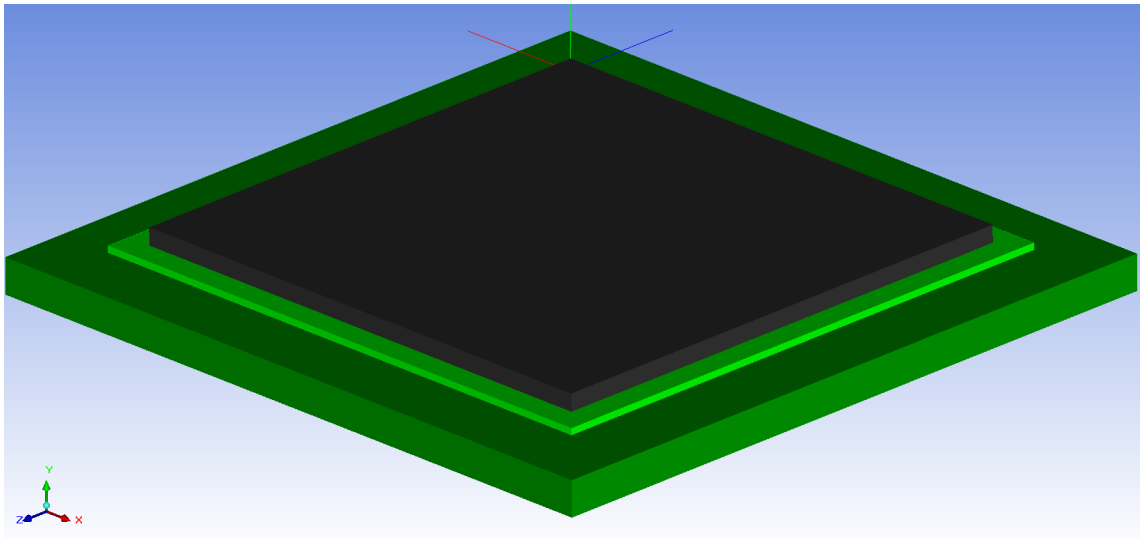
The main heat source, the GR765, is placed in the middle of the organic substrate. According to theory on thermal uniformity, this would allow for the best heat dissipation from the die. The GR765 is then surrounded by 12 memory dice. The memories are spaced from the GR765 to not be heavily affected by the heat from the main die. Distance between memories are meant to accommodate the wire bonds and their bonding pads. The layout of the SIP can be seen in figure 4.1.

As a baseline, this model features plastic encapsulation. The overmold leaves a margin of 2 mm from the substrate edges, and a thickness of 1.36 mm leaves a margin of 0.5 mm to the apex of the wire bonds. The overmold was implemented as a single block with a low meshing priority. The low priority means that other objects are formed before, and the remaining volumes get occupied by the overmold.

The complete SIP model is placed on top of a section of the PWB. The PWB edges extend 5 mm to each side of the substrate. The thickness of the PWB was measured from existing circuit boards in Gaisler's lab at 2.8 mm. The bottom side of the PWB acts as the heat sink of the model. A screenshot of the model can be seen in figure 4.2. The figure also shows the model with the overmold removed, to display the dice placement on the substrate.



(a) The dice placements of Model I in Icepak.



(b) Plastic overmold covering the dice of Model I.

Figure 4.2: An overview of the baseline Model I of the SIP. For figure **(a)** the overmold was made invisible to get a view of the dice placement.

4.2 Non-ideal Model Practices

While Model I works as a point of reference, many assumptions were made during its design that could impact the results of the simulation. Two common simplifications

for heat transfer analysis include ideal contact areas and uniform heat generation. Making a model with these simplifications would yield a lower maximum temperature than what would be expected in a more accurate simulation. The following two models address each respective simplification to understand how large of an impact they have on the thermal developments of the SIP.

The design choices presented in this section were made to generate a model as representative as possible with the available resources. The designs were motivated through a combination of data provided by Gaisler and their suppliers, research papers, and previous experience of experienced engineers.

4.2.1 Model II: Contact Resistances

The thermal simulation will by default assume an ideal contact area between two surfaces. As explained in section 2.2.3, real surfaces have a microscopic roughness reducing the contact between objects. One of the ways to implement non-ideal contact in Icepak is through use of contact resistances. This model aims to investigate how large of an impact contact resistances has on the temperatures of the SIP. If the impact is large enough, the contact resistances should be added to future model iterations for better accuracy.

The contact resistances as well as their method of implementation were provided by one of my technical advisors. The resistance is applied through surface conditions of the defined geometries. The resistances depend on what materials are part of the interface. All interfaces considered are shown in table 4.3.

Table 4.3: Thermal contact resistances for different material interfaces used in Model II.

Interface	Thermal Impedance (Km^2 / W)
Silicon-Metal	$1 \cdot 10^{-6}$
Silicon-Plastic	$1 \cdot 10^{-4}$
Metal-Metal	$1 \cdot 10^{-6}$
Metal-Plastic	$1 \cdot 10^{-4}$
Plastic-Plastic	$1 \cdot 10^{-5}$

The interfaces between solder and circuit board is assumed to be metal-metal connections. This is because the metal interconnects fasten to metalized bonding pads on the circuit boards and die. The resistance of the metal-metal connection is so low due to the good contact area of soldered connections.

Many materials in the model are categorized as plastics, including adhesives, underfill, the overmold and the surface insulation of the substrate and PWB.

4.2.2 Model III: GR765 Hot Spots

The heat generation of a real die is not homogeneous, as assumed in Model I. Through use of preliminary data on power consumption and layout of the GR765,

a simple hot spot model was built. The purpose is to get a more accurate representation of the temperatures of the SIP. The only component changed is the GR765 die. All other aspects of the model are identical.

The die was divided into hot spot regions according to four parts: cores, FPGA, DDR4 PHY, and other. The area of the first three parts was estimated and placed on the die according to an early layout proposal. The fourth part, other, is meant to represent the less dense parts of the IC. The heat generation of each part was dimensioned to be equal to that of the homogeneous version. Table 4.4 shows the heat generation and areas of the respective parts.

Table 4.4: The heat generated and dimensions of different areas of the GR765 hot spot used in Model III.

Part	Heat Generated (W)	Width (mm)	Length (mm)	Area ratio of total die (%)
Cores	10	6.5	9	37.44
FPGA	2	5.7	5.3	19.33
DDR4 PHY	1	6.5	3	12.48
Other	1	-	-	30.75
Total	**14**	**12.5**	**12.5**	**100**

The implementation of the hot spots in the design was done through meshing priority. The hot spot layout used can be seen in Figure 4.3. The individual parts had a higher priority than the other, ensuring their higher power density was used for the applicable CVs. When configuring contact resistances, the model was made to have no contact resistances within the die itself, but features the same contact resistance between die and surrounding materials as the previous model.

4.3 Thermal Target

Electronic components have a thermal limit after which they begin to break down and fail. Component failure can happen in the die itself, in an interconnect, or through mechanical stresses caused by thermal expansion. For this particular SIP, Gaisler aimed to keep temperatures below 125°C throughout the entire package.

The space environment also introduces fluctuations in ambient temperature. When the space vehicle absorbs large amount of radiation, for example when in direct sunlight, the ambient temperatures in the system will rise. The 20°C ambient temperature is useful for comparison to lab work, but in a real applications the surrounding environment could reach higher temperatures. Gaisler provided 55°C as a high ambient temperature reference. The following models aim to improve thermal management through implementation of different packaging techniques. Ideally, the maximum temperatures of the package should not exceed 125°C at an ambient temperature of 55°C.

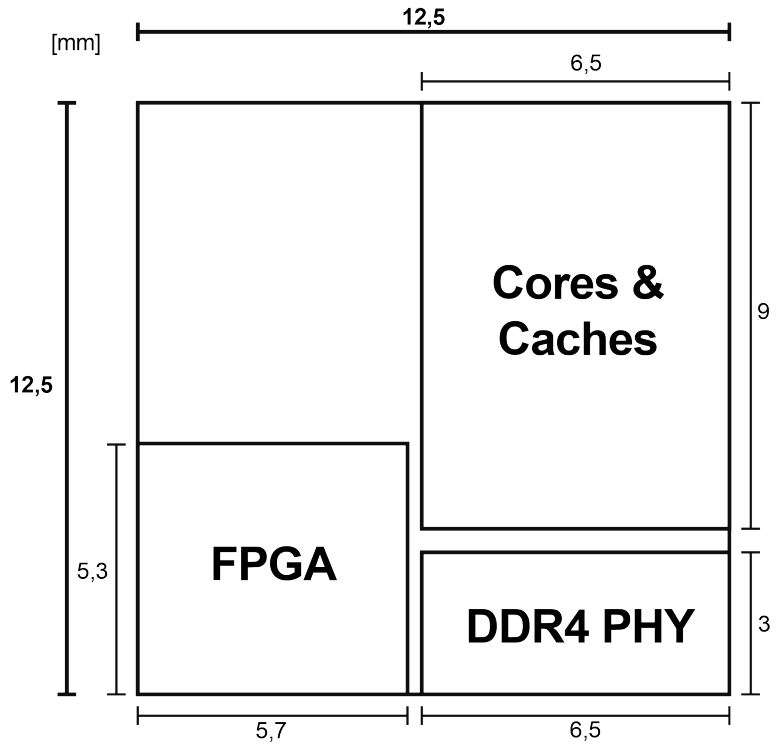


Figure 4.3: The locations of the hot spots on the GR765 used in Model III.

4.3.1 Model IV: Metal Lid

To improve heat dissipation capabilities of the previous models, a metal lid is employed. The thermally insulating plastics in the overmold traps heat by the die. By completely removing the overmold, the plastic can be replaced with a metal lid.

According to one of Gaisler's suppliers, a Kovar lid would most likely be used for this type of component. Available data from the supplier suggests a lid thickness of 380 μm and a height of 2.25 mm above the substrate. The lid is fastened around the outside of the memory dice with the same conductive adhesive used for the memories. The adhesion area of the lid forms a square along the substrate edges. The thickness of the square is kept the same as the rest of the lid at 380 μm, and the width of the square is 2 mm. The implementation of the lid can be seen in figure 4.4.

The GR765 is put into contact with the top lid through a thermal pad. The pad is a form of TIM that is well suited for the somewhat large gap between the top of the die and the underside of the Kovar lid. The pressure from the lid will push the pad together between the two surfaces, providing excellent thermal qualities to the pad. Due to the wire bonded memories, they would be more complicated to connect to the lid. Therefore, they are assumed to only connect to package through the adhesive to the substrate. The remainder of the cavity is filled with nitrogen gas. With organic materials in both the substrate and adhesive the nitrogen will not

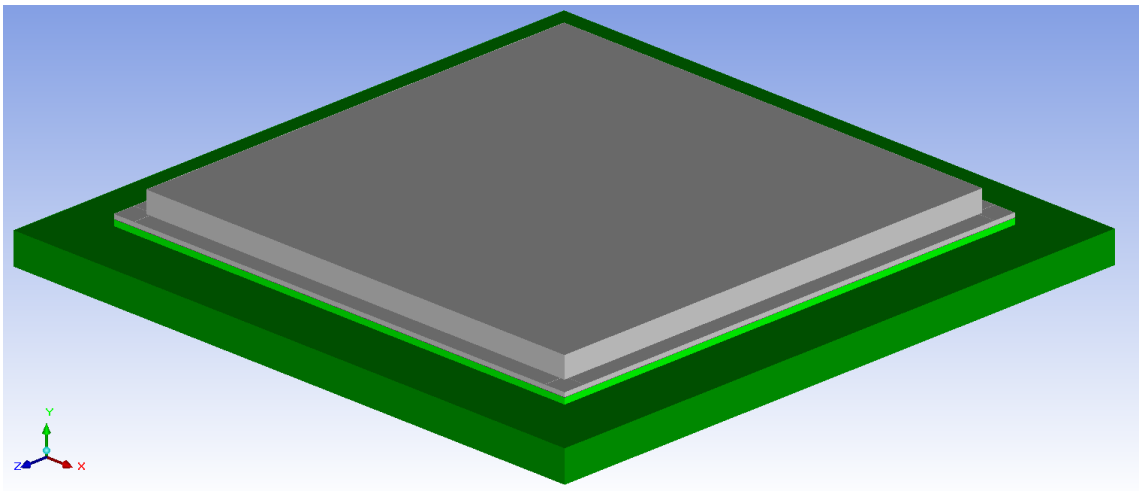


Figure 4.4: An overview of the Kovar lid covering the dice in Model IV. The lid was fastened to the substrate by a thin layer of adhesive.

stay permanently but slowly leak from the package. If a hermetic seal was essential, the package would need to feature different materials and lid attachment methods.

Even without the addition of a top heat sink, the increased thermal conductivity of the encapsulation should lead to faster heat dissipation and thereby lower temperatures compared to the plastic overmold. The lid provides low thermal resistance paths for the heat to travel from the die to the substrate. The GR765 will no longer be covered on all sides, and can only conduct heat through the top and the bottom of the die. The reduced contact area could hinder some heat dissipation, but the increased thermal conductivity is predicted to be more impactful.

4.3.2 Model V: Dedicated Heat Sink

Until this point, the only way for heat to leave the package has been to conduct downwards through the substrate. The metal lid with higher thermal conduction than a plastic overmold allows for the addition of a heat sink on top of the package as well. A dedicated heat sink in this environment would be something like a cold plate aimed at conducting heat towards a larger radiator somewhere else in the system. The cold plate is attached with mounting fixtures connected to the PWB for extra stability. For the simulations, however, these mounting points are deemed out of scope.

The cold plate was implemented as a copper block on top of the package. The block extends 0.5 mm further than the SIP substrate, similarly to the PWB. The thickness of the block was 3 mm. To increase conductivity between the lid and cold plate another instance of the thermal pad was used. The pad covers the entire top of the lid and has a thickness of 200 μm. A side view of the model is shown in figure 4.5.

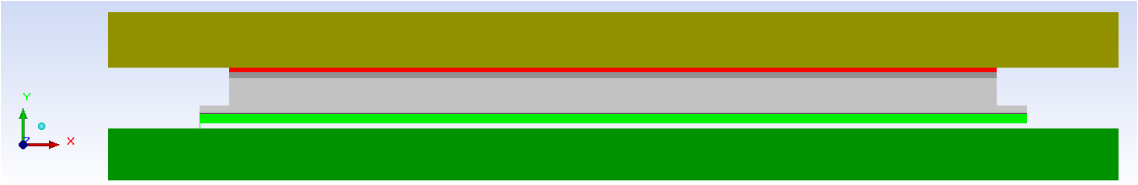


Figure 4.5: A side view of Model V showing the PWB, substrate, metal lid and dedicated heat sink. The lid was connected to the heat sink via a thermal pad.

4.4 Downscaling Form Factor

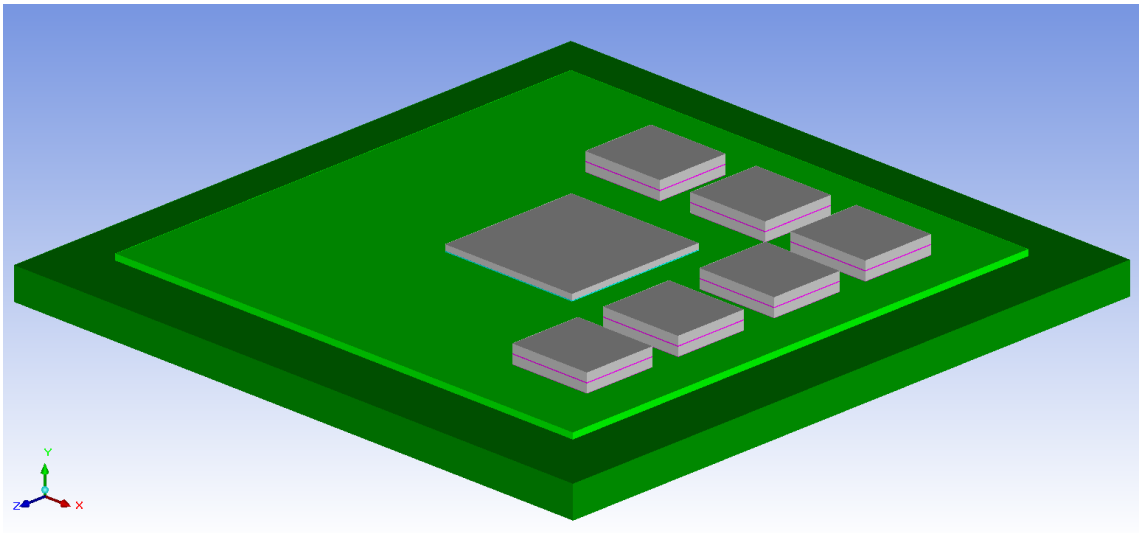
One of the primary benefits of a SIP is the reduced form factor which the technology provides. While this can be achieved in a couple of ways, the method used is limited by the dice and their requirements. For the GR765 SIP, high I/O count excludes for example double sided mounting as the dice would occupy too much space on the underside of the substrate. The GR765 die is too large for panel level packaging, stretching outside the dimensions of the largest possible frame. While memory dice are small enough, their thickness can not fit without significant backgrinding. The following model will instead reduce the form factor through die stacking.

4.4.1 Model VI: Memory Stacking

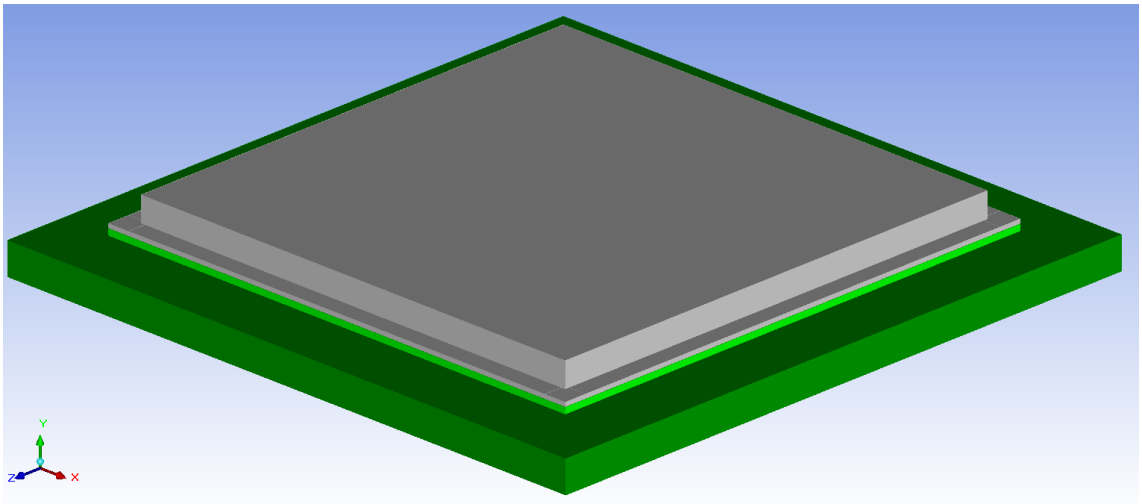
According to the DDR4 memory data sheet, the bonding pads of the memory die are positioned along the middle of the die. The commonly used techniques of offsetting dice or stacking in alternating directions can therefore not be used as the wire bonds need to connect to the middle of the die. The die stack needs to be manufactured through FOW.

The non-conductive adhesive used for FOW is manufactured up to a 80 μm thickness, which is the thickness used for the model. The memories were placed in a total of six stacks, with two memories in each stack. As the preliminary die layout of the GR765 suggests, the DDR4 interface is located in a corner of the die. The DDR4 stacks were placed in the locations closest to that corner of the GR765. It is assumed that there is enough space between the stacks to perform the wire bonds from both dice in each stack.

For an additional margin above the highest points of the wire bonds, the metal lid had to be raised. For a margin of 0.5 mm, the lid is raised by 290 μm. The new lid height above the substrate is 2.54 mm, and the complete package can be seen in figure 4.6. The thermal pad inside the package was adjusted to fit the new lid height. The pad on top of the lid and the cold plate retained their dimensions from the previous model.



(a) The dice placements and stacking with FOW used in Model VI.



(b) A raised metal lid used to cover the dice of Model VI.

Figure 4.6: An overview of Model VI featuring stacked memories using FOW. For figure **(a)** the package lid was made invisible to get a view of the dice placement and memory stacks.

5

Results

Thermal simulation results are shown in this chapter. The results take the form of temperature gradients, as well as temperatures at a few important geometrical points of the different models.

5.1 Model I: Baseline

The placement of detailed temperature measurements is important in order to perform an accurate comparison of the different models. In Figure A.1 of the Appendix, some points of interest have been marked out in the model. The points were chosen through preliminary testing, which showed the locations with the highest temperature at thermal equilibrium for the respective components. For the DDR4 memories, a single point was chosen to represent all dice. On the PWB an additional point was added as a representative of the connection between the SIP and PWB at the package extremities.

The simulation of Model I was performed with an ambient temperature of 20°C. The heat generated by the dice dissipate throughout the package creating a temperature gradient, an overview of which is shown in figure 5.1. To see the dissipation along the Y-axis, a cross section was made. The positioning of the cross section and the temperature along that plane can be seen in figure 5.2. The cross section was positioned to capture both the GR765 as well as the DDR4 dice on either side.

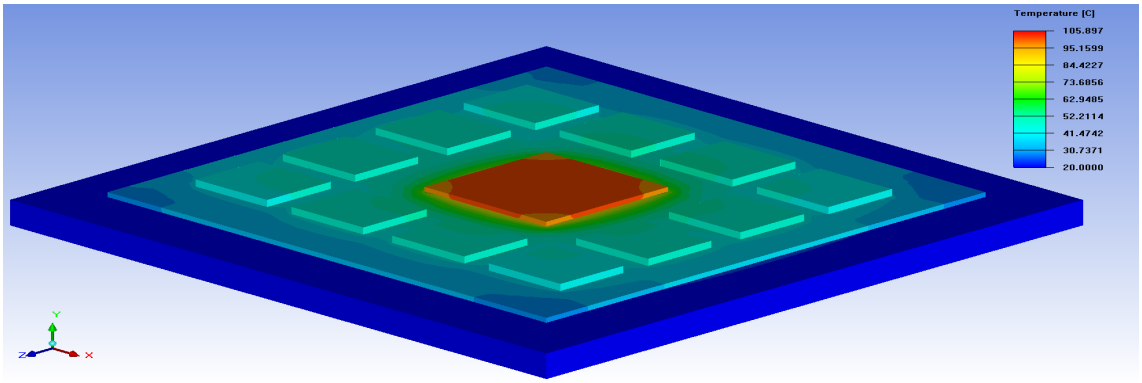
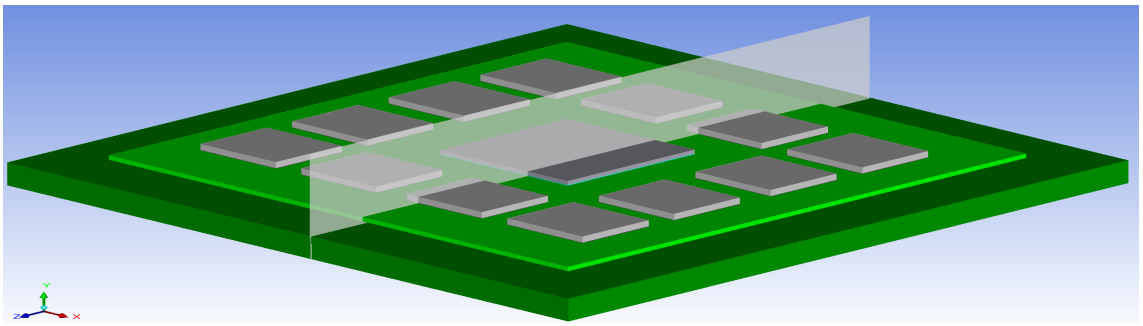
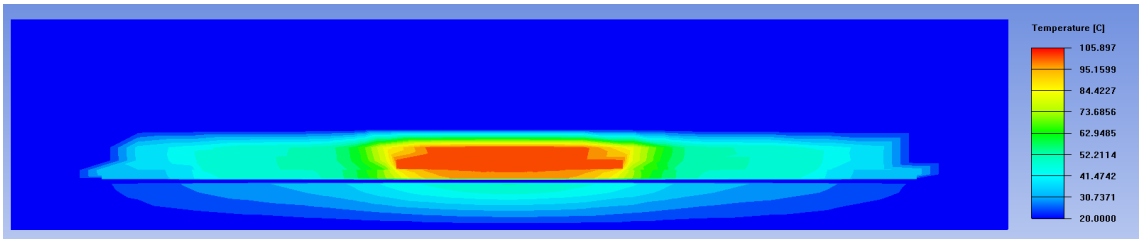


Figure 5.1: An overview of the temperature gradient of Model I. In order to expose the dice the overmold has been made invisible. Ambient temperature for the simulation was 20°C.



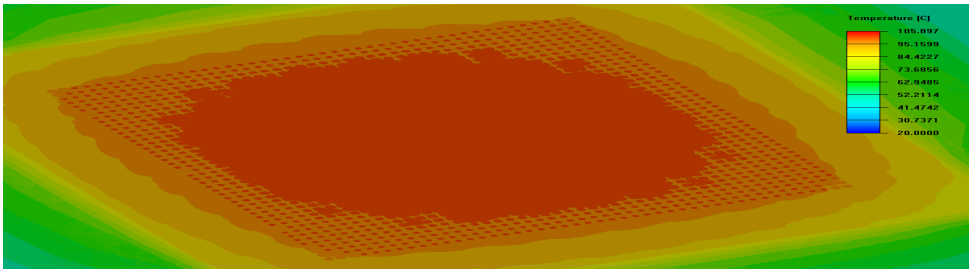
(a) Positioning of the cross section of Model I. The cross section was made in line with the highest temperature point on the DDR4s.



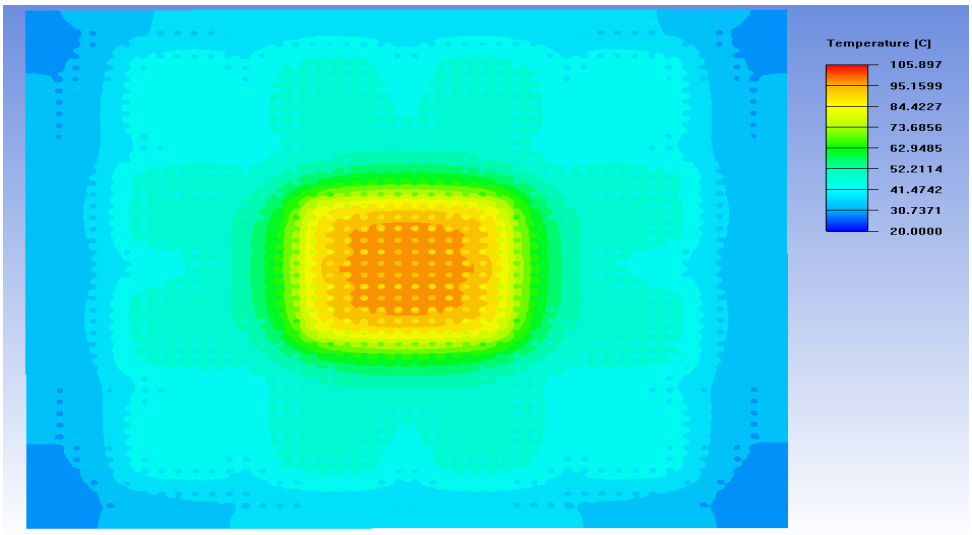
(b) Temperature gradient over the cross sectional plane of Model I.

Figure 5.2: A cross section was made to observe the heat dissipation throughout the y-axis of Model I. Figure **(a)** shows the placement of the cross section and figure **(b)** shows the temperature gradient over the defined plane. Ambient temperature was set to 20°C.

The GR765 which generates the most heat represented the highest temperature part of the model. The memory dice were lower temperature in comparison to the GR765. Note though that all memory dice were observed to have higher temperatures at the edge closest to the GR765. The substrate just below the GR765 also reached high temperatures as the heat passed through it towards the PWB. A closeup of the top side of the substrate in figure 5.3 shows the heat transferred well between the GR765 and substrate through the microbumps. The same effect was observed on the underside of the substrate, where heat left the substrate through the solder balls towards the PWB. The PWB itself saw a small temperature increase at the connection to the highest temperature area of the SIP, but overall remained close to ambient temperature.



(a) Closeup of substrate under flip chip GR765



(b) View of the underside of substrate

Figure 5.3: Temperature gradients showing the impact of microbumps and solder balls on the substrate of Model I.

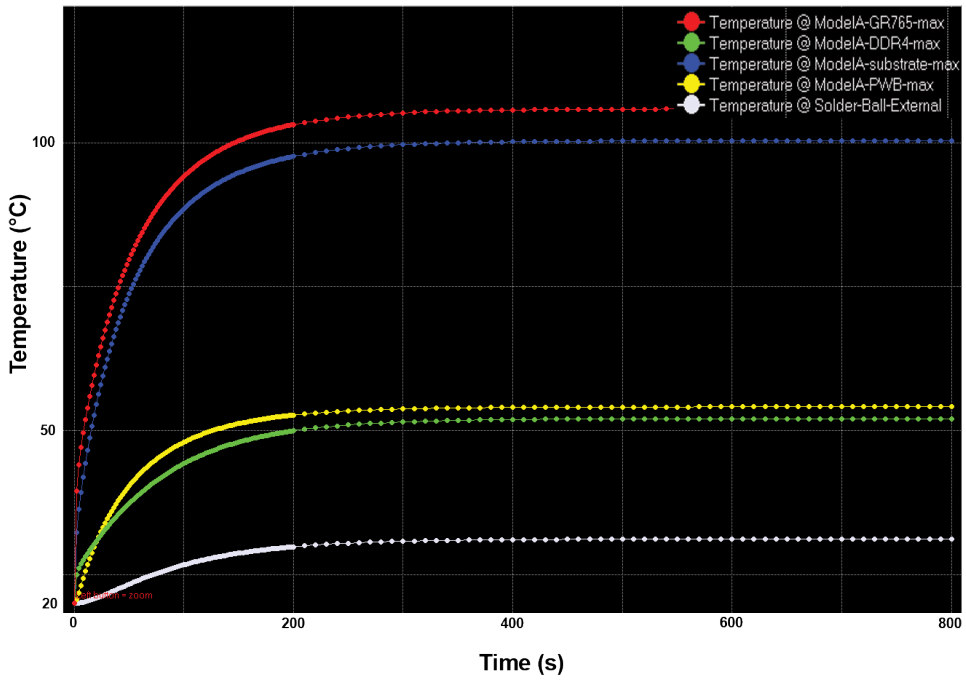


Figure 5.4: Graph showing the temperatures at points of interest over time.

Table 5.1: Maximum temperatures of different components in Model I. Ambient temperature was set to 20°C.

Component	Average Temperature (°C)	Maximum temperature (°C)
GR765	103	106
DDR4s	50	52
Substrate	46	100
PWB	24	54
Solder Ball External	-	31

The temperature at the points of interest marked in figure A.1 were plotted over time, shown in the graph in figure 5.4. The frequency of measurements were lowered later on due to slow changes in temperature. The graph shows that temperature changes quickly before 200 seconds, and reach thermal equilibrium at around 300 seconds. Table 5.1 shows the average temperatures of some key components, as well as the temperatures at each point of interest when thermal equilibrium had been reached.

5.2 Non-ideal Model Practices

Model I is quite simplistic, excluding contact resistances and concentrated heat generation. These factors may have affected the heat transfer through the package in such a way that it is not a good representation of a real case. The following results show how the two model qualities impact the package temperatures.

5.2.1 Model II: Contact Resistances

The introduction of contact resistances only changed surface conditions, meaning the points of interest for this model were the same as for Model I. The same location was also used for the cross section. With an ambient temperature of 20°C, figures 5.5 and 5.6 shows an overview and a cross section temperature gradient of Model II.

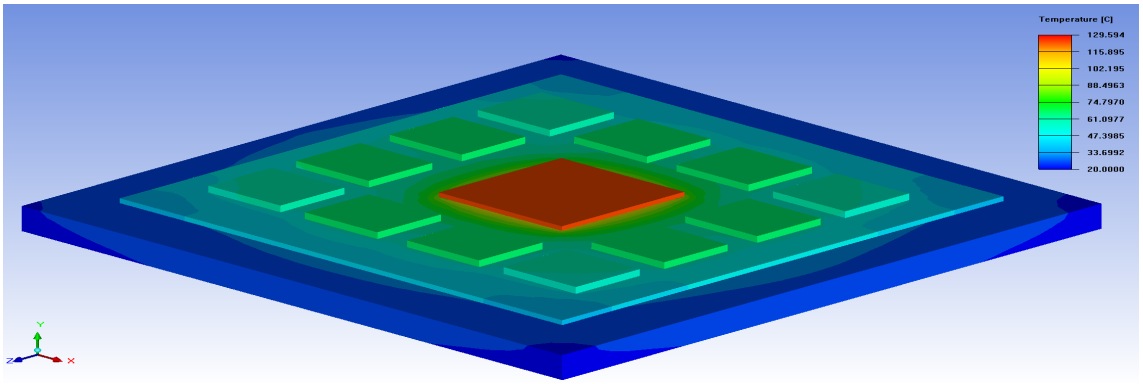


Figure 5.5: An overview of the temperature gradient of Model II. in order to expose the dice the overmold has been made invisible. Ambient temperature for the simulation was 20°C.

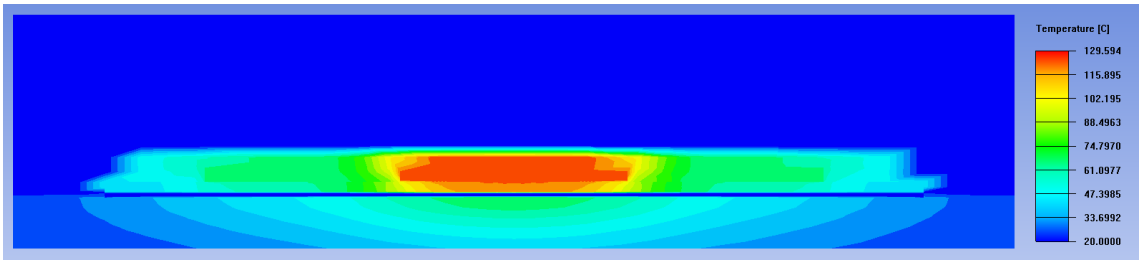


Figure 5.6: Temperature gradient over the cross sectional plane of Model II. Ambient temperature for the simulation was 20°C.

While the temperature gradients look similar to those of Model I, the temperature increased throughout the entire model. The temperatures at thermal equilibrium can be seen in table 5.2.

Table 5.2: Maximum temperatures of different components in Model II. Ambient temperature was set to 20°C.

Component	Average Temperature (°C)	Maximum temperature (°C)
GR765	127	130
DDR4s	65	68
Substrate	59	122
PWB	34	74
Solder Ball External	-	40

5.2.2 Model III: GR765 Hot Spots

The non-uniform heat generation of this model causes the hot spots to shift. The new points of interest can be seen in figure A.2

Simulation ambient temperature was again set to 20°C. Figure 5.7 shows an overview temperature gradient. A cross sectional temperature gradient captures both the highest temperature of the GR765 and the hottest point on the memories. The positioning of the cross section and temperature gradient are shown in figure 5.8.

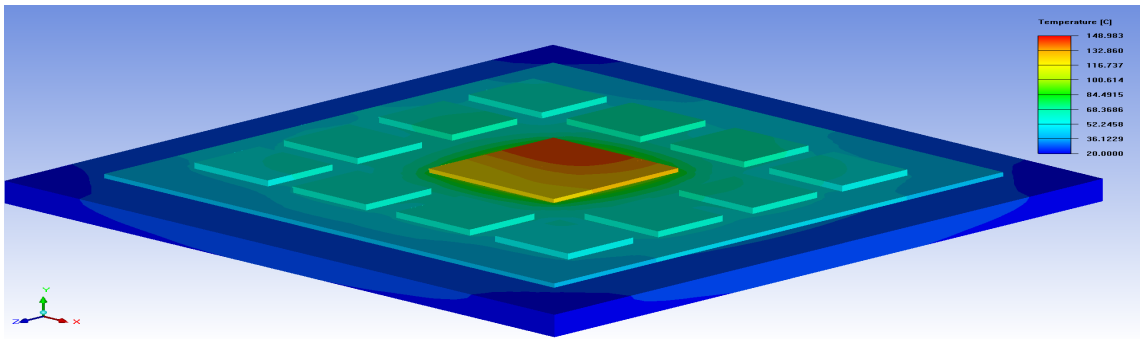
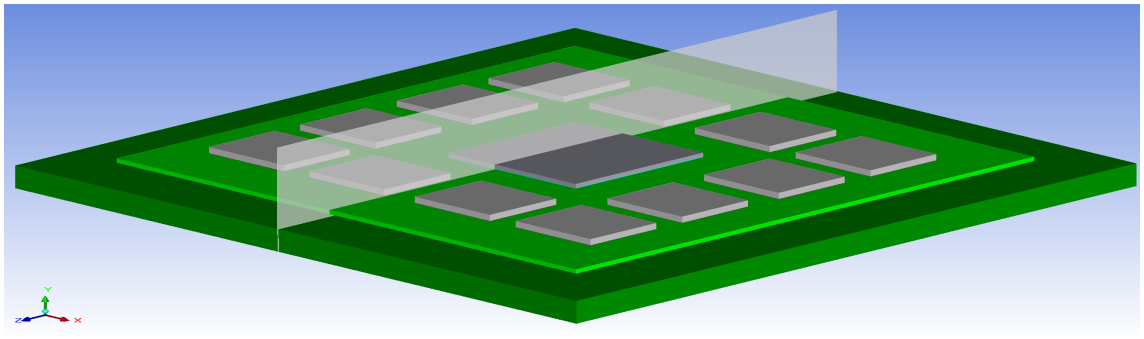
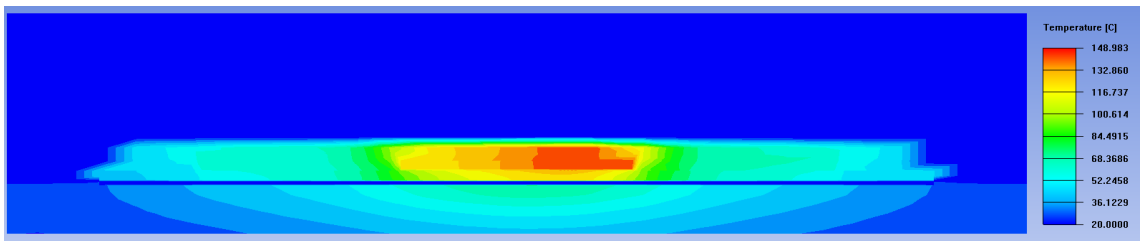


Figure 5.7: An overview of the temperature gradient of Model III. In order to expose the dice the overmold has been made invisible. Ambient temperature for the simulation was 20°C.



(a) Positioning of the cross section of Model III. The cross section was made in line with the highest temperature point on the DDR4s.



(b) Temperature gradient over the cross sectional plane of Model III.

Figure 5.8: A cross section was made to observe the heat dissipation throughout the y-axis of Model III. Figure **(a)** shows the placement of the cross section and figure **(b)** shows the temperature gradient over the defined plane. Ambient temperature was set to 20°C.

The highest temperature of the SIP was once again at the GR765. This time, however, the point of interest had moved towards the corner of the die representing the processor cores. The increased heat generation in this corner of the GR765 can also be seen in the temperatures of the memory dice. The dice closest to the new hot spot had higher temperatures in comparison to dice placed elsewhere. Temperatures were documented in table 5.3.

Table 5.3: Maximum temperatures of different components in Model III. Ambient temperature was set to 20°C.

Component	Average Temperature (°C)	Maximum temperature (°C)
GR765	135	149
DDR4s	65	69
Substrate	59	127
PWB	34	75
Solder Ball External	-	40

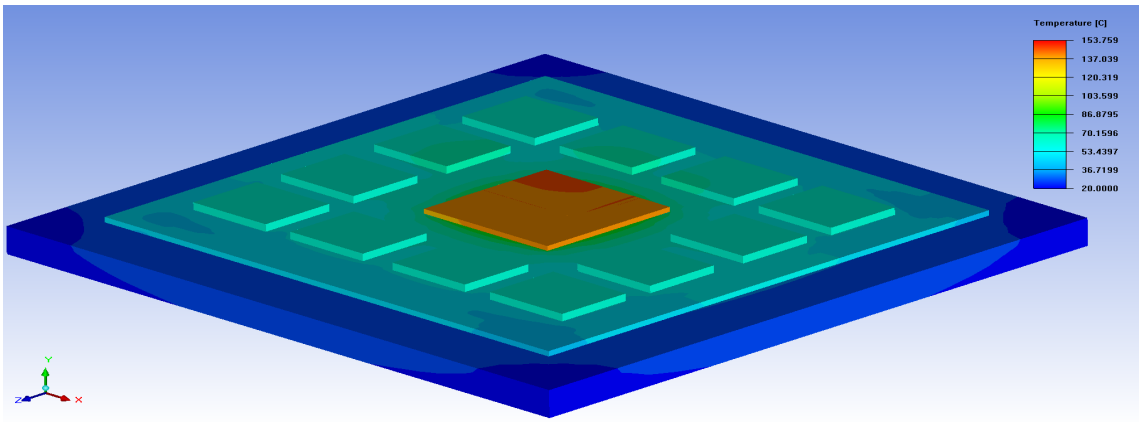
5.3 Thermal Target

When the impact of non-ideal model practices have been established, the temperatures fall outside of our target range of 125°C at 55°C ammbient temperature. The following section presents the results of models meant to bring temperatures down to reach this target.

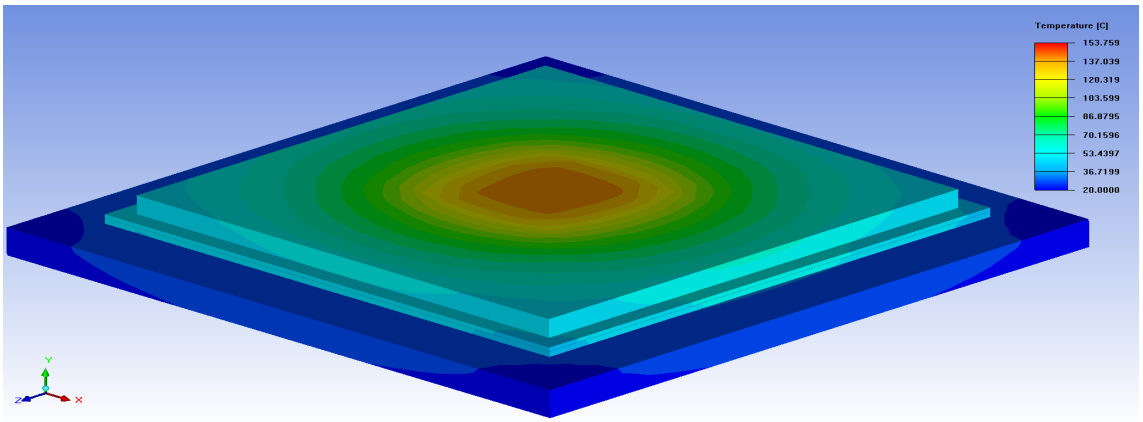
5.3.1 Model IV: Metal Lid

The metal lid introduces a new thermal path from the GR765. The new points of interest are marked in figure A.3. The simulation was performed at 20°C. Figure 5.9 shows the temperature gradient over both the metal lid as well as for the dice and substrate below. The ring where the lid is fastened to the substrate has a notable impact on the temperatures of the substrate. The changed temperature profile can also be seen in the cross section in figure 5.10.

The temperature gradient overview in figure 5.9 shows the substrate temperatures as more uniform than previous models. The heat dissipated through the metal lid, and the uneven temperatures were observed on its gradient instead. The cross section in figure 5.10 also shows higher temperatures moving towards the lid.



(a) An overview of the temperature gradient of Model IV. In order to expose the dice the metal lid has been made invisible.



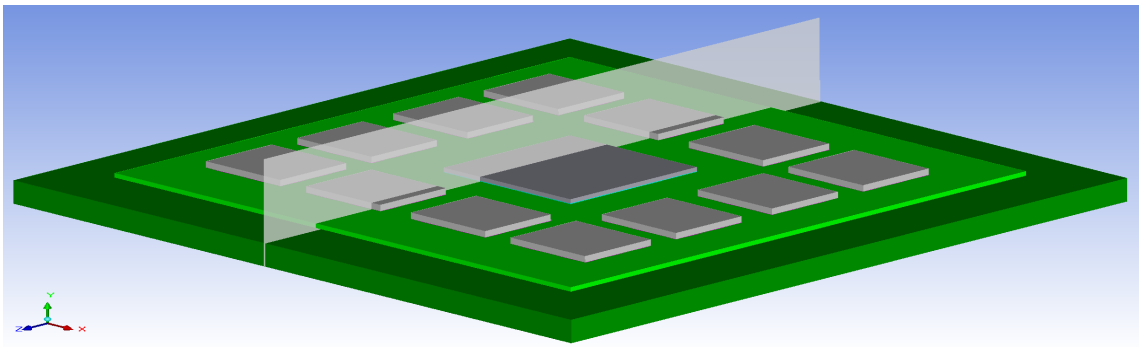
(b) The temperature gradient of the lid in Model IV.

Figure 5.9: Temperature gradients of Model IV. Figure (a) show the dice and substrate, and figure (b) shows the metal lid. Ambient temperature for the simulation was 20°C.

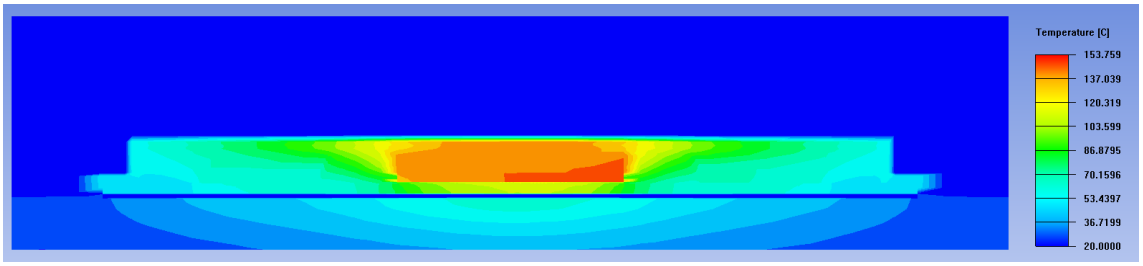
Even though the metal lid was predicted to lower temperatures of the package, this model reached higher maximum temperatures in comparison with Model III. This means that the heat generated by the GR765 still raises the temperatures too high for our thermal target. The average temperature of important components as well as the maximum temperature at points of interest is showed in table 5.4. Notably, the metal lid spreading the heat led to significantly lower maximum temperatures for the substrate and PWB, despite remaining at similar average temperatures when compared to Model III.

5.3.2 Model V: Dedicated Heat Sink

The additional heat sink of this model allowed for much better heat dissipation from the GR765 die. The thermal path from the die to the cold plate also had a very low thermal resistance, which made the dissipation more effective than through the substrate. The highest temperature point of the GR765 shifted down towards the underside of the die. The point is marked in figure A.4.



(a) Positioning of the cross section of Model IV. The cross section was made in line with the highest temperature point on the DDR4s.



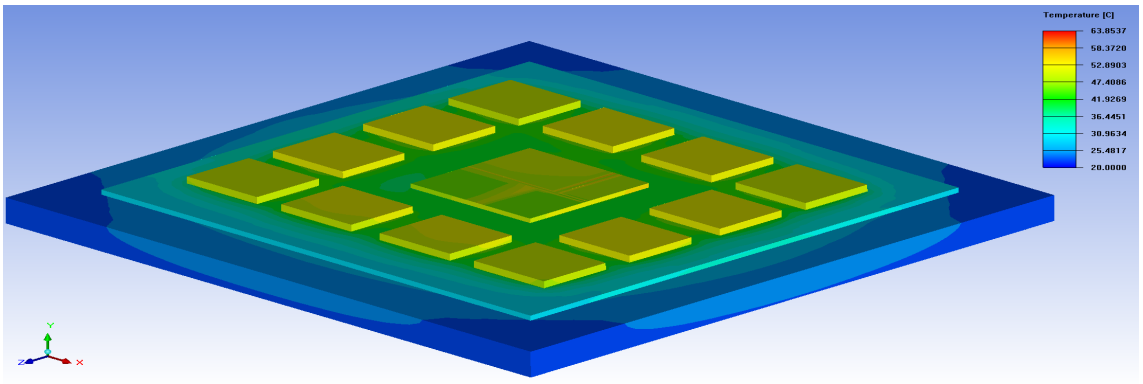
(b) Temperature gradient over the cross sectional plane of Model IV.

Figure 5.10: A cross section was made to observe the heat dissipation throughout the y-axis of Model IV. Figure **(a)** shows the placement of the cross section and figure **(b)** shows the temperature gradient over the defined plane. Ambient temperature was set to 20°C.

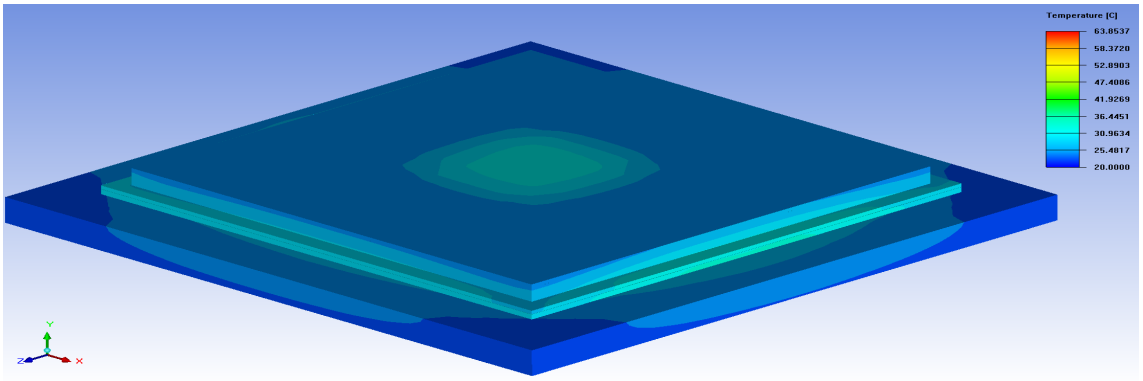
Table 5.4: Maximum temperatures of different components in Model IV. Ambient temperature was set to 20°C.

Component	Average Temperature (°C)	Maximum temperature (°C)
GR765	145	154
DDR4s	67	70
Substrate	59	115
Lid	75	146
PWB	34	69
Solder Ball External	-	45

The cold plate introduced a new way for heat to leave the package. Comparing the temperature gradient overview in figure 5.11 with those from Model IV in figure 5.9 shows what a large impact the new thermal path had on the SIP. The high thermal conductivity of the copper cold plate also allows the heat sink itself to remain at close to ambient temperature. The comparison of the copper heat sink and PWB heat sink is clear in the cross section of figure 5.12.



(a) An overview of the temperature gradient of Model V. In order to expose the dice the metal lid has been made invisible.



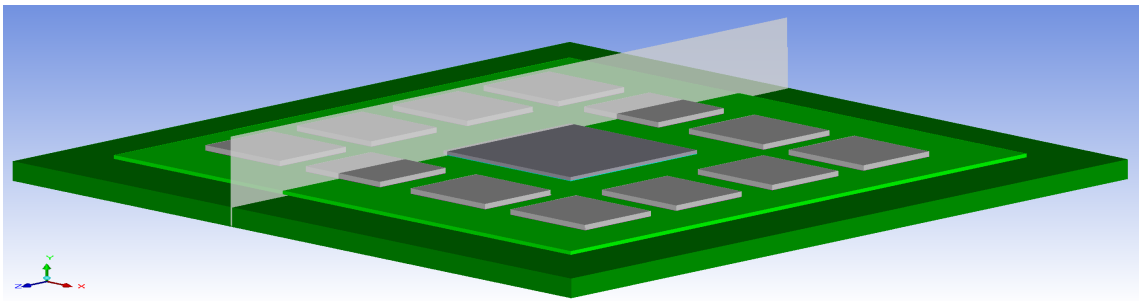
(b) The temperature gradient of the lid in Model V.

Figure 5.11: Temperature gradients of Model V. Figure (a) show the dice and substrate, and figure (b) shows the metal lid. Ambient temperature for the simulation was 20°C.

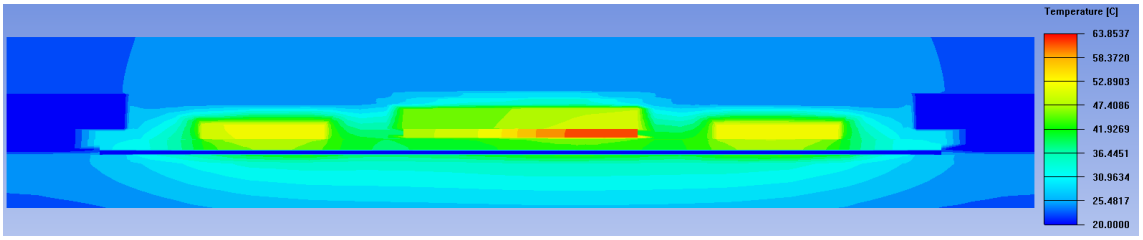
The addition of a cold plate greatly reduced the temperatures of the entire model. The GR765 and lid, which had good connection to the cold plate, saw large drops in temperature when comparing to Model IV. For previous models, all heat generated by the SIP had to pass through the substrate to reach a heat sink. This would elevate substrate temperatures. With the cold plate connected the substrate did not need to manage as much heat, which led to a huge drop in maximum temperature of the substrate. Average and maximum temperatures of key components are presented in table 5.5.

Increased Ambient Temperature

With the thermal target reached for an ambient temperature of 20°C, another simulation was run with the ambient temperature increased to 55°C. The points of interest did not move from the last simulation. The cross section was also made at the same place in the model. The temperature gradients for the simulation with elevated ambient temperature can be seen in figures 5.13 and 5.14. Average and maximum temperatures are also listed in table 5.6.



(a) Positioning of the cross section of Model V. The cross section was made in line with the highest temperature point on the DDR4s.



(b) Temperature gradient over the cross sectional plane of Model V.

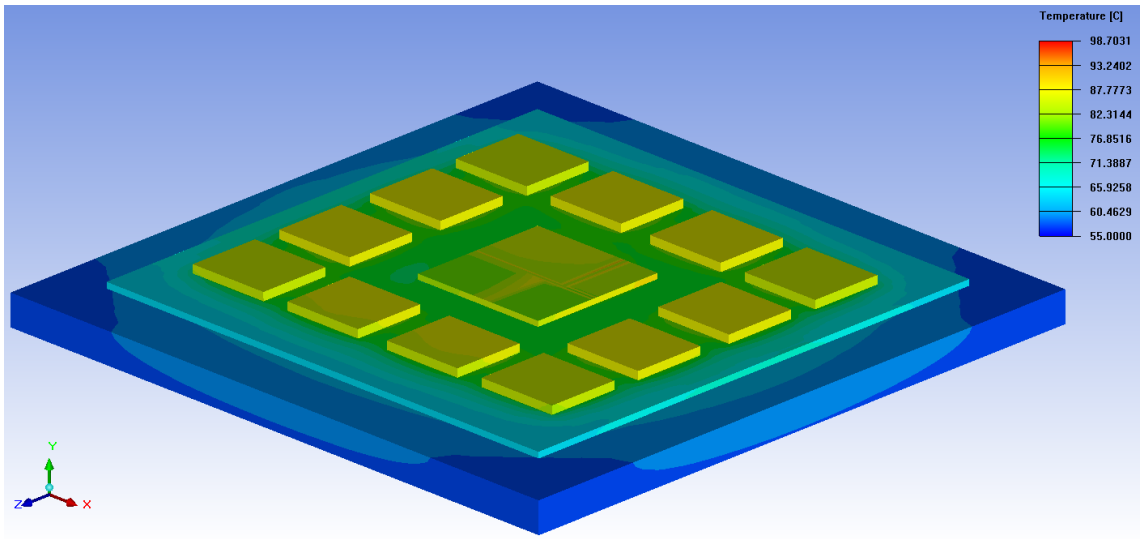
Figure 5.12: A cross section was made to observe the heat dissipation throughout the y-axis of Model V. Figure **(a)** shows the placement of the cross section and figure **(b)** shows the temperature gradient over the defined plane. Ambient temperature was set to 20°C.

Table 5.5: Maximum temperatures of different components in Model V. Ambient temperature was set to 20°C.

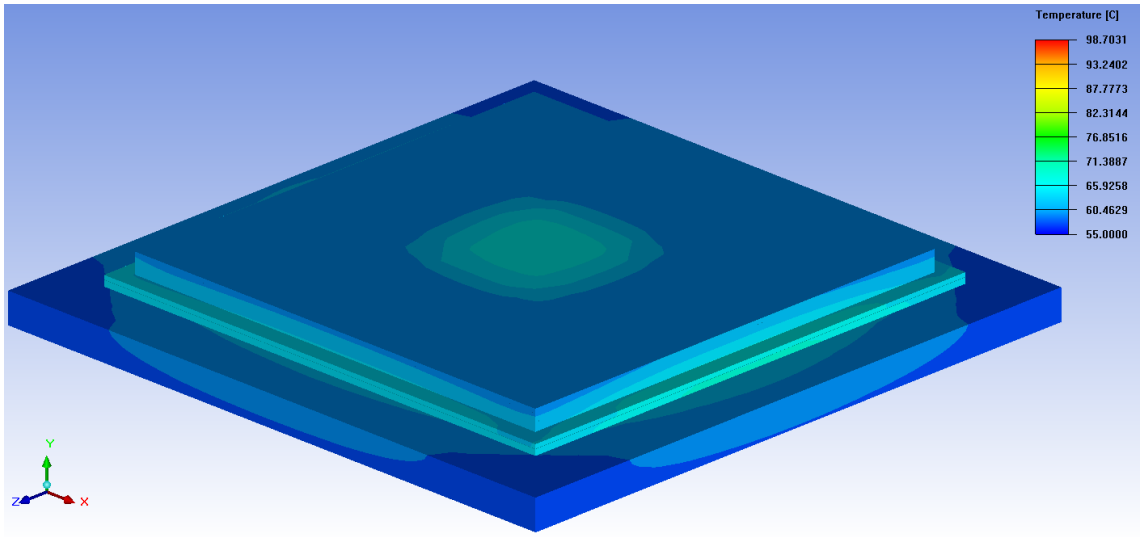
Component	Average Temperature (°C)	Maximum temperature (°C)
GR765	53	64
DDR4s	52	53
Substrate	40	49
Lid	28	49
PWB	29	46
Cold plate	25	33
Solder Ball External	-	29

5.4 Downscaling Form Factor

After reaching our temperature goal in Model V, we could instead look towards compacting the dice together inside of the package. This would allow for either adding additional memories or even completely new ICs to the SIP. If no more chips are needed, the entire package could be downsized, making it more compatible with different size PWBs used in the space vehicle. The favored method for reducing the form factor for this project was to use stacked memory dice, as outlined in section 4.4.



(a) An overview of the temperature gradient of Model V. In order to expose the dice the overmold has been made invisible.



(b) Overview of the temperature gradient of Model V.

Figure 5.13: Temperature gradients of Model V. Figure (a) show the dice and substrate, and figure (b) shows the metal lid. Ambient temperature for the simulation was 55°C.

5.4.1 Model VI: Memory Stacking

With stacked dice, there were multiple heat sources that needed to transfer their heat through the same adhesive at the bottom of the stack. The low thermal conductivity of the plastic adhesive limited heat transfer, leaving much of the heat generated stuck in the stack which raised the temperatures. As the DDR4s were not in contact with the metal lid, a lot of heat had to be transferred through the substrate. The increased temperature of the DDR4s moved the points of interest from the GR765 towards the memory stacks. The new points of interests can be seen in figure A.5.

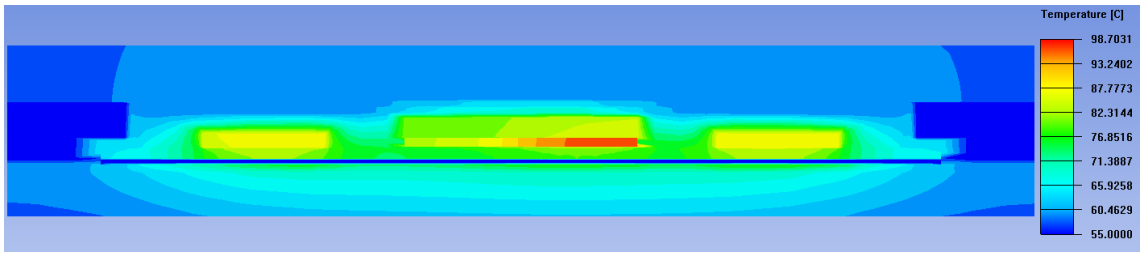
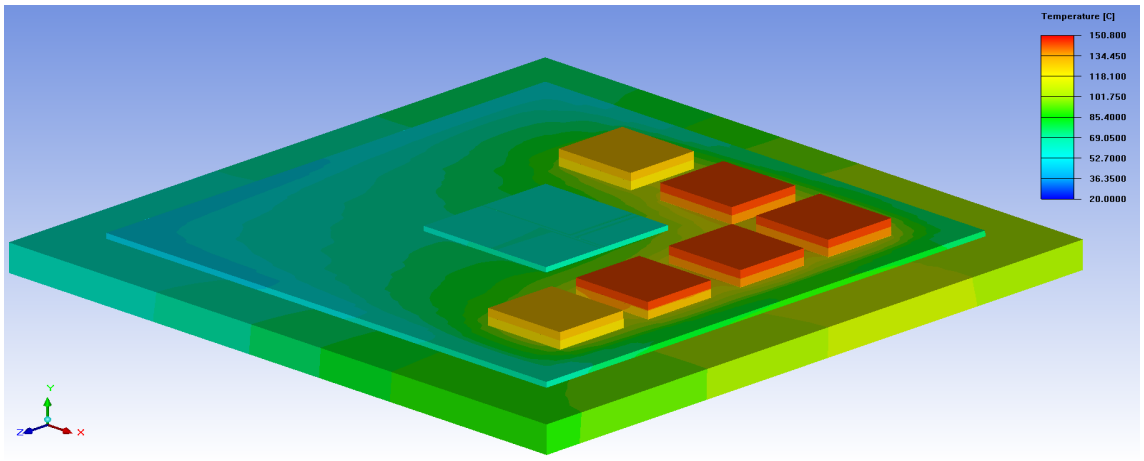


Figure 5.14: Temperature gradient over the cross sectional plane of Model V. Ambient temperature for the simulation was 55°C.

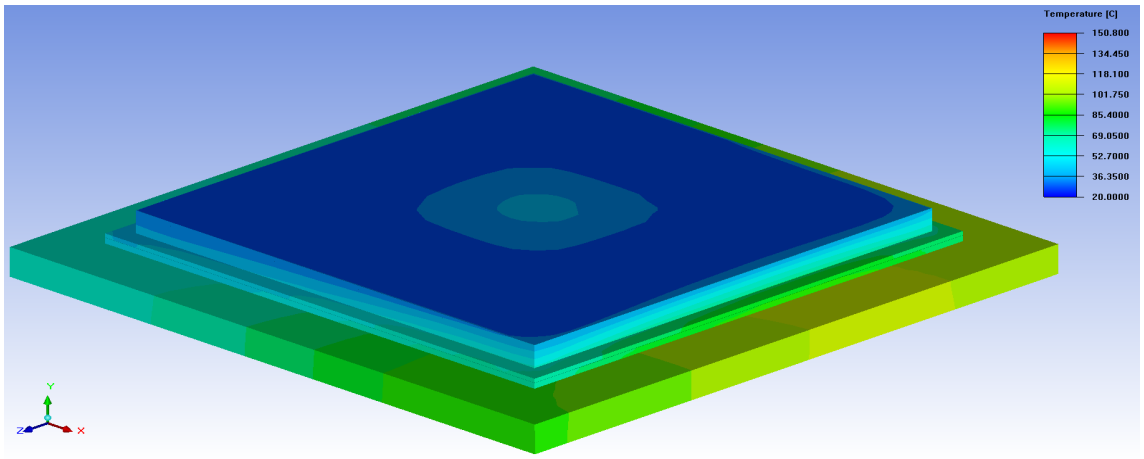
Table 5.6: Maximum temperatures of different components in Model V. Ambient temperature was set to 55°C.

Component	Average Temperature (°C)	Maximum temperature (°C)
GR765	88	99
DDR4s	87	88
Substrate	74	85
Lid	63	84
PWB	64	82
Cold plate	60	68
Solder Ball External	-	64

Figure 5.15 shows the high temperature DDR4s, as well as the gradient over the metal lid. Even though the highest temperature point of the lid was located at the contact point with the substrate, close to the memories, there was still a notable temperature increase around the GR765. Two cross sections were made in order to capture the asymmetry of the package. The images in figure 5.16 are evidence of the impact the high DDR4 temperatures have on the PWB.



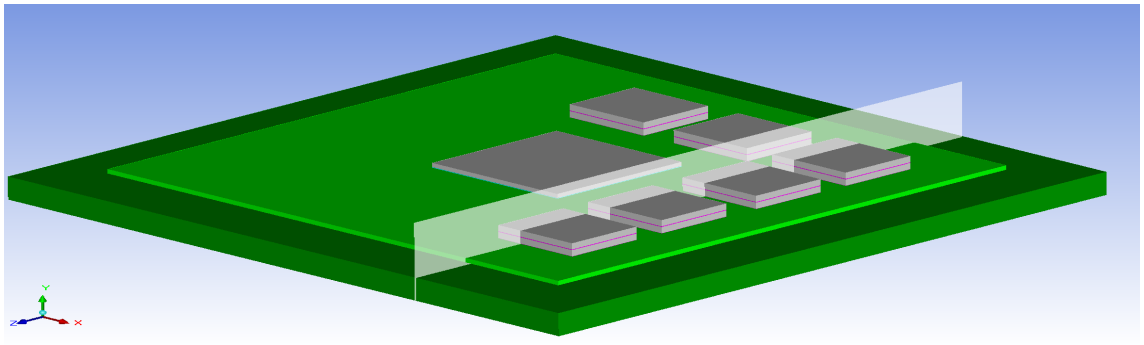
(a) An overview of the temperature gradient of Model VI. In order to expose the dice the metal lid has been made invisible.



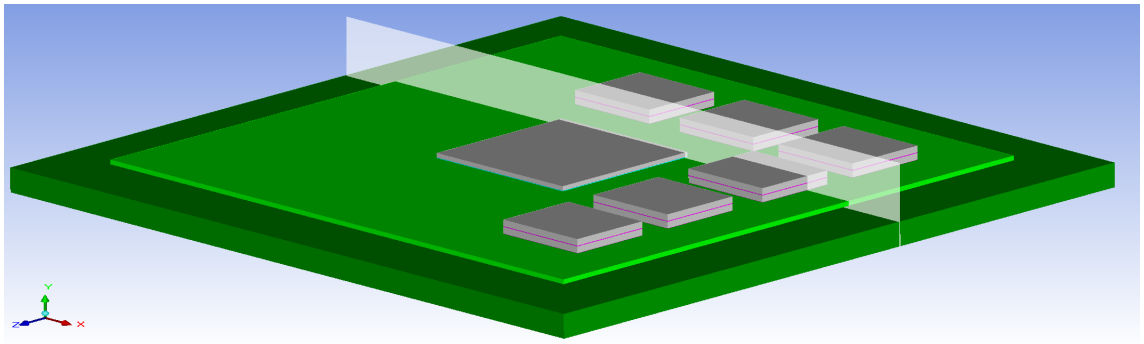
(b) The temperature gradient of the lid in Model VI.

Figure 5.15: Temperature gradients of Model VI. Figure (a) show the dice and substrate, and figure (b) shows the metal lid. Ambient temperature for the simulation was 20°C.

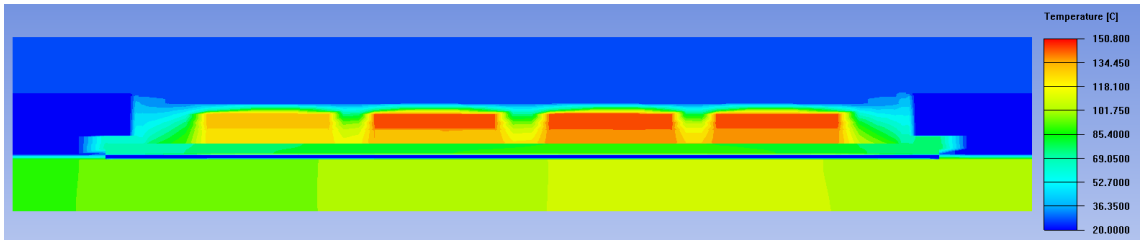
The increased temperature of the DDR4s introduced some unpredictable temperature changes throughout the entire package. The average and maximum temperature of key components are listed in Table 5.7. Most notably, the DDR4s showed higher temperatures than the GR765. Comparing the temperatures to those found in table 5.5 from Model V it was noticed that the GR765 reached higher temperatures in Model VI.



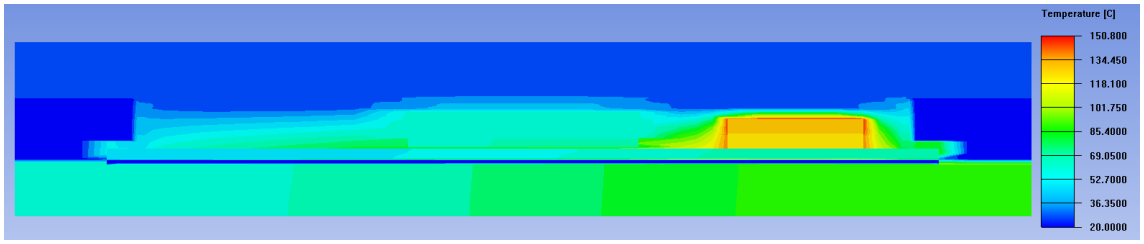
(a) Positioning of the cross section of the x-axis in Model VI. The cross section was made in line with the highest temperature point on the DDR4s.



(b) Positioning of the cross section of the z-axis in Model VI. The cross section was made in line with the highest temperature point on the DDR4s.



(c) Temperature gradient over the cross sectional plane of the x-axis in Model VI.



(d) Temperature gradient over the cross sectional plane of the z-axis in Model VI.

Figure 5.16: A cross section was made to observe the heat dissipation throughout the y-axis of III. Figures **(a)** and **(b)** show the placement of the cross sections and figures **(c)** and **(d)** show the temperature gradient over the defined planes. Ambient temperature was set to 20°C.

Table 5.7: Maximum temperatures of different components in Model VI. Ambient temperature was set to 20°C.

Component	Average Temperature (°C)	Maximum temperature (°C)
GR765	70	81
DDR4s	138	151
Substrate	85	136
Lid	41	91
PWB	90	131
Cold plate	31	41
Solder Ball External	-	62

6
Discussion

The models were built to replicate reality but many aspects of the models can still be improved upon. This chapter aims to make clear what insights can be found through the results, and some precautions to keep in mind when analyzing. The chapter ends with some potential ways to build on the work through continued simulations or experimental work.

This thesis has focused on the thermal design aspect of developing a SIP for space applications. Choosing a certain aspect, e.g. thermal management, of the design and making decisions purely based on the impact on this specific aspect is usually not a very good approach. While the main designs feature commonly used materials and processes, this work does not prove that they are compatible in reality. Instead, a more holistic design should focus on thermal management, electrical performance and mechanical aspects simultaneously. The narrow focus was necessary when considering the time frame of a thesis project compared to performing a complete design study.

6.1 Model I: Baseline

The simulation results from Model I were close to expectations. The model had the highest temperature at the center of the GR765, which was the main heat source. The heat dissipated downwards through the substrate, and also in a lesser degree throughout the plastic encapsulation. Despite the low thermal conductivity of the overmolded plastic, the heat from the GR765 managed to have an impact on the closest memory dice. If the temperatures of the DDR4s were to be of concern, they could be moved further from the GR765 to have this impact reduced.

The custom material used to simulate thermal properties of vacuum adapted from ANSYS Vacuum modeling guide worked as anticipated [41]. The low thermal conductivity and high specific heat capacity ensured little heat escaped the package through the surrounding fluid. Not even the highest temperature area of the encapsulation managed to dissipate much heat throughout the vacuum. What little heat did get absorbed by the vacuum was deemed to be negligible.

The impact of high thermal conductivity solders on the substrate can be seen from both the top and bottom side in figure 5.3. These results also give merit to the theory that a higher metal concentration in the package leads to better heat dissipation. If there is room below the flip chipped GR765, additional thermal vias could be a useful tool to improve heat dissipation.

6.2 Non-ideal Model Practices

As the GR765 SIP was in early stages of development during this work, many assumptions and simplifications had to be made regarding the package. The only electrical components considered were the GR765 and DDR4 memories. No other potential dice or passive electrical components were taken into account when producing the models. The arguably largest thermal bottleneck of the models was the substrate, which also had to be simplified due to lack of data. Improving on the substrate model would be a good step towards a more confident solution.

With the exception of a few cases, all the material properties used were set to a constant value. In reality, the thermal conductivity and specific heat capacity will be dependent on the temperature of the object. For a better representation, more time could have been invested into finding detailed material characterizations and implement them as piecewise functions into Icepak.

Due to the computational complexity, the wire bonds for DDR4 memories had to be omitted from the simulations. Despite the relatively high thermal conductivity of gold, the small contact area with the actual die would limit the heat flow through the bond wires. A comparison of the DDR4s with and without wire bonds would have been desirable to get a better understanding of their thermal impact.

6.2.1 Model II: Contact Resistances

The temperature gradients generated through Model II followed the expected rise in temperature suspected to occur when introducing thermal contact resistances. The heat dissipation looked to be similar to that of Model I, but with higher temperatures in the entire model. Comparing the gradient of Model I from figure 5.1 with gradient from Model II in figure 5.5 shows the GR765 reaching a higher temperature especially at the corners. The elevated temperatures of the GR765 also looked to raise the temperatures of the closest DDR4 dice. The DDR4s placed in the corners of the SIP did not seem to be impacted as heavily by the higher GR765 temperatures.

The thermal contact resistances used were general values provided through a technical advisor based on experience. For more precise values the particular materials used should be considered rather than a general interface value. The thermal contact resistance is also dependent on the pressure applied to the interface, which could mean two interfaces with the same materials would still have different thermal contact resistances.

6.2.2 Model III: GR765 Hot Spots

The introduction of hot spots yielded a larger temperature change than anticipated. It was theorized that the thermal conductivity of silicon as combined with the lack of contact resistance within the die itself would quickly spread the heat throughout the die. Instead, a large difference in temperature could be found when comparing the highest temperature points to lower temperature areas.

As the temperature in one corner of the GR765 increased, so did also the temperatures of the DDR4s in closest proximity. The comparison of a memory close to the GR765 cores and a memory close to the remainder section of the die showed a notable difference in temperature. To lower the impact on the highest temperature memories, the layout could be rearranged in order to move memories further from the highest temperature areas of the GR765.

6.3 Thermal Target

For ease of implementation, the SIP would benefit from being self sufficient in regards to thermal management. The addition of dedicated cooling in form of additional heat sinks limits the possibilities for implementing the SIP. On the other hand, the simplest way to reduce the temperature of the model would be to provide alternative thermal paths. Based on the results of Model IV it was decided that a dedicated heat sink in form of a cold plate would be needed in order to bring temperatures down enough to reach the thermal target.

The maximum temperatures from the simulation were all acquired by running the simulation for an extended time. As can be seen in figure 5.4 it takes approximately 300 seconds, around five minutes, to reach thermal equilibrium and the maximum temperatures. In a realistic scenario, it is unlikely that the GR765 SIP would be operating with all components at maximum capacity for such an extended time. For more realistic behavior, the heat generation could be defined through time dependent functions. This would instead provide a perspective closer to realistic component utilization and how the temperatures evolve as the heat sources change around the package.

6.3.1 Model IV: Metal Lid

Contrary to expectations, Model IV featuring a metal lid saw increased temperatures compared to Model III. The increased thermal conductivity of the metal lid did not outweigh the downside of reduced contact area compared to the plastic overmold. This is likely due to the low thermal conductivity of Kovar in comparison to other metals. If other materials for the lid were chosen, for example aluminum or copper, they should be able to better manage the hot spots of the GR765 and dissipate enough heat to see reduced temperatures.

The alternative thermal path from the top of the die, through the lid, and back to the substrate through the lid adhesive, efficiently spreads the heat to a larger part of the substrate. The result is a more even temperature distribution throughout the substrate. This is indicated by the substrate's similar temperature average between Model III and Model IV, despite the maximum temperature of the substrate being much higher for Model III.

The ideal operating conditions for the thermal pad requires a lot of pressure between the die and lid. No calculations were made on the forces this pressure would apply to the adhesive used to fasten the lid. If the adhesive were to be unfit for this kind of application, the lid could for example be soldered or welded to the substrate. This

would likely increase stability and thermal conductivity from the lid to the substrate at the cost of a more complicated manufacturing process.

6.3.2 Model V: Dedicated Heat Sink

After adding the dedicated cold plate the temperatures were drastically reduced. These results followed expectations, as there was now a much shorter, low resistance thermal path for the heat from GR765 to reach ambient temperature.

The DDR4 memories also saw reduced temperatures when the cold plate was added, despite the memories not being in contact with the lid and cold plate in any way other than through the substrate. The temperature reduction of the main heat source led to reduced temperatures in the memories. These results indicate that for a lidded package, the memories may be greatly impacted by the heat from other dice in the SIP.

Even when the ambient temperature was increased to 55°C the highest temperature of the package was stayed below the set thermal target. The large margin is a good indication that even if the model is not a perfect representation, the component should be fine to operate under these conditions. However, no recommendations can be made before knowing more about the heat generation and properties of other components of the SIP.

6.4 Downscaling Form Factor

For this project, the concept of memory stacking was explored as the method of downscaling the SIP. With this specific package a simpler approach could be to simply move the DDR4 dice closer to the GR765. The results from Model V indicates that even with some heat exchange between GR765 and memories the maximum temperatures could fit our thermal target. The achievable form factor reduction with this approach would however be quite limited.

The change of layout did not consider the necessary rerouting of electrical signals to the memories. It has been assumed for all designs that memory timings would not be an issue independent of the layout. The increased I/O density of stacked memories opens up for the consideration of an interposer to help the design to achieve better connectivity. However, due to predicted low impact on the thermal performance, this sort of study was excluded to fit within the time frame of the thesis.

6.4.1 Model VI: Memory Stacking

The temperatures of DDR4s reached unexpectedly high values. It is suspected that the low thermal conductivity of the adhesives was to blame for the large increase. The flip chipped GR765 performed better due to the metal in the microbumps. Another notable point was the increased temperatures of the PWB. There might be a limit to how much heat can be transferred from the SIP to other components on the board. To make the design more viable, the DDR4s should somehow be put in contact with the metal lid. This would allow more heat to dissipate to the heat

sink on top of the package and lower the temperatures of both the components of the SIP and the PWB.

The lowest temperature memory stacks were those with only one neighboring stack. Perhaps spacing the stacks more evenly around the GR765 would help even out the temperatures of the package. For instance a stack in each corner, where the memories of previous models were the lowest temperature, could yield better thermal performance. This would also require that no other heat generating components were placed close to the stacks, which would be a limitation of possible layouts.

6.5 Future Works

The future works explain how the findings of this thesis can be used as well as potential ways to improve the existing work. A few examples categorized as either simulation or experimental approaches have been described below.

6.5.1 Continued Simulations

There are many ways to continue working with the models through simulation. A common continuation of thermal analysis is to extend the work to thermal expansion. These simulations analyze the warping produced by the temperatures throughout the package caused by the differences in CTE of different package components. The studies often aim to evaluate the reliability of connections, as their functionality is crucial for the SIPs functionality.

A key assumption of the produced models is electrical aspects of the DDR4 memories. The proposed layouts have not been analyzed in terms of signal integrity or memory timing. Using the models as ground works for signal routing on the substrate, and then performing simulation on those signals could either validate or debunk the proposed layouts.

6.5.2 Experimental Work

One way to improve on the existing models would be to find a more representative definition of the materials and interfaces used. The necessary properties for the material definition can all be found through experimental methods. Along with experiments aimed at finding contact resistance between materials in the model would aid building a much better representation of reality.

If the GR765 SIP is eventually manufactured, and if the SIP is similar to the models produced during this thesis work, the models could be compared to reality using thermal probes or IR sensors. Comparisons with a real SIP would give insights into the quality of the methods and assumptions made during the project.

7
Conclusion

This thesis work aimed to assist in the investigation of a SIP based on the GR765 microprocessor and DDR4 memories. The work focused on thermal management and how different design choices impact the maximum temperature of the package. The work briefly covers common manufacturing techniques with added thermal perspective to help designers quickly get an overview of the advantages and disadvantages of particular methods.

A few example SIP models were designed and tested through CFD simulations in ANSYS Icepak. The software uses the FVM to simulate heat conduction through a simple CAD model of example designs of the SIP. The first few model iterations helped define a representative SIP model, before utilizing better thermal management techniques to reach a thermal target. After a viable design had been found, an attempt was made to reduce the area in the SIP occupied by memories.

The results of the simulations indicated that contact resistances between material interfaces had noticeable impact on the temperatures of the SIP. Additionally, using a die model with more detailed heat generation compared to homogeneous heat generation had a larger impact than expected on maximum temperature of the package.

The use of a metal lid as a heat spreader did not seem to lower temperatures of the GR765 die, but provided more even temperature gradients for the remaining package. The addition of a dedicated heat sink on top of the lid yielded a great reduction in temperatures for the entire package and especially the GR765. Stacking of memory dice using FOW technology freed up more of the substrate for other components, but showed an increase in maximum temperature of the memories.

There are a couple of options available to continue building on the work of this thesis. Improving the simulation could be done through more detailed material data found through lab analyses. Mechanical aspects like warpage of the substrate can be explored by using the temperatures generated to simulate thermal expansion of the package. One of the main concerns is the viability of the DDR4 layout with respect to memory timing. Investigating the routing and PHY of the memories could be a useful addition either validating or debunking the dice placements of the proposed designs.

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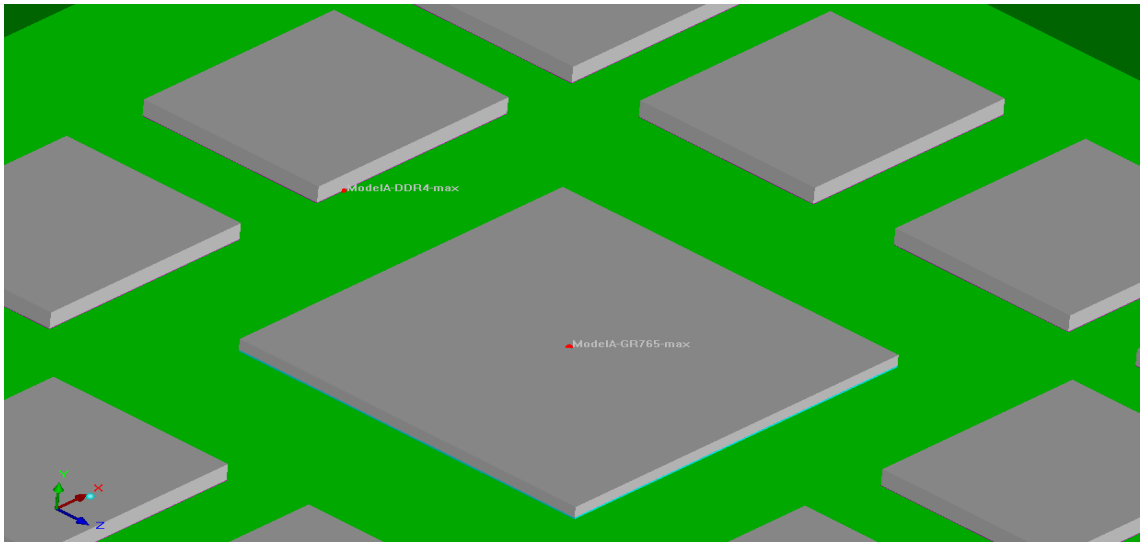
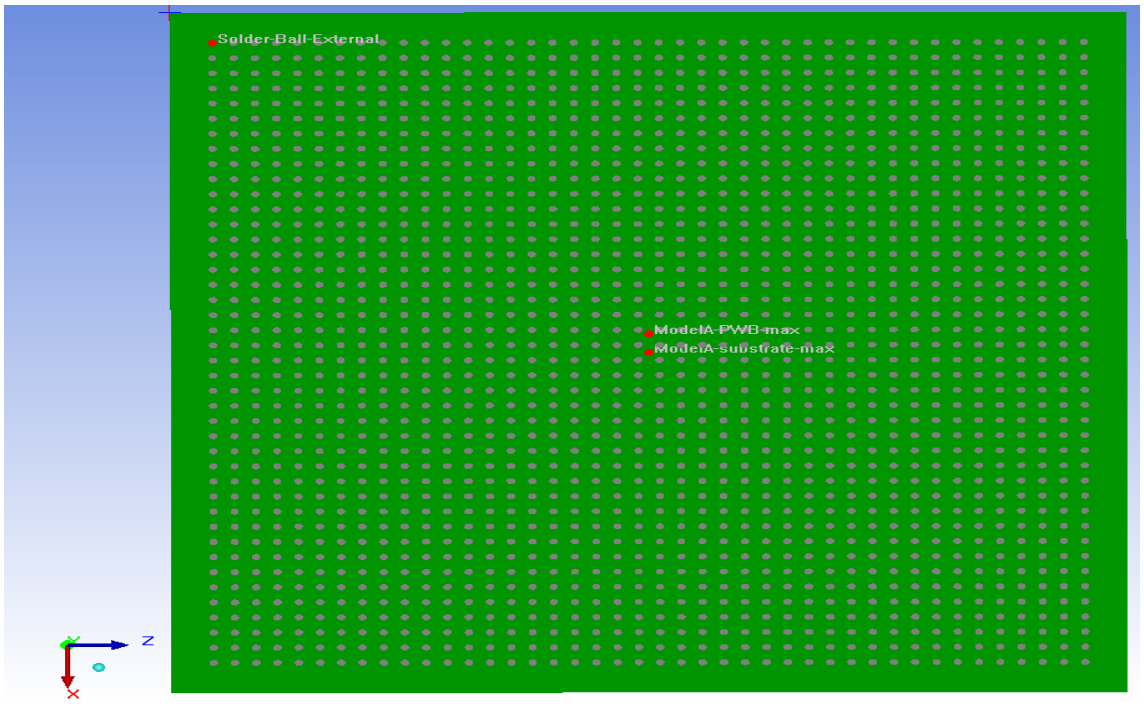
A

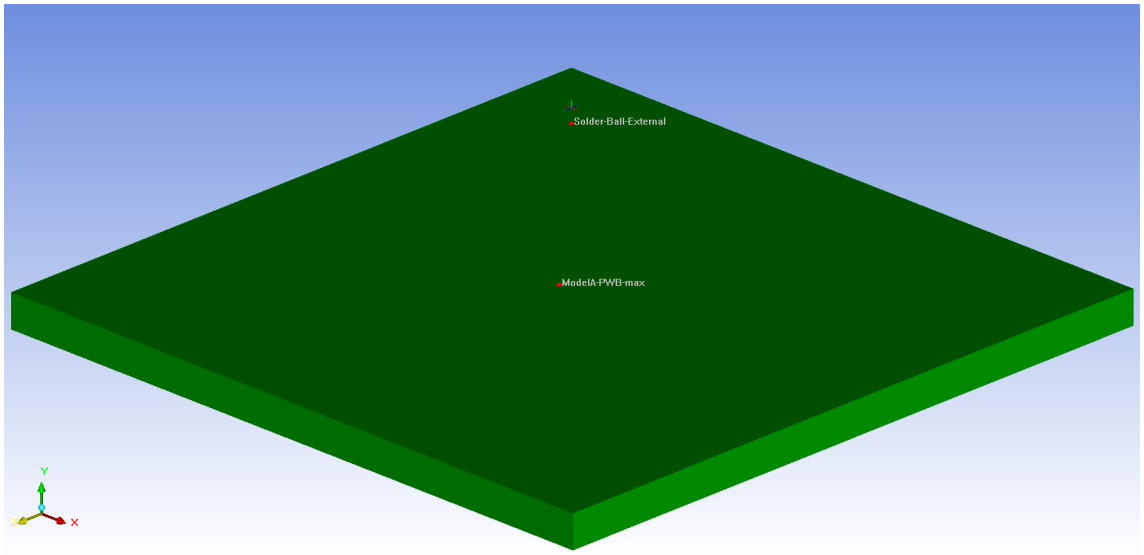
Appendix 1



(a) Points of interest marked on the GR765 and DDR4 chips of Model I.

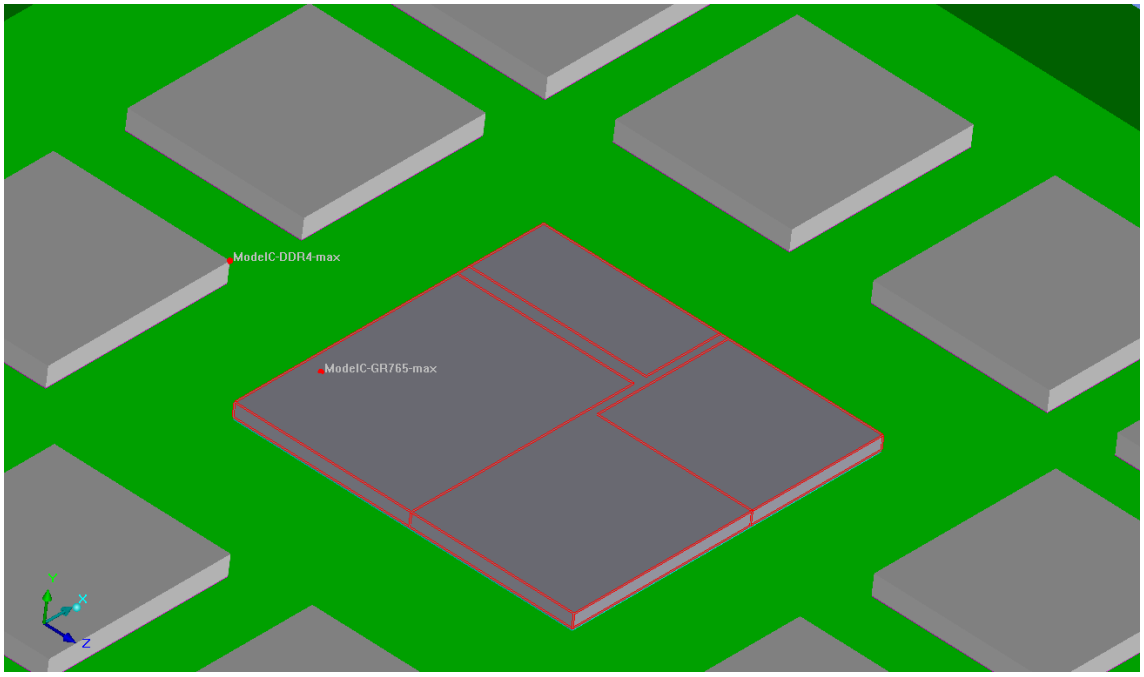


(b) Points of interest marked on the underside of the substrate of Model I.

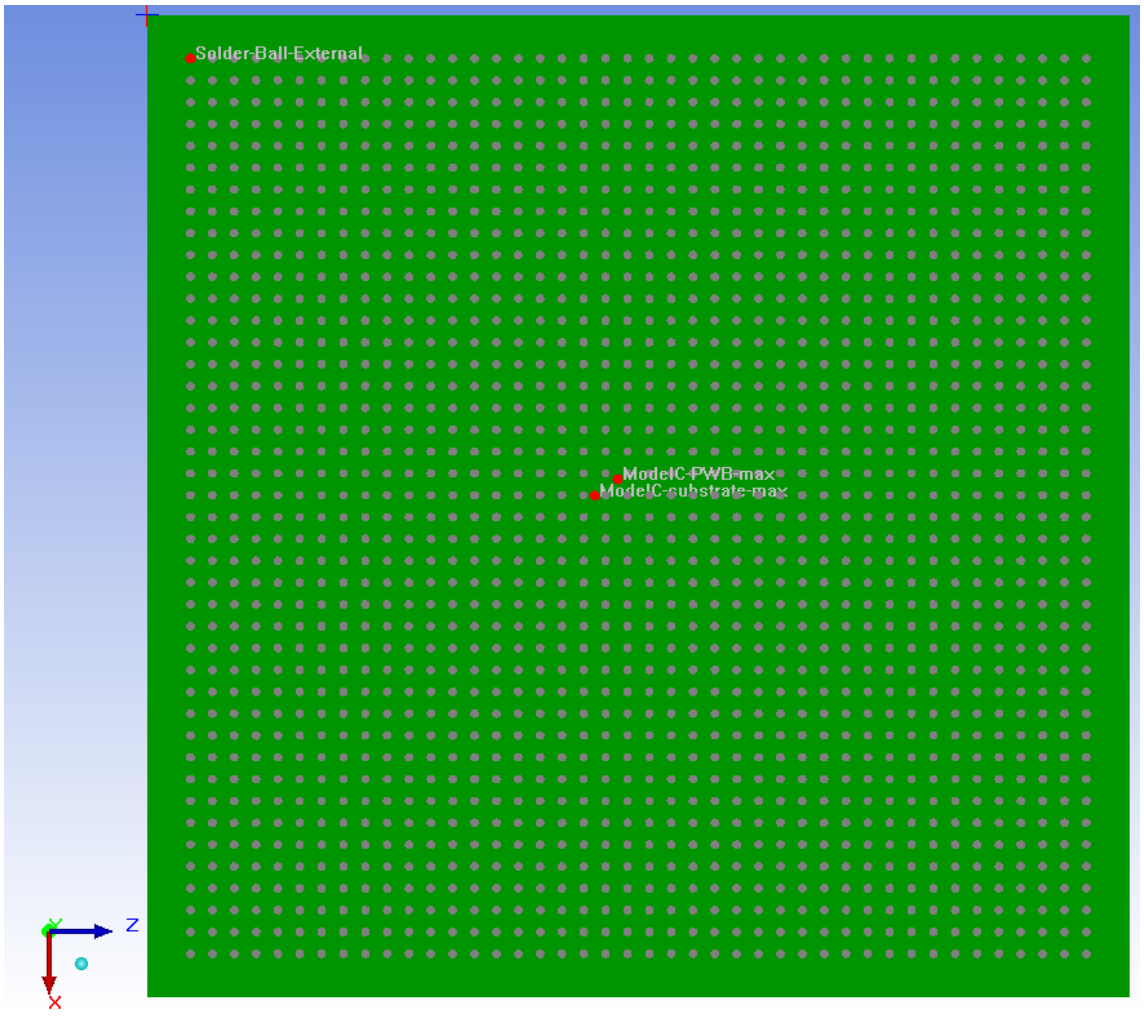


(c) Points of interest marked on the top side of the PWB of Model I.

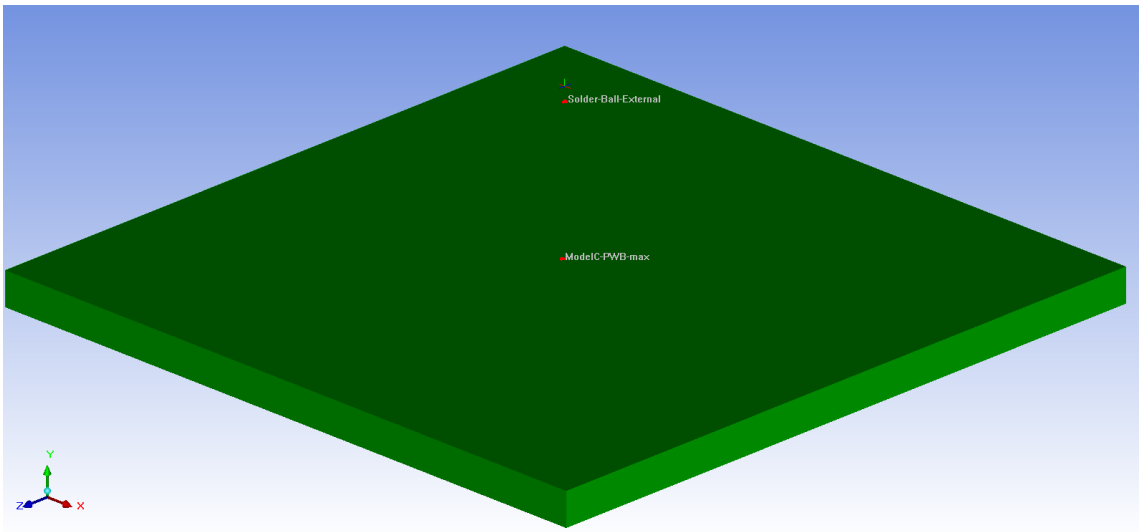
Figure A.1: Points of interest marked on different components of Model I. The points represent the highest temperature point on their respective component.



(a) Points of interest marked on the GR765 and DDR4 chips of Model III.

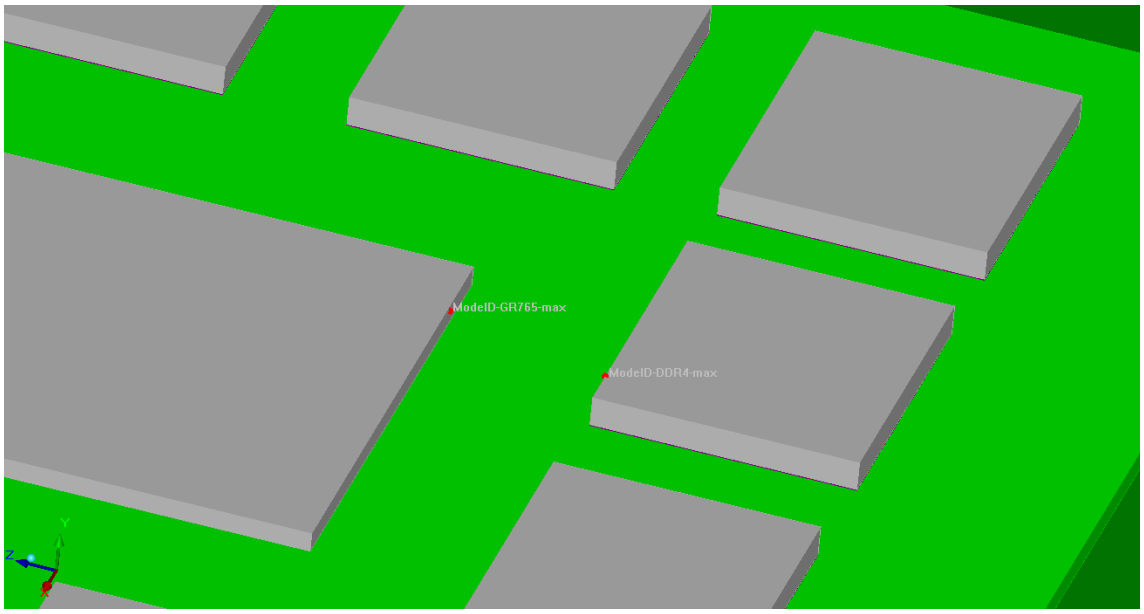


(b) Points of interest marked on the underside of the substrate of Model III.

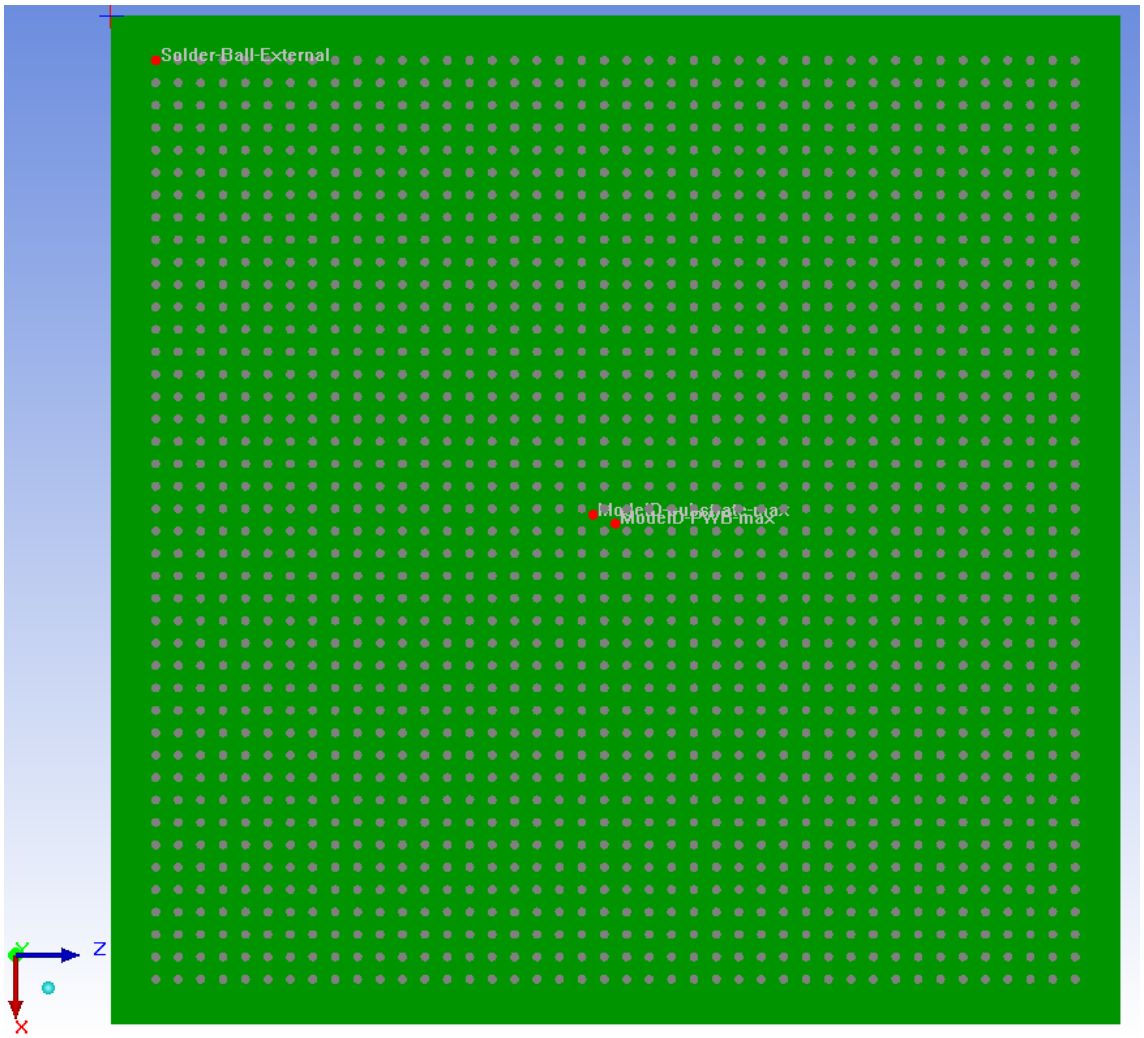


(c) Points of interest marked on the top side of the PWB of Model III.

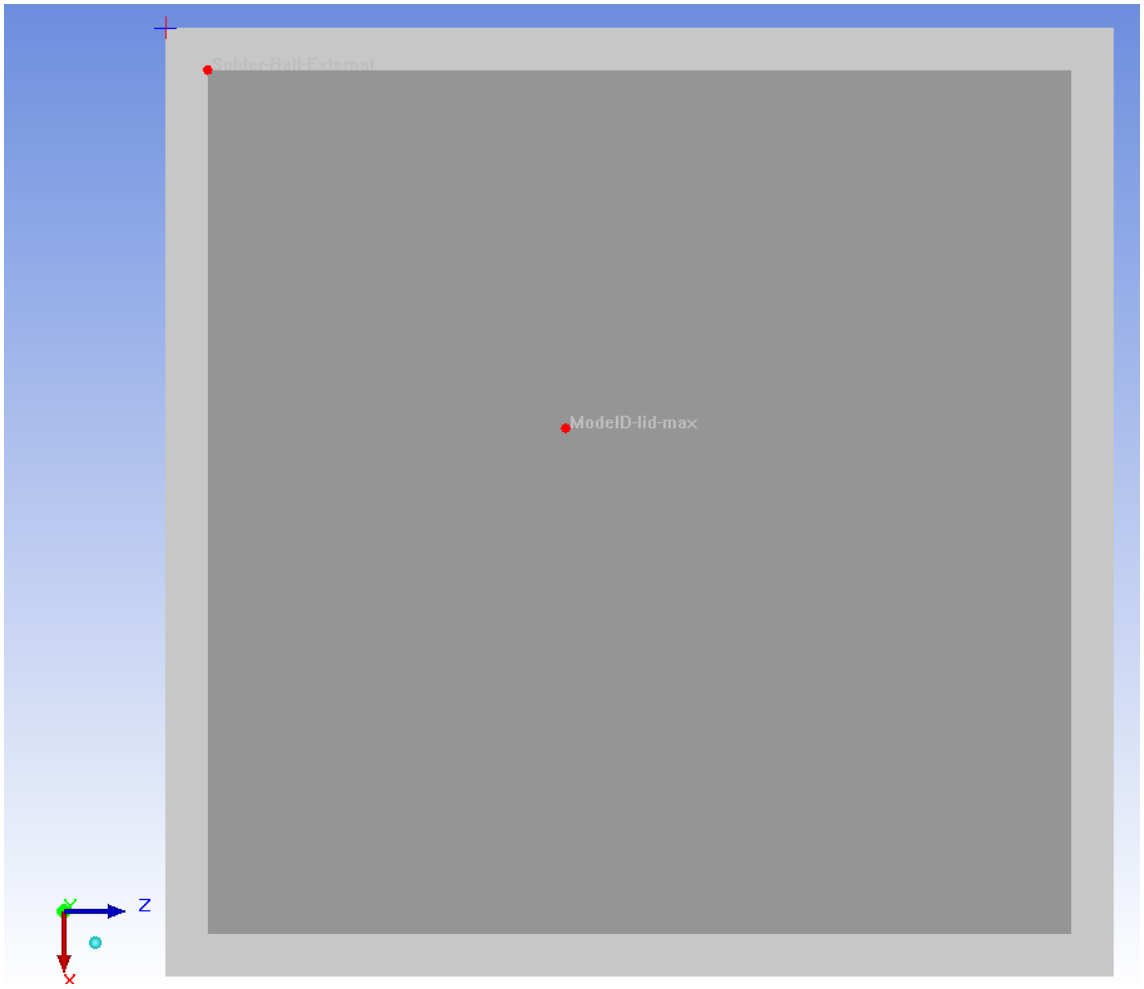
Figure A.2: Points of interest marked on different components of Model III. The points represent the highest temperature point on their respective component.



(a) Points of interest marked on the GR765 and DDR4 chips of Model IV.

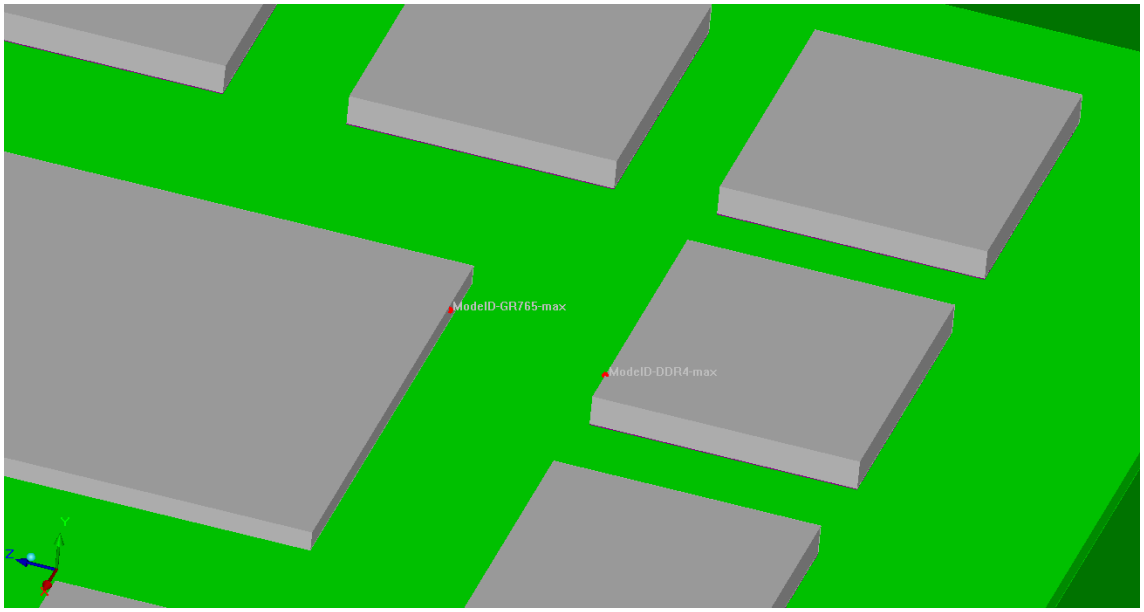


(b) Points of interest marked on the underside of the substrate of Model IV.

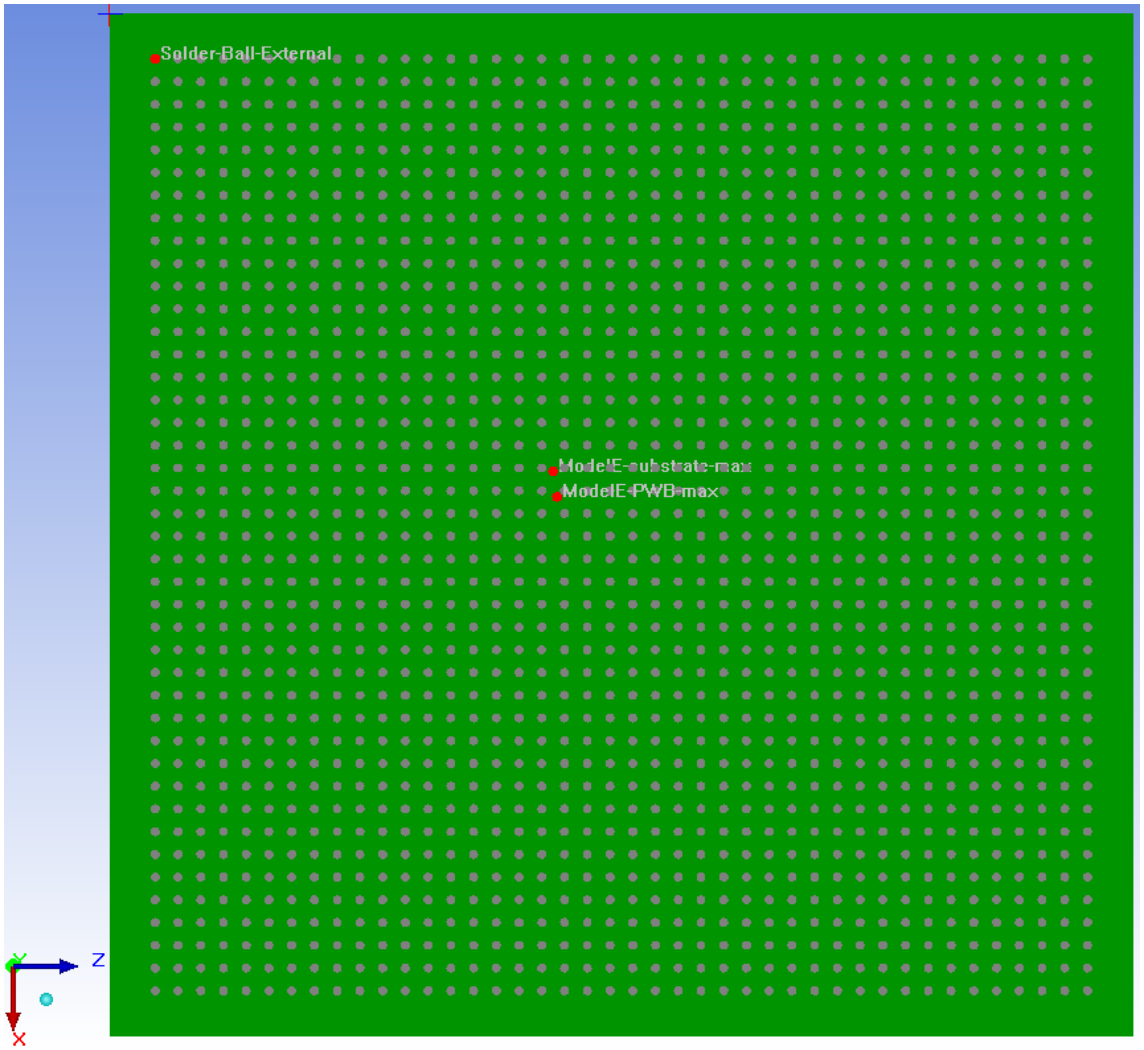


(c) Points of interest marked on the inside of the metal lid of Model IV.

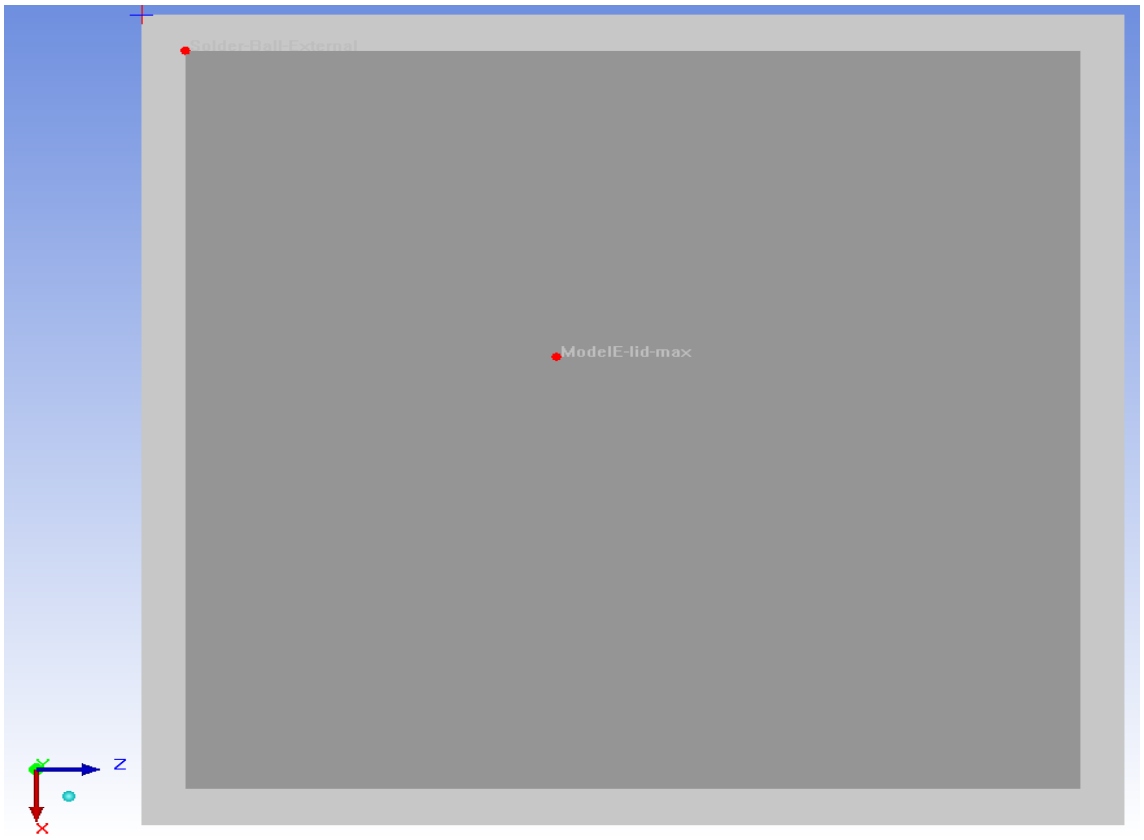
Figure A.3: Points of interest marked on different components of Model IV. The points represent the highest temperature point on their respective component.



(a) Points of interest marked on the GR765 and DDR4 chips of Model V.



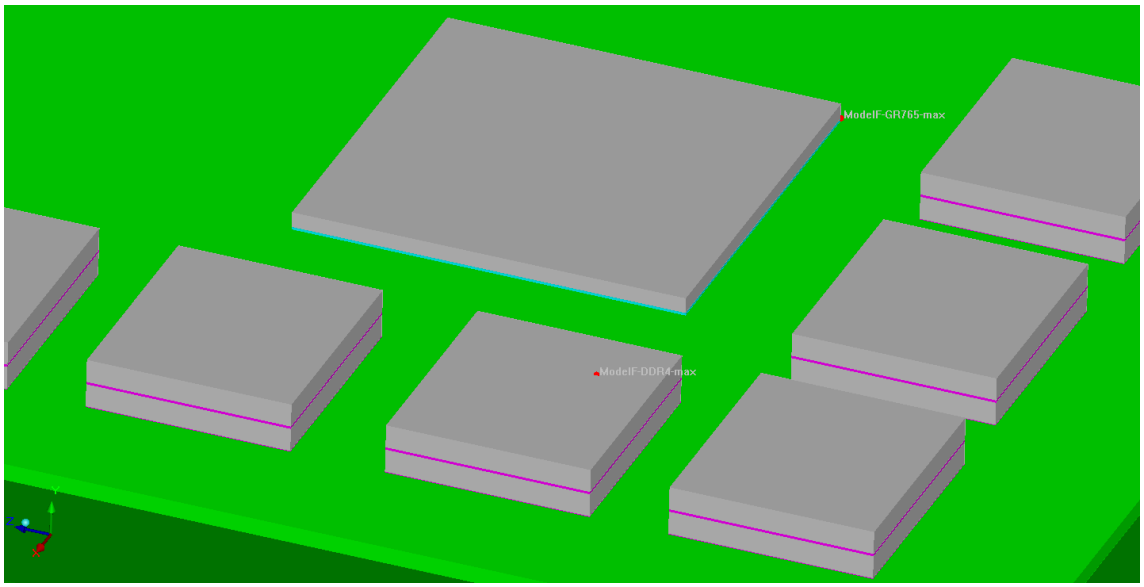
(b) Points of interest marked on the underside of the substrate of Model V.



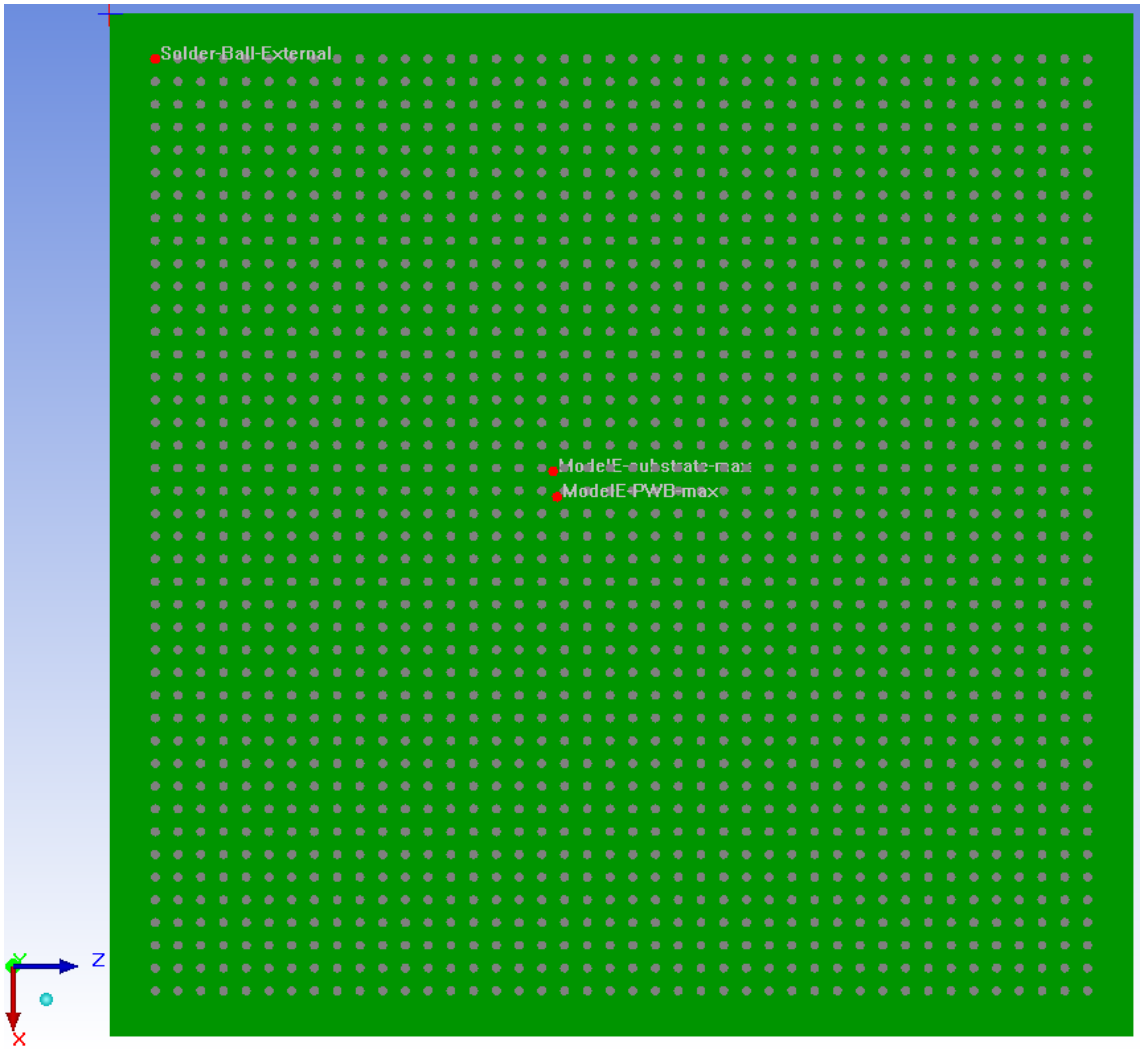
(c) Points of interest marked on the inside of the metal lid of Model V.

(d) Points of interest marked on the underside of the cold plate of Model V.

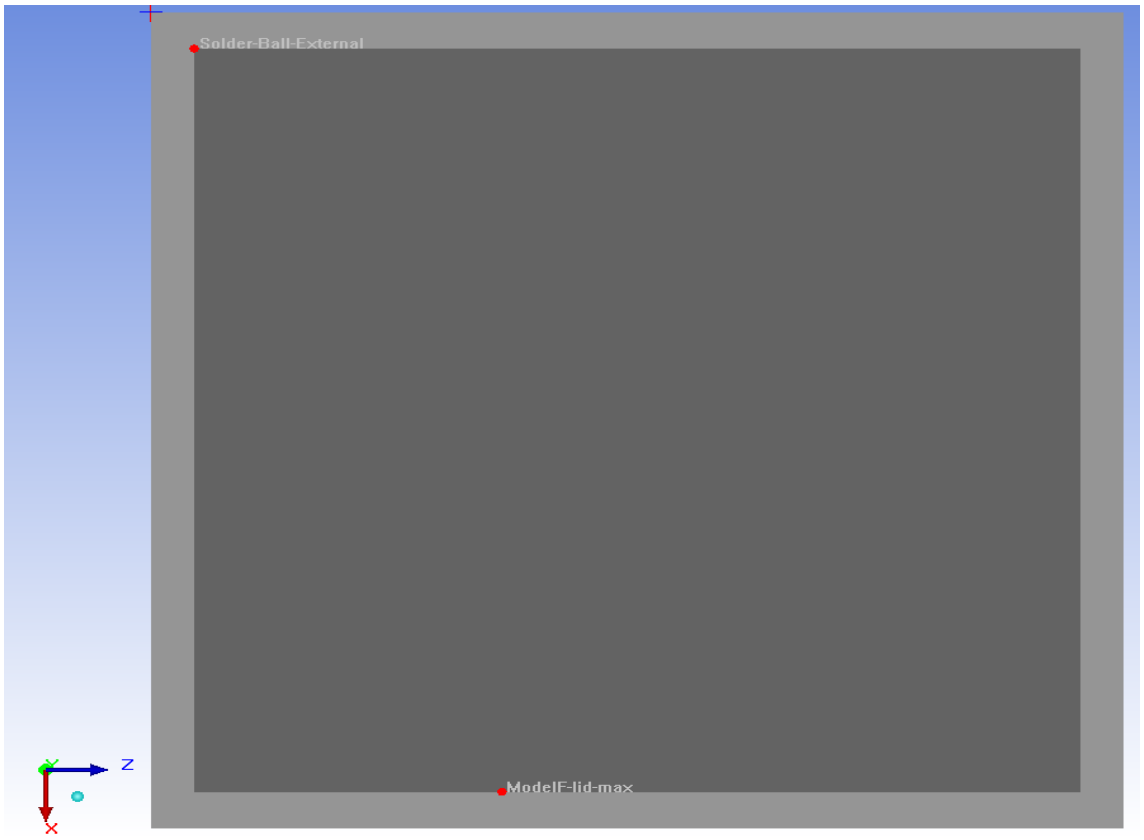
Figure A.4: Points of interest marked on different components of Model V. The points represent the highest temperature point on their respective component.



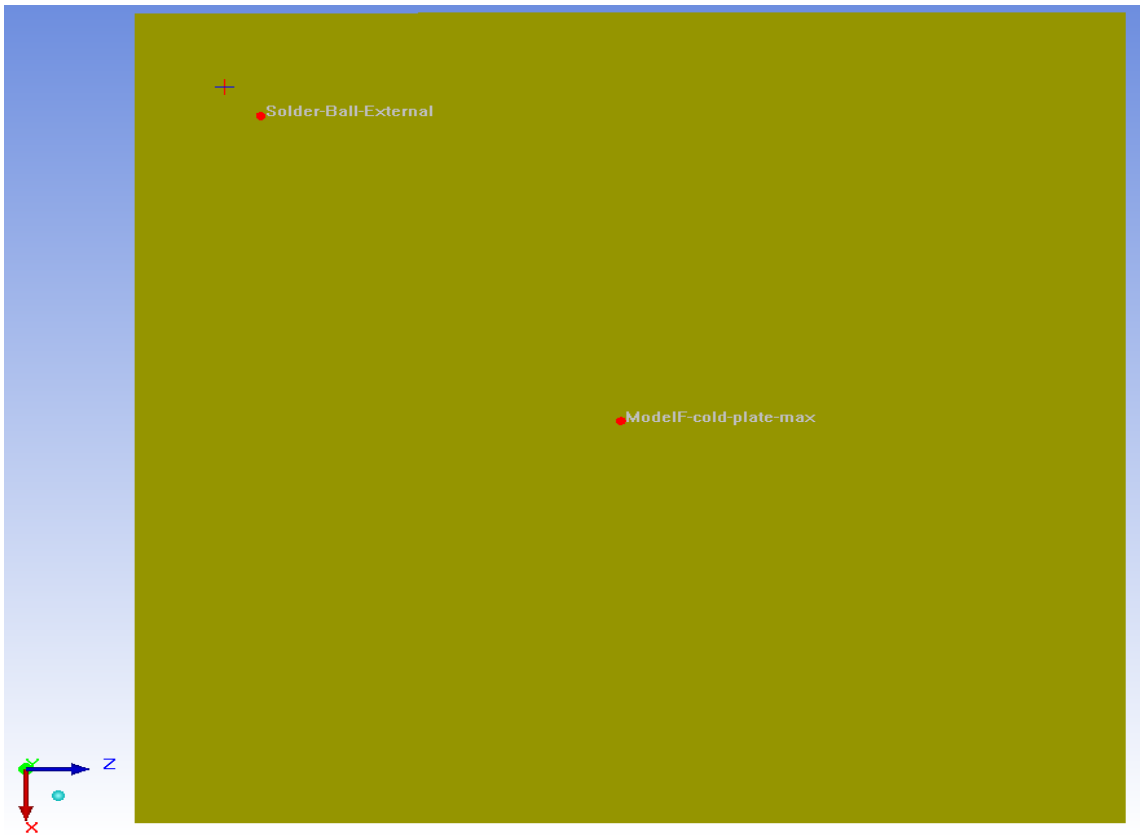
(a) Points of interest marked on the GR765 and DDR4 chips of Model VI.



(b) Points of interest marked on the underside of the substrate of Model VI.



(c) Points of interest marked on the inside of the metal lid of Model VI.



(d) Points of interest marked on the underside of the cold plate of Model VI.

Figure A.5: Points of interest marked on different components of Model VI. The points represent the highest temperature point on their respective component.