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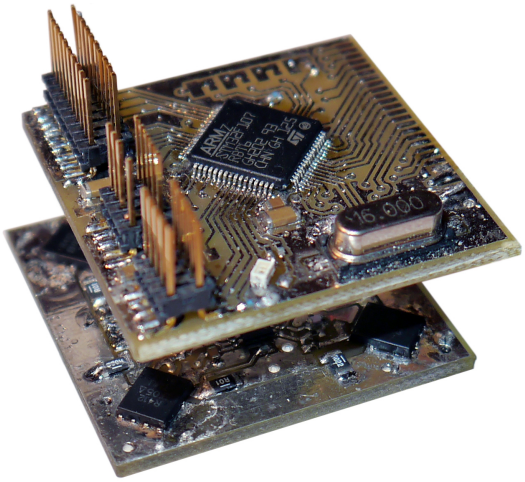

Small Electronic Load

Design and analysis of a small electronic load for testing on-board DC/DC converters

Master of Science Thesis

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Department of Energy and Environment
Division of Electric Power Engineering
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Göteborg, Sweden 2012

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Cover:
A picture of the Small Electronic Load prototype.

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Lukas Rosén, Sahar Samimi
Göteborg, Sweden, 2012

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Abstract

Electronic loads are used at Ericsson AB for test and verification of on-board DC/DC converters. The problem with the existing electronic loads is that they require cables to connect to the board due to their dimensions. Cables will introduce inductance in the load current path and affect the testing results, especially the current slew rate.

In this thesis a new load design is developed which can be soldered directly on the circuit board and eliminating the use of cables. In this way the converters can be tested with higher current slew rates than before, meeting future needs. With the existing electronic loads the maximum achievable current slew rate was 2.5 A/μs from a 3.3 V supply using 80 cm cable. The prototype designed in this thesis managed to achieve 32 A/μs for the same supply voltage.

Index Terms: Active load, Electronic Load, Converter, Current Slew Rate.

Abbreviations

ASIC	Application Specific Integrated Circuit
ARM	Advanced RISC (Reduced Instruction Set Computing) Machine
BJT	Bipolar Junction Transistor
DAC	Digital to Analog Converter
DMA	Direct Memory Access
DUT	Device Under Test
GPIB	General Purpose Interface Bus
I^2C	Inter-Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PMBUS	Power Management Bus
PSU	Power Supply Unit
PWM	Pulse Width Modulation
SRAM	Static Random Access Memory

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Chapter 1

Introduction

Ericsson AB as a world-leading provider of telecommunications equipment and related services to mobile and fixed network operators, has more than 5 million telecommunication sites globally, a number that continuously increases. Different converters and power supplies are used within these sites and they need to be tested to make sure they can reach the required specifications.

1.1 Background

Application-specific integrated circuits or ASICs are now being widely used in circuit design technologies and in telecommunication system design as well. Higher current and current steps with higher slew rates are a need in ASIC and system designs nowadays. Designers try to consider these requirements in all parts of their design process, but due to the process steps and non-ideal conditions in design and manufacturing, the final product always shows some deviation from primary design specifications. It is a challenging process to have a final product with specification as close as possible to the required details.

As an important part of every design, testing and verification of performance aspects are needed in order to produce high efficiency systems and must be done as accurately as possible. When verifying the performance of a designed circuit, it is necessary to create a similar environment to the real situation. Many studies are done in order to increase the precision in the verification step. If testing is done in an accurate way, then the results can be used to improve the system specifications in a way to get results as close as possible to the system requirements.

Switched mode converters are tested using load steps. When testing on-board power supplies at Ericsson AB, different kinds of external electronic loads are used. These external loads are often placed at a significant distance from the converter which means that long cables must be used to connect the equipment together. This leads to high inductance in the load current path, which limits the maximum slew rate. To make the test environment as good as possible, the wire inductance must be minimized so that the tests can be performed with high slew rates.

1.2 Previous Work

There are a few active loads available at Ericsson, one of them is the Chroma 63103A manufactured by Chroma Systems Solutions. As mentioned before, the main problem with this kind of load is the high inductance introduced when connecting it by wire to the circuit board under test. This limits the slew rate and makes it more difficult to test the power supply precisely.

There is one active load designed by Linear Technology which is designed for current amplitudes up to 100 A. This load uses many discrete components which makes it considerably large and not suitable for an on-board design. Additionally, the circuit uses different supply voltages which makes a final design even more complex.

There is also a active load designed by Power Solution department at Ericsson AB. It is close to the design specifications of this thesis and use relatively few components. All these previous designs are studied for better understandings of considerations for active load design.

1.3 Purpose

There are a couple of active loads available at Ericsson, but they all require long wires to reach the converters being tested. The inductance in the long wires will affect the precision and accuracy of the verification process. The purpose of this master thesis is to design a small active controllable load that can be put directly into a socket for an integrated circuit. It will minimize the connection path to the converter output and thereby improve the verification process compared to when using an external electronic load. The active load must be able to simulate the current dynamics of a real integrated circuit and in this way test the converter. The load must be designed for the voltage range 0.2 V – 3.3 V and be able to sink up to 20 A DC with a slew rate of at least 6 A/μs.

Chapter 2

Technical Background

2.1 Power Transistors

Transistors are frequently used within digital integrated circuits where they process information but power transistors process power, hence their packaging and structure is different. The two major desirable characteristics for power semiconductors are the switching speed and power handling capability. Today the most common power transistors are the MOSFET (Metal Oxide Semiconductor Field Effect Transistor), the IGBT (Insulated Gate Bipolar Transistor) and the BJT (Bipolar Junction Transistor). The main difference in terms of performance between the technologies lies within their switching speed, blocking voltage and current capability [1] [2].

2.1.1 MOSFET Transistors

Among the available power transistor technologies the one with the highest switching speed is the MOSFET. The fastest units can handle switching frequencies higher than 1 MHz. This makes them an excellent choice when it comes to designing small power supplies since the energy storage inductor can be made smaller as the frequency increases [2].

The MOSFET can operate in three different regions; cutoff, ohmic and saturation. Figure 2.1 shows the characteristics of an arbitrary n-channel MOSFET transistor. It can be seen that the current flowing between drain and source (I_D), does not only depend on the voltage applied to the gate (V_{GS}) but also the voltage between drain and source (V_{DS}). When the voltage at the gate is lower than the device threshold voltage (V_{TH}), the MOSFET is operating in its cut-off region. No channel is created between drain and source and the MOSFET will not carry drain current. In its ohmic region, the MOSFET can be treated as a voltage controlled resistor. The gate voltage will control the resistance between drain and source. When operating in its saturation region the drain current is independent of the voltage between drain and source.

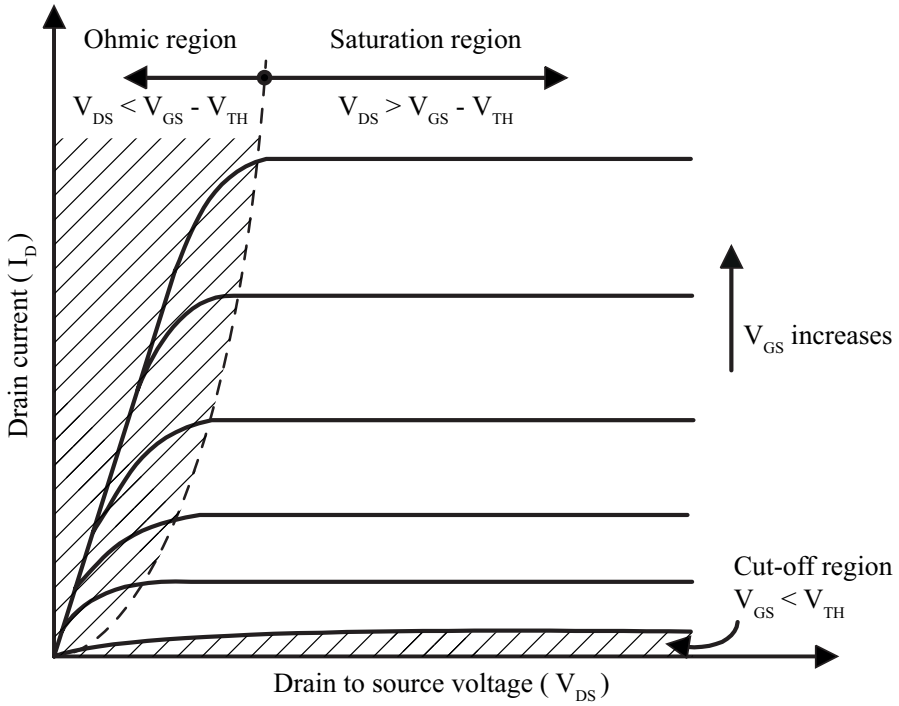


Figure 2.1: Typical MOSFET characteristics

In the ohmic region, the channel of the device acts as a constant resistance, $R_{DS(on)}$. Its relation to V_{DS} and I_D follows ohms law as

$$R_{DS(on)} = \frac{V_{DS}}{I_D}|_{V_{GS}=Constant} \tag{2.1}$$

The value of the on-state resistance $R_{DS(on)}$ varies significantly between devices, from tens of milliohms to a few ohms. It is an important parameter which determines the device forward voltage drop and its power losses. The MOSFET has slightly higher conduction losses compared to the BJT but it's electrical properties are less sensitive to temperature changes.

Between the different regions inside the MOSFET there exist parasitic elements as resistance's and capacitance's due to charge accumulation. The values of these capacitance's are non-linear and a function of device structure, geometry and applied external voltages. The sum of the capacitive elements C_{GD} and C_{GS} which affects the gate is called Miller capacitance, see Figure 2.2. This is an important parameter when using the MOSFET in high speed applications because this capacitance has to be charged via the gate during turn on. The Miller capacitance has to be charged and discharged very fast which must be taken into consideration when designing the gate drive circuit [2].

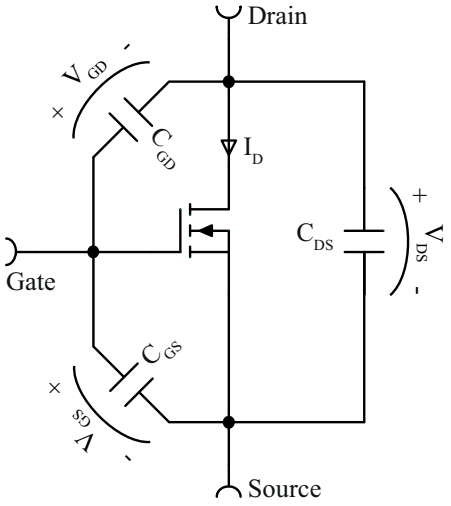


Figure 2.2: Parasitic capacitances, C_{GD} and C_{GS} forming the Miller Capacitance

A power MOSFET uses vertical channel structure in order to increase the device power rating. Figure 2.3 shows the cross section of a vertically diffused n-channel power MOSFET. The difference from lateral channel MOSFETs used in many integrated circuits is that the drain and source are in opposite side of the silicon wafer. When a voltage is applied over the gate conductor, charge carries are gathered under the gate to create a conducting channel between the drain and source. When no voltage or a voltage less than the threshold level (V_{TH}) is applied to the gate, there will be no charge carriers and therefore no current can pass from drain to source. The source has its name because it is the source of the charge carriers and in a similar way the drain is where the charge carriers leave the channel [2].

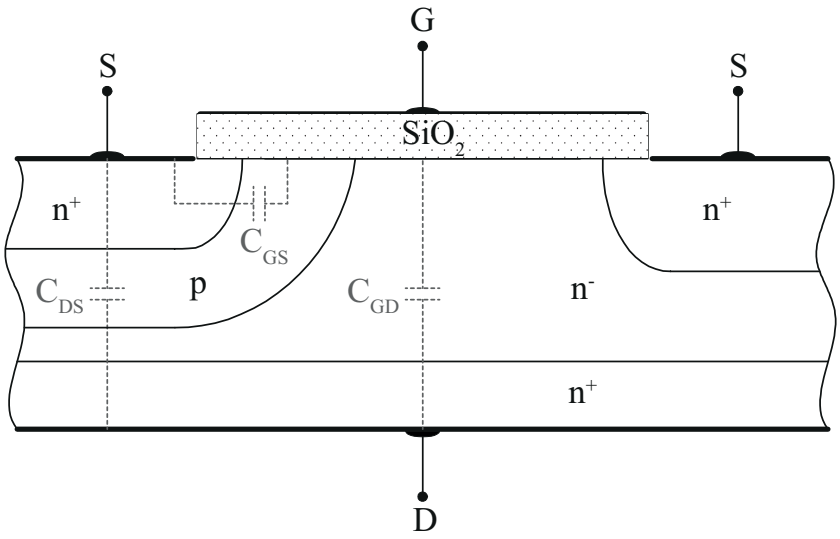


Figure 2.3: Cross section of a vertically diffused n-channel power MOSFET

2.1.2 BJT and IGBT Transistors

A BJT is a kind of transistor which can be treated as a current controlled resistor or amplifier. The current flowing into its base controls a larger current flowing between the collector and emitter. The relationship between the currents is close to static and commonly in the interval 50 to 1000. This transistor is used as a switch or a current amplifier that is controlled by its base current input. At voltages below 500 V, the MOSFET has replaced the BJT and this limit is increasing. There are still some areas where the BJT outperforms the MOSFET, for example they have lower saturation voltages over their operating temperature range. The BJT has a lower input capacitance than the MOSFET and IGBT but is current driven, therefore the drive circuit must provide high and prolonged input currents.

The IGBT have similar conduction properties as the BJT but with a voltage driven gate. It can handle higher switching frequencies, though lower current and voltage specifications. The internal structure of the IGBT combines BJT and MOSFET technologies. A high impedance, voltage driven gate input but with the BJTs higher voltage and current specifications.

One drawback with the BJT and IGBT is that both electrons and holes contribute to conduction. The holes have a relatively long carrier lifetime, therefore the current control abilities for them can be considered as low. The BJT and IGBT are considerably slower at switching than the MOSFET, exhibiting long turn-on and turn-off times. Another drawback with these technologies compared to the MOSFET is that they suffer from thermal runaway. Their forward voltage drop has a negative temperature coefficient and therefore it will decrease with temperature. This makes them hard to connect in parallel for sharing a load because the transistor with highest temperature will take more current than the other ones and thereby worsen the situation further [1].

2.2 Operational Amplifiers and Relevant Application Circuits

2.2.1 The Operational Amplifier

The operational amplifier is a fundamental building block in analog circuits. Its name originates from its usage within analog computers where it can achieve scaling, summation and integration. It is mostly built up by transistors, one operational amplifier consists of about 20 - 50 transistors. The non-ideal operational amplifier has limitations in form of finite gain, bandwidth and input and output resistances, common-mode rejection, offset voltage and bias current [3].

Figure 2.4 shows an internal model for the basic operational amplifier. It has two inputs and one output. The inputs consist of one non-inverting input marked with a plus sign and one inverting input marked with a minus sign. For simplicity the schematic symbol is often drawn without the power and ground pin.

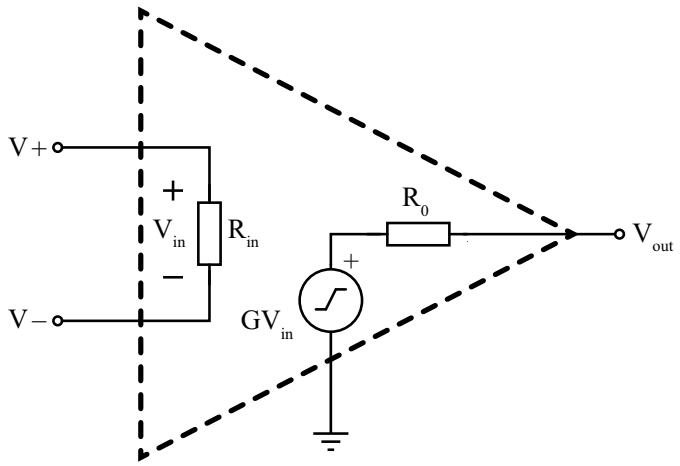


Figure 2.4: Internal model of a basic operational amplifier

The operational amplifiers output is a high amplification of the voltage difference between the inputs. When using an ideal model of the operational amplifier, the input impedance R_{in} is considered to be infinitely large and the output impedance R_0 to be zero. This results in zero current flowing at the inputs and the ability to supply unlimited current at the output without voltage drop. In reality, R_{in} can be a few megaohms and R_0 some tens of ohms.

Several different standard circuits can be designed by using the operational amplifier, this project uses two of them. First it is used as an impedance converter, described in Section 2.2.2 and also as an error amplifier described in Section 2.2.3.

2.2.2 Operational Amplifier as an Impedance Converter

The high input impedance and the low output impedance of the operational amplifier makes it useful as an impedance converter. By feeding the output signal back to the inverting input (see Figure 2.5), the output voltage will follow the non-inverting input but will be able to drive loads without affecting the input signal. The high impedance inputs results in input currents which can be considered to be close to zero. The output is low impedance which makes it able to output currents without significant voltage drop at the output [4]. The impedance converter is found in many sensor and data acquisition applications where it is needed to drive loads with a signal without loss of signal voltage [3].

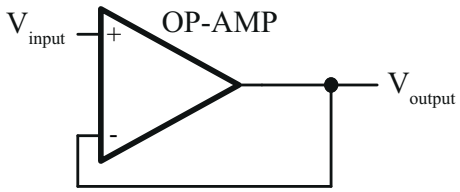


Figure 2.5: Operational amplifier as an impedance converter

2.2.3 Operational Amplifier as an Error Amplifier in a Control Circuit

Within electronics, one of the strong usage areas for the operational amplifier is to use it in controller circuits as an error amplifier. The error signal is the difference between the input reference value and the actual value. The process or variable that needs to be controlled by the output of the operational amplifier is fed back into the inverting input. The result is that the operational amplifier constantly will change its output so that the difference between the inputs gets as low as possible. In a good controller circuit, the operational amplifier will force the feedback signal equal to the signal fed into the non-inverting input. For example voltage regulators works this way and uses a feedback loop to control the output voltage and keep it constant [4].

Figure 2.6 shows the basic control loop used in this thesis. The error signal which is the difference between the input reference signal (V_{input}) and feedback signal ($V_{feedback}$) is amplified to control the MOSFET. The gate voltage controls the current flowing through the MOSFET and the current sensing resistor (R_{sense}) and therefore the feedback voltage. From a functional perspective, the voltage over R_{sense} matches the input voltage.

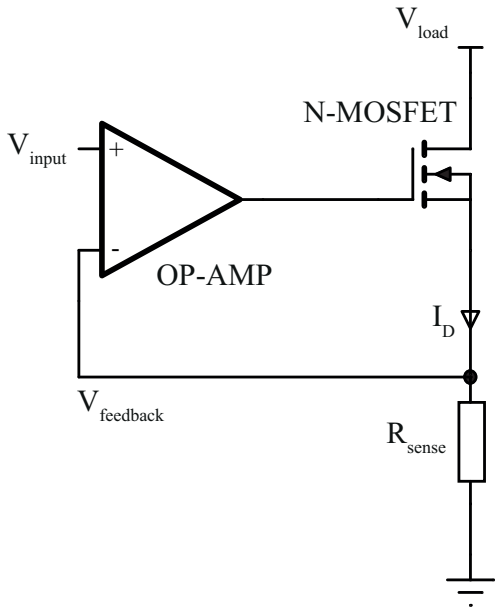


Figure 2.6: Operational Amplifier as an error amplifier

As described in Section 2.1.1, the MOSFET has three different working regions. There is no distinct transition between the different regions and it can change from linear to saturation mode and vice verse very fast. The electrical properties can also vary depending on manufacturing variations, mounting and body temperature. By using feedback that is proportional to the actual current, many of these influencing factors can be eliminated.

2.3 Operational Amplifier Stability

2.3.1 Introduction to Control Theory

A system transfer function can give lots of useful information about the system. The transfer function is calculated using the relation between input and output of a linear time-invariant system. A system transfer function can be written as

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = K\frac{(s-z_1)(s-z_2)...(s-z_m)}{(s-p_1)(s-p_2)...(s-p_n)} \tag{2.2}$$

where H(s) is the rational transfer function in complex variables, V_{out}(s) is the system output and V_{in}(s) is the system input. In this formula, V_{out}(s) is the Laplace transform of the output and V_{in}(s) is Laplace transform of the input signal. Roots to the numerator of 2.2 ($V_{out}(s) = 0$) are called zeros and the roots of the denominator ($V_{in}(s) = 0$) are called poles. System zeros and poles gives useful information about the system behaviour [5].

Another practical tool to represent electronic systems and circuits are block diagrams. Many system specifications can be obtained from system block diagram. Figure 2.7 shows an electronic feedback system in which A is the system gain and β is the feedback gain.

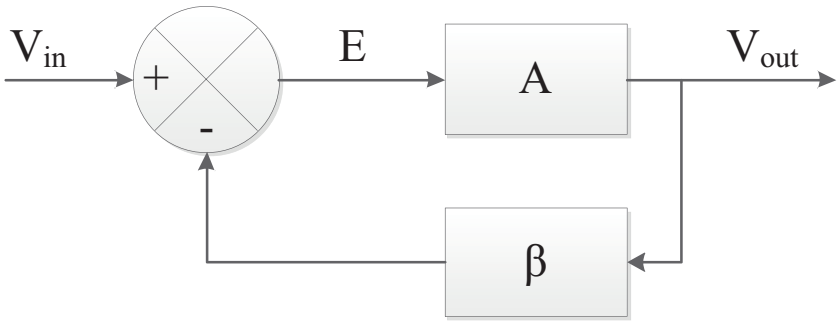


Figure 2.7: Electronic feedback system block diagram

The output signal in Figure 2.7 can be represented as

$$V_{out} = EA \tag{2.3}$$

in which A is the open loop gain. The signal E is called the error and it is the difference between the input signal and the fed back output signal with the feedback gain β. Substituting E gives

$$V_{out} = (V_{in} - \beta V_{out})A \tag{2.4}$$

By rearranging 2.4, it becomes

$$\frac{V_{out}}{V_{in}} = \frac{A}{1 + A\beta} \tag{2.5}$$

It can be seen from 2.5 that if the system gain (A) and feedback gain (β) are large, the system gain is defined by feedback gain as

$$\frac{V_{out}}{V_{in}} = \frac{1}{\beta} \tag{2.6}$$

The equation shows that the ideal system with passive components in the feedback, is controllable and stable. The product Aβ is called the loop gain. If the loop gain as a complex number reach -1 ($|1| \angle -180°$), then 2.5 go towards infinity [6].

In order to check the system specifications using transfer functions, a bode plot can be used. The system frequency response is plotted against frequency in two different plots, one magnitude plot with the voltage gain in dB and one phase plot with the phase shift in degrees. The frequency axis is plotted in log-scale with each grid step representing one decade (x10 increase in frequency). By using the bode plot it is easy to locate system poles and zeros. Every pole in the transfer function represents a -20dB/decade slope change and every zero represents a +20dB/decade slope change in the magnitude plot starting at the pole/zero location. In the phase plot, each pole makes a -90° phase shift and each zero makes a +90° phase shift. The phase shifts are centred around the pole/zero location and starts one decade before and ends one decade after.

A first-order system with a single pole can be represented by a simple RC low pass filter, see Figure 2.8. The transfer function for the circuit is calculated as

$$H_{LP}(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{sRC + 1} \tag{2.7}$$

with the pole location frequency calculated as

$$f_p = \frac{1}{2\pi RC} \tag{2.8}$$

The corresponding Bode plot can be seen in Figure 2.9.

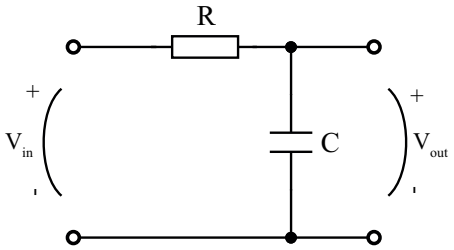


Figure 2.8: RC low pass filter circuit

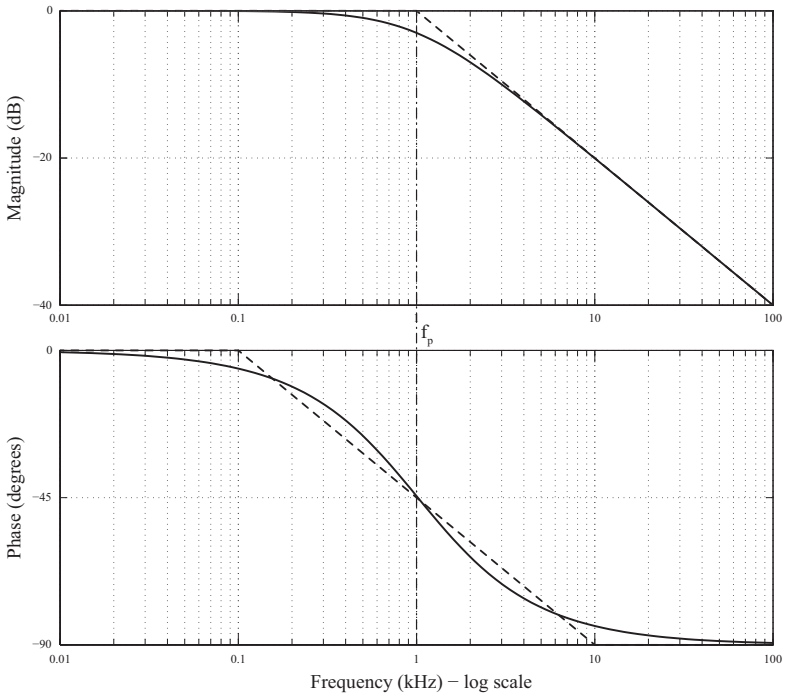


Figure 2.9: Bode plot for RC low pass filter

A RC high pass filter, see Figure 2.10, represents a first-order system with both a zero and a pole. The transfer function of the circuit is calculated as

$$H_{HP}(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{sRC}{sRC + 1} \tag{2.9}$$

The zero is located at zero frequency in this case and is contributing with +90° phase shift for all frequencies. This is the reason behind the phase plot starting at 90° instead of 0° as for the RC low pass filter. This is also the causes the magnitude plot to start with a +20dB/decade slope. The pole location is the same as for the RC low pass filter if using the same value for the product of R and C, see 2.8. In this case the pole will change the slope of the magnitude plot to zero and the phase shift will be -90°, see the Bode plot in Figure 2.11 [7].

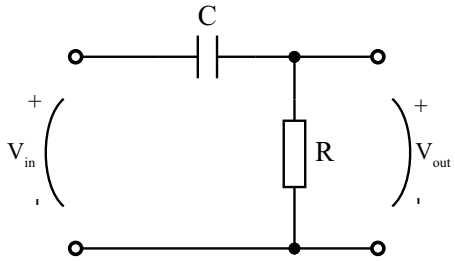


Figure 2.10: RC high pass filter circuit

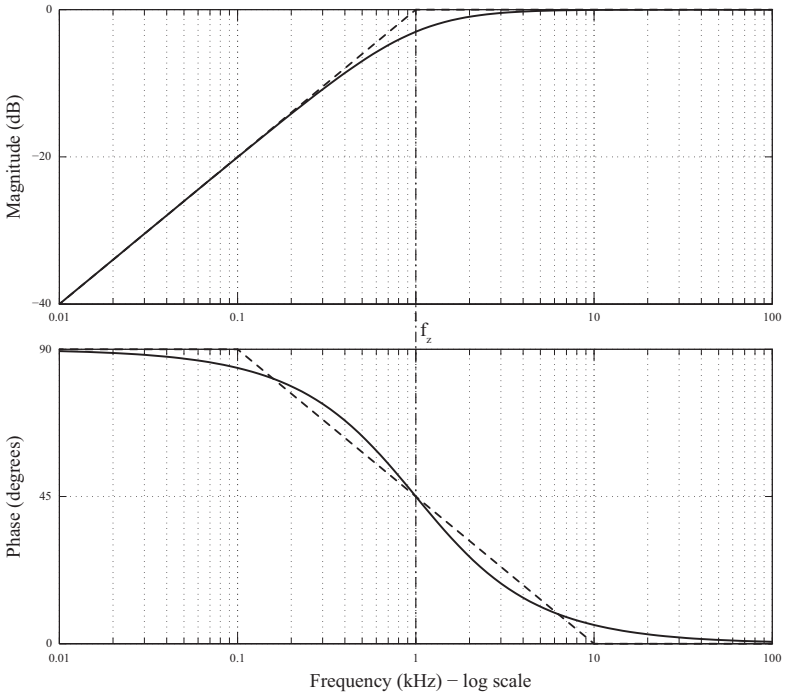


Figure 2.11: Bode plot for RC high pass filter

2.3.2 Stability Analysis

An important property that must be taken into account is the system stability. The system must be designed in a way that prevents oscillations and overshoots as much as possible. Different operational amplifiers have different stability properties. It is common that the amplifiers are internally compensated and therefore stable within load limits defined in their specifications. Uncompensated amplifiers requires external components in form of impedance feedback networks to ensure stable operation. Even internally compensated amplifiers can become unstable if they are driving loads outside its specifications, especially when driving capacitive loads or when capacitive loads are present at their inputs. Unstable internally compensated amplifiers can also be stabilized using external feedback networks [6].

In 2.5, the value Aβ is an important factor called the loop gain. If it reaches -1 ($|1| \angle -180°$), the transfer function gain in 2.5 will go towards infinity. Any small changes in the input voltage will result in large changes in the output voltage. The feedback network will send the output signal back to the input of the system which will amplify it once again. This behaviour will cause oscillations and instability in system [8]. The critical value of Aβ can be expressed as

$$A\beta = -1 = |1| \angle -180° \tag{2.10}$$

Two terms commonly used to describe the stability of a closed-loop control system are the phase and gain margins. The Bode plot in Figure 2.12 shows how to extract the margins from an existing plot.

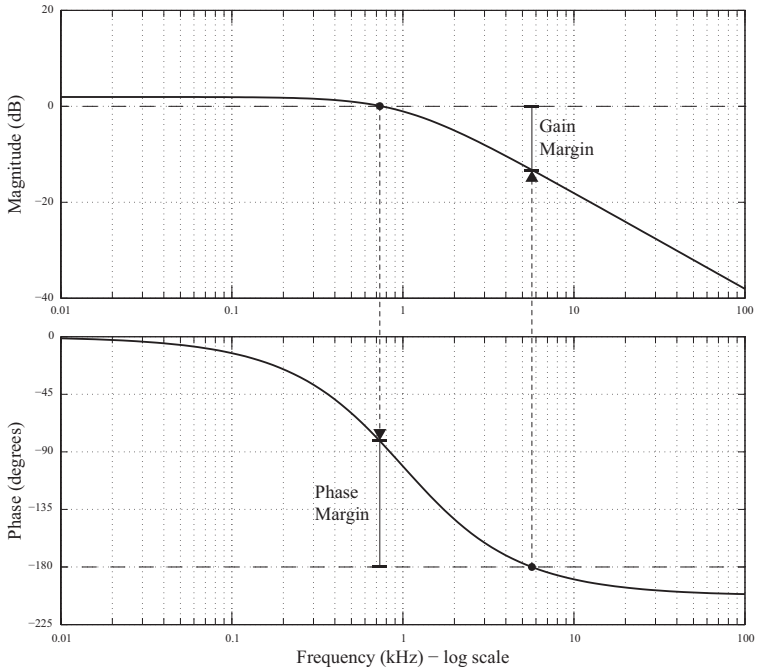


Figure 2.12: Bode plot describing phase and gain margin

The phase margin indicates relative stability, the tendency to oscillate during its response to input changes. It indicates how far the system is from the critical point in 2.10. It is defined as the difference in degrees between the critical -180° and the phase value at the point when the magnitude plot crosses 0 dB (unity gain) as

$$PM = \arg[A\beta(j\omega_{0dB})] - (-180°) \tag{2.11}$$

The gain margin shows how much the gain can be increased before reaching the critical point. It is defined as the difference in dB between unity gain (0 dB) and the gain where the phase plot crosses -180° as

$$GM = -A\beta(j\omega_{-180^\circ}) \tag{2.12}$$

In a system consisting of an operational amplifier with feedback, the phase margin for the loop gain gives a good measurement of the stability. As a rule of thumb, a system is considered to be sufficient stable if the phase margin is larger than 45° [8].

2.3.3 Operational Amplifier with a Capacitive Load

A drawback with the MOSFET is its gate capacitance which complicates the control, at least in high speed operation. When driving a capacitive load as the MOSFETs gate capacitance directly from the operational amplifier, instability problems can occur if the capacitance is large. Figure 2.13 shows the internal model of the operational amplifier with its output resistance (R_0) and with a load capacitance (C) connected to the output.

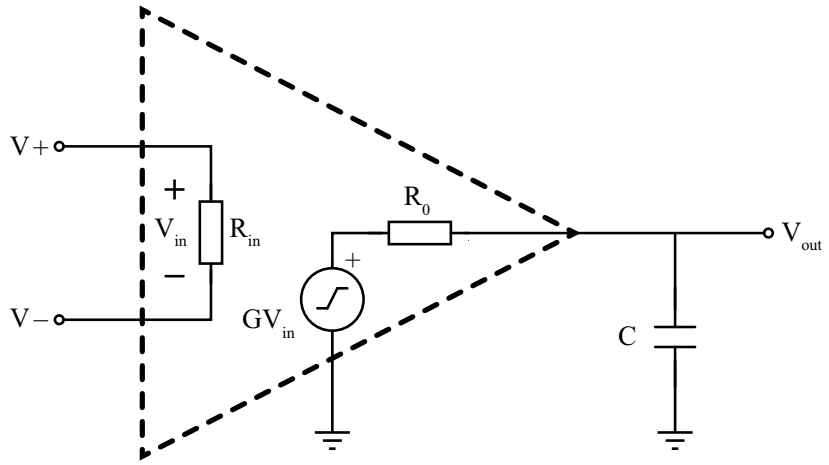


Figure 2.13: Internal model of the operational amplifier with a capacitive load at the output

The operational amplifiers output resistance (R_0) and the capacitive load (C) forms an low pass filter as the circuit in Figure 2.8. As mentioned in Section 2.3.1, the RC low pass filter introduces a pole in the system transfer function and its location can be calculated as

$$f_p = \frac{1}{2\pi R_0 C} \tag{2.13}$$

This extra pole can cause instability problems, especially when the product of R_0 and C is big. The pole frequency location will then decrease. An extra pole at low frequencies often results in smaller phase margin because the pole will shift the phase faster than the gain. The phase shift will occur earlier and further away from the unity gain crossing in the magnitude plot. As mentioned in Section 2.3.2, the phase margin should be above 45° for the system to be considered as sufficiently stable.

2.4 Conductor Inductance

Electrical conductors consist of parasitic elements as capacitance, inductance and resistance. Lumped models where a few discrete components represents a length unit of a cable is often used to simplify calculations. When transferring high slew rate currents the conductor inductance will have the largest impact.

The self-inductance in a free hanging conductor with circular cross section in air can be approximated as

$$L \approx 2 * 10^{-7} l(\ln \frac{2l}{r} - 1) \tag{2.14}$$

the equation is valid if the conductor length (l) is considered to be much larger than the conductor radius (r), $l \gg r$, which is common in practical cases [9].

Figure 2.14 shows a simplified active load circuit with a power supply, a conductor that connects the units and an active load. The conductor is treated as a pure inductance in this case and the return conductor is assumed to be ideal.

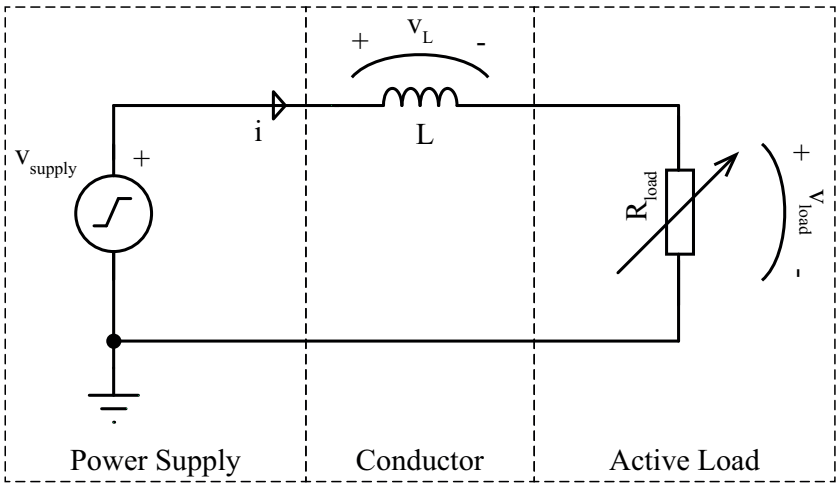


Figure 2.14: Simplified circuit with pure inductance conductor

The voltage over the inductor is equal to the product of the inductance and the current derivative as

$$v_L = L\frac{di}{dt} \tag{2.15}$$

in which v_L is the voltage over the inductance, i the current flowing through it and L is the inductance in H. The current flowing in the circuit can be calculated using Kirchhoff's voltage law as

$$v_{supply} - v_L - v_{load} = 0 \tag{2.16}$$

Rearranging 2.16 and substitute with v_L from 2.15 gives

$$v_{load} = v_{supply} - L\frac{di}{dt} \tag{2.17}$$

By applying ohms law on the active load resistance R_{load} and substitute v_{load}, it becomes a differential equation as in 2.18 with the solution in 2.19.

$$i = \frac{v_{supply} - L\frac{di}{dt}}{R_{load}} \tag{2.18}$$

$$i = \frac{v_{supply}}{R_{load}}(1 - e^{-\frac{R_{load}}{L}t}) \tag{2.19}$$

The current i is a exponentially growing function with the time constant calculated as

$$\tau = \frac{L}{R_{load}} \tag{2.20}$$

The time constant is proportional to the inductance and inversely proportional to the resistance. Increasing the resistance will limit the maximum current in the circuit which is not desirable. To decrease the time constant the conductor inductance must be minimized [10].

The average slew rate during the first time constant, $0-\tau$, is calculated by 2.21. The time constant denotes the time needed to reach 63 % of the final value $0.63i_{max}$. The parameters affecting the current slew rate is not only the inductance as shown in 2.21, but also the supply voltage. Lowering the voltage when the inductance is constant will decrease the current slew rate.

$$\frac{di}{dt} = \frac{0.63i_{max}}{\tau} = \frac{0.63i_{max}}{\frac{L}{R_{load}}} = \frac{0.63\frac{v_{supply}}{R_{load}}}{\frac{L}{R_{load}}} = \frac{0.63v_{supply}}{L} \tag{2.21}$$

2.5 Pulse Waveform Generation

In digital circuits a signal can only have two distinct states, either on or off. Digital outputs works in the same way, if the system voltage is 3.3 V then it is either 3.3 V or 0 V. When there is a need to produce an output voltage that is in between these levels a form of Digital-to-Analog Converter (DAC) is needed. The DAC methods relevant for this project are described in chapter 2.5.1 and 2.5.2.

When the shape of the test pattern or pulse has been decided, it must be created as a voltage pulse which will be transformed to a current pulse in the active load circuit. This can be done in many different ways but the most important factor for this application is that it will be easy to configure and change.

2.5.1 DAC using Pulse Width Modulation (PWM)

Constructing analog voltages with this method involves high frequency switching between two output states, on or off. If the user demands a voltage that is half of the system voltage the duty cycle must be set to 50 %, which means that the output is high for half the switching period and low for the other half. This gives an average value that corresponds to 50 % of the on-state output voltage. To achieve a smooth output waveform and not a high frequency pulse train with varying duty cycle a low pass filter is often used. Figure 2.15 shows the output voltage when using PWM together with a low pass filter. In order to achieve a smooth waveform, the switching frequency needs to be much higher than the frequency of the signal that should be generated.

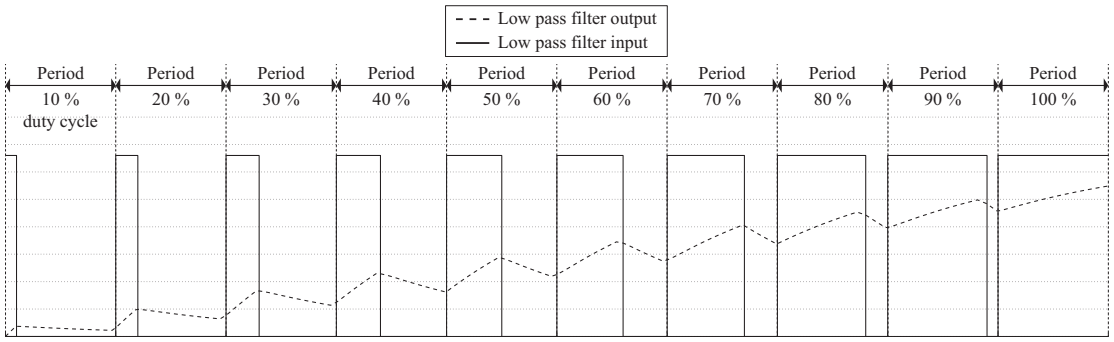


Figure 2.15: Digital to Analog Converter (DAC) using Pulse Width Modulation (PWM)

2.5.2 DAC using Integrated Resistor Strings

Many microprocessors with built in Digital to Analog Converter (DAC) functions use integrated resistor strings to convert a digital signal to an analog. The resistor string contains 2^b resistors with equal resistance connected in series between the supply voltage and ground. A small current will flow through the resistors and create an equal voltage drop over each one.

The digital signals controls 2^b number of switches. Writing a digital value to the DAC will set the switches in the corresponding positions and creating a voltage path from the resistor string to the output. The digital value determines how many of the resistors in the string that are connected between ground and output. With equal voltage drop over each resistor, the output voltage can be calculated as

$$V_{out} = \frac{V_{ref}}{2^b} DAC \tag{2.22}$$

where V_{out} is the output voltage, V_{ref} the supply voltage and DAC is the register value in base 10. In Figure 2.16, a 2-bit resistor string DAC is illustrated. For higher resolutions, the pattern is expanded with more resistors and switches, common resolution values are 8 and 12-bit [3].

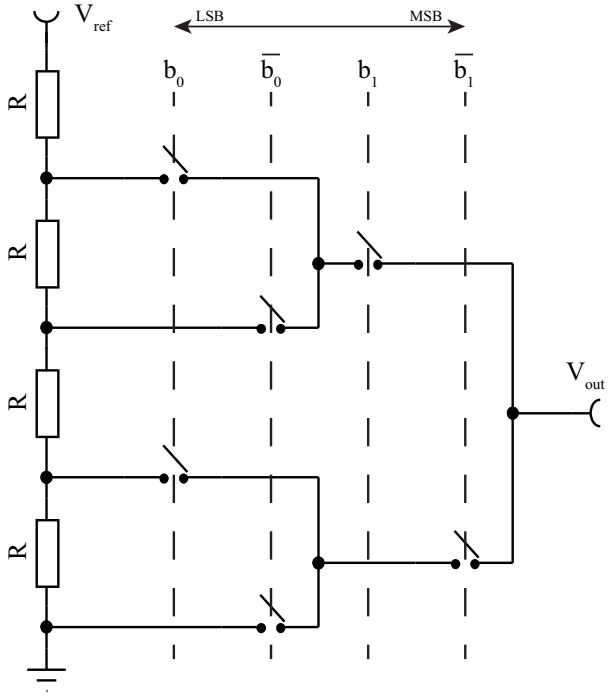


Figure 2.16: 2-bit resistor string Digital to Analog Converter (DAC)

2.5.3 Direct Memory Access (DMA)

Direct Memory Access is a built in function in most medium and high performance microprocessors. The main idea is to perform data transfers between registers in the microprocessor without occupying the CPU. Figure 2.17 shows the DMA functionality towards a DAC. Digital sample values that are to be converted into a analog value by the digital to analog converter (DAC) are stored in arrays in the memory.

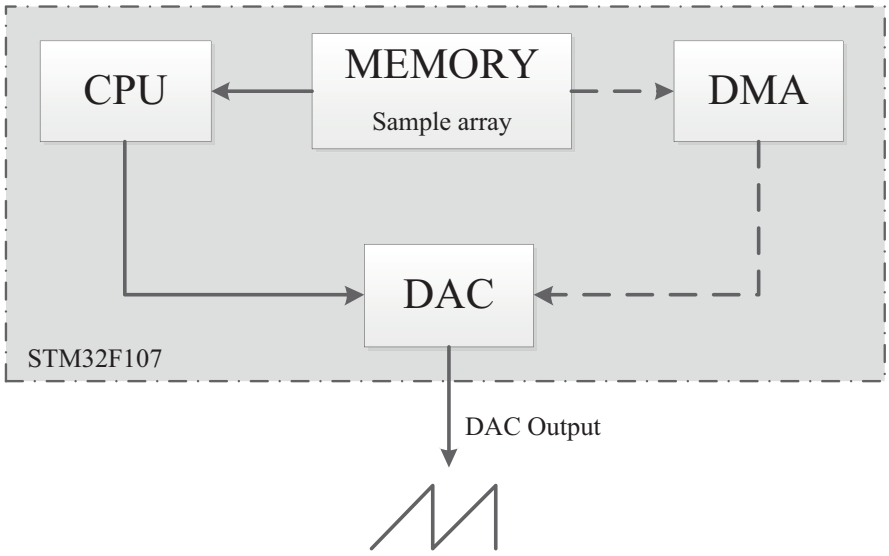


Figure 2.17: Block diagram describing Direct Memory Access functionality in data transfer between memory and the Digital to Analog Converter registers

When not using DMA, the CPU has to pick the data from the memory and transfer it to the DAC registers. The data follows the solid line in Figure 2.17. When using DMA, the data can be transferred directly from the memory to the DAC registers without having the CPU involved. The data follows the dotted path in Figure 2.17. Dedicated data transfer using a DMA controller is faster and gives the possibility to use the CPU for other purposes simultaneously [11].

Chapter 3

Available Active Loads Designs

As mentioned in Section 1.2, there are some active loads and similar circuits available. In this project, three active loads are studied in the following section. The first one is the external active load used in Ericsson laboratory. Then the circuit designed by Linear Technology will be discussed which has good performance with similar specification to this project. The third one is a design done in Power Solution department at Ericsson AB and is used as the basis for this project.

3.1 Introduction to Active Loads

An active load is a circuit which acts like a current-stable non-linear resistor and consists of active components such as transistors. Active loads can be used for testing power supplies or other electrical power sources. They are used to compare the output voltage and current of these sources with the required specification during loading.

The main idea is to use the active load to simulate the behaviour of a set of resistors with different values by using active components such as MOSFETs. The active load resistance value is controlled using electronic control [3].

Device under test (DUT) and the specification of the testing process must be defined carefully when using an active load in order to optimize the load specifications. Some of the specifications include:

- Lowest and highest desired current level
- Specific measurements setup
- Number of DUTs [12]

3.2 BJT Based Designs

There are some available active load solutions using BJTs. Often they are used in the form of a Darlington pair. In this pair one transistor controls the base current to the second one and therefore effectively achieves a higher gain. As explained in section 2.1.2, the BJT is a slower device compared to the MOSFET and also requires prolonged drive currents since it is current driven. The solutions for power supply testing using this technology are therefore of the static kind with a constant loading and slow current dynamics.

3.3 Chroma 63103A

Chroma is one of the world leaders in DC electronic load manufacturing. These loads can be used in many different applications such as power supply testing, battery testing and automatic test systems.

The Chroma 6310/A series is suitable for testing of multi-output power supplies and power components due to its multi-channel set up. It provides parallel operation of modules which can work synchronously to perform high power testing. Also the user can use the modules independently and test 8 DUTs at the same time. Figure 3.1 shows the Chroma 6310/A series system block diagram.

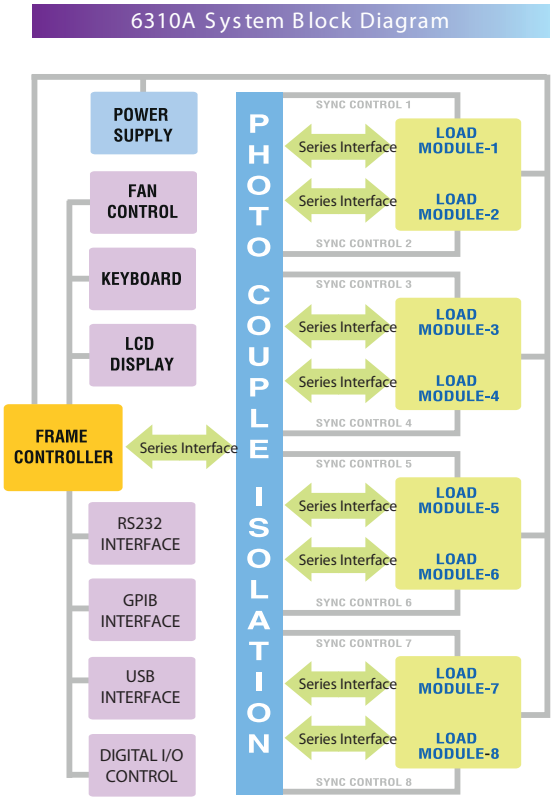


Figure 3.1: Chroma 6310/A System Block Diagram

The user is able to configure the setup parameters manually for the load with power ratings from 100 W to 1200 W and current ratings from 0.5 mA to 240 A. The control abilities are good since the user can set the values for slew rate, current levels, timings and satisfy the needs for fast dynamic operations. Figure 3.2 shows the programmable parameters of Chroma 6310/A series [12].

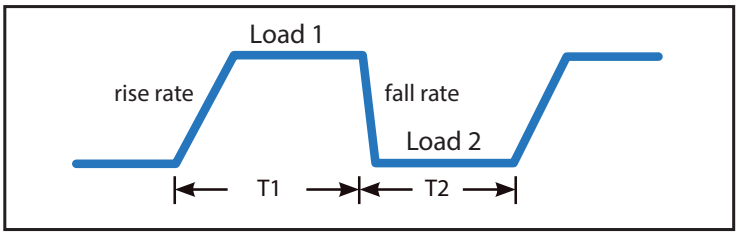


Figure 3.2: Chroma 6310/A programmable parameters

In Figure 3.3, the control part of this load on the right side and four load modules to the left. The loads in this series also have USB, GPIB and RS-232 interfaces which makes it easy to connect to different control units.

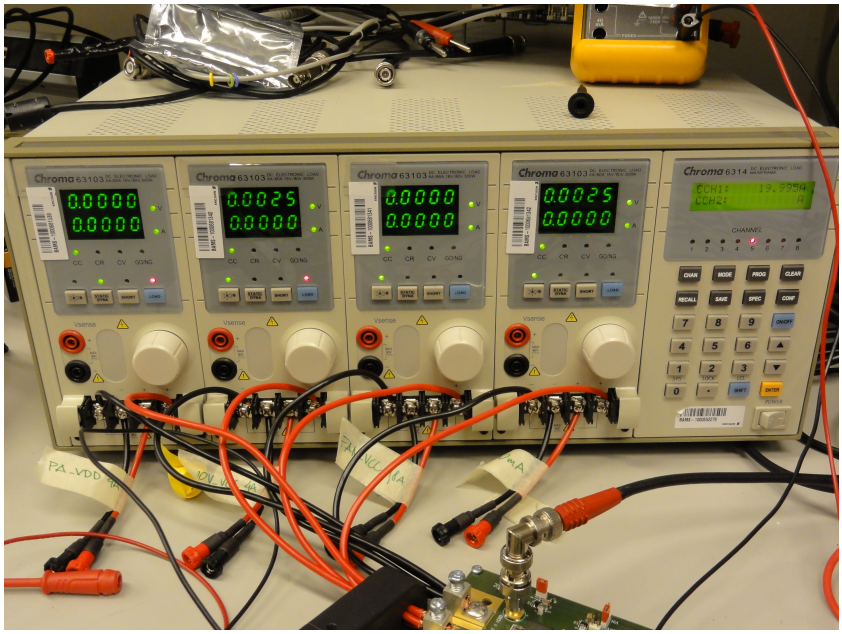


Figure 3.3: Chroma 6310/A mainframe equipped with Chroma 63103A load modules

The electronic DC load module chosen to be analysed is the Chroma 63103A which is rated up to 60 A, 80 V and 300 W. The most important parameter for this project is the slew rate and its maximum rating is 2.5 A/μs. There are a few different models of Chroma loads in Ericssons laboratory, but Chroma 63103A has the fastest current slew rate specification among them and is used in applications where the DC/DC converters has to be tested with high slew rate currents. The active load modules in the Chroma uses several MOSFET transistors in parallel to lower the minimum input resistance. This will make them able to sink high current at low voltage levels (60 A at 1 V) and allow high power dissipation.

3.4 Linear Technology Design

As a comparison for what was needed in this project, one of the latest load designs done at Linear Technology is chosen. This design is an active load test circuit which can be used to test power supplies up to current levels of 100 A. It can act as a DC-load for power supply and also switch between DC levels. The circuit is a closed-loop, 50 kHz bandwidth active load with linear response [13].

Figure 3.4 shows the concept of the design. The DUT drives a constant load R_{dcload} and a switch controlled load $R_{switched}$. The position of the switch represents two different current levels, one with only R_{dcload} and one with both resistors in parallel. At the output, current and voltage can be measured.

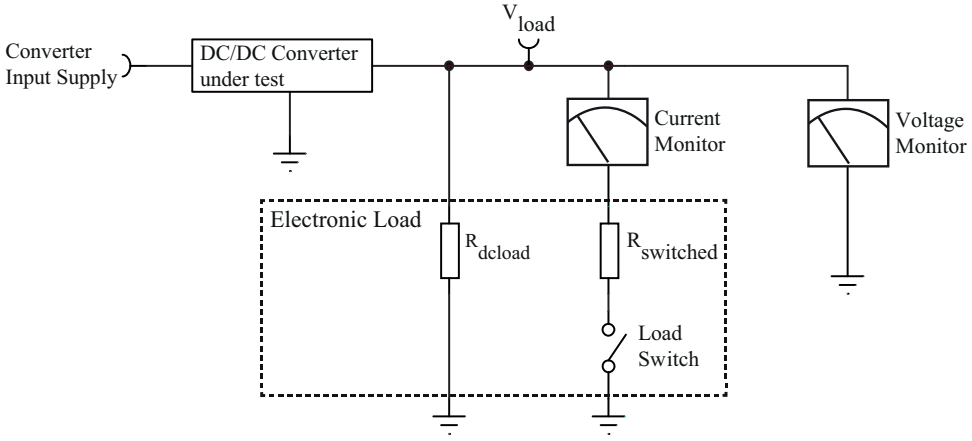


Figure 3.4: Linear Technology conceptual design

To make the load faster and more controllable, a transistor is added instead of the switch, see Figure 3.5. By using a MOSFET as a switch, the drain current becomes controllable by the gate voltage. In this design, the input signal switches the MOSFET via a gate-driver stage; the load current flows through the switch and is monitored and compared against the voltage output of the converter.

In order to control the load linearly and to compensate for instability in the transistor output due to the gate capacitance, a negative feedback is added, see Figure 3.6.

The feedback from R_{sense} to the controller (error amplifier) forms a control loop and the value of the current-sense resistor sets the scale of the feedback voltage which is linear to the current flowing through the MOSFET. When the voltage at 'Input Pulse' changes, the input pins of the amplifiers will get different voltage values. As explained in section 2.2.3, the operational amplifier will act as an error amplifier to control and minimize the voltage difference at the input pins. The operational amplifier will change the voltage at the gate of the MOSFET (T_{mosfet}) until the voltage over R_{sense} match the input of the amplifier.

The complete design is improved by adding more components, such as a differential amplifier in feedback loop to provide high-resolution sensing. Also a gate-drive stage is used to isolate the transistor's gate capacitance from the amplifier. A complete schematic of the design is found in Appendix A.1.

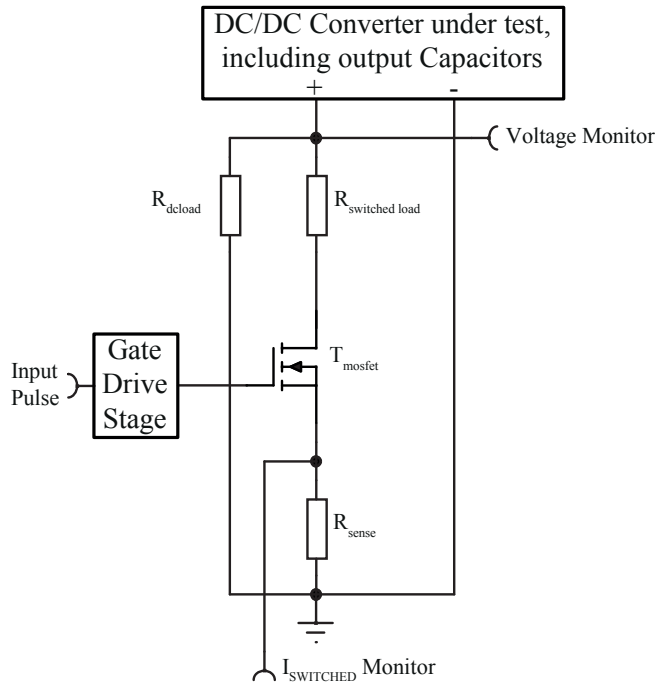


Figure 3.5: Linear Technology FET-based active load tester

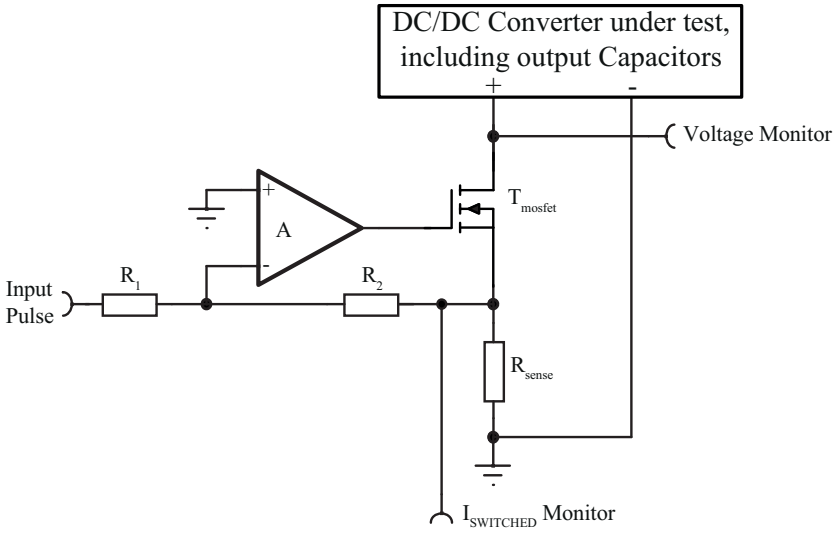


Figure 3.6: Linear Technology design with feedback control

3.5 Power Solution Department, Ericsson AB Design

There has been one active load design developed in Power Solution department at Ericsson by Martin Svensson [14]. Figure 3.7 shows a schematic of this design in which the load current is 1 A for each 100 mV input voltage.

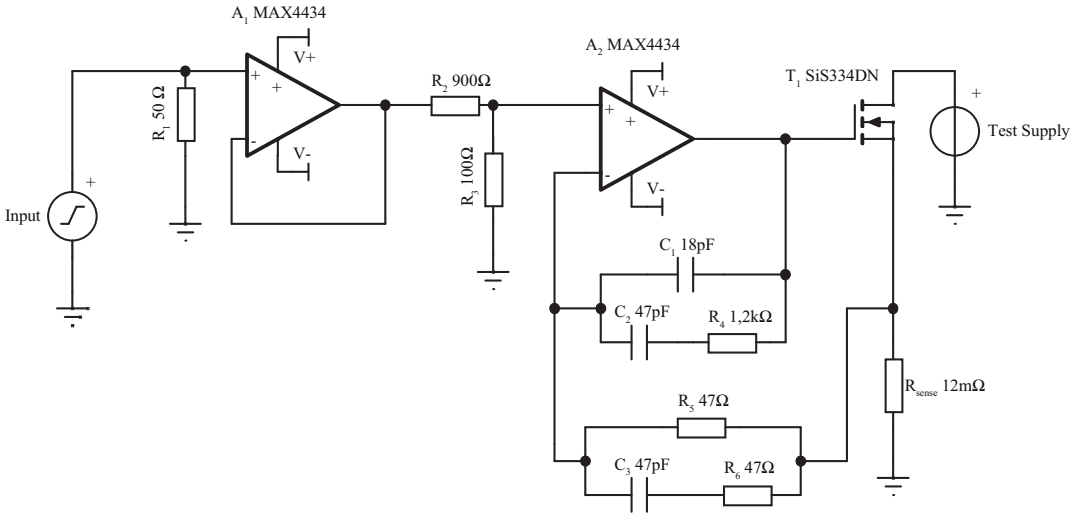


Figure 3.7: Power Solution department, Ericsson AB Design

In the specifications of this circuit, the maximum pulse width is set to 50 μs and the maximum duty cycle is set to 5 %. As shown in Figure 3.7, there are two stages of operational amplifiers. The first stage is used as an impedance converter as described in Section 2.2.2. The output of the first amplifier will drive the voltage divider and the second operational amplifier without loading the input. The second amplifier acts as an error amplifier (see Section 2.2.3) which controls the MOSFETs gate and thereby the drain current that flows through the MOSFET and the current sensing resistor. Any change in the current through the current sensing resistor will result in a voltage being fed back to the error amplifier via the feedback loop. The operational amplifier will control the MOSFET so that this voltage matches the non-inverting input voltage.

The voltage divider (R_2, R_3) passes 10 % of the input voltage to the error amplifier. This divider is used to scale the input voltage so that it matches the same voltage interval as measured by R_{sense}. For example if the load current is 5 A, the 12 mΩ current sensing resistor will result in a voltage of 60 mV being fed back to the operational amplifier. The voltage divider makes this voltage correspond to 600 mV at the circuit input.

In this design, there are two feedback loops connected to the error amplifier. The first loop is feeding back the voltage signal created by the current sensing resistor which is proportional to the actual load current. The second feedback loop is connected between the error amplifier output and its inverting input. This is used for stabilizing the circuit at high frequency operation. The impedance networks present in both feedback loops are used to stabilize the circuit at high frequency operation. A good selection of the impedance network components results in a control loop with a sufficiently high phase margin and therefore a stable active load. The schematic is also included in Appendix A.2.

Chapter 4

Calculations and Prototype Construction

The study of the previous designs shows that the active load designed at Ericsson Power Solutions can be used as a base for the design in this thesis. This chapter describes the design process and the steps taken to meet the active load requirements.

4.1 Small Electronic Load Requirements

The main purpose of the design is to be physically small which makes it possible to solder it onto the DUT for DC/DC converter verification. This will reduce the effects of the cables on the current slew rate which makes the testing process more accurate. The testing current slew rate is specified to be at least 6 A/μs for this project, which is more than the available loads in the Ericsson laboratory can accomplish. The desired maximum testing current amplitude is 20 A for a converter with a output voltage between 0.2 V and 3.3 V. An important issue which must be considered is the cooling method used for the load. To correctly simulate the behaviour of a digital ASIC, the cooling is performed through the PCB because nearby components may get affected by temperature differences. The load current PCB path should have as small resistance and inductance as possible to not affect the active load performance. This adds some extra considerations regarding the circuit layout.

4.2 Small Electronic Load Prototype

The small electronic load prototype consists of two circuit boards connected with a pin header. Each of these modules are described in chapter 4.3 and 4.4. The I_{ref} signal is passed from the digital control module to the active load module together with ground and power, see Figure 4.1 that shows a block diagram describing the signal routing. Both modules has the PCB dimensions 30x30mm to mimic the size of the digital ASICs used in Ericsson. The PCB layout was designed with CadSoft EAGLE [15].

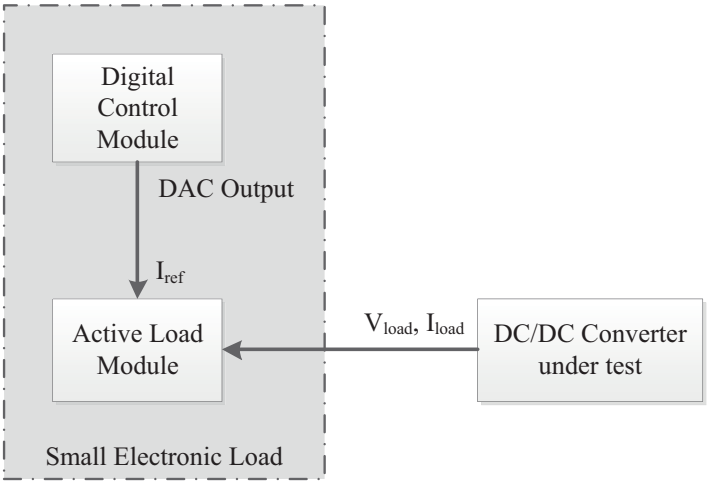


Figure 4.1: Small electronic load prototype block diagram

4.3 Active Load Module

The schematic and simulation tool TINA-Ti was used in the design process. It is a circuit design and simulation tool developed by Texas Instrument which is easy to use for analog and switched-mode power supply circuits [16].

The operational amplifier used in the previous design at the Power Solution Department (see section 3.5) was the MAX4434 from Maxim. Due to better simulation models a similar operational amplifier from Texas Instruments, OPA354 was chosen instead. They are both single supply and rail-to-rail amplifiers with high bandwidth which is needed for this application. The OPA354 has a high current output, over 100 mA and a unity-gain bandwidth of 250 MHz which makes it appropriate in e.g. video applications [17].

The transistors needs to control the current very fast and they should be able to be connected in parallel to share the current. The transistor technology best suited for these requirements is the MOSFET, see section 2.1.1. The two most important parameters of the MOSFET in this application is its gate capacitance (C_g) and its on-resistance ($R_{DS(on)}$). The on-state resistance needs to be low to make the load able to sink the specified current at low drain to source (V_{DS}) voltage. Another important factor is the gate capacitance which should be low to enable fast MOSFET turn on and off. As mentioned in section 2.3.3, a lower gate capacitance moves the pole created by the operational amplifiers output impedance and the capacitive load. This results in a higher cut-off frequency in the control loop, resulting in higher bandwidth. It seems reasonable to choose a MOSFET with both as low gate capacitance and on-state resistance as possible but there is a compromise situation. The two parameters are related, a small gate capacitance often implies a large on-state resistance and vice versa.

For this load module it is reasonable to use four MOSFETs in parallel since it is a good compromise between the MOSFET parameters and the active load requirements. The equivalent shunt resistance needed for the active load module to sink 20 A from a 0.2 V supply is calculated as

$$R_{req,tot} = \frac{V_{supply,min}}{I_{D,max}} = \frac{0.2V}{20A} = 10m\Omega \tag{4.1}$$

By using four parallel stages the shunt resistance of each stage should be able to go below the resistance calculated as

$$R_{req,stage} = 4R_{req,tot} = 40m\Omega \tag{4.2}$$

As mentioned earlier, the MOSFET used in the Linear Technology design has a very large gate capacitance and is therefore not suitable to be driven directly by an operational amplifier if high switching speed is desirable. However, its on-state resistance is very low and it should be able to meet the current amplitude requirements without parallel stages. Another benefit by using several MOSFETs in parallel divides the power dissipation between them and increases the power limit.

Other MOSFETs from companies such as Texas Instrument, Vishay, Infineon and Fairchild were studied and compared to choose the one most qualified for this task. The SiR412DP from Vishay was chosen due to its low gate capacitance 600 pF and its low on-state resistance 15 mΩ [18]. Using this MOSFET together with a current sense resistance of 10 mΩ gives a total stage minimum resistance of approximately 25 mΩ, leaving margin to the limit 40 mΩ. Figure 4.2 shows the complete circuit schematic of the active load module designed in TINA-Ti, a larger version is available in Appendix A.3.

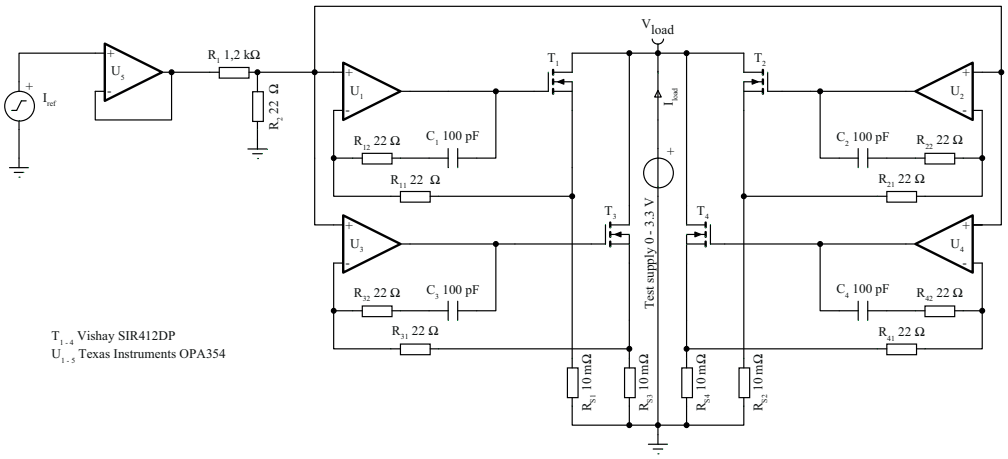


Figure 4.2: Active load module using four transistor stages in parallel

Figure 4.3 shows a close up on one stage together with the voltage divider (R_1, R_2) and impedance converter (U_2) which are common for all four stages. Each stage handles a current up to 5 A.

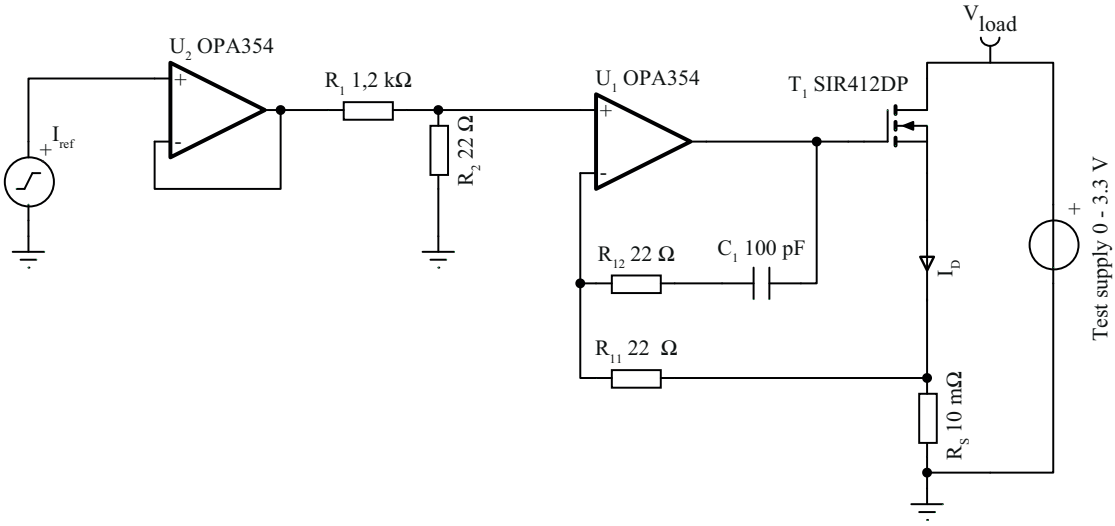


Figure 4.3: One transistor stage of the active load module

There are two stages of operational amplifiers in this active load module, similar to the Power Solution Department design. The first amplifier acts as an impedance converter (see section 2.2.2) which passes the input voltage to the output in order to supply a high current level for the next stage without any voltage drop. The second amplifier acts as an error amplifier (see section 2.2.3) and gate driver for the MOSFET.

Since the requirements for the output current is 20 A and there are four parallel load stages, each stage must be able to handle 5 A. To convert the load current to a voltage signal, a current sensing resistor is used. The current sense resistor R_{sense} is chosen to be 10 mΩ to keep the shunt resistance low. This results in a voltage of 50 mV over R_{sense} at the maximum current. The input reference voltage is in the interval 0 V - 3.3 V, therefore the maximum input value of 3.3 V should correspond to 5 A current through the MOSFET and R_{sense}. A voltage divider is used at the impedance converters output to scale the input voltage range to the current output range, passing approximately 1.8 % of the input voltage to the error amplifier.

Together with each error amplifier there are two feedback networks, see Figure 4.3. The first one is the network feeding back the voltage over the current sensing resistor. This voltage is proportional to the current flowing through the resistor and MOSFET. The error amplifier compares this voltage with the input reference voltage and then controls the MOSFET gate so that they become equal. The second feedback network connects the error amplifiers output with its inverting input. This is a stabilizing feedback network to prevent oscillations when there are fast transients, see section 4.3.1.

4.3.1 Active Load Module Stability Simulations in TINA-Ti

To simulate the stability of the active load circuit, a simulation model was implemented in TINA-Ti, see Figure 4.4. It uses an external model for the output resistance of the operational amplifier. In this way the operational amplifier open loop characteristic (Aol), the dual feedback network characteristic ($1/\beta$) and the loop gain characteristic can be obtained [7].

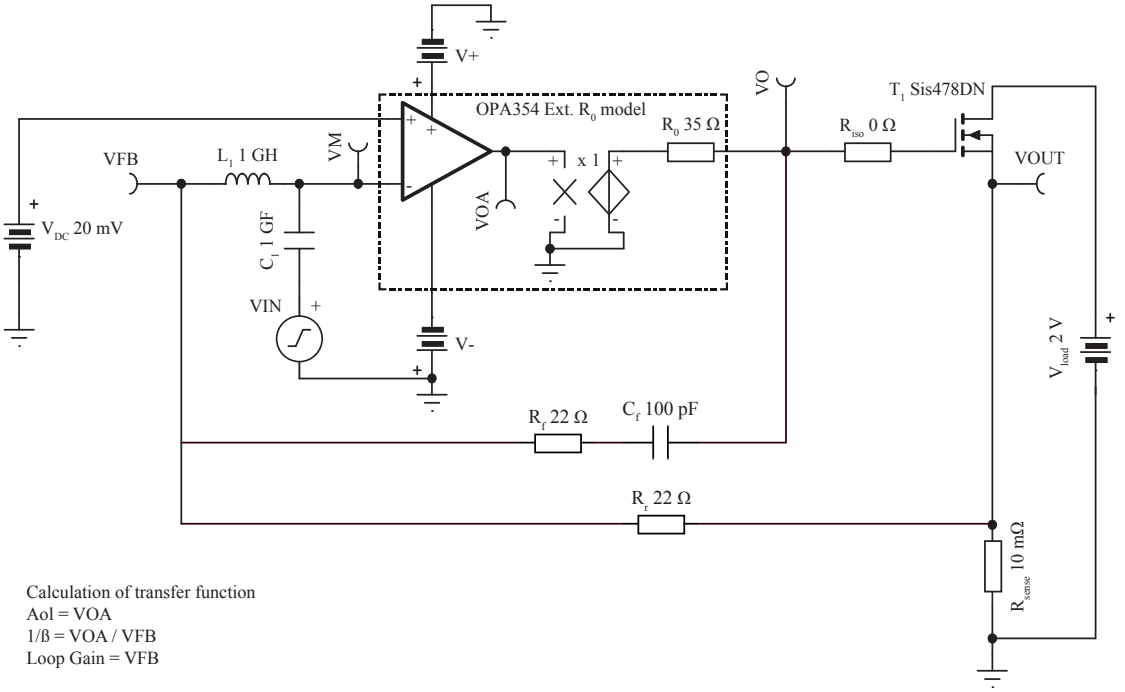


Figure 4.4: Circuit for simulating feedback stability in TINA-Ti

The best results was achieved with the first feedback loop using a 22 Ω resistor and the second loop using a 22 Ω resistor and a 100 pF capacitor in series. A Bode plot of the loop gain is shown in Figure 4.5. The dotted line shows the characteristics when not using feedback compensation (R_s = 0 and R_f, C_f removed). TINA-Ti has a built in function for extracting the phase margin. When not using feedback compensation the phase margin is 35.0° at 10.2 MHz and using it gives a phase margin of 67.5° at 12.8 MHz. The feedback compensation is needed to increase the phase margin over 45°.

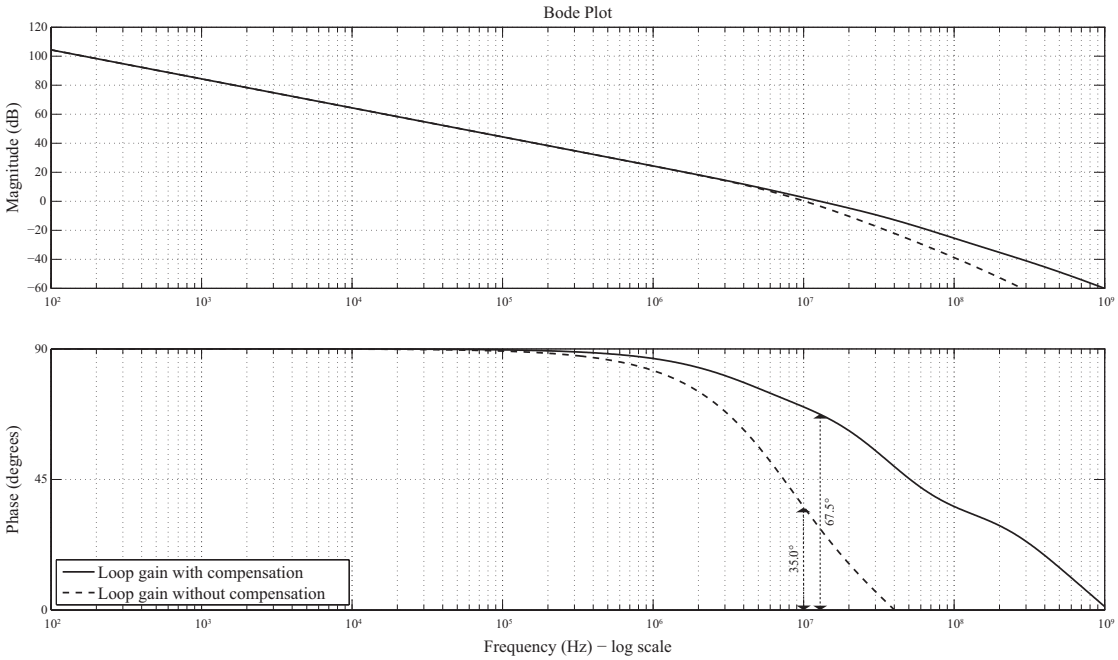


Figure 4.5: Loop gain Bode plot for the active load module simulated in TINA-Ti

4.3.2 Circuit Board Layout in Cadsoft Eagle

Almost all power dissipation on the circuit board is dissipated in the MOSFETs, therefore their position on the circuit board is important. To achieve proper cooling, they have to be mounted on a large copper area with sufficient distance between them. Also, a large circuit board copper area is needed for minimizing the resistance in the load current path. Figure 4.6 shows the layout of the active load module, the four MOSFETs are placed in the corners of the board and the operational amplifiers are placed in the middle. The power supply or converter being tested is soldered to the bottom layer of the PCB, the ground to the area in the center and the positive voltage supply to the area closest to the edges.

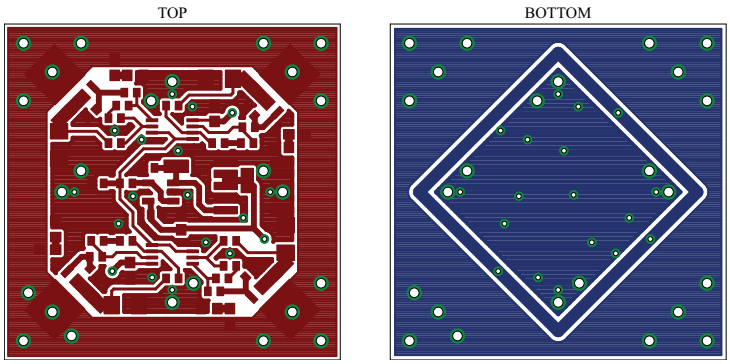


Figure 4.6: Active load module PCB layout

4.4 Digital Control Module

The active load module of the small electronic load is controlled by using a microprocessor. The microprocessor generates and controls the voltage pulse that is transformed to a current pulse in the active load circuit, see Figure 4.7. The pulse shape is created by the microprocessors built in resistor string DAC (Digital to Analog Converter), see section 2.5.2. The PWM pulse generation described in section 2.5.1 was not used as the needed low pass filter distorted the pulse shape. Software for the microprocessor is written in c code and compiled using the integrated development environment Keil.

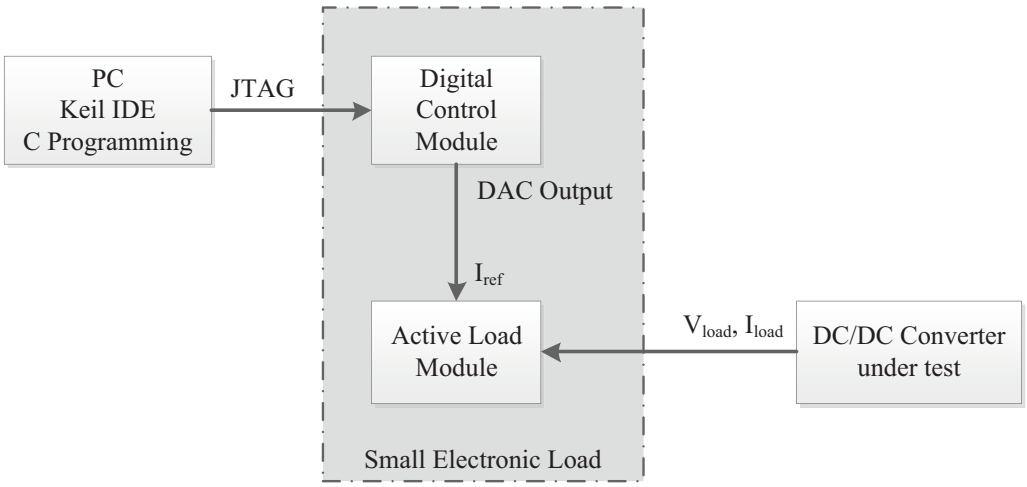


Figure 4.7: Small electronic load prototype block diagram

4.4.1 Choosing Microprocessor

Due to Ericsson preferences, a microprocessor from STMicroelectronics should be used. The microprocessor should have an inbuilt DAC peripheral to create the voltage pulse that is transformed to a current in the active load module. Also it is important that the microprocessor supports I^2C connection for future communication development of the load.

After analyzing the STMicroelectronics microprocessors, STM32F107RBT6 was found appropriate for this design. It is an ARM-based 32-bit processor with 72 MHz maximum clock frequency and built in DAC peripheral with two 12-bit channels. The processor has 128 kB of flash memory and up to 64 kB of SRAM, DMA controller and two I^2C interfaces [19].

4.4.2 Digital Control Module Software

The microprocessor software is programmed in c code using the integrated development environment Keil. The six parameters that can be set by the user are shown in Figure 4.8. In the first part of the software there is a check to control that the parameters doesn't violate the limits. Using these parameters the code then calculates and stores samples values representing the pulse. These samples are then written to the DAC continuously using the DMA functionality. As mentioned in section 2.5.3, the CPU is not involved in the data transfer when using DMA. After the DMA and DAC is configured, the CPU is free for other assignments. The complete source code can be found in Appendix B.

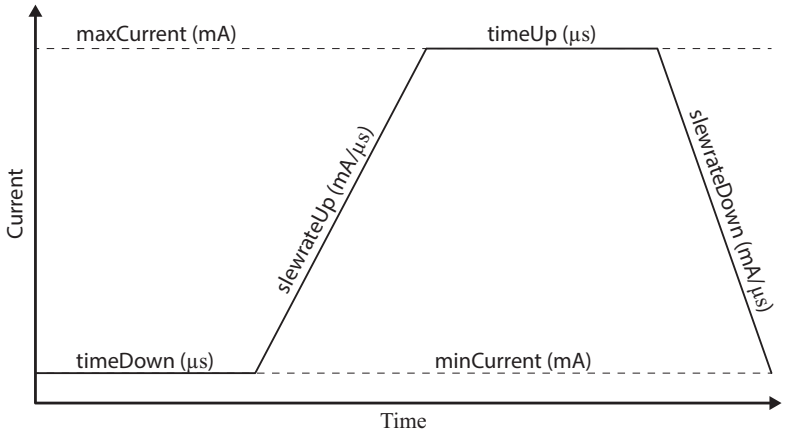


Figure 4.8: Pulse shape variables used in the digital control module

4.4.3 Circuit Board Layout in Cadsoft Eagle

Figure 4.9 shows the layout of the digital control PCB. The number of components on the PCB is rather low, it mainly consists of the microprocessor and the crystal oscillator used for clock frequency reference. The large amount of pads are used to access the I/Os of the microprocessor.

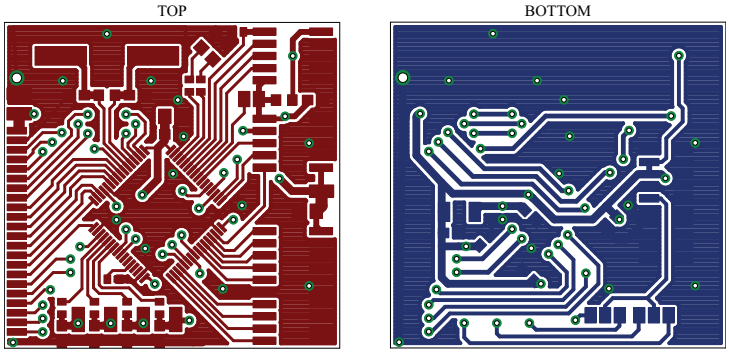


Figure 4.9: Digital control prototype PCB layout

Chapter 5

Analysis of Available Loads

5.1 Chroma 63103A

As mentioned in section 3.3, the Chroma 63103A electronic load has to be connected to the circuit board under test (DUT) with cables. The main problem with this kind of connection is the effect of the cable length to the current slew rate. Different lengths of the cables and also their placement will affect the inductance in the load current path. Results from tests with this setup may be inaccurate due to different cable types and lengths being used. Also the fastest slew rate is 2.5 A/μs which is less than the specification of the device being designed in this project.

Figure 5.1 shows an example of the connection between the Chroma loads and the DUT. The cables in the figure affect the output slew rate depending on their length. Also, the size of the rig is very large compared to the DUT.

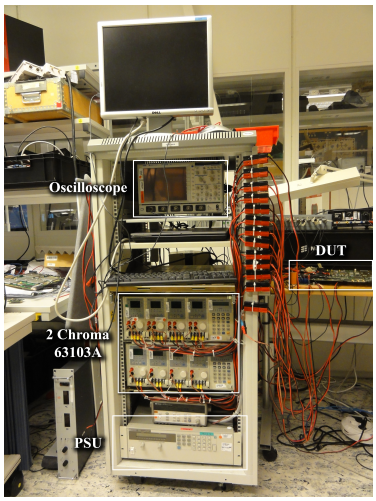


Figure 5.1: On-board DC/DC converter test rig with Chromas

5.1.1 Cable Length Influence

In order to show how the cable length between the electronic load and the power supply under test affects the slew rate, a test with different cable lengths was carried out using the Chroma 63103A. The test setup can be seen in Figure 5.2.

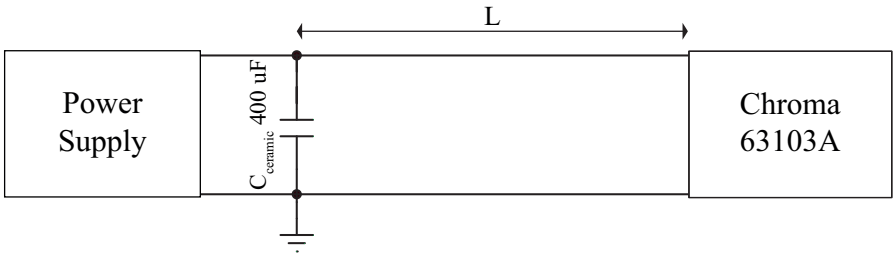


Figure 5.2: Cable length influence test setup

The test was carried out by using 8 different lengths of supply cable. The cable is the most commonly used for the electronic loads in the lab with a cross section area of approximately 3 mm^2. The capacitor bank connected in parallel with the supply is used to obtain a reference point so that the conductors before it doesn't affect the results. It consists of ceramic capacitors due to their good high frequency performance. Three different pulse shapes where used; all of them use the maximum slew rate of the Chroma (2.5 A/μs) and a pulse length of 50 μs. The rise times were measured using the built-in functions in the oscilloscope. The results are presented in Figure 5.3. Figure 5.4 shows the average slew rate based on the 20 % - 80 % rise times.

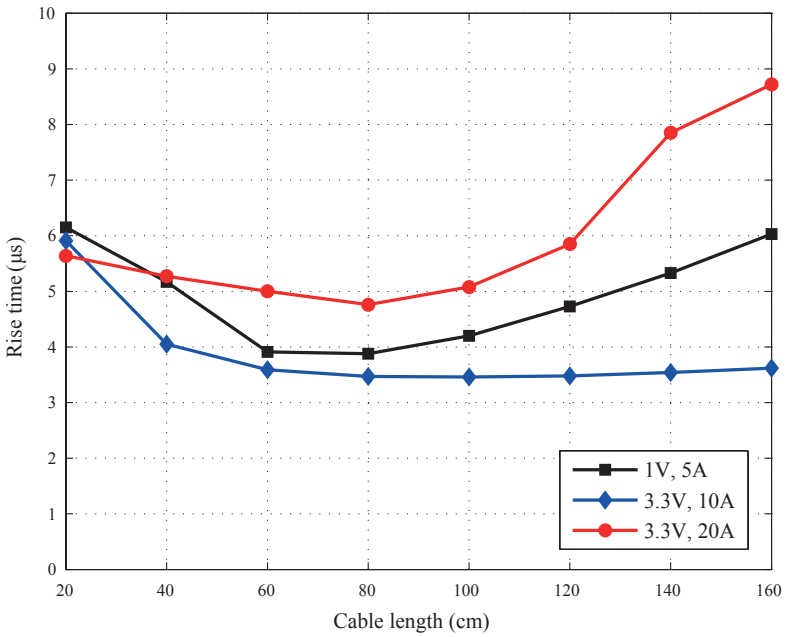


Figure 5.3: Chroma cable length test, rise time

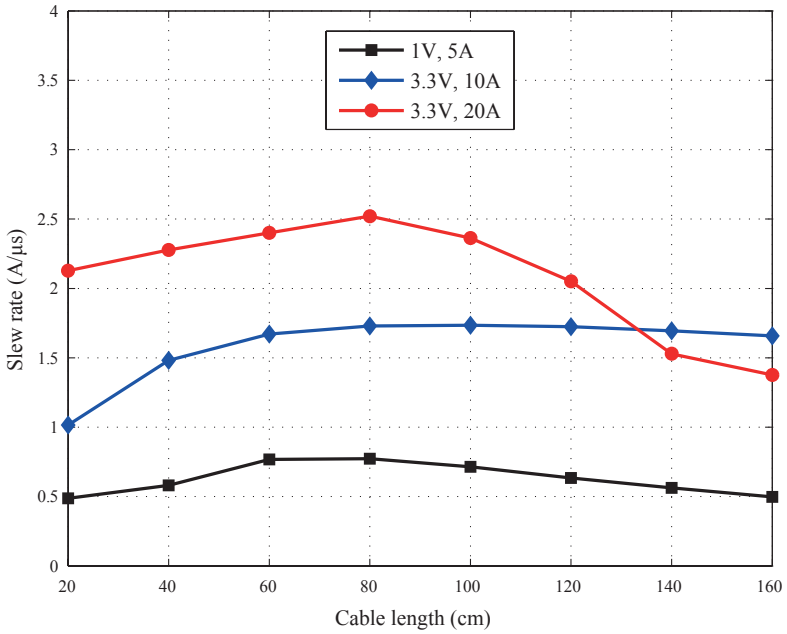


Figure 5.4: Chroma cable length test, average slew rate based on rise time

When studying the plots above, some unexpected results can be seen. The cable inductance decreases with decreasing cable length as in 2.14 and the current slew rate should therefore increase as in 2.21. In Figure 5.4 it is seen that when the cable length is decreased from 160 cm to 80 cm, the results shows the expected behaviour. With cable lengths below 80 cm it is not acting the same way; the current slew rate is decreasing with cable length from 80 cm to 20 cm.

The reason of this behaviour is that the test was carried out outside the specifications of the Chroma and that some resonances maybe occur between the impedance of the cable and the Chroma.

5.2 Linear Technology Design

The transistor used in this load is the Infineon IPB015N04LG, which is a power transistor optimized for DC/DC converters [20]. In this transistor, $R_{DS(on)}$ is approximately 1.5 mΩ and C_g = 21000 pF. Although it has low drain-to-source on-resistance, the gate capacitance is very large which increases the demand on the driving stage since it has to supply more energy to the gate during turn on and turn off.

The operational amplifiers used in the design are dual supply +/- 15 V which complicates the power supply. The need of a separate gate driving stage makes this design require a lot of components, see Appendix A.1 and therefore also large space requirements. A design like this one would suffer from the same problems as the Chroma, connection cables introducing inductance in the load current path and limiting the current slew rate.

5.3 Power Solution Department, Ericsson AB Design

As shown in Figure 3.7, the transistor used in this design is the Vishay SiS334DN which has a $R_{DS(on)}$ of approximately 12 mΩ and a C_g of 640 pF [21].

When saturating the transistor in this design, the minimum shunt resistance will be approximately 24 mΩ. The maximum current that the load can sink when the test supply voltage is 0.2 V is

$$I_{D,max} = \frac{V_{load}}{R_{DS(on)} + R_{sense}} \approx \frac{0.2V}{12m\Omega + 12m\Omega} \approx 8.3A \tag{5.1}$$

This does not fulfill the load requirements which is 20 A at 0.2 V. However, a parallel set up of this design would meet the electrical requirements for the small electronic load. Also, this design uses many components in the feedback loops (three resistors and three capacitors) which would make this design large when using it in a parallel set up.

Chapter 6

Prototype Analysis

6.1 Measurement Setup

The measurement setup used for all measurements is described in this chapter. The small electronic load is fully assembled and an oscilloscope is used to measure the load current by using a current probe. From the capacitor bank acting as the DUTs output capacitance, there is approximately 5 cm cable to the bottom of the active load module, see Figure 6.1. This is used to be able to connect the current probe and it will affect the results since it introduces extra inductance in the current path. The inductance of the load current path on the PCB is very hard to calculate but the inductance of the added cable can be approximated with 2.14 as

$$L \approx 2 * 10^{-7} l(\ln \frac{2l}{r} - 1) \approx 2 * 10^{-7} * 0.1(\ln \frac{2 * 0.1}{0.0015} - 1) \approx 80nH \tag{6.1}$$

The total current path inductance is the sum of the cable inductance and the inductance in the PCB. For the calculations the total current path inductance is approximated to 100 nH.

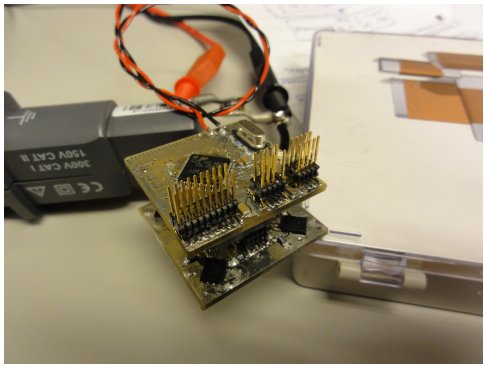


Figure 6.1: Measurement setup for prototype analysis chapter

6.2 Simulation Results versus Measurement Results

In Figure 6.2, a comparison between simulations performed in TINA-Ti and measurements on the prototype is plotted. As seen, the simulations do not match the measurements very well. The measured current has much lower slew rate than the simulated current at the start of the pulse. Also some oscillations occur at maximum amplitude which is not revealed in the simulations. The reason is probably inductance in the load current path which is not accounted for in the simulations. Even though it is very small, around 100 nH it has a great impact on fast current pulses.

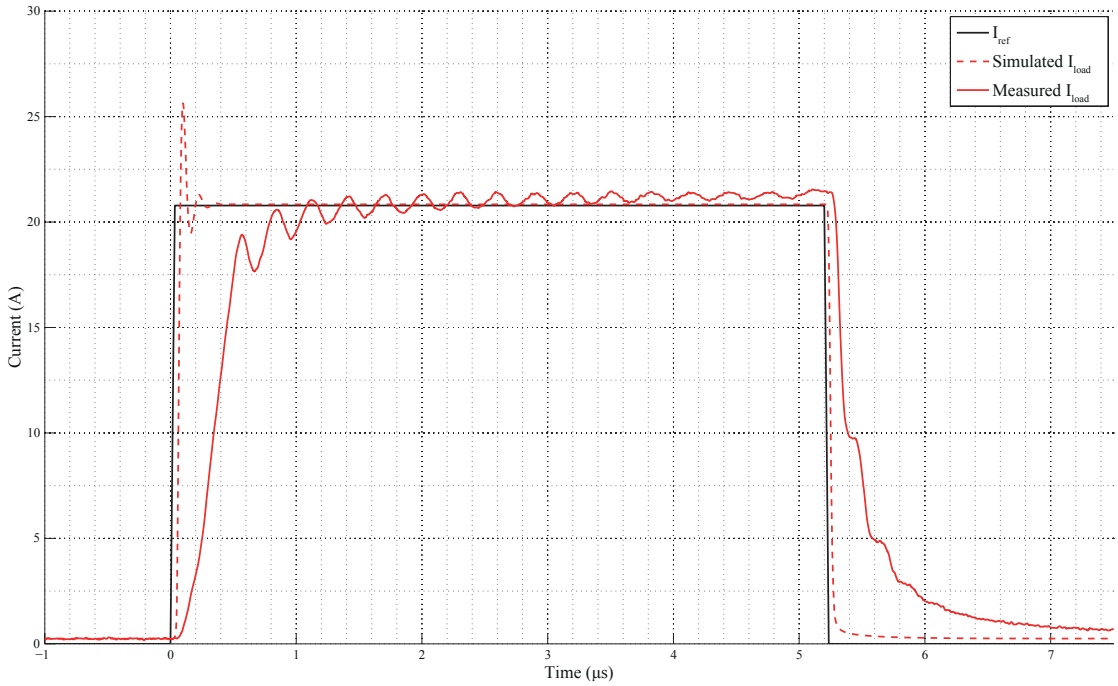


Figure 6.2: Comparison between simulation in TINA-Ti and measurements on prototype

6.3 Feedback Compensation Analysis

Measurements of the load current was performed when the active load was fed with a step with maximum amplitude. The solid line represents the load current when using the second feedback loop and the dotted line represents the load current when not using it. As seen in Figure 6.3, the second feedback loop effectively dampens the oscillations that occurs when the active load is used with high slew rate signals. The results are consistent with the bode diagram from simulation in TINA-Ti (see Figure 4.5). The fact that the oscillations are dampened indicates a greater phase margin when using the second feedback loop.

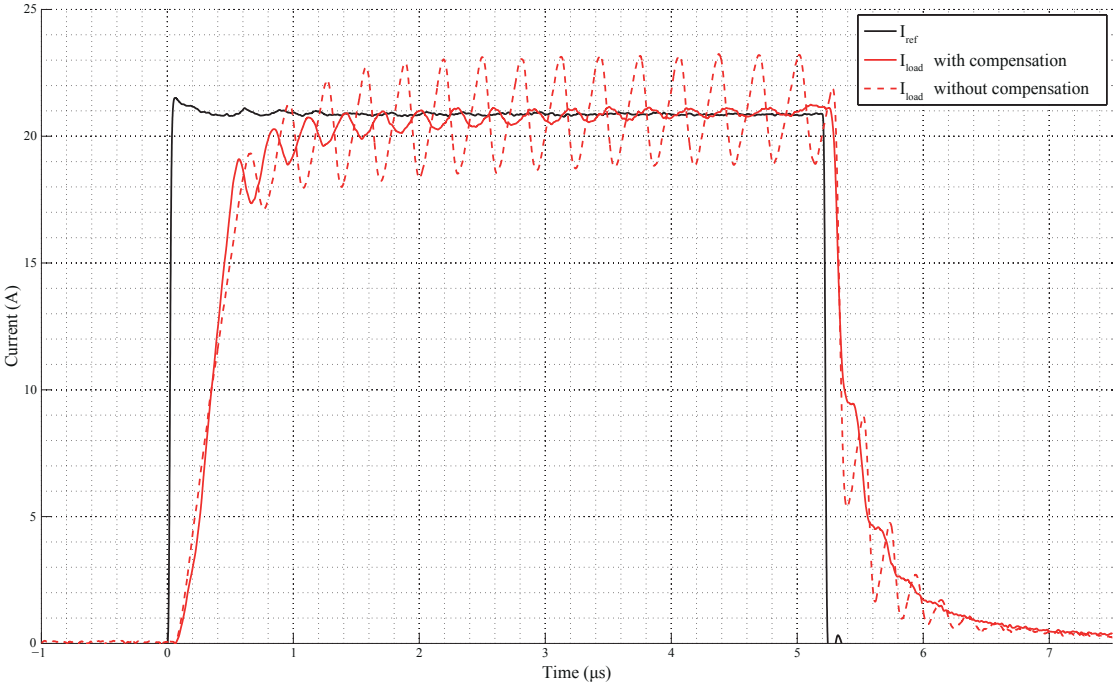


Figure 6.3: Feedback compensation influence on step response

6.4 Current Slew Rate Dependency on Tested Supply Voltage

The maximum current slew rate the active load can achieve is dependent on the voltage level of the tested converter, see Section 2.4. In Figure 6.4, the step response has been measured with different voltage levels at the converter output. The corresponding slew rates are found in Table 6.1.

The rather poor slew rates at lower voltage can be explained by the short cable used in the setup. In Section 6.1 the current path inductance was approximated to be 100 nH. Using 2.21 from Section 2.4 with this inductance value, the average slew rate during the first time constant (time between 0 and 63 % of the final value) can be calculated. Results can be found in Table 6.1.

The measured slew rates are linearly consistent with the calculated ones using L = 100 nH. The error could be the approximated inductance. The process is reversed and the inductance is calculated by using the measured results, see 6.2. Using this value of the inductance, the calculations matches the measurements very well, see Table 6.1.

$$\frac{dI}{dt} = \frac{0.63V_{supply}}{L} \Rightarrow L = \frac{0.63V_{supply}}{\frac{dI}{dt}} = \frac{0.63 * 0.2V}{2 * 10^6 A/s} = 63nH \tag{6.2}$$

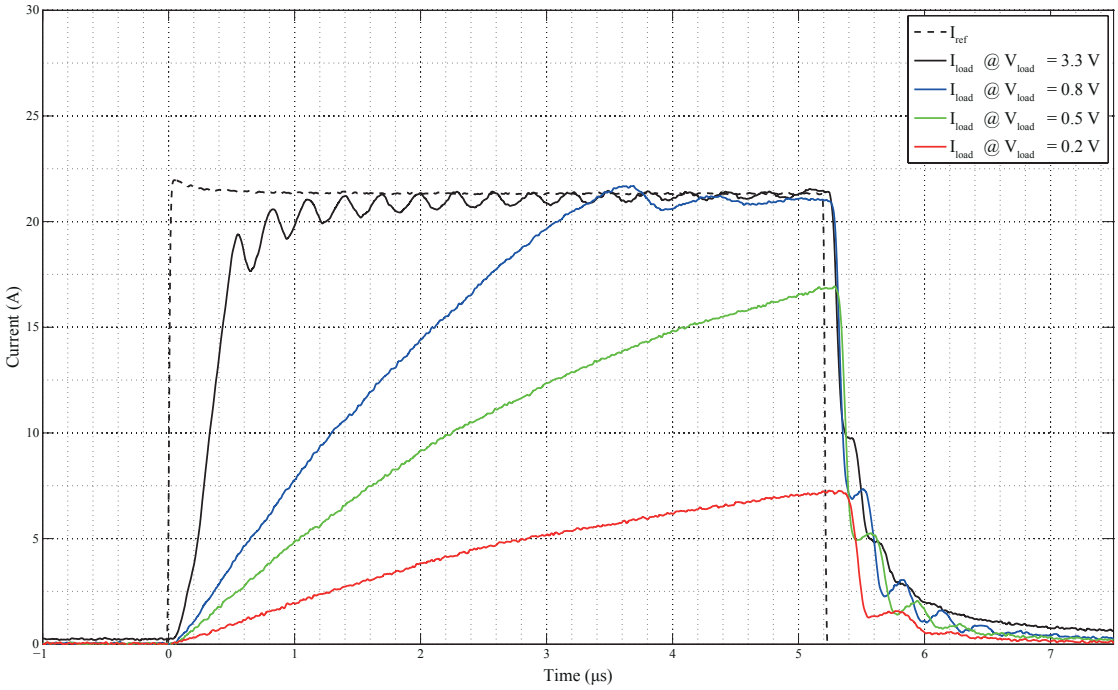


Figure 6.4: Current slew rate depending on V_{load} voltage

V_{load}	I_{load} slew rate, from Figure 6.4	I_{load} slew rate using 2.21 and L = 100 nH	I_{load} slew rate using 2.21 and L = 63 nH
3.3 V	32 A/μs	21 A/μs	33 A/μs
0.8 V	8 A/μs	5 A/μs	8 A/μs
0.5 V	5 A/μs	3 A/μs	5 A/μs
0.2 V	2 A/μs	1 A/μs	2 A/μs

Table 6.1: Measured and calculated values comparison

6.5 DMA Influence on DAC Created Pulse

By using Direct Memory Access (DMA) which is described in Section 2.5.3, faster usage of the DAC peripheral is enabled. The time span between the output samples was decreased from 1000 ns to 200 ns, around 5 times faster. Figure 6.5 shows the load current for a pulse going from 2 A to 20 A with a slew rate of 6 A/μs. When not using DMA there is only time to output 3 samples during the rise and fall which results in a crude looking waveform. This is corrected by using low pass filtering but it will distort the pulse shape in other ways. Fewer sample steps will also lower the slew rate precision. When using DMA, there is time to output 15 samples during same rise and fall times, which makes the waveform smooth and precise.

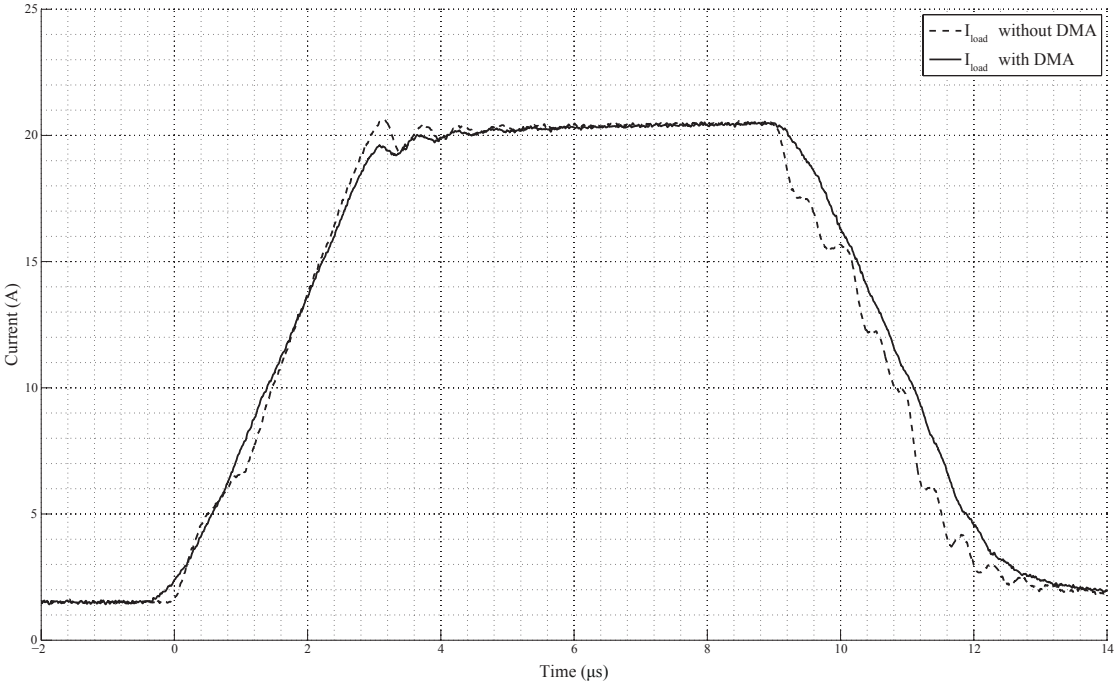


Figure 6.5: DMA influence on load current pulse shape

6.6 Temperature Measurements

The power dissipation in the MOSFETs results in heat development. Semiconductors break or life time degrades if the temperature is outside its specified limits. To find out the loading capacity of the constructed prototype temperature measurements were carried out during operation. The circuit was tested with a 50 % duty cycle pulse train with amplitude of 5 A. The load voltage was varied to change the power dissipation in the circuit. An IR picture of the warmest MOSFET can be seen in Figure 6.6.

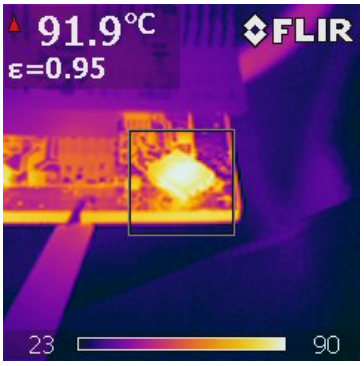


Figure 6.6: Temperature measurement of operating active load taken with FLIR i50 IR camera

Table 6.2 shows the stable working temperature of the MOSFET with highest temperature when varying the power dissipated in the circuit. The surrounding temperature can be assumed to be 25°C and cooling was only achieved through the PCB.

P_{RMS}	MOSFET steady state temperature
3.0 W	70°C
4.5 W	90°C

Table 6.2: MOSFETs stable temperature with different P_{RMS}

Chapter 7

Summary and Conclusion

7.1 Summary

In this master thesis, a Small Electronic Load for testing on-board DC/DC converters has been designed. Existing active load designs have been analysed and a prototype improving the current slew rates was built. The prototype was based on a previous prototype designed by the Power Solutions department at Ericsson AB, Lindholmen. This design was improved to meet the requirements specified in this thesis.

7.2 Future Work

The circuit boards used in Ericssons products often contain more than one DC/DC converter. A future improvement would be to develop the communication between the electronic loads and therefore make them able to run synchronized tests. Verification of the converters in this way would probably give very realistic results because it is almost as close as you can come to the real set up with different ASICs with varying current dynamics. Also DC/DC converters on the same circuit board can affect each other when sharing power supply paths etc.

The first idea to use a GPIB (IEEE-488) interface to configure the active load units will be a bulky solution since the connector itself has larger dimensions than the active load and uses 24 conductors. The advantage with GPIB will be the compatibility to the equipment available in the lab and testing routines used by Ericsson AB. At the Power Department, PMBUS (Power Management Bus) is used to control and communicate with the power modules. It can be described as a standard way to communicate with power converters over a digital bus [22]. It's based on I^2C and uses the same physical layer with one data and one clock signal. In addition it supports two optional extra signals, alert and on/off control. A future improvement in this area would be to develop PC based software that could communicate and configure the active loads using PMBUS, see Figure 7.1. Since PMBUS is a bus communication standard with several connected nodes, there must be a way to assign a unique address to each small electronic load.

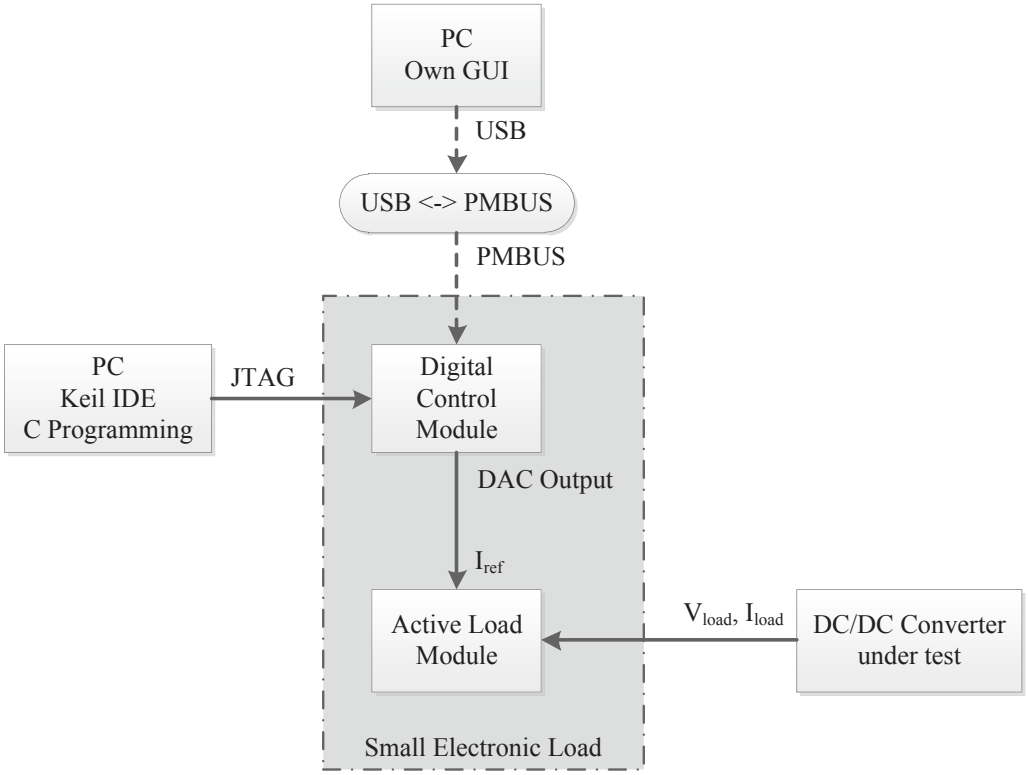


Figure 7.1: Using PMBUS to configure the Small Electronic Load

7.3 Economical Point of View

The price of a Chroma 63103A main frame with 4 dual channel modules is approximately 70 000 SEK. The equivalent price per load channel becomes 9 000 SEK. The manufacturing cost for the small electronic load described in this project is less than 100 SEK.

References

[1] M. G. Simoes, "Power bipolar transistors," in *Power Electronics Handbook (Second Edition)* (M. H. Rashid, ed.), pp. 27–39, Elsevier Inc, 2007.

[2] I. Batarseh, "The power MOSFET," in *Power Electronics Handbook (Second Edition)* (M. H. Rashid, ed.), pp. 41–69, Elsevier Inc, 2007.

[3] R. C. Jaeger, *Microelectronic Circuit Design*. New York: McGraw-Hill Companies Inc, 1997.

[4] B. Carter and T. R. Brown, "Handbook of operational amplifier applications." Texas Instruments, October 2001.

[5] "Analysis and design of feedback control systems - understanding poles and zeros," Massachusetts Institute of Technology Department of Mechanical Engineering.

[6] R. Mancini, "Op-amp stability and input capacitance." Texas Instruments, 2004.

[7] T. Green, "Operational amplifier stability." Texas Instruments.

[8] R. Mancini, "Op-amps for everyone." Texas Instruments, 2002.

[9] P. R. Clayton, "The concept of 'partial' inductance," in *Inductance: Loop and Partial*, pp. 195–245, John Wiley & Sons, Inc, 2010.

[10] U. A. Bakshi and A. V. Bakshi, *Electrical Network Analysis and Synthesis*. Pune: Technical Publications Pune, 2008.

[11] "Audio and waveform generation using the DAC in STM32 microcontroller families." STMicroelectronics, May 2010.

[12] "Programmable DC electronic load, model 6310A series." Chroma ATE INC, 2000.

[13] J. Williams, "A closed-loop wideband 100 A active load." Linear Technology, October 2011.

[14] M. Svensson, *1911-INX110175/1 PA12*. Ericsson AB.

[15] CadSoft Computer, *EAGLE - Easily Applicable Graphical Layout Editor, Tutorial Version 6*, 2011.

[16] Texas Instruments, *Getting Started with TINA-TI*, August 2008.

[17] Texas Instruments, *OPA354/OPA2354/OPA4354 Datasheet*, March 2002.

[18] Vishay Siliconix, *N-Channel 25-V (D-S) MOSFET-SiR412DP Datasheet*, October 2009.

[19] STMicroelectronics, *STM32F105xx/STM32F107xx Datasheet*, August 2011.

[20] Infineon, *OptiMOS 3 Power Transistor - IPB015N04LG Datasheet*, November 2009.

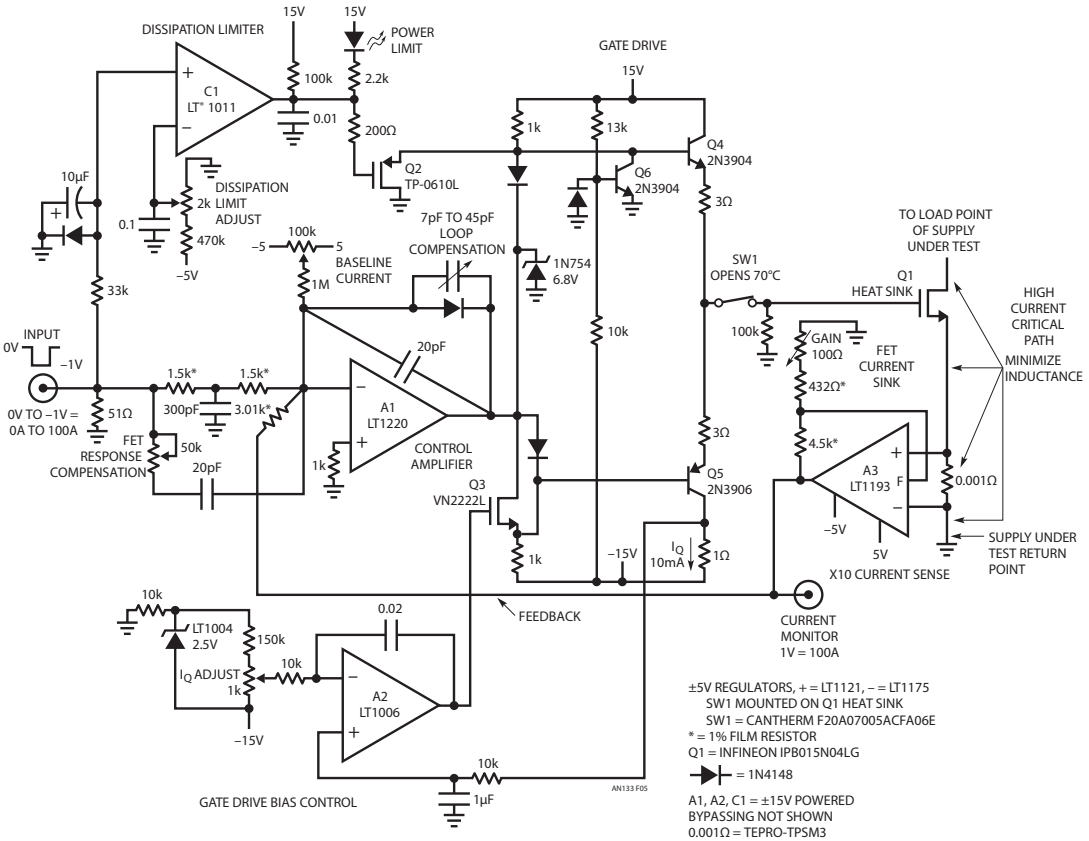
[21] Vishay Siliconix, *N-Channel 30 V (D-S) MOSFET-SiS334DN Datasheet*, September 2011.

[22] R. V. White, “Introduction to PMBUS,” PMBus.org, 2005.

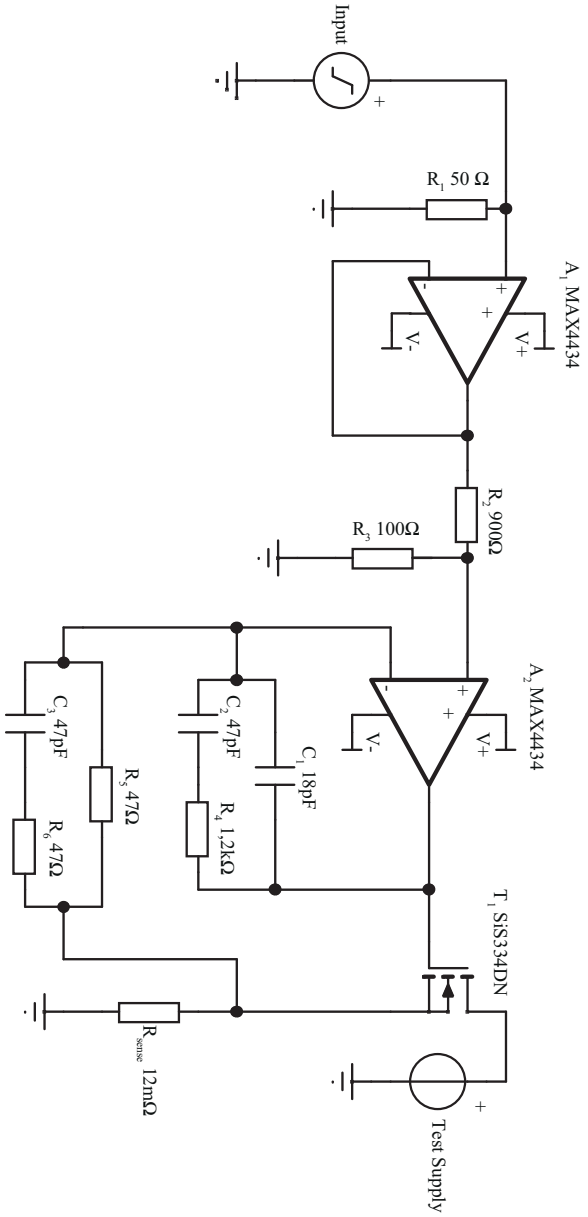
Appendix A

Schematics

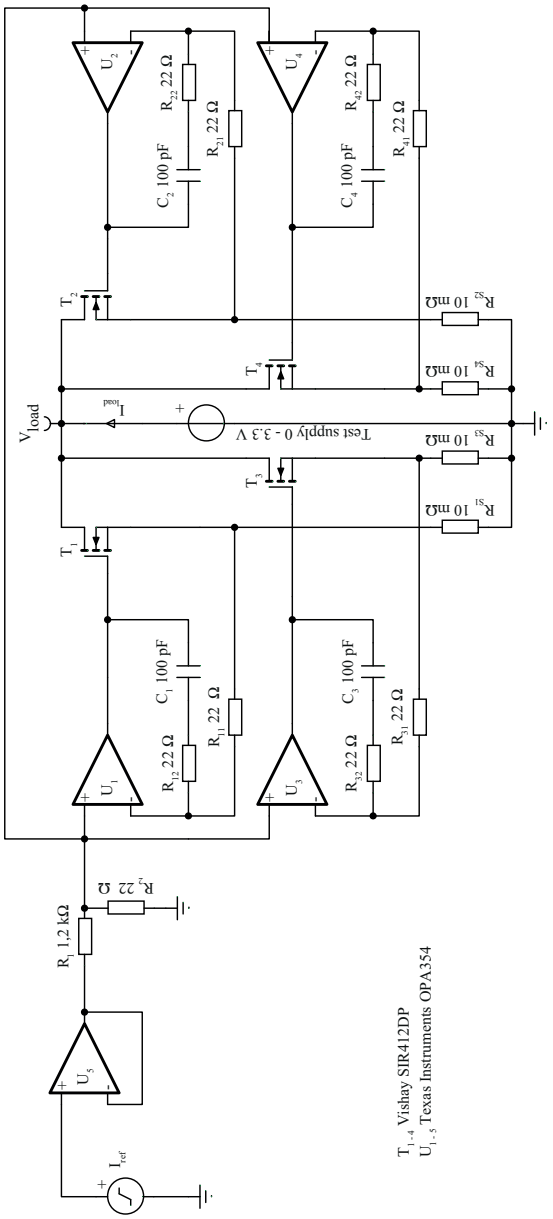
A.1 Linear Technology Design



A.2 Power Solutions Department, Ericsson AB Design



A.3 Thesis Prototype Load Module



Appendix B

Digital Control Module Source Code

```
1  /******************************************************************************
2    * @file Small Electronic Load/main.c
3    * @author Lukas Rosén, Sahar Samimi
4    * @date 19-nov-2012
5    * @brief Main program body
6    * Code uses STM32F10x Standard Peripherals Library
7  ******************************************************************************/
8
9  /* Includes */
10 #include "main.h"
11 #include "stm32f10x.h"
12 #include "stm32f10x_it.h"
13
14 /* Private typedef */
15 TIM_TimeBaseInitTypeDef TIM_TimeBaseStructure;
16 GPIO_InitTypeDef GPIO_InitStructure;
17 DAC_InitTypeDef  DAC_InitStructure;
18 DMA_InitTypeDef DMA_InitStructure;
19
20 /* Private define */
21 #define LED_on GPIO_SetBits(GPIOB, GPIO_Pin_8); // LED at PB9 on
22 #define LED_off GPIO_ResetBits(GPIOB, GPIO_Pin_8); // LED at PB9 off
23 #define DAC_DHR8R1_Address 0x40007410 // Address to DAC output register
24
25 /* Private variables */
26 static uint32_t timingdelay;
27 unsigned int i, stepsUp, stepsDown;
28 uint8_t pulseupsamples[225], pulsedownsamples[225];// DAC sample arrays holds 50us
29 const double conversion = (double) 240 / 20000; // Calibration value for current level
30 const double sampleperiod = (double) 0.2232; // Time between samples in us using DMA
31 double stepsizeUp, stepsizeDown;
32
```

```
33 // The DMA reconfigure process takes 2.5us, this means that the minimum timeup and down is 2.5us
34 // Following variables contain the pulse configuration parameters, currents in mA, times in us
35 double slewrateUp = 10000;
36 double slewrateDown = 2500;
37 double maxCurrent = 15000;
38 double minCurrent = 1000;
39 double timeDown = 200;
40 double timeUp = 10;
41
42 /* Delay functions */
43 void timingdelay_decrement(void){
44         if (timingdelay != 0x00)
45                 timingdelay--;
46 }
47
48 void delayms(uint32_t ms){
49         timingdelay = ms;
50         while(timingdelay != 0);
51 }
52
53 void delay1us(void){
54   volatile int us = 5;
55         while (us != 0){
56                 us--;
57         }
58 }
59
60 void delayus(uint32_t us){
61         while (us != 0) {
62                 delay1us();
63                 us--;
64         }
65 }
66
67 /* Initialization function for setting up GPIO, DAC and communication peripherals */
68 void init (void){
69
70 // Peripheral clock enable
71 RCC_APB1PeriphClockCmd(RCC_APB1Periph_TIM6 | RCC_APB1Periph_DAC | RCC_APB1Periph_I2C1, ENABLE);
72 RCC_APB2PeriphClockCmd(RCC_APB2Periph_GPIOA | RCC_APB2Periph_GPIOB, ENABLE);
73 RCC_AHBPeriphClockCmd(RCC_AHBPeriph_DMA2, ENABLE);
74
75 // Configure port A pins
76 // Once the DAC channel is enabled, the corresponding GPIO pin is automatically
77 // connected to the DAC converter. In order to avoid parasitic consumption,
78 // the GPIO pin should be configured in analog
79 GPIO_InitStructure.GPIO_Pin = (GPIO_Pin_4 | GPIO_Pin_5);
80 GPIO_InitStructure.GPIO_Mode = GPIO_Mode_AIN;
81 GPIO_Init(GPIOA, &GPIO_InitStructure);
```

```
82
83  // Configure port B pins
84  // PB5,PB6,PB7 used for I2C
85  // PB8,PB9 used for indicator LEDs
86  GPIO_InitStructure.GPIO_Pin = (GPIO_Pin_5 | GPIO_Pin_6 |GPIO_Pin_7);
87  GPIO_InitStructure.GPIO_Speed = GPIO_Speed_50MHz;
88  GPIO_InitStructure.GPIO_Mode = GPIO_Mode_AF_PP;
89  GPIO_Init(GPIOB, &GPIO_InitStructure);
90
91  GPIO_InitStructure.GPIO_Pin = (GPIO_Pin_8 | GPIO_Pin_9);
92  GPIO_InitStructure.GPIO_Speed = GPIO_Speed_50MHz;
93  GPIO_InitStructure.GPIO_Mode = GPIO_Mode_Out_PP;
94  GPIO_Init(GPIOB, &GPIO_InitStructure);
95
96  // Configure TIM6 used to trigger the DMA
97  TIM_PrescalerConfig(TIM6, 0, TIM_PSCReloadMode_Update);
98  TIM_SetAutoreload(TIM6, 1);
99  TIM_SelectOutputTrigger(TIM6, TIM_TRGOSource_Update);
100
101 // DAC channel 1 configuration
102 DAC_InitStructure.DAC_Trigger = DAC_Trigger_T6_TRGO;
103 DAC_InitStructure.DAC_WaveGeneration = DAC_WaveGeneration_None;
104 DAC_InitStructure.DAC_OutputBuffer = DAC_OutputBuffer_Disable;
105 DAC_Init(DAC_Channel_1, &DAC_InitStructure);
106
107 // DMA Configuration
108 DMA_DeInit(DMA2_Channel3);
109 DMA_InitStructure.DMA_PeripheralBaseAddr = DAC_DHR8R1_Address;
110 DMA_InitStructure.DMA_DIR = DMA_DIR_PeripheralDST;
111 DMA_InitStructure.DMA_PeripheralInc = DMA_PeripheralInc_Disable;
112 DMA_InitStructure.DMA_MemoryInc = DMA_MemoryInc_Enable;
113 DMA_InitStructure.DMA_PeripheralDataSize = DMA_PeripheralDataSize_Byte;
114 DMA_InitStructure.DMA_MemoryDataSize = DMA_MemoryDataSize_Byte;
115 DMA_InitStructure.DMA_Priority = DMA_Priority_VeryHigh;
116 DMA_InitStructure.DMA_M2M = DMA_M2M_Disable;
117 DMA_InitStructure.DMA_Mode = DMA_Mode_Normal; // Can also be used in Circular mode
118 // DMA_InitStructure.DMA_MemoryBaseAddr = (uint32_t)&pulsesamples8bitup;
119 // DMA_InitStructure.DMA_BufferSize = 16;
120
121 // Write configuration and enable DMA2 Channel3
122 DMA_Init(DMA2_Channel3, &DMA_InitStructure);
123 DMA_Cmd(DMA2_Channel3, ENABLE);
124
125 // Enable DAC channel 1: Once the DAC channel 1 is enabled, PA4 is
126 // automatically connected to the DAC converter.
127 DAC_Cmd(DAC_Channel_1, ENABLE);
128
129 // Enable DMA for DAC channel 1
130 DAC_DMACmd(DAC_Channel_1, ENABLE);
```

```
131
132 // Enable interrupt generation at DMA transfer complete
133 // DMA_ITConfig(DMA2_Channel3, DMA_IT_TC3, ENABLE);
134
135 // Enable TIM6 to trigger the DMA
136 TIM_Cmd(TIM6, ENABLE);
137
138 SysTick_Config(72000);
139 }
140
141 /* Main function */
142 int main (void){
143
144 init();  // Setup GPIO, DAC and communication peripherals
145
146 // Check so that the vaiable values are within resonable limits
147 if ((minCurrent < 0) || (minCurrent > maxCurrent) || (maxCurrent > 20000)){
148         LED_on
149         while(1); // Unvalid current amplitude values, yellow led illuminates
150         }
151
152 if ((slewrateDown < 400) || (slewrateUp < 400) || (slewrateDown > 10000) || (slewrateUp > 10000)) {
153         LED_on
154         while(1); // Unvalid slewrate values, yellow led illuminates
155         }
156
157 if ((timeDown <= 6) || (timeUp <= 6) || (timeUp / (timeUp + timeDown) > 0.5)) {
158         LED_on
159         while(1); // Unvalid time values, yellow led illuminates
160         }
161
162 // Calculate variables that is used for creating the pulse
163 stepsUp = (int)(((maxCurrent - minCurrent) / slewrateUp) / sampleperiod);
164 stepsDown = (int)(((maxCurrent - minCurrent) / slewrateDown) / sampleperiod);
165
166 stepsizeUp = (maxCurrent - minCurrent) / (stepsUp + 1);
167 stepsizeDown = (maxCurrent - minCurrent) / (stepsDown + 1);
168
169 // The two for-loops calculates and fills the sample arrays with the desired pulse shape
170 for (i=0;i<stepsUp;i++){
171         pulseupsamples[i] = (uint8_t)(conversion*(minCurrent + i*stepsizeUp));
172         }
173 pulseupsamples[i] = (uint8_t)(conversion*maxCurrent);
174
175 for (i=0;i<stepsDown;i++){
176         pulsedownsamples[i] = (uint8_t)(conversion*(maxCurrent - i*stepsizeDown));
177         }
178 pulsedownsamples[i] = (uint8_t)(conversion*minCurrent);
179
```

```
180 // Endless loop, resets the DMA after each rise or fall by checking the DMA transfer complete flag
181 while(1){
182
183         DMA_Cmd(DMA2_Channel3, DISABLE);
184         DMA_InitStructure.DMA_MemoryBaseAddr = (uint32_t)&pulseupsamples;
185         DMA_InitStructure.DMA_BufferSize = stepsUp + 1;
186         DMA_Init(DMA2_Channel3, &DMA_InitStructure);
187         DMA_Cmd(DMA2_Channel3, ENABLE);
188
189         while (!DMA_GetFlagStatus(DMA2_FLAG_TC3)) {}
190         DMA_ClearFlag(DMA2_FLAG_TC3);
191
192         delayus((int)timeUp - 6);
193
194         DMA_Cmd(DMA2_Channel3, DISABLE);
195         DMA_InitStructure.DMA_MemoryBaseAddr = (uint32_t)&pulsedownsamples;
196         DMA_InitStructure.DMA_BufferSize = stepsDown + 1;
197         DMA_Init(DMA2_Channel3, &DMA_InitStructure);
198         DMA_Cmd(DMA2_Channel3, ENABLE);
199
200         while (!DMA_GetFlagStatus(DMA2_FLAG_TC3)) {}
201         DMA_ClearFlag(DMA2_FLAG_TC3);
202
203         delayus((int)timeDown - 6);
204         }
205 }
206
207 /*****************************************************************************/
```