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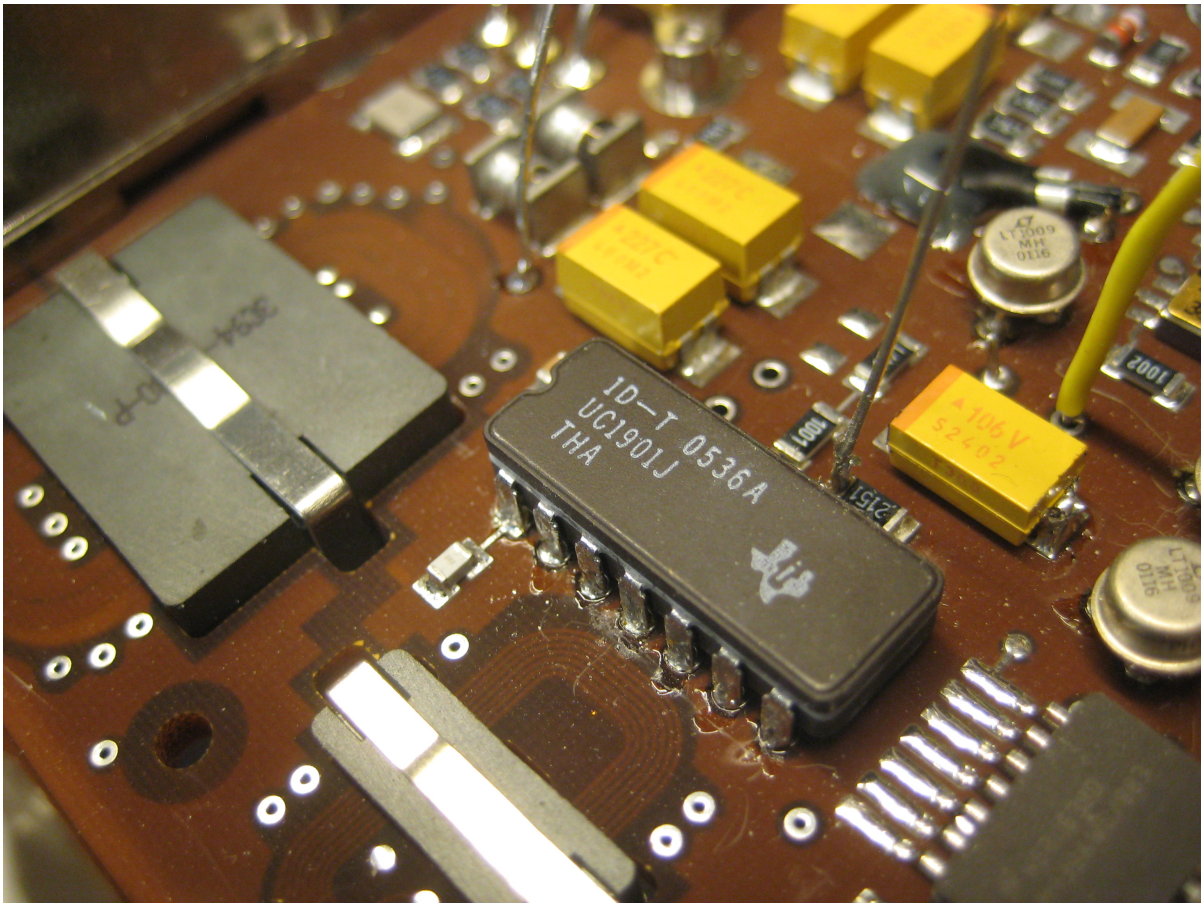

Galvanically isolated transmission of analog control signals and study of commercial state of the art technology for satellites and launchers

Master's thesis in Electrical Engineering

LARS JOHANSSON

Department of Energy and Environment
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Cover:
Illustrate an IC-circuit, *UC1901*, used in a DC/DC converter as feedback.

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Abstract

Space, the unknown place where satellites operate on our behalf. In space, the only known renewable energy comes from the sun, where the energy is captured by solar cells that supply all electronics on-board the satellite via rechargeable batteries. With an environment surrounded by vacuum and radiation, electronics need to be protected and constructed to manage the harsh conditions.

Today, a DC/DC converter unit is available at RUAG Space to supply electronics with different voltages and power requirements. It consists of a galvanically isolated flyback topology with a feedback path and is currently operational in space, but there exists potential for improvements of the feedback path and therefore this thesis has been created. The current feedback (the IC-unit *UC1901*) use amplitude modulation to transfer a voltage error back to a PWM-circuit that adjust the pulse width and thereby regulate the secondary output voltages.

A state of the art technology study was performed to investigate other potential feedback solutions on the market. It concluded in some radiation qualified digital solutions, but these were rejected due to high costs. A few commercial products were found too, which might have potential in future development. No directly new concept guaranteed a radiation tolerance alternative except in one case, where the costs were too high, so a decision of improving the original feedback was made.

Three new alternative solutions were evaluated in the form of simulations with a base of synchronization: a load design, an improved *UC1901* design and a delta sigma design, where the two first alternatives were planned to be constructed on a PCB. But due to high manufacturing cost of the PCB, consequence led to that only the load alternative was constructed on a stripboard.

The load feedback uses a three winding transformer, where one winding is pulsed with a square carrier signal. The secondary side act as a load which includes the voltage error in the carrier and couple the signal to the PWM-circuit via the other primary winding. Implementation of the load feedback to the original converter was made and resulted in a stable operation as in the original feedback. Due to some issues with the optimization of the load feedback, the thesis resulted in an operational load feedback with limited performance. A major advantage with the new load feedback compared to the original is the use of simple radiation hardened components.

In addition, an alternative symmetric load variant was simulated and showed promising result for further development.

Future work would be a closer analysis and optimization of the load alternatives after a PCB implementation, but also evaluation and testing of the other alternatives.

Keywords: Radiation, Space environment, TID, SEE, Galvanic isolation, DC/DC converter, Feedback, Amplitude modulation, Delta sigma modulation.

Sammanfattning

Rymden, den okända platsen där satelliter arbetar på våra vägnar. I rymden är solen den enda kända förnyelsebara energikälla, där energin tas upp av solceller som förser all elektronik ombord satelliten via uppladdningsbara batterier. Med en miljö omgiven av vakuum och strålning, behöver elektronik skyddas och konstrueras för att klara av de hårda förhållandena.

Idag finns en DC/DC omvandlare tillgänglig på RUAG Space för att tillgodose elektronik med olika spänningar och effektbehov. Den består av en galvaniskt isolerad flyback topologi med en återkoppling och är för närvarande i drift i rymden, men det finns potential för förbättringar av återkopplingen och därmed har ett examensarbete skapats. Den nuvarande återkopplingen (IC-enheten *UC1901*) använder amplitudmodulering för att överföra ett spänningsfel tillbaka till en PWM-krets som justerar pulsbredden och därmed reglerar sekundärsidans spänningar.

En spjutspetsteknologisk studie har genomförts för att undersöka andra potentiella återkopplings lösningar på marknaden. Den resulterade i några stråltåliga digitala lösningar, men avvisades på grund av för höga kostnader. Några kommersiella produkter hittades också som skulle kunna ha potential för framtida utveckling. Inget direkt nytt koncept garanterade en stråltålig alternativ utom ett fall där kostnaderna var för höga, så ett beslut togs att förbättra den ursprungliga designen.

Tre nya alternativa lösningar utvärderades genom simuleringar med utgångspunkt på synkronisering: en last design, en förbättrad *UC1901* design och en delta sigma design, där de två första alternativen planerades att konstrueras på ett kretskort. Men på grund av för höga tillverkningskostnader för kretskortet slutade det med att endast last alternativet konstruerades på ett experimentkort.

Laståterkopplingen använder en trelindad transformator, där en lindning är pulsad med en fyrkant bärvågssignal. Sekundärsidan fungerar som en last som inkluderar spänningsfelet i bärvågen och skickar signalen vidare till PWM-kretsen via den andra primära lindningen. Implementeringen av laståterkopplingen till den ursprungliga omvandlaren gjordes och resulterade i en stabil arbetspunkt som för den ursprungliga återkopplingen. På grund av problem med optimeringen av laståterkopplingen, resulterade arbetet i en fungerade laståterkoppling med begränsad prestanda. En fördel med den nya laståterkopplingen jämfört med originalåterkopplingen är användandet av enkla stråltåliga komponenter.

Utöver ovanstående lösningar hittades en symmetrisk laståterkoppling som simulerades och visade lovande resultat för vidareutveckling.

Framtida arbete skulle kunna vara en noggrannare analys och optimering av laståterkopplings alternativen efter en implementering på ett kretskort, men också utvärdering och testning av de andra alternativen.

Acknowledgements

I would like to thank Fredik Öhlund, manager of the Digital Data-Handling Electronics (DHE) department at RUAG Space, for giving me the opportunity to work on this thesis and improve my knowledge in the field of power electronics.

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Lars Johansson, Gothenburg, 1 December 2015

Contents

1 Introduction

Satellites and launchers that operate in space have a much more extraordinary environment compared to earth environment, for example vacuum, radiation etc. A key component in space applications are power electronics which must be able to withstand specific requirements to operate in space. The most vital problem lies in radiation that degrades commercial components.

The requirements on space components are very high as they can not be replaced if failures occur. The power supply is often batteries that distribute the power to the different devices through DC/DC converters. Normally, each circuit design tries to keep the amount of components to a minimum as space/weight is generally a limitation.

At RUAG Space, a flyback typology is used with a PWM controlled transistor. The DC/DC converters that are developed at RUAG Space in Gothenburg are both galvanically isolated– and non-isolated converters. With a galvanically isolated transformer, it is possible to connect several secondary windings to feed different devices with its required voltage. This implies that the primary side grounding is placed separately from the secondary side which has a floating ground that is commonly connected to the frame of each device. In general, transformers are widely used as isolation in space associations as it has been around for many years and has showed to be a proven and reliable method.

There are an amount of commercial state of the art technologies available on the market, but they are probably not suitable for space applications due to radiation. A number of these technologies may have potential to be developed even further to handle the space conditions.

Today's challenge is to transfer feedback signals from the secondary side over the galvanically insulated transformer to a PWM-circuit on the primary side in order to control the voltage output. The analog control signal that needs to be transferred to the primary side is today solved by using amplitude modulation, but there are potentials for improvements. Due to this, a thesis has been created in order to investigate if there are any other topologies or solutions that could improve the DC/DC converter feedback for space applications.

A previous thesis has investigated (2006) different ways to transfer feedback signal for space applications. Theirs results ended up in two recommendations for further developing, but they also suffered from some drawbacks. The first one was based on a pulse edge transformer which uses a pulse detector as receiver on the primary side. The concept was to generate PWM pulses containing information from the secondary side and take out the ON- and OFF-times of the pulses through a pulse edge transformer, so that only small peaks with a very narrow width are transferred. For reconstruction, additional components are needed to convert the peaks back into PWM pulses to the transistor. Some issues were that no radiation testing data was available for the evaluated constructed component and also some start-up problems as the PWM is located on the secondary side.

The second option was a synchronized forced output converter, pre-designed by the staff of RUAG Space, which had two coupled output windings on the transformer. The first primary winding is fed with constant duty cycle and is linked with the two other windings located at the primary and at the secondary side respectively. The secondary output (feedback path) forced the primary output voltage to be linked making the feedback signal be seen as a variation of the output voltage on the primary side. The conclusion was that the bandwidth causes a trade off with the ripple magnitude and resulted in a low-reliable feedback. The recommendation concluded a continuous use of the present solution with an IC-unit called *UC1901*, an amplitude modulation circuit. For more detailed information of the previous thesis, the reader is referred to [1].

1.1 Purpose

The purpose/goal of this thesis is to evaluate topologies or new circuit solutions to galvanically transfer analog control signals for satellites and launchers. This could be done by analysing in what way commercial state of the art technology in power electronics can be inspired to be further developed for use in satellites and launchers with its specific requirements for the environment and reliability.

1.2 Limitation

The thesis is focused on finding a better solution for the present galvanically insulated feedback circuit and relevant limitations will be made during the time that are considered to be reasonable. As the time is a limiting factor, only a few alternatives will be evaluated at the end. The new solutions will tend to be as close to space compatibility as possible.

1.3 Task

This master thesis deals with a number of aspects that need to be investigated. From how the harsh space environment influence the electric components to possibilities of finding new solutions to galvanically transfer feedback signals. Examples of methods that can be used to transfer feedback signals are transformers, optocouplers etc. The main problems and hypotheses that are going to be discussed in this report are the following:

- How the space environment affect the electrical components and use protective measurements?
- What are the basic requirements for power electronics in space?
- How the current switched DC/DC converter at RUAG Space is operating with its feedback?
- Are there any better available solutions for galvanically transfer signals today?
- Research after state of the art technologies towards feedback solutions, if they are suitable for space applications?

1.4 Method

To be able to search for new solutions and technologies for galvanically transferred signals, it is necessary to gain an understanding of how the electrical components are affected by the space environment. It will require literature studies at start and followed by researching after state of the art technologies. Also an insight of the present solution will be included. During the research, evaluations and simulations will take place to find the most suitable alternatives. A construction of a circuit-prototype of the selected alternatives including verification of the models will be made.

2 Space Environment

Satellites and launchers are exposed for a harsh environment in space, with many factors to consider. Simulation and reconstruction of the space environment are very complex and costly for its effects on electronics and are severe to perform on earth. There are certain tests that can emulate some effects from space, i.e. certain radiation conditions, vacuum etc. The primary effect that results in failures and decrease in performance in space electronics is radiation. On earth, where commercial products are used, they are not affected by the radiation in the same extent as in space. Except in nuclear – and military environment, where radiation exist. Earth magnetic field and atmosphere act as a filter and stop a large amount and highly energetic radiation. The magnetic field is divided into different zones under the name Van Allen belts.

There are a lot of phenomena that can happen in space and next is a brief introduction in space conditions towards electronics on radiation and thermodynamic [2], [3].

2.1 Radiation

Electronics in space are in general exposed for radiation in the form of protons, neutrons, electrons, nucleus, photons, heavy ions etc. These effects emerge from solar irradiations and cosmic rays. The interaction between radiation and electronics cause severe damage in both material and performance of the component under its life spans. It is common to divide the radiation environment in three different categories:

- Radiation belts: In the radiation belts or Van Allan belts there are mainly protons and electrons in the range of MeV that are trapped by the earth magnetic field.
- Cosmic rays: Arise from continues background radiation from outer space and consist of heavy ions (protons) with energy levels beyond TeV that can induce malfunction or breakdown of electronic devices.
- Solar flares: Radiate mostly energetic protons in the range of 500 MeV, but also heavy ions and electrons arise from the sun [4].

Earth magnetic field trap particles and form the Van Allan Belts. These particles experience a phenomenon that cause them to oscillate back and forth from pole to pole due to the earth magnetic field (density) and make satellites a target for impact [5]. Geomagnetic shielding provides a certain extent of protection for satellites against cosmic rays. The higher the orbit from earth, the lower will the protection from cosmic rays be. At the GEO orbit, altitude of 35 860 km, where most communication satellites operate, the geomagnetic shielding decay strongly and the satellites are exposed to higher radiation. This can be compared with the International Space Station (ISS) that has an altitude around 350 km, depending on the orbit [2], [3].

In contact with electronics various effects can occur. Most sensitive devices to radiation are semiconductors, i.e. MOSFETs, CMOSs, BJTs etc. Other electronics like inductors, resistances and capacitors are very resistant to radiation. Passive electronics can then be considered to be relative immune to radiation [2], [6].

In the space industry there are two main types of terms that characterized components tolerance against radiation: Total Ionization Dose (TID) and Single Event Effects (SEE), where TID is a long-term degradation effect while SEE is an instant damage effect.

2.1.1 Total Ionization Dose

The total ionization dose expresses a long time exposure of radiation for an electrical component in space. This long-term radiation cause altering of the device parameters and performance with time and can result in device failure, i.e. long-term degradation. The unit for TID is measured in Radiation Absorbed Dose (Rad) and indicates the radiation dose for a specific material. The SI unit for Rad is expressed in 1 Gray (Gy) which correspond to 100 Rad. One Gray is defined as the amount of energy per kilogram substrate, where the substrate often is referred to silicon (Si) as it is the most common used semiconductor material [7].

RUAG Space constructs theirs electronics to managed TID levels of 100 kRad [8].

2.1.2 Single Event Effects

Single event effects are rare events that is caused by a single high energetic particles in MeV range. As the name suggest, it creates a single instant damage effect. Radiation has a certain amount of energy when it interacts with a component. During the interaction, the radiation transfers its energy into the material of the component and it is defined as Linear Energy Transfer (LET). LET described the amount of radiation energy that is deposited in the material per unit distance under collision. The SI unit is newton (N) but is more commonly used in MeVcm^2/mg in space associations, where

$$N = \frac{MeV}{cm} = \frac{MeV}{cm} / \frac{mg}{cm^3} = \frac{MeVcm^2}{mg}$$

and mg/cm^3 is the density of the material. SEE causes several effects on components and can be categorized in different special events depending on the energy level, radiation type and LET: Single Event Latch-up (SEL), Single Event Transient (SET), Single Event Upset (SEU), Single Event Burnout (SEB) etc. Note that SEE are single events and are very hard to predict when and if they will happen. It requires probability calculations as well as knowledge of other factors to come up with a certified guess. Manufactures might define SEE with the energy in MeV that is the maximum energy of a particle which the component can withstand independent of the incident angle or with the level of LET [7].

SEU

Single event upset error is associated with radiation on digital electronic. The effect changes the state of data bits, i.e. from 1 to 0 or vice versa. It might even take an undefined value. For memory devices, it can lead to corrupt data and requires a cleaver error detection algorithm to correct the error. No physical permanent damage occurs on the device and it will continue to work [2].

SEL and SEB

Are classified as hard errors and are applicable in n-p-n-p structures, such as MOS transistors. Single event latch-up can occur when a single high energetic particle collide with a MOSFET transistor, causing an ON-state on one of the parasitic transistors inside its structure. The

ON-state of the parasitic BJT opens a path between drain and source, creating a short circuit. Depending on the application, normal operation of the device can be achieved without any damages after a complete shutdown of the power supply. For example in low power applications such as driver circuits using CMOS technology. But the influence of the error can naturally cause greater damages on components in the vicinity [2], [7].

The effect of SEL can also cause catastrophic damage as stated above and can be related with SEB. The term SEB is often referred to higher power applications, DC/DC converters. The SEB effect was initially noted for power semiconductors (power BJT, power MOSFET) vertical structures which also inherent an unwanted parasitic BJT from its manufacture stage. Figure 2.1 shows a part of parasitic elements for a power MOSFET model. The parasitic BJT is normal OFF during operation and is also present in normal MOSFETs (both vertical and horizontal). SEB is related to strike interactions in the component during its OFF-state and can lead to a short circuit between drain and source when the parasitic BJT is activated [2], [9], [10].

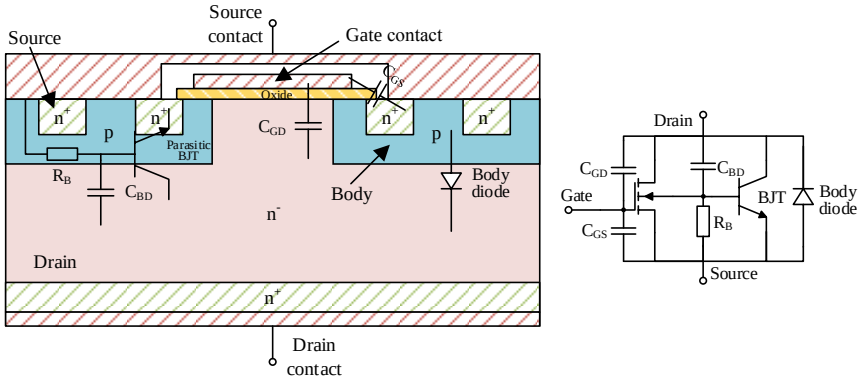


Figure 2.1: Representation of a power MOSFET with a part of parasitic elements.

Appendix A presents an example of the effect of a SEL for a CMOS device and a SEB for a power MOSFET.

SET

When a particle hit a supplied electrical device an induced voltage can emerge. This can cause a SEU for digital devices or voltage transients for analog circuits. This set further requirements for components in space environment to handle transient condition [7].

2.2 Thermal and Vacuum

Many are familiar that vacuum appears in space or at least very low pressure. Ideal vacuum is defined as zero pressure and with no particles around. In such an environment, heat transfer for components is limited as no medium is available.

Thermal heat can be divided into three states: radiation, conduction and convention. Radiation in the form of EM-waves that radiate energy to matter or vice versa and is described in wave-length, IR-light >700 nm. Conduction is to transfer energy between two solid materials. The energy is

transferred by moments of the atoms inside the material. Convention is similar to conduction except it is only valid for liquids and gases, for example heat pipes.

In satellite constructions, without any free molecules, the only way to transfer heat is through radiation as vacuum is present. Conduction and conventions are possible too, but only to direct the heat to another place on the satellites. Figure 2.2 illustrates the two concepts for a component. To remove waste heat created from electronics and absorb heat from the environment, satellites use special radiator surfaces to reject heat in infrared (IR) radiation into space. Satellite radiators can radiate around 200 W waste heat from electronics per square meter. For more details about radiator on satellites structure, the reader is referred to [11].

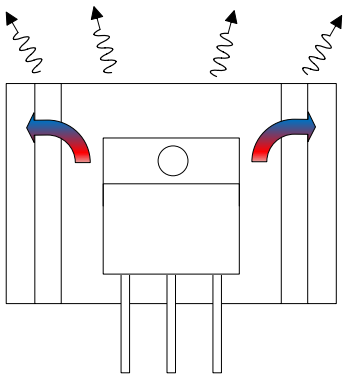


Figure 2.2: Illustration of radiation and conduction for a component.

3 Material Influence of Radiation and Vacuum on Semiconductor Components

A consequent from TID and SEE when a material is irradiated can result in two situations: ionization and atomic displacement. Which effect that occurs depends on the radiation and its strength. Both these effects can have permanent damage on the components. High energetic partials (ions, protons, photons etc) can penetrate into the material and transfer its energy through interaction with the material, it can also lead to a scattering mechanism which increase the damages.

Materials that are used in space need to tolerate radiation over a long time span. Radiation attenuation is related partly to the material density, where higher density gives a better radiation tolerant material. Besides consideration of radiation, outgassing of chemicals is another factor that can cause failures in vacuum. Other aspects to consider are high thermal cycling, flammability, material stress etc. Some materials used in space associations are ceramic, aluminium (Al), copper (Cu), metals and different alloys combinations [12].

3.1 Displacement Damage from Radiation

The materials of the electrical components consist of many crystal lattice structures that make the core of its operation. When high energy photons and particles interact with the material, it can alter the lattice structure through atomic displacement, i.e. shift the atoms arrangement from its original position. This causes some unwanted effects as changing the electrical properties, creating forbidden band gaps and possibilities to become ionized or more displacement. A defect lattice structure introduces degradation and in worst case failure of the component. There exists a self-healing process that starts after the displacement of the atoms to bring them back to their original position, but some damage will be permanent.

Especially bipolar components are very sensitive to displacement damage due to theirs structure, i.e. base conduction devices. The shift of atoms in the base lattice structure influence on the minority carrier lifetime in terms of increased recombination within the base region. Where the minority carrier affect the transistor gain, $\beta = I_c/I_b$.

The minority carrier lifetime is defined as the average time it takes for a minority carrier to recombine. With increased recombination of the minority carriers in the base region (or reduced minority carrier lifetime), less majority carriers from the emitter will diffuse into the collector as they recombine in the base, which decrease the collector current. In standard use (in non-radiation environment) this effect is relative low. In space, designers must take a large range of the transistors gain into account when designing electronics compared to normal conditions where the gain β is more stable [2], [5], [13]. Figure 3.1 illustrates the electrons– and holes direction for a NPN-transistor.

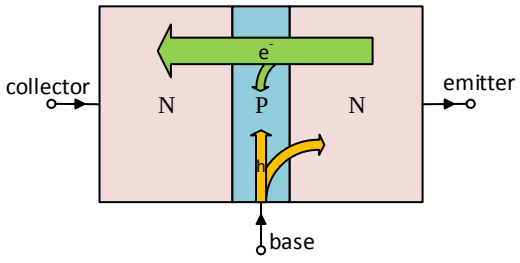


Figure 3.1: Illustration of a NPN BJT transistor with electrons– and holes direction in the active region.

3.2 Ionization from Radiation

When radiation with enough energy collides with an atom inside the material, the outcome is ionization. It means that the bindings inside the atom breaks and valance electrons are excited to the conduction band and leaving a certain number of free holes and free electrons in the material. A fraction of these extra holes and electrons recombine instantly and others drift inside the material. The effects from ionization can lead to charge build-up, shift of the threshold voltage for example a MOSFET, increased leakage current, transient effects and in other words degradation. Ionization affect mainly MOSFETS structures, i.e. surface conduction devices [2], [5], [14].

But there exist effects for BJT transistors as well. For example a NPN BJT, there positive charges may be captured inside the screen oxide layer surface between the base and emitter, see figure 3.2. With a certain base current that is required to set the BJT to ON-state, an amount of electrons will recombine at the surface with the positive charges between the base and emitter. This will lower the total electrons that will reach the collector and will then affect the transistor gain, $\beta = I_c/I_b$ [2], [5], [13].

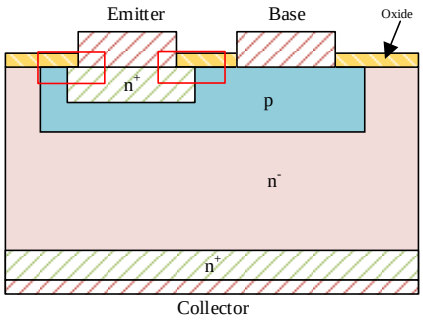


Figure 3.2: Illustration of NPN BJT transistor.

3.2.1 Threshold Voltage Shift in MOSFET Transistors

Enhanced MOSFET transistors have a threshold voltage of a couple of volts which is used to switch operation state (OFF/ON-state), namely open a conducting channel in between the drain and the source. Due to ionization from radiation, induced charge is build-up close to the gate and results in shift of the threshold voltage. An N-MOSFET will be taken as an example to illustrate the concept of threshold voltage shift.

One of the sensitive places for radiation to interact is beneath the gate contact, where a narrow layer (nm) of oxide is present. When irradiation on semiconductor occurs, in this case in the gate oxide, electron-hole pairs are created in the oxide, where some of these will recombine at instant inside the material.

The remaining electrons caused by the radiation will be swept out from the oxide layer in less than a few picoseconds as the mobility of electrons is almost the double of holes. In contrast, the remaining holes stay in the gate oxide and build-up a positive charge. With continued radiation, the charge start to increase and will attract free electrons in the substrate below the oxide and when it reached the threshold voltage a conducted channel opens between the drain and the source.

These external charges act as a continuous voltage source and will reduce the amount of positive

voltage that needs to be applied to the gate in order to set the MOSFET transistor to ON-state. This result can be seen as a decrease of the threshold voltage, namely a shift to the left in a drain-current gate-voltage diagram, see figure 3.3. The curves (I) to (IV) illustrate the effect of increasing radiation. When the positive charge becomes higher than the threshold voltage (II), the MOSFET transistor will be turned-ON all the time. To shut down the N-MOSFET transistor a negative voltage is necessary to be applied to the gate.

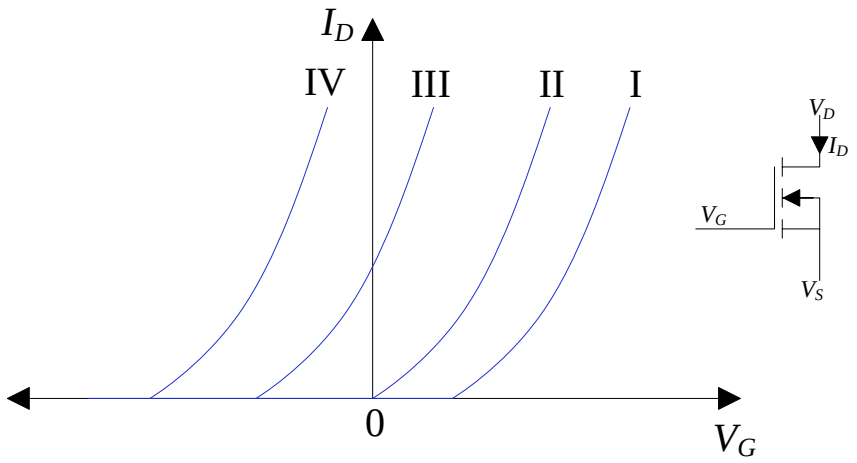


Figure 3.3: Voltage threshold shift due to radiation for a N-MOSFET, where (I) represents the manufacture default design and (II) to (IV) indicate increased radiation.

The trapped holes inside the oxide also experience a long term recovery and aim toward zero volts. The recovery process is dependent on several factors as the annealing temperature, time, continuous radiation etc. The last part delays the recovery process as new electron-hole pair is formed [15].

MOSFETs that are used in space are influenced by this phenomenon above over a long time period as they are constructed for the space environment, but not in the same scale as for commercial MOSFETs that would be ON all the time after a short period.

3.3 Shielding and Vacuum

Shielding against radiation is important both for electronics and for crews on spaceships. To stop particles, a shield in the form of a mass is placed between the objects. Low energy particles in the range of keV to MeV can be absorbed by the shielding material if it has enough depth. In the Van Allan belts where most of this particle levels lie, the satellites can be protected. For higher energy levels as GeV or higher, it will require a very thick shielding and would not be practical in reality, then other methods need to be applied [2]. Aluminium is one of the main materials used for the satellite in terms of weight and formability. For example shiny Al-foils cover the satellites and act as cloth for the satellites to adjust the temperature [8].

Ceramic IC-packages are often used for space components, partly to withstand high temperature cycles and prevent outgassing of chemical. Plastics IC-packages are avoided as it contains chemicals that might expand under vacuum and crack the plastic IC-package and thereby damage the component [8].

A comparison of a space– and a commercial component can be seen in figure 3.4. From a visual point of view, the space component looks more robust and seems to be of better quality. Besides that, a weight different can be noted when comparing them by hand.

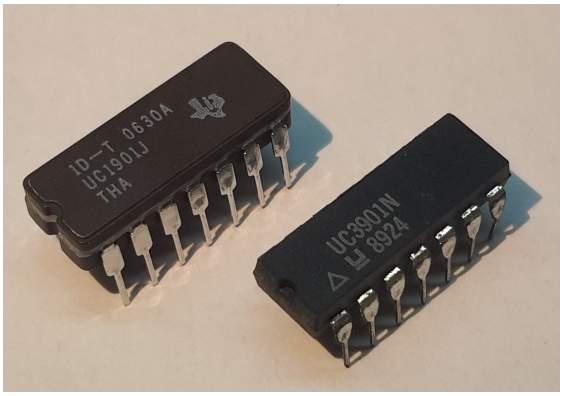


Figure 3.4: Space– (left) and commercial (right) component of the *UC1901*.

4 Present DC/DC Converter and its Feedback Solution

At RUAG Space today, two feedback solutions are available, one with galvanic isolation and the other with a non-isolated feedback. The isolated one uses a planar transformer to transfer the feedback signal which consists of the error between the actual value of the feedback voltage and a reference value.

The galvanically insulated design at RUAG Space consists of a flyback DC/DC converter topology, which can operate in both DCM and CCM. It has a PWM control circuit on the primary side and several magnetically coupled outputs on the secondary side, i.e. poly outputs. Where one secondary output is chosen to act as feedback to regulate the voltage level. The other voltages on the secondary side are cross-regulated which is an effect from a single feedback. A schematic illustration of the converter can be seen in figure 4.1.

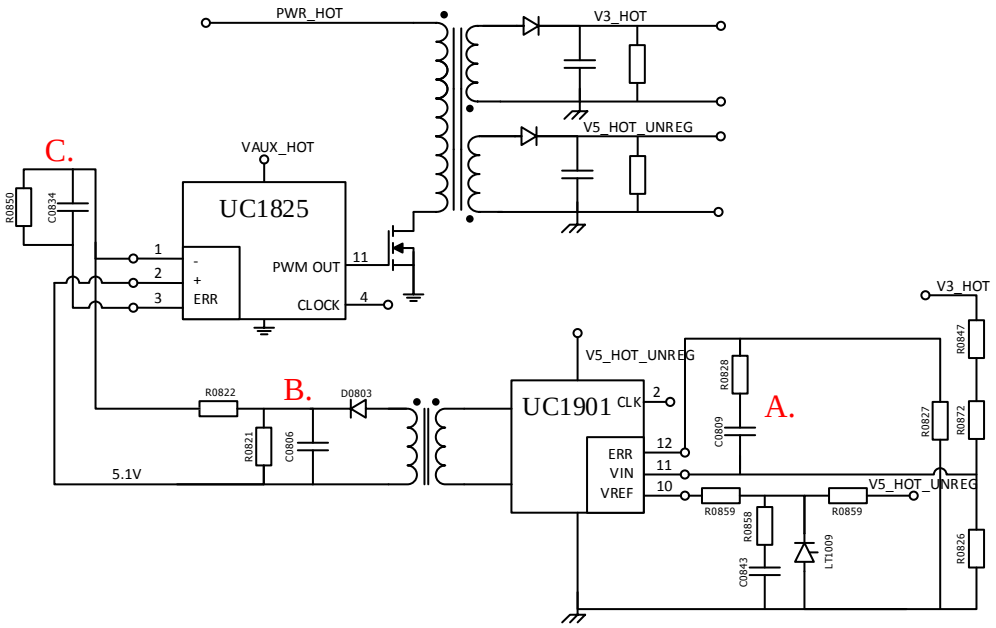


Figure 4.1: A schematic illustration of the current DC/DC converter with the isolated feedback, where A, B and C symbolize compensation nets.

The PWM controller *UC1825* from Texas Instruments (TI) is used on the primary side to control the gate pulses to a MOSFET transistor [16]. This component is space classified and has been tested for radiation environment. On the secondary side, the feedback consists of the TI-component *UC1901*, an amplitude modulator component with a built-in error amplifier (EA) that shall transfer the voltage error over a transformer [17]. The principle of Amplitude Modulation (AM) is described in section 4.2. A DIP-package is used at RUAG Space and is shown in figure 4.2 for both components mention above. For pin-configuration, the reader is referred to the data sheet of respective component.

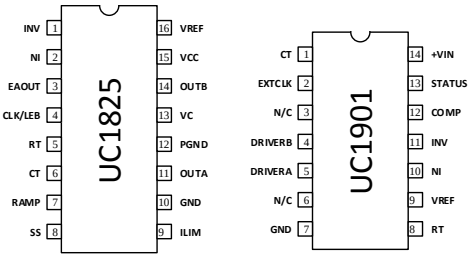
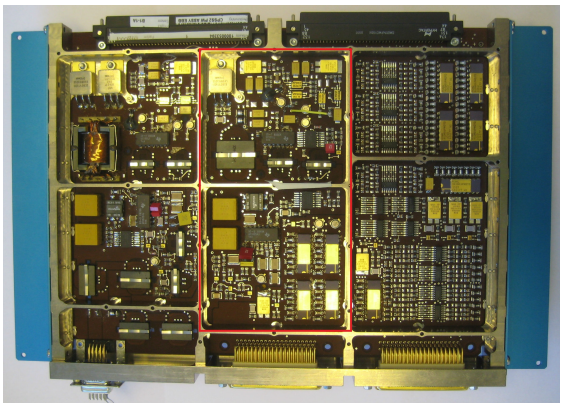


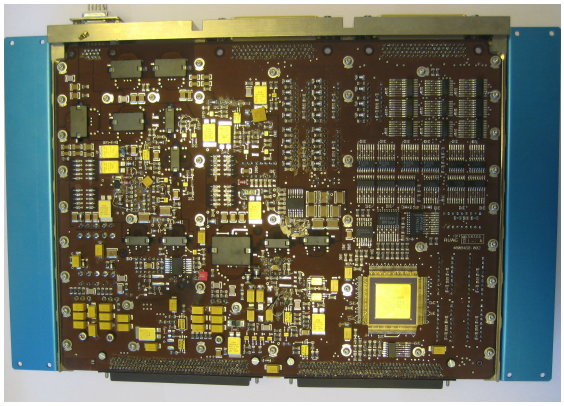
Figure 4.2: DIP-package of the *UC1825* and the *UC1901*.

The *UC1901* has been tested for radiation conditions and is certified as a space component. From the behalf of RUAG Space, radiation tests have been performed 2011 for a specific batch for TID doses up to 150 kRad and heavy ions in range of MeV. No functional failures occur for TID, but some minor parameter failures were observed. It was considered to withstand TID up to 100 kRad [18]. For SSE-tests no latch-up was detected up to LET level of 85 MeVcm^2/mg and no SET up to 60 MeVcm^2/mg resulted in abnormal function longer than 32 μs [19].

The current DC/DC converter with the *UC1901* as feedback has already been installed in several satellites and is operational. The circuit board is circa 19.2 mm x 25.6 mm and consists of 16 layers PCB. On this particular module in figure 4.3 there exist two more or less identical DC/DC converters with a power of approximately 35 W each. The two DC/DC converters are referred as index HOT and COLD, where the HOT converter will be used as a reference through the report. Figure 4.3 shows the top side respective the back side of the circuit board [8]. The HOT converter is marked in red in figure 4.3a.



(a) Top side of the circuit board, where the red square indicate the HOT converter.



(b) Back side of the circuit board.

Figure 4.3: The circuit board module of the present DC/DC converter.

The principle of operation can be described as following from figure 4.1. The voltage $V3\_HOT$ is selected as the regulated feedback voltage, where the other voltage outputs are cross-regulated. The $V3\_HOT$ has a reference voltage of 3.29 V and is chosen for the purpose that most processors in satellites use it as supply voltage. The 3.29 V is scaled with a resistor network to correspond to the fixed reference voltage of 2.5 V, which is the input to the error amplifier in the *UC1901*. The error is modulated into AM-pulses inside the *UC1901* with a maximum magnitude from $\pm$2.5 V

over a transformer. The amplitude of the AM-pulses is proportional to the magnitude of the error from the amplifier. On the receiver (primary) side, the error is recovered and continues to a second error amplifier in the *UC1825*, which generates gate pulses with correlation to the received error. The *UC1825* Pin 2 is connected to a 5.1 V reference voltage that is generated from the IC-unit.

Observe that this particular DC/DC converter use the *UC1825* component to act as a boost for the PWM pulses if the Scaled voltage level at $V3\_HOT$ is below the reference of 2.5 V in the *UC1901* error amplifier. And for voltage above 2.5 V reference, the *UC1901* acts as a brake to lower the voltage, thereby lower the pulse width of the PWM. The boost option comes from the surrounding components that makes the pulse width increase when the *UC1901* output zero voltage. The negative error is rejected inside the *UC1901*, i.e. the feedback can only lower the voltage $V3\_HOT$.

4.1 Feedback Parameters

For both open loop and closed loop systems, stability is very important to obtain. In some cases a closed loop systems can be stable even if the open loop system is unstable. Consider an open loop system, to prevent a such system to be unstable, the system can not contain any poles in the right half pole plane of a Nyquist diagram. Namely, the phase must not reach $-180°$ until the total gain of an open loop system is below 0 dB. This is referred as a phase margin, see figure 4.4, where (I) represents the phase and (II) the gain. Instability and an oscillating system are the result of poles in left half pole plane. Usually, a phase margin of at least 40° is preferable for safe operation.

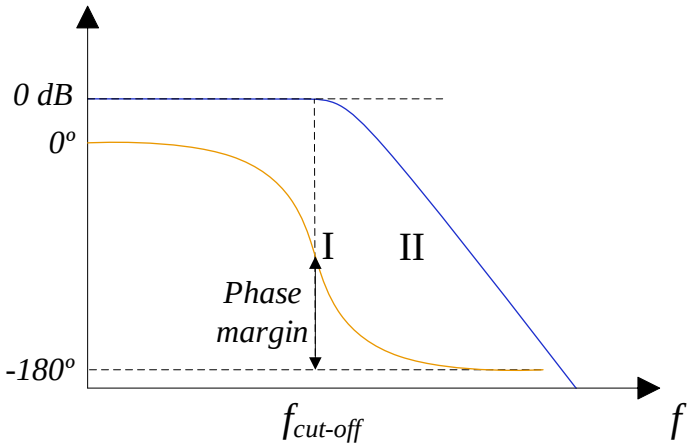


Figure 4.4: Phase margin definition at a cut-off frequency $f_{cut-off}$ for a system.

A system bandwidth (BW) indicates how fast the system can adjust to changes. A high bandwidth is often desirable in most system, but that can also introduce high-frequency noise which may influence on the performance.

A system with both high bandwidth and phase margin are preferable, but they are contradictions to each other. In order to increase the phase margin, for example by introducing a dominate pole at a lower frequency in the bode diagram. The 0 dB cross-frequency occur earlier and the phase margin increase. This in turns decrease the bandwidth with cost of stability.

4.1.1 Potential Improvements of the DC/DC Converter

Today, a working system with the *UC1901* and the *UC1825* are available, but there are potential for improvements. Some issues with the current model are:

- Several filters are required in the feedback which set performance limitation of the DC/DC converter.
- Unwanted frequency components in the system due to asynchronous switching between the PWM and feedback circuit.
- Start-up issues.
- Dependence on the IC-component *UC1901*.

Filter in the feedback loop is required to obtain a functional system. If only poles were investigated, a quick overview from the input Pin 11 of the *UC1901* to Pin 3 of the *UC1825* in figure 4.1 shows that the first compensation net (A.) has a pole that set a phase shift in the bode diagram with $-90°$. Then an additional pole at the demodulation step (B.) shift the phase to total $-180°$. The last compensation net (C.) into the *UC1825* to $-270°$ in total plus a $-180°$ shift of the negative feedback. This would cause an unstable system for frequencies above the unity gain. Naturally, there exist zeros that compensate for phase shifts in the system.

To comment, the pole at the demodulation step (B.) is probably a high frequency pole (due to low input resistance) and will not influence on the stability as it lies fare away from the other poles. Meaning that the 0 dB level is reached before the pole creates a $-90°$ phase shift.

The start-up procedure is always a problem with isolated systems as the power often only comes directly from the primary side. Today's solution is based on using a soft starter from the *UC1825* component. The soft starter use a capacitance connected in parallel to the input Pin SS. As a constant current is fed to the capacitor, it causes a charge build-up and thereby increased voltage at SS-pin. The EAOUT Pin 3 follows the SS-pin with the increased voltage and increases the gate pulse width at the output until the secondary side feedback (*UC1901*) start after acquired enough supply voltage and take over the control.

The presence of the IC-unit *UC1901*, cause a dependence on that every bought batch could manage the radiation requirements as the manufacture procedure might differ from batch to batch. Also the built-in complexity in the *UC1901* increase the fault occurrence. This is valid for most of the components, but simpler construction may give better reliability and robustness. A recent radiation report (2015) revealed that for a current batch of the IC-unit *UC1901* only could managed less than 25 Rad. Which shows that there exists a need for other solutions.

Besides the radiation, the *UC1901* is bounded to have two integration in the feedback path and thereby makes is more difficult of increasing the bandwidth for example. Also as each component of the IC-unit is unique, optimization of each DC/DC converter module is necessary, which leads to a costly development process. Furthermore, the current IC-package does not go through all the PCB layers, which is another complication.

Another influence is the voltage ripple that arises at reconstruction of the error (B.). The maximum allowed voltage ripple from the reconstruction signal is set by the compensation network/filter (C.) into the *UC1825*. It is due to the available dynamic range for the *UC1825* amplifier that sets this limitation, which lies with margins around 1 V to 5 V. This will be explained further in the report.

4.2 Amplitude Modulation

Modulation techniques are used to modulate data in such cases where the data can not be transferred alone. It is common to apply such techniques to systems that do not have any physical contact. From the use of transmitting radio signals to electrical isolation. One type of modulation is called Amplitude Modulation (AM), which is commonly used in radio application. There are different types of AM available, but the most common used is the Double-Side Band Full Carrier (DSB-FC) and is often referred as the ordinary AM. Other types are Single Side Band (SSB) and Double Side Band (DSB), see figure 4.6 [20].

The concept of AM is a modulation of a signal with a carrier signal in such a way that the amplitude of the AM-signal is proportional to the input signal. The AM-signal can then be transmitted via an antenna as EM-signal or via a transformer as magnetic field. At the receiver end (B.), a demodulation step occurs to reconstruct the signal.

The carrier signal can be modelled in many shapes: sinusoidal, sawtooth, square waves etc. According to Nyquist sample criteria, the carrier frequency shall be at least the double of the message/input signal frequency to be able to fully reconstruct the signal [20]. The principle of a modulated sinus signal can be seen in figure 4.5.

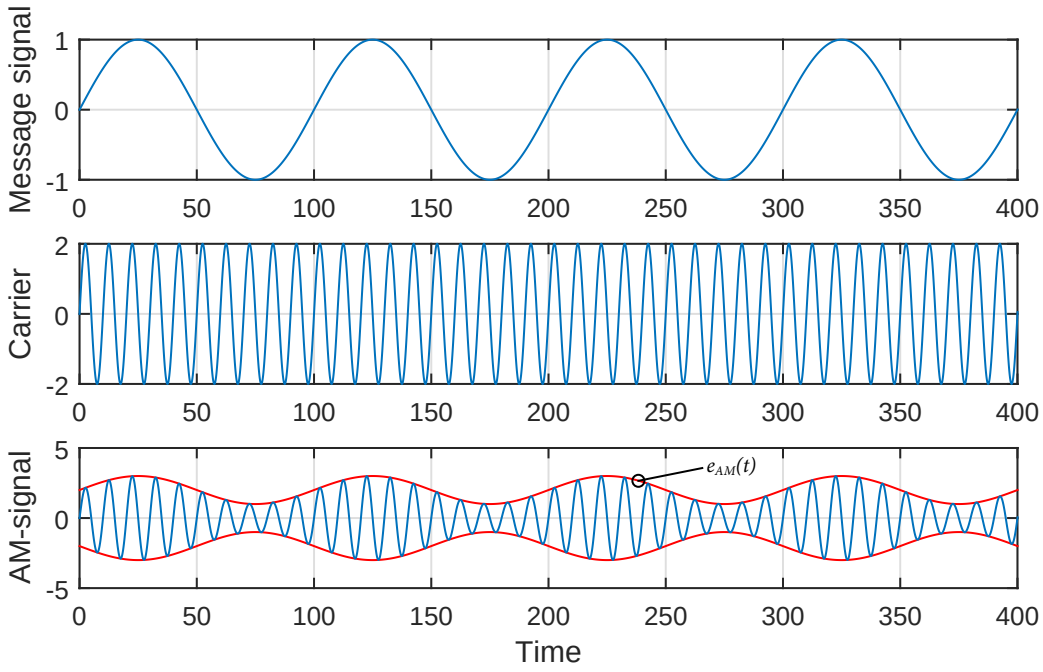


Figure 4.5: The principle of amplitude modulation with a sinusoidal carrier and message signal, where the red curve illustrates the envelope curve.

Let $m(t)$ represents the input signal, $c(t)$ the carrier signal, $e_{AM}(t)$ the envelope signal and $s_{AM}(t)$ the AM-signal. Assume that

$$m(t) = A_m sin(\omega_m t) \tag{4.1}$$

and

$$c(t) = A_c sin(\omega_c t), \tag{4.2}$$

where A_x represents the amplitude of each signal and let $\omega_m \ll \omega_c$. To be able to reconstruct the modulated signal an additional criteria must be fulfilled. That is, the amplitude of $m(t)$ must be less or equal to the carrier signal amplitude $c(t)$, i.e. $A_m \leq A_c$. In case of the opposite, there will be distortion in the signal $s_{AM}(t)$. This phenomenon is referred as overmodulation. From the signals amplitudes, a modulation index can be defined as

$$M = \frac{A_m}{A_c} = \frac{e_{AM,max} - e_{AM,min}}{e_{AM,max} + e_{AM,min}}. \tag{4.3}$$

The modulation index can obtain values from 0 to 1, where 1 indicate $A_m = A_c$ and is said to be 100 % modulated. Index greater than 1 cause overmodulation and fully reconstruction is not possible.

The envelope curve is describe as a combination of the modulated signal with the carrier amplitude A_c. The upper and lower curve can be computed according to

$$e_{AM}(t) = \pm[A_c + A_m sin(\omega_m t)] \tag{4.4}$$

and are visible in figure 4.5 (red). To express the AM-signal function, (4.4) is multiplied with the carrier AC-part and a complete model of the signal is obtained as

$$s_{AM}(t) = e_{AM}(t)sin(\omega_c t) = A_c sin(\omega_c t) + \frac{A_m}{2}cos((\omega_c - \omega_m)t) - \frac{A_m}{2}cos((\omega_c + \omega_m)t). \tag{4.5}$$

The sign for s_{AM} from (4.4) only set the starting value sign and can be selected arbitrary as the signal is symmetric.

According to (4.5), the frequency content consists of two new signals. Depending on the carrier signal, these Low Side Band (LSB) and Upper Side Band (USB) arise and include a range of frequencies. For a sinusoidal signal as carrier, two new frequencies are created,

$$f_{LSB} = f_c - f_m \text{ and } f_{USB} = f_c + f_m, \tag{4.6}$$

where f_c is the carrier frequency and f_m the modulation frequency.

The bandwidth of the AM-signal is then defined as $f_{USB,max} - f_{LSB,min}$. Note that the message is stored in the side bands and not in the carrier, see figure 4.6.

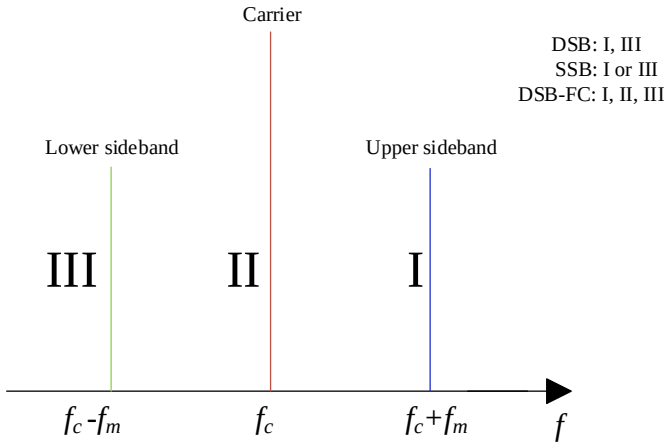


Figure 4.6: Side bands frequencies of a amplitude modulated signal with a sinusoidal carrier.

To recover the message from the AM-signal, a type of detector is required, a diode (envelope) detector or a product detector. The diode detector is by far the simplest one and gives quite good result. The product detector is more accurate, but more complex compared to the other one.

For space context, simplicity is often preferred, therefore the diode detector is an attractive choice. A diode detector consists of a diode and an RC-circuit, see figure 4.7.

When an AM-signal is received by the primary winding, under the positive half-period, it is rectified and starts to charge the capacitor. During the negative half-period the capacitor is discharged through the resistor with the time constant RC. For optimal demodulation of the modulated signal for a diode detector, the time constant shall lie in the range of

$$\frac{1}{f_c} << RC << \frac{1}{f_m} \tag{4.7}$$

and it can only happen when $f_c > f_m$ [20].

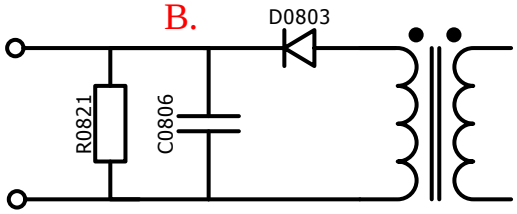


Figure 4.7: A diode/envelope detector for reconstruction of a message signal from an AM-signal.

In our application, the *UC1901* uses a square signal to modulate the message signal. Figure 4.8 illustrates the concept with a sinusoidal as error signal. A square carrier consists of several sinusoidal signals at different frequencies which generate a number of LSBs/USBs in the frequency spectrum, see figure 4.9. The signal is retrieved with the diode detector presented in figure 4.1. Note that in the present circuit configuration with the *UC1901*, the reconstruction is only concerned about the absolute value of the envelop curve. Also that the message consists of a range of frequencies, from DC and up.

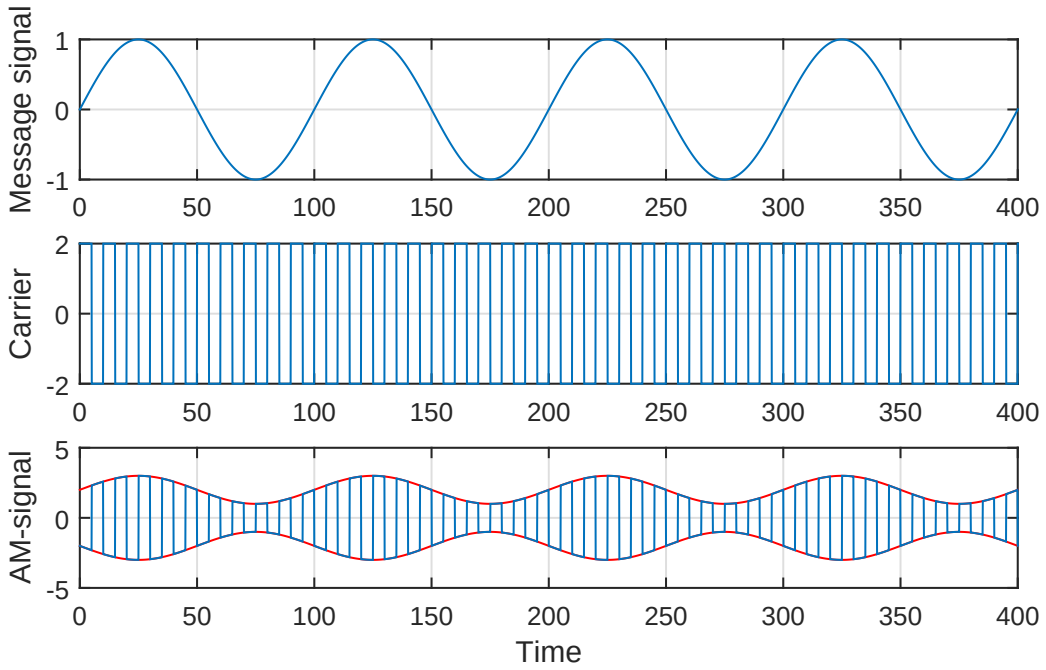


Figure 4.8: Amplitude modulation with a square wave carrier and a sinusoidal error signal. The red curve illustrate the envelope curve.

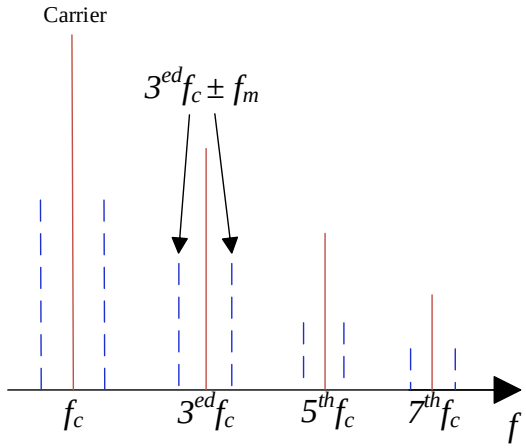


Figure 4.9: Frequency spectrum of the amplitude modulated signal with the carrier (orange) and LSBs/USBs (blue).

4.3 Measurements on the Original DC/DC Converter

To verify the exciting DC/DC converter performance a couple of measurement were made. Two different setups were performed: the DC/DC converter in its original state and a setup where only the *UC1901* was studied. A test report was written and following is a summary of the result.

The input voltage (PWR_HOT) to the system is 28 V and was achieved with a power supply. To assist, an oscilloscope *Tektronix TDS 5104*, a signal generator *Agilent 33250A*, a potentiometer rated 30 W@1.73 A and Fluke multimeter's 179 and 75 were used. The following measurements are performed at a load of 1 A unless otherwise noted. During the measurement a small disturbance signal appeared at the lab bench, a sinusoidal signal with frequency of 50 Hz from the power grid. Countermeasures took place to minimize it to a voltage amplitude of 1 V, but no disturbances were notated during the measurements.

The purpose of the first setup was to see how it operated under normal conditions. Usually, the outputs are connected to different loads, but to insure that the PWM regulation is active, a variable load was placed at the output of $V3\_HOT$ (see figure 4.1) via a breakout cable. A couple of measurements were made at different nodes: output voltages, AM-signal, feedback signal, PWM signal etc.

The gate pulse or PWM pulse operated at a frequency of 170 kHz and the pulse width varied with the load on $V3\_HOT$ as expected. The output gate pulses are generated from the internal clock named CT and CLK/LEB, where the leading edge blanking (LEB) is used to reject inherent noise when terminate the gate pulse. The clock pulse denoted by CT (Pin 6) and CLK/LEB (Pin 4) at the *UC1825* circuit are illustrated in figure 4.10 under stable condition. The frequency was measured to around 340 kHz with a peak of almost 4.3 V for CLK/LEB and 2.8 V for CT.

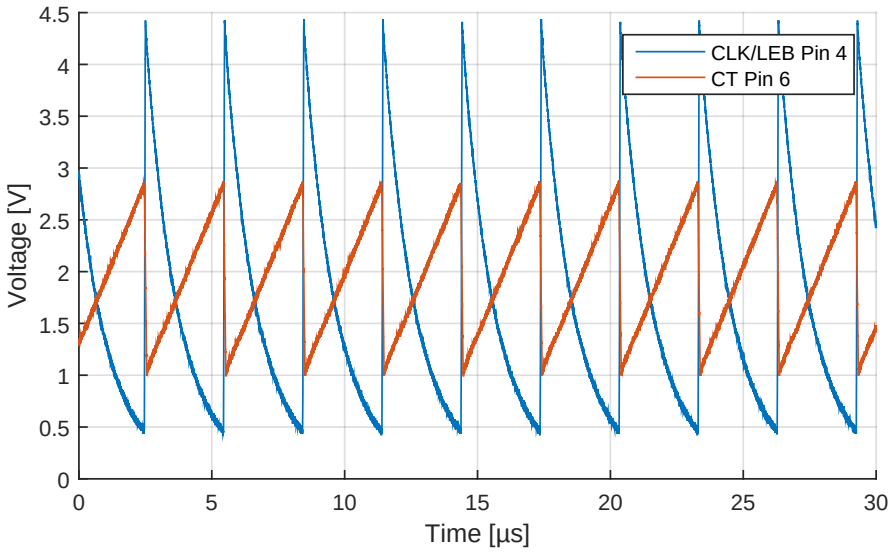


Figure 4.10: The measurement results from CLK/LEB (Pin 4) and CT (Pin 6) at the *UC1825*.

The voltage measurements showed that $V5\_HOT\_UNREG$ had a voltage of 5.48 V and $V3\_HOT$ of 3.29 V respectively. Measured ripple parameters at different nodes can be seen in table 4.1.

Table 4.1: Measured voltage ripple at different nodes.

Parameter	**Ripple [mV]**
$V3\_HOT$	162
Demodulation stage	300
EAOUT Pin 3 *UC1825*	103

The transmitted AM-signal and the receiving signal including the clock can be seen in figure 4.11. From the specification of the transformer, the ratio was 1:1, which can visually be observed to be consistent. The *UC1901* internal clock (yellow) had a frequency of around 670 kHz and showed that the AM-pulses clock on the negative flank at the present probe configuration.

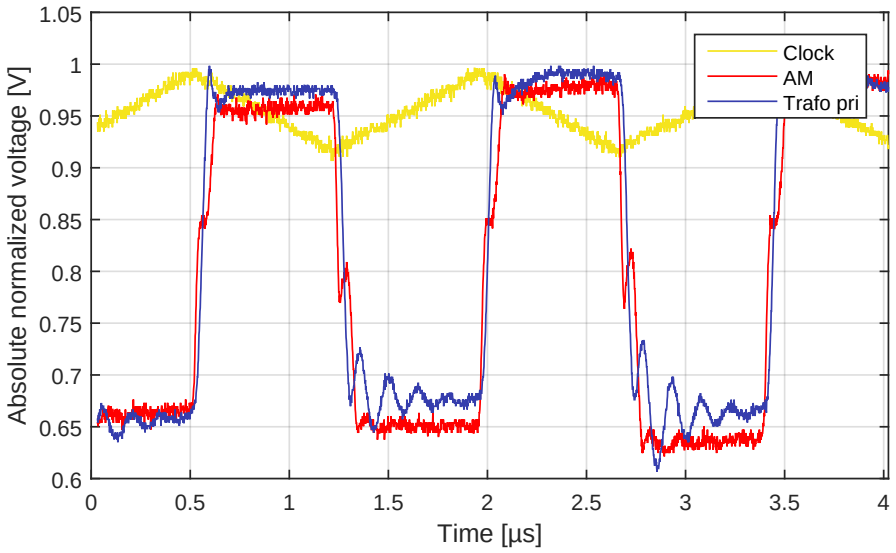


Figure 4.11: Feedback transformer signals from the secondary side (red) and primary side (dark blue), the *UC1901* internal clock represents by the yellow curve.

Reconstruction of an error signal from the secondary side can be seen in figure 4.12, where the demodulation is performed with a diode detector, i.e. diode-RC-circuit.

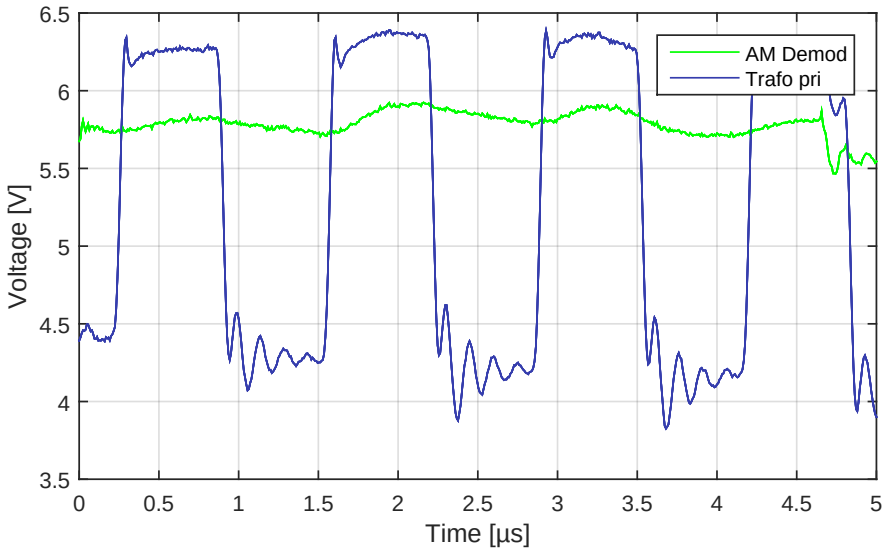


Figure 4.12: Reconstructed error signal (green) after diode rectification on primary side (dark blue).

4.3.1 Study of the Feedback *UC1901*

With the second setup some adjustment needed to be implemented in order to study only the feedback mechanism. In our case, it was a question of making sure that the PWM-circuit does not produce any gate pulses so no voltage is present on the secondary side. But also change the amplification of the compensation network (A.) into the internal amplifier of the *UC1901*, due to infinity gain at DC-voltage. Figure 4.13 shows the second case setup (no load present) where power supplies are used to power the $V3\_HOT$ and the $V5\_HOT\_UNREG$ to theirs voltage levels.

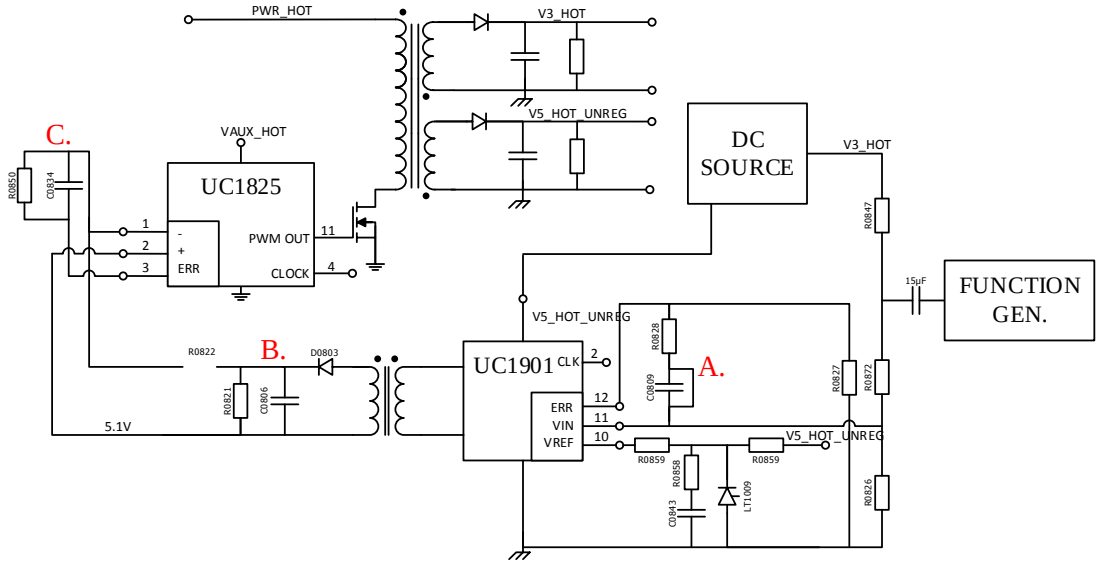


Figure 4.13: The second setup for studying of the feedback mechanism.

In order to investigate how the AM is applicable, a sinusoidal error signal was injected. The injected signal comes from a function generator and was connected between two resistors via a capacitor. There the resistors are used to scale down the voltage to a pre-decided voltage reference of 2.5 V. The 2.5 V reference is given by an IC-unit named *LT1009*.

The results of all above changes and some tuning of the $V3\_HOT$ voltage ended up in figure 4.14. The function generator parameters for the error signal (blue) were at 1 kHz and amplitude of $4\,\mathrm{mV_{pp}}$. The amplitude modulation shape (red) shows the variation of the amplitude and that the envelop curve resemble the injected signal. The demodulation signal (green) appearance distinctly comes from the input signal with a ripple formed by the discharge of the capacitor *C0806*.

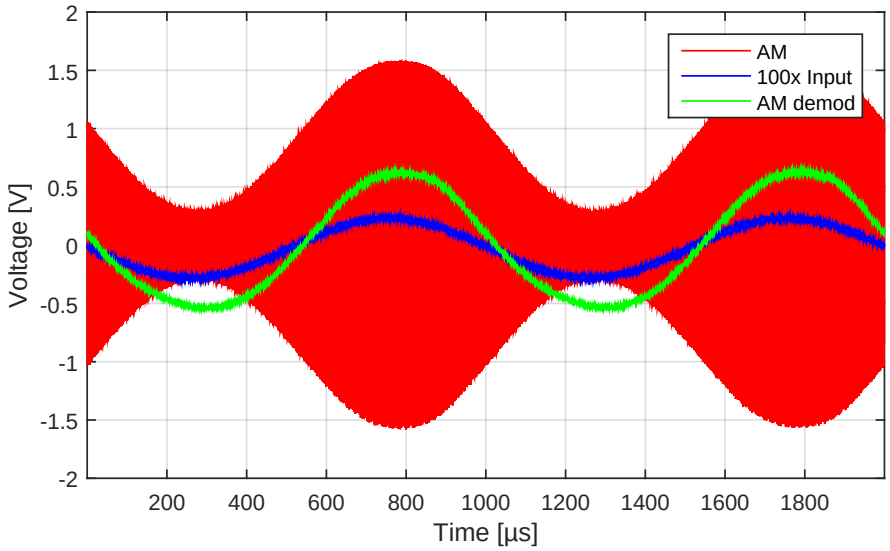


Figure 4.14: The reconstructed signal (green) on primary side, the input signal (blue) and AM-signal (red) from the second setup.

A dynamic range at the output (B.) was measured in the magnitude of $\pm 1.21\,\mathrm{V}$ at 600 Hz and decreased with higher frequency. Also the response time and rise/fall time of the open loop system were determined by applying a step function modulated with a pulse with long duty cycle. With a rise time of 21.3 μs and fall time of 94.8 μs were the result of a step of $4\,\mathrm{mV_{pp}}$. The response time resulted in 1.84 μs and with increased amplitude showed a longer time delay as well as longer fall time and faster rise time. This delay in time domain implies a phase shift in the frequency domain and is often constant and independent of the frequency. For example, a frequency of 1 kHz gives a period of 1 ms, which suggests a phase shift of 0.7°. With 10 kHz it should correspond to 7°. If this time constant would be dependent on the frequency that means with higher frequency, the more significant is the time response, i.e. larger phase shift.

Investigation of the frequency response was made on the second measurement setup with the feedback circuit only. This was done by using the function generator and make a sweep from 100 Hz to around 100 kHz. The frequency sweep was performed manually with arbitrary steps and the amplitude differences and the phase were noted down. The results were processed in Matlab and can be seen in figures 4.15 and 4.16 with the label “Data”.

The transfer function is based from the injected node (between the resistors) to the output on primary side (cathode of *D0803*). The result revealed at least one pole with a fall of $-31\,\mathrm{dB/decade}$. As the data was recorded manually with an oscilloscope, the resolution at higher frequencies where hard to distinguish from noise/ripple, especially the phase shift can be considered to be less reliable at higher frequencies.

As no capacitances where located in the transfer loop, there should not exist any decreased in amplitude or at least no large one. The reason was that the internal amplifier had a built-in dominate pole which is categorised by a gain bandwidth product of 1 MHz@0 dB and an open loop gain maximum of 60 dB. With a gain of nearly 36.7 dB and an internal 12 dB amplification inside the *UC1901* sums up to a total gain of 48.7 dB. This implies that the limited bandwidth

is set by the internal amplifier and gives approximately a cut-off frequency around 10 kHz, if 20 dB/decade is assumed for the error amplifier.

In figure 4.15, the cut-off frequency of 7.5 kHz to 8 kHz correspond to the measured data performed manually. In theory, one pole indicate a −20 dB/decade and the curve should follow the error amplifier, but as there is a larger decrease and as well the phase continue toward −180°. It indicates some kind of pole characteristics, even though there is no −40 dB/decade. From the figures there are mismatches as the phase goes to −180°, but no −40 dB/decade can be found in the magnitude plot. It might be that the error amplifier is not as ideal as assumed. What effect that causes this is unknown.

In order to get more reliable results, a network analyzer was used. The results confirmed the measured data with increased phase and the phenomena mentioned above. The measurements with the network analyzer were performed at different injection gains as can be seen in figures 4.15 and 4.16, i.e −20 dBm and −10 dBm respectively. In our case, the −20 dBm correspond with the manual calculated data as it had a magnitude of 48.7 dB.

The blue and green curves show measurements from the network analyzer at two different magnitudes. Also visible is a double pole (21 kHz) which shows −40 dB/decade for comparison. The measurement data measured manually is represented by the red curve. The orange curve shows the error amplifier *UC1901* assumed open loop appearance with the dominate pole.

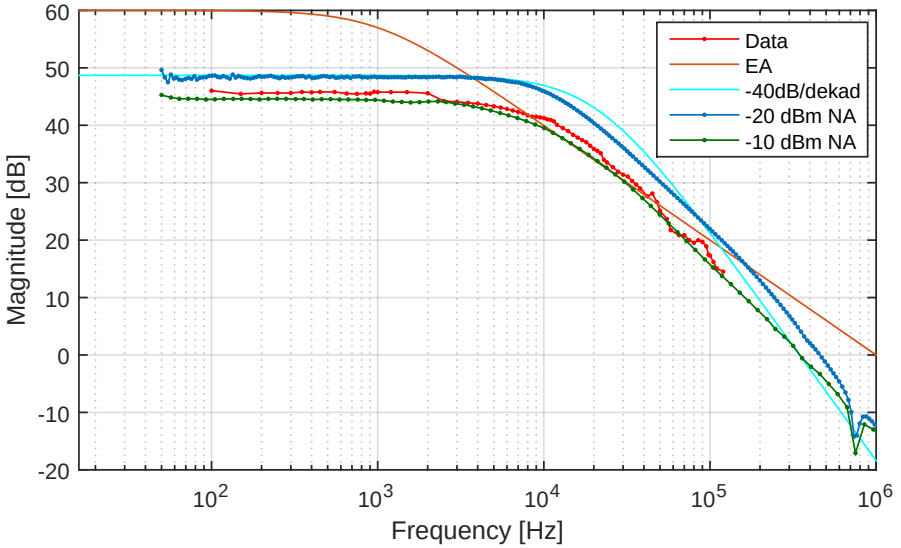


Figure 4.15: Bode plot of the magnitude measured from the injection input to the output (B.), including network analyzer measurement and error amplifier model.

The measured phase curve seems to follow the network analyzer and as well as the double pole (cyan) to an extent with exception for higher frequencies.

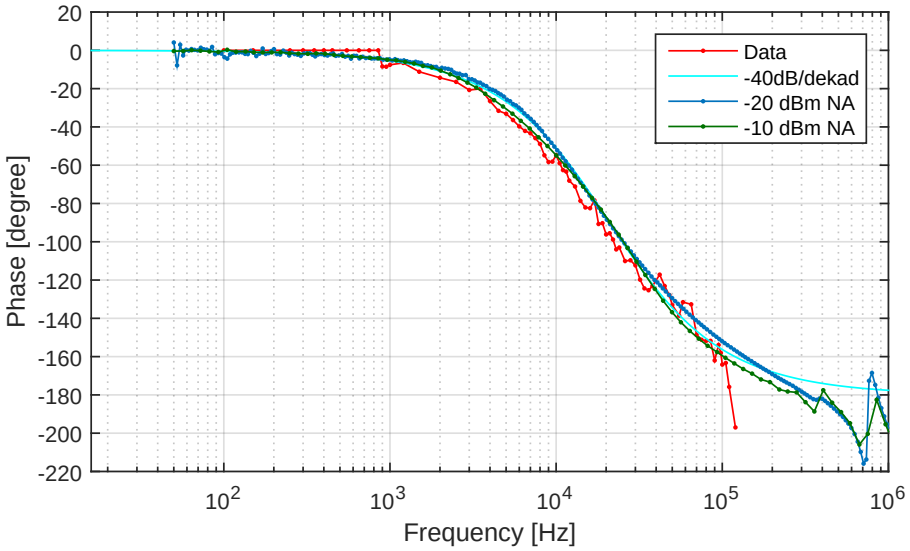


Figure 4.16: Bode plot of the phase measured from the injection input to the output (B.), including network analyzer measurement and error amplifier model.

4.4 Simulation of the Amplitude Modulation Feedback

To be able to compare potential new solutions and alternatives, a simulation model of the present solution is needed to be designed. The modelling program Cadence OrCAD PSpice was used, a well-known electronic simulation program. With base from the *UC1901* application note and data sheet, an AM-modulator has been build-up [21]. Besides that, an isolated barrier was implemented as well as a differential amplifier.

Note that the input to the internal differential amplifier in the *UC1901* was reversed in the simulation models, i.e. the signs positive and negative. The *UC1901* acts as an inverted differential amplifier compared to an ordinary differential amplifier with positive gain. This is not implemented in the simulation as it results in a more complex solution and does not contribute to its function. Therefore, this can be overseen as there is already a working component available, i.e. the *UC1901*. The same can be said for a negative supply voltage.

As demodulation detector, a diode detector was used as in the current model. An amplifier (*LM324*) was used to act as a differential amplifier, see figure 4.17. More detailed information about error amplifier is available in appendix C. The amplifier is constructed with a resistor network with $x4$ amplification. The input to the negative sign represents the voltage reference (Pin 10 at the *UC1901*) and input signal on positive sign (Pin 11 at the *UC1901*).

The AM-modulation circuit in figure 4.17 consists of a pair of BJTs ($Q16$ and $Q19$) connected to a square wave oscillator over an additional BJT ($Q15$) that sets the amplitude of the AM-signal. A bias voltage for the BJT $Q15$ is set by connecting another BJT in reversed to minimize the interference with the error signal. In the *UC1901*, a bias voltage is already present. The supply voltage feeds the Darlington connected BJTs and form the amplitude variation. The Darlington BJTs are used to increase the current amplification which only require a small base current compared with only one BJT, $I_C = \beta^2 I_B$. The resistors ($R4$ and $R5$) above the pair BJTs act as

an amplifier gain to the modulator output in relation to $R3$. The driver output BJTs are biased at 700 μA, which also set a requirement on the transformer. The transformer used here, has a transfer ratio of 1 with an inductance of 2x2.65 mH. Also a leakage inductance of 1 % has been added.

The secondary output circuit use a diode detector with the relationship of RC according to (4.7). The simulation outputs of this model can be seen in figure 4.18. Important to clarify is that the AM-signal does not use negative voltage as it can be assumed in figure 4.18, which is also valid for the *UC1901*. The model consists of an amplifier step, which resembles a class A amplifier. The amplifier uses current sources which have very low output resistance such that the voltage remains constant independent of the load. If an error is present, for example a sinus signal, the Darlington transistors will be biased at different base currents that will drag the supply voltage up and down and create a potential difference over the transformer. The output voltage over the transformer is a positive symmetric signal.

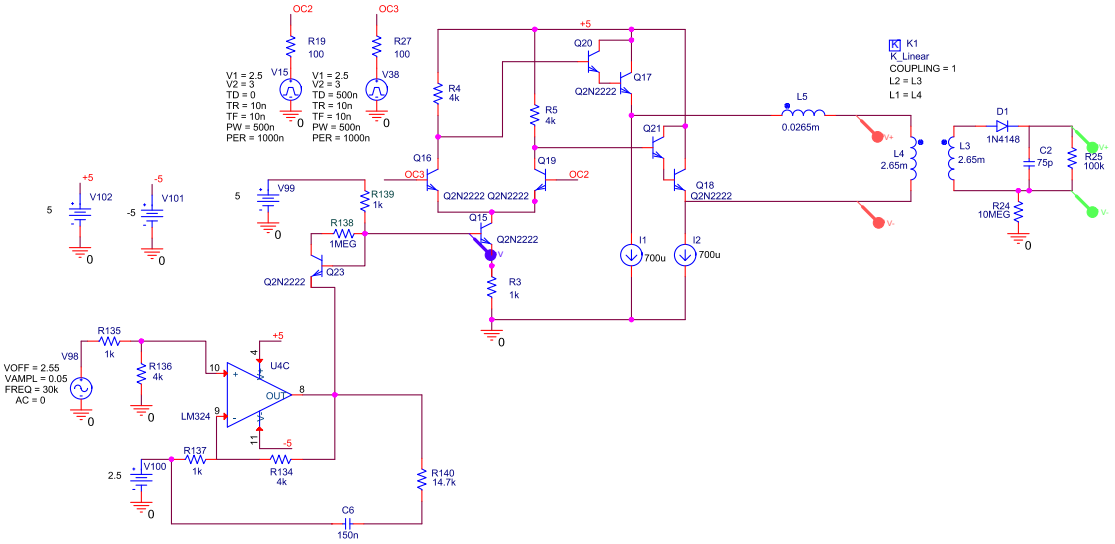


Figure 4.17: PSpice model of AM-modulation with an isolated transformer and a demodulation step.

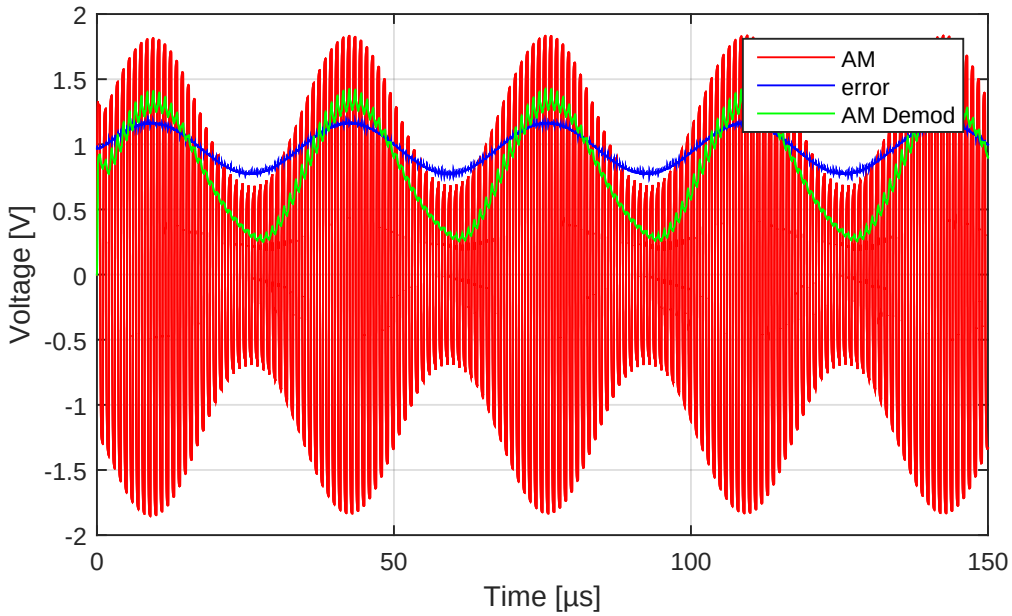


Figure 4.18: Simulation results from the PSpice model showing the operation of the AM-modulation.

5 Requirement for New Potential Feedback Solutions

RUAG Space has some component restrictions that shall be considered as guidelines in order to find new suitable candidates. Compared to the current solution with the isolated feedback circuit *UC1901*, a minimum use of filters are preferable as well as that the feedback output shall be compatible to the current PWM controller at the primary side (the *UC1825*).

For components ability to withstand and operate in space environment, certain requirements have been set. These conditions for space are available in a number of variations and here are the usual requirements presented.

For components selection, the manufactures offer three categories: commercial, radiation tolerant and radiation hardened. Commercial products are not tested for any radiation as the most are used on earth in common application without any radiation requirements. Their radiation performances are unknown. The next two definitions vary from manufacturer to manufacturer, however for radiation tolerant a level around 20-50 kRad(Si) and radiation hardened greater than 100 kRad(Si) is to be expected. Some may even use one definition for all levels and let the radiation test decide the tolerance. There are also classifications called MIL standards, military specifications, and they are often mention in context with components that require high reliability in special environments, such as space [2], [8].

A satellite life span lies in the order of 15 years and that is the span which the electrical product shall be reliable and still be operational. During this time all components are exposed for radiation, TID and SEE. For space products, it is preferable to withstand TID above 100 kRad and SEE above 60 MeV [8].

Depending where the products are located in the satellite, the temperature will vary with the time. Inside satellites, the temperature can be regulated to an extent in order to achieve high operation performance of the electronics. Usually during launching and before placed in orbit, the main components in the satellite are turned-OFF and waiting to be started when entering orbit. At start-up, the electronics shall manage to start at $-40\,^{\circ}\mathrm{C}$, not necessary have the optimal performance, but be able to work.

The most preferred area to place electronics are as near the centre as possible in satellites for radiation protection and temperature conditions. That is generally not the case, for example antennas, where the microwave electronics need to be placed on the edge. The maximum limit that has been set for operation of the electrical components inside the satellite are a surface temperature of 85° [8].

There are certain operation (junction) temperature qualifications for different applications. The most common classifications can be seen in table 5.1, where the highest range is preferable [22].

Table 5.1: Junction temperature qualifications.

Application	**Temperature Range**
Commercial	$0\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$
Industrial	$-40\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$
Extended Industrial	$-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$
Military	$-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$

5.1 Special Requirements

A list of important parameters are presented in table 5.2 and shall act as a guideline for research for new components/solutions. The highest quality level is radiation hardened components, which is desirable for new solutions.

Table 5.2: Parameters that shall act as guidelines for research after new solutions.

Requirement	**Value**	**Unit**
Bandwidth	100	kHz
TID	100	kRad
Temperature (junction)	-40 to 125	°C
Life span	15	years
Response time	<8	μs
Power consumption	low	W
Supply voltage (VDD)	3+	V
SEE	60	MeV

Besides technical requirements there are also some component functionalities that are preferable for new solutions.

- Minimum use of filter.
- The feedback output should be adjusted to the *UC1825*.
- Handle start-ups without to many fixes.
- Simple to implement on existing PCB.
- Size restriction (circuit board).
- Minimum use of additional components.
- Reasonable costs.

5.2 Transmission Options

There exist a number of opportunities to transfer a signal, but for our concept and practice, there are three configurations that can be considered to transfer feedback signals. The present solution with the *UC1901* use a built-in error amplifier which transfers the error signal to the primary side and into the PWM controller unit. The following concepts are the ones that are suitable for the feedback transfer:

- Transfer the error signal from the secondary side as present solution.
- Transfer the actual value from the secondary side and generate the error signal on the primary side.
- Place the PWM controller at the secondary side and transfer the gate signal to the primary side.

The first alternative requires a differential amplifier and is necessary if there is no built-in as it is in the *UC1901*. The second option is similar but the actual value is transferred to the primary side directly and then make the necessary operations at the primary side. The advantage with

the error signal configuration is that higher accuracy can be achieved. With galvanically transfer of the actual value (a couple of volts), the receiver side is highly affected by a voltage drop such as when using a diode as it influence on the input to an EA, while the amplified error signal is perhaps ten times larger and a voltage drop over a diode is neglectable.

If digital conversion is applied for transmitting the signal over an isolated barrier, then the tolerance levels will be much better if the error is transferred compared to the actual value, as higher resolution can be achieved with a lower voltage range.

The last option is to make all necessary operations on the secondary side and transfer the gate pulses to the transistor at the primary side. This solution will require an extra start-up DC/DC converter on the primary side to start as no voltage is present at the secondary side.

5.3 Transfer Signals in Different Mediums

Galvanic isolation methods are used to transmit signals over a barrier without any physical contact between the sides and are sometime essential for the application. Providing electrical separation from two grounds can be achieved in a lot of ways, each solution having different properties. Here, the most common electrical isolation techniques are presented for transfer of feedback signals in different mediums.

5.3.1 Transformer Feedback

A common way of transfer feedback signals in space is over a transformer. It is based on magnetic field coupling between two or more windings that share the same medium as core. The transferred signal current generates a magnetic field in the first winding that is linked to the second winding through a core medium which induces a current in the second winding and thereby creating an isolated barrier. The main drawback with transformers is that DC-signals must be modulated into an AC-signal. This can be done for example as amplitude modulation (AM) or pulse width modulation (PWM).

As previously mention, AM uses a fix frequency and duty cycle as carrier signal which is multiplied with the input signal into different amplitudes. The PWM working principle is similar to AM, but is correlated with the pulse width instead of the amplitude to the input signal. A clear advantage with a good design of the transformer is that the transferred signal energy can almost resemble an ideal component. Also EMI (electromagnetic interference) can cause problems for the feedback signals and it needs to be considered when placing the component. An illustration of an isolated transformer feedback can be seen in figure 5.1 [23].

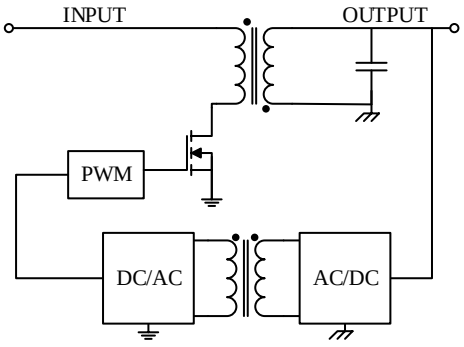


Figure 5.1: Isolated transformer feedback.

5.3.2 Capacitive Feedback

Capacitive coupling uses electrostatic in terms of an electric field to transmit signals over a barrier. It consists of capacitors that act as isolated barriers with a dialectic medium in between the two groundings. The input signal can be modulated for example with PWM or voltage-to-frequency modulation if the frequency is too low. The output circuit demodulates and filters the signal back to an analog signal if a modulation technique is used. A schematic model of a galvanically isolated capacitive coupling can be seen in figure 5.2.

For insulation purpose often two capacitors are used to convert a single signal into differential mode. This makes the signal more resistant to common mode transients since a single capacitor is missing the differential mode compared to an inductor. At the receiver, the differential signals are converted back to its original signal by comparator circuits and additional components. For a wide bandwidth of frequencies, the capacitors can be divided into a DC-channel and an AC-channel. The expression DC-channel is referred to low frequencies. As low frequencies would require large capacitors, they are instead process with a modulation step, for example PWM, which modulates a low frequency signal to a high carrier frequency [23].

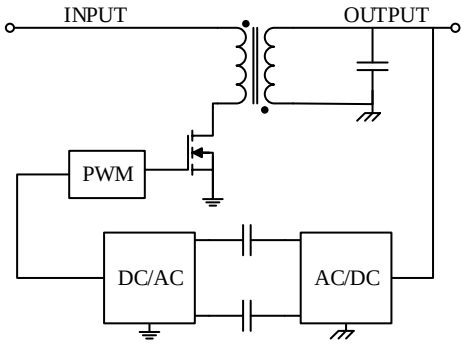


Figure 5.2: Isolated capacitive feedback with two capacitor.

5.3.3 Optocoupler Feedback

A feedback path by using an optical coupling to transfer signals over a gap in terms of light. They are called optocouplers and are commonly used in the commercial sectors. The isolation consists mainly of a Light Emitting Diode (LED) as transmitter and a phototransistor as receiver with a medium in between, for example air, see figure 5.3. The LED driver circuit senses the input analog signal (can be both AC and DC) and converts it into a pulse signal that in turn drives a current through the LED. The emitting light is received by the phototransistor which generates a current that is used to reconstruct the signal into a voltage.

There exists a linear relationship between the current on each side of the barrier, referred as Current Transfer Ratio (CTR) and is defined as CTR= I_C/I_D. It can operate in space as well as on earth, but due to exposure of radiation, the phototransistor and LED degrade with time. The main cause of degradation is displacement damage that is introduced by SEE and TID, but also darkening of LED coating, which limits the transmitting light. Other drawbacks that also are present on earth are that CTR is temperature and ageing dependent, which would influence the transmitted signal. The advantages are that magnetic– and electrostatic field influences are minimized on the feedback signal and DC-signals are possible to send compared to transformers that require AC-signals [23].

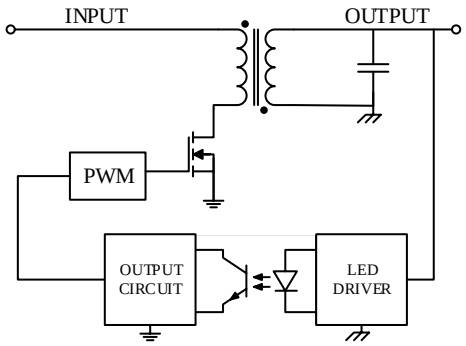


Figure 5.3: An isolated optocoupler feedback representation with a LED and a phototransistor.

5.3.4 Radio Frequency Feedback

Radio Frequencies (RF) are used more in far field operation as ground communication to satellites. Near field operation is one possibility of isolated feedback, see figure 5.4. Due to other RFs in the vicinity, one needs to be aware of reflection and interference with other signals. But as the isolating distance is in the range of millimetres, it might be possible to screen away unwanted external signals. Other advantages are that the error signal can be modulated with high frequencies and that it is total electrical isolated system. A drawback might be complexity with more digital circuits.

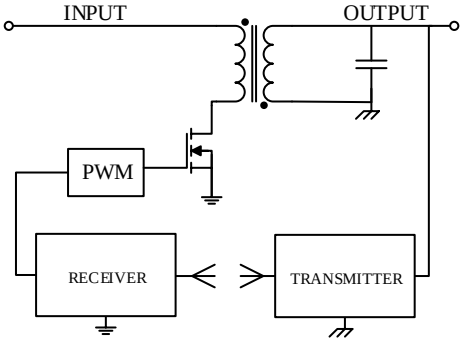


Figure 5.4: Isolated RF feedback.

5.3.5 Other Feedback Alternatives

Thermal sensing is another alternative, but it requires stable operation temperatures in order to have high precision. In space, temperature can be a largely variable factor dependent on where it is located and may not be so easily controlled. Therefore it is not the most suitable alternative for space applications.

There is an acoustic transformer available on the market for isolated transfer. It uses a kind of piezoelectric material to convert electrical signals to acoustic and vice versa. By replacing the traditional coils against a non-conducting piezoceramic core and an acoustic wave transmitter, an acoustic transformer is created [24]. Although it is an isolated coupling, the alternative is not

feasible to use in space satellites as vacuum occur. No acoustic wave can travel in vacuum as there is no medium (molecules) to send pressure waves in. Also that the feedback signal would be probably highly affected by vibrations that occur during launches.

Visual feedback in the form of image processing with a camera and some kind of visual effect (example LED-bars) can be possible to send information over a barrier, but the response time is probably a disadvantage.

6 Alternatives for Galvanically Isolated Feedback

6.1 Case Setup

The main part of this thesis is to find better solutions to transfer galvanically isolated signals. At start, research for technologies in both commercial – and radiation hardened (Rad Hard) components through manufactures, patents, published documents will take place. Next step is to find possible alternatives and then go further into details to see if the technologies are plausible and make a first elimination of the alternatives. Second step is to concentrate and extend the research for the most suitable technologies and find components that are available today. During the research, simulations will be made for the possible alternatives to verify theirs function. If the findings look promising and work in the simulations, a construction of a circuit board is planned to take place with the selected alternatives.

The theoretical study of the space environment and its influence on components, section 2 and section 3, contributes to the basic knowledge in terms and understanding of the space sector and will be used to evaluate new alternatives.

6.2 Research Results

The literature search using various sources such as IEEE, patents and others sources resulted unfortunately in no direct attractive concepts compared to what the manufactures had to offer. The manufactures might use information from these sources to create theirs solutions, but the main approaches presented here are based on the manufactures information.

After an initial research, a general setup of the feedback alternatives has been created based on the findings. It can be seen in figure 6.1 and consists from the secondary side of an amplifier, a modulation step, a galvanic isolated step, a demodulation step and output filter. Each step in this general setup can be model in several configurations. The steps can be broken down into the following points:

Amplifier:

- With a differential amplifier, the error value can be extracted and act as the input signal to the modulator.
- Without amplifier, the actual value act as the input signal to the modulator.

Modulator:

- PWM modulation, apply pulse width modulation to the input signal.
- AM-modulation, apply the amplitude modulation to the input signal.
- Frequency modulation, use different frequencies to modulate the input signal.
- $\Delta\Sigma$-modulation, apply analog-to-digital conversion to the input signal.

Isolation step:

- Transformer, transmit information through magnetic field.
- Capacitive, transmit information through electrical field.
- RF, transmit information through EM-waves.

Demodulation step (output filter):

- Depending on the modulation and state (digital or analog) some kind of x-order filter is required to reconstruct the input signal.

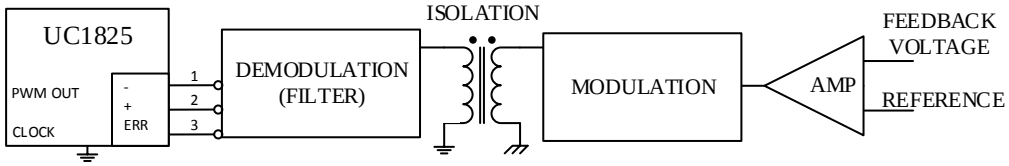


Figure 6.1: A general setup of a feedback with different stages.

An example could be if the amplifier is removed so that the actual value is the input signal. The modulation step can be PWM modulation, a capacitive barrier as isolation and demodulation with an analog filter.

The component market showed that most isolated feedback components use some kind of modulator and the signals are transmitted mainly through a transformer– or a capacitive barrier. There are both analog isolators as well as digital isolators available. With that in mind, the question arises, in which type of state is the most suitable. The advantages with analog isolators are that no ADC/DAC is needed and that can save both space and supplementary components. With digital signal, digital filters (with infinite poles) can be used that have the advantage to give higher bandwidth of the system compared to an analog filter. Also processing techniques can be used to improve the output signal.

6.2.1 Alternative Feedback Methods Compared to the Present Feedback

The advantages and drawbacks with each step can be evaluated in detail, but we will concentrate on the advantages and drawbacks compared with the present solution with the *UC1901*.

The first step deals with which type of input signal that is the most suitable to transfer to the primary side, the real value or the error signal. The real value amplitude lies at a couple of volts compared to the error signal in millivolts range. As higher accuracy can be achieved for the error signal compared to the actual value, as stated in section 5.2, it has more potential. Also if the signal is converted to a digital signal, the resolution set by the ADC/DAC will be better with the error signal.

With the findings as reference, a $\Delta\Sigma$-modulation ADC will be able to operate at a higher frequency, but might introduce unwanted frequencies in the system. Also higher frequency gives lower voltage ripple at the receiver output and smaller filter can be used to minimize components which were desired in section 5.1.

$\Delta\Sigma$-modulation is based on clock pulses and accuracy (x-bits) to convert the input signal to the right state. A property of this modulation technique is that the output signal acts as an average function over many samples and thereby achieves a high accuracy. The active clock needs to be relatively accurate to record the right input level, but with tiny clock variations, the output level will differ but probably correct itself in time. More details about $\Delta\Sigma$-modulation is available in section 9, where it is specified to our purpose of use.

For AM-modulation, clock accuracy is not required as the information in the signal is stored in the voltage amplitude of the modulation. For PWM, the clock pulse needs to be accurate and not drift in order to get the correct pulse width.

RF use a carrier wave that is modulated with a signal through either AM or frequency modulation. This solution can be complex as it must send information bit per bit and then demodulate it back to an analog signal. Example, if two bits per period is transmitted with a frequency of 1 MHz, this correspond to a data rate of 2 Mbps.

A transformer has a total electric galvanic isolation compared to a capacitive isolation. Both the capacitive and the transformer isolation are sensitive to EMI and not directly influenced by radiation. For large capacitors, charge accumulation has a minimal effect. Both types can be used for high bandwidth transfer. The transformer might be less susceptible to Common-Mode Transient Immunity (CMTI) than a capacitive barrier since no normal differential mode is present, as stated in [25].

RF uses EM-signals as isolation between two sides and interference with other radio signals can be an issue. If the component itself is compactly packaged, interference from the surroundings can be avoided to an extent.

For demodulation of the modulated signal, a suitable filter is needed to recover the signal. Digital filters have the advantage of increasing the bandwidth at the cut-off frequency and eliminate unwanted frequencies compared to analog filters. However, analog filters are simpler to implement and effective to an extent while digital filters are more complex, require power, clock signal, FPGA etc. Figure 6.2 represents the difference between an analog– and a digital filter.

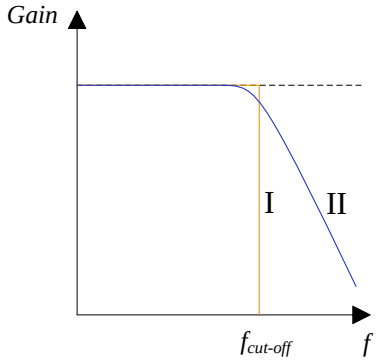


Figure 6.2: The different between an analog filter (II) and a digital filter (I).

6.2.2 New Components from the Research

The collected information of new solutions ended mainly in commercial products, but also some space compatible products. A $\Delta\Sigma$-modulation product named *AD7403* from Analog Devices suits our first view of inspection and can be a possible alternative. Unfortunately, it is classified as a normal commercial component. A dialogue was established with the AeroSpace group of Analog Devices to check if there was a qualified space variant component available. The response was that no radiation test data was available, but based on data from other similar devices they assumed a tolerance of SEE in the range of 10 MeV to 15 MeV, where most space level applications require a minimum of 40 MeV but 60 MeV is preferable.

Besides the information on *AD7403* another component was recommended, *ADUM7442S* (released Jan 2016). This is a 4-channel digital isolator with transformer as isolation. It transfers data rates up to 25 Mpbs and had a supply voltage of 3 V to 5.5 V. Temperature qualified to over the

military temperature range and with a guaranteed radiation performance up to 50 kRad.

As the *ADUM7442S* is a digital device, it will require an ADC to convert the input signal. The output will also then need to be digitally filtered through for example a FPGA or an ASIC component. This enforced additional components in comparison with the present solution and will also increase the cost for the feedback loop. The principle is clear and that this will probably function very well and be very accurate compared to the *UC1901* since radiation tolerant DACs and FPGAs are accessible. Although, the price is a limitation and a question is if such high accuracy is needed. This alternative is rejected due to complexity, space on the circuit board but mainly for the expensive cost of additional components (FPGA), see section 11.4.

A related product (digital isolator) was found from the manufacturer TI that is HiRel (High-Reliability) which can withstand an extreme environment. The *ISO721M-EP* uses a capacitive isolation barrier [26]. No radiation tests were found for this device and no request was made to TI for confirmation as the digital isolator was rejected. The same from Silicon Labs *Si88x4x*, a commercial product [27].

From TI, the commercial component *AMC1305x* could be a possible replacement [28]. It is based on $\Delta\Sigma$-modulation with a capacitive isolation barrier with a built-in DAC. It operates at frequency up to 20 MHz and has an extended industrial temperature range. Contact with the Swedish TI-group was established, but no further information was received. Therefore the assumption that there was no radiation tolerant product available as no other compact packaged $\Delta\Sigma$ radiation components has been found so far.

Searching for RF solutions in a compact package turned out to be unavailable in such context. An alternative is to use a transmitter and a receiver separately, but that makes it more vulnerable to interfere as the isolation distance is larger and it would also increase the space needed on the board. A possible variant could be to use equal transceivers.

Optical products are ruled out due to the lack of radiation tolerance and accuracy and thereby not suitable as feedback for space. RF circuit could be a good investment, but is for now not available as a compact component for use as low power feedback.

The two commercial components *ADuM4190* and *AMC1200* were some of all that not suited the performance as well as radiation requirements. But these two had on the other hand the function that was desired, an isolated error amplifier. The first one used a transformer barrier and the other a capacitive barrier.

The possible concepts that passed the first review were some sort of digital delta sigma modulation. No specified component, only the modulation step. The isolation barrier is considered to be a transformer barrier rather than a capacitive barrier due to better CMRR/CMTI and radiation tolerance. RF barrier is still a valid option and has potential, but due to a lack of components that suits our purpose, it is ruled out. It can be built with discrete components as well, but this will not be evaluated.

6.3 Review of Research Results

From the previous mentioned information and findings. As no new concept guaranteed a radiation tolerant component, except a case where the cost was not reasonable. The focus tended to make improvements of the present solution with an evaluation of the $\Delta\Sigma$ modulation step. The new alternatives have been selected in collaboration with RUAG Space staff. Besides the research, an additional alternative (a load alternative) was found. The alternatives that found to be of interest and will be investigated closer are:

- Original state (internal clock) (asynchronous)
- Clock pulse from the *UC1825* as input to external clock of the *UC1901* (synchronous).
- Gate driver as clock from the *UC1825* as input to external clock of the *UC1901* (synchronous).
- Use the secondary side as a load without the *UC1901* (synchronous).
- $\Delta\Sigma$-modulation alternative (asynchronous).

Although there were no direct radiation tolerant products found for $\Delta\Sigma$ method, a simulation will be made on the concept for future studies as the most commercial products will in time come as a space compatible product.

The new way of improving the feedback circuit with the *UC1901* has emerged by replacing its internal clock that is around 700 kHz with an external clock signal. This in two combinations: one is to use the gate pulses from the *UC1825* driver output or its internal clock directly. These solutions will work synchronously compared to the current model, explanation of the synchronous– and the asynchronous operation mode is found in the text further down.

The advantage with these solutions are that the compensation network likely can be reduced on the *UC1825* to a proportional regulator (or very little capacitance), thereby remove a pole and improve the performance of the system. As the ripple output will increase with lower frequencies, an extra winding has been added to the primary output. As the AM-signal is positive symmetric, a decrease of a factor around seven in ripple was achieved with an extra winding. The factor was determine at a certain operation point with synchronous alternative presented in section 8.1, but it is naturally dependent of the value of the demodulation filter capacitor.

The alternative of using the secondary side as a load, the *UC1901* will be replaced with an error amplifier and an additional winding will be placed on the primary side that will oscillate at a fixed duty cycle. The receiver winding will recover a voltage which will vary dependent on the error located on the secondary side and act as a load.

Mixed frequencies will appear in the system as a side effect from the primary side switching as well as the feedback switching and are one of the reasons that synchronous mode will be used to avoid such phenomenon and thereby minimize filtering.

Synchronous mode and asynchronous mode are referred as the switching relation between the clock frequency from the *UC1825* and the feedback clock frequency. Today's solution is asynchronous, 340 kHz gate frequency and circa 700 kHz feedback frequency. The benefit with a high modulation frequency in the feedback loop is that the transmitted error signal can be reconstructed with low voltage ripple. By having two dominating frequencies in the system, mixed frequencies of the two will occur, side bands and harmonics. This requires high filtering to get rid of unwanted signals as it has been done today, which limit the performance of the DC/DC converter. In theory with synchronous mode, no extra frequencies should be produced and hence no interference with the signal. This will hopefully minimize the need of filtering and thereby make the system more stable and possibilities of improving the bandwidth.

A win with synchronous mode is that the maximum error will be in sync with the on-switching of the PWM signal, which results in the largest error will be transferred in the feedback path. The cost will be the output ripple on the primary side that will be larger than with higher sample frequency. The information below the maximum error will be unseen and not necessary as the maximum error will be integrated away.

In sections 8 and 9 are the alternatives described more in detail and simulation profiles are shown for each model.

7 Design of the New Alternatives

To establish a working system of each alternative, considerations to the surrounding electronics need be included. Discussed in this following sections are important design parameters, a short introduction how to design a transformer and details of the error amplifier at the *UC1825*.

7.1 Initial Parameters for the New Designs

At the primary side, the voltage $VAUX\_HOT$ acts partly as the supply voltage to the PWM-circuit *UC1825*. Almost instantly during start-up, the voltage $VAUX\_HOT$ is present and makes the *UC1825* use a soft starter in the form of P-regulation to send PWM pulses to the secondary side, while the *UC1901* has not gain enough supply voltage to start.

The use of an external clock for synchronization from the primary side will be provided over a separate transformer and will be available almost at instant when the *UC1825* start. This concludes that synchronization is possible for the different solutions and it takes no major time delay for the clock signal to reach the secondary side. For example, the clock signal would go to Pin 2 at the *UC1901*.

New transformers need to be designed for several factors: frequencies, number of turns, core material, current etc. For example, the lower frequency, the larger transformer is required under the circumstance that the same core material is used. Lower switching frequencies result in an increase of magnetic flux/current, i.e. $I \sim \phi \sim 1/f$, see section 7.2. This implies that saturation can occur at lower frequencies.

The output voltage ripple that arise at the reconstruction (B.) of the transferred signal from secondary side can for AM be improved with cost of space (not necessary, but often) with an additional winding at the output that uses the negative complimentary pulses rather than just the positive pulses as in the current design. This can almost be seen as a requirement to gain the ripple in an acceptable level for lower frequencies, i.e. synchronous mode. The ripple is also dependent on the filter capacitance and can be lowered with increased capacitance. Larger capacitance also leads to that the pole becomes more significant and may impact on the system. The current model use high frequency which lower the discharge time of the capacitor in the demodulation step and thereby achieve lower ripple without the extra winding.

The following table 7.1 summarises important factors that need to be considered.

Table 7.1: Present different factors that shall act as advice for the design of the coming alternatives.

Parameter	**Min**	**Max**	**Notes**
The *UC1901* operation voltage.	4.5 V	40 V	When the secondary voltage $V5\_HOT\_UNREG$ reaches the minimum supply value of around 4.5 V, the *UC1901* start to operate. Its internal clock start with the *UC1901* and will take over the regulation from the *UC1825*.
Current limitation for the *UC1901*.	-	700 μA	Another perspective are components connected to the transformers. They may have certain limitation as for the *UC1901* which has a current limitation of 700 μA. Exceeding this limit leads to saturation.
EA dynamic range of the *UC1825*.	1 V	5.1 V	The reconstruction step of the signal set the maximum allowed ripple and is directly connected to the internal amplifier of the *UC1825* DC-gain. If too high voltage ripple occurs with combination of a high DC-gain, it might saturate the amplifier as the error can only be located in the dynamic range.
Differential error Pin 3 *UC1825*.	0 V	3.3 V	A protection will be enable and shut down the converter if the maximum value is reached.
$VAUX\_HOT$.	10 V	15 V	Primary supply voltage to the *UC1825* and is available to supply additional components.
$V5\_HOT\_UNREG$.	-	5.5 V	Secondary voltage which can be used to supply additional components.
$V3\_HOT$.	-	3.7 V	Secondary voltage used as feedback. A protection is enabled at voltage higher than 3.7 V.
CT Pin 6 *UC1825*.	0.7 V	3 V	The minimum and maximum voltage level the clock signal can obtain under operation.
Circuit board space.	-	-	Space on the circuit board is a limited parameter and can be the factor that rule out certain alternatives.
Feedback alternatives.	-	-	The alternatives shall be adjusted to the existing DC/DC converter such that only the feedback circuit can be replaced.

A quick overview of the new alternative compared to the present solution with the *UC1901* is shown in table 7.2. Also credible assumptions are included.

Table 7.2: A comparison of the alternatives compared to the present solution.

	Clock design with the *UC1901*/ Gate driver as clock	**$\Delta\Sigma$ design**	**Load design**
Main transformer	Redesign	Redesign	Redesign
Total space (board)	Larger	Larger	Larger
Filter use	Less	-	Less
Type	Syn.	Asyn.	Syn.
Start-up	Same	-	Fair
Additional components	Yes	Yes	Yes
Complexity	Fair	High	Fair
Accuracy error transfer	High	-	Fair
Extra transformer	Yes	No	No
Implementation	Fair	High	Fair

These parameters in table 7.3 will be one of the key quantities that will be evaluated for the new alternatives.

Table 7.3: Quantities that will be evaluated for the new alternatives.

Dynamic range (reconstruction stage)
Voltage ripple
Bandwidth (complete system)
Phase margin (complete system)
Power consumption
Costs

7.2 Transformer Calculations and Transformer Designs for the New Alternatives

The key component in all solutions is the transformer. An assumption that this component is just to pick and place is a misconception, instead it will require carefully thought through. A signal transformer differs from a normal used in converters and high voltage transformers, such as low current and low power.

A transformer consists of two or more coupled windings with a certain number of turns which set the transfer ratio. Normally, a core medium is used to enhance the linked magnetic flux in respective winding. This is usually applied, as air/vacuum has low permeability, which states that higher current is needed to send the same information over the transformer compared with one with a core material. The type of material used in the core sets both temperature restriction as well as the magnetic properties as permeability.

The absolute permeability is defined as $\mu = \mu_r \mu_0$, where $\mu_0 = 4\pi \times 10^{-7}$ H/m. But in core data sheets, the effective permeability is often detonated rather than the relative permeability (μ_r), due to geometry of the core. The effective μ_e is the combination of a closed core (two pieces) with air-gaps included and gives a more accurate permeability when designing transformers.

The effect of air-gap is illustrated in figure 7.1, where B is the magnetic field in Tesla and H is the magnetic field strength in ampere per meter. With air-gaps, the B-H curve saturation occurs at a

later stage compared with the one without. Different magnetization materials and compositions create different hysteresis loop with varied width in the B-H curve and thereby introduces core losses. With a magnetic field applied, magnetic alignment occurs inside the material. They are called domains and will start to orientate in the same direction as the supplied field. The B_{sat} symbolize that all domains are orientated in the same direction. These domains act like a memory and hold the magnetization even when the field is removed. To change the orientation, an opposite field is required and due to the magnetic strength, material etc, the reorientation will have a slower decrease, i.e. hysteresis is the result [29].

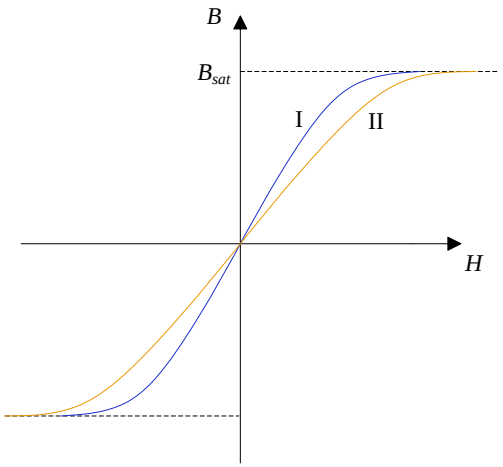


Figure 7.1: The B-H curve of a core medium with (II) and without air-gap (I) with very narrow hysteresis.

There are a lot of different materials and combinations available that have different magnetic properties. The current feedback use a core material called *3C94* and a core model *E14/3.5/5*. A potential core material has already been chosen to *3E6* due to its good temperature range (up to 150°) and high permeability [29]. The *3E6* has a saturation limit of magnetic field (B) of around 380 mT, which says that no more energy can be stored above that limit. The core model *E14* is used for the feedback transfer at RUAG Space which is the smallest core for planar transformers and next size is *E18*. Two E-model pieces are used in combination to create a closed path for the flux. The *3E6* consists of compressed powder of the material which lower leakage currents.

Each core model has given data as effective cross-section area A_e, effective magnetic path length l_e, A_L-value, core dimensions, effective permeability etc. In data sheets, A_L-values are typically given instead of defining the air-gap length to simplify calculations for the designer. A_L-value is a conversion factor for each specific material and is used to calculate inductances with given number of turns N. The unit for A_L is denoted in nH/1000 turns and is defined as

$$A_L = \frac{\mu_0 \mu_e A_e}{l_e} \tag{7.1}$$

and then the inductance can be expressed as

$$L = A_L N^2 \tag{7.2}$$

with the unit in mH. For the *3E6* material with an *E14* model, the A_L-value is 6400 nH/1000 turns with an effective permeability (μ_e) of 5900. Similar for the *3C94* has an A_L-value of 1500 nH/1000 turns [29].

To design a transformer, certain parameters need to be defined. First the number of turns is determined as it is a question of available space. Planar transformers are used in our design, which limit the number of turns per layer. The use of planar transformers is to integrate a component in the circuit board and that contribute several other factors like mechanical robustness etc. But normal discrete transformers are possible to use as well.

Increased number of turns results in more inductance with the cost of decreased saturation current. For signal transformers, current in mA range or lower is desirable as no high power is needed to transfer signals. From Gauss law, we can express the magnetic flux through a closed surface with a magnetic field as

$$\phi = \oint B\, dA = BA_e \tag{7.3}$$

and combine it with the inductance relationship, expressed as

$$L = \frac{N\phi}{I} = \frac{NBA_e}{I} \tag{7.4}$$

which results with (7.2) in

$$I_{sat} = \frac{B_{sat}A_e}{NA_L}, \tag{7.5}$$

where B_{sat} is the magnetic field saturation and I_{sat} is the saturation current.

With all parameters known, the saturation current can be calculated and as well as the inductance from (7.2). Additionally to the parameters above, the size of the transformer is related to the operation frequency. By applying ohms law, the current can be expressed as

$$I_{L,peak} = \frac{V_{L,peak}}{2\pi fL}, \tag{7.6}$$

where $V_{L,peak}$ is the voltage over the inductor L. As (7.6) is inversely proportional to the frequency, the saturation current I_{sat} tends to be reached with lower frequency.

For design purposes, a calculation model in excel has been used for a specified planar core, see appendix B. The calculations are based on the above equations and give the designer the inductance, maximum current, power losses etc. The input parameters are the materiel (A_L-value), magnetic field saturation, turns and dimension of the core. Usually, parameters are selected with a margin to avoid unforeseen events, for example the magnetic field saturation is set to $0.6B_{sat}$ and $0.7A_L$.

Table 7.4 presents the transformer designs in the simulation models in sections 8 and 9 with specified details, which was obtained from the excel document.

Table 7.4: The transformer designs of the coming feedback alternatives.

Transformer	**Turns N**	**L [mH]**	**Material/Core**	I_{sat} **[mA]**	**Sim** $I_{L,peak}$ **[mA]**
Clock transfer	42:42	2.65:2.65	3C94/E14	70:70	3:3
AM synchronous	38:28:28	6.47:3.51:3.51	3E6/E14	20:20:20	0.8:1.4:1.4
Load model (sec:prim:out)	33:22:33	4.88:2.17:4.88	3E6/E14	20:30:20	7.5:6.8:5.5
Delta sigma	42:18	7.9:1.45	3E6/E14	20:40	5:10

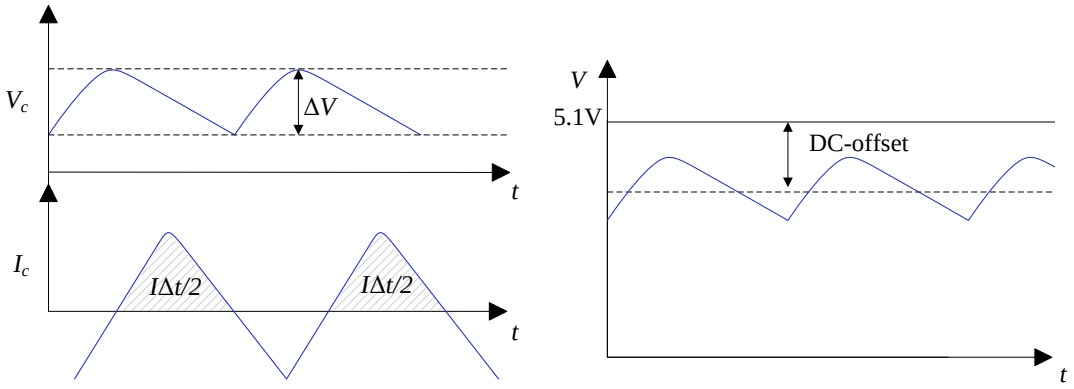
From section 7.1, a limitation of the *UC1901* current was 700 μA, but is higher in table 7.4. This was caused by oscillation in the simulation and is probably due to resonance related to usage of large BJT models in the Darlington couplings. In reality, the BJTs are much smaller than the ones in the simulation and can be neglected for now.

7.3 Error Amplifier at the PWM-circuit

From previous mentioned information, the *UC1825* had a limited dynamic range for the error signal. This will need to be correlated with the magnitude of the ripple that enters the error amplifier. The ripple is set by the filter capacitance in the demodulation step and is defined as

$$C = \frac{I_c \Delta t}{2\Delta V}, \tag{7.7}$$

where $I_c \Delta t/2$ is the capacitance charge and ΔV the voltage ripple, as can be seen in figure 7.2a.



(a) Definition of the voltage ripple and the capacitive charge.

(b) Illustrate the internal amplifier feedback output Pin 3 of the *UC1825*.

Figure 7.2: Relation between the voltage ripple and the internal amplifier of the *UC1825*.

The DC-gain from the inverted amplifier is set from a voltage level of 5.1 V and the DC-offset can be calculated as

$$\text{DC-offset} = \frac{\Delta V}{2}\,\text{DC-gain}, \tag{7.8}$$

where the gain is set by the designer. Clearly, the minimum voltage offset must be greater than half the ripple to avoid any strange behaviour in the system as well as a marginal should be considered, see figure 7.2b. Equation (7.8) is only valid with a proportional gain, but usually there exists capacitance in the negative feedback loop of the amplifier that attenuates the ripple even further.

Worth mentioning is that the original DC/DC converter has an implemented protection such that the differential error can not exceed the limit of 3.3 V otherwise the DC/DC converter powers down.

8 Synchronous Feedback Alternatives

Here, three feedback alternatives are presented based on synchronization with the PWM-circuit on either using the clock pulses or the gate pulses out from the *UC1825* and an alternative of using the secondary side as a load. The parameter values used in these simulations have not been evaluated in detail to correspond to theirs optimum state, instead engineering methods have been applied.

8.1 Clock Design with the *UC1901*

This design includes an extra transformer that needs to be coupled between the two sides. The clock from the *UC1825* (Pin 4 or Pin 6) shall act as the synchronous clock to the *UC1901*. From the *UC1825* data sheet, it can be seen that there exist two PWM outputs, but the current DC/DC converter operate only with one phase (Pin 11) of maximum two phases. That implies that the gate (PWM) pulses switch with half the clock frequency.

The first alternative is to use the clock frequency directly to the *UC1901* external clock (Pin 2). This means that the switching will be synchronous with the gate pulses with one extra sample in between, see figure 8.1. Hence, it will be retrieved as the maximum positive respective negative error out of the *UC1901* differential amplifier. If only the precise synchronization is requested that can be achieved with implementation of a D flip-flop (dashed) in toggle mode.

A schematic overview of the clock design can be seen in figure 8.2.

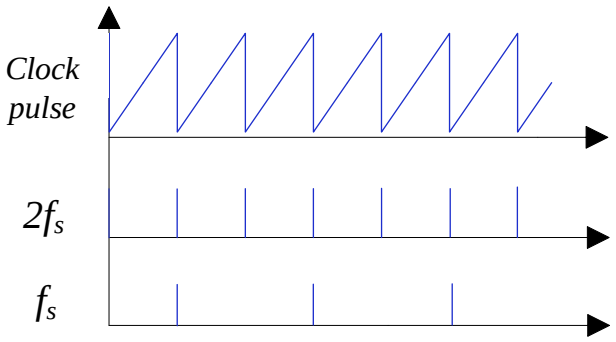


Figure 8.1: Illustration of the two synchronous switching frequencies, where f_s is achieved with a D flip-flop.

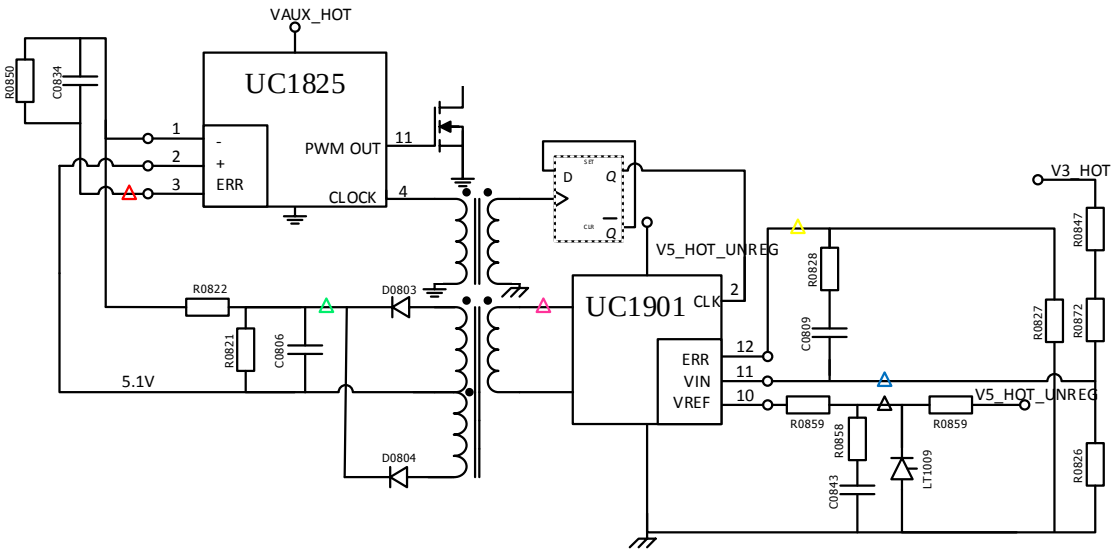


Figure 8.2: A schematic setup of the clock alternative with half the clock frequency.

8.2 Clock Design with the *UC1901* Simulation

The realization of this model uses the base simulation design of the *UC1901* in figure 4.17. In addition to the old simulation circuit, an amplifier corresponding to the *UC1825* internal amplifier has been connected to the diode detector at the demodulation stage and an extra output winding has been added, see figure 8.6.

As synchronous switching is the primary focus, an extra transformer coupling has been designed to transfer the clock signals from the primary side. As stated earlier, the clock frequency from the PWM-circuit will be used for synchronization. Section 4.3 showed that the CLK/LEB had enough voltage magnitude range to trigger most 5 V components such as a buffer called *74AC244*, which is used here. The simulations will however use an ideal clock pulse as clock for simplicity.

In figure 8.3, the clock pulses enter a buffer named *74AC244* which generates a pulse when trigged with the frequency of the clock. The pulse width is later scaled in time with an RC-circuit (high pass filter) to shorten the pulse as only the voltage rise points are needed and thereby avoiding potential saturation of the transformer. The only information that needs to be transferred is time.

Some voltage losses and altering shape occur and an extra buffer is added before the coupling stage. The 5 V pulses with narrow ON-time enter the transformer that later are transmitted to the secondary side where the signal is reconstructed after another buffer *74AC244*.

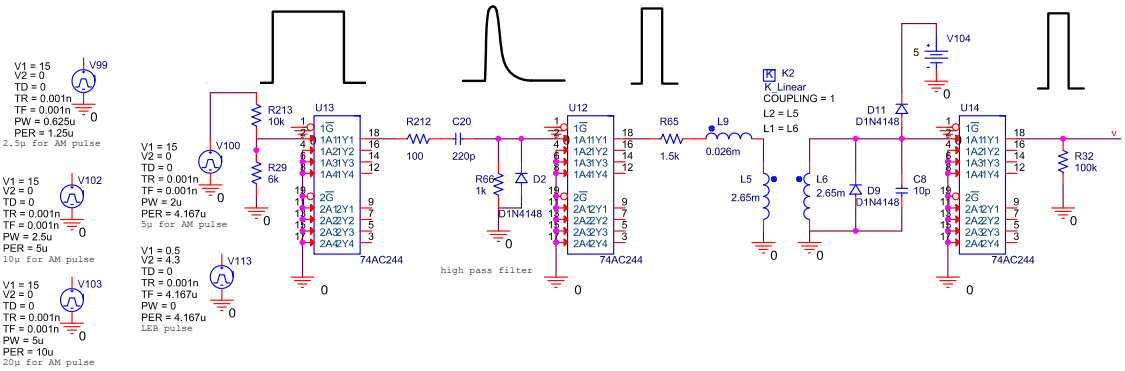


Figure 8.3: The simulation profile for the transmission of the clock pulses from the primary side to the secondary side.

Hereafter is the signal (v) in figure 8.3 connected to the *UC1901* Pin 2 and is considering to be synchronized. In the simulation model, an oscillation pulse is required to control the switches for the AM-modulation. This is generated by using D flip-flops in toggle mode to create 50 % duty cycle signals.

In figure 8.4, the clock pulses (v) enter the D flip-flops that control the switching in figure 8.6, OCI_D- and OCI_D+. As mentioned in section 8.1, one could select one of the two frequencies as switching frequency. The top circuit correspond to the double synchronization frequency and the other to the synchronization frequency. The switches $U31$, $U32$, $U35$ and $U36$ are used to set the operation mode, for example $RR0 = 0$ and $RR = inf$ give the double synchronization frequency. Note that a toggle D flip-flop reduces the frequency of the input by a factor of 2. This implies that different conditions must be tested in the simulations for the two transformers and will be explained further down.

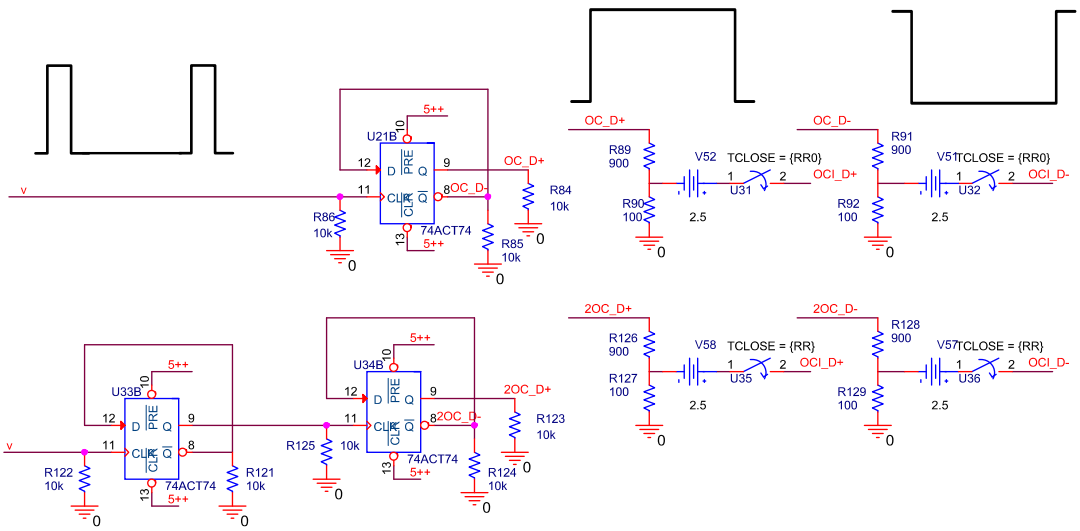


Figure 8.4: The oscillation circuit used to control the switches in the simulated AM-circuit.

Figures 8.5 and 8.6 show the new improved feedback circuit from the internal differential amplifier in the *UC1901* to the AM-modulation circuit and at the end with the internal amplifier in the *UC1825*.

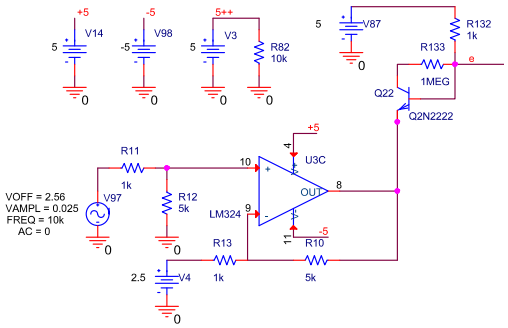


Figure 8.5: The differential amplifier that shall corresponds to the internal amplifier of the *UC1901*.

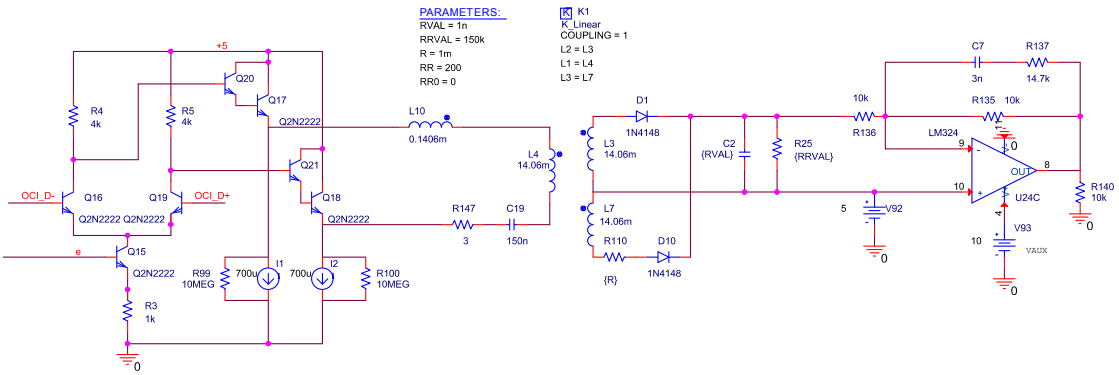


Figure 8.6: The AM-modulation circuit with the redesign transformer and the *UC1825* inverted amplifier.

The clock transformer values was obtained with an excel calculation sheet and are given in table 7.4. Other parameter values as the feedback path for the differential amplifier are chosen with respect to the present model and no exact calculations have yet been made as the real implementation with the *UC1901* will be altered. The negative voltage in figure 8.5 exists to simplify the simulation and is not present in the *UC1901*.

To gain an understanding of how the circuit operate at a certain point, a simulation with the following inputs were made at *U3C* in figure 8.5: a DC-offset of 2.56 V with a sinusoidal signal with an amplitude of 25 mV@10 kHz. Before the simulation was conducted, some adjustments of the amplifications were made to a gain of 5 at the input error amplifier and a gain of 1 at the corresponding amplifier at the *UC1825*. Figure 8.7 shows the results with an AM-signal frequency of 200 kHz and figure 8.8 the results with a frequency of 400 kHz, of which the later one shall correspond to the clock of the *UC1825*. Note that the circuit is DC-coupled and tends to operate in AC-mode when implemented.

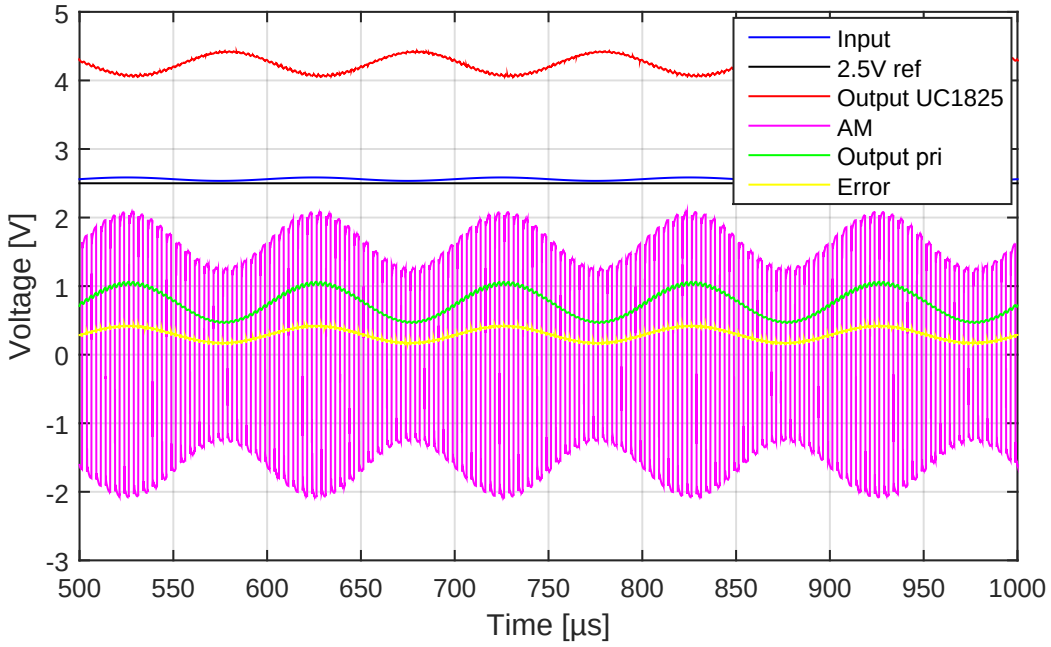


Figure 8.7: The clock model simulation results at a 200 kHz AM-signal.

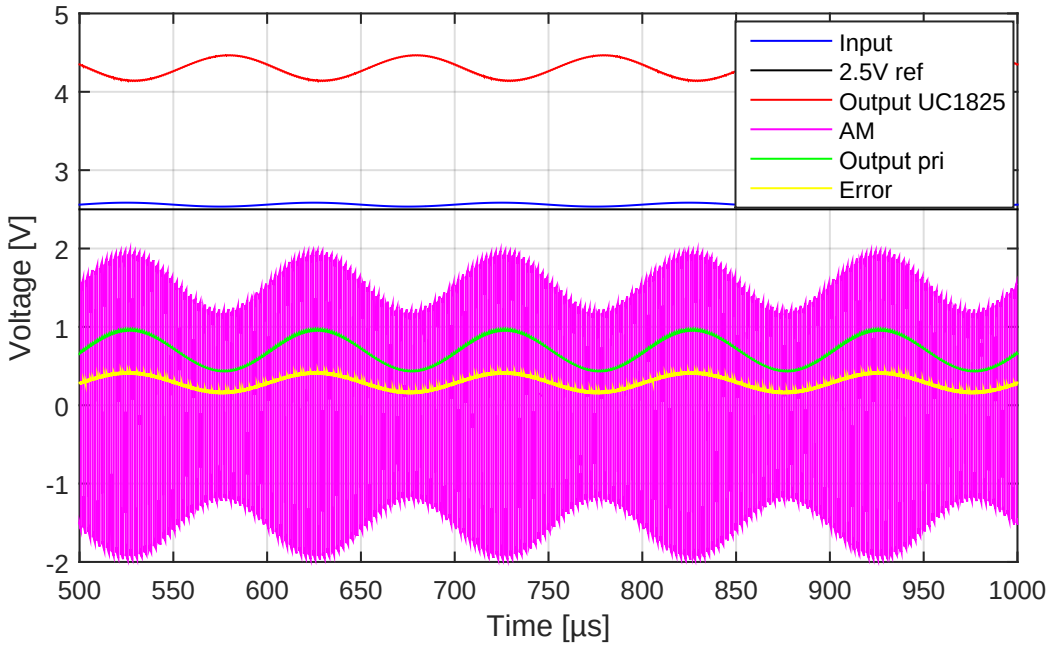


Figure 8.8: The clock model simulation results at a 400 kHz AM-signal.

The interpretations of the simulations show that synchronous switching is working. From a visual point of view, the synchronous switching with the clock can be considered better. For example the demodulation ripple was recorded with an injection error of 500 mV at different frequencies of the AM-signal. It resulted in 22 mV@400 kHz, 45 mV@200 kHz and 124 mV@100 kHz. The transformer currents were in these simulations within the margins stated in table 7.4.

Except of testing the new three winding transformer, the clock transformer needs to be evaluated at the correct frequencies. Due to simulation structure, this look-up table (table 8.1) can clarify the different frequencies, for example a 400 kHz input clock gives an AM-frequency of 200 kHz. Saturation problems can occur at lower frequencies, where both 100 kHz and 400 kHz have been tested for both transformers. A CLK/LEB pulse, see figure 4.10 has been generated as input to the clock transformer and showed promising results.

Table 8.1: Conversation table over the simulation frequencies due to the simulation profile.

Clock input		**AM-signal**	
1.25 μs	800 kHz	2.5 μs	400 kHz
2.5 μs	400 kHz	5 μs	200 kHz
5 μs	200 kHz	10 μs	100 kHz
10 μs	100 kHz	20 μs	50 kHz

8.3 Gate Driver as Clock Design

The gate driver design use the gate pulses (Pin 11) of the *UC1825* as clock. Once again, the rise time of the pulses are enough to send across the isolated barrier to the *UC1901*.

The same circuit as in the clock model is used to transmit the clock pulses over the transformer, see figure 8.3. A problem can be during transient occurrence such as load steps, where the gate pulse sticks in a certain state and therefore a redundancy is necessary. If there would be no clock pulses into the *UC1901*, the DC/DC converter will not work. This problem can be avoided by implementing a sense circuit that act as an automatic clock if no gate pulses are detected after a certain time. This sense circuit consists of inverting schmitt triggers with a pulsed RC-circuit that generates pulses with a constant frequency. The switching frequency is not the crucial part as if it was none at all. A lower frequency will also increase the output voltage ripple.

8.4 Gate Driver as Clock Design Simulation

The operation of this design is similar to the clock model with some modification. The extra winding transformer at the output is used as before. The clock transformer would instead have the gate pulses as input which means that the switching will be half clock frequency. As the clock transformer is designed for higher frequencies, the automatic clock has been placed on the secondary side to avoid saturation of the transformer. The current transformer can handle lower frequencies as long as the pulse width is narrow, in such a way that saturation is avoided.

This pulse generator is in reality placed between the node v and the *UC1901*, see figure 8.9. The node CK will then be the input to the *UC1901* clock Pin 2. In the simulation this node is connected to the upper D flip-flop circuit node v in figure 8.4. The purpose of this circuit is to handle situations when pulse-skipping occur. In such cases an automatic clock will start to produce pulses with a fix frequency set by a RC-network.

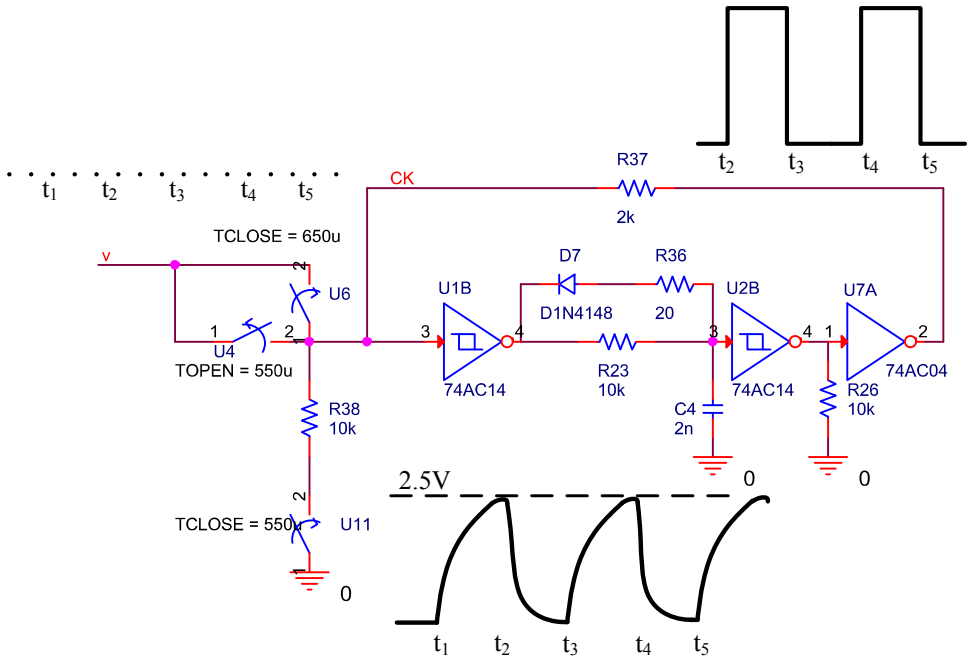


Figure 8.9: The automatic clock circuit for the gate design.

Suppose pulse-skipping occurs in figure 8.9, then the following sequence is executed. No pulse implies zero volts at node v/CK, the inverted schmitt trigger start to charge the capacitor C_4 through R_{23}. When the voltage of 2.5 V is reached over the capacitor, a fast discharge occurs through the diode $D7$ and the inverter $74AC04$ send out a pulse. This process continues until the original clock pulse returns and takes the control due to the high resistance in the feedback loop. Also as the original frequency is higher which lower the charging time of the capacitor such as the trigger voltage is not reached.

The node v has a short pulse width below 100 ns which is set by the clock transformer stage. The automatic clock is design with a time constant of

$$R_{23}C_4 = 10k\,2n = 20\,\mu s, \tag{8.1}$$

where the time delay between each new pulse is half the time constant, i.e. 10 μs. This means for example if $R23$ is equal to 5 kΩ, the delay would be 5 μs.

As mentioned before, D flip-flops are used in toggle mode to create the clock pulses to the simulated AM-circuit and will therefore have half the frequency of the pulses at CK. This implies that the model needs to be evaluated at two different cases: one with the clock transformer at the correct frequency and one with the correct AM-frequency, which also has been done.

With an activated automatic clock results in a period of 20 μs for the AM-signal and period of 5 μs when disabled at an input clock period of 2.5 μs. This can be seen in figure 8.10.

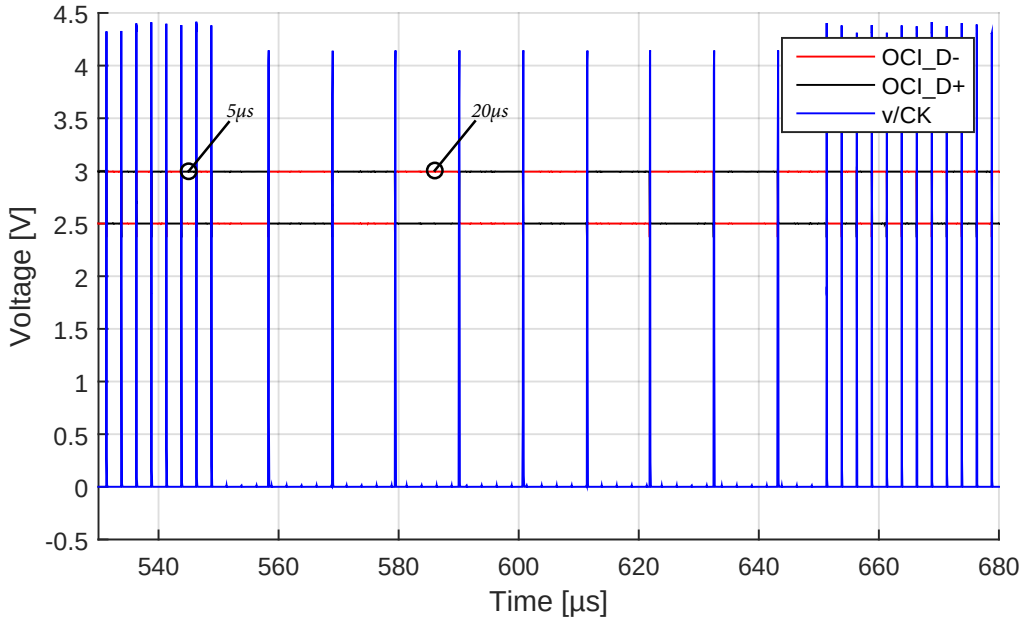


Figure 8.10: The clock pulses (blue) and the oscillation pulses to the AM-modulation circuit when the automatic clock is activated and deactivated.

To illustrate the automatic clock, a disconnection of the clock transformer is made at 550 μs to 650 μs. The parameter v/CK in figure 8.10 goes from a frequency of 400 kHz to 100 kHz, which implies that clock signal to the *UC1901* will have a delay of approximate 10 μs before the automatic clock is activated. The output results in figure 8.11 are based on the same input as for the clock design with an AM-signal of 200 kHz.

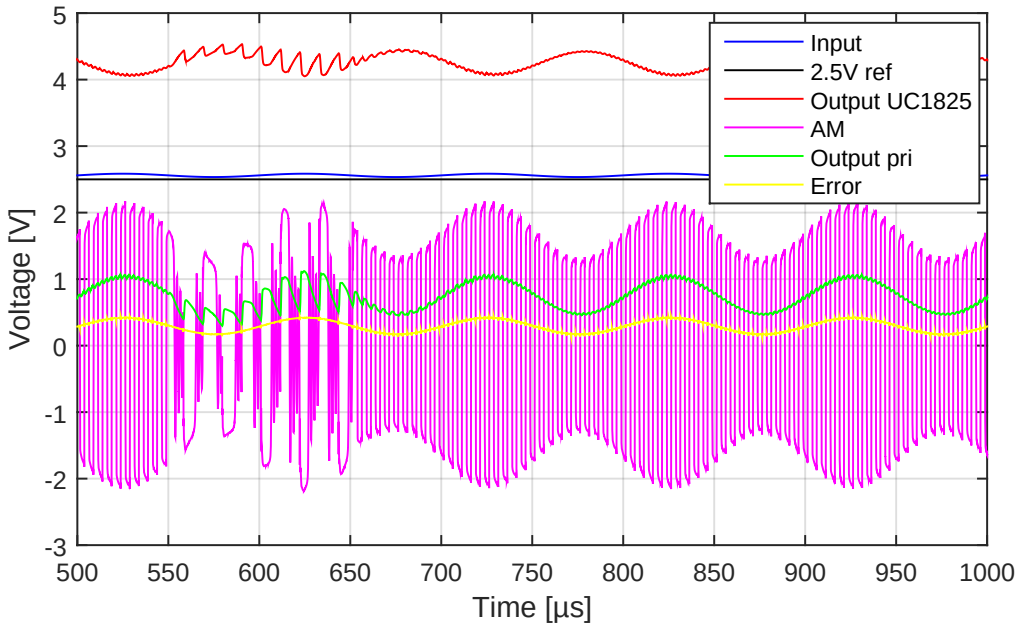


Figure 8.11: The gate driver simulation results at an AM-signal of 200 kHz with the automatic clock activated under 100 μs.

8.5 Load Design

The configuration setup of the load design is illustrated in figure 8.12 with a start-up circuit symbolized as a box. This design concept is based without using the *UC1901* as modulator, instead an error amplifier is located at the secondary side. The extra amplifier in figure 8.12 is just an inversion step and is necessary to obtain the right sign of the error signal. One large advantage that can be assumed to be better with this design is the reliability of the radiation tolerance compared to the *UC1901*.

The load design uses a three winding transformer where one of the primary winding is pulsed with a square signal. This square signal is generated by a comparator that has a clock input signal and a reference voltage. As synchronous mode is preferred, a clock from the PWM-circuit is used (as in figure 8.12), but an external clock source can also be used to set the frequency of the signal.

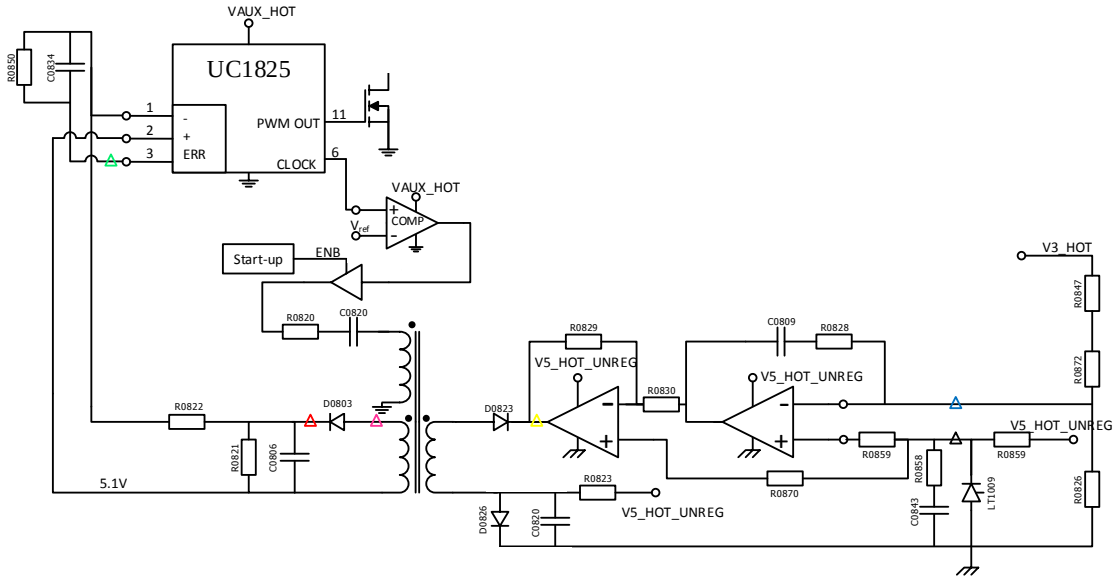


Figure 8.12: A schematic illustration of the load design circuit by using the secondary side as a load.

The injected square signal in figure 8.13 is used as a carrier and will magnetically coupled to the other two windings with a fixed ratio. When $V3\_HOT$ becomes too high such that a positive error is present at the secondary output amplifier, the carrier signal will include this error and coupled it to the primary output winding as a variation in the voltage, i.e. the secondary side is unloaded.

To boost the voltage when $V3\_HOT$ becomes low is accomplish by the *UC1825* and then the differential output shall be zero at the primary output winding according to the original topology, i.e. the *UC1901* could only brake the secondary voltage. When the scaled $V3\_HOT$ is less than 2.5 V, the node at the secondary output amplifier will be dragged down to ground, i.e. the secondary side is loaded. And cause the carrier signal to follow as they are magnetically coupled such that an approximate zero differential error is present at the primary output.

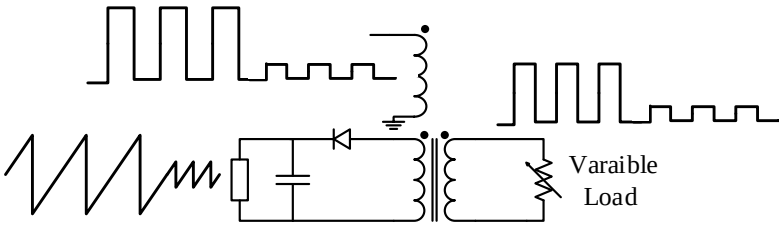


Figure 8.13: A simple illustration of the load design operation states when the secondary side is unloaded and loaded.

To clarify, the error is only transferred during the positive square pulses to the primary side, i.e. the diode becomes forward biased at the secondary side.

8.6 Load Design Simulation

From the schematic load design a simulation profile has been constructed and can be seen in figure 8.14. The operation of the simulation model reflects the original feedback solution by only brake the voltage when $V3\_HOT$ is too high. By using the secondary side as a load, an error can be transferred to the PWM-circuit. The special three winding transformer is designed to fit in an *E14* planar model with the core material *3E6* as described in section 7.2.

Initial at zero voltage error (loaded) at the secondary side, the voltage at the primary output ($L4$) experienced an offset. The unwanted DC-offset came from the forward voltage drop of the diode $D11$ which is coupled to the output. It revealed in an approximate 250 mV DC-offset and to compensate for the voltage drop an extra diode has been added between the inductor $L3$ and ground at the secondary side and thereby remove the offset directly from the origin.

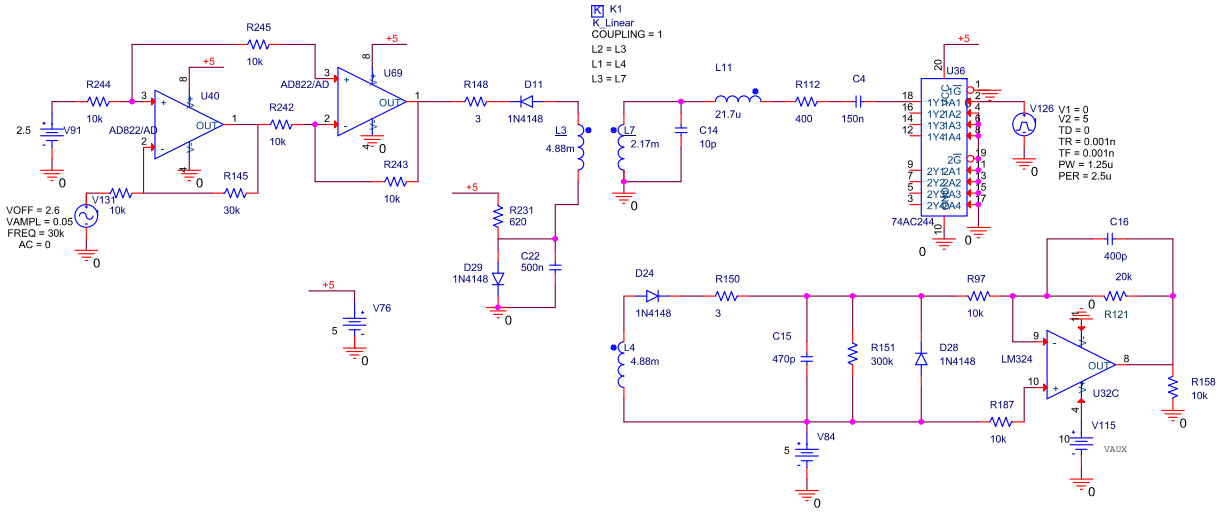


Figure 8.14: The load simulation model is based on a square carrier that couple the error to the primary side via a transformer by using the secondary side as a load.

The simulation results shown in figure 8.15 are with a DC-input of 2.6 V and an AC-signal amplitude of 50 mV@30 kHz. In this particular case uses an amplification from secondary side of 3 at the EA and 2 at the *UC1825*. The clock frequency used in the simulation was 400 kHz.

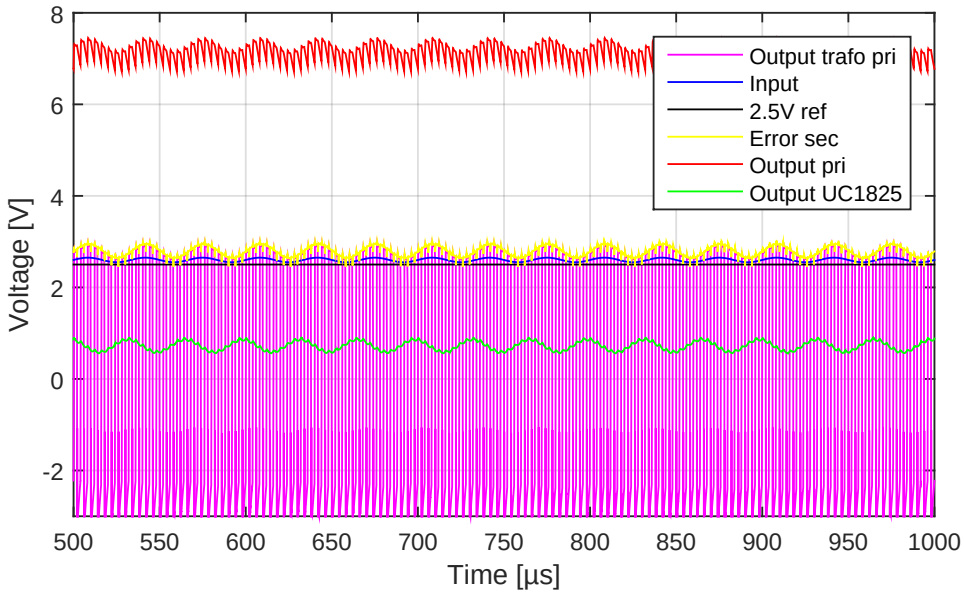


Figure 8.15: Simulation results with a sinusoidal input for the load design with the voltage over the inductor $L4$ (pink) and the error (yellow) at output of the inverted operational amplifier.

Depending on the compensation net at the *UC1825* and the filter capacitor, the ripple level can be lowered to an extent. This topology also makes the output ripple increase with the load, i.e. higher error. This phenomena is not present in the clock design alternative with the *UC1901*. The primary output ripple resulted at a frequency of 400 kHz in 586 mV.

A square pulse with preferably 50 % is desirable in order to get a low ripple output. The duty cycle is set by a comparator with an input of a reference voltage and a clock pulse, for example CT. A variation in the clock pulse magnitude, see table 7.1 for CT, with a fixed reference including tolerance of components can lead to a different duty cycle output and results in higher voltage ripple.

At relative low operation frequency (100 Hz), the ripple becomes too large even with some fixes. One way could be to use larger capacitance, but then an additional frequency pole is present in the feedback path and the concept of reducing the filter is gone such that the current model with the *UC1901* can be considered to be better. With higher frequency available, the ripple decrease distinctly but on the other hand we are back to the asynchronous switching as the *UC1901* with less components. For this alternative to be comparable and have potential, the synchronous switching of the clock frequency can be seen as a requirement.

Note that the error signal in the simulation lies at a couple of volts which is a consequence of a DC-coupled mode. In a sharp implementation of the load feedback, it would operate in AC-coupled mode where the error would be below 1 V.

Symmetric Load Design

A bit more complex alternative design to the presented load model was simulated, where it was based on symmetry. It operates in the same way as in the simple load design by using the secondary side as a load. The diode and the inverted operational amplifier were replaced with a pair of BJTs, where the internal diodes are used in each complimentary pulse of the carrier signal. At the receiver output an extra winding has been added to lower the ripple even further, see figure 8.16. The complexity comes from that a relative square pulse must be generated from the clock of the PWM-circuit to feed the primary winding. With variation in the carrier magnitude and the duty cycle will lead to increased ripple in the output windings as both pulses are rectified, i.e. symmetry.

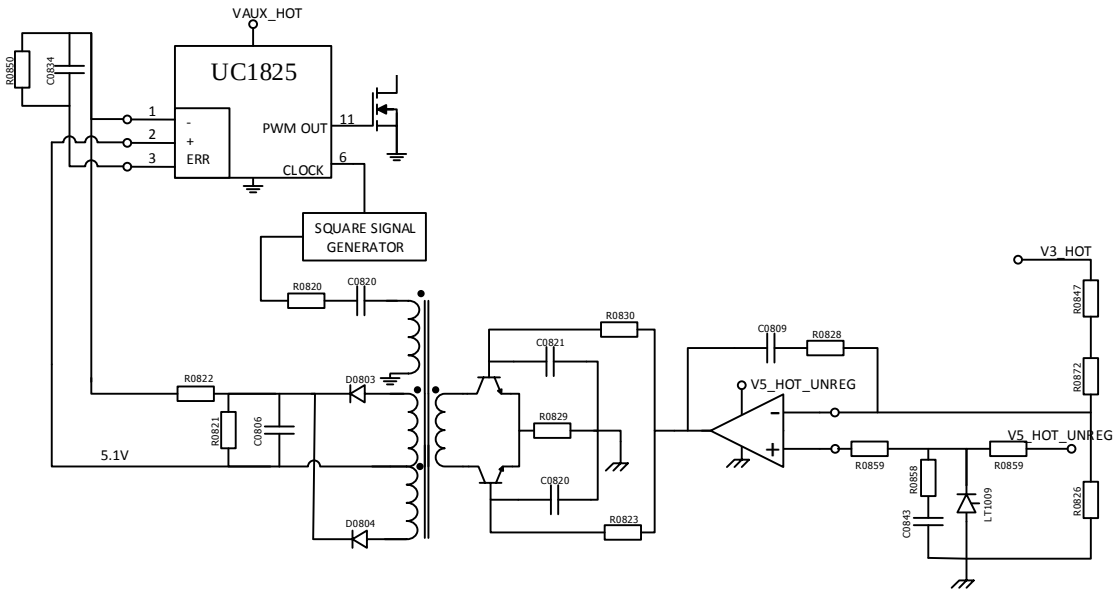


Figure 8.16: A load design based on symmetrical behaviour.

A square pulse signal can always be constructed, but require more analysis and extra components. This concept has potential, but due to lack of simplicity, the focus will be on the simple load design and this symmetric load design can be seen as an improved load design if this concept is found to be interested. A simulation profile is available in appendix E.

If the alternative load design is considered to be synchronized and achieve low ripple, the filter used can likely be reduced to a minimum and having a great potential to be optimized to at least the same performance as the *UC1901*, including total radiation independence.

9 Asynchronous Feedback Alternative

The performed study revealed an interesting modulation step named delta sigma modulation, which is an asynchronous alternative. The following section presents an overview of the modulation step but also a simulation profile that is adapted to the original feedback design.

9.1 Delta Sigma Theory

A delta sigma modulator or ΔΣ-modulator is an analog to digital conversion (ADC). Both an ADC and a digital to analog converter (DAC) of ΔΣ have very similar structure. Signals of both analog and digital nature can be handled as minor differences occur and an overview of a DAC model is available in appendix D.1.

The main principle of an ADC is to inject an analog signal into the ADC which generates a digital data stream of 1s and 0s with correlations to the input signal, which then can be transferred over an isolated barrier if wished. At the output, the digital signal is filtered to remove noise and ready to use. One key outcome from the ΔΣ process is the included feedback pulse of the ADC. In fact, if the analog feedback pulse is averaged, it corresponds to the input value. This property will be exploited in our design of a delta sigma solution.

A first order ΔΣ-ADC consists of a summation, an integrator, a clocked comparator, a D latch and suitable filter. A block diagram of a first order ΔΣ-modulator is illustrated in figure 9.1. The term Δ comes from the comparison between the input value and the feedback value as a difference. The Σ origin from the summation of the error in the Δ operation and is mathematical described as an integral for continuous time [30].

There exist also higher order of ΔΣ-modulation systems. The advantages with higher order are partly that less noise is generated at the filtering stage, but a second order is often considered as a balance between performance and complexity, which most components on the market are, for example *AD7403*. A second order delta sigma can be constructed with a cascade coupling of two first order delta sigma units, but for higher order, it is not recommended as more than two integrations cause an unstable system. In such cases other methods need to be applied. Hereafter a first order modulator is described.

There are two variants available: a switch-capacitor model (discrete time) and an active-RC model (continuous time), which can be used for both DC– and AC-signals. Here, the focus will be on the continuous time model, while the switch-capacitor circuit include switches that need to be controlled, i.e. lead to complexity and also increased radiation dependence.

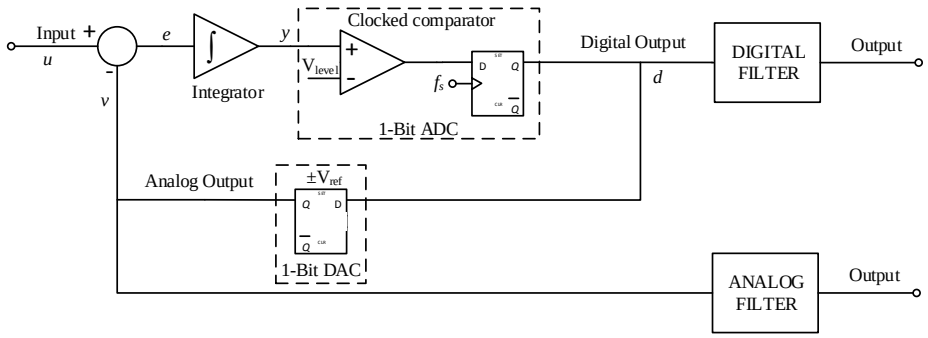


Figure 9.1: A block diagram of a continuous time first order ΔΣ-modulation system.

The operation in figure 9.1 can be described as following. The analog input signal (u) is summarized with the analog feedback signal (v) from the 1-Bit DAC that enters into an integration stage. The feedback signal (v) makes the integrator ramp up and down and gives an analog output (y). The output value is presented to a 1-Bit clocked comparator that generates a digital bit steam (d) with a defined sampling frequency f_s. Depending on the difference between the comparator reference voltage and the integrated signal, 1s and 0s are fed out. The digital signal is then digitally filtered to remove noise from the switching. A digital sinc filter is often used in such context.

The digital output (d) is also fed back through a 1-Bit DAC that output $\pm V_{ref}$ voltage to the summation with the input signal. The response from the 1-Bit DAC changes the error value (e) and force the integrator to constantly alter the derivative, a detailed behaviour of the integrator is shown in appendix D, figure D.3. A consequence from the operation leads to that the average value of the analog feedback pulse (v) with the sampling frequency f_s will follow the input value (u) over time. This implies that an analog low pass filter can be used to recover the injected signal as it acts as an average function [30], [31].

For understanding purpose, the discrete domain will be used for explanation, but the same principle can be applied to continuous time domain. In figure 9.1, the states can be described in discrete domain as

$$y(n) = \underbrace{y(n-1)}_{\text{initial value}} + \underbrace{u(n) - v(n-1)}_{\text{error}} \tag{9.1}$$

for $n = 1, 2, ...N$, where n represent discrete time, i.e. $n = f_s t$. For a number of time samples N, (9.1) can be defined as the summation from 1 to N as

$$y(N) - y(0) = \sum_{n=1}^{N} [y(n) - y(n-1)] = \sum_{n=1}^{N} [u(n) - v(n-1)] \tag{9.2}$$

and by dividing both sides with the number of time samples leads to

$$\frac{y(N) - y(0)}{N} = \frac{\sum_{n=1}^{N} [u(n) - v(n-1)]}{N}. \tag{9.3}$$

If $y(n)$ is finite (reach a maximum value) that implies that the left side of (9.3) for limes $N \to \infty$ equal zero. Hence,

$$U_{AVG} = \lim_{N\to\infty} \frac{1}{N} \sum_{n=1}^{N} u(n) = \lim_{N\to\infty} \frac{1}{N} \sum_{n=1}^{N} v(n-1) = V_{AVG}, \tag{9.4}$$

which state that the average value of the analog output tends to be equal the input value [30].

The delay of $(n-1)$ correspond to a sample and hold which is modelled as a clock D flip-flop in continuous time, where the delay vary with the selected frequency. For infinity switching frequency, there will not exist any time delay and thereby the system will lose its operation capability.

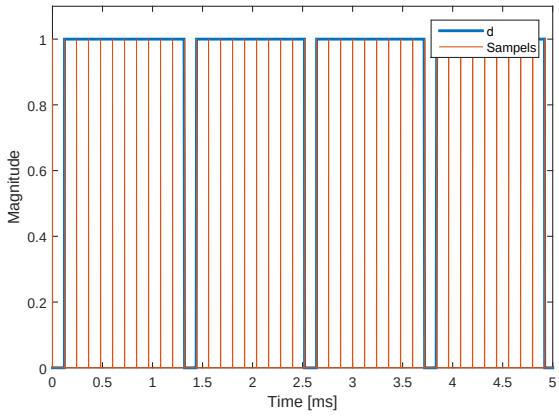
To understand the concept of the output values, a digital density is defined. If the input voltage (u) is set to a fix value as $(u + V_{ref})/(2V_{ref}) = 90\,\%$ of the supply range ($\pm V_{ref}$), the modulator will try to accomplish this value with time by using 1s and 0s. This generates a bit-stream after 9 samples to 0111 1111 1, which has a density of $8/9 = 0.88$. With increasing number of samples N, the closer the digital density will come to 90 %.

The average analog value of the digital output can be calculated according to

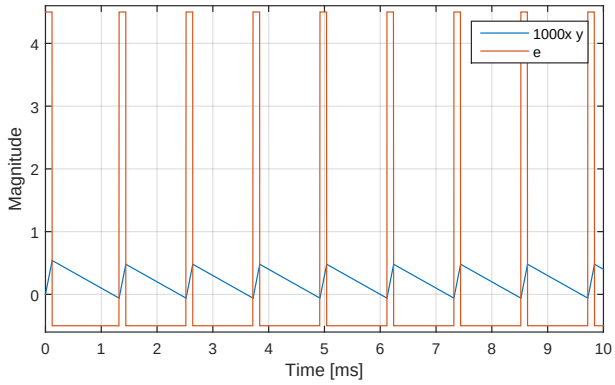
$$V_{AVG} = \frac{2V_{ref}}{N} \sum_{n=0}^{N} d(n) - V_{ref}. \tag{9.5}$$

From the above example with an input voltage of 2 V and a supply range of 5 V, would give the analog value 1.94 V according to (9.5) with 9 samples and in time reach the value of 2 V [28]. A repeated bit-stream of 0111 1111 11 can be observed over time in figure 9.2a, which force the output result to $9/10 = 0.9$.

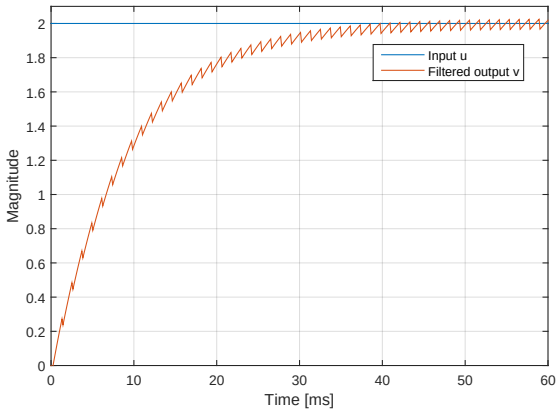
In figure 9.2, the operation signals are shown at different nodes referred to figure 9.1. Equation (9.5) is the pure mathematical representation and in figure 9.2c, an analog filter is used to recover the signal which explains the rise of the output value (v). That means with less filtering, a faster rise time is achieved with the consequence of higher ripple. A Simulink model of the presented results can be seen in appendix D.



(a) The digital bit-stream and sample times.



(b) The integrated error as a triangle shape and the input error signal (e).



(c) The filtered analog output (orange) tends to reach the input value (blue) over time.

Figure 9.2: The operation signals at the different nodes presented in figure 9.1 for a certain operation point of a ΔΣ-modulation.

To realize this model electrically, a differential mode implementation is needed which can be seen on page 31 in [30]. Although a non-differential mode will work with the difference that the output will be inverted to the input value. In the next section, just a non-differential circuit has been selected and is described further.

9.2 Delta Sigma Design and Simulation

A design and simulation of a first order delta sigma modulator was made in Orcad PSpice to investigate the operation. Figure 9.3 illustrates a continuous time non-differential mode delta sigma circuit. With non-differential means that if 2 V is injected, the output will be −2 V. Modifications of the described model in section 9.1 have been made to suit our purpose.

In our design there are no digital signals present, only analog signals. Also, negative voltage is not available at the current circuit board, it is then preferable to design according to these conditions. That means that the feedback loop can not consists of $\pm V_{ref}$, namely ground can not be the common zero voltage. Instead, a reference of 2.5 V has been selected to avoid negative voltages. This adjustment makes it possible to switch the feedback V_{ref} in section 9.1 with the values 0 V or 5 V instead. Note that a positive voltage reference is present all the time at the integrator capacitor except when the feedback loop change to high and INV node becomes lower than the reference value. Thereby has the slope direction of the integration been solved.

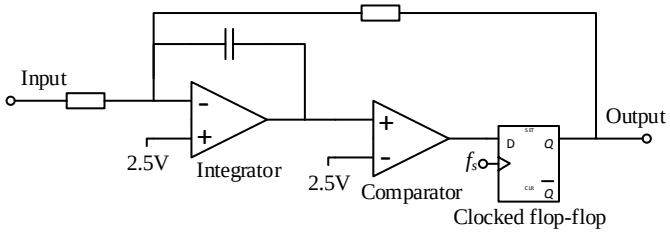


Figure 9.3: Illustration of a non-differential first order delta sigma modulator.

This concept is built to transfer the real value as described in section 5.2, but it is possible to transfer the error with some modifications. The PSpice model can be seen in figures 9.4 and 9.5. Important to comment is that all components used in the simulations only give a good indication of the operation in reality, but the operation principle can be verified and be used to improve the design.

In our design for input voltages above the reference 2.5 V, a negative voltage response at the reconstruction stage is given in relation to the reference and vice versa. An example with an input of 2.6 V results in a voltage of 2.4 V at the output ($x0$) in figure 9.5.

In figure 9.4, the analog input enter an operational amplifier *LM108A* that acts as an integrator with the capacitor $C8$ and is compared with a reference of 2.5 V. The capacitor value $C8$ does not directly influence on the operation behaviour, the only requirement would be that the integrator time constant should be comparable with the switching frequency.

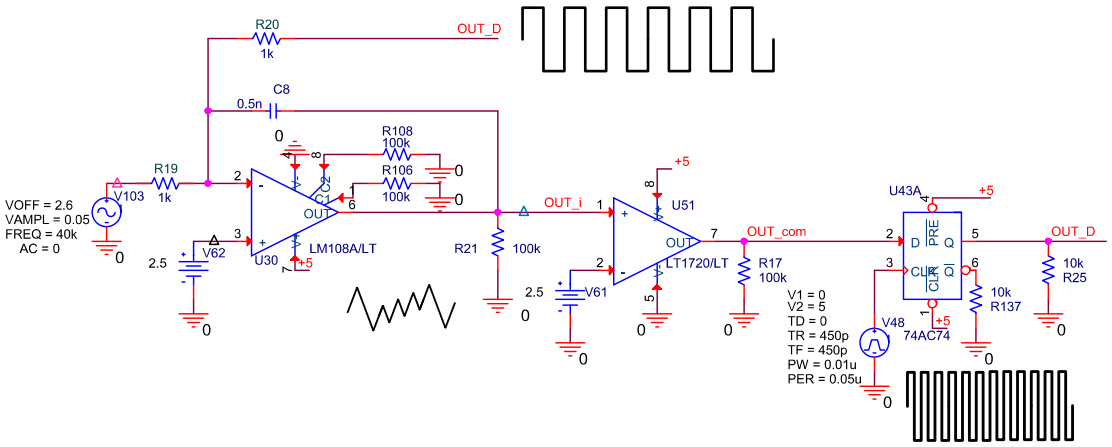


Figure 9.4: The simulation profile of a delta sigma modulation.

The integrated value is fed to a rail-to-rail comparator that generates pulses for voltage over 2.5 V with a certain amplitude. These pulses are reshaped with a magnitude of 5 V through a clocked D flip-flop *74AC244* [32]. The feedback from the D flip-flop is then added with the input signal that forces the integration to constantly change derivative. For negative slope at the integrator, 5 V is supplied by the D flip-flop. Meanwhile a reference of 2.5 V acts as positive slope for the integrator when the feedback voltage is 0 V. A consequence from this structure, the operational amplifier *LM108A* can be used at the same time as an amplifier with a gain of approximate $-R20/R19$.

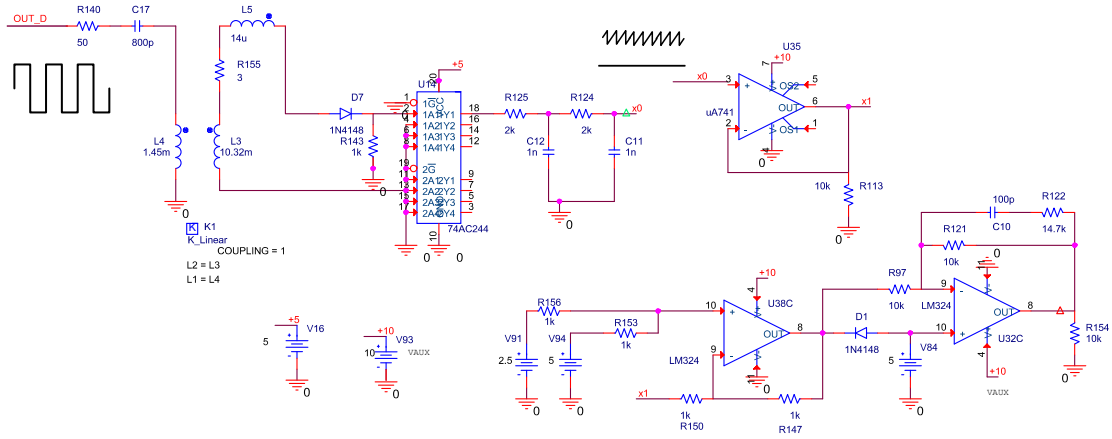


Figure 9.5: Transmission of the analog feedback signal (*OUT_D*) and reconstruction as well as necessary implementation to adjust the output to the *UC1825*.

The output signal (*OUT_D*) from the D flip-flop is transmitted to the primary side over a transformer and reshaped to a pulse with a voltage magnitude of 5 V, see figure 9.5. A second order low pass filter is used as an average function to recover the signal with an amount of ripple, but a first order filter can be calculated to avoid an additional pole.

The recovered signal in the simulation showed sensitivity to load variation and a voltage follower was added to act as a buffer ($U35$). To be able to implement this model to the current PWM-circuit *UC1825*, a summing differential amplifier is used. A stable voltage of 7.5 V is needed at the amplifier where 2.5 V and 5.1 V are available on the primary side. But to achieve an accurate reference voltage, it can easily be created with a zener diode in reverse mode.

This amplifier ($U38C$) delivers a positive error for input voltages ($x1$) below 2.5 V to the EA of the *UC1825*. For voltages above the reference, the output will be less than 5 V and this can cause problems for the EA so the output is clamped with 5 V. A low pass filter is also used at the internal amplifier at the *UC1825* to minimize the ripple and at the end a working simulation concept is available.

The simulation results from the model are shown in figure 9.6 with a DC-offset of 2.6 V and a sinusoidal amplitude of 50 mV@40 kHz. The amplification gain in the simulation was selected to 1 at the secondary side and to 1 at the *UC1825* amplifier. The D flip-flop was clocked with 20 MHz.

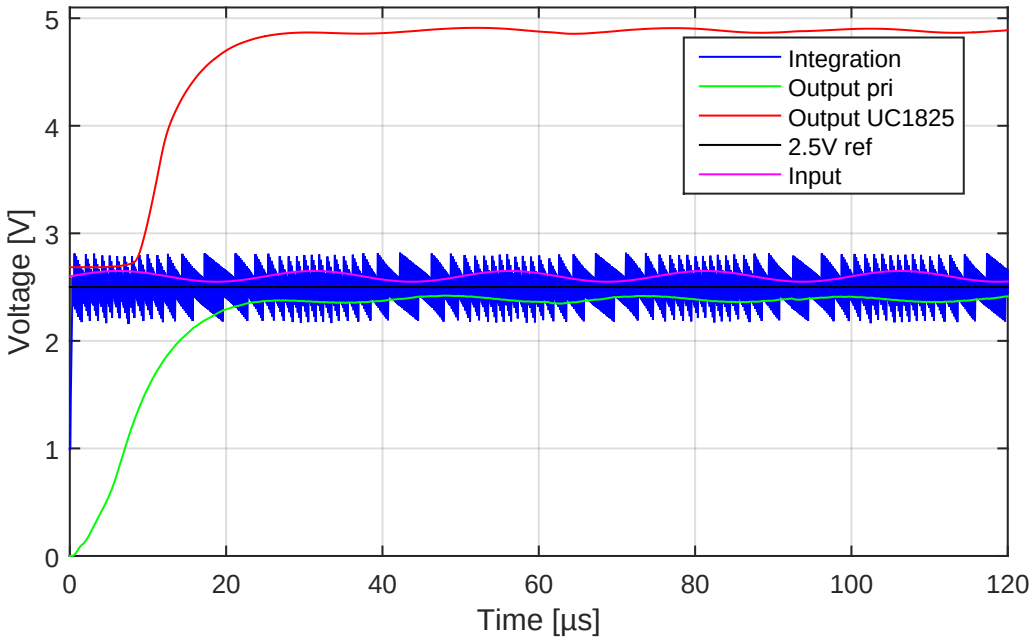


Figure 9.6: The simulation results of the $\Delta\Sigma$ model.

An issue during the simulation was noted. For a zero error input, the average output would be 2.5 V, but a small offset in mV can be expected for the circuit. An reconstruction offset of around 160 mV was the result at the primary output, see figure 9.7. A more detail analysis showed that the D flip-flop behaves abnormal at its undefined area despite a quite steep V/μs. If the reconstruction occurs at the secondary side directly only 0.6 mV offset was noted. This effect can be explained as the feedback path is on the secondary side and follow the output of the D flip-flop. In contrast to the reconstruction signal on the primary side where the buffer does not trigger on the undefined voltage as voltage is divided equal over the transformer. This effect will not happen in reality except if a very low slew rate buffer is used.

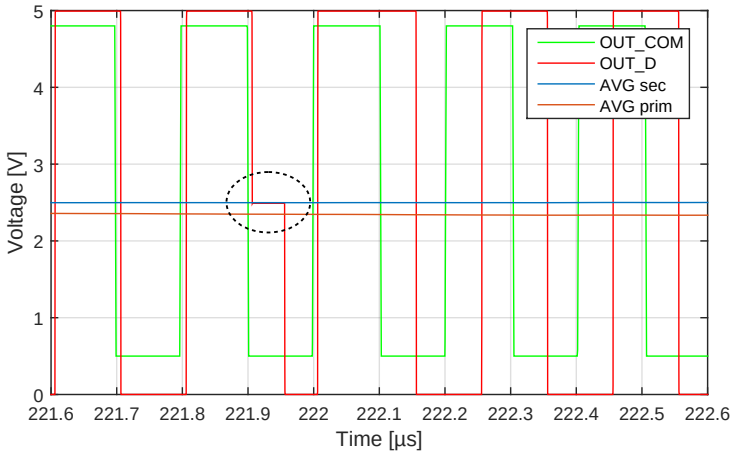


Figure 9.7: The D flip-flop output reacts strange in its undefined voltage region in the simulation at zero error.

The primary side double pole can in a real implementation be changed to a single filter. Also there exists a lot of building blocks that makes this solution more complex compared to the original *UC1901*. The output showed load sensitivity and can be an indication that the error signal might be better to transfer as it can be amplified without loss of information. Another implication with use of an error signal is that unnecessary operational amplifiers can be minimized.

As a $\Delta\Sigma$ design consists of elements that are radiation tolerant, it would be possible to build with discrete components and construct it on a circuit board. But the advantage of using a manufactured component is that everything would be included in a small package such that unwanted effects that might arise can be avoided.

This current configuration of $\Delta\Sigma$ use a lot of components as well as the same amount of filter as in the original solution. To optimize this model can be problematic due to usage of many operational amplifiers that have internal compensation in such a way performance parameters becomes limited as the bandwidth.

A working $\Delta\Sigma$-modulator has been simulated and demonstrated that a galvanically isolated feedback can be built by using $\Delta\Sigma$-modulation, in terms of taking the advantage of averaging the feedback response. To be able to exploit this topology further analysis is needed and considerations of rather transfer the voltage error instead of the real value.

10 Selected Feedback Designs

Although $\Delta\Sigma$-modulation could be a candidate, we have chosen to build the improved AM-modulation with the synchronous mode and the alternatives noted in the list below. The gate driver design presented in section 8.3 is similar to the clock design but is more complex and operates at a lower frequency and therefore this alternative will not be evaluated. The load alternative has potential as it is independent of the *UC1901*.

- Original feedback (internal clock) (asynchronous)
- Original feedback (internal clock) with improved transformer (asynchronous).
- Clock pulse from the *UC1825* as input to external clock of the *UC1901* (synchronous).
- Use the secondary side as a load without the *UC1901* (synchronous).

The planned circuit board shall be made in such a way that the second option is the same as the third, just some disconnection and connection of components to evaluate the new transformer against the original transformer. The original feedback will also be available on the circuit board for the purpose of comparing the other feedback alternatives.

11 Evaluation of the Feedback Alternatives

The scope of this thesis was to find new possible alternatives to the current design. As no directly new concepts were found, improvement of the present design has been investigated. To verify the simulations of the selected models, a circuit board is planned to be constructed. With start from the original circuit CAD-design, a redesigned was made in Mentor Graphic Design Capture (2012) with implementation of the extra feedback alternatives. Due to complexity and time limitation, the PCB-layout from the CAD-design was made by the staff of RUAG Space.

11.1 Inspection and Redesign of the Original CAD-design

During inspection of the CAD-design of the selected alternatives, a number of issues arose. As the feedback alternatives are based on simulation, factors like supply voltages, sensitive signals and integration of the components to the original design need to be reviewed.

Usually many IC-components have several units in a package that can be used in several feedback alternatives, but there also exist two grounding points, primary– and secondary ground. This will need planning in the design to minimize the component usage. It is preferable to have only one alternative at the time, such that a lot of $0\,\Omega$s have been implemented to activate and deactivate the feedback alternatives.

The synchronization with an external clock to the *UC1901* showed that not only will it trigger on the external frequency but also set the duty cycle of the AM-signal. That means that no 50 % duty cycle will be produced automatically by the *UC1901*. The simplest solution but also a rollback is to use a D flip-flop in toggle mode such that only half the clock frequency is fed to the *UC1901*. This is clearly a drawback that increase the ripple compared to if the double switching frequency would be used.

In order to lower the ripple, another small extra circuit has been added. It is built to double the clock frequency in such a way when it passes through the D flip-flop, the clock frequency with 50 % duty cycle is the input to the *UC1901*. From logic elements and a comparator, the double frequency circuit in figure 11.1 is designed.

This logic circuit is intended to be located at the primary side with the clock source as input and part of the clock transformer circuit (figure 8.3) connected to its output.

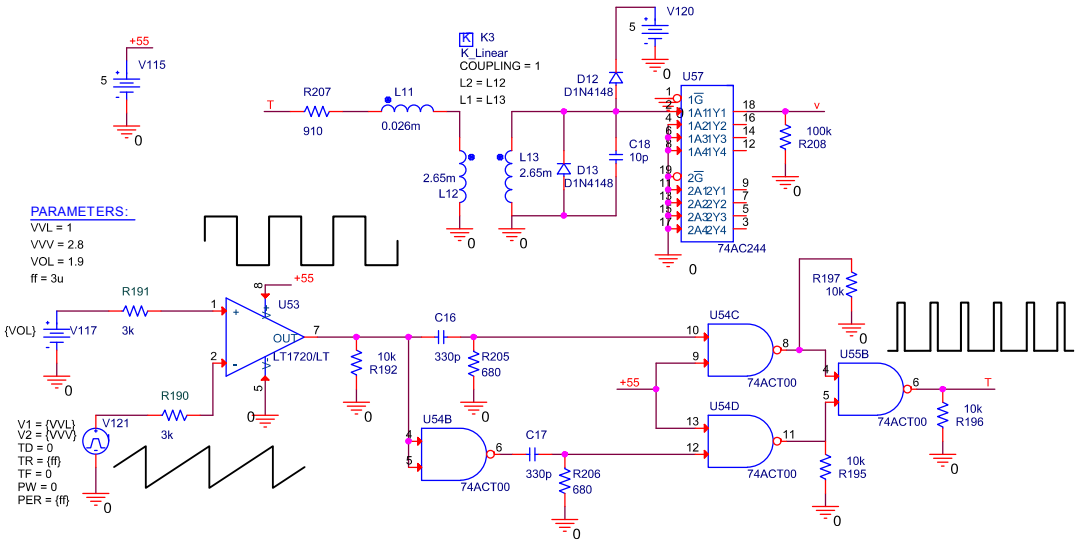


Figure 11.1: Double frequency circuit by using a comparator and NAND-gates.

Initially was the *CLK/LEB* supposed to act as the synchronous clock, but compared with the *CT* of the *UC1825*, a ramp signal, a 50 % duty cycle was easier to achieved. But by using the clock signal in the logic solution comes drawbacks. The voltage ramp of *CT* has a tolerance level that can vary the valley-to-peak voltage as stated in table 7.1, which implies that the duty cycle might deviate with a fix reference voltage into the comparator. That consequently leads to that saturation may occur in the new design transformer for the *UC1901*. A simulation with a shifted duty cycle revealed just that phenomenon.

A reasonable shift of the duty cycle is set to 56/44 and a redesign of the new transformer is needed. The new one is constructed width an *E18* core to increase the inductance and to prevent saturation. Also a capacitor (150 nF) is added to the AM-signal transformer at the *UC1901* to reject DC-offseted current that arise with a non-uniform duty cycle. From the calculation sheet, the new transformer with the *3E6* material resulted in table 11.1 [29].

Table 11.1: The new AM-transformer due to duty cycle variations.

Transformer	**Turns N**	**L [mH]**	**Material/Core**	I_{sat} **[mA]**	**Sim** $I_{L,peak}$ **[mA]**
AM synchronous	36:36:36	14.06:14.06:14.06	3E6/E18	18.4:18.4:18.4	0.63:5.3:5.3

The logic circuit in figure 11.1 has a square wave input signal which is generated from the comparator with a frequency of $2f_s$. The pulses enter several NAND gates, where they are firstly high pass filtered to get a clear 1 and 0 state. The logic gates trigger on both rising and falling edge of the square input signal and is combined at the output (T). This results that the logic circuit double the frequency set by the square signal to $4f_s$ and figure 11.2 shows the behaviour from input to output. The output (T) can later be transferred to the secondary side over the clock transformer and enters a toggled D flip-flop with the input (v), see figure 11.1.

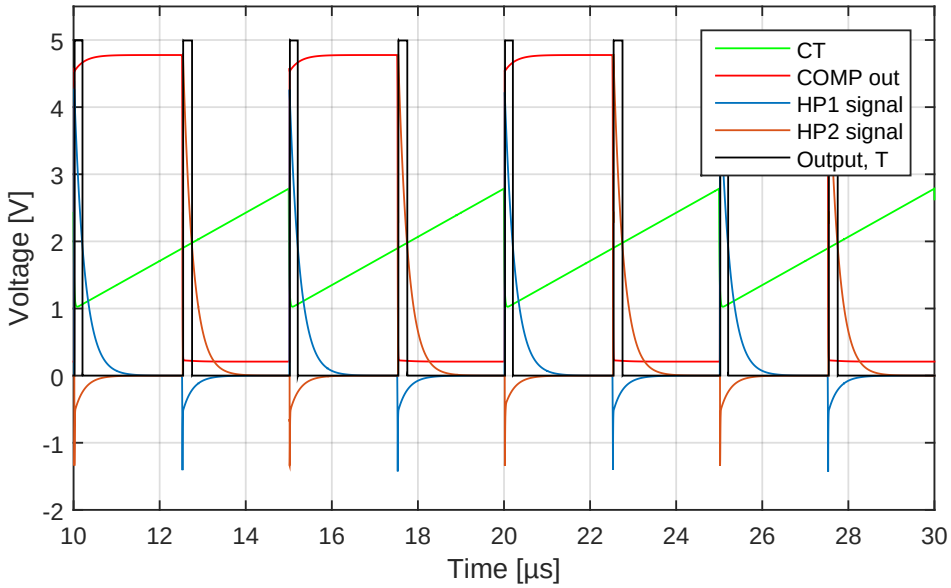


Figure 11.2: Simulation of a double frequency circuit with logic elements.

Although this implementation will give the double switching frequency, it can not guarantee a 50 % duty cycle which might lead to saturation of the AM-transformer at too high duty cycle variation. An accurate 50 % duty cycle with the double switching frequency is feasible to design for future operation, but it will increase the complexity and additional components.

11.2 The New Circuit Board with the Feedback Alternatives

The new circuit board would be constructed with one DC/DC converter, i.e. one *UC1825*, and several feedback methods. Surrounding components on the original circuit board that is not essential for testing the feedbacks have been removed. The different feedback alternatives are designed so that each feedback can be switched by connecting/removing resistors, i.e. resistors act as switches. The PCB will not be a qualified flight circuit board but rather a simple green circuit board as the function is in focus.

To receive cost quotations of a 16 layers PCB, the PCB-layout was sent to several PCB-manufactures. Unfortunately, the received cost quotations revealed in too high costs for the available budget. So the outcome became to not order any PCB. The major costs were due to few ordered PCBs and several layers which were costly. One of the cost quotation ended up in £4160 for two boards, which correspond to approximate 55 000 SEK at today's currency. Note that the cost quotations can firstly be estimated after a complete PCB-layout that is based on the CAD-design.

Although, no circuit board was ordered, the layout and CAD-design are available for future development. The new circuit board PCB-layout and the feedback CAD-design are available in appendix F.

Under the current circumstances, the decision was made to build one of the alternatives on a separate board that could later be implemented to the original PCB shown in figure 4.3. One possible option could be to redesign the feedback CAD-design into smaller PCBs with fewer layers and then implemented them to the original board. But as the CAD-design and PCB-layout will take more handling time and work, the decision was made to build the load design on a stripboard. Components (commercial and space) available at RUAG Space stock will be used to avoid the lead time for orders.

11.3 The Load Feedback Circuit Board

The first alternative to build would be the load alternative due to its simplicity and also as there is a need for independence of the *UC1901*. Even as the symmetrical load design may probably have better performance than the first one, it will be complicated to build on a stripboard.

As planar transformer is obviously not feasible for stripboards, a discrete transformer will be used. The discrete transformer has been wounded by hand with approximate the same inductance given in table 7.4. The core material *3E6* that would have been used for the planar model *E14/E18* (E-core) is replaced with a RM8-core with the material *N41*, which has an A_L-value of 4100 nH/1000. It resulted in 2x34.5 turns and 23 turns which correspond very well with (7.2). The inductances were verified with a LCR-meter at 100 kHz.

The CAD-design of the load alternative is based on the simulation profile and necessary modifications have been made to establish a working circuit. Figure 11.3 shows the current CAD-design of the load alternative and figure 11.4 the circuit board in reality. The real circuit board is built with a mixture of commercial– and space components. Notice that for all the commercial components used here, there exists a corresponding space qualified component. The operation of commercial– and space components is more or less identical.

The performance and operation of the load circuit are presented further in section 12.2.

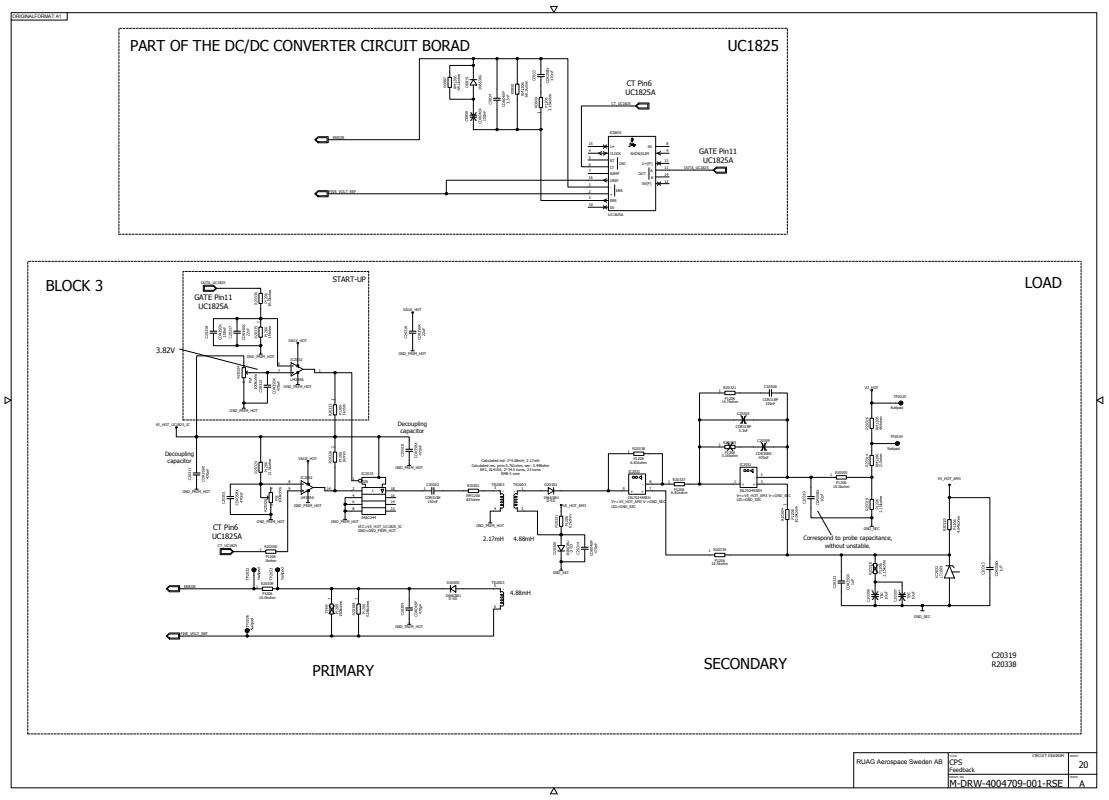


Figure 11.3: The CAD-design of the load feedback alternative.

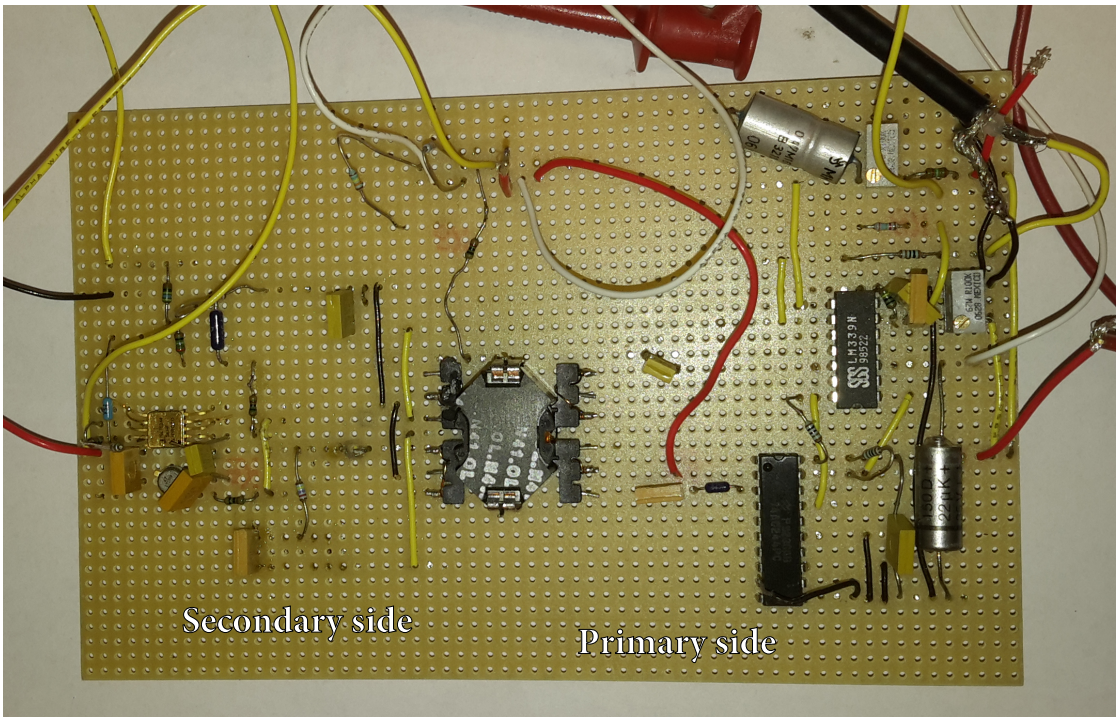


Figure 11.4: Load feedback circuit on a stripboard.

11.4 A Price Comparison Between Space– and Commercial Components

The original circuit board use obvious space compatible components, but for evaluation and due to costs, similar components are going to be used for the new circuit board. Some components might be space quality depending on the current stock at RUAG Space. Table 11.2 shows a list over components used in the designs as well as a comparison in price for other components. Note that the price is a variable factor and stated here is an estimation to give a feeling of the difference between space– and commercial components.

Table 11.2: Price difference between space components and commercial components.

Function	**Space Component**	**Component**	**Space Price/Price [SEK]**
AM-modulator	UC1901-SP	UC3901	2000/60
PWM modulator	UC1825-SP	UC3825	2040/50
Buffer	54AC244	74AC244	1575/7
D flip-flop	54AC74	74AC74	1560/6
NAND	54AC00	74AC00	1570/5
Operational amplifier	ISL70244SEH	LT1490A	1661/60
Comparator	LM139	LM339N	1500/6
2.5V Reference	LT1009	LT1009	1200/15
Diode	1N6638U	SB3100	324/5
MOSFET (PWM)	IRHNJ57130	FDMC3612	4029/10
BJT	2N3700	2N3700	540/10
FPGA	RTAX2000S 624-CGA	XC6SLX4	204 580/300
FPGA (low power)	RTAX2000SL 624-CGA	-	141 725/-

From the findings in section 6.2.1, digital processing and filtering do not pay off due to high cost of FPGAs. But if there was a FPGA available for other purpose, some I/O:s can be used in that sense to make a digital solution feasible.

12 On-board Verifications of the Feedback Alternatives

A feedback alternative is now available and in the following sections are verifications and tests performed on the load feedback presented, but first a network analyzer measurement from the original design.

12.1 Network Analyzer Measurement of the Original Design

An analysis of the feedback response in frequency domain is of interest for determining the stability of the system, i.e. locate poles and zeros as well as to establish the bandwidth. The test was performed on the existing circuit board called *CPSS2*, see figure 4.3.

To sweep over a range of frequencies, a network analyzer *HP 4395A* was used. It sweeps the frequency meanwhile it measure the gain as well as the phase of the system. The outcome from a theoretical analysis and a network analyzer (NA) measurement of the transfer function can be seen in figures 12.1 and 12.2. More detailed information of the theoretical analysis can be found in appendix C.

The measurement is from the secondary voltage node $V3\_HOT$ to Pin 3 at the *UC1825*. As can be seen in figure 12.1, the NA measurement was performed from 100 Hz to 1 MHz. Frequencies $> 10^6$ is not of interest as the DC/DC converter operates below 1 MHz. Different magnitudes of the injected signal were performed, from -40 dBm to 10 dBm with a step of 10 dBm. The results with too high magnitudes (0 dBm) resolved in a sudden drop of gain in the bode diagram and affected the system. With that in mind, -20 dBm was selected and the results are plotted in the figures below.

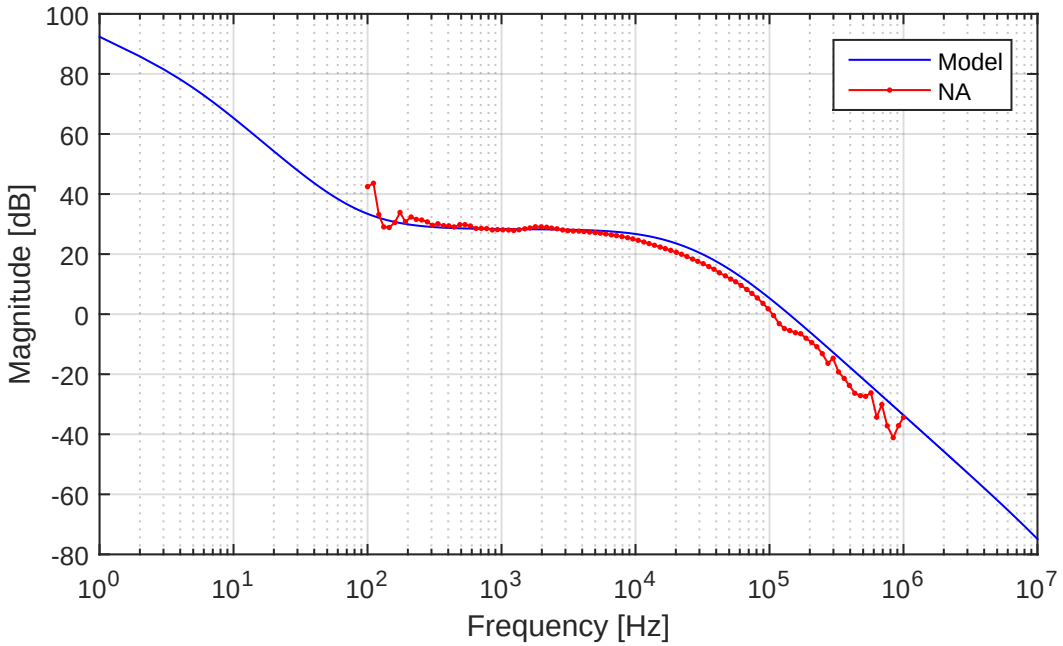


Figure 12.1: Bode diagram of the theoretical model and network analyzer (NA) gain for the present feedback path from $V3\_HOT$ to Pin 3 at the *UC1825*.

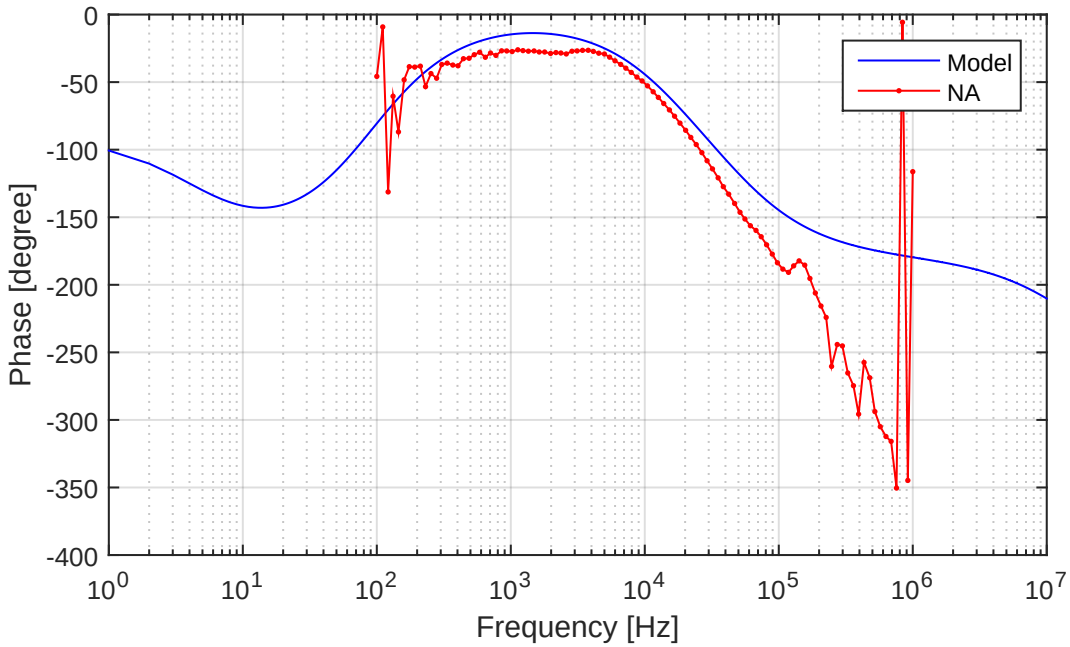


Figure 12.2: Bode diagram of the theoretical model and network analyzer (NA) phase for the present feedback path from $V3\_HOT$ to Pin 3 at the *UC1825*.

From the above figures, a correlation between the theoretical model and the measurements performed by the network analyzer can be seen, but there also exists some deviations that have not been located in the theoretical model. From the open loop system showed a small negative phase margin which would implies an unstable system, but as this is only a part of the system, the entire system needs to be evaluated to determinate the operation state. This is described in the following part.

During the setup with the network analyzer, a closed loop frequency sweep was performed on the complete system. The result is available in figure 12.3. The input had a magnitude of $-20\,\mathrm{dBm}$ and a load of 1 A at $V3\_HOT$. It resulted in a bandwidth of 5.5 kHz and a positive phase margin of 80°. Hence, the current system is stable, as expected.

Figure 12.3 states that for any injected errors in the converter above 5.5 kHz will be attenuated, i.e. frequencies below 0 dB. The collected data at low and high frequencies respectively showed fluctuations which depend partly on different injection levels. For example at low frequencies the injection level is too low to get an accurate measurement as the NA measures the ratio of output vs input. In the NA measurement figure 12.3, the phase crosses the 360° level and shifts 180°.

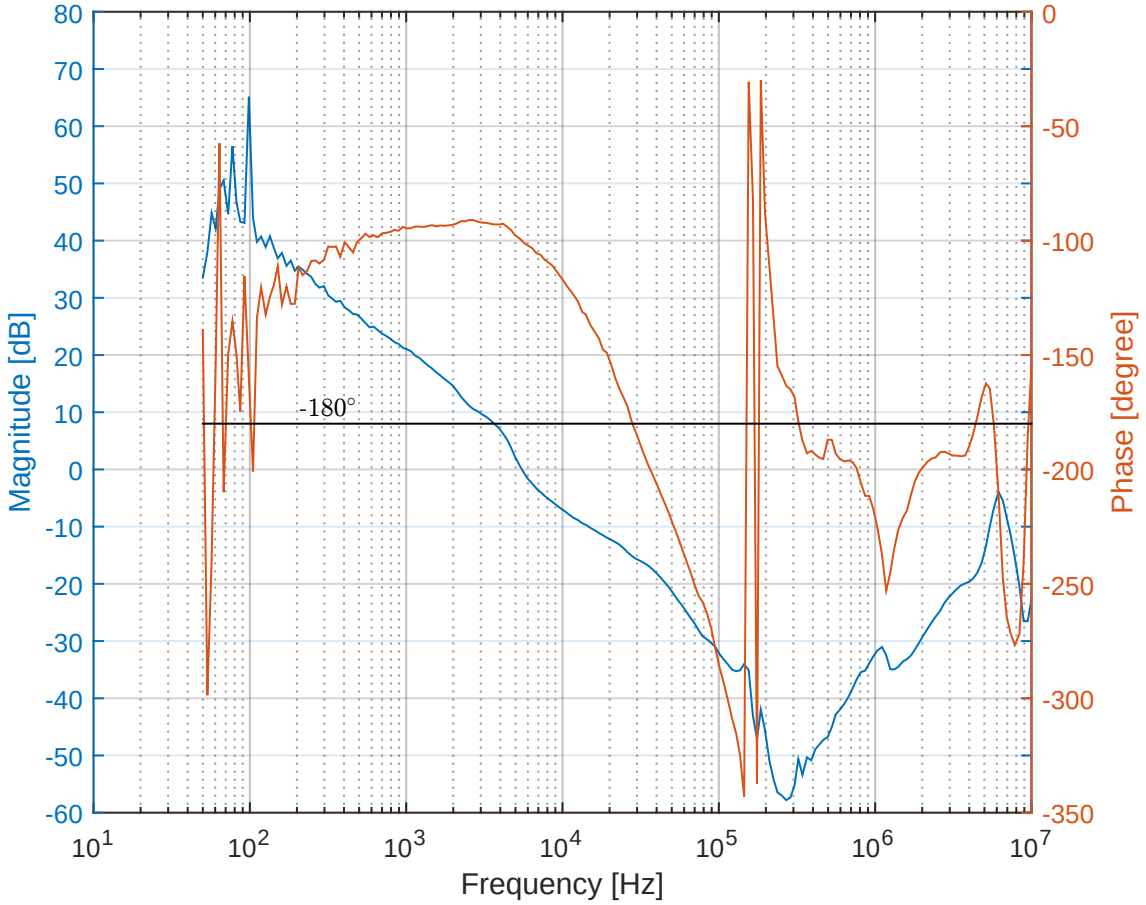


Figure 12.3: Bode diagram of the complete system performed by a network analyzer from $V3\_HOT$ to $V3\_HOT$.

12.2 The Load Feedback Results

The prototype load feedback in figure 11.4 started with verifications of the circuit externally with the clock signal as input. At first the prototype is DC-coupled although it tends to operate in AC-mode when implemented.

The clock signal is captured from the original circuit board Pin 6 *CT* at the *UC1825* and is transferred via a coaxial cable which had a capacitance of 340 pF. The switching frequency of the converter is set by capacitors connected to Pin 6 and this created a new switching frequency of approximate 530 kHz with the coaxial cable. That led to that the coaxial cable was replaced with an existing capacitance on the circuit board.

The first approach was to use a radiation hardened operational amplifier *ISL70244SEH* as comparator at a high DC-gain, but that did not fulfilled the operation behaviour. With that in mind a standard component *LM339N* was used instead and shall later be replaced with a space compatible comparator, example *LM139*. The *LM339N* use the single supply voltage $VAUX\_HOT$ where the output is sourced to 5.1 V, corresponding to the *UC1825* reference

voltage. With some adjustment, 50 % duty cycle pulses were achieved at Pin 14 at the *IC2032*, see figure 11.3.

At the secondary side, the voltages were generated by using power supplies to verify its operation behaviour. The reference 2.5 V is compared with scaled $V3\_HOT$ at the amplifier *ISL70244SEH*. The second operational amplifier just inverts the signal to achieve right output sign. At no error present (loaded), a small negative offset was seen from the 5.1 V reference and at increased error (unloaded) resulted in an increased voltage on the primary output. Namely, the operation of the load feedback was satisfied.

With a couple of fixes the entire circuit worked as in the simulation of the alternative. A step was injected at the secondary side, see figure 12.4. The response times were hard to distinguish due to the high voltage ripple which with approximation gave a rise time of 650 ns and a fall time of 10.5 μs.

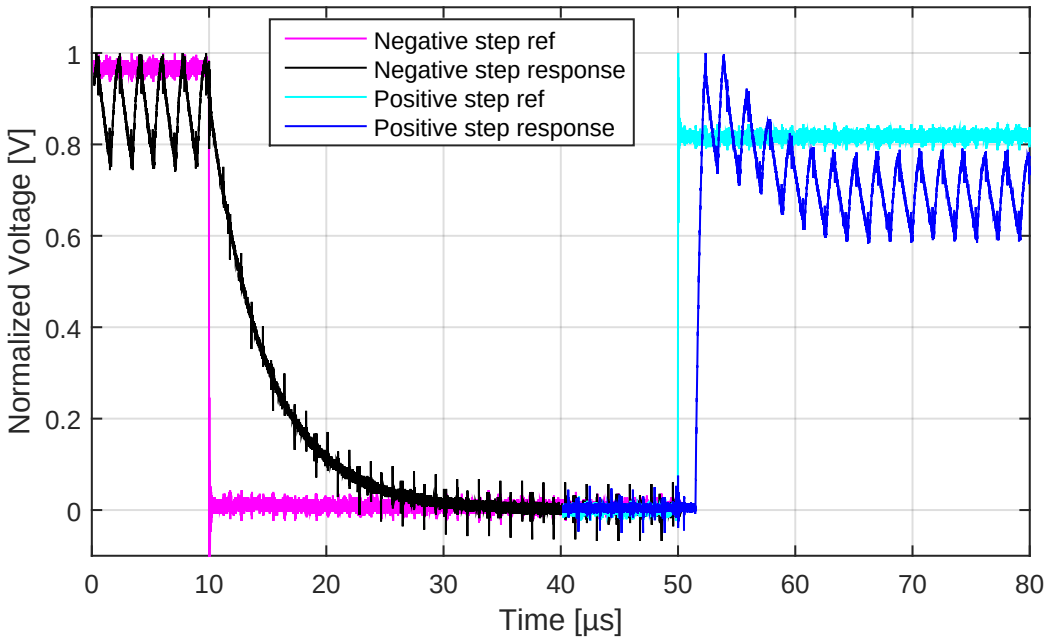


Figure 12.4: Step response of the load feedback from $V3\_HOT$ to the primary output $TP2033$.

12.2.1 Implementation of the Load Feedback

By disabling the present feedback solution on the circuit board (the *UC1901*), the load feedback could be connected. An amount of long cables (compared to PCB tracks) were necessary to join the two circuit boards at specific nodes. This consequently makes the system more sensitive to interference.

To obtain a stable system at start, the same compensation nets as in the original feedback were used, i.e. the same poles. During the first start-up of the DC/DC converter with the load feedback, it showed no voltage increase on the secondary side and thereby no functional system. One of the reasons when investigating the start-up sequence using an oscilloscope was that saturation

occurred on the error Pin 3 at the *UC1825*, which triggered a protection that shut down the converter. The reason was that during start-up the square pulse at the primary winding will be directly coupled to the output winding that sense a large error such as a protection will be enable and shut down the converter. This is a consequence as the secondary side has not been loaded to drag down the error at the start (no secondary voltages).

In the current feedback with the *UC1901* this problem is not available as it starts to operate when a minimum supply voltage is reached, like a soft start and has no directly coupling to the primary side as in the load alternative.

This problem is solved with a start-up delay circuit that controls the enable Pin 1 of the buffer *IC2033* for the square pulses, such that the secondary voltage can increase, see figure 11.3. The start-up circuit use a comparator with the inputs from Pin 11 at the *UC1825* and a fix reference voltage. During start-up, the gate voltage increases and when it reached the fix reference, the buffer is enabled and square pulses are injected into the transformer, i.e. the square pulse is delayed. To hold the enable pin activated during normal operation a large capacitor is connected to the comparator input of the gate pulses Pin 11. A start-up event is available in figure G.1.

An observation at too large time delays of the start-up circuit resulted in that an OVP (Over Voltage Protection) was activated as the output $V3\_HOT$ reached 3.7 V and shut down the converter.

After several start-ups, the load feedback finally passed the start-up procedure and began to regulate the voltage and it operated in a stable condition. An overview of a stable condition setup in available in figure G.2. The voltage $V3\_HOT$ was in fact regulated to the same voltage level as in the original feedback with the *UC1901* to 3.29 V without any optimization.

The load feedback circuit is now operational and under the stable operation point, the following output in figure 12.5 was achieved. Note that the circuit is now AC-coupled. A relatively large ripple of 565 mV was noted which is filtered to a level of 117 mV at the *UC1825* EAOUT. Part of the ripple propagates through the circuit such that the $V3\_HOT$ variate with 246 mV.

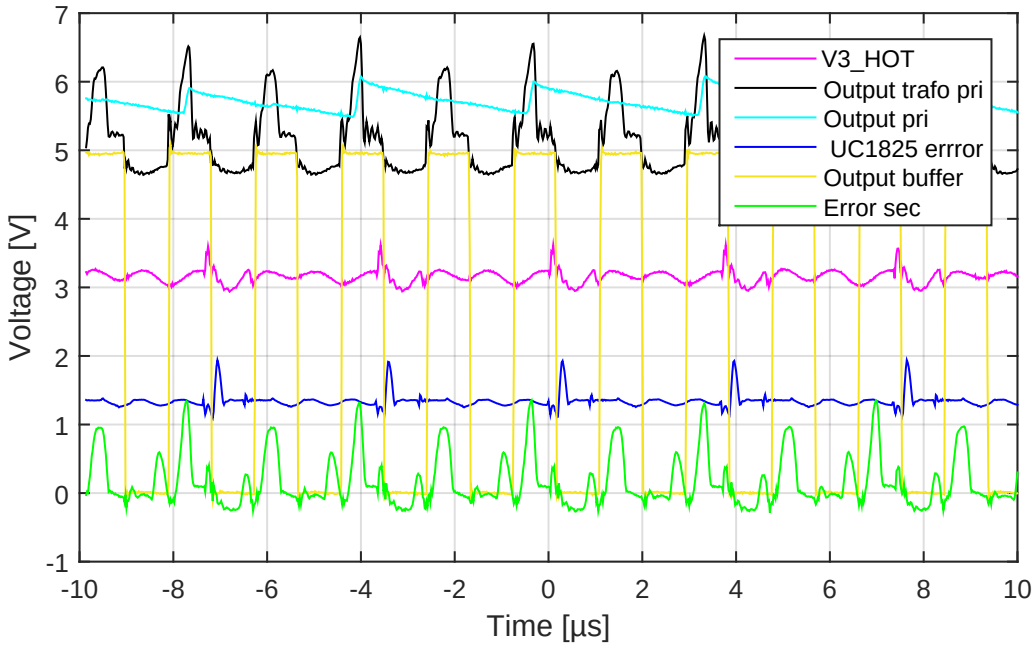


Figure 12.5: The Outputs from the load feedback circuit at steady state when connected to the original DC/DC converter.

A stable closed loop network analyzer measurement of the DC/DC converter showed a phase margin of 87° and a bandwidth of 917 Hz, see figure 12.6.

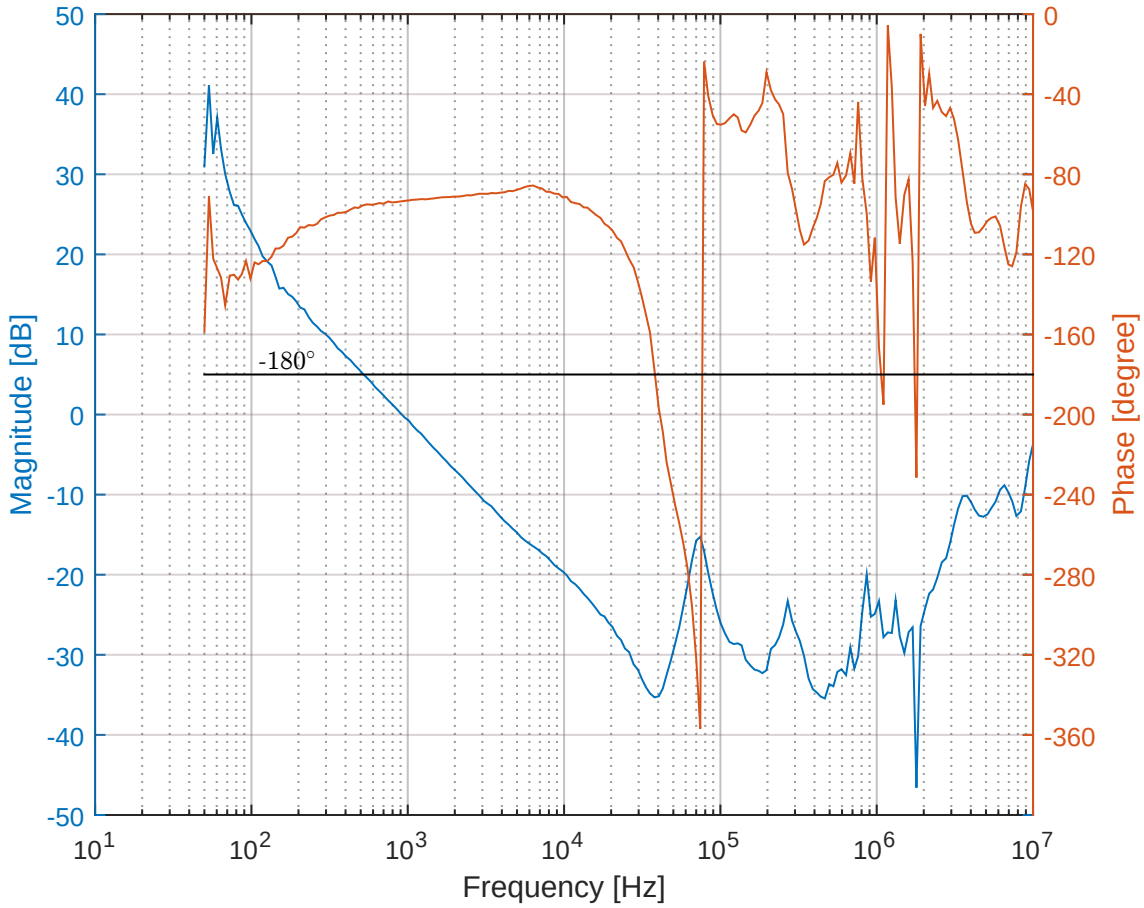


Figure 12.6: Bode diagram of the complete system with the load feedback alternative at a stable operation point from $V3\_HOT$ to $V3\_HOT$.

12.2.2 Optimization of the Load Feedback

To improve the load feedback in terms of performance such as bandwidth of the DC/DC converter, optimization was needed. Instead of testing different compensation networks manually, an optimization tool was used. From the network analyzer measurement of the DC/DC converter, the two compensation nets present in the feedback (correspond to A. and C.) are calculated/removed of their influence in the optimization tool and can be replaced by a number of combinations from pre-set values to gain improved parameters.

The optimization tool outputs possible combinations of compensation nets which would increase the bandwidth as well as positive phase margin. A number of implementations of the new

networks were made, but all ended up in an unstable operation point in the form of a ringing sound from the converter and no constant trigger occurred on the oscilloscope.

A closer investigation of the network analyser measurement showed that there existed an unwanted zero characteristic at around 13 kHz, see figure 12.6. And with the new parameters bode diagram in the optimization tools, see figure G.3, revealed that there exists two zero crossing. Where the second zero crossing causes a positive gain which might amplify unwanted signals in the system and cause instability.

A test revealed also that at different orientation of the long cables between the two circuit boards influenced on the system, see figure 12.7. Case #1 is with all cables together and case #2 under normal orientation. The inductance in one cable lies around 300 nH. Case #1, indicates an increased inductance compared to case #2, approximate 10 dB difference. The zero can be characterized by $(j\omega X + 1)$, but is more complicated in the reality, which is an unwanted affect that limits the optimization tool. At the current state, further optimization would not be useful as it will need to be re-optimized for a real implementation on a PCB. Due to this phenomenon further improvements are cancelled.

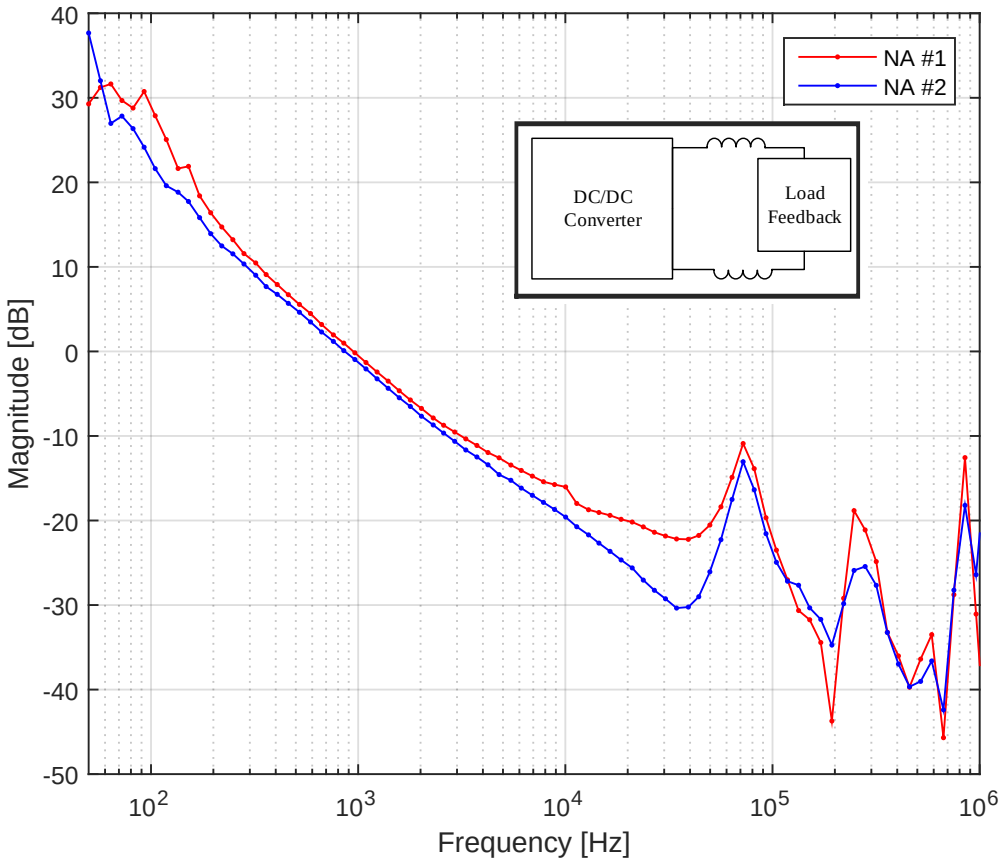


Figure 12.7: Bode diagram of the complete system with different configuration of the long cables from $V3\_HOT$ to $V3\_HOT$.

12.3 A Comparison Between the Feedback Alternatives

Of all the alternatives, the following two feedbacks: original feedback with the *UC1901* and the load feedback are the ones that can be compared from a measured point of view. An overall review of the two shows that both are able to operate at a stable point with the present DC/DC converter. From the specified quantities in table 7.3, the following parameters are summarized in table 12.1.

Table 12.1: Measured parameters between the original feedback and the load feedback.

Parameter	**Original**	**Load**
V3_HOT ripple	162 mV	246 mV
Demodulation stage ripple	300 mV	565 mV
EAOUT Pin 3 ripple	103 mV	117 mV
Dynamic range	2.4 V	3.4 V
Bandwidth (closed loop)	5.5 kHz	1 kHz
Phase margin (closed loop)	80°	87°

The load alternative ripple turns out to be higher than the original, especially in the reconstruction stage. The main influence of the ripple comes from the signal appearance in the transformer, see figure 12.5 curve "output trafo pri". The shape appears a bit strange and was expected to be more towards a flat shape, this effect might come from the operation of the amplifier with combination of leakage inductance in the transformer. In case with the *UC1901*, an almost square pulse is achieved. By trying a different operational amplifier the signal shape became more similar to a square signal, but the peak was still present and thereby the ripple. This indicates that the behaviour comes from the operation of the secondary side and counter measurements are needed for the load feedback. Where one would be to use the symmetrical load design, where the BJTs form the shape of the signal and not the operational amplifier.

The closed loop measurement of the system showed good phase margin in both cases, but lack of bandwidth for the load alternative. Note that the comparison is made with an optimized alternative and a non-optimized alternative.

From the project description a high bandwidth was wished for the feedback, while in the original setup, a limitation of the converter bandwidth is set by a dominate pole. The total feedback path from *V3_HOT* (A.) to Pin 3 at the *UC1825* (C.) is available in figures 12.8 and 12.9 for the load alternative and the original solution. A correct answer of the feedback bandwidth cannot be defined when comparing the alternatives, as it depends on how and under which circumstances the bandwidth is seen, different cases can be set. For example the bandwidth which the gain drop -3 dB from a certain constant gain or perhaps the bandwidth of the unit gain intersection, which can be discussed for the load alternative. To comment the figures, the original feedback has better characteristics, in terms of phase shift and gain decrease.

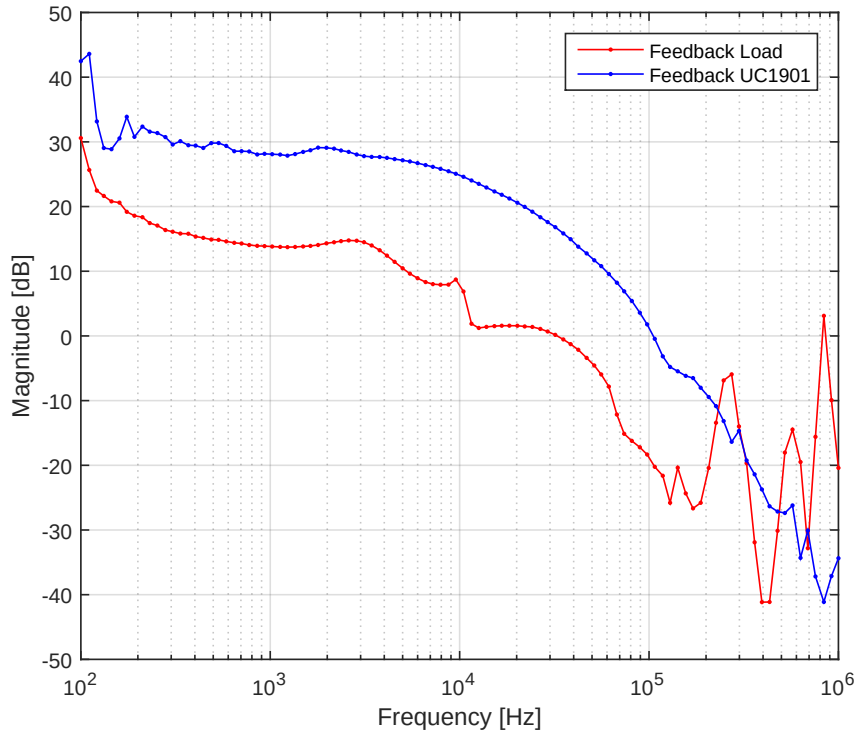


Figure 12.8: Bode diagram of the gain with both feedback alternatives from $V3\_HOT$ to Pin 3 at the *UC1825*.

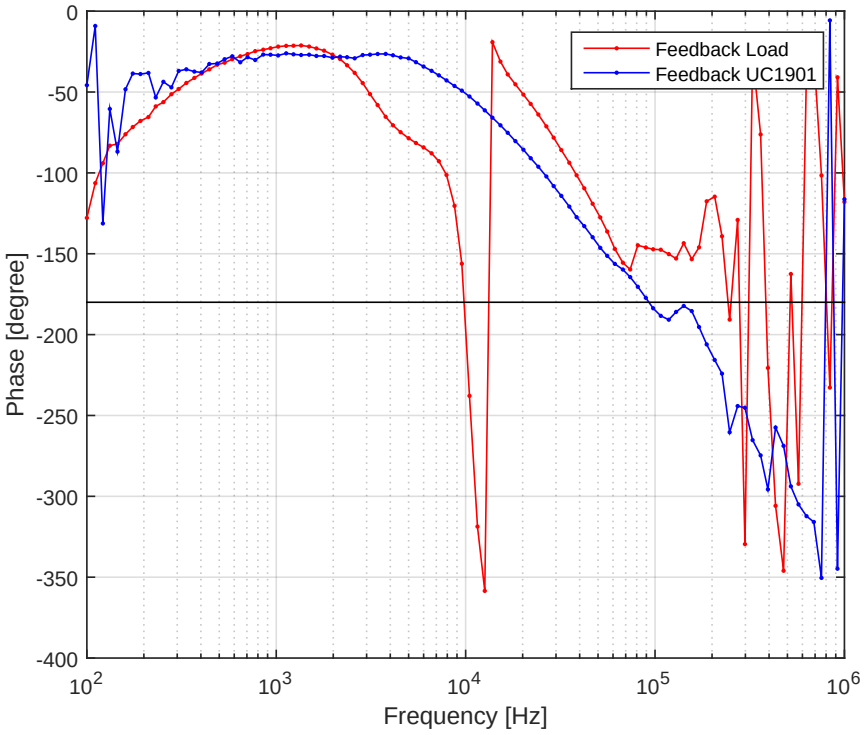


Figure 12.9: Bode diagram of the phase with both feedback alternatives from $V3\_HOT$ to Pin 3 at the *UC1825*.

Even if the other alternatives were not built and tested they had potential. In both the synchronous and asynchronous case, the ripple could be minimized with the extra winding and probably decrease the amount of filtering at the *UC1825*. Theoretically with the synchronous mode, mixed signals can be reduced as well as less filtering which can consequently lead to increased bandwidth.

In terms of costs of the new load feedback, more components are used and therefore a tendency to cost more, but the amount is insignificant if other aspects are concern as they are radiation hardened reliable compared to the *UC1901*. The power consumption would be minimal and comparable with the original feedback.

With an optimized load feedback alternative, one less integration could hopefully be achieved, where all integration would be located on the secondary side and only use a proportional gain at the *UC1825* (might need a small capacitor in pF for the ripple). This should give a significant increase of the bandwidth for the system. The load feedback will be constructed with simple radiation tolerant components (buffer) which are available from different manufactures and that gives the advantage on not being dependent on specific component and manufacture as with the *UC1901*.

The load feedback has shown that although the influence from the long connection cables that it is a working concept and also that it can be exposed for unwanted signals from the surrounding and still operates at a stable point. A comment, this alternative has only been tested in room temperature with a specific load and further development require except from optimization to be evaluated at different condition such as temperature, loads etc.

13 Conclusion

From the performed studies, we have seen different alternatives in case of transmission methods, mediums, simulations and real implementations. The report has shown a clear potential in the load feedback alternative or more specific the symmetrical load feedback alternative, i.e. proof of concept. Even though, the improved transformer design with the *UC1901* would almost certainly be an improvement with and without synchronous mode, it has not been tested.

The major advantages with the load alternative is that it consists only of simple, qualified and tested radiation hardened components and no dependence of the IC-unit *UC1901* radiation tolerance.

Both the load feedback as well as the synchronous clock with the *UC1901* can be implemented to the current DC/DC converter without too many changes. But for now, lack of optimization resulted in limited performance parameters for the load alternative, but ended up in a stable working feedback.

This concludes that two alternative feedbacks have been found: the load alternative by loading the secondary side and the synchronous clock design (*UC1901*) with the improved transformer, where one has been tested in reality.

13.1 Future Work

There exists a great potential of future work in case of optimization and PCB implementation. The next step would be to evaluate the clock design (*UC1901*) with the improved transformer as well as build the alternatives, especially the load alternatives, on a PCB to get rid of unwanted effects that arose. Furthermore, optimization of the symmetric load alternative might have great potential and might even lead to a sharp flight implementation in the future.

And perhaps someday, a load feedback might be available in a satellite DC/DC converter in outer space.

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A Example of CMOS Latch-up and Power MOSFET Burnout

Latch-ups are most applicable in CMOS semiconductors. Latch-up can occur when a single high energetic particle hit the CMOS and causes an ON-state in one of the parasitic transistors inside the CMOS circuit. This leads automatically that the other parasitic transistor turns ON, making a short circuit between the supply voltage VDD and VSS. Only a complete shut down of the power supply can set the COMS to normal operation state again. The effect of SEL can cause catastrophic damage, but there are ways to minimize the outcome, for example implementation of a current limiter or improved process steps to avoid the parasitic elements.

An example of the above concept can be if a particle strike into the substrate and induce a current at node x in figure A.1, which represents the electrical structure of a CMOS with a number of parasitic elements. The strike leads to a voltage build-up at node x that turns ON the transistor Q_n. The current I_n increases and creates a voltage drop at node y, resulting Q_p to ON-state. At this stage, a clear path from VDD and VSS is present and as I_p increases, the voltage at node x increases which in turn enhance the current I_n even further.

With a current amplification β greater than 1, consequently leads to a higher current built-up until maximum current flows through the CMOS structure. For a low power circuit, a restart is necessary to reach normal operation and for higher power circuits this might lead to a total burn out [2], [7].

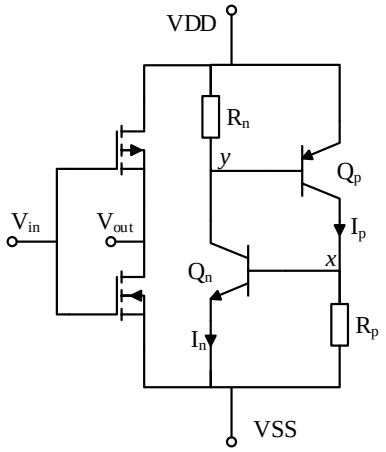

Figure A.1: Electrical representation of a CMOS with a number of parasitic elements.

SEB for a power MOSFET can be described from figure 2.1 as following. When heavy ions or energetic protons penetrate a power MOSFET structure, it creates an ionisation path of electron-hole pair. With a present electrical field, the electrons move towards drain and the holes towards source respectively. During the process a voltage drop occurs inside the p-region (R_B) and a current is generated which trigger a parasitic BJT. The parasitic BJT base open a path for the current between drain to source.

The ON-state parasitic BJT cause further electrons in the drain direction which collide with other electron-hole pair and cause avalanches. This chain regenerates an increased current to the parasitic BJT base and continues until a total breakdown of the whole transistor is established and ends up in a burnout.

To prevent SEB, the parasitic BJT base can be short circuited with the emitter in such a way that the voltage drop over R_B is minimized and ends up with only the body diode [2], [9].

B Transformer Calculation Sheet

Here, a transformer calculation sheet is presented for an *E14* core model with the core material *3E6* and also margins of the input parameters have been used. In figure B.1, the transformer is design for the synchronous AM-transformer used in the clock– and gate driver design.

		Global parameters												**Core type**																				
		Isolation between tracks [mil]							8					*Type*				E14																
		Isolation to PCB edge [mil]							24					*Window witdh [mm]*				3,28																
		Clearance to core [mil]							N/A					*MLT [mm]*				31,8																
		Temperature [deg C]							100					*Available width [mm]*				2,26																
Model																																	
			N1			**N2**			**N3**			**N4**			**N5**			**N6**			**N7**			**N8**									
			Prim			***VAUX***			***V12***			***V12***			***V6_5***			***V6_5***			***VN6***												
	Layer Cu thickness [um]	**# of turns**	**Track width [mil]**	**Track resistance [mOhm]**	**# of turns**	**Track width [mil]**	**Track resistance [mOhm]**	**# of turns**	**Track width [mil]**	**Track resistance [mOhm]**	**# of turns**	**Track width [mil]**	**Track resistance [mOhm]**	**# of turns**	**Track width [mil]**	**Track resistance [mOhm]**	**# of turns**	**Track width [mil]**	**Track resistance [mOhm]**	**# of turns**	**Track width [mil]**	**Track resistance [mOhm]**	**# of turns**	**Track width [mil]**	**Track resistance [mOhm]**	**Total occupied width incl. isolation between turns [mm]**	**Total occupied width [%]**
Layer 18	35																										
Layer 17	35																										
Layer 16	35																										
Layer 15	70	6	8	309																					2,24	99
Layer 14	70	6	8	309																					2,24	99
Layer 13	35	7	6	960																					2,29	101
Layer 12	35				7	6	960																		2,29	101
Layer 11	35				7	6	960																		2,29	101
Layer 10	35				7	6	960																		2,29	101
Layer 9	35				7	6	960																		2,29	101
Layer 8	35							7	6	960															2,29	101
Layer 7	35							7	6	960															2,29	101
Layer 6	35							7	6	960															2,29	101
Layer 5	35							7	6	960															2,29	101
Layer 4	35	7	6	960																					2,29	101
Layer 3	70	6	8	309																					2,24	99
Layer 2	70	6	8	309																					2,24	99
Layer 1	35																									
# of turns to wind		36			24			24			0			0			0			0			0			
Total # of turns		38			28			28			0			0			0			0			0			
Winding current [A]		0			0			0,3			0,3			2			2			0,05			0			
Total resistance [mOhm]		3155			3841			3841			0			0			0			0			0			
DC power loss [mW]		0			0			345,7			0			0			0			0			0			
Inductance		6,47	(mH)		3,51	(mH)		3,51	(mH)											**Assumed Rac/Rdc**			2			
Ae		1E-05			1,5E-05			1E-05												**Total power loss [mW]**			691,43			
AL [nH/turn]		4480			4480			4480																		
B_max		0,2			0,2			0,2																		
I_max		0,02			0,02			0,02																		

Figure B.1: Transformer calculation sheet for an *E14* core.

C Error Amplifier Model and Analysis of the Feedback Transfer Function

A differential amplifier or an error amplifier amplifies the difference between two input signals. In figure C.1, a general illustration of an EA is shown without the power supply to the amplifier.

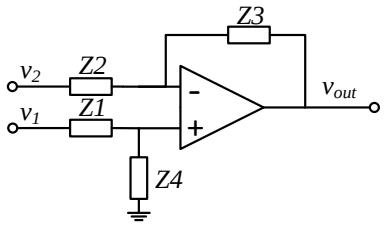

Figure C.1: A traditional differential amplifier.

By applying Kirchhoff's current law an expression for the given model can be derived as

$$v_{out} = \frac{Z4(Z2+Z3)}{Z2(Z4+Z1)}v_1 - \frac{Z3}{Z2}v_2, \tag{C.1}$$

where ZX is impedance and v_x voltages. By defining the differential voltage as

$$v_{diff} = v_1 - v_2 \iff v_1 = v_{diff} + v_2 \tag{C.2}$$

and the common mode voltage to

$$v_{com} = \frac{v_1 + v_2}{2} \iff v_2 = v_{com} - \frac{v_{diff}}{2}. \tag{C.3}$$

The result of inserting (C.2) and (C.3) into (C.1) results in

$$v_{out} = \left(\frac{Z4(Z2+Z3)}{Z2(Z4+Z1)} - \frac{Z3}{Z2}\right)v_{com} + \left(\frac{Z4(Z2+Z3)}{Z2(Z4+Z1)} + \frac{Z3}{Z2}\right)\frac{v_{diff}}{2}. \tag{C.4}$$

With impedance matched according to $Z4 = Z3$ and $Z2 = Z1$, it can be simplified to

$$v_{out} = \frac{Z3}{Z2}v_{diff} = \frac{Z3}{Z2}(v_1 - v_2). \tag{C.5}$$

The Common mode voltage in (C.4) leads to that a certain gain will influence on the output. Equation (C.5) clearly states that differential amplifiers should be used with matched impedances to avoid the effect from a common mode voltage.

In the current model with the *UC1901*, impedance mismatch occur. But the input v_1 consists of a constant voltage which is fixed and leaves v_2 to the only differential input. This can be modelled as in figure C.2.

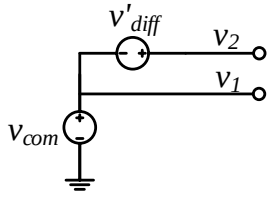

Figure C.2: Input model of the differential amplifier for the original feedback design.

The impedance $Z4$ is composed of a capacitor (C0843) and a resistor (R0858) in series, seen in figure 4.1. Due to DC-voltage, the capacitor acts as an infinite impedance, meaning open circuit. With this approach, KCL at negative input node result in

$$\frac{v_{com} - (v_{com} + v_{diff}^{'})}{Z2} + \frac{v_{com} - v_{out}}{Z3} = 0 \tag{C.6}$$

which can be reduced to

$$v_{out} = v_{com} - \frac{Z3}{Z2} v_{diff}^{'}, \tag{C.7}$$

where $v_{diff}^{'}$ is defined as $v_2 - v_1$.

Operational amplifiers tend to have high CMRR, where the *UC1901* has a CMRR of 80 dB and this concludes at high amplification that the differential signal only passes through the feedback path and therefore with a static value of v_{com} gives the transfer function

$$\frac{v_{out}}{v_{diff}} = -\frac{Z3}{Z2}. \tag{C.8}$$

Feedback Transfer Function

An analysis for the feedback transfer path was made with start from the secondary side: a differential amplifier (A), a low pass filter (B) and an inverting amplifier (C), see figure 4.1. The transfer function of the input to the *UC1901* can be defined according to (C.8) as

$$H_1(jw) = -\frac{1 + j\omega R_{R0828} C_{C0809}}{j\omega (R_{R0847} + R_{R0872}) C_{C0809}}. \tag{C.9}$$

From the diode detector, a low pass filter is created with the input resistance from the transformer as

$$H_2(jw) = \frac{1}{1 + j\omega R_{out} C_{C0806}}, \tag{C.10}$$

where R_{out} is assumed to be around 20 Ω. The last step is an inverting amplifier with a transfer function of

$$H_3(jw) = -\frac{Z_{tot}}{R_{R0822}}, \tag{C.11}$$

where

$$Z_{tot} = R_3 \frac{(1 + j\omega R_4 C_4)}{jw(C_4 R_4 + (C_4 + C_3) R_3) + 1 - \omega^2 R_3 R_4 C_3 C_4}. \tag{C.12}$$

The parameter values to the above equation are given in table C.1. From a maximum open loop gain and an internal compensation of the error amplifier *UC1901*, it has been seen that the transfer function start to decease at a rate of approximately −20 dB/decade at the intersection with the error amplifier curve, which happens at approximate 50 kHz. This has been implemented as a low pass filter expressed

$$H_4(jw) = \frac{1}{1 + j\frac{\omega}{2\pi 50k}}. \tag{C.13}$$

This sums up in a total transfer function of

$$H(jw) = H_1 \cdot H_2 \cdot H_3 \cdot H_4 \cdot 4, \tag{C.14}$$

where the factor 4 comes from the internal amplification inside the *UC1901*. The results are available in figures 12.1 and 12.2.

Table C.1: Parameter values used in the theoretical analysis.

Parameter	**Value**	**Parameter**	**Value**
R_3	68.1 kΩ	C_3	3.3 nF
R_4	3.16 kΩ	C_4	470 nF
R_{R0847}	464 Ω	C_{C0809}	150 nF
R_{R0872}	215 Ω	C_{C0806}	470 pF
R_{R0828}	14.7 kΩ	-	-
R_{R0822}	10 kΩ	-	-

D Delta Sigma Matlab/Simulink Simulation

A first order differential delta sigma simulation model is presented here using Matlab. A Simulink model is available in figure D.1.

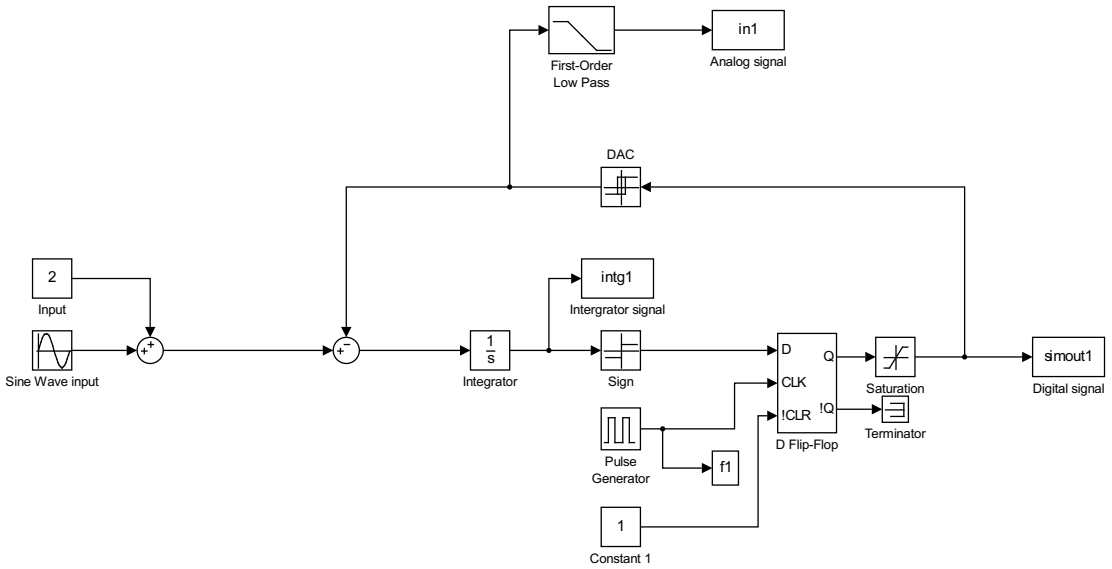

Figure D.1: First order differential delta sigma model.

The results seen in figure 9.2 was made from this model which had an input of 2 and was summed with a feedback represented as a 1-Bit DAC that can be either ±2.5. The error enters a integrator amplifier followed by a comparator element that send out ±1 to a clock D flip-flop.

The clock frequency must be at least the double of the message signal, i.e. according to Nyquist sample criteria to fully reconstruct the signal. In this simulation a 1.3 kHz clock was used and

a filter with cut-off frequency of 17 Hz. Next to the flip-flop a saturation block is used to scale the sign-signal to a digital signal. Without that block, ±1 will be the output, but clocked. The digital signal go through a 1-Bit DAC and back to the summation and from there to a low-pass filter to retrieve the input signal.

To verify its performance under AC-signals, figure D.2 shows an input of a sinusoidal signal with an amplitude of 0.2 V@200 Hz and a DC-offset of 1 V. The low pass filter had a cut-off frequency of 1 kHz and the D flip-flip was clocked with 1.3 MHz. As expected, the signal was retrieved with the same information. The phase shift that is present in figure D.2 is an effect from the delay time that is used to reconstruct the signal and it performs as foreseen.

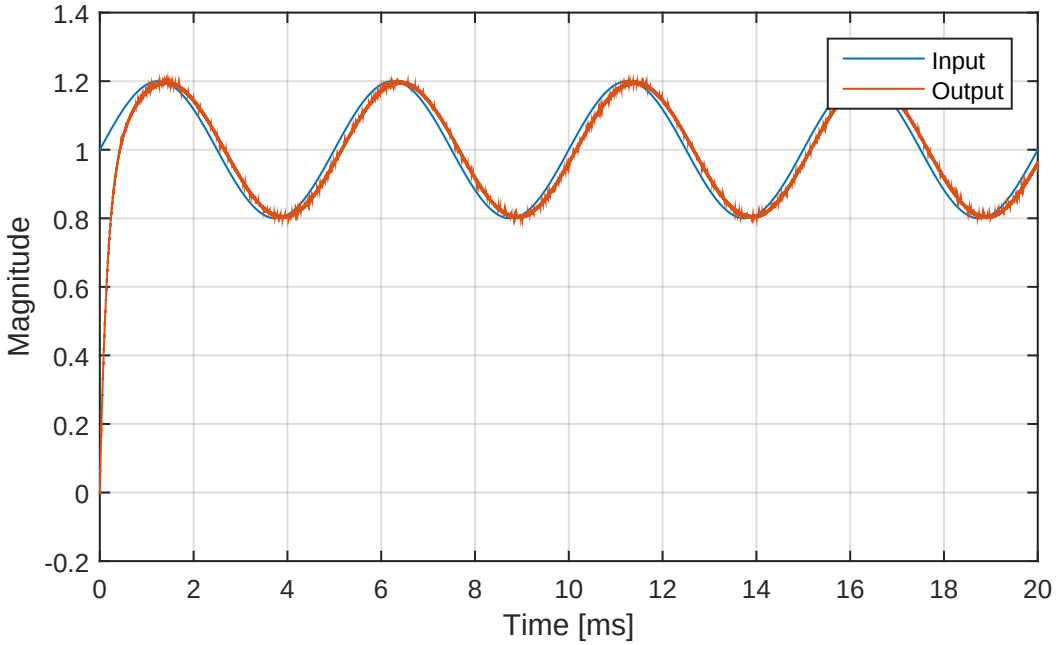

Figure D.2: Delta sigma modulation of an input AC-signal and the filtered output signal from the feedback loop.

The integration error in figure D.3 shows a clear picture of how the capacitor behaves in a delta sigma circuit. Here, the integrated error was at a DC-offset of 0.8 and a supply range of 10 V, i.e. ±5 V.

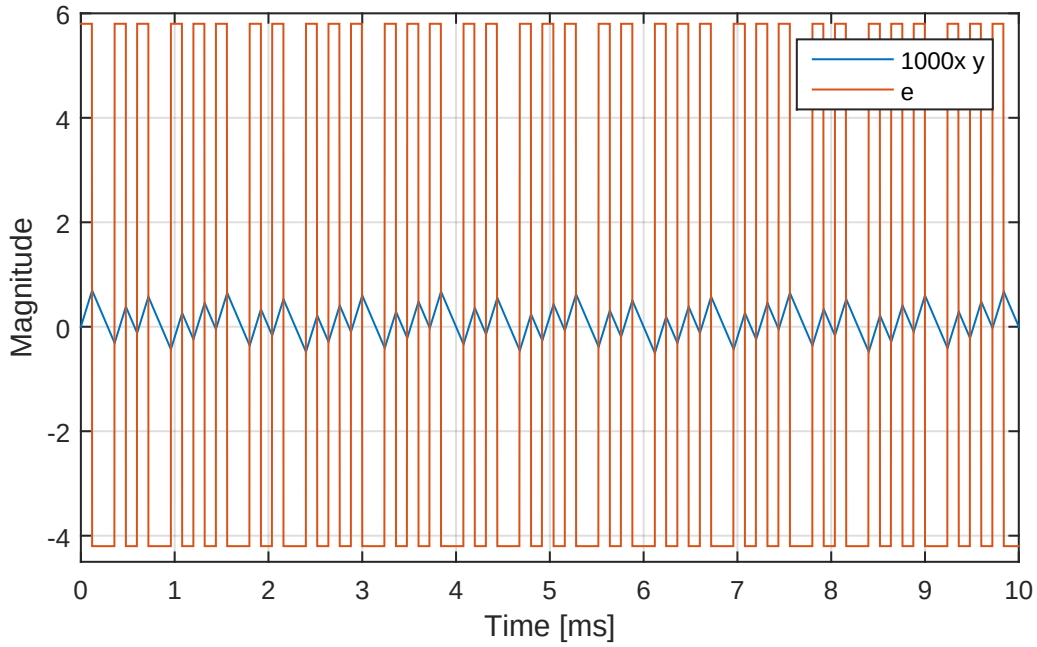

Figure D.3: The integrated error (blue) and the input error (orange) at a DC-offset of 0.8.

D.1 Delta Sigma Digital to Analog Converter

The continuous model of a DAC is similar to an ADC with some modification. The ΔΣ-DAC is more precise a DD-converter and a 1-Bit DAC. The action is to replace and connect the 1-Bit DAC in figure 9.1 to the digital filter and let the input be a digital signal.

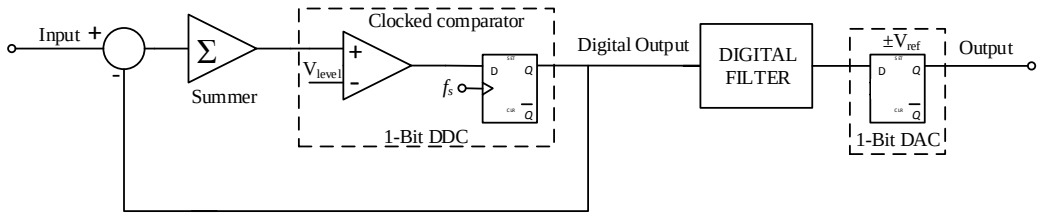

Figure D.4: Schematic model of a ΔΣ-DAC.

E Simulation Profile of a Symmetrical Load Feedback Alternative

Figure E.1 shows a PSpice simulation model of the symmetrical load design where the ripple resulted in less than 100 mV at the reconstruction stage.

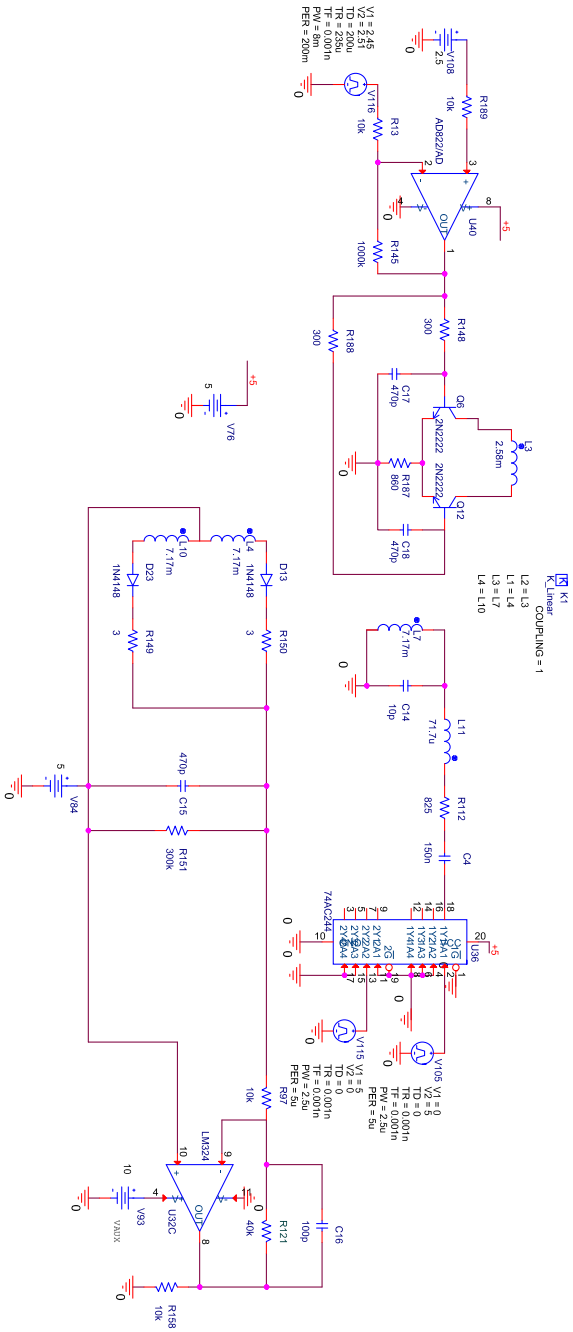

Figure E.1: Simulation model of a load design based on symmetrical behaviour.

F CAD-design and PCB-layout of the Planned New Circuit Board

The CAD-design is shown in figure F.1 of the feedback alternatives. The PCB-layout top view in figure F.2 and the back view in figure F.3 respectively. The DC/DC converter is not present in the CAD-design sheet due to company restrictions.

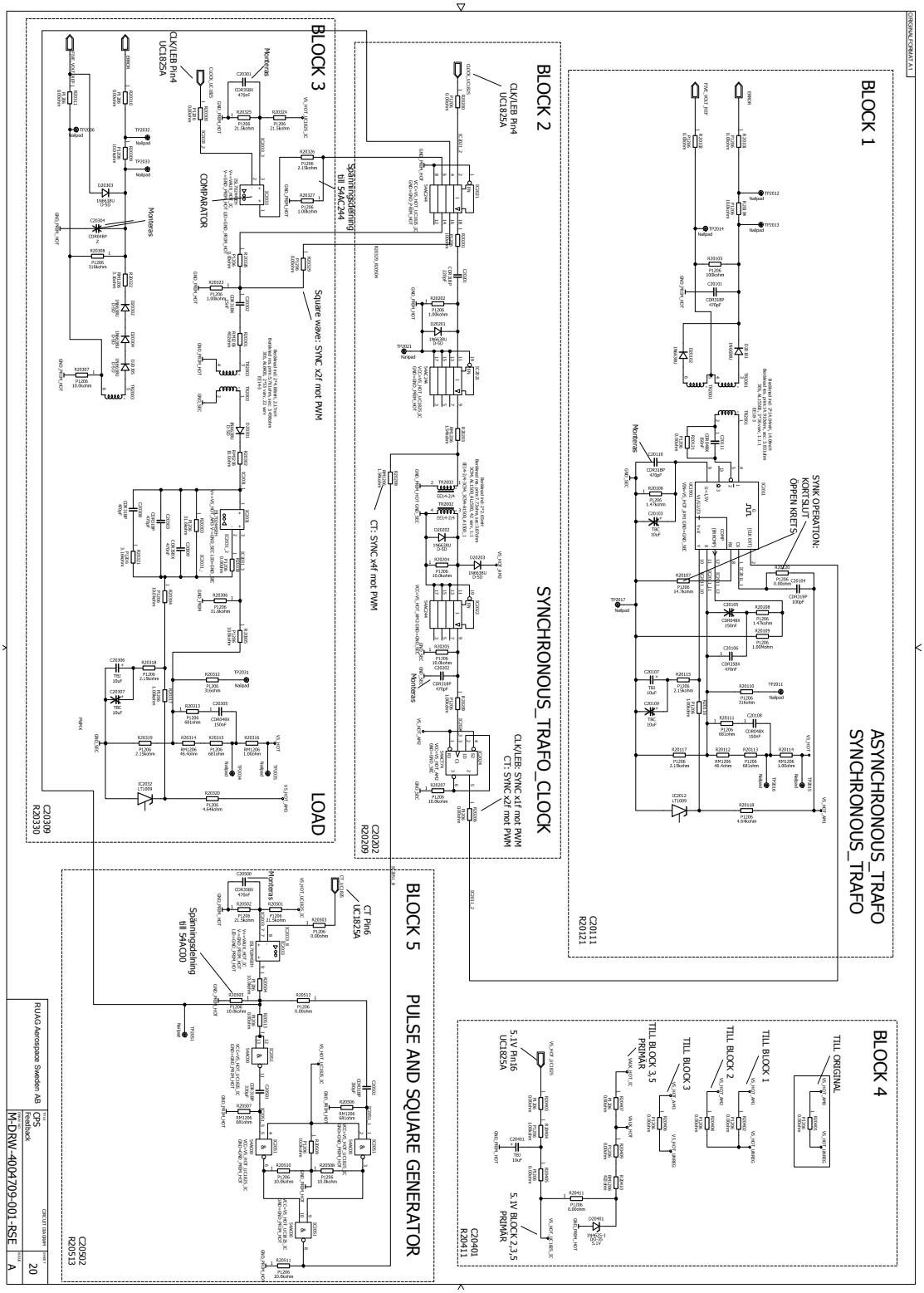

Figure F.1: The CAD-design of the feedback alternatives.

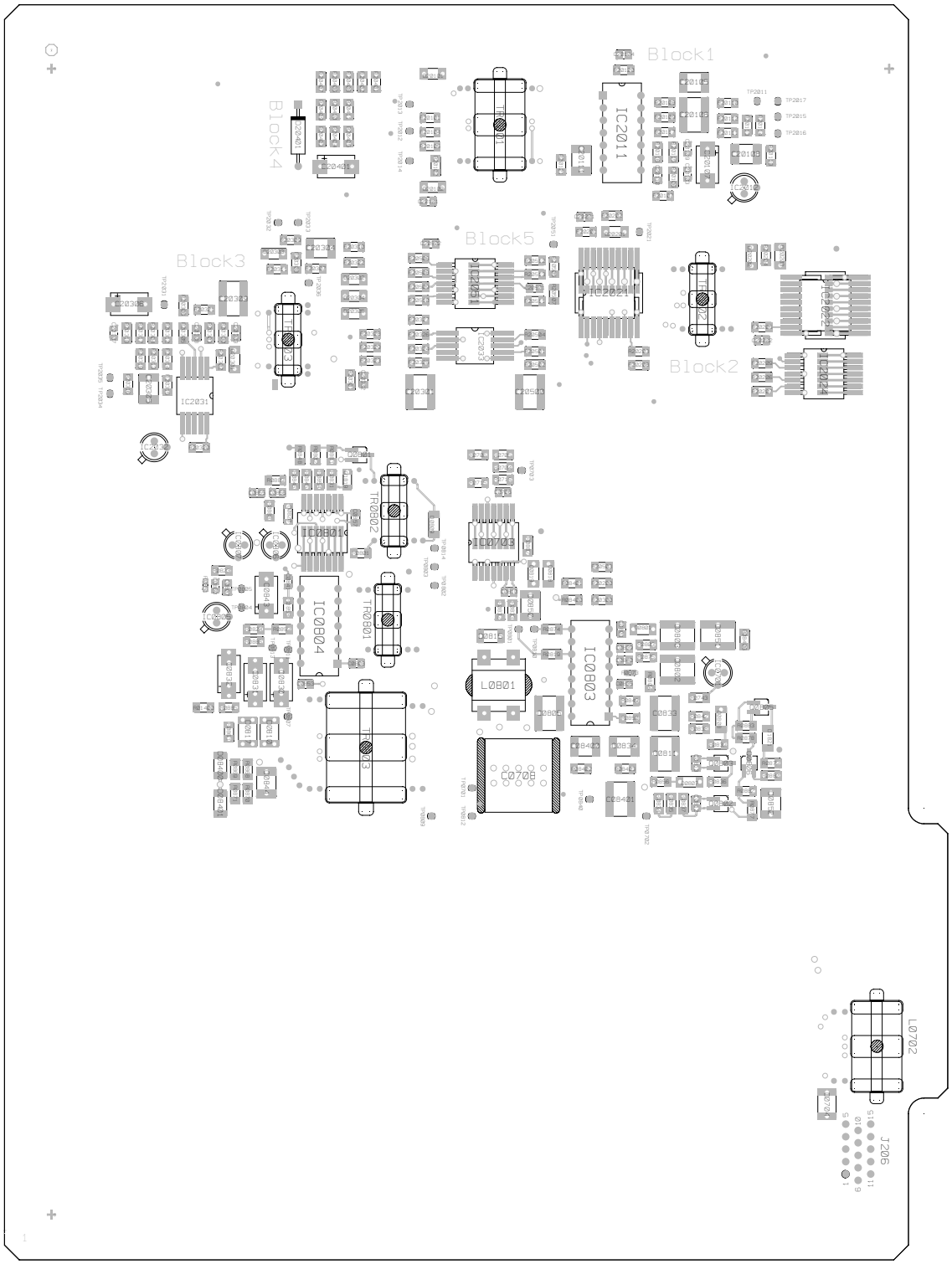

Figure F.2: PCB component side (top view).

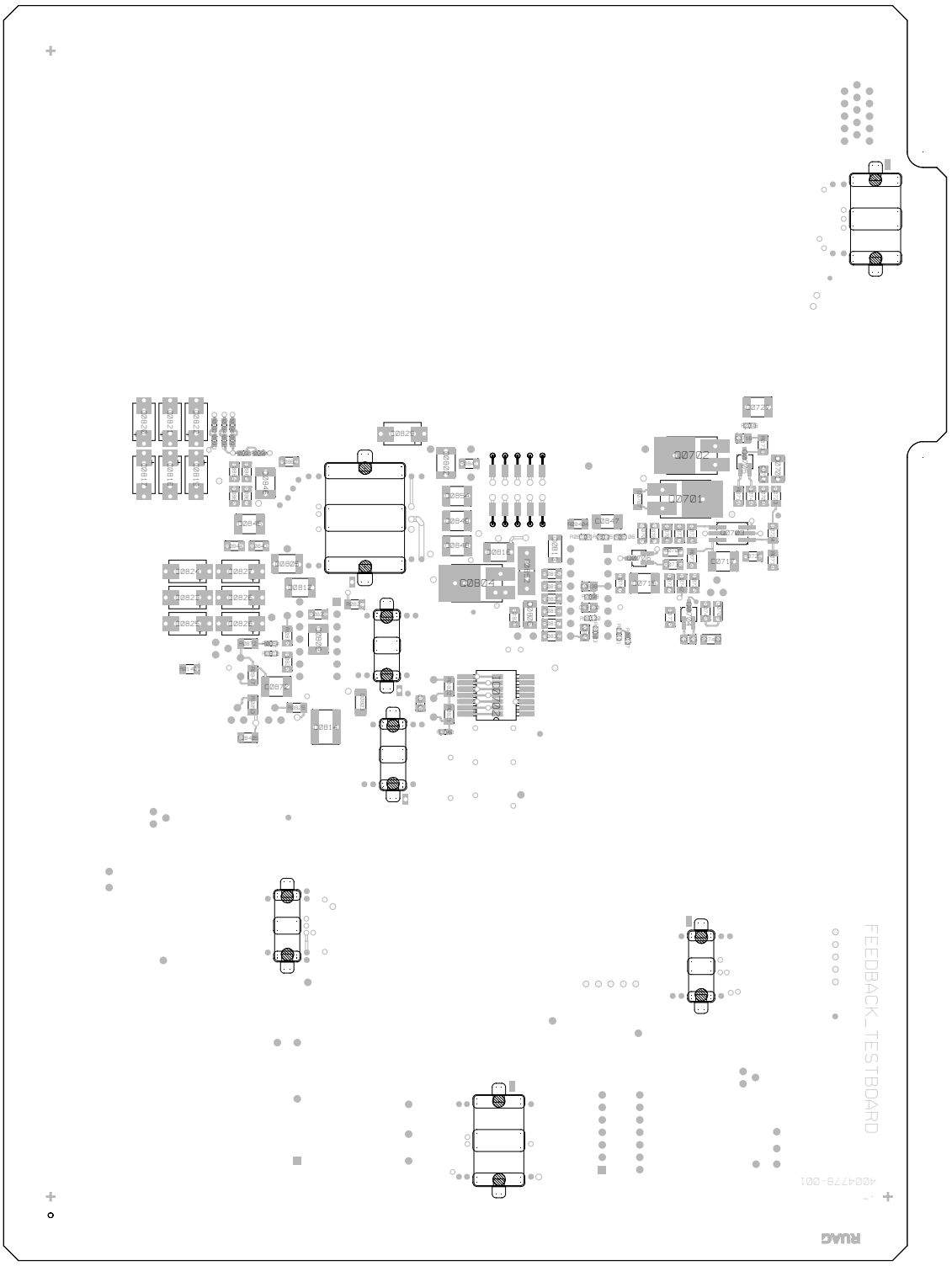

Figure F.3: PCB solder side (back view).

G Additional Data for the Load Feedback

A start-up event of the DC/DC converter can be seen in figure G.1, where the error clearly follows the soft start of the *UC1825* until the load feedback is activated. The delay time of the start-up (enable buffer pin) can be adjusted, but must be in the range in such a way that $V3\_HOT$ not reach 3.7 V nor the error voltage reach the protection level of 3.3 V. The total start-up is approximate 110 ms while the delay time is around 10 ms at the current setup.

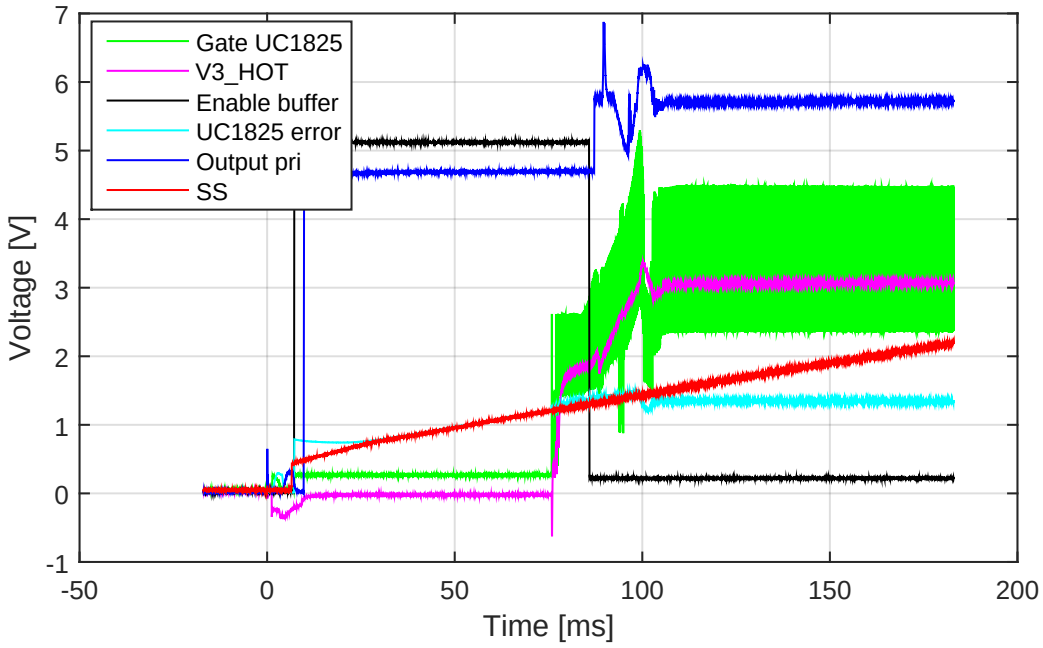

Figure G.1: A start-up event of the DC/DC converter with the load feedback circuit.

Figure G.2 shows an overview of the stable load feedback operation with the correct regulated voltages.

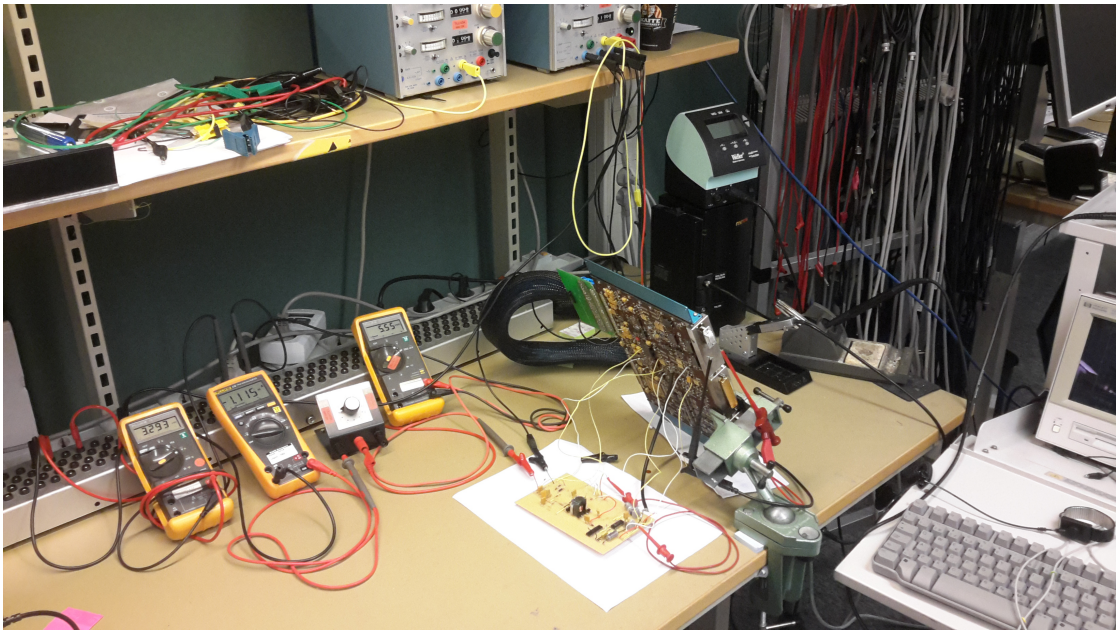

Figure G.2: The load feedback implemented on the original DC/DC converter and operation at a stable condition.

The optimization results of two different compensation nets can be seen in figure G.3, where the green curve reflects the DC/DC converter in a stable condition and the white the new optimized close loop curve.

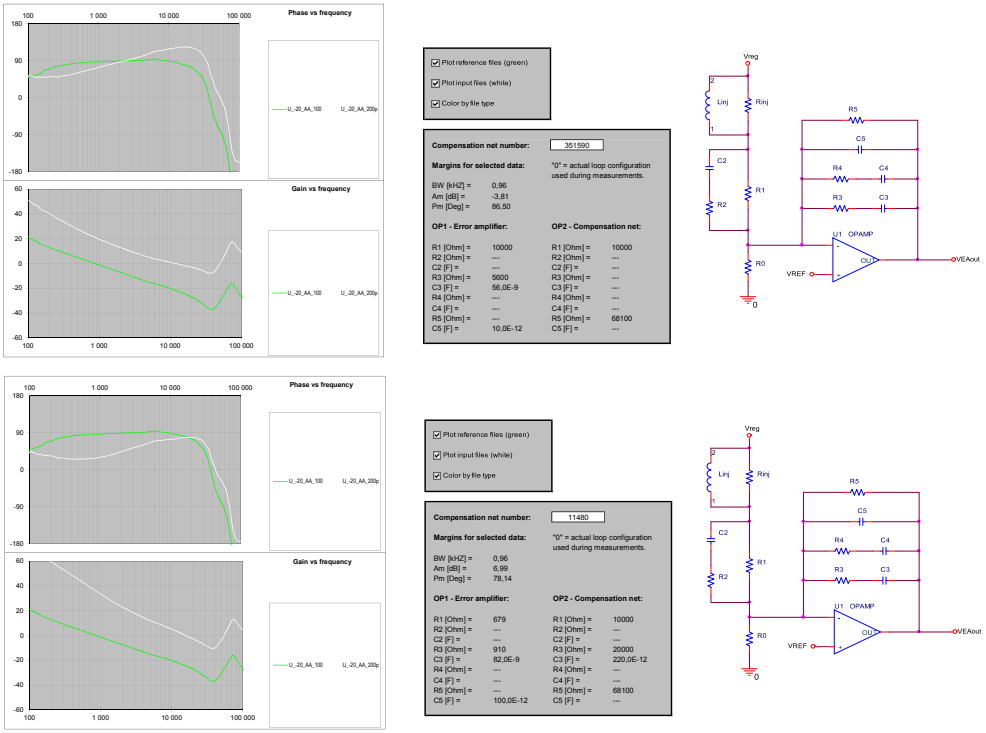

Figure G.3: Two alternative compensation nets for the load alternative.

H General Operation of a Flyback Converter

A flyback converter originates from the back-boost converter and can be seen as an isolated version of it. An illustration of the flyback converter can be seen in figure H.1. The transformer model use a magnetization inductance and one ideal transformer for understanding purpose.

There are two operation modes: when the transistor is ON and when it is OFF. During the OFF-state the ideal transformer induces a current on the secondary side which forward bias the diode. When the transistor is OFF, no current goes through the ideal transformer as the diode block and the current decrease while the capacitor discharge through the load. The different operation modes are shown in figure H.1, where the green symbolize ON-state and orange OFF-state in continuous conduction mode (CCM). Figure H.1 can also be seen as discontinuous conduction mode (DCM) with operations according to the arrows except after the OFF-time when a dead time occurs and cause the capacitor to discharge (blue arrow). For CCM, the voltage and current equation can be expressed in the different operation modes. As the voltage over an inductor is zero, we can express V_{L_1} for the two state as

$$\text{ON: } V_{L_1} = V_1, \tag{H.1}$$

$$\text{OFF: } V_{L_1} = -\frac{N_1}{N_2} V_2 \tag{H.2}$$

and the time integral over a period results in

$$0 = \frac{1}{T} \int_0^T V_{L_1} dt = V_1 DT - \frac{N_1}{N_2} V_2 (1 - D) T, \tag{H.3}$$

where D is the duty cycle and T is the period time. By solving (H.3), the voltage transfer function can be obtained as

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} \frac{D}{(1 - D)}. \tag{H.4}$$

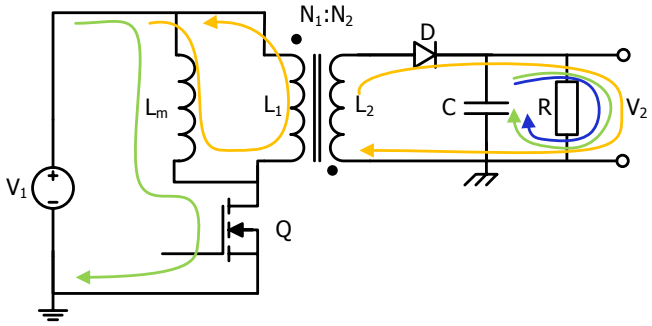

Figure H.1: Flyback converter with illustration of its operation mode CCM and DCM. Green ON-state, yellow OFF-state and the special case for dead time in DCM, blue.

A similar approach can be made in DCM, but no linear relationship is obtained as for CCM. The DCM has a dead time Δ_1 over a period where the current through the transformer is zero.

A quick review of the above calculation gives the expression

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}\frac{D}{\Delta_1} \tag{H.5}$$

for DCM operation. To clarify the non-linearity, a more detail analyse is needed. Starting with defining the current ripple for DCM at ON-time as

$$i_m = \frac{V_{L_1} D}{Lf} \tag{H.6}$$

and the stored energy as

$$W = \frac{1}{2} L i_m^2, \tag{H.7}$$

where f is the switching frequency of the transistor. At the secondary side an energy loss occurs in the load (resistor), which state

$$P_2 = Wf = \frac{V_2^2}{R} f. \tag{H.8}$$

Using the (H.6),(H.7) and (H.8) together results in

$$\frac{V_2}{V_1} = \sqrt{\frac{R}{2Lf}}\, D. \tag{H.9}$$

Although, the transformer operates in OFF– and ON-state, the total current is unchanged. It is only distributed differently.