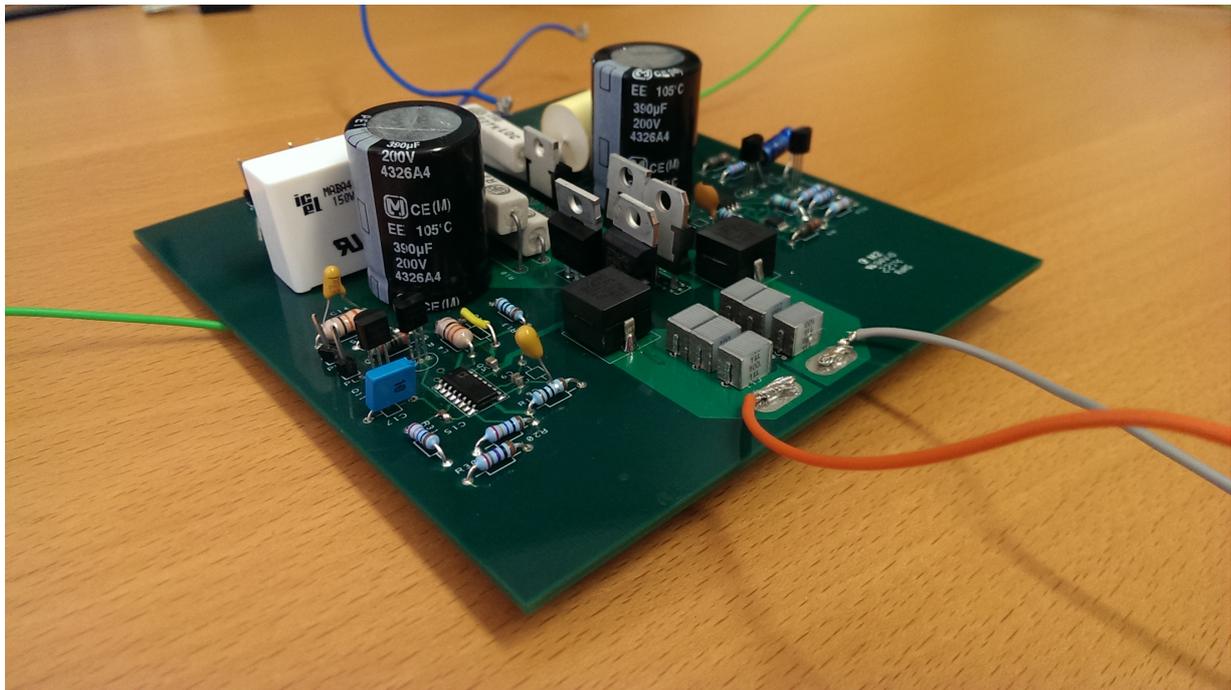


CHALMERS



Improving idle power consumption in class D audio amplifiers

Master of Science Thesis

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Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2014

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Cover:
Picture of prototype dual-polarity buck converter.

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Abstract

A class D audio amplifier usually have a high efficiency for medium to high output power. However, in idle mode and for small power outputs, the efficiency drops. During idle mode, the output switches runs with a 50 % duty cycle in order to create zero volt over the load. The main task of this thesis was to investigate if the idle losses could be decreased by lowering the voltage feeding the amplifier. This without lowering the efficiency on normal operation.

Three designs solutions to lower the voltage have been created and investigated. Two solutions switches between two separate rails, each at a different voltage level. The third uses a dual-polarity buck converter to feed the amplifier with just above the necessary voltage at all times. The designs were simulated in PSpice and the result analysed using both PSpice and MATLAB. It was concluded that all three solutions work as intended and lowers the idle power consumption without adding any extra loss of efficiency at normal operation.

An attempt was made at implementing the buck converters on a printed circuit board. The results from the measurements performed on the prototype showed that the PWM signal generation and surrounding control circuits worked. The power path was also intact, however only DC output could be achieved for frequencies above 500 Hz.

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Sebastian Andersson
Tobias Lindemark
Göteborg, June 2014

List of abbreviations

MOSFET	Metal Oxide Semiconducting Field Effect Transistor
BJT	Bipolar Junction Transistor
IPS	Input Stage
VAS	Voltage Amplification Stage
OPS	Output Stage
PWM	Pulse Width Modulation
SRM	Smart Rails Management
PCB	Printed Circuit Board
DCM	Discontinuous Conduction Mode

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1

Introduction

TODAY more and more effort is put into making electric devices more efficient, both due to environmental and economic aspects [1]. When it comes to high power devices, even a small improvement in efficiency can lead to great energy savings. This is beneficial to both the end user regarding electric bills and it reduces the environmental impact of the device [2]. It might also reduce the demand for cooling of the device due to less wasted energy in form of heat.

In audio installations, the majority of the power losses will be produced when the device is idle [2]. One major contributor to these power losses are the output stages of audio amplifiers. Modern amplifier topologies, such as class D, have high efficiency during moderate to high output power levels but little effort has been made to increase low power and idle performance.

Practical tests by Company A [2] have shown that temporarily reducing the voltage supply to the amplifier from $\pm 90\text{Vdc}$ to $\pm 30\text{Vdc}$ can reduce the idle power consumption from 9 W to 2 W per output channel. In audio amplifiers there can be 8 discrete channels in a single amplifier. In a large installation, used for big events like live performances, the system can contain 100 amplifiers or more. Therefore the reduction of idle power losses will be substantial if the amplifier is more efficient.

1.1 Project description

Company A designs and manufactures high quality sound amplification products. Their work regarding efficiency of their amplifiers have to this date mainly focused on improving efficiency at high power output. Class D amplifiers helps with this since they are inherently efficient for high power [3]. However, not much work has been done when it comes to low power output, or idle efficiency.

1.1.1 Purpose

The purpose of this thesis is to find two main design solutions that lower the idle power consumption of class D audio power amplifiers. One additional design is also investigated and builds on the concept of one of the main designs. The main focus is to reduce the voltage on the rails feeding the output stage of the amplifier. Furthermore, the designs will be evaluated and simulated in PSpice and MATLAB in order to obtain data about how effective and realizable they are. Based on the evaluation, the best designs will be chosen for prototyping if time allows it. The prototype will verify whether the simulated version is reasonable and if any further improvements can be made.

1.1.2 Limitations

The design should all stay within reasonable limits when it comes to:

- Idle versus full power losses
- Cost
- Reliability and complexity
- Size

The solutions that are investigated have to strike a compromise between full power and idle power efficiency. For example, by adding power electronics in series, the full power efficiency might decrease while the idle power efficiency increases. Moreover, the delay between the input and output signal cannot be too long. This is especially true in live performances, but a small delay may be possible in other environments. The cost and size have to be within reasonable limits and still be reliable.

The project will only focus on the power supplied to a class D audio amplifier and will not make any changes to other components within the class D set-up. Too costly and complex solutions will not be investigated since the audio amplifier still has to be competitive on the market.

1.2 Outline

The report is divided into the following chapters:

Chapter 2 - Theory

The chapter is dedicated to theory relevant to know before reading any further material in the report.

Chapter 3 - Case Set-up

Each of the cases with design suggestions is presented and explained.

Chapter 4 - Simulation Analysis

Each of the case is simulated together with a class D amplifier and the result is analysed and evaluated.

Chapter 5 - Prototype Building

One of the designs is used for a building a prototype, the result is analysed and evaluated.

Chapter 6 - Conclusions

Discussion of the results.

Appendix

Any MATLAB code, circuit schematic or similar will be presented here.

2

Theory

THIS chapter will deal with the basic theory behind audio amplifiers and the different classes associated with them. This will lead into a thorough description of the class D amplifier, which is the main amplifier class of this project. Moreover, a description of clipping and distortion and semiconductor devices will be presented. Last, a surrounding world analysis will investigate other solutions dealing with the problem at hand.

2.1 Power amplifiers

Amplifier circuits have numerous areas of operation and only a fraction of these deal with audio amplification. These are classified as power amplifiers and are devices that takes an input audio signal and amplifies it to the desired level for the output audio signal [4]. The amplification is achieved through a series of Bipolar Junction Transistors (BJT) and/or Metal Oxide Semiconductor Field Effect Transistors (MOSFET) connections that enhances both voltage and current to achieve a much higher output than input power. A basic schematic of an audio power amplifier circuit can be seen in Figure 2.1.

The basic power amplifier can be divided into three stages; an input stage, a voltage amplification stage and an output stage. The input stage (IPS) compares the input with a fraction of the output and determines how close they are and whether it needs to be adjusted. The middle stage is called voltage amplification stage (VAS) and this stage stands for most of the voltage amplification of the signal [4]. The third and final stage is called the output stage (OPS) and provides the current gain. The output stage is built up with two pairs pairs of BJTs, one for each half period of the signal that needs to be amplified. Other possibilities incorporate MOSFETs in the output stage [4].

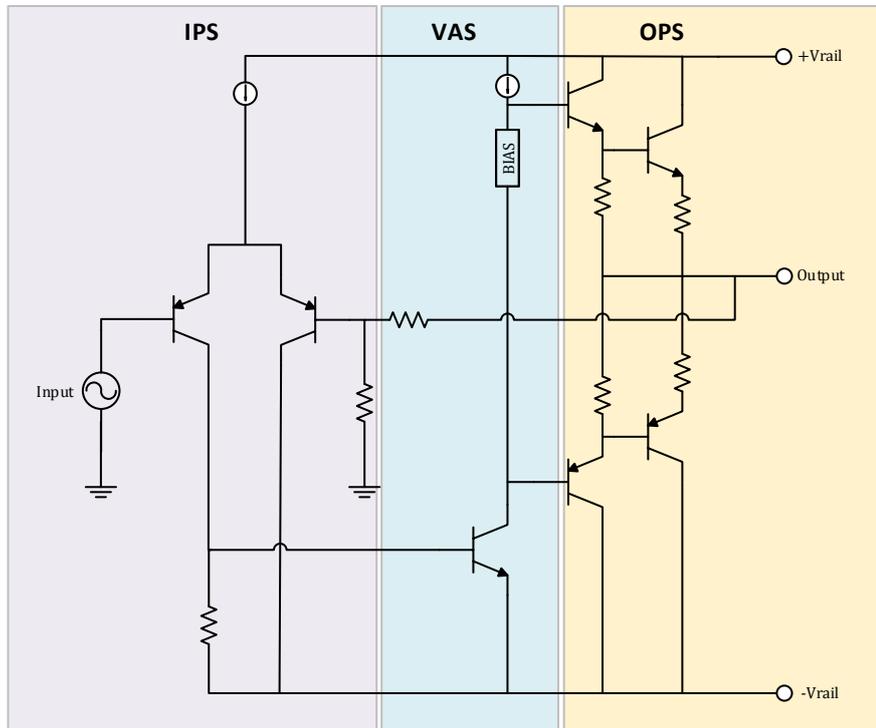


Figure 2.1: A basic circuit of a power amplifier, the amplifier is colour-coded for each stage.

2.1.1 Amplifier classes

There are several different classes of amplifiers and in general the class is determined by what kind of output stage is used. For purely analog amplifiers, class A, B or AB are mainly used. The output stage of a class A amplifier can be seen in Figure 2.2.

The output stage can consist of a single BJT that conducts for the entirety of the period of the output signal. The output stage of a class B can be seen in Figure 2.3 and in Figure 2.4. Here one BJT conducts for half the period of the output signal. The class B amplifier is used in a push-pull configuration, meaning that there are two BJTs working on opposite half period [4].

An output stage of a class AB is very similar to a class B output stage. Both uses the push-pull configuration with two BJTs, but the difference is that class AB has an overlap in the conduction of the two devices. This means that the BJTs both conduct on the same time for a small period of time and therefore smooths out the transition from positive to negative half period [4]. Because of this the design incorporates some traits from both class A and B. The set-up is similar to Figure 2.4 and is a common output stage in analog audio amplifiers [5]. The circuitry can also be seen in 2.1.

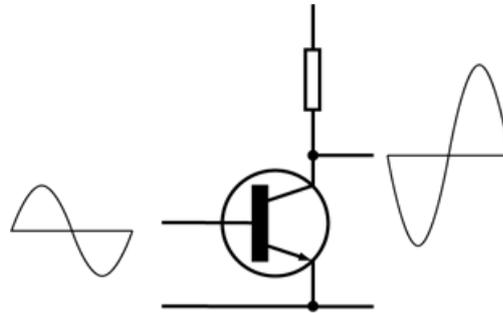


Figure 2.2: Output stage in a class A amplifier. Author wikipedia user GRAHAMUK with modification of Yves-Laurent Allaert. Figure is licensed under the Creative Commons Attribution-Share Alike 3.0 Unported license. <http://creativecommons.org/licenses/by-sa/3.0/legalcode>

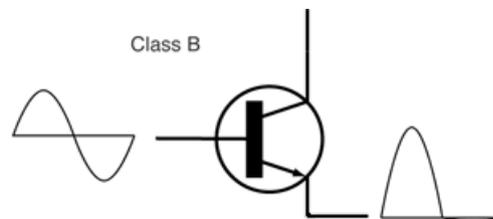


Figure 2.3: Output stage in a class B amplifier. Author: Wikipedia user Nitram cero. Figure is licensed under the Creative Commons Attribution-Share Alike 3.0 Unported license. <http://creativecommons.org/licenses/by-sa/3.0/legalcode>

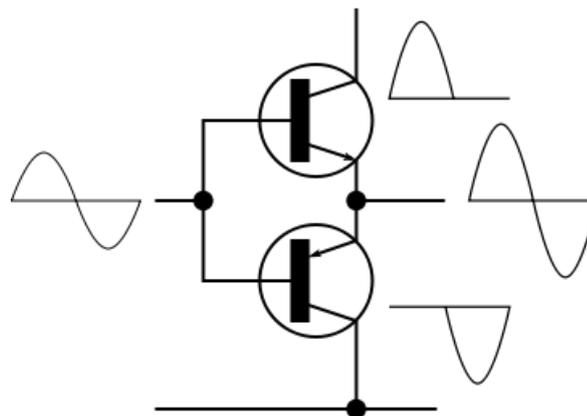


Figure 2.4: Output stage of a class B amplifier using push-pull configuration. Author: Wikipedia user Nitram cero. Figure is licensed under the Creative Commons Attribution-Share Alike 3.0 Unported license. <http://creativecommons.org/licenses/by-sa/3.0/legalcode>

All of the classes examined so far suffers from low efficiency. Class A amplifiers have the lowest efficiency with a power dissipation around twice the output power [6]. Class

B and AB have higher efficiency than class A because of the turn-off of one BJT each half period. There are several other output stages in addition to the ones mentioned here [6]. Only class D will be examined further since this is the class which the design study will build on. The other classes will not be investigated since they are not used in the design.

2.1.2 Class G and class H

Increasing efficiency by lowering rail voltage when possible is something that is present in class G and class H amplifiers. These are usually used with class B output stages. The idea behind these amplifier classes are visualized in Figure 2.5 and in Figure 2.6. Previous work on this subject shows that and there are several examples of using class G or H topologies in conjunction with class A, B and AB output stages [6]. A paper on a class H topology together with a class B output stage can also be seen in a technical paper by Jungqi Liu et. al. [7]. The paper states "*The proposed structure shows 5 to 7 times efficiency improvement under low voltage signals*".

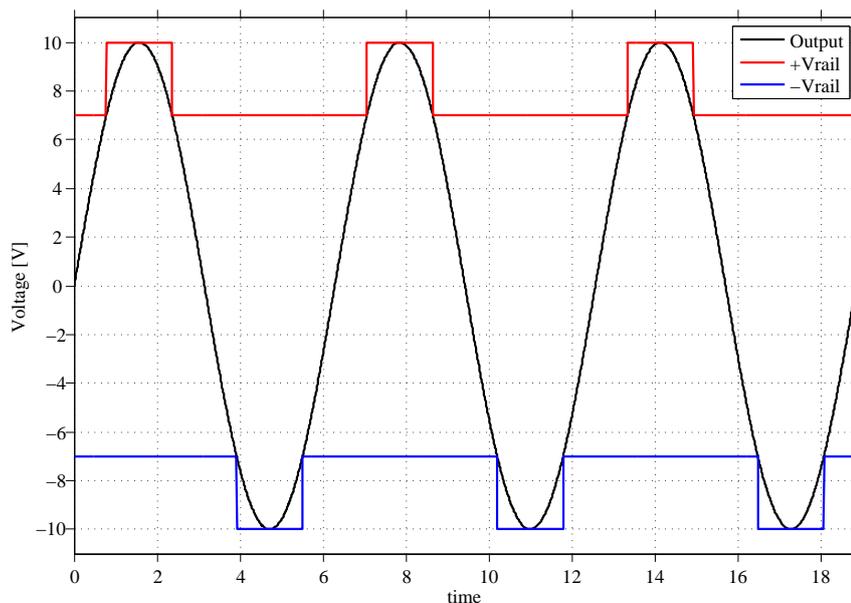


Figure 2.5: Behaviour of a class G amplifier. The amplifier switches between two different rail voltages depending on what the output requires.

2.1.3 Class D

The low efficiency of the previously mentioned amplifier classes has led the development of other design solutions [6]. One of these is the class D amplifier which incorporates high frequency switching. Because of this, a class D amplifier works differently than the other classes and has a much higher efficiency of around 90% [4]. The efficiency does not mean

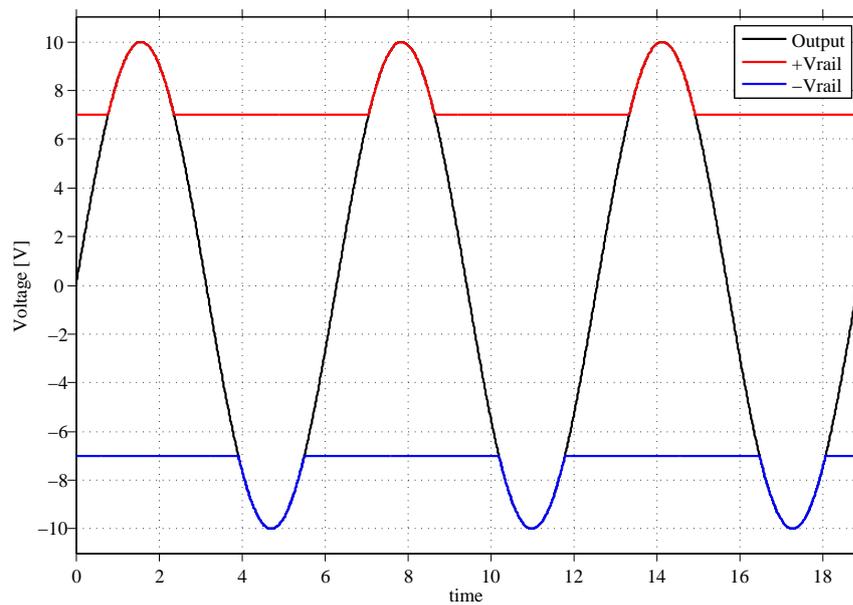


Figure 2.6: Behaviour of a class H amplifier. The amplifier switches between two different rail voltages depending on what the output requires.

much though, if the sound quality is poor. Therefore one may need to sacrifice some of the former in favour of the latter. Instead of several stages of amplification, which requires many linear circuit elements and BJTs, it produces a Pulse Width Modulated (PWM) version of the input signal which is amplified in the output stage using MOSFETs [6].

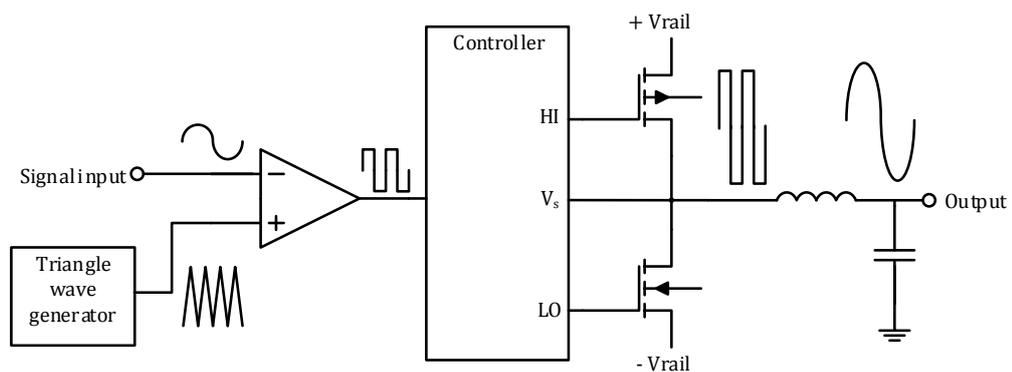


Figure 2.7: A basic schematic of a class D amplifier.

A basic overview of a class D amplifier with controller can be seen in Figure 2.7. The input signal passes through a comparator, together with a triangular wave, to produce

a square wave output with a duty-cycle corresponding to the amplitude of the input signal [4]. This signal has the same average value as the sinusoidal input. The PWM signal is controlled either digitally by a controller or by an analog circuit to switch the output stage MOSFETs on or off and thereby achieving an amplification of the signal corresponding to the supply rail voltage [4]. The amplified square wave signal passes through a low-pass filter to obtain a smooth output to the loudspeaker [6].

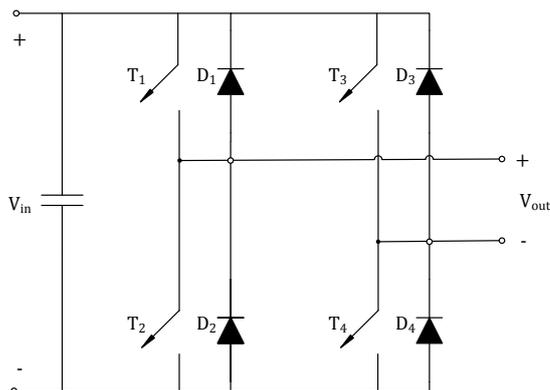


Figure 2.8: Basic circuit of a full-bridge topology.

The output stage of the amplifier in Figure 2.7 is a half-bridge topology since it only incorporates two switches. An alternative would be to use a full-bridge output stage with two switching legs that are controlled separately [3], as seen in Figure 2.8. The amount of components that are required for a full-bridge topology are the double, but it can deliver the same amount of power with only half the supply voltage [3], making this set-up preferable in the class D output stage. At voltages under 150 V, MOSFETs have more desirable properties than BJTs [4]. Therefore, it is preferable to use MOSFETs in a full-bridge setup used in high power class D amplifiers, where the supply voltage is usually limited [2]. This is also the design used by Company A in their devices.

2.1.4 PWM switching

The switching scheme to generate a PWM signal to drive the MOSFETs in the class D output is shown in Figure 2.9. A high frequency, triangular wave is used and compared with the sinusoidal input signal. When this wave is lower than the input signal, a switch connected to a DC voltage is turned on at the intersection between the triangular wave and the input. The opposite happens when the triangular wave is higher than the input. This generates a square wave [3].

There is also the possibility of creating two PWM versions of the input signal. In Figure 2.10 two control signals are generated from the input signal but with different signs. The control signal that is positive in the beginning generates the first square-wave in Figure 2.10 and the other generates the second square-wave. The result is shown at

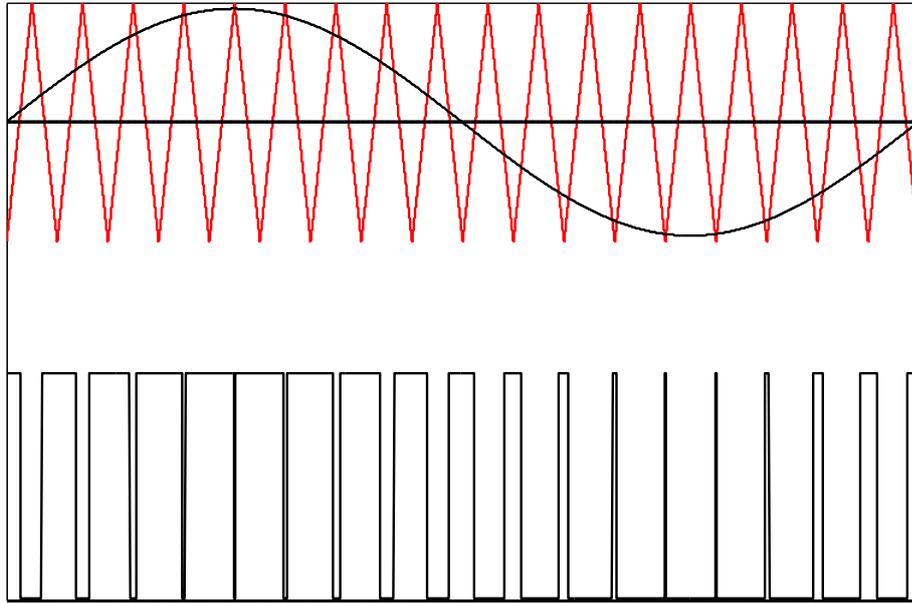


Figure 2.9: Switching scheme of PWM.

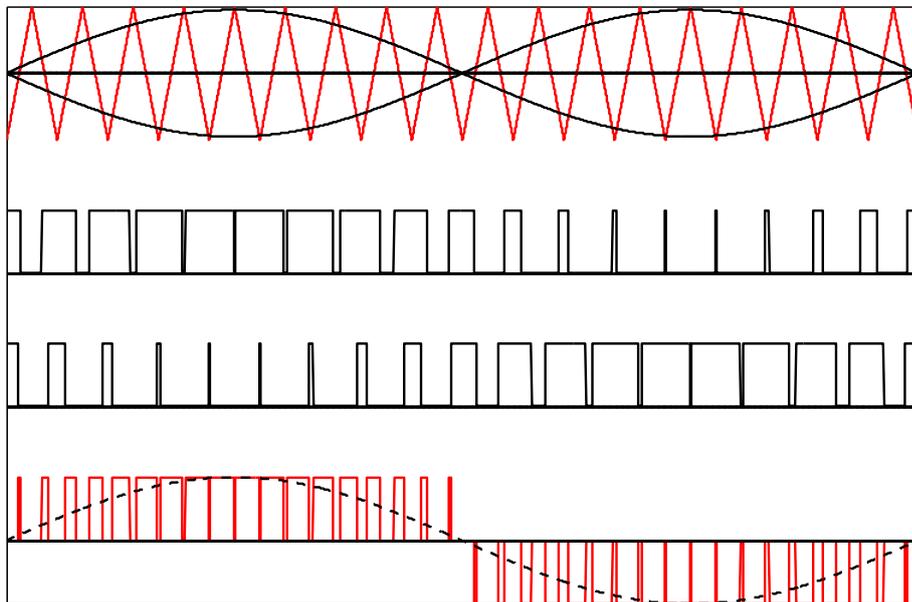


Figure 2.10: Switching scheme of unipolar PWM.

the bottom were the second wave is subtracted from the first one, creating a signal that has a sinusoidal average with a low current ripple [3]. This switching scheme is called unipolar switching and is used together with the full-bridge topology. When both of the PWM signals are connected to the same voltage source the resulting voltage will be zero.

2.2 Buck-converters

A buck- or step-down converter is used to control the average voltage to a value that is the same or lower than the input voltage. The topology can be seen in Figure 2.11 where an input DC voltage, V_{in} , is lowered to produce V_{out} .

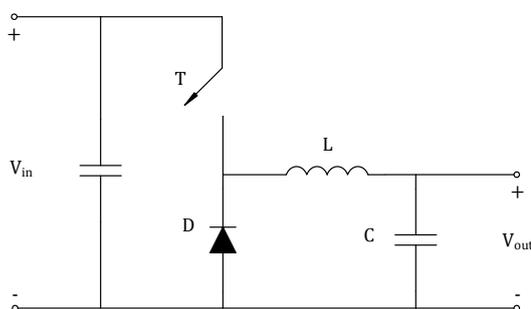


Figure 2.11: Circuit diagram of a simple buck converter.

The converter operates by varying the duty-cycle of the switch and thereby controlling the output voltage to the required level. During its on-time, the switch conducts and the whole input voltage is applied over the diode. When the switch is off, the voltage is close to zero but the current is now free-wheeling through the diode and through the load since the inductor is current stiff. To smooth out the output voltage, a low-pass filter containing an inductor and a capacitor is used. In this way, an output of the same characteristic as the input is produced, but with a lower amplitude. By varying the duty-cycle, the output can be made close to the input amplitude or as low as zero.

2.3 Clipping and distortion

Clipping is the result of the amplifier trying to deliver more power than the power supply is capable of providing and the signal can not be amplified further. In practice this means that the amplifier will not be able to deliver enough power during the peaks of the audio signal to the speakers. The result for an audio signal is that loud notes would sound as loud as soft notes since everything will have the same amplitude (Peak output power).

Clipping is usually divided into two types: hard clipping and soft clipping. Hard clipping occurs when the amplifier simply delivers maximum power to the speaker for all signals exceeding the maximum power available. This may cause the loudspeaker and amplifier to overheat since maximum power is being supplied for a long time [8]. Soft

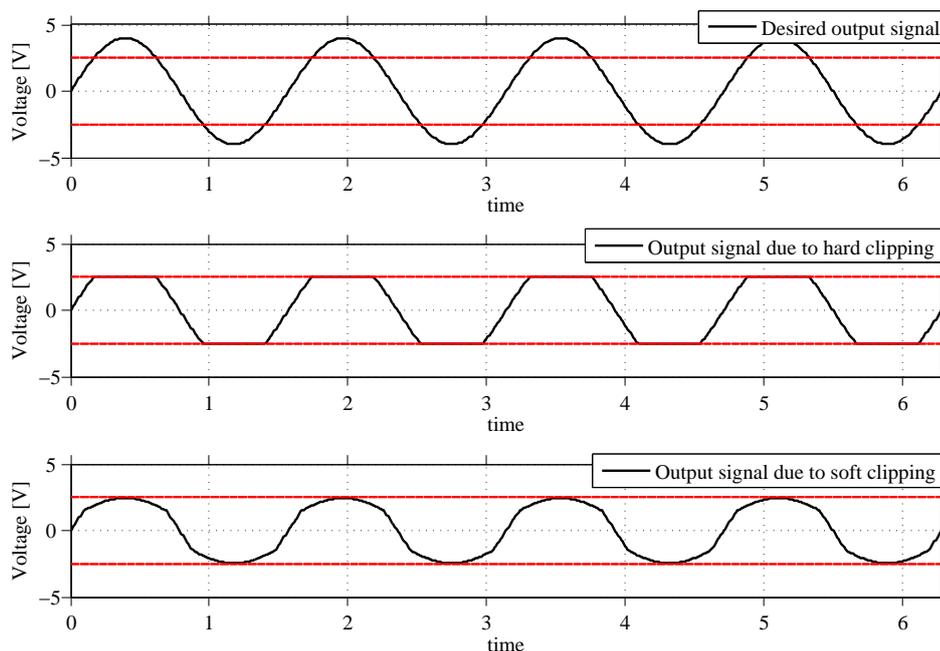


Figure 2.12: From top to bottom: The desired, pure sinusoidal wave form, the wave form due to hard clipping and the wave form due to soft clipping

clipping is a way to deal with this issue by creating a smooth transition to peak power. This method lowers the risk of overheating the loudspeaker and amplifier. However, both methods creates undesirable harmonics which can contribute to distortion and a poorly sounding audio signal [8]. An illustration of hard- and soft clipping can be seen in Figure 2.12. The clipping can be detected by simply knowing the desired amplification and comparing the input with a fraction of the output (corresponding to the amplification). If the input is larger than the fraction of the output, a signal can be sent and notify the users that the amplifier is working at its limit.

Another source of distortion can occur during the crossover from negative to positive half-period of the output signal and vice versa. This is a more common problem for class A, B and AB than it is for class D. In class D amplifiers the MOSFETs can be controlled to minimize the crossover distortion.

2.4 MOSFET

The MOSFET, Metal-Oxide-Semiconductor Field-Effect Transistor, is a transistor that is commonly used in class D amplifiers. The MOSFET can be used to switch on and off depending on the voltage applied at the gate-terminal. A current will flow through the drain and source terminals, the direction of the current is dependent on the type of MOSFET used. In an n-channel MOSFET the current flows from drain to source. The

opposite is true for a p-channel MOSFET [3].

The output characteristic of an n-channel MOSFET can be seen in Figure 2.13 using Shockley's transistor model [9]. As long as the gate voltage is higher than a certain threshold voltage, a current can flow through the drain and source terminals. The drain current i_D will increase linearly with an increase in voltage over the drain source terminals in the ohmic, also known as linear, region. In the saturation region it can only be increased by a raise in gate voltage [3], [9].

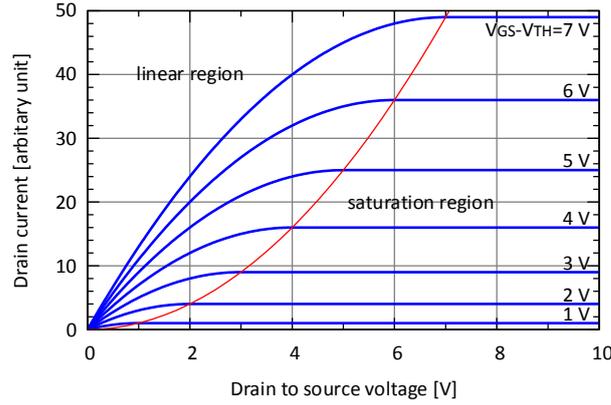


Figure 2.13: Characteristic of n-channel MOSFET. The figure has been made by wikipedia user CyrilB. Figure is licensed under the Creative Commons Attribution-Share Alike 3.0 Unported license. <http://creativecommons.org/licenses/by-sa/3.0/legalcode>.

2.4.1 Switching losses

An ideal switching scheme would not result in any switching losses at all. The current through the MOSFET would decrease to zero immediately and the voltage across drain and source would rise at the exact same moment. In a real switch however, this is not the case. A simple illustration of how switching losses in a MOSFET occurs can be seen in Figure 2.14 [3]. When the gate voltage is applied, the current through the MOSFET increases linearly until a final value I_0 is reached and this time is hereafter denoted as t_{ri} . After the time t_{ri} the voltage across the drain and source terminals start to fall, the voltage fall time is denoted as t_{fv} . For turn off a similar situation arises, the current will start to fall when the voltage across drain and source has reached its final value. This time is denoted as t_{rv} [3]. The time the current takes to fall is denoted as t_{fi} . The switching losses can then be expressed as

$$W_{on} = \frac{1}{2}V_d I_0 t_{on} = \frac{1}{2}V_d I_0 (t_{ri} + t_{fv}) \quad (2.1)$$

$$W_{off} = \frac{1}{2}V_d I_0 t_{off} = \frac{1}{2}V_d I_0 (t_{rv} + t_{fi}) \quad (2.2)$$

during turn-on and turn-off respectively. This is assuming the switching characteristics form perfect triangles during turn on and turn off. If the switching is simulated and several data points on the curve are known. The losses can be calculated more accurately as

$$P_{sw} = f_{sw} \int_0^{T_{sw}} i(t) * v(t) dt \quad (2.3)$$

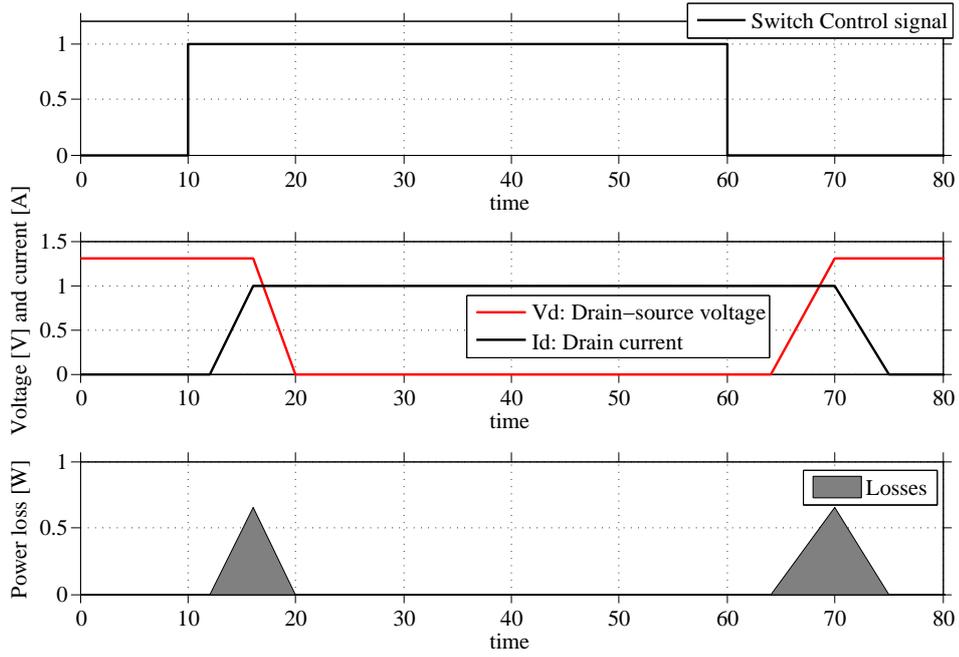


Figure 2.14: Switching losses in a MOSFET. The two triangles represent heat dissipation in MOSFET during turn on and turn off.

2.4.2 Conduction Losses

There is an internal resistance in the MOSFET, meaning that there will be small conduction losses. The conduction losses can therefore be calculated as

$$W_{on} = I^2 r_{DS(on)} \quad (2.4)$$

where $r_{DS(on)}$ is the resistance of the MOSFET during conduction [3]. Both switching and conduction losses have to be known and accounted for when incorporating a MOSFET in a circuit and when considering efficiency.

2.5 Surrounding world analysis

In order to avoid any patent infringements a surrounding world analysis has been conducted. The main focus of the project is to lower idle power losses in a class D amplifier. This can be done by lowering the rail voltage when maximum voltage is not required but other options may be more preferable. By knowing this, other audio amplifier manufacturers were investigated in order to discover other designs that are already implemented and if the designs in this report infringes on any existing patents.

2.5.1 Competing companies

One solution comes from Company 1 and is used in their amplifiers. They claim their technology have reduced the idle power consumption by a great deal.

Company 2 has a patent pending regarding a circuit they claim improves their class D topology. Their solution have two modes of operation, which are dependant on whether it is in a high-impedance connection or a low-impedance connection. In high-impedance, 70 V or 100 V operation is available. At a low-impedance, the amplifier switches to a lower voltage drive. This technology does not seem to infringe on the desired solution, but is worth noting.

Company 3 has a patent for their technology which integrates the amplifier drive stage into the power output stage. According to them, this makes the amplifiers as efficient as a class D amplifier while still maintaining a sound quality similar to a class AB amplifier. None of the presented technologies from Company 3 seem to infringe on the desired solutions.

3

Case set-up

THE main purpose of the thesis, as explained in Chapter 1, is to design and evaluate at least three set-ups to lower the idle power consumption of class D amplifiers. This can be done in a number of ways but the focus is put on temporarily lowering the rail voltage when the input signal is low and thereby lowering the power consumption. In this report the word idle may be confusing since idle is defined as no output signal. Here, small input signals will also be supplied from lower voltage designs in favour of lowering the consumption even more.

The designs were built using PSpice and MATLAB and to test their functionality a simplified class D output stage was used as a reference and test bench.

3.1 Building test bench

Before any design solutions could be built the first step was to represent the class D output stage from Company A so that the different solutions could be tested and evaluated properly. As explained in Section 2.1 the output stage from Company A is essentially a full-bridge converter and a simplified circuit was built using PSpice. Together with this a controller for driving the gates of the MOSFETs was needed.

3.1.1 Class D output stage

A schematic of a first version of the test bench circuit can be seen in Figure 3.1. The MOSFETs are of the type IRFB5615PBF and are also found in the design by Company A. A datasheet for the MOSFET can be seen in Appendix A.1. The size of the low-pass filter was tuned until the ripple on the output was within reasonable limits and are of similar size as its real counterpart.

The first basic circuit had a number of problems that needed to be fixed. For example, there was no current limitation, which means that the controller could draw as much current as it wanted, disregarding the fact that there are limitations in real

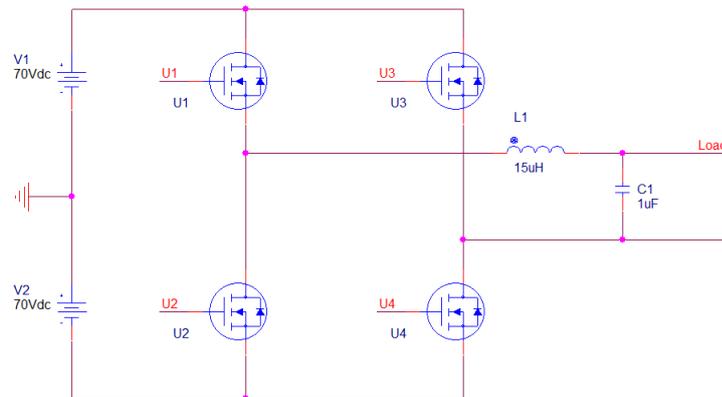


Figure 3.1: First model of the output stage of a class D amplifier.

life implementation. Therefore, small current limitation networks were added, after the power supply, to the test bench. These networks were built using BJTs together with two resistors and two diodes. The resistor in series with the BJT controls the current amplitude limit while the one in parallel only provides a reasonable base current to the BJT. This can be seen in the top left in Figure 3.2. When the current increases, the voltage over the series resistor will increase and the base-emitter voltage of the BJT will decrease, therefore decreasing the maximum allowable current.

Another problem is that all the power must be drawn instantaneously from the grid which puts great demand on the power supply. By implementing the current limiters this is no longer possible. The solution was to implement rail capacitors, which are present in the real life counterpart, which discharge quickly when power is needed and are charged the rest of the time. These are explained more thoroughly in the next sub-chapter.

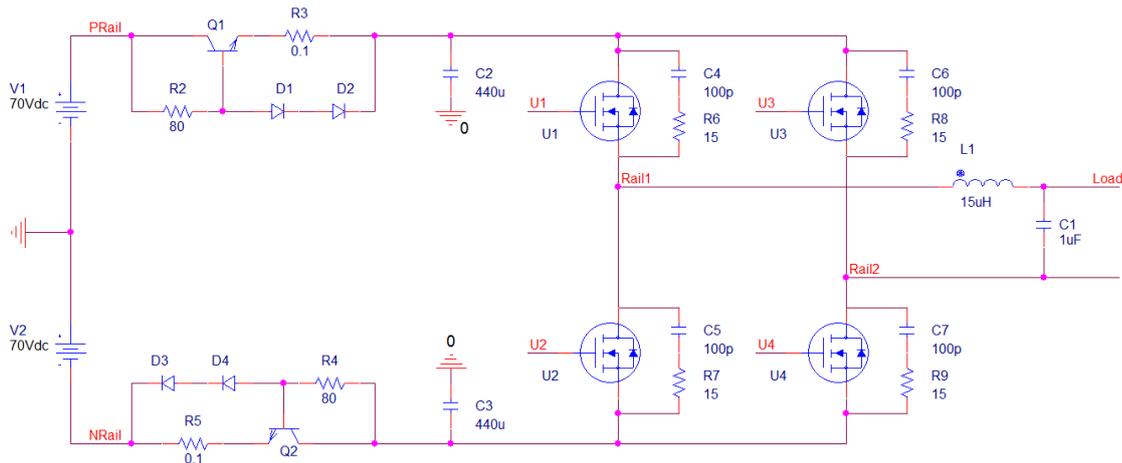


Figure 3.2: A more realistic design of the class D output stage containing current limiters, rail capacitors and snubbers.

A third step was to implement turn-off snubber networks across each MOSFET to limit the voltage during turn-off. The size of the snubber network is the same as in the design by Company A. The more realistic design of the class D output stage can be seen in Figure 3.2. This circuit will be used in the rest of the report as the reference for the power consumption solutions.

3.1.2 Rail Capacitors

The amount of power required to amplify a signal from music varies a lot. Most of the time it is within what can be supplied by the grid. However, there are spikes that can occur due to, for example, a hard strike on the bass drum during live performances. It is not desirable to supply such short bursts of power directly from the grid and one way to solve this is by using large capacitors on the voltage rails to the amplifier. A current limiter is also used to limit the amount of current drawn from the grid. Most of the time this is enough to drive the amplifier but when the amplifier requires more current than what is allowed by the current limiter the rail capacitors discharge. The capacitors are then charged again by current from the grid when the amount of power required is low.

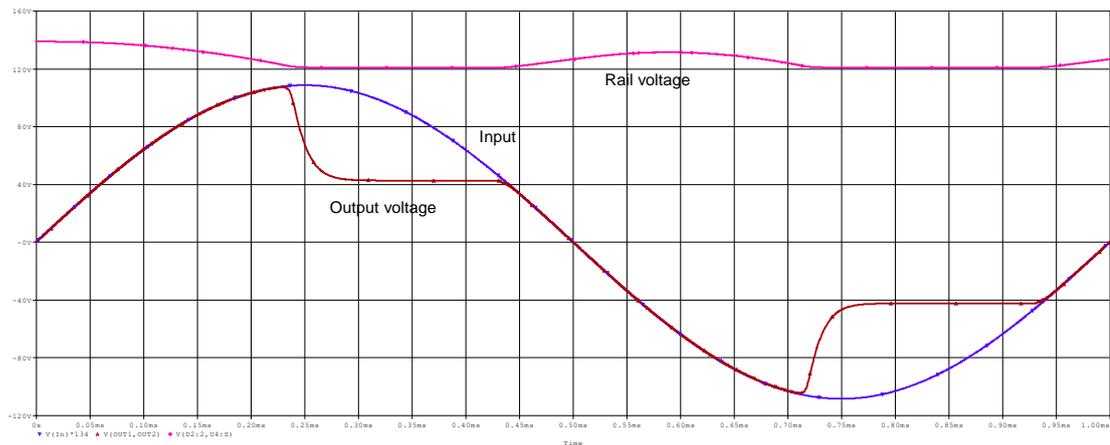


Figure 3.3: Extreme case where the rail capacitors tries to supply current for too long.

The effects of the rail capacitors can be seen in Figure 3.3. The voltage on the rails drop as the capacitor discharges. When the capacitors are completely discharged, a dip can be seen in the output signal. In Figure 3.3 this is done purposefully and the capacitors are smaller than the actual ones, plus the required power lasts longer than usual. When the capacitors are discharged the signal clips as the power supply cannot supply enough power.

3.1.3 Output stage gate driver

Building a class D output stage with MOSFETs, in PSpice, require precise timing of the gate drivers to eliminate current spikes. This is because the MOSFETs in one leg can act as a short circuit if not switched properly. This will happen if the switches, in the

same leg, are turned on at the same time. The result will be large current spikes which, in turn, could result in breaking the MOSFETs.

One solution to eliminate this problem can be seen in Figure 3.4. A PWM signal is generated by the block Ecomp. To be able to trigger the MOSFETs in the same leg with some margin, also called dead time, a small RC-circuit together with two ideal switches in a totem-pole configuration is used. The capacitor and resistance will delay the time it takes to reach the final voltage level of the PWM generator, which here is set to ± 1 V. The two ideal switches will turn on as soon as a positive voltage is applied across the two terminals. The capacitor will then discharge through the diode.

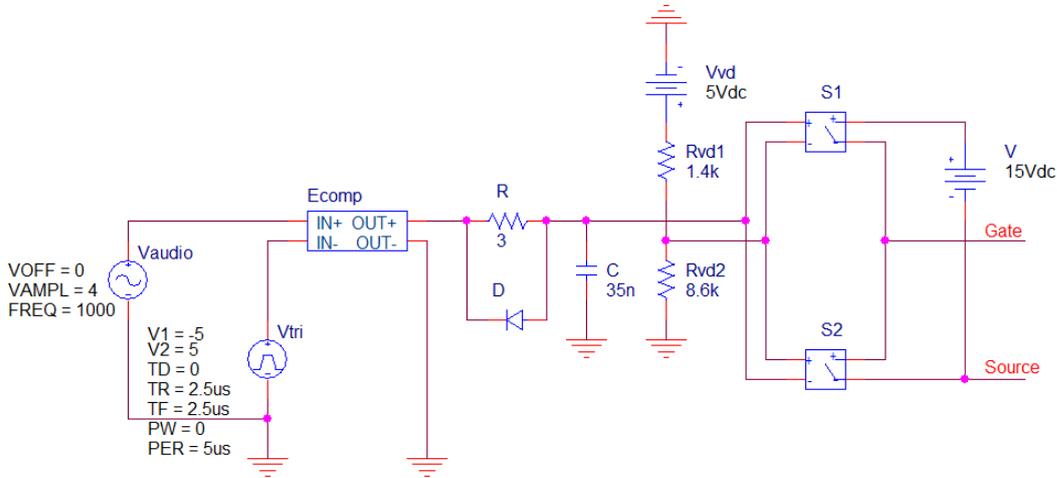


Figure 3.4: First PWM controller solution, The Ecomp component applies +5 V if the audio signal is larger than the triangle wave. If it is smaller, -5 V is applied. The capacitor C gives the voltage a longer rise time, which leads to a dead time between switching of the MOSFETs.

In Figure 3.4 the switches are connected to the same node, here called Gate, but with different polarities. The voltage in the node is controlled by adjusting the size of the resistances connected to the voltage source V_{vd} and is related by

$$V_{node} = V_{vd} \frac{R_{vd2}}{R_{vd1} + R_{vd2}} \quad (3.1)$$

In this case, voltage of the node will be 4.3 V. This results in switch S_1 applying 15 V over source on one of the MOSFETs when the PWM signal is larger than 4.3 V. The same is true for switch S_2 . When the PWM signal is below 4.3 V the source voltage is applied on the MOSFETs, resulting in 0 V applied to the gate-source voltage and making sure the MOSFET does not conduct. Figure 3.5 shows how the RC-circuit delays the PWM signal and making it possible for the switches to turn on at a specified voltage.

The PWM generation needs to be able to adapt to changes in rail voltage. Therefore, a controller that uses a feedback loop was built. This controller compares the input

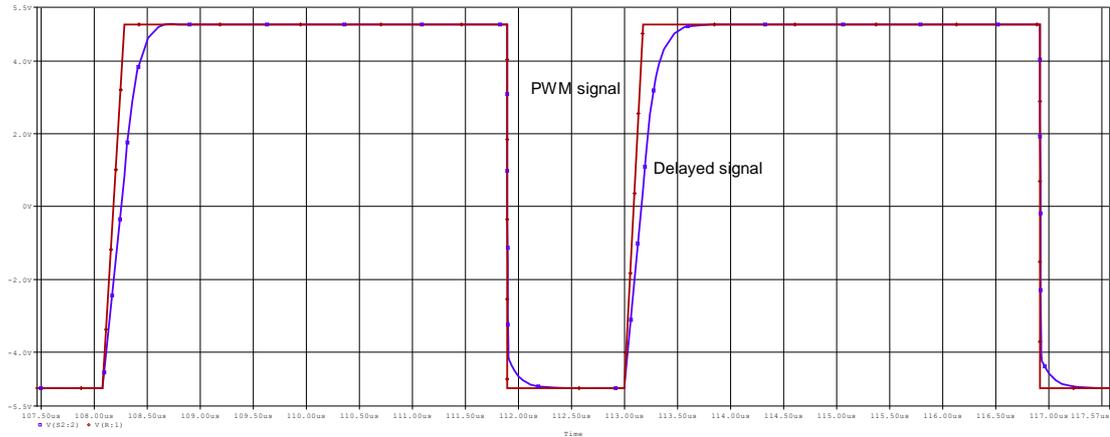


Figure 3.5: Voltage waveform for a delayed switching waveform and the real PWM signal. PWM signal is shown in red and the delayed waveform is shown in purple.

signal with a fraction of the output. The error produced is amplified and compared with a triangular wave to determine the switching scheme, just as the PWM generation described in Section 2.1. Figure 3.6 shows a flowchart of the implementation.

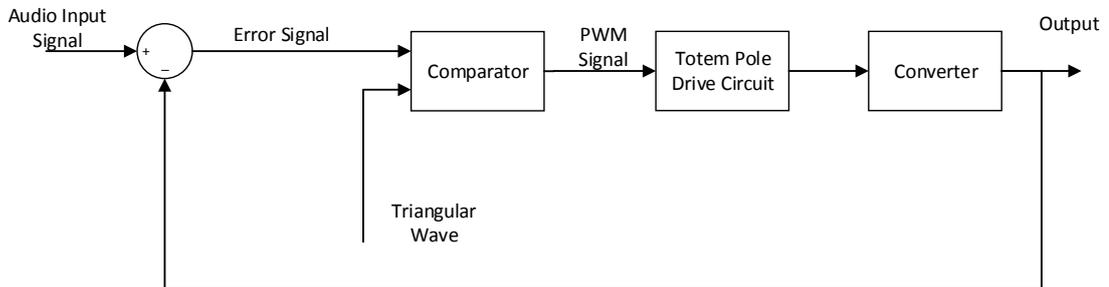


Figure 3.6: Block Diagram over the control-system using feedback from the output.

3.2 Design solution 1a

The first design solution, to minimize idle power losses, switches from ± 70 V to ± 30 V rails depending on the input signal. The idea is that this will be done constantly which will lower the consumption when there is only a small amount of power needed. Both rails will either be high or low depending on the amplitude of the input signal, meaning synchronous switching of the MOSFETs. The entire circuit can be seen in Figure 3.7.

The detection of when the switching occurs is done by using a precision full-wave rectifier together with a simple comparator circuit. These are located to the left, before the gate drivers, in Figure 3.7. The precision full-wave rectifier essentially consists of two "Superdiodes" [10]. A "Superdiode" is basically a operational amplifier in series with a diode which has a negative feedback loop. By using this set-up, the small voltage drop of an ordinary diode is eliminated, which results in a much more precise rectification of the input signal [10]. One of the "Superdiodes" handles positive periods and can be connected to the output of another, modified, "Superdiode", which handles negative periods. The result is a very precise full-wave rectifier that is suitable for very small signals.

A comparator, that is located just after the rectifier, simply decides a voltage level where the switching between rails is done [10]. Here, it represents a level just below 30 V. The signal then controls the gate drivers and the following MOSFETs that put out the voltage to the load. The entire circuit can be seen in Figure 3.7.

This version will, however, have a problem during idle mode operation. When the amplifier is in idle mode, the switches in the class D output stage work with a 50% duty cycle. This will cause a problem for the solution. The current, through the inductor in the output filter of the amplifier, cannot change direction immediately when the OPS switches change voltage polarity. A rapid change in current is not possible since the voltage across the inductor is described as

$$V = L \frac{di}{dt} \quad (3.2)$$

When the OPS switches change polarity over the inductor a current will still flow in the same direction as before the switching occurred. Therefore, the current will be drawn from the negative 70 V rail to the positive 70 V rail through the MOSFET diodes. This is the only path the current can flow during this moment, as the low voltage rail diodes are blocking any current from negative to positive rail. In turn, this will lead to excess losses in both high voltage rail diodes and rail switches.

The problem can be solved by replacing the low voltage rail diodes with MOSFETs that turn on during low output operation. The MOSFETs are connected in such a way that the MOSFET diode is positioned in the same way as in Figure 3.7 in order to avoid discontinuities in the voltage supply. However, the forward voltage drop across these diodes are 1.3 V. Because of this, an alternative is to place separate diodes, with a lower forward voltage drop in parallel with the MOSFETs. The improved rail solution can be seen in Figure 3.8.

Another approach to avoid the current path problem in idle would be to not switch with a 50 % duty cycle in the OPS, but to put a very small signal on the output instead. However, this will lead to unnecessary losses since a small output is produced.

A small adjustment was necessary regarding the placement of the current limiters and rail capacitors. If they were placed in the same location as before, just before the class D output stage, this meant that the operation of the rail switches was compromised. The current through the rail switches need to react to the current demand of the full-bridge switches and this require a fast response. The previous placement of limiters and rail

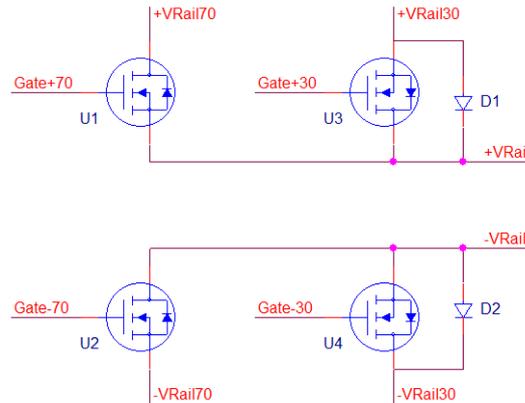


Figure 3.8: Schematic of the first design solution with fixed idle mode operation. The ± 30 V rail diodes are replaced with MOSFETs to be able to conduct with negative currents that comes from the output inductor during idle operation.

capacitors meant that the current could only go up to a certain value and therefore the demand from the full-bridge switches was not met. The current ended up charging the rail capacitors slowly.

The solution was to place the current limiters and rail capacitors in connection with the supply grid, before the rail switches. This meant a fast response since current spikes could be drawn from the capacitors.

3.3 Design solution 1b

This solution is based on the first design, solution 1a, but instead of switching down from ± 70 V every time the input goes below a certain level, the idea is that the voltage is kept high as long as there is an input signal. In the design, the switches can be either MOSFETs or thyristors that are switched on at a certain level and stay on as long as the input signal is above zero. The rails can be controlled by using a similar circuit to the one seen in Figure 3.7, but with a minor modification. This means that the full-wave precision rectifier can be modified to a peak wave detector by mounting a capacitor on the output of the rectifier. The full-wave rectifier can also be replaced by a super diode, simplifying the circuit even more.

If a large capacitor is used the voltage will stay above zero for a long time. This solution is suitable for MOSFETs since they are voltage controlled. The MOSFETs will remain closed and rails will therefore not change, unless the audio input has remained at zero for a given time period. The time required for the rail switching can be determined by setting the size of the capacitor and of the discharging resistor placed in parallel with the capacitor. The two components determines the time constant τ described as

$$\tau = RC \tag{3.3}$$

where τ is the time it takes to discharge the capacitor to 36.8 % of the final voltage level [11]. The rails can then be kept high for several minutes after the music has stopped. This will guarantee a good output signal quality as the maximum voltage is always available. The switching present in solution 1a will not be able to interfere in case there is just a short break in the music. The capacitor voltage during the discharge is described as

$$V(t) = V_0 e^{-t/\tau} \quad (3.4)$$

A simpler circuit can be built by using thyristors which only require a turn-on signal. This means that the circuit only applies a signal to the thyristors every time the audio input is above a certain threshold. Since the thyristors turns off naturally at zero current, only turn-on matters. However, the thyristors will be turned off immediately at zero current, and have to be turned on again afterwards, even if it is just a short break in the music. This may result in higher switching losses than in the MOSFET variant.

Solution 1b is here treated as a design that builds on design solution 1a with only small changes in the circuit topology. Therefore, this section is shorter and the pictures presented in Section 3.2 is still viable.

3.4 Design solution 2

Design solution 1 only switches between two rail voltages, which is a quite simple design. The drawback is that it does not follow the input signal very closely. To further decrease the idle losses, another solution was designed with the goal of making the amplifier follow the input signal more closely and only put out a small amount above the required voltage at every time instant. This design solution, design 2, uses a buck converter to change voltage on the rails supplying the voltage to the OPS.

A schematic of the implementation can be seen in Figure 3.9. Two basic buck converters have been combined to produce dual-polarity voltage and give a varying output on both the rails. The two MOSFETs, here IRFB5615pbf, are controlled simultaneously. The voltage on each rail will therefore be identical to the other, relative to ground, but with opposite sign. Since the MOSFETs will operate in the same frequency range and handle roughly the same voltage, they are of the same type as the ones already installed in the class D full-bridge configuration. The switches need to be controlled synchronously to be able to give a balanced output to the class D output stage. Otherwise, if there would be voltage levels on high and low rail, the output stage would not work properly [2].

The switching frequency of the buck switches were tested and evaluated and the analysis is presented in Section 4.4. The frequency is important because it affects the current and voltage ripple, as well as the component size. Moreover, it also affects the switching losses during a set period of time. This results in a compromise between a low switching frequency, that produces a ripply output but with low switching losses, and a high frequency, with smoother output but with higher losses.

The component size of the capacitor and inductor in the low-pass filter, supplying the output stage, also affects the voltage and current ripple. A larger capacitor would, for example, make the voltage ripple smaller, in the same way as increasing the switching frequency. The cost of the component goes up with size which leads to compromises regarding the selection. An iterative process to obtain the most suitable values were conducted and is described more thoroughly in Section 4.4. Furthermore, the diodes in this design are important to choose with care since they will handle the same current amplitudes as the inductors. In the design, they also need to be able to block more than 70 V plus they need to be very fast to work together with the buck switches. Since better diodes are more costly, the size and speed need to be kept low.

In the circuit layout presented in Figure 3.9, there is a steady flow of current supplied by the current limiter, which is the same circuit as explained in Section 3.1, but placed before the switches. The rail capacitors are also of the same size as before and are placed in connection to the limiter, before the buck converter. The supply current flows from the rail capacitor to the output capacitor of the buck converter during the on-time of the converter. This current is then delivered to the output stage of the amplifier. The size of Lb1 and Lb2 determines the size of this current. Too large and there will not be enough to supply the load, too small and excessive currents are drawn.

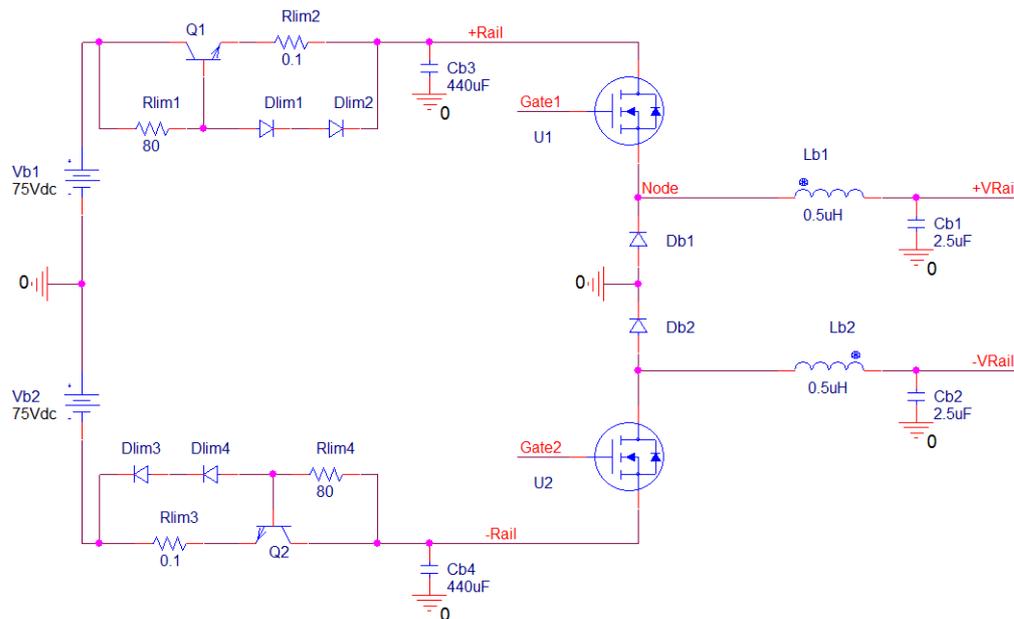


Figure 3.9: The final buck converter. Is controlled using feedback and synchronous switching.

4

Simulation analysis

THE designs were evaluated using simulation in PSpice and MATLAB. The result from both the class D amplifier itself, the rail solutions as well as the conjunction of the rail solutions and the class D amplifier are presented in this chapter. The simulations were done for both one channel and two channels using PSpice.

4.1 Simulation test-bench

Here the behaviour of the class D output stage, also called test-bench, is simulated and evaluated in idle mode and with medium voltage output. The numbers are presented for both ± 70 V rail voltage, which is the standard operation of the class D output stage, and ± 30 V rail voltage. The second level is just to have something to compare with when analysing the design solution and is not a possible mode for the test-bench in reality. All medium voltage output tests are performed with a similar power consumed by the load, at around 192 W. This makes comparing of solutions easier. If nothing else is stated, the higher voltage will be the reference as it is the standard operation.

4.1.1 Idle

In idle mode the input of the class D output stage is 0 V and the amplifier therefore attempts to put 0 V across the load. In the full-bridge converter, this is done by switching the MOSFETs with a 50 % duty cycle, since this equals zero on the PWM wave. However, this type of control results in a small voltage ripple across the output filter capacitor and the load. Because of this, a small power loss will occur in the load, the MOSFETs and the snubber circuits. Simulations with ± 70 V on the rails resulted in sine wave shaped ripple with an RMS voltage of 1.71 V and an RMS current of 216 mA in the load. The output signal produced can be seen in Figure 4.1. The same behaviour also occurred

with ± 30 V rails since the switching principle is similar. However, the voltage was 729 mV and the current 91 mA due to the lower voltage.

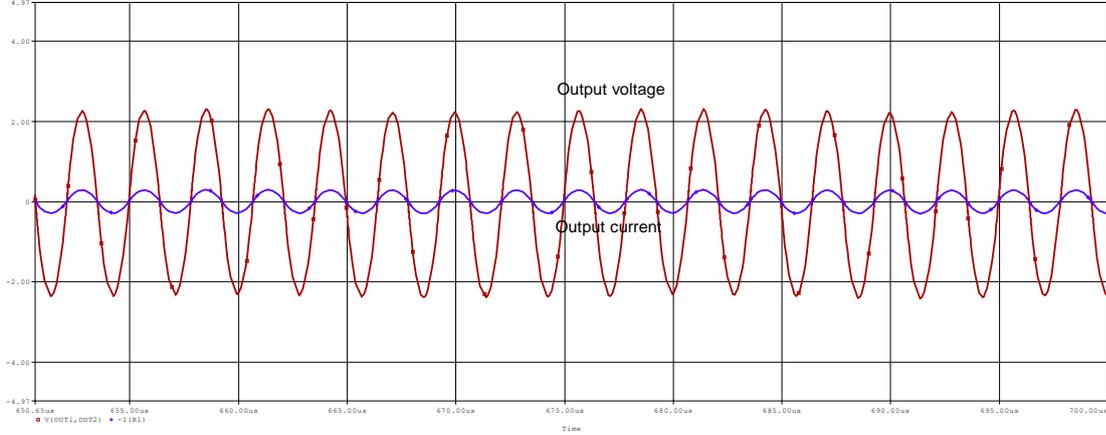


Figure 4.1: A small ripple of voltage and current through the load during 50 % duty cycle with ± 70 V on the rails. The ripple has a frequency of 350 kHz, same as the switching frequency.

The idle load losses were calculated by measuring the amplitude of the voltage and the current in the load with reference to Figure 3.2. The same was done for the snubber resistance. The losses in the MOSFETs were calculated by integrating the product of the voltage over them and the current through the MOSFETs. This was performed both during turn on, turn off and conduction. The calculations are similar to what was shown in (2.3) and the total losses can now be calculated as

$$P_{tot} = P_{sw} + P_{snubber} + P_{load} \quad (4.1)$$

where P_{sw} are the switching losses, $P_{snubber}$ are the snubber losses and P_{load} are the idle losses in the load. The MATLAB code for all calculations can be found in Appendix A.2. The result can be seen in Table 4.1, which summarizes the power input and power losses in the circuit. All power calculations are based on the RMS values of voltage and current. The total active power demand is 5.39 W for ± 70 V and 1.28 W for ± 30 V rail voltage. For a high rail voltage, more power is lost in every component present from input to output, compared to the low rail voltage.

The output filter acts as a reactive load and therefore a larger current than what is necessary will flow through the circuit. A better understanding of the power demand of the circuit was achieved by calculating the power input from the power supply as well as the total input through the switches. Using the ± 70 V rails, the total input power was 532.54 VA. Of these 4.23 VA was supplied by the power supply and the rest is therefore discharged from the rail capacitors.

Based on this information the reactive power consumed during idle operation can be calculated as

Table 4.1: The losses in the components of the amplifier for different rail voltage. All losses are for idle mode, using a duty cycle of 0.5

Component	Rail Voltage	
	+/-70 V	+/-30 V
Class D OPS Switches	4.40 W	1.13 W
Load	0.37 W	0.07 W
Snubber	0.62 W	0.08 W
Total Loss	5.39 W	1.28 W
Apparent input power from supply	5.59 VA	1.37 VA
Total apparent input power	533.65 VA	94.61 VA
Total reactive power	533.62 VAR	94.60 VAR

$$Q_{tot} = \sqrt{S_{tot}^2 - P_{tot}^2} \quad (4.2)$$

and resulted in a total reactive power of 532.51 VAR. Based on the result in Table 4.1 the active power is mainly supplied by the power supply, while the reactive power flows from the positive rail capacitor to the negative rail capacitor during positive half period, and vice versa for the negative half period.

From Table 4.1 the large difference in reactive power is due to the lower rail voltage. A rail voltage less than half the size of the original rail voltage leads to less than a quarter of reactive power when using the +/-30 V rails. The voltage ripple over the load is equal to the switching frequency, 350 kHz, resulting in a large inductive load. Since the amount of reactive power in the circuit is lowered for low rail voltage, the amount of current drawn is halved. This results in a quarter of the active power loss compared to the high voltage rails.

4.1.2 Medium output power

The test-bench was also evaluated for a medium output voltage, which corresponds to 60 V with around 192 W consumed by the load. This level was chosen to be able to compare the test-bench for both high and low rail voltage. In order to get a better understanding of the efficiency of the class D amplifier, an efficiency curve was plotted and can be seen in Figure 4.2. The curve is based on the the first model of the test-bench, presented in Section 3.1 which can be seen in Figure 3.1. The curve might therefore not be accurate compared with the real amplifier but was merely done to show the effects on efficiency when switching between high voltage rails, to low voltage rails.

As can be seen, the efficiency remains fairly constant for medium to high output and it is only at low output the efficiency goes down. The +/-30 V curve lies just above the +/-70 V curve at medium output, but for lower output there is more to gain in efficiency

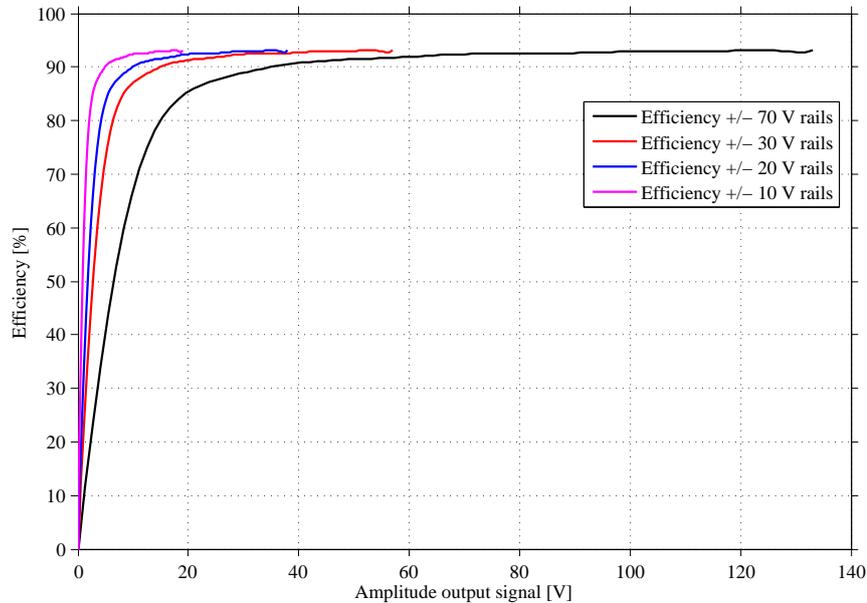


Figure 4.2: Efficiency of a class D converter. By applying a lower rail voltage high efficiency can be reached quicker for small output signals.

for the lower voltage level. A real class D amplifier will have a similar efficiency curve but higher losses overall, due to extra components.

For medium power output, the losses were calculated with a 1 kHz sinusoidal input signal. Both the high and low voltage rails were switched synchronously. The input voltage of the low rail was adjusted to ± 32.5 V, instead of ± 30 V, due to a voltage drop across the current limiters. The voltage drop would otherwise result in less power consumed by the load for the low voltage rails, compared to the high voltage rails. This would, in turn, make the levels hard to compare with each other. The result is summarized in Table 4.2.

From Table 4.2, a similar trend to what was shown in idle mode can be seen and all power losses are reduced for the low rails compared to the high rails. The power consumed by the load were approximately the same for both ± 32.5 V and ± 70 V, but the active power losses more than halved in the circuit. This is due to the fact that the current is the same for both high and low voltage, independent of the voltage level.

The switching losses were calculated over one period of the output signal, 1 ms. During this period, the current through the switches and the voltage over the them varies depending on where on the sine-wave measurements are performed. The power loss in the switch were therefore integrated over one period of the output signal, and

Table 4.2: The losses in the components of the amplifier for different rail voltages. All losses are for 1 kHz sine wave input. This produced a 55 V amplitude 1 kHz sine on the output.

Component	Rail Voltage	
	+/-70 V	+/-32.5 V
Class D OPS Switches	11.51 W	5.52 W
Load	192.93 W	191.27 W
Snubber	0.88 W	0.20 W
Total active loss	12.39 W	5.72 W
Total active power	205.32 W	196.99 W
Apparent input power from supply	203.61 VA	198.22 VA
Total apparent input power	433.41 VA	276.925 VA
Total reactive power	381.69 VAR	194.63 VAR

not over one turn-on and turn-off interval, as seen in the idle mode calculations. The reactive power that needs to be drawn from the rail capacitors is also less for +/-32.5 V, with 194.63 VAR compared to 381.69 VAR for +/-70 V.

4.2 Simulation Solution 1a

Design solution 1a was described in Section 3.2 and uses switching between two different rail voltages and can be seen in Figure 3.7 and in Figure 3.8. The solution was evaluated both for idle mode and with medium output. A 1 kHz sine wave was used as input and reference for all medium power calculations, similarly to the evaluation of the test-bench. Since the sine wave varies in amplitude over one period, the power output will also vary. This was also used to set an appropriate level when the switching of the rails takes place and the level was set to a value just below +/-30 V. The supply voltage feeding the low rail switches was slightly increased to compensate for the voltage drop over the current limiters.

The behaviour of the design solution 1a circuit is demonstrated in Figure 4.3. Here, the rail voltage represents both rails put together and this is why the voltage is doubled compared to 30 V and 70 V. When the input signal goes above the threshold value at around +/-30 V, the voltage on the rails is raised. Worth noting is that a small ringing is present in the output signal which probably can be suppressed even more if the feedback loop is polished further. The waveforms in Figure 4.3 uses synchronous switching of the rails.

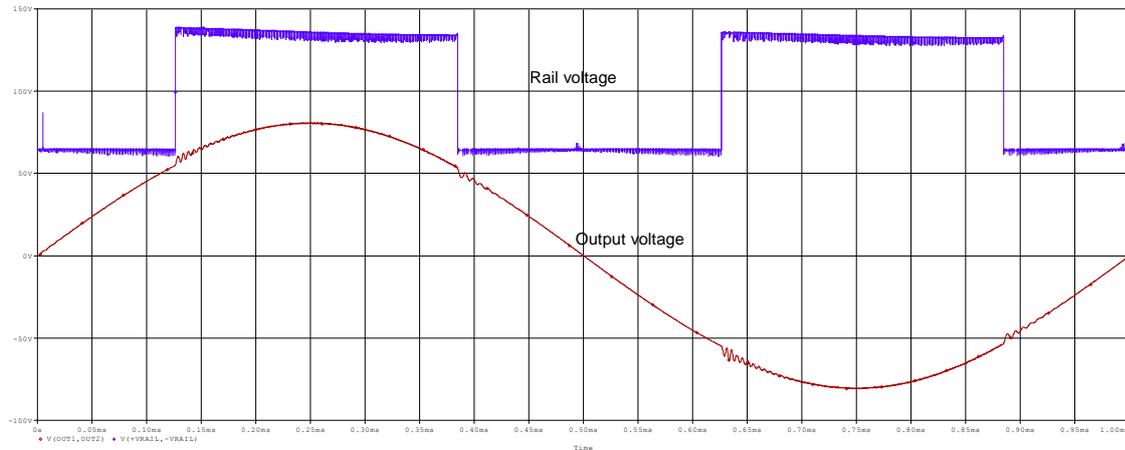


Figure 4.3: The behaviour of design solution 1a when switching between low and high rail. The output is close to a sine wave but there was a small ringing issue during the switch from low to high rail and vice versa.

4.2.1 Idle

The idle power consumption for solution 1 was close to what was shown for the test-bench, with ± 30 V applied, in section 3.1, since only the low voltage rails are active. The design also produced nearly the same current and voltage ripple over the load and this is because of the class D switches that always have a 50 % duty cycle in idle. The result should in reality be compared to the ± 70 V rail voltage of the test-bench. By doing this, the losses have decreased significantly. In Table 4.3 the power consumption figures are shown and can be compared with Table 4.1. There is a small extra power loss in the diodes of the low voltage MOSFETs, which are caused by a negative current in the circuit for some periods. This was explained in section 3.1.

In idle mode the class D amplifier benefits greatly from having a lower rail voltage. This was expected since the current remains the same while the voltage is decreased.

4.2.2 Medium Power Output

An evaluation of design solution 1 was performed when running the circuit with a medium output power level at 60 V. As mentioned before, the voltage supplying the low voltage rails was adjusted to a level of ± 31.5 V to compensate for the current limiter and to produce a power output of around 192 W. This makes comparison with previous results presented in Section 4.1 much easier. The power consumption and losses are presented in Table 4.4.

Comparing the result to what was presented for the test-bench reveals a slightly lower loss in the class D switches, with 9.88 W compared to 11.51 W for the test-bench. This was expected since the amplifiers spend time supplying the output from the low rails and was shown in Figure 4.3. However, there is power lost in the extra rail switches apparent in this design, but they only contribute with a small amount. Therefore, the

Table 4.3: The losses in the components of rail solution 1. Losses are for when the amplifier is in idle mode.

Component	Losses
Class D OPS Switches	1.15 W
High voltage rail switches	0 W
Low voltage rail switches	0.30 W
Rail Diodes	0 W
Load	0.07 W
Snubber	0.11 W
Total active loss	1.63 W
Apparent input power from supply	1.06 VA
Total apparent input power	104.72 VA
Total reactive power	104.71 VAR

Table 4.4: The losses in the components of rail solution 1. Losses are for when the output power is close to 200 W

Component	Losses
Class D OPS Switches	9.88 W
High Voltage rail switches	0.48 W
Low Voltage rail switches	0.08 W
Rail Diodes	0.16 W
Load	191.80 W
Snubber	0.36 W
Total active loss	10.96 W
Total active power	202.75 W
Apparent input power from supply	205.94 VA
Total apparent input power	356.93 VA
Total reactive power	293.75 VAR

overall active power loss in solution 1a is lower than running the full-bridge output stage with +/-70 V. The overall active loss was 10.96 W compared to 12.39 W.

A drawback with two rail voltages is that the solution require two sets of current limiters and rail capacitors to supply the load properly. The two sets of limiters is necessary because of the split supply and that a current protection advisable to have

from both supplies. Since less power is needed when the amplifier is connected to the low voltage rails, these rail capacitors can be relatively small at 50 μF . Moreover, the high rail voltage capacitors can be made smaller, around 220 μF , since they do not need to supply the circuit the same amount of time as before.

4.3 Simulation Solution 1b

The results for design solution 1b are expected to be similar to $\pm 70\text{ V}$ operation of the class D output stage when operated normally. Depending on the time constant and how much of the time the amplifier is operated in idle, the losses will decrease and be closer to what was presented for $\pm 30\text{ V}$ operation in Section 4.2. The solution is very simple but the total losses will not be lower than those of solution 1a. Moreover, it is generally hard to estimate how much of the time the amplifier will operate in idle and even harder to simulate since this would require very long run-times. Therefore, no simulations were conducted.

4.4 Simulation Solution 2

Design solution 2, consisting of the buck converter presented in Section 3.4, will here be analysed and validated based on simulations performed in PSpice. Before any measurements were performed, it was concluded that the switching frequency of the buck switches would influence the result. More precisely, it would influence the voltage ripple and the switching losses of the buck switches. Therefore a frequency sweep was performed and analysed.

4.4.1 Effect of switching frequency of the buck converter

In Table 4.5, the results from changing the switching frequency of the buck converter are presented. This include switching and conduction losses, current amplitude through output inductor and the voltage ripple in amplitude and percentage. The capacitor and inductor of the filter are of the same size for all frequencies, at 2.5 μF and 0.5 μH respectively.

As described in Section 3.1 the class D output stage of the amplifier used runs with a frequency of 350 kHz. If the buck converter would run with the same frequency the output would still be viable. The voltage ripple at 350 kHz is 13.12 % and is declining with higher frequency. However, as can be seen in Table 4.5, the switching and conduction losses are more than double for the highest frequency. There is a positive effect regarding the maximum current through inductor, which decrease with higher frequency and will in turn make it possible to choose smaller diodes. The average current was roughly the same at around 4 A for all the frequencies.

From the results it can be seen that the ripple amplitude decreased with a big step in the beginning and decreased with smaller steps as the frequency became higher. The most important part was to lower the size of the capacitor and therefore, a frequency

Table 4.5: The losses in the switches of the buck converter while changing the switching frequency. Losses are for an output power of close to 200 W and when the amplifier is putting out 1 kHz sinus. Switching losses include both switching- and conduction losses over one 1 kHz period.

Switching freq.	Switch power loss	Ripple amplitude	Percent	Max current
350.0 kHz	6.06 W	9.90 V	13.12 %	39.65 A
525.0 kHz	8.38 W	5.92 V	7.99 %	31.42 A
700.0 kHz	8.24 W	5.01 V	6.93 %	24.70 A
875.0 kHz	9.50 W	4.79 V	6.69 %	23.44 A
1.050 MHz	10.14 W	3.34 V	4.69 %	20.39 A
1.225 MHz	11.50 W	3.14 V	4.47 %	19.77 A
1.400 MHz	12.58 W	2.49 V	3.56 %	17.49 A

of 525 kHz was suitable and this level. This was tuned to 500 kHz to obtain a small decrease in switching power loss. This frequency, 500 kHz, was used for all the tests performed on solution 2.

Worth noting is that a voltage ripple no more than 1 % is good for a power supply [3]. In this implementation, the voltage ripple is of less importance since the buck converter is only feeding the output stage and is not the actual output. The class D full-bridge connection seems to be quite resistant to voltage ripple at its input and a large ripple works as long as it is at a level above what is put out.

4.4.2 Performance of the buck converter

The buck converter adjusts the rail voltage to a level above what is needed by the amplifier. Throughout one period, this level varies, but is as a minimum around 10 V above the output voltage. For all the figures presented in this section, the output voltage is at its maximum at 100 V. This was partly done to simplify the analysis and partly to show that there is no problem in doing this. The rail voltage follows the absolute value of the input signal, which was described in Section 3.4 and is shown in Figure 4.4. To run the class D output stage, the buck switches are controlled synchronously by the gate signals. The two rail voltages are therefore identical but with opposite polarity as seen in Figure 4.5.

The quality of the rail voltage was not as high as the quality of the output signal of the amplifier and had a ripple of around 8 V at most. This did not influence the quality of the output signal and the amplifier worked fine as long as enough power was supplied to it through the rails.

The behaviour of the current at the output of the buck converter can be seen in Figure 4.6. Here, the current through the inductor is shown, as well as the rail voltage. The rail voltage needs to rise above a certain level for the current to flow and it rises to

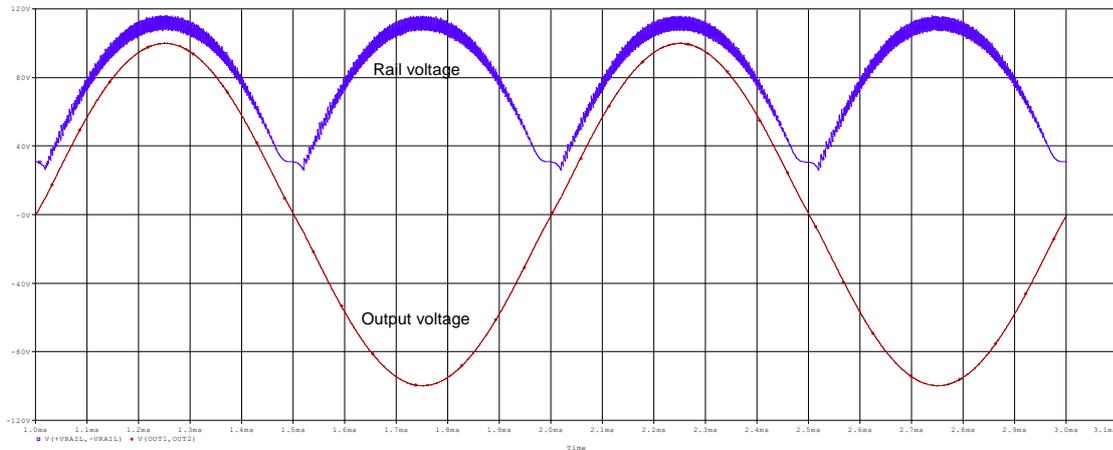


Figure 4.4: Voltage waveforms for the second solution. A buck converter adjusts the rail voltage to be close to what is needed. The two buck switches switch synchronously.

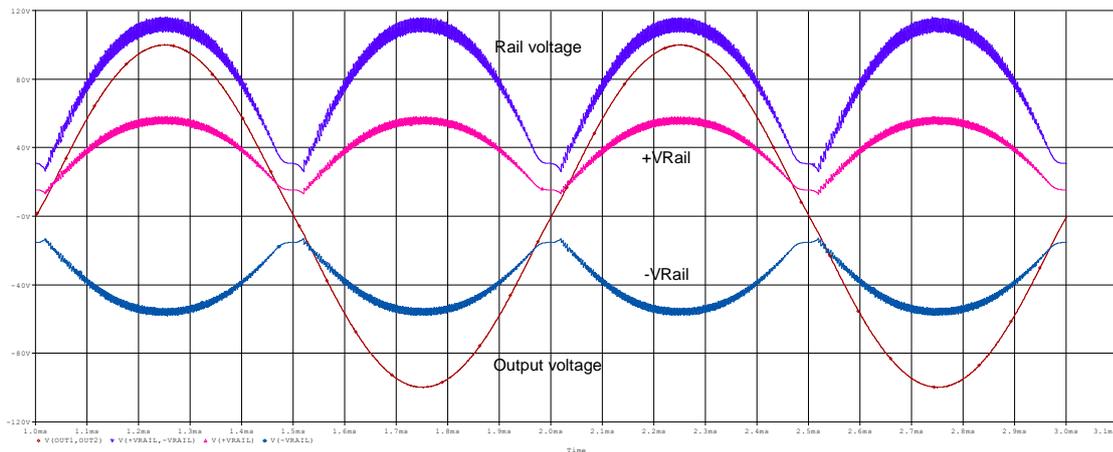


Figure 4.5: The result of using the buck converter when producing a sine-wave with 100 V in amplitude. Both the output voltage, the total rail voltage across the rails and the separate rail voltages are shown.

a peak value of 35 A as maximum. During the low voltage period, a current is supplied to the amplifier by the output capacitor of the buck converter.

Figure 4.7 shows in detail the current through the inductor and the buck converter diode respectively. During the on period of the switch, the current is supplied through the MOSFET and during the off period, a current is drawn from ground, through the diode. Both the MOSFET and diode current are supplied by the large rail capacitors. Worth noting is that the converter operates in Discontinuous Conduction Mode (DCM) and the current goes to zero before the next switching period.

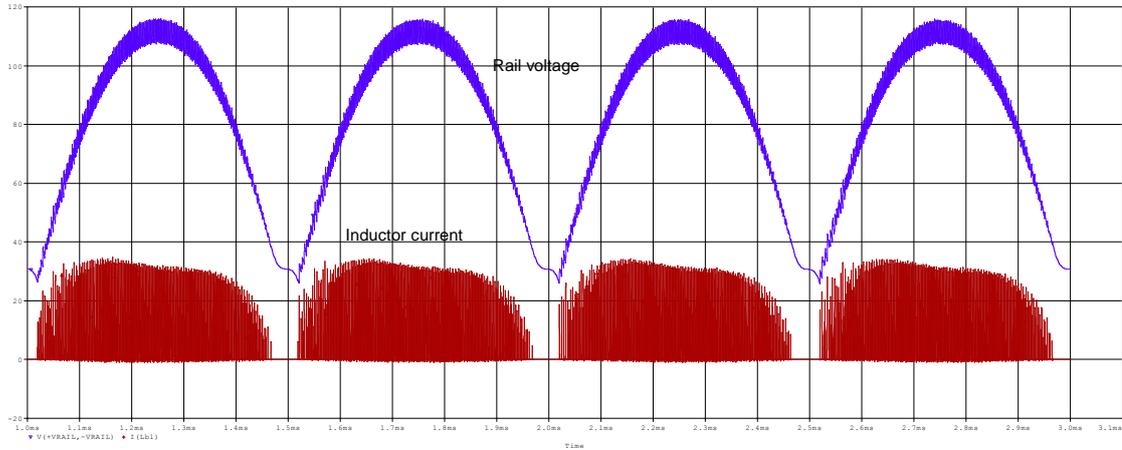


Figure 4.6: Currents through the inductor in the buck converter and the rail voltage.

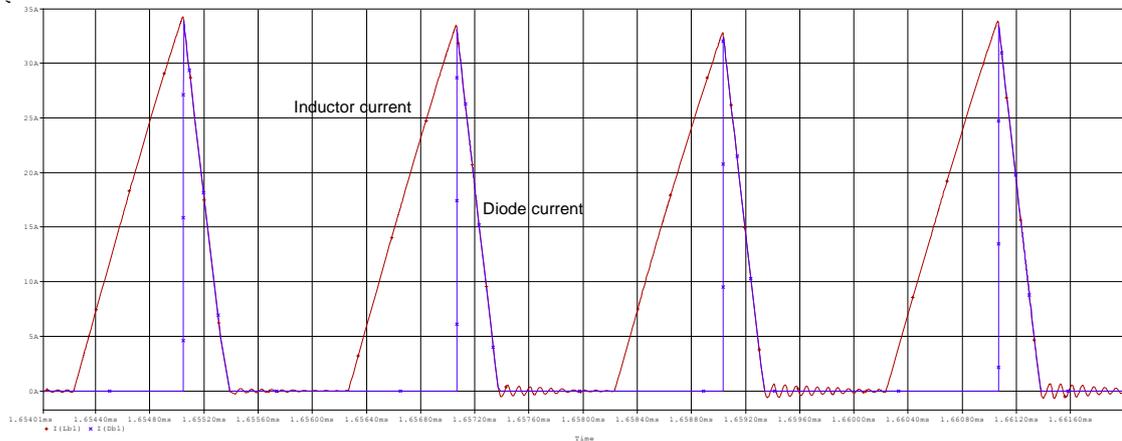


Figure 4.7: Currents through the MOSFET and diode in the buck converter

4.4.3 idle losses

For the buck converter, the losses when in idle was measured and calculated in same way as in Section 4.1, meaning that an input voltage of 0 V was applied. Measurements were performed both before and after the buck switches, as well as at the output rails. The results can be seen in Table 4.6.

The class D output stage requires some voltage to able to run properly. Therefore, the rail voltage was clamped at around 16 V as minimum, by using a simple voltage divider circuit. As can be seen in Table 4.6, there are considerably lower losses in all output stage components when the rail voltage was 16 V (+/- 8 V on each rail). The total losses for only the class D output stage, presented in Section 4.1 showed total losses of around 5.39 W at +/-70 V and 1.28 W at +/-30 V. For solution 2, the total loss for the whole circuit is 0.48 W.

Table 4.6: The losses in the components of rail solution 2. Losses are for when the amplifier is in idle mode.

Component	Power Loss
Class D OPS Switches	0.17 W
Buck Switches	0.29 W
Load	0.0054 W
Snubber	0.01 W
Total active loss	0.48 W
Apparent input power from supply	0.73 VA
Total apparent input power	7.97 VA
Total reactive power	0.54 VAR

4.4.4 Medium output power

Similarly as the test-bench, losses were also measured when running the converter with a medium output voltage of 60 V. The same test-points as in idle mode were used and the result can be seen in Table 4.7.

Table 4.7: The losses in the components of rail solution 2. Losses are for close to 200 W.

Component	Power Loss
Class D OPS Switches	4.73 W
Buck Switches	7.20 W
Load	191.96 W
Snubber	0.20 W
Total active loss	12.13 W
Total active power	204.13 W
Apparent input power from supply	253.70 VA
Total apparent input power	242.97 VA
Total reactive power	150.70 VAR

The result do not differ that much compared to the result for the test-bench. The total losses are 12.13 W for solution 2 and 12.39 for only the class D output stage. Similarly, a big part of the losses are switching losses and these are spread out over both the class D OPS switches and the buck switches. Worth noting is that the amount of reactive power in the circuit has decreased substantially.

4.4.5 Multiple channels

Simulations were also performed when the buck converter supplies two different class D output stages, which are creating two different output signals. One 1 kHz signal and the other 20 kHz. The amplitude of the two signals was around 100 V. The results can be seen in Figure 4.8, which shows the rail voltage and the outputs of the two channels and in Figure 4.9, where also the inductor current is visible.

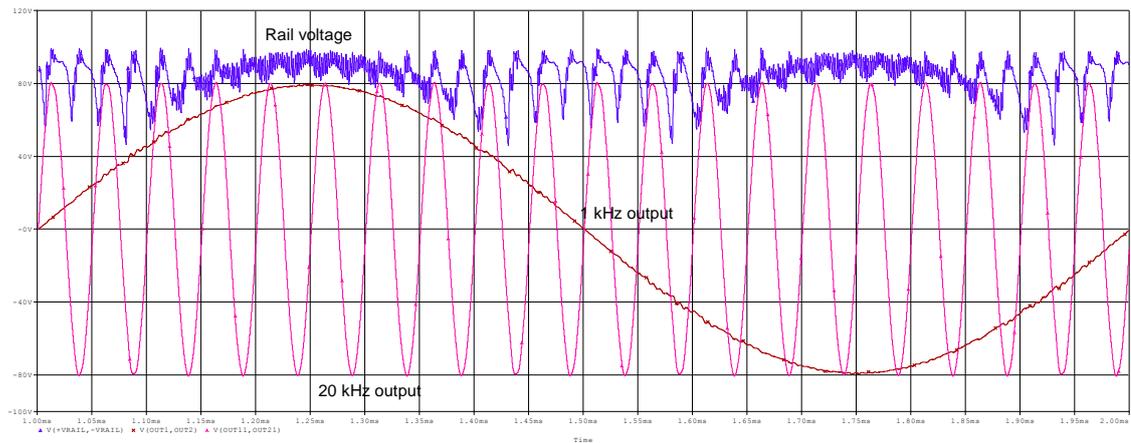


Figure 4.8: The result of using the solution 2 buck converter when supplying two separate output channels. Both channels and the total rail voltage are visible.

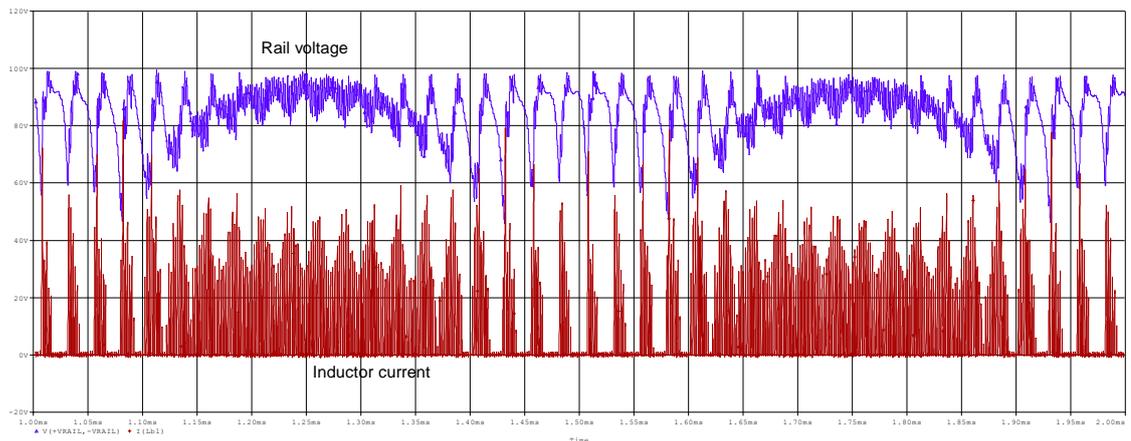


Figure 4.9: The resulting current through the inductor in the buck converter when supplying two separate channels.

4.5 Design solution comparison

A summary of the idle and medium power losses for the test-bench, solution 1a and solution 2 can be seen in Figure 4.10. The values have been placed next to each other to highlight the differences. As already seen, both solution 1a and 2 succeeded in lowering the idle power losses quite drastically. For solution 2, the idle losses are very low and might not be fully accurate in reality. Data for solution 1b is not present here. In chapter 4, no actual measurements were performed on this solution and the losses were considered to be a mean of solution 1a and the real class D output stage. This will also depend how much time is spent in idle mode.

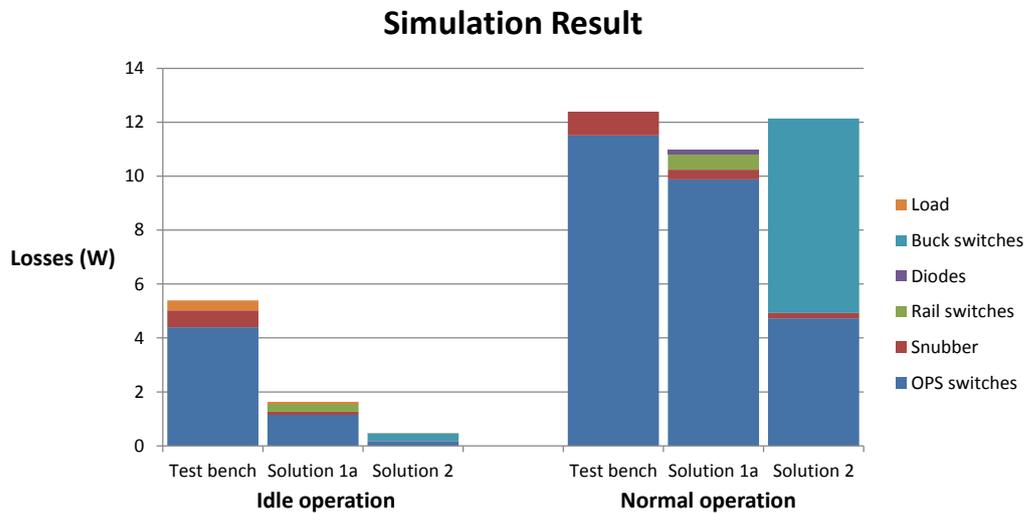


Figure 4.10: The summary of the consumption losses for the different design solutions.

By examining Figure 4.10, it can be seen that the final simulated designs had a lower consumption also in medium power output, compared to the test-bench. This is a very positive result and should mainly be due to the fact that the rail voltage follows the input more closely, putting out lower voltage when possible, even for higher outputs. Before the analysis was conducted, one concern was that the losses would increase for higher outputs. This concern came from the fact that an extra switching stage is present in all the design solutions just before the class D output stage. The result shows that this concern was false.

5

Prototype building

TO prove the concept designs that were produced and analysed using MATLAB and PSpice in Chapter 3 and 4, a prototype of design solution 2 was built. This chapter contains practical implementation theory regarding PCB layout and component considerations and selection. The PCB was implemented using DesignSpark [12], which is a free-of-charge schematic capture and PCB layout program from RS Components and EDA software developer Number One Systems. In addition, the prototype was evaluated with regard to the actual and the simulated performance.

5.1 Practical theory

Here, theory behind implementing a simulated design from PSpice to a practical circuit will be presented. This includes how to practically generate PWM signals, how to control MOSFETs with an IC and how the final circuit is built.

5.1.1 PWM generation

The feedback circuit used for the buck converter is a proportional controller, meaning that a fraction of the positive rail voltage is fed back to a differential amplifier. The fraction of the fed back rail voltage is subtracted from the reference, which is the rectified input audio signal. The resulting error is then amplified and compared to a triangle wave generated by an oscillating circuit.

The oscillating circuit can be seen in Figure 5.1 and is a bistable multivibrator. The triangular wave is created by connecting an amplifier, with a gain greater than one, in a positive feedback loop [10]. A fraction of the output of the amplifier is fed back to the input using a voltage divider and is expressed as

$$\beta = \frac{R_1}{R_1 + R_2} \quad (5.1)$$

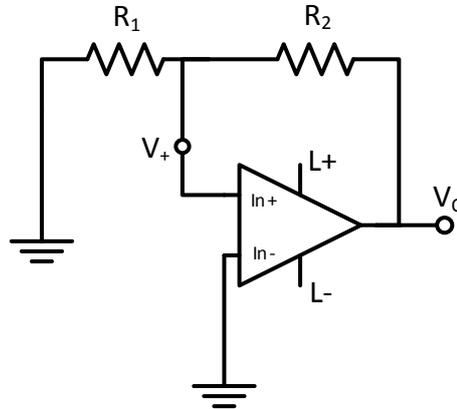


Figure 5.1: Circuit diagram of the bistable circuit. The voltage V_o will increase until it saturates at $L+$, if a voltage higher than of V_+ is applied at $In-$, V_o will decrease until it reaches $L-$.

where R_1 and R_2 are the resistors in the circuit. Because of this, the amplifier will keep amplifying the output until it saturates.

The circuit will change state if a voltage larger than $V_+ = \beta L+$ is applied to the negative terminal, which causes the output to decrease until it saturates in the negative direction, at $V_o = L-$ [10]. Now $V_+ = \beta L-$. To change state again, the voltage at the negative input must decrease and become negative until its lower than $V_+ = \beta L-$, otherwise the circuit will keep its current state. This makes $V_o = L+$. The property of the bistable circuit can be used to create a triangle wave generator by connecting an integrating circuit to the oscillator. The circuit can be seen in Figure 5.2.

The slope of the triangle wave is determined by changing the values of the resistor R_{tri} and capacitor C_{tri} and the slope can be described by

$$Slope = \frac{L+}{R_{tri}C_{tri}} \quad (5.2)$$

where L_+ is the saturation level of the bistable circuit. Note that the bistable circuit in Figure 5.2 is of the non inverting type. The amplitude of the triangle wave is determined by the fraction β in (5.1), as this determines the threshold voltage where the bistable circuit changes direction. A PWM signal is created by comparing the triangle wave with the amplified error, in the same way as was explained in Section 2.1. This PWM signal is fed to the gate controller IC. Datasheets of the op-amps and comparators can be found in Appendix A.1.

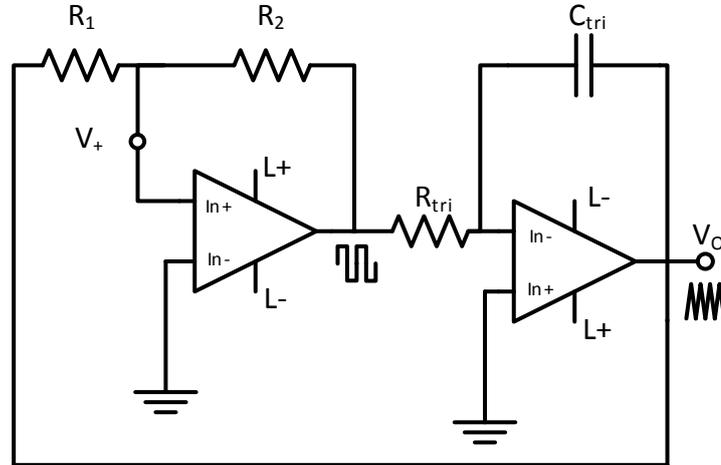


Figure 5.2: Circuit diagram of the triangle wave generator. The bistable circuit is connected to an integrator. The output of the integrator is then fed back to the bistable circuit, causing a triangle wave at V_o .

5.1.2 Gate driver

In order to open and close the two MOSFETs in the buck converter, a proper voltage needs to be applied on their respective gates. It was determined that a gate-source voltage of 15 V was appropriate to close the switches. This guarantees a maximum current through the MOSFET, as seen in the datasheet in the Appendix A.1. The source voltage of the high MOSFET varies depending on whether the MOSFETs or the diodes are conducting. This results in a source voltage that oscillates between +75 V and around zero volts and is a problem when controlling the high switch. The simplest way to solve this problem is to use a controller circuit that utilizes a bootstrap capacitor.

The bootstrap technique allows a very high voltage to be applied to the gates of a MOSFET, but still keep the gate-source voltage at a fixed value. The principle can be seen in Figure 5.3. A bootstrap capacitor, C_{boot} , begins charging when the node V_s is pulled to ground through the lower MOSFET. The capacitor is charged through the bootstrap diode and bootstrap resistor and the path is shown in green in Figure 5.3. When the upper MOSFET closes, the node V_s is pushed up to the DC supply voltage. Since the bootstrap capacitor cannot discharge through the diode, it will discharge through the path marked in red. The voltage across the capacitor will always remain the same but the node V_b , along with V_s is pushed up to a voltage $V_s + V_{boot}$ relative to ground. Therefore, the MOSFET can remain closed, even though a very high voltage is applied at its source.

Many controllers use the bootstrapping technique and there exists controllers for both buck converters and half-bridges. Both are appropriate for the set-up used in this

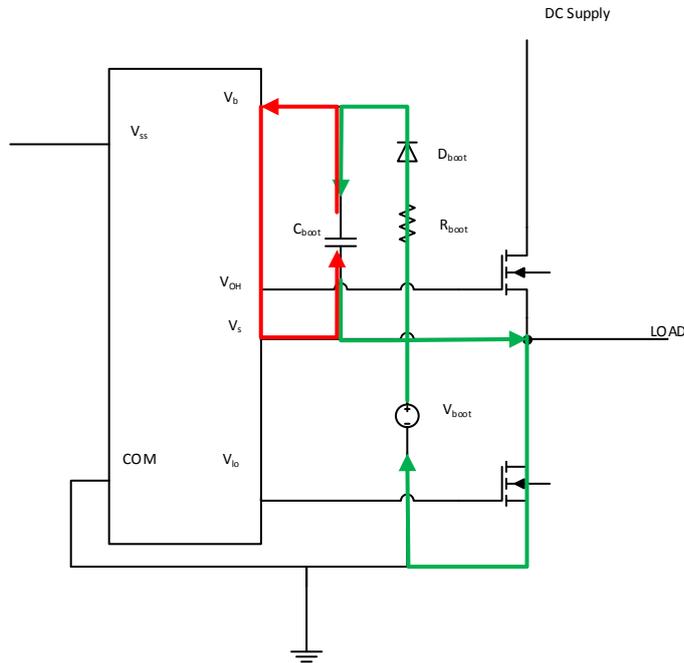


Figure 5.3: Circuit diagram of a bootstrap circuit. The charging path is shown in green and the discharging path is seen in red.

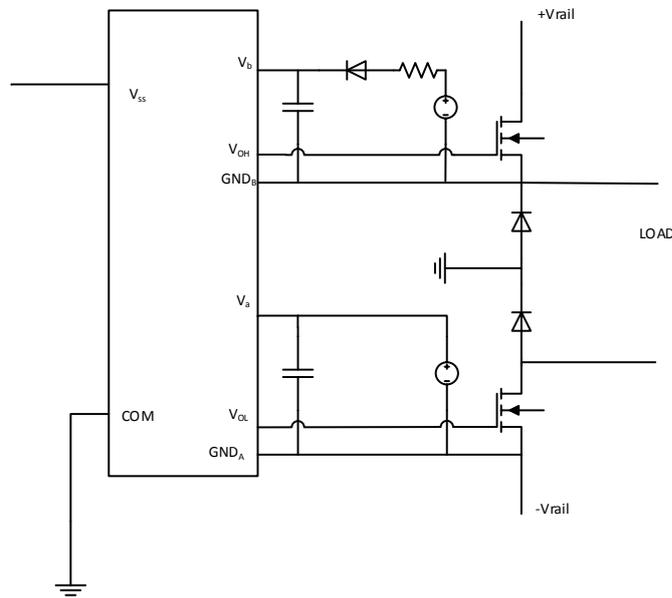


Figure 5.4: Circuit diagram of the bootstrap circuit. The capacitors that keep the voltage at 15 V above GND_A and GND_B is visible, as well as the resistor and diode.

project. However, using two separate controllers designed for buck converters proved to be a bad alternative here. The input side and the output side usually requires a connection to the same ground, or at most a few volts apart. Since the two source voltages are at least 70 V apart at all times this would mean two separate PWM signals would be required, or else the input of the controllers would not be able to function properly.

The chosen controller, ADuM3223, is a half-bridge topology and uses galvanic isolation between the input and the output. This means that the controller has three separate grounds, one for the input, one for the low output and one for the high output. This makes it possible to use one voltage level for the PWM signal that is appropriate for the op-amps and comparators and one voltage level for the control of the MOSFETs. The controller set-up with bootstrap capacitors can be seen in Figure 5.4. This set-up uses two separate bootstrap capacitors, supplied with two separate charging voltages. Both at 15 V above the two MOSFET sources respectively.

The power consumption of the controller was calculated based on Figure 5.5 and Figure 5.6. These show the input and output current required to drive the 2 nF load. The input capacitance of the MOSFETs used in the converter is 1750 pF according to the datasheet in Appendix A.1. Since the input voltage $V_{in} = V_{DD1}$ was set to 5 V and the desired frequency was 500 kHz, the input current I_{DD1} could be obtained from Figure 5.5. The output currents I_{DDA} and I_{DDB} could be obtained from Figure 5.6 by knowing the desired output voltage $V_{out} = V_{DD2}$ of 15 V. Now, the total power consumption for the controller was calculated as

$$P_{controller} = V_{in}I_{DD1} + V_{out}I_{DDA} + V_{out}I_{DDB} \quad (5.3)$$

This gave a total power consumption of 0.64 W.

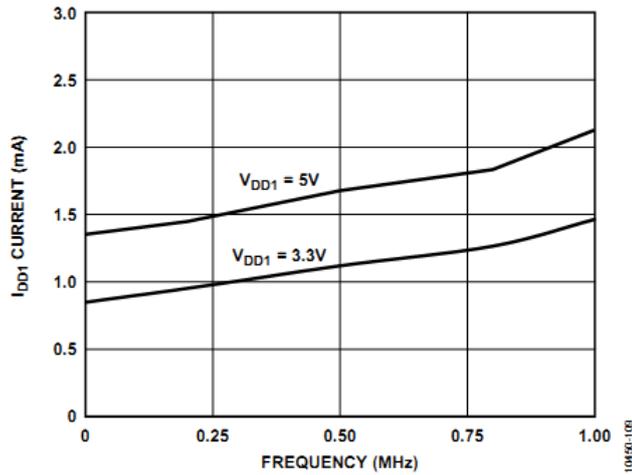


Figure 5.5: Input current of the controller as a function of switching frequency for the two available input voltages. V_{DD1} is the voltage required to drive to controller.

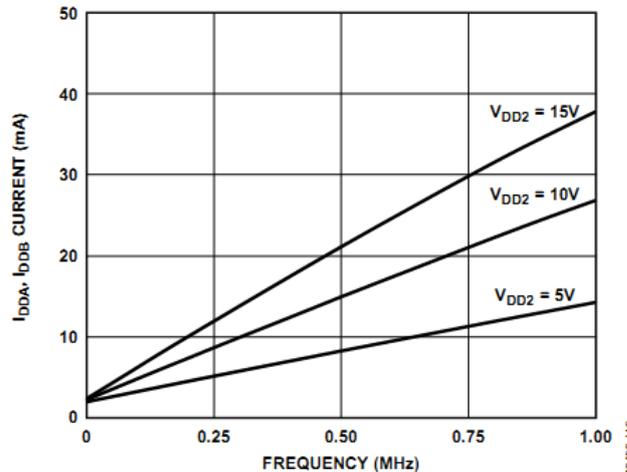


Figure 5.6: Output current of the controller as a function of switching frequency for three different output voltages.

5.1.3 PCB layout

The buck converter circuit produced in PSpice needed to be transferred to a practical circuit. Here, the procedure was to produce the circuit on a printed circuit board (PCB). When it comes to planning the layout of the PCB, there are several design considerations that must be fulfilled for it to work properly. One of the most important considerations is to have several layers to separate and shield the noisy power traces and components from the small signal traces. Otherwise the power layer that transport high current will affect the small signal layer, leading to unwanted behaviour of the circuit [13]. The separation can be accomplished by inserting a ground plane between the power layer and the small signal layer, providing the required shielding.

In reality, the design has 4 layers, placed in the order: power, ground, VCC and small signal layer. The VCC layer, or control layer, mainly controls the power supplied to the IC and op-amps which require voltages of around 15 V but not much current. Therefore they will not affect the small signals very much [13].

The designed buck converter, that is transformed to the PCB, will transport high current in the main current loop, which consists of the MOSFETs, the diodes, the low-pass filter and the load. To handle this, the power layer of the PCB should have short and wide current traces. This will minimize PCB inductance, resistance, voltage drop and work as heat sinks to keep the temperature down [13]. Since the buck converter is a switching device, a high pulsating current will be present in the switching node. This makes the large traces critical for the high di/dt current [13].

Parasitic inductances are always present in a real PCB and the pulsating current will radiate magnetic field and generate large voltage spikes and ringing. Therefore, it is also important to place the components that are connected to the switching node very close to each other to minimize the effective pulsating current loop and thereby the parasitic

inductance [13]. In addition to these considerations, it is also important to connect the power components to large copper pads, or use several vias, to minimize inductance even further.

As previously mentioned, the power traces and components are very noisy and can affect the rest of the circuitry in a negative way. Therefore, it is preferable to place the control circuitry a bit away from these large traces. Especially the IC should not be placed closer than 13-25 mm from the power MOSFETs and inductors [13]. On the other hand, the gate drive traces should be short and wide to minimize the inductance. The gate driver traces, consisting of the gate signal and the source signal, should also be coupled together so that the loop created is kept small.

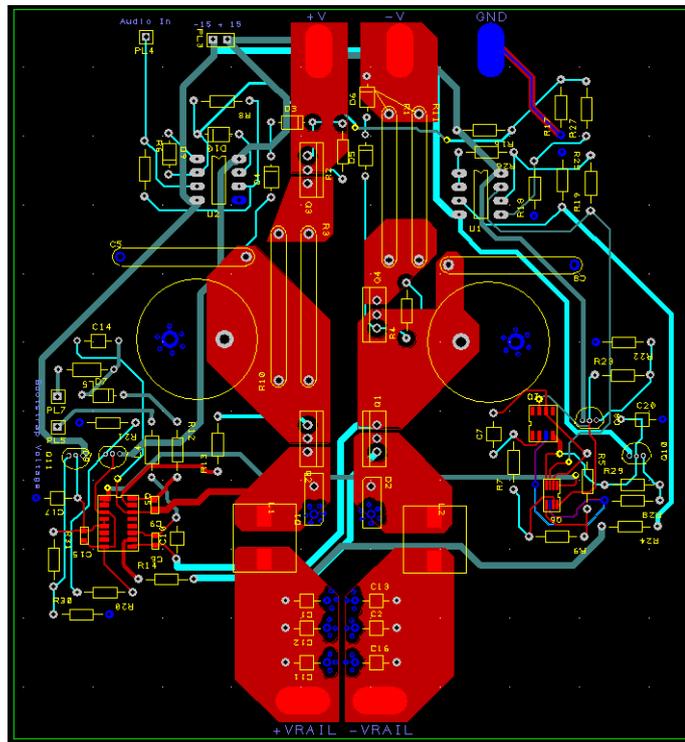


Figure 5.7: The final PCB layout created in DesignSpark. Each color represents a separate layer.

In Figure 5.7, the final design of the PCB is presented. Here, the short and wide power traces are dark red and are placed on the top layer, in the middle of the board, closed to each other. The light red ovals, plus the blue one, are connections for the power supply and for the load. The VCC traces are dark blue and the small signal traces are light blue and both are separated from the power layer with a ground layer that is not visible here. In the bottom left corner the IC is placed on a safe distance from the power MOSFETs and inductors. To the bottom right the PWM generation is performed which in turn is connected to the op-amps located at the top corners. Due to problems regarding routing of the signals in the last two layers, they share some of the

traces between them.

The ground layer, that is located between the top power layer and the two signal layers at the bottom, is shown in Figure 5.8. It was important to have a small separation between the switch node ground and the ground for the rest of the circuit. The switch node ground has a very high pulsating current that will otherwise affect the other components. With this solution it is almost guaranteed that the high pulsating current only are present in the power components.

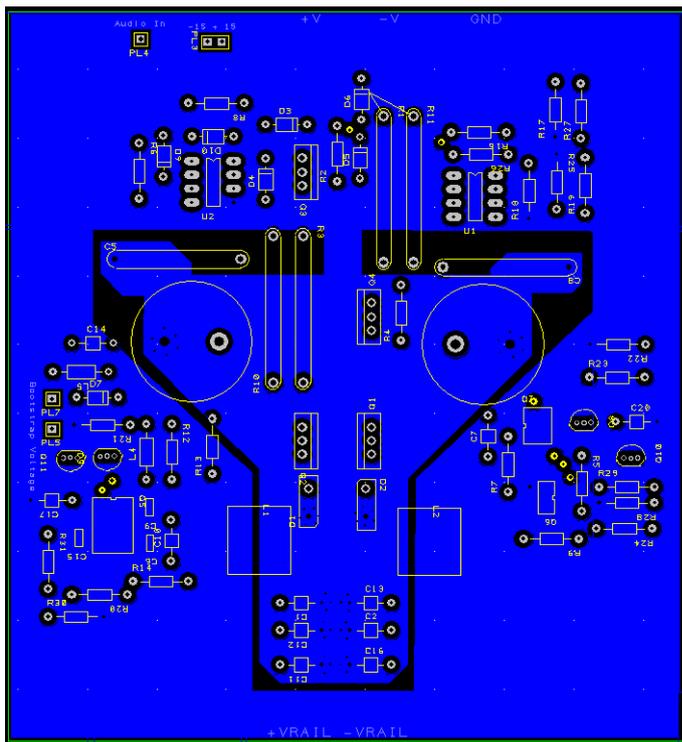


Figure 5.8: The final PCB layout, ground layer, created in DesignSpark.

For the PWM generator, several op-amps were used. The triangle wave generator consists of a comparator of the type TLV3202, creating a precise square wave, and an op-amp of the type OPA365, used for integration and creating the final triangle wave. The op-amp MC33078PG was used for the feedback circuit, the full wave precision rectifier and the error amplifier. The triangle wave and the amplified error signal was then compared using one more TLV3202, creating the final PWM signal as input to the IC. Datasheets of all op-amps and comparators can be seen in Appendix A.1. Moreover, voltage regulators were used to obtain suitable voltage levels to operate the comparators and op-amps in the PWM generator and precision rectifier. These are of the type LM317L and LM337L and the datasheets can also be found in Appendix A.1.

The resistors in the current limiter are power resistors able to withstand 5 W each. The current through these is usually around 7 A. Given their size of 0.1Ω , it was determined to use two 0.27Ω power resistors in parallel. This still makes them capable

of operating up to 5 W, but the current through them is halved and therefore gives the current limiter some headroom. The schematic of the PCB layout shown in Figure 5.7 and in Figure 5.8 can be seen in Figure 5.9. Here, all the components and circuits that has been mentioned in this section is shown.

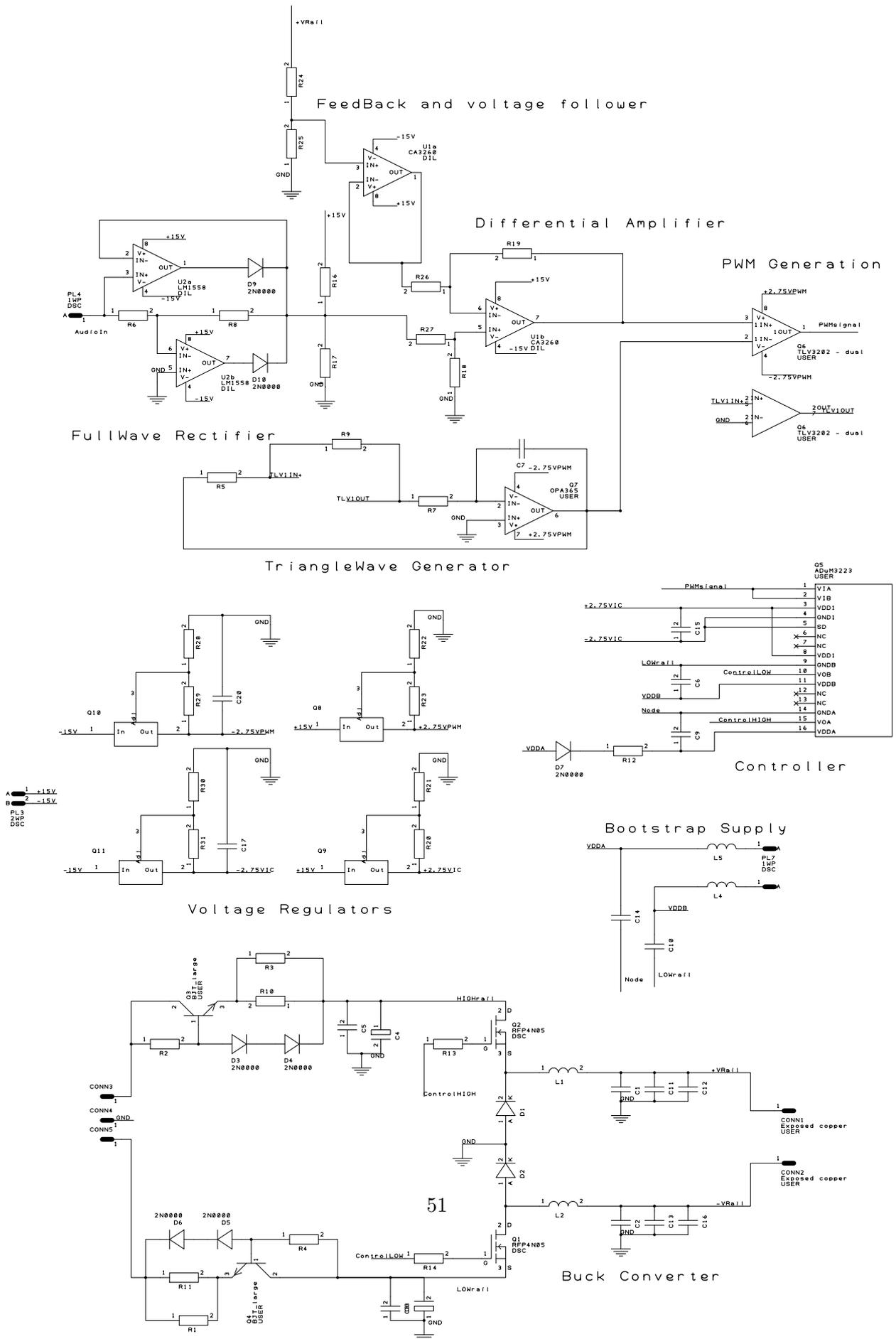


Figure 5.9: The final PCB schematic created in DesignSpark.

5.2 Prototype analysis

The final printed circuit board can be seen in Figure 5.10. It measures almost 12.5 x 13.5 cm. Here, all the component locations and connections on the top layer is visible.

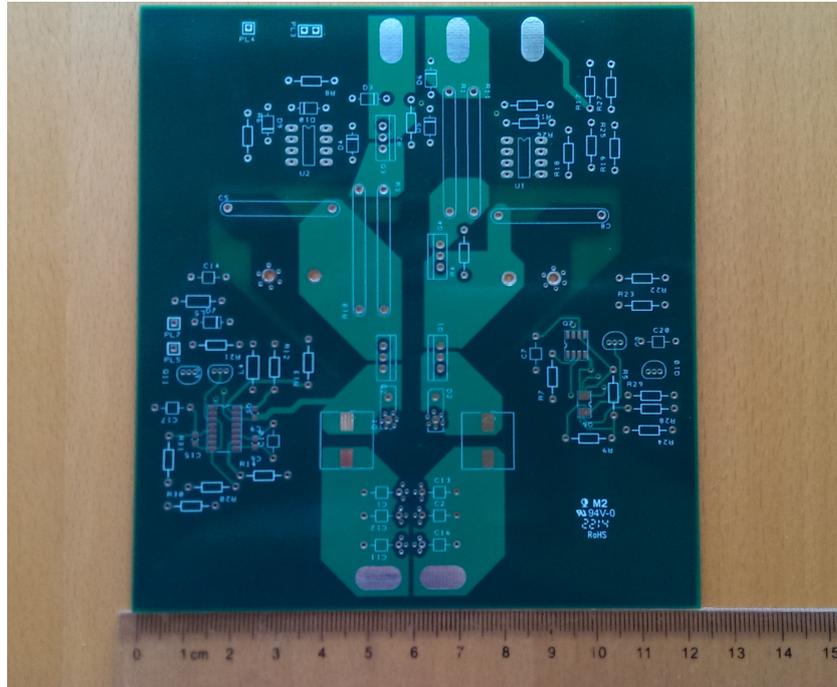


Figure 5.10: The PCB without components soldered on.

The different segments of the board were constructed one by one and tested as they were completed. The triangle wave generator and the audio rectification, as well as the amplification, were the main blocks of the controller circuit that could be tested individually. The resulting waveform from the triangle wave generator can be seen in Figure 5.11.

The waveform of the PWM signal, generated by the triangular wave and the audio input signal, should now be a square wave. To test this, the audio signal was first set to zero volts which would result in a PWM signal with 50% duty cycle. This PWM signal can be seen in Figure 5.12. The audio signal was then raised and this resulted in a PWM signal with larger duty-cycle.

In Figure 5.13, the finalized version of the board is shown. All the components plus the connections to the power supply and the load have been soldered. The board placement was a bit optimistic and the components turned out to take more space than first expected. Therefore, some extra modifications were necessary and that is why the small noise removal caps are of different types. However, their size and specifications are the same and should not affect the result.

At this point issues occurred at the output, the load was a 12 k Ω , 2 W, resistor.

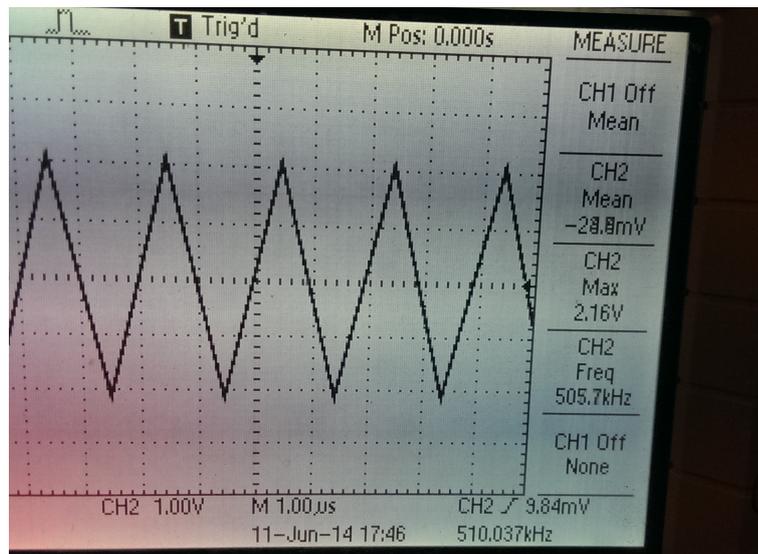


Figure 5.11: The triangle wave created by the oscillating circuit. The frequency varies a bit according to the oscilloscope, but is centred around 500 kHz.

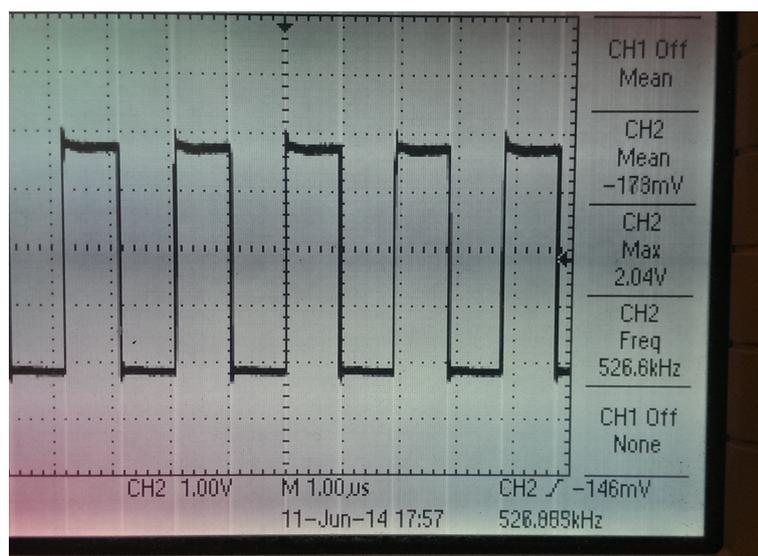


Figure 5.12: The resulting PWM signal from the controller circuit.

Since the current can't be too large, the size of the load was oversized substantially. However there was only DC output at frequencies above 500 Hz. This may be due to the extremely small amounts of current being drawn by the load. Unfortunately no more tests could be performed as the controller to the MOSFETs broke during measurements. Probably due to accidentally short circuiting when measuring, or similarly, and there was no time to replacing it and do new tests.

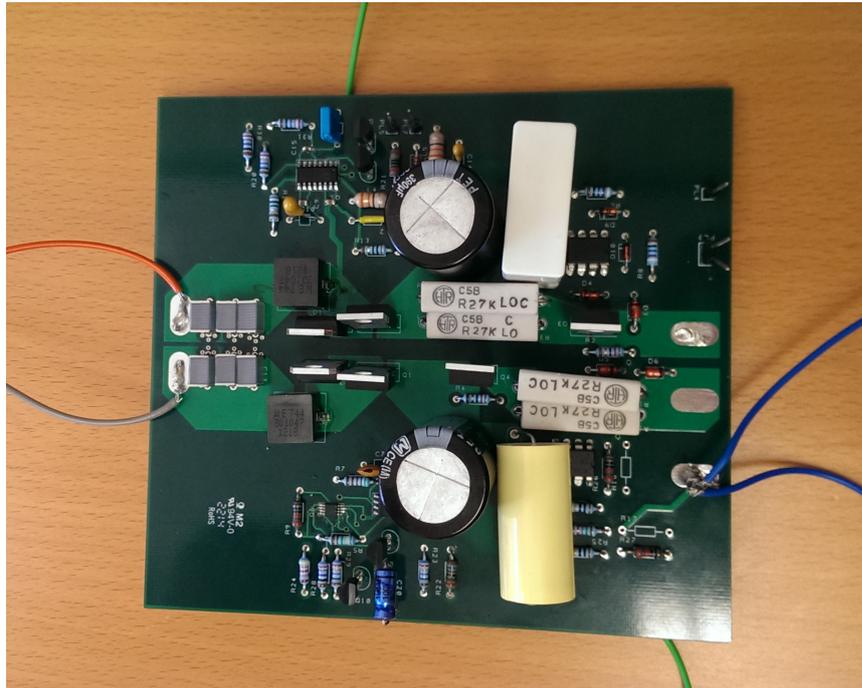


Figure 5.13: The finalized PCB with all the components soldered.

The cost of the components, without any optimization with regard to cost, was around 350 SEK. This does not include manufacturing of the board itself. Some of the components was already available at Company A and these are not included in the cost mentioned. It is very likely that the cost will decrease significantly as the number of boards manufactured increases. All components were ordered from either ELFA or Farnell.

6

Discussion and conclusion

IN this report, primarily two solutions have been designed and analysed with the regard to the idle power consumption losses. Both of the designs succeeded in lowering idle consumption and they both had lower losses than the original class D output stage when operating with medium power output. A sub-design was also built upon the first solution, but with a simpler control circuit. It was decided to implement design solution 2 as a real circuit in order to test it, as it had the most interesting behaviour. It was also the most interesting of all the solutions. Because of this, solution 2 was transferred to a prototype design that was implemented on a PCB.

6.1 Discussion

As was presented in Chapter 4, the losses were lowered both in idle and for medium power for both solution 1a and solution 2. This was in comparison with only the class D output stage and was a very positive result. A possible drawback in practice is the extra space that is required to implement all the solutions in the real casing. Here, special consideration regarding which design that best fits in reality should be done. Design solution 2 showed the positive results regarding the idle losses but is more complex and might take up more space than solution 1a. The simplest design would be solution 1b since it only needs a turn-on signal and the control circuit will therefore be quite small.

Both solution 1a and solution 2 uses the same MOSFETs that is present in the class D output stage and therefore no strange behaviour should be seen regarding the reliability. Solution 1a will at most switch 4 times the frequency of the input signal, putting little stress on the switches. For solution 2, the switches operates at 500 kHz and might therefore age a little faster than the class D OPS switches operating at 350 kHz. The switching level is, however, far from the limit of the MOSFETs and a level of 500 kHz should therefore not contribute significantly. The thyristor design in solution 1b basically switches very seldom, under low-stress conditions and because of this the

reliability should be very high.

The only solution that was transferred to a prototype design was solution 2. The cost associated with the prototype will be higher than a fully optimized mass produced design, because of high unit price when ordering single components. When ordering large quantities, the price can be around half of the unit price. The total price for all the components ordered was around 350 SEK but can be made much cheaper by ordering many of them. This price also comes from the fact that the components are of good quality and need to handle relatively high current. No cost calculations have been presented for solution 1a and 1b since they were not transferred into prototypes. The final price for those designs should be marginally smaller than solution 2 due to practically the same parts but fewer of them.

The prototype buck converter had a functional PWM signal generation and was able to produce a proper output for frequencies below 500 Hz. Above this frequency only constant DC voltage was produced. However, tests were only performed on a large, 12 k Ω , resistive load, in an attempt to keep the current low. The current was most likely too low for the converter to work properly. Shortly thereafter the MOSFET controller broke and no further tests could be performed. Proper testing on a 4 or 8 Ω load is necessary to be able to draw correct conclusions regarding the converter.

The thermal considerations for solution 1a and 1b should be quite small. These designs do not switch very often and the switches will therefore need less cooling than the class D OPS. Solution 2 switches faster and might need some special consideration but it should not be hard to manage. For high power, the current will be high and the power traces on the PCB will need to be wide short. However, this is true when only using the class D OPS as well. The more channels the converter is designed to supply, the higher the current will be. As was seen in Section 4.4 a minor test was run with two channels. This means more current through the MOSFETs, therefore more cooling and optimization of the PCB traces will be required.

The class D OPS can remain largely intact when installing the extra components in the design solutions. The only modification that needs to be done is regarding rail capacitors that need to be located before the design solutions.

No testing of the idle losses in the real class D OPS has been performed but instead the simulated test-bench has been used. This was built to represent its real counterpart as closely as possible, containing the same set-up and components. The only thing that is not present in the simulation set-up was the IC in the real design. This might have caused some differences in the gate control but should not be a significant change. Moreover, even if the losses are a bit different in the real class D OPS, all the solutions have been tested and compared against the simulated test-bench and the ratio should therefore be maintained.

6.2 Conclusion

It is possible to lower the idle power loss in the amplifier by designing a rail switching solution. All the designs in the project succeeds in lowering the idle power consumption

at no expense of the efficiency in normal operation. The choice therefore comes down to complexity, cost and possible thermal considerations.

Solution 2 may be the better choice when it comes to efficiency, but this requires more consideration when it comes to cooling due to the switching losses in the MOSFETs. Also this design has a more complex control scheme and may therefore be harder and more expensive to implement. The actual material cost from building the prototype based on this design was around 350 SEK, without board and some of the components. The design cost will be much lower if the design is mass produced. The results from the measurements performed on the prototype showed that the PWM signal generation and surrounding control circuits worked. The power path was also intact, however only DC output could be achieved for frequencies above 500 Hz.

Solution 1a has a much simpler design and will not need much consideration regarding cooling. The efficiency is not as good as for solution 2 and it produced some ringing on the output audio signal. However, the ringing can be suppressed by using a better feedback loop. This design was not transferred into a prototype and therefore, no exact numbers regarding actual efficiency and cost can be presented.

The modifications that needs to be performed on the actual class D amplifier is to move the rail capacitors and to make room for the design solutions.

6.3 Future work

Future work should continue evaluation of the designs to gain even more in efficiency, cost and size. Moreover, the control for all solutions could possibly be made even better and could potentially remove the ringing in the output of solution 1. The performance of the solution 2 prototype needs to be investigated more and with a real speaker, or similar 4-8 Ω load, working as a load.

A

Appendix

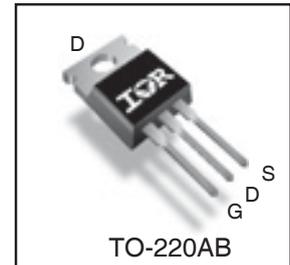
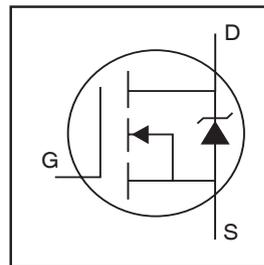
A.1 Datasheets

Here, the datasheets over all components used in design solution 2 is presented.

Features

- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low $R_{DS(ON)}$ for Improved Efficiency
- Low Q_G and Q_{SW} for Better THD and Improved Efficiency
- Low Q_{RR} for Better THD and Lower EMI
- 175°C Operating Junction Temperature for Ruggedness
- Can Deliver up to 300W per Channel into 4Ω Load in Half-Bridge Configuration Amplifier

Key Parameters		
V_{DS}	150	V
$R_{DS(ON)}$ typ. @ 10V	32	mΩ
Q_g typ.	26	nC
Q_{sw} typ.	11	nC
$R_{G(int)}$ typ.	2.7	Ω
T_J max	175	°C



G	D	S
Gate	Drain	Source

Description

This Digital Audio MOSFET is specifically designed for Class-D audio amplifier applications. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery and internal Gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD and EMI. Additional features of this MOSFET are 175°C operating junction temperature and repetitive avalanche capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for ClassD audio amplifier applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	150	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	35	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	25	
I_{DM}	Pulsed Drain Current ①	140	
P_D @ $T_C = 25^\circ C$	Power Dissipation ④	144	W
P_D @ $T_C = 100^\circ C$	Power Dissipation ④	72	
	Linear Derating Factor	0.96	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

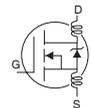
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	1.045	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ④	—	62	

Notes ① through ⑤ are on page 2

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	150	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	32	39	mΩ	V _{GS} = 10V, I _D = 21A ③
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 100μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-13	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 150V, V _{GS} = 0V
		—	—	250		V _{DS} = 150V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	35	—	—	S	V _{DS} = 50V, I _D = 21A
Q _g	Total Gate Charge	—	26	40	nC	V _{DS} = 75V V _{GS} = 10V I _D = 21A See Fig. 6 and 19
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	6.4	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	2.2	—		
Q _{gd}	Gate-to-Drain Charge	—	9.0	—		
Q _{godr}	Gate Charge Overdrive	—	8.9	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	11	—		
R _{G(int)}	Internal Gate Resistance	—	2.7	5.0	Ω	
t _{d(on)}	Turn-On Delay Time	—	8.9	—	ns	V _{DD} = 75V, V _{GS} = 10V ③ I _D = 21A R _G = 2.4Ω
t _r	Rise Time	—	23.1	—		
t _{d(off)}	Turn-Off Delay Time	—	17.2	—		
t _f	Fall Time	—	13.1	—		
C _{iss}	Input Capacitance	—	1750	—	pF	V _{GS} = 0V V _{DS} = 50V f = 1.0MHz, See Fig.5 V _{GS} = 0V, V _{DS} = 0V to 120V
C _{oss}	Output Capacitance	—	155	—		
C _{rss}	Reverse Transfer Capacitance	—	40	—		
C _{oss}	Effective Output Capacitance	—	175	—		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		

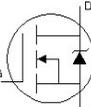


Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	109	mJ
I _{AR}	Avalanche Current ⑤	See Fig. 14, 15, 17a, 17b		A
E _{AR}	Repetitive Avalanche Energy ⑤			mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S @ T _C = 25°C	Continuous Source Current (Body Diode)	—	—	35	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	140		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 21A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	80	120	ns	T _J = 25°C, I _F = 21A, V _R = 120V
Q _{rr}	Reverse Recovery Charge	—	312	468	nC	di/dt = 100A/μs ③



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T_J = 25°C, L = 0.51mH, R_G = 25Ω, I_{AS} = 21A.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R_θ is measured at T_J of approximately 90°C.
- ⑤ Limited by T_{Jmax}. See Figs. 14, 15, 17a, 17b for repetitive avalanche information

Ultrafast recovery diode

Main product characteristics

$I_{F(AV)}$	12 A
V_{RRM}	200 V
$T_j(\text{max})$	175° C
$V_F(\text{typ})$	0.82 V
$t_{rr}(\text{typ})$	18 ns

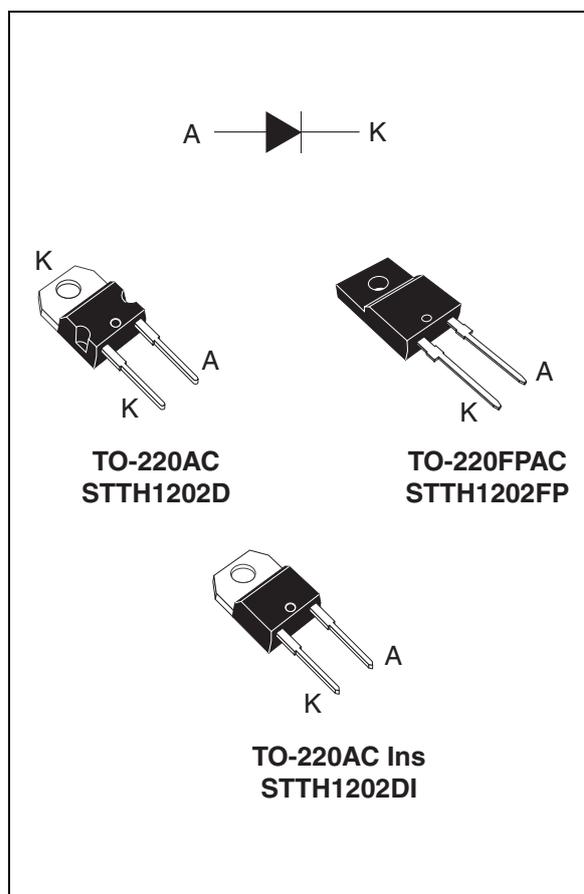
Features and benefits

- Very low conduction losses
- Negligible switching losses
- Low forward and reverse recovery time
- High junction temperature
- Insulated packages
 - TO-220FPAC
Electrical insulation 1500 V_{RMS}
 - TO-220AC Ins
Electrical insulation 2500 V_{RMS}

Description

The STTH1202 uses ST's new 200V planar Pt doping technology, and is specially suited for switching mode base drive and transistor circuits.

Packaged in TO-220AC, TO-220FPAC, and TO-220AC Ins, this device is intended for use in low voltage, high frequency inverters, free wheeling and polarity protection.



Order codes

Part Number	Marking
STTH1202D	STTH1202
STTH1202FP	STTH1202
STTH1202DI	STTH1202DI

1 Characteristics

Table 1. Absolute ratings (limiting values at $T_j = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter		Value	Unit	
V_{RRM}	Repetitive peak reverse voltage		200	V	
V_{RSM}	Non repetitive peak reverse voltage		200		
$I_{F(RMS)}$	RMS forward current		30	A	
$I_{F(AV)}$	Average forward current, $\delta = 0.5$	TO-220AC	$T_c = 140^\circ\text{C}$	12	A
		TO-220AC Ins	$T_c = 130^\circ\text{C}$		
		TO-220FPAC	$T_c = 105^\circ\text{C}$		
I_{FRM}	Repetitive peak forward current	$t_p = 10\ \mu\text{s}$ F = 5 kHz square	130	A	
I_{FSM}	Surge non repetitive forward current	$t_p = 10\ \text{ms}$ Sinusoidal	100	A	
T_{stg}	Storage temperature range		-65 to + 175	$^\circ\text{C}$	
T_j	Maximum operating junction temperature		175	$^\circ\text{C}$	

Table 2. Thermal parameters

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case	TO-220AC	2.5	$^\circ\text{C/W}$
		TO-220AC Ins	3	
		TO-220FPAC	5	

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ	Max.	Unit
$I_R^{(1)}$	Reverse leakage current	$T_j = 25^\circ\text{C}$	$V_R = V_{RRM}$			10	μA
		$T_j = 125^\circ\text{C}$			10	100	
$V_F^{(2)}$	Forward voltage drop	$T_j = 25^\circ\text{C}$	$I_F = 12\ \text{A}$		1.0	1.10	V
		$T_j = 150^\circ\text{C}$			0.82	0.95	
		$T_j = 25^\circ\text{C}$	$I_F = 15\ \text{A}$			1.15	
		$T_j = 125^\circ\text{C}$			0.91	1.05	
		$T_j = 150^\circ\text{C}$			0.87	1.0	

1. Pulse test: $t_p = 5\ \text{ms}$, $\delta < 2\ \%$

2. Pulse test: $t_p = 380\ \mu\text{s}$, $\delta < 2\ \%$

To evaluate the conduction losses use the following equation:

$$P = 0.77 \times I_{F(AV)} + 0.015 \times I_{F(RMS)}^2$$

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Unit
t_{rr}	Reverse recovery time	$I_F = 1\text{ A}$, $di_F/dt = -50\text{ A}/\mu\text{s}$, $V_R = 30\text{ V}$, $T_j = 25^\circ\text{ C}$		28	35	ns
		$I_F = 1\text{ A}$, $di_F/dt = -100\text{ A}/\mu\text{s}$, $V_R = 30\text{ V}$, $T_j = 25^\circ\text{ C}$		18	24	
I_{RM}	Reverse recovery current	$I_F = 12\text{ A}$, $di_F/dt = -200\text{ A}/\mu\text{s}$, $V_R = 160\text{ V}$, $T_j = 125^\circ\text{ C}$		5.8	7.5	A
t_{fr}	Forward recovery time	$I_F = 12\text{ A}$, $di_F/dt = 100\text{ A}/\mu\text{s}$ $V_{FR} = 1.1 \times V_{Fmax}$, $T_j = 25^\circ\text{ C}$		110		ns
V_{FP}	Forward recovery voltage	$I_F = 12\text{ A}$, $di_F/dt = 100\text{ A}/\mu\text{s}$, $T_j = 25^\circ\text{ C}$		2		V

Figure 1. Peak current versus duty cycle

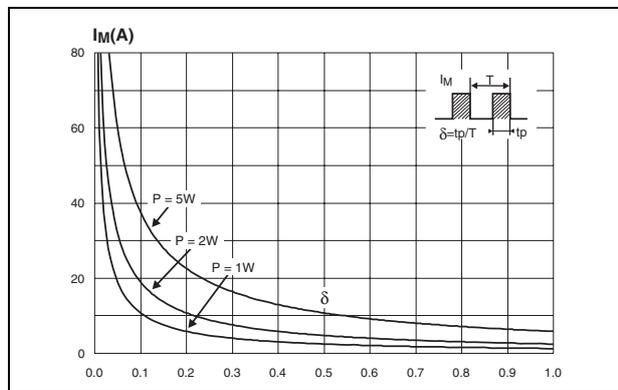


Figure 2. Forward voltage drop versus forward current (typical values)

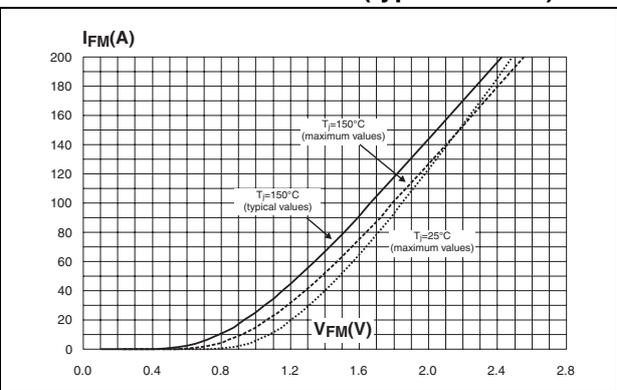


Figure 3. Relative variation of thermal impedance, junction to case, versus pulse duration (TO-220AC, TO-220AC Ins)

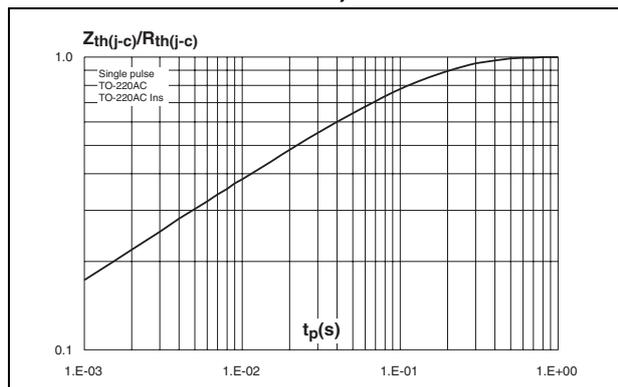
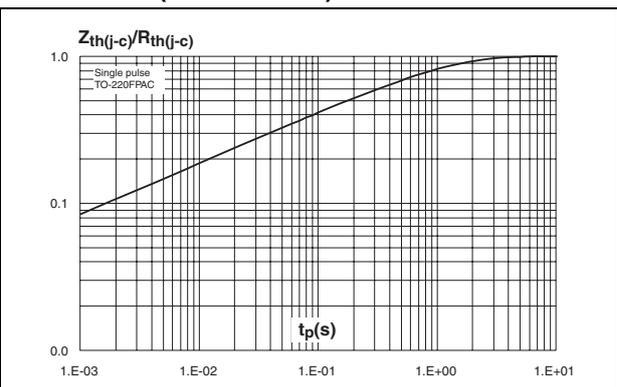


Figure 4. Relative variation of thermal impedance, junction to case, versus pulse duration (TO-220FPAC)



FEATURES

- 4 A peak output current**
- Working voltage**
 - High-side or low-side relative to input: **565 V peak**
 - High-side to low-side differential: **800 V peak**
- High frequency operation: 1 MHz maximum**
- 3.3 V to 5 V CMOS input logic**
- 4.5 V to 18 V output drive**
- UVLO at 2.5 V V_{DD1}**
 - ADuM3223A/ADuM4223A UVLO at 4.1 V V_{DD2}
 - ADuM3223B/ADuM4223B UVLO at 7.0 V V_{DD2}
 - ADuM3223C/ADuM4223C UVLO at 11.0 V V_{DD2}
- Precise timing characteristics**
 - 54 ns maximum isolator and driver propagation delay
 - 5 ns maximum channel-to-channel matching
- CMOS input logic levels**
- High common-mode transient immunity: >25 kV/ μ s**
- Enhanced system-level ESD performance per IEC 61000-4-x**
- High junction temperature operation: 125°C**
- Thermal shutdown protection**
- Default low output**
- Safety and regulatory approvals**
 - ADuM3223 narrow body, 16-lead SOIC
 - UL 1577 3000 V rms input-to-output withstand voltage
 - ADuM4223 wide body, 16-lead SOIC
 - UL 1577 5000 V rms input-to-output withstand voltage
- Qualified for automotive applications**

APPLICATIONS

- Switching power supplies
- Isolated IGBT/MOSFET gate drives
- Industrial inverters

GENERAL DESCRIPTION

The ADuM3223/ADuM4223¹ are 4 A isolated, half-bridge gate drivers that employ the Analog Devices, Inc., *iCoupler*® technology to provide independent and isolated high-side and low-side outputs. The ADuM3223 provides 3000 V rms isolation in the narrow body, 16-lead SOIC package, and the ADuM4223 provides 5000 V rms isolation in the wide body, 16-lead SOIC package. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to the alternatives, such as the combination of pulse transformers and gate drivers.

The ADuM3223/ADuM4223 isolators each provide two independent isolated channels. They operate with an input supply ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM3223/ADuM4223 offer the benefit of true, galvanic isolation between the input and each output. Each output may be continuously operated up to 565 V peak relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high-side and low-side may be as high as 800 V peak.

As a result, the ADuM3223/ADuM4223 provide reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

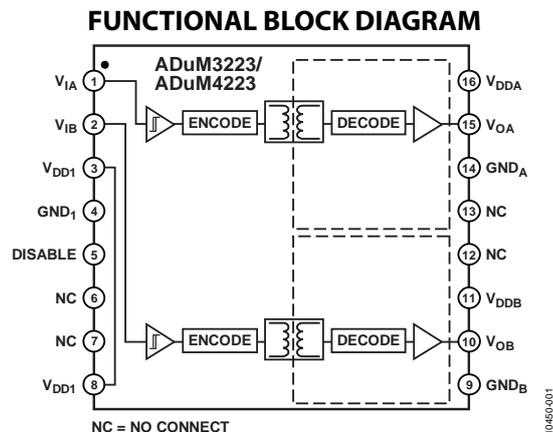


Figure 1.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

Rev. C

Document Feedback

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REVISION HISTORY

12/13—Rev. B to Rev. C

Change to Features Section	1
Changes to Switching Specifications Parameter, Table 1	3
Added Thermal Shutdown Temperatures Parameter, Table 1....	3
Changes to Switching Specifications Parameter, Table 2	4
Added Thermal Shutdown Temperatures Parameter, Table 2....	4
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Change to Boot-Strapped Half-Bridge Operation Section	16

5/13—Rev. A to Rev. B

Added V_{DDA} , V_{DDB} Rise Time of 0.5 V/ μ s; Table 10.....	8
Changes to Figure 22.....	16

1/13—Rev. 0 to Rev. A

Added Automotive Information (Throughout)	1
Updated Safety and Regulatory Approvals (Throughout)	1
Changed High-Side to Low-Side Differential from 700 $V_{DC\ PEAK}$	
to 800 V peak.....	1
Added R_{OA} , R_{OB} Minimum and Maximum Values, Table 1.....	3
Added R_{OA} , R_{OB} Minimum and Maximum Values, Table 2.....	4
Changes to Table 13.....	10
Changes to Figure 19.....	15
Added Boot-Strapped Half Bridge Operation Section and	
Figure 22; Renumbered Sequentially	16
Changes to Ordering Guide	20

5/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 18\text{ V}$, unless stated otherwise. All minimum/maximum specifications apply over $T_J = -40^\circ\text{C}$ to 125°C . All typical specifications are at $T_J = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 12\text{ V}$. Switching specifications are tested with CMOS signal levels.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DD1(Q)}$		1.4	2.4	mA	
Output Supply Current, Per Channel, Quiescent	$I_{DDO(Q)}$		2.3	3.2	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.6	2.5	mA	Up to 1 MHz, no load
V_{DDA}/V_{ddb} Supply Current	$I_{DDA}/I_{ddb(Q)}$		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_{IA}, I_{IB}	-1	+0.01	+1	μA	$0 \leq V_{IA}, V_{IB} \leq V_{DD1}$
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DD1}$	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	$V_{DD2} - 0.1$	V_{DD2}		V	$I_{OX} = -20\text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	$I_{OX} = +20\text{ mA}, V_{IX} = V_{IXL}$
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		4.1	4.4	V	A-grade
Negative Going Threshold	V_{DD2UV-}	3.2	3.6		V	A-grade
Hysteresis	V_{DD2UVH}		0.5		V	A-grade
Positive Going Threshold	V_{DD2UV+}		6.9	7.4	V	B-grade
Negative Going Threshold	V_{DD2UV-}	5.7	6.2		V	B-grade
Hysteresis	V_{DD2UVH}		0.7		V	B-grade
Positive Going Threshold	V_{DD2UV+}		10.5	11.1	V	C-grade
Negative Going Threshold	V_{DD2UV-}	8.9	9.6		V	C-grade
Hysteresis	V_{DD2UVH}		0.9		V	C-grade
Output Short-Circuit Pulsed Current ¹	$I_{OA(SC)}, I_{OB(SC)}$	2.0	4.0		A	$V_{DD2} = 12\text{ V}$
Output Pulsed Source Resistance	R_{OA}, R_{OB}	0.3	1.1	3.0	Ω	$V_{DD2} = 12\text{ V}$
Output Pulsed Sink Resistance	R_{OA}, R_{OB}	0.3	0.6	3.0	Ω	$V_{DD2} = 12\text{ V}$
THERMAL SHUTDOWN TEMPERATURES						
Junction Temperature Shutdown, Rising Edge	T_{JR}		150		$^\circ\text{C}$	
Junction Temperature Shutdown, Falling Edge	T_{JF}		140		$^\circ\text{C}$	
SWITCHING SPECIFICATIONS						
Pulse Width ²	PW	50			ns	$C_L = 2\text{ nF}, V_{DD2} = 12\text{ V}$
Maximum Data Rate ³		1			MHz	$C_L = 2\text{ nF}, V_{DD2} = 12\text{ V}$
Propagation Delay ⁴	t_{DHL}, t_{DLH}	31	43	54	ns	$C_L = 2\text{ nF}, V_{DD2} = 12\text{ V}$; see Figure 20
ADuM3223A/ADuM4223A	t_{DHL}, t_{DLH}	35	47	59	ns	$C_L = 2\text{ nF}, V_{DD2} = 4.5\text{ V}$; see Figure 20
Propagation Delay Skew ⁵	t_{PSK}			12	ns	$C_L = 2\text{ nF}, V_{DD2} = 12\text{ V}$; see Figure 20
Channel-to-Channel Matching ⁶	t_{PSKCD}		1	5	ns	$C_L = 2\text{ nF}, V_{DD2} = 12\text{ V}$; see Figure 20
	t_{PSKCD}		1	7	ns	$C_L = 2\text{ nF}, V_{DD2} = 4.5\text{ V}$; see Figure 20
Output Rise/Fall Time (10% to 90%)	t_R/t_F	6	12	18	ns	$C_L = 2\text{ nF}, V_{DD2} = 12\text{ V}$; see Figure 20
Dynamic Input Supply Current Per Channel	$I_{DDI(D)}$		0.05		mA/Mbps	$V_{DD2} = 12\text{ V}$
Dynamic Output Supply Current Per Channel	$I_{DDO(D)}$		1.65		mA/Mbps	$V_{DD2} = 12\text{ V}$
Refresh Rate	f_r		1.2		Mbps	

¹ Short-circuit duration less than 1 μs . Average power must conform to the limit shown under the Absolute Maximum Ratings.

² The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.

⁴ t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH} , to the output rising 10% level of the V_{OX} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL} , to the output falling 90% threshold of the V_{OX} signal. See Figure 20 for waveforms of propagation delay parameters.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.

⁶ Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 18\text{ V}$, unless stated otherwise. All minimum/maximum specifications apply over $T_J = -40^\circ\text{C}$ to 125°C . All typical specifications are at $T_J = 25^\circ\text{C}$, $V_{DD1} = 3.3\text{ V}$, $V_{DD2} = 12\text{ V}$. Switching specifications are tested with CMOS signal levels.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DD1(Q)}$		0.87	1.4	mA	
Output Supply Current, Per Channel, Quiescent	$I_{DDO(Q)}$		2.3	3.2	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.1	1.5	mA	Up to 1 MHz, no load
V_{DDA}/V_{DDB} Supply Current	$I_{DDA}/I_{DDB(Q)}$		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0 \leq V_{IA}, V_{IB} \leq V_{DD1}$
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DD1}$	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	$V_{DD2} - 0.1$	V_{DD2}		V	$I_{Ox} = -20\text{ mA}$, $V_{Ix} = V_{IH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	$I_{Ox} = +20\text{ mA}$, $V_{Ix} = V_{IL}$
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		4.1	4.4	V	A-grade
Negative Going Threshold	V_{DD2UV-}	3.2	3.6		V	A-grade
Hysteresis	V_{DD2UVH}		0.5		V	A-grade
Positive Going Threshold	V_{DD2UV+}		6.9	7.4	V	B-grade
Negative Going Threshold	V_{DD2UV-}	5.7	6.2		V	B-grade
Hysteresis	V_{DD2UVH}		0.7		V	B-grade
Positive Going Threshold	V_{DD2UV+}		10.5	11.1	V	C-grade
Negative Going Threshold	V_{DD2UV-}	8.9	9.6		V	C-grade
Hysteresis	V_{DD2UVH}		0.9		V	C-grade
Output Short-Circuit Pulsed Current ¹	$I_{OA(SC)}, I_{OB(SC)}$	2.0	4.0		A	$V_{DD2} = 12\text{ V}$
Output Pulsed Source Resistance	R_{OA}, R_{OB}	0.3	1.1	3.0	Ω	$V_{DD2} = 12\text{ V}$
Output Pulsed Sink Resistance	R_{OA}, R_{OB}	0.3	0.6	3.0	Ω	$V_{DD2} = 12\text{ V}$
THERMAL SHUTDOWN TEMPERATURE						
Junction Temperature Shutdown, Rising Edge	T_{JR}		150		$^\circ\text{C}$	
Junction Temperature Shutdown, Falling Edge	T_{JF}		140		$^\circ\text{C}$	
SWITCHING SPECIFICATIONS						
Pulse Width ²	PW	50			ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$
Maximum Data Rate ³		1			MHz	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$
Propagation Delay ⁴	t_{DHL}, t_{DLH}	35	47	59	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$, see Figure 20
ADuM3223A/ADuM4223A	t_{DHL}, t_{DLH}	37	51	65	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 4.5\text{ V}$, see Figure 20
Propagation Delay Skew ⁵	t_{PSK}			12	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$, see Figure 20
Channel-to-Channel Matching ⁶	t_{PSKCD}		1	5	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$, see Figure 20
	t_{PSKCD}		1	7	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 4.5\text{ V}$, see Figure 20
Output Rise/Fall Time (10% to 90%)	t_R/t_F	6	12	22	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$, see Figure 20
Dynamic Input Supply Current Per Channel	$I_{DDI(D)}$		0.05		mA/Mbps	$V_{DD2} = 12\text{ V}$
Dynamic Output Supply Current Per Channel	$I_{DDO(D)}$		1.65		mA/Mbps	$V_{DD2} = 12\text{ V}$
Refresh Rate	f_r		1.1		Mbps	

¹ Short-circuit duration less than 1 μs . Average power must conform to the limit shown under the Absolute Maximum Ratings.

² The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.

⁴ t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH} , to the output rising 10% level of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL} , to the output falling 90% threshold of the V_{Ox} signal. See Figure 20 for waveforms of propagation delay parameters.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.

⁶ Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)	R _{I-O}		10 ¹²		Ω	f = 1 MHz
Capacitance (Input-to-Output)	C _{I-O}		2.0		pF	
Input Capacitance	C _I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance						
ADuM3223	θ _{JA}		76		°C/W	
ADuM4223	θ _{JA}		45		°C/W	
IC Junction-to-Case Thermal Resistance						
ADuM3223	θ _{JC}		42		°C/W	
ADuM4223	θ _{JC}		29		°C/W	

INSULATION AND SAFETY-RELATED SPECIFICATIONS**ADuM3223**

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		3000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.0 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

ADuM4223

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

REGULATORY INFORMATION

The [ADuM3223](#) is approved by the organizations listed in Table 6.

Table 6.

UL	CSA	VDE
Recognized under UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ²
Single/Protection 3000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

¹ In accordance with UL 1577, each [ADuM3223](#) is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 second (current leakage detection limit = 6 μ A).

² In accordance with DIN V VDE V 0884-10, each [ADuM3223](#) is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

The [ADuM4223](#) is approved by the organizations listed in Table 7.

Table 7.

UL	CSA	VDE
Recognized under UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ²
Single/Protection 5000 V rms Isolation Voltage	Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Basic insulation per CSA 60950-1-07 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

¹ In accordance with UL 1577, each [ADuM4223](#) is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 μ A).

² In accordance with DIN V VDE V 0884-10, each [ADuM4223](#) is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

LM337L 3-Terminal Adjustable Regulator

General Description

The LM337L is an adjustable 3-terminal negative voltage regulator capable of supplying 100mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Furthermore, both line and load regulation are better than standard fixed regulators. Also, the LM337L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM337L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, only a single 1 μ F solid tantalum output capacitor is needed unless the device is situated more than 6 inches from the input filter capacitors, in which case an input bypass is needed. A larger output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM337L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting

a fixed resistor between the adjustment and output, the LM337L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

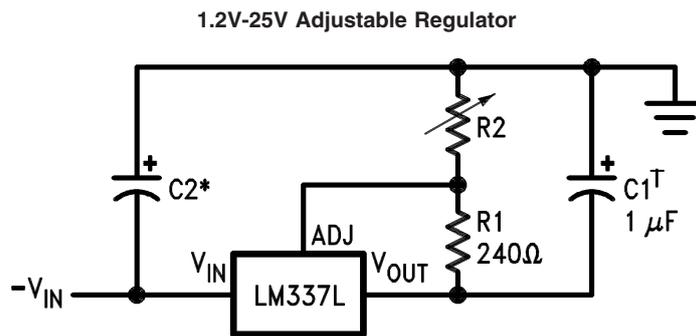
The LM337L is available in a standard TO-92 transistor package, SO-8 surface mount package, and in our new 12 mil diameter bump micro SMD package. The LM337L is rated for operation over a -25°C to +125°C range.

For applications requiring greater output current in excess of 0.5A and 1.5A, see LM137 series data sheets. For the positive complement, see series LM117 and LM317L data sheets.

Features

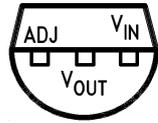
- Adjustable output down to 1.2V
- Guaranteed 100mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short circuit protected
- Available in the 6-Bump micro SMD package
- See AN-1112 for micro SMD considerations

Typical Application



Connection Diagrams

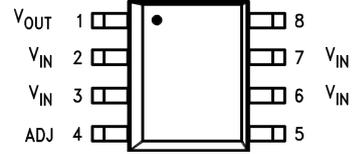
3-Pin TO92



00913401

Bottom View

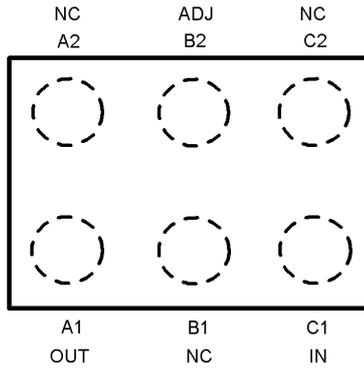
8-Pin SOIC



00913402

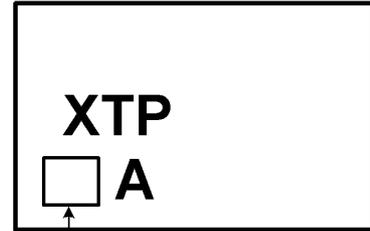
Top View

6-Bump micro SMD



00913408

micro SMD Laser mark



Pin A1 Identifier

00913407

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
3-Pin TO92	LM337LZ	LM337LZ	1800 per Bag	Z03A
8-Pin SOIC	LM337LM	LM337LM	Rails	M08A
	LM337LMX		2.5k Units Tape and Reel	
6-Bump micro SMD	LM337LBL	PA	250 Units Tape and Reel	BLA06FNB
	LM337LBLX		3k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input–Output Voltage Differential	40V
Operating Junction Temperature Range	–25°C to +125°C

Storage Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Plastic Package (Soldering 4 sec.)	260°C
ESD Rating	1.5kV (Note 5)

Electrical Characteristics (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
Line Regulation	$T_A = 25^\circ\text{C}$, $3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$, (Note 3)		0.01	0.04	%/V
Load Regulation	$T_A = 25^\circ\text{C}$, $5\text{mA} \leq I_{\text{OUT}} \leq I_{\text{MAX}}$, (Note 3)		0.1	0.5	%
Thermal Regulation	$T_A = 25^\circ\text{C}$, 10ms Pulse		0.04	0.2	%/W
Adjustment Pin Current			50	100	μA
Adjustment Pin Current Change	$5\text{mA} \leq I_L \leq 100\text{mA}$ $3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$		0.2	5	μA
Reference Voltage	$3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$, (Note 4) $10\text{mA} \leq I_{\text{OUT}} \leq 100\text{mA}$, $P \leq 625\text{mW}$	1.20	1.25	1.30	V
Line Regulation	$3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$, (Note 3)		0.02	0.07	%/V
Load Regulation	$5\text{mA} \leq I_{\text{OUT}} \leq 100\text{mA}$, (Note 3)		0.3	1.5	%
Temperature Stability	$T_{\text{MIN}} \leq T_j \leq T_{\text{MAX}}$		0.65		%
Minimum Load Current	$ V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$ $3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 15\text{V}$		3.5 2.2	5 3.5	mA mA
Current Limit	$3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 13\text{V}$ $ V_{\text{IN}} - V_{\text{OUT}} = 40\text{V}$	100 25	200 50	320 120	mA mA
Rms Output Noise, % of V_{OUT}	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{kHz}$		0.003		%
Ripple Rejection Ratio	$V_{\text{OUT}} = -10\text{V}$, $F = 120\text{Hz}$, $C_{\text{ADJ}} = 0$ $C_{\text{ADJ}} = 10\mu\text{F}$	66	65 80		dB dB
Long-Term Stability	$T_A = 125^\circ\text{C}$		0.3	1	%

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: Unless otherwise specified, these specifications apply $-25^\circ\text{C} \leq T_j \leq +125^\circ\text{C}$ for the LM337L; $|V_{\text{IN}} - V_{\text{OUT}}| = 5\text{V}$ and $I_{\text{OUT}} = 40\text{mA}$. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. I_{MAX} is 100mA.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

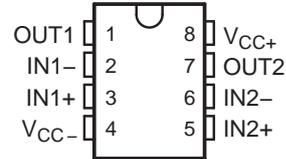
Note 4: Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to PC board. The M package θ_{JA} is 180°C/W in still air. The 6-Bump micro SMD package θ_{JA} is 290°C/W in still air.

Note 5: Human body model, 1.5k Ω in series with 100pF.

FEATURES

- Dual-Supply Operation . . . $\pm 5\text{ V}$ to $\pm 18\text{ V}$
- Low Noise Voltage . . . $4.5\text{ nV}/\sqrt{\text{Hz}}$
- Low Input Offset Voltage . . . 0.15 mV
- Low Total Harmonic Distortion . . . 0.002%
- High Slew Rate . . . $7\text{ V}/\mu\text{s}$
- High-Gain Bandwidth Product . . . 16 MHz
- High Open-Loop AC Gain . . . 800 at 20 kHz
- Large Output-Voltage Swing . . . 14.1 V to -14.6 V
- Excellent Gain and Phase Margins

D (SOIC), DGK (MSOP), OR P (PDIP) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

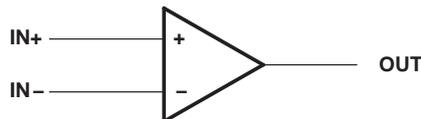
The MC33078 is a bipolar dual operational amplifier with high-performance specifications for use in quality audio and data-signal applications. This device operates over a wide range of single- and dual-supply voltages and offers low noise, high-gain bandwidth, and high slew rate. Additional features include low total harmonic distortion, excellent phase and gain margins, large output voltage swing with no deadband crossover distortion, and symmetrical sink/source performance.

ORDERING INFORMATION

T _A	PACKAGE (1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING (2)
-40°C to 85°C	PDIP – P	Tube of 50	MC33078P	MC33078P
	SOIC – D	Tube of 75	MC33078D	M33078
		Reel of 2500	MC33078DR	
	VSSOP/MSOP – DGK	Reel of 2500	MC33078DGKR	MY_
		Reel of 250	MC33078DGKT	

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
 (2) DGK: The actual top-side marking has one additional character that designates the assembly/test site.

SYMBOL (EACH AMPLIFIER)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MC33078
DUAL HIGH-SPEED LOW-NOISE OPERATIONAL AMPLIFIER

SLLS633C – OCTOBER 2004 – REVISED NOVEMBER 2006

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC+}	Supply voltage ⁽²⁾		18	V
V _{CC-}	Supply voltage ⁽²⁾		-18	V
V _{CC+} - V _{CC-}	Supply voltage		36	V
	Input voltage, either input ⁽²⁾⁽³⁾		V _{CC+} or V _{CC-}	V
	Input current ⁽⁴⁾		±10	mA
	Duration of output short circuit ⁽⁵⁾		Unlimited	
θ _{JA}	Package thermal impedance, junction to free air ⁽⁶⁾⁽⁷⁾	D package	97	°C/W
		DGK package	172	
		P package	85	
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
- (3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
- (4) Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
- (5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
- (6) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC-}	Supply voltage	-5	-18	V
V _{CC+}		5	18	
T _A	Operating free-air temperature range	-40	85	°C

Electrical Characteristics

$V_{CC-} = -15\text{ V}$, $V_{CC+} = 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 10\ \Omega$, $V_{CM} = 0$	$T_A = 25^\circ\text{C}$	0.15	2		mV
			$T_A = -40^\circ\text{C}$ to 85°C			3	
αV_{IO}	Input offset voltage temperature coefficient	$V_O = 0$, $R_S = 10\ \Omega$, $V_{CM} = 0$	$T_A = -40^\circ\text{C}$ to 85°C		2		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input bias current	$V_O = 0$, $V_{CM} = 0$	$T_A = 25^\circ\text{C}$	300	750		nA
			$T_A = -40^\circ\text{C}$ to 85°C			800	
I_{IO}	Input offset current	$V_O = 0$, $V_{CM} = 0$	$T_A = 25^\circ\text{C}$	25	150		nA
			$T_A = -40^\circ\text{C}$ to 85°C			175	
V_{ICR}	Common-mode input voltage range	$\Delta V_{IO} = 5\text{ mV}$, $V_O = 0$		± 13	± 14		V
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	$T_A = 25^\circ\text{C}$	90	110		dB
			$T_A = -40^\circ\text{C}$ to 85°C	85			
V_{OM}	Maximum output voltage swing	$V_{ID} = \pm 1\text{ V}$	$R_L = 600\ \Omega$	V_{OM+}	10.7		V
				V_{OM-}	-11.9		
			$R_L = 2\text{ k}\Omega$	V_{OM+}	13.2	13.8	
				V_{OM-}	-13.2	-13.7	
			$R_L = 10\text{ k}\Omega$	V_{OM+}	13.5	14.1	
				V_{OM-}	-14	-14.6	
CMMR	Common-mode rejection ratio	$V_{IN} = \pm 13\text{ V}$		80	100		dB
$k_{SVR}^{(1)}$	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to 15 V , $V_{CC-} = -5\text{ V}$ to -15 V		80	105		dB
I_{OS}	Output short-circuit current	$ V_{ID} = 1\text{ V}$, Output to GND	Source current	15	29		mA
			Sink current	-20	-37		
I_{CC}	Supply current (per channel)	$V_O = 0$	$T_A = 25^\circ\text{C}$	2.05	2.5		mA
			$T_A = -40^\circ\text{C}$ to 85°C			2.75	

(1) Measured with $V_{CC\pm}$ differentially varied at the same time

Operating Characteristics

$V_{CC-} = -15\text{ V}$, $V_{CC+} = 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$A_{VD} = 1$, $V_{IN} = -10\text{ V}$ to 10 V , $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		5	7		$\text{V}/\mu\text{s}$
GBW	Gain bandwidth product	$f = 100\text{ kHz}$		10	16		MHz
B_1	Unity gain frequency	Open loop			9		MHz
G_m	Gain margin	$R_L = 2\text{ k}\Omega$	$C_L = 0\text{ pF}$		-11		dB
			$C_L = 100\text{ pF}$		-6		
Φ_m	Phase margin	$R_L = 2\text{ k}\Omega$	$C_L = 0\text{ pF}$		55		deg
			$C_L = 100\text{ pF}$		40		
	Amp-to-amp isolation	$f = 20\text{ Hz}$ to 20 kHz			-120		dB
	Power bandwidth	$V_O = 27\text{ V}_{(PP)}$, $R_L = 2\text{ k}\Omega$, $\text{THD} \leq 1\%$			120		kHz
THD	Total harmonic distortion	$V_O = 3\text{ V}_{\text{rms}}$, $A_{VD} = 1$, $R_L = 2\text{ k}\Omega$, $f = 20\text{ Hz}$ to 20 kHz			0.002		%
z_o	Open-loop output impedance	$V_O = 0$, $f = 9\text{ MHz}$			37		Ω
r_{id}	Differential input resistance	$V_{CM} = 0$			175		$\text{k}\Omega$
C_{id}	Differential input capacitance	$V_{CM} = 0$			12		pF
V_n	Equivalent input noise voltage	$f = 1\text{ kHz}$, $R_S = 100\ \Omega$			4.5		$\text{nV}/\sqrt{\text{Hz}}$
I_n	Equivalent input noise current	$f = 1\text{ kHz}$			0.5		$\text{pA}/\sqrt{\text{Hz}}$



50MHz, Low-Distortion, High CMRR, RRI/O, Single-Supply OPERATIONAL AMPLIFIER

FEATURES

- **GAIN BANDWIDTH: 50MHz**
- **ZERO-CROSSOVER DISTORTION TOPOLOGY:**
 - Excellent THD+N: 0.0004%
 - CMRR: 100dB (min)
 - Rail-to-Rail Input and Output
 - Input 100mV Beyond Supply Rail
- **LOW NOISE: 4.5nV/√Hz at 100kHz**
- **SLEW RATE: 25V/μs**
- **FAST SETTLING: 0.3μs to 0.01%**
- **PRECISION:**
 - Low Offset: 100μV
 - Low Input Bias Current: 0.2pA
- **2.2V TO 5.5V OPERATION**

APPLICATIONS

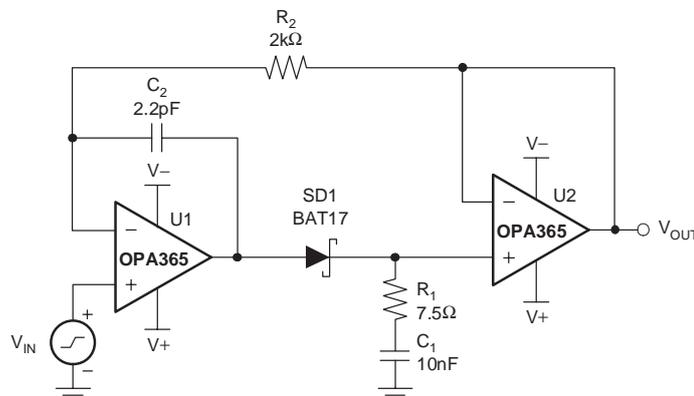
- SIGNAL CONDITIONING
- DATA ACQUISITION
- PROCESS CONTROL
- ACTIVE FILTERS
- TEST EQUIPMENT
- AUDIO
- WIDEBAND AMPLIFIERS

DESCRIPTION

The OPAx365 zero-crossover series, rail-to-rail, high-performance, CMOS operational amplifiers are optimized for very low voltage, single-supply applications. Rail-to-rail input/output, low-noise (4.5nV/√Hz) and high-speed operation (50MHz Gain Bandwidth) make these devices ideal for driving sampling analog-to-digital converters (ADCs). Applications include audio, signal conditioning, and sensor amplification. The OPA365 family of op amps are also well-suited for cell phone power amplifier control loops.

Special features include an excellent common-mode rejection ratio (CMRR), no input stage crossover distortion, high input impedance, and rail-to-rail input and output swing. The input common-mode range includes both the negative and positive supplies. The output voltage swing is within 10mV of the rails.

The OPA365 (single version) is available in the *micro-SIZE* SOT23-5 and SO-8 packages. The OPA2365 (dual version) is offered in the SO-8 package. All versions are specified for operation from –40°C to +125°C. Single and dual versions have identical specifications for maximum design flexibility.



Fast Settling Peak Detector



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+5.5V
Signal Input Terminals, Voltage(2)	(V-) -0.5V to (V+) + 0.5V
Signal Input Terminals, Current(2)	±10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	-40°C to +150°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
ESD Rating	
Human Body Model	4000V
Charged Device Model	1000V
Machine Model	400V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

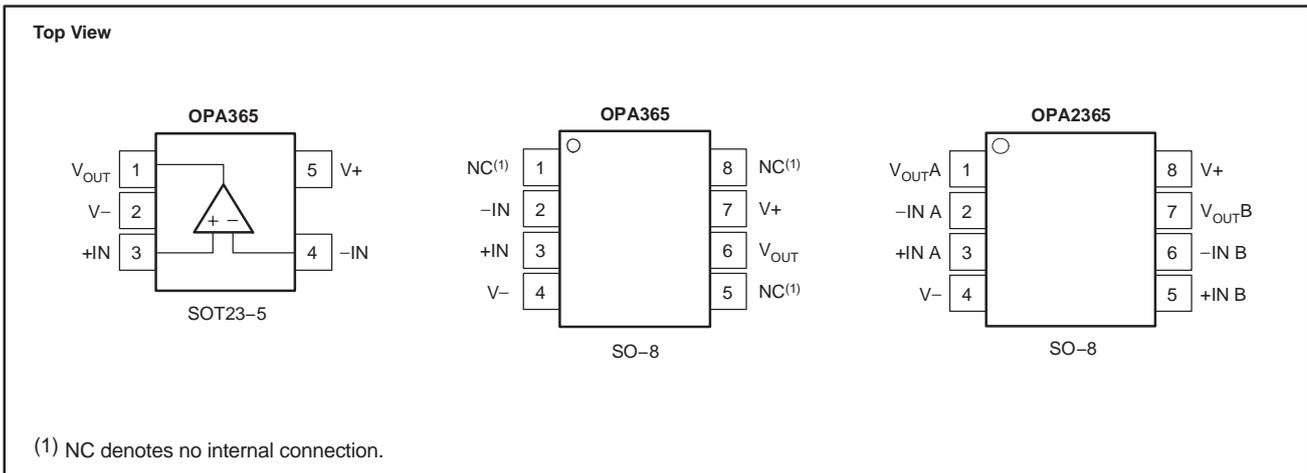
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA365	SOT23-5	DBV	OAVQ
	SO-8	D	O365A
OPA2365	SO-8	D	O2365A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS: $V_S = +2.2V$ to $+5.5V$
Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPAx365			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage	V_{OS}		100	200	μV
Drift vs Power Supply	dV_{OS}/dT		1		$\mu\text{V}/^\circ\text{C}$
Channel Separation, dc	PSRR		10	100	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT					
Input Bias Current	I_B		± 0.2	± 10	pA
over Temperature			See Typical Characteristics		
Input Offset Current	I_{OS}		± 0.2	± 10	pA
NOISE					
Input Voltage Noise, $f = 0.1\text{Hz}$ to 10Hz	e_n		5		μV_{PP}
Input Voltage Noise Density, $f = 100\text{kHz}$	e_n		4.5		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise Density, $f = 10\text{kHz}$	i_n		4		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range	V_{CM}	$(V-) - 0.1$		$(V+) + 0.1$	V
Common-Mode Rejection Ratio	CMRR	$(V-) - 0.1\text{V} \leq V_{CM} \leq (V+) + 0.1\text{V}$	100	120	dB
INPUT CAPACITANCE					
Differential			6		pF
Common-Mode			2		pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	A_{OL}	$R_L = 10\text{k}\Omega, 100\text{mV} < V_O < (V+) - 100\text{mV}$	100	120	dB
		$R_L = 600\Omega, 200\text{mV} < V_O < (V+) - 200\text{mV}$	100	120	dB
		$R_L = 600\Omega, 200\text{mV} < V_O < (V+) - 200\text{mV}$	94		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product	GBW	$V_S = 5V$		50	MHz
Slew Rate	SR	$G = +1$		25	$\text{V}/\mu\text{s}$
Settling Time, 0.1%	t_S	4V Step, $G = +1$		200	ns
0.01%		4V Step, $G = +1$		300	ns
Overload Recovery Time		$V_{IN} \times \text{Gain} > V_S$		< 0.1	μs
Total Harmonic Distortion + Noise ⁽¹⁾	THD+N	$R_L = 600\Omega, V_O = 4V_{PP}, G = +1, f = 1\text{kHz}$		0.0004	%
OUTPUT					
Voltage Output Swing from Rail		$R_L = 10\text{k}\Omega, V_S = 5.5V$		10	mV
over Temperature				20	mV
Short-Circuit Current	I_{SC}			± 65	mA
Capacitive Load Drive	C_L			See Typical Characteristics	
Open-Loop Output Impedance		$f = 1\text{MHz}, I_O = 0$		30	Ω
POWER SUPPLY					
Specified Voltage Range	V_S		2.2	5.5	V
Quiescent Current Per Amplifier	I_Q	$I_O = 0$		4.6	mA
over Temperature				5	mA
TEMPERATURE RANGE					
Specified Range			-40	+125	$^\circ\text{C}$
Thermal Resistance	θ_{JA}				$^\circ\text{C}/\text{W}$
SOT23-5				200	$^\circ\text{C}/\text{W}$
SO-8				150	$^\circ\text{C}/\text{W}$

(1) 3rd-order filter; bandwidth 80kHz at -3dB.



40-ns, microPOWER, Push-Pull Output Comparators

Check for Samples: [TLV3201](#), [TLV3202](#)

FEATURES

- Low Propagation Delay: 40 ns
- Low Quiescent Current:
40 μ A per Channel
- Input Common-Mode Range Extends 200 mV Beyond Either Rail
- Low Input Offset Voltage: 1 mV
- Push-Pull Outputs
- Supply Range: +2.7 V to +5.5 V
- Industrial Temperature Range:
–40°C to +125°C
- Small Packages:
SC70-5, SOT23-5, SOIC-8, MSOP-8

APPLICATIONS

- Inspection Equipment
- Test and Measurement
- High-Speed Sampling Systems
- Telecom
- Portable Communications

DESCRIPTION

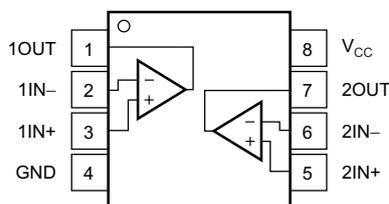
The TLV3201 and TLV3202 are single- and dual-channel comparators that offer the ultimate combination of high-speed (40 ns) and low-power consumption (40 μ A), all in extremely small packages with features such as rail-to-rail inputs, low offset voltage (1 mV), and large output drive current. The devices are also very easy to implement in a wide variety of applications where response time is critical.

The TLV320x family is available in single (TLV3201) and dual (TLV3202) channel versions, both with push-pull outputs. The TLV3201 is available in SOT23-5 and SC70-5 packages. The TLV3202 is available in SOIC-8 and MSOP-8 packages. All devices are specified for operation across the expanded industrial temperature range of –40°C to +125°C.

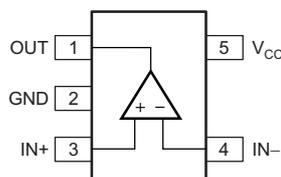
RELATED PRODUCTS

DEVICE	DESCRIPTION
TLV3011	5- μ A (max) open-drain, 1.8-V to 5.5-V with integrated voltage reference in 1.5-mm x 1.5-mm micro-sized packages
TLV3012	5- μ A (max) push-pull, 1.8-V to 5.5-V with integrated voltage reference in micro-sized packages
TLV3501	4.5-ns, rail-to-rail, push-pull comparator in micro-sized packages
LMV7235	75-ns, 65- μ A, 2.7-V to 5.5-V, rail-to-rail input comparator with open-drain output
REF3333	30-ppm/°C drift, 3.9- μ A, SOT23-3, SC70-3 voltage reference

**D AND DGK PACKAGES
SOIC-8 AND MSOP-8
(TOP VIEW)**



**DCK AND DBV PACKAGES
SC70-5 AND SOT23-5
(TOP VIEW)**



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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD ⁽²⁾	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER
TLV3201	SOT23-5	DBV	RAI	TLV3201AIDBV
	SC70-5	DCK	SDP	TLV3201AIDCK
TLV3202	SOIC-8	D	TL3202	TLV3202AID
	MSOP-8	DGK	VUDC	TLV3202AIDGK

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage		7	V
Signal input terminals	Voltage ⁽²⁾	-0.5 to (V _{CC}) + 0.5	V
	Current ⁽²⁾	±10	mA
Output short circuit ⁽³⁾		100	mA
Operating temperature range		-55 to +125	°C
Storage temperature range, T _{stg}		-65 to +150	°C
Junction temperature, T _J		+150	°C
Electrostatic discharge (ESD) ratings TLV3201	Human body model (HBM)	2000	V
Electrostatic discharge (ESD) ratings TLV3202	Human body model (HBM)	1000	V

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.
- (3) Short-circuit to ground.

ELECTRICAL CHARACTERISTICS: $V_{CC} = 5.0\text{ V}$

At $T_A = +25^\circ\text{C}$ and $V_{CC} = 5.0\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			6	mV
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1	10	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$, $V_{CC} = 2.5\text{ V}$ to 5.5 V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	μA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			5	nA
I_{IO}	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	μA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$(V_{EE}) - 0.2$		$(V_{CC}) + 0.2$	V
CMRR	Common-mode rejection ratio	$-0.2\text{ V} < V_{CM} < 5.2\text{ V}$	60	70		dB
INPUT IMPEDANCE						
	Common-mode			$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$
	Differential			$10^{13} \parallel 4$		$\Omega \parallel \text{pF}$
SWITCHING CHARACTERISTICS						
t_{pd}	Propagation delay time	Low to high	Input overdrive = 20 mV, $C_L = 15\text{ pF}$	47	50	ns
			Input overdrive = 100 mV, $C_L = 15\text{ pF}$	43	50	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		55	ns
		High to low	Input overdrive = 20 mV, $C_L = 15\text{ pF}$	45	50	ns
			Input overdrive = 100 mV, $C_L = 15\text{ pF}$	42	50	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		55	ns
Propagation delay skew		Input overdrive = 20mV, $C_L = 15\text{ pF}$		2		ns
Propagation delay matching (TLV3202)		High to low, Low to High	Input overdrive = 20 mV, $C_L = 15\text{ pF}$		5	ns
t_r	Rise time	10% to 90%		2.9		ns
t_f	Fall time	10% to 90%		3.7		ns
OUTPUT						
V_{OL}	Voltage output swing	From lower rail	$I_{SINK} = 4\text{ mA}$	175	190	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		225	mV
From upper rail		$I_{SOURCE} = 4\text{ mA}$	120	140	mV	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		170	mV	
I_{SC}	Short-circuit current (per comparator)	Sinking		40	48	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See Typical Curve	mA
		Sourcing		52	60	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See Typical Curve	mA
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current			40	50	μA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			65	μA
TEMPERATURE						
	Specified range		-40		+125	$^\circ\text{C}$
	Storage range		-65		+150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: $V_{CC} = 2.7\text{ V}$

At $T_A = +25^\circ\text{C}$ and $V_{CC} = 2.7\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			6	mV
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1	10	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$, $V_{CC} = 2.5\text{ V}$ to 5.5 V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	μA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			5	nA
I_{IO}	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	μA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$(V_{EE}) - 0.2$		$(V_{CC}) + 0.2$	V
CMRR	Common-mode rejection ratio	$-0.2\text{ V} < V_{CM} < 2.9\text{ V}$	56	68		dB
INPUT IMPEDANCE						
	Common-mode			$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$
	Differential			$10^{13} \parallel 4$		$\Omega \parallel \text{pF}$
SWITCHING CHARACTERISTICS						
t_{pd}	Propagation delay time	Low to high	Input overdrive = 20 mV, $C_L = 15\text{ pF}$	47	50	ns
			Input overdrive = 100 mV, $C_L = 15\text{ pF}$	42	50	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		55	ns
		High to low	Input overdrive = 20 mV, $C_L = 15\text{ pF}$	40	50	ns
			Input overdrive = 100 mV, $C_L = 15\text{ pF}$	38	50	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		55	ns
Propagation delay skew		Input overdrive = 20mV, $C_L = 15\text{ pF}$		2		ns
Propagation delay matching (TLV3202)		High to low, Low to High	Input overdrive = 20 mV, $C_L = 15\text{ pF}$		5	ns
t_r	Rise time	10% to 90%		4.8		ns
t_f	Fall time	10% to 90%		5.2		ns
OUTPUT						
V_{OL}	Voltage output swing	From lower rail	$I_{SINK} = 4\text{ mA}$	230	260	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		325	mV
From upper rail		$I_{SOURCE} = 4\text{ mA}$	210	250	mV	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		350	mV	
I_{SC}	Short-circuit current (per comparator)	Sinking		13		mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See Typical Curve	mA
		Sourcing		15	21	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See Typical Curve	mA
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current			36	46	μA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			60	μA
TEMPERATURE						
	Specified range		-40		+125	$^\circ\text{C}$
	Storage range		-65		+150	$^\circ\text{C}$

A.2 MATLAB code

Here, the Matlab code for calculating the losses present in the design solution 2 is presented. Similar coding was done for solution 1a.

A.2.1 Idle operation

```

clc
clear all
grid on

VRail = 70; % Voltage on the rails [V]
R1 = 8; % load resistance [Ohm]
C1 = 1e-6; % Output filter capacitance [F]
L1 = 15e-6; % Output filter inductance [H]
C_snubber = 1e-9; % Snubber capacitor [F]
R_snubber = 15; % Snubber resistance [Ohm]
R_sw = 32e-3; % On resistance in switches [Ohm]
Cb = 2.5e-6; % Buck filter capacitance [F]
Lb = 0.5e-6; % Buck filter inductance [H]

%% Losses in load during , 50 % duty cycle (0 V over load ideally)

UR1_rms = 208.5e-3; % RMS voltage over the load [V]
LR1_rms = 26.01e-3; % RMS current through the load [A]
PR1 = UR1_rms*LR1_rms; % Power consumed by load [W]

%% Losses in switches and load , 50 % duty cycle (0 V over load ideally)

% Buck switches
load('BuckSw_idle.mat');
A = BuckSw_idle(:,2).*BuckSw_idle(:,3);
P_sw = trapz(BuckSw_idle(:,1),abs(A))*2*1e3;

% Class D outputstage switches
load('ClassDsw_idle.mat');
B = ClassDSw_idle(:,2).*ClassDSw_idle(:,3);
P_swD = trapz(ClassDSw_idle(:,1),abs(B))*4*1e3;

% Load losses
load('Load_idle.mat');
C = Load_idle(:,2).*Load_idle(:,3);
P_load = trapz(Load_idle(:,1),abs(C))*1e3;

%% Losses in snubber resistors

P_snubb_tot = 12.37e-3; % Losses in the snubber resistors [W]

```

```

%% Input apparent power, 50 % duty cycle (0 V over load ideally)
% Buck Converter

U_in_RMS = 16.53;           % Input voltage to output stage (from buck) [V]
I_in_RMS = 482.15e-3;      % Input current to output stage (from buck) [A]
S_in_RMS = U_in_RMS*I_in_RMS; % apparent power entering
                                % the output stage [VA]

% Input from voltage source
Us_in_RMS = 148.36;        % Input voltage after current limiter [V]
Is_in_RMS = 4.9e-3;        % Input through the current limiter [A]
Ss_in_RMS = Us_in_RMS.*Is_in_RMS; % Input power from the source
                                % (during steady state) [VA]

% The reactive input power will therefore be:

Qs_in_RMS = sqrt( (Ss_in_RMS)^2 - (P_sw+P_R1+P_snubb_tot+P_swD)^2 );

```

A.2.2 Medium output power

```

clc
clear all
grid on

VRail = 70;           % Voltage on the rails [V]
R1 = 8;               % load resistance [Ohm]
C1 = 1e-6;            % Output filter capacitance [F]
L1 = 15e-6;           % Output filter inductance [H]
C_snubber = 1e-9;     % Snubber capacitor [F]
R_snubber = 15;       % Snubber resistance [Ohm]
R_sw = 32e-3;         % On resistance in switches [Ohm]
Cb = 2.5e-6;          % Buck filter capacitance [F]
Lb = 0.5e-6;          % Buck filter inductance [H]

%% Losses in load during

U_R1_rms = 55.4/sqrt(2); % RMS voltage over the load [V]
I_R1_rms = 6.93/sqrt(2); % RMS current through the load [A]
P_R1 = U_R1_rms*I_R1_rms; % Power consumed by load [W]

%% Losses in switches

% Buck switches
load('BuckSw_60V.mat');
A = BuckSw_60V(:,2).*BuckSw_60V(:,3);
P_sw = trapz(BuckSw_60V(:,1),abs(A))*2*1e3;

% Class D outputstage switches
load('ClassDsw_60V.mat');

```

```

B = ClassDSw_60V(:,2).*ClassDSw_60V(:,3);
P_swD = trapz(ClassDSw_60V(:,1),abs(B))*4*1e3;

%% Losses in snubber resistors

P_snubb_tot = 203.7e-3;           % Losses in the snubber resistors [W]

%% Input apparent power
% Buck Converter
U_in_RMS = 57.17;                % Input voltage to output stage (from buck) [V]
L_in_RMS = 4.25;                % Input current to output stage (from buck) [A]
S_in_RMS = U_in_RMS*L_in_RMS;   % apparent power entering
                                % the output stage [VA]

% Input from voltage source
Us_in_RMS = 144.97;             % Input voltage after current limiter [V]
Is_in_RMS = 1.75;              % Input through the current limiter [A]
Ss_in_RMS = Us_in_RMS.*Is_in_RMS; % Input power from the source
                                % (during steady state) [VA]

% The reactive input power will therefore be:

Qs_in_RMS = sqrt( (Ss_in_RMS)^2 - (P_sw+P_R1+P_snubb_tot+P_swD)^2 );

```

Bibliography

- [1] National Measurement Office, "Standby and off leaflet", *Department for business innovation & Skills*, [2010-03-22], [Online]. Available: <http://www.bis.gov.uk/assets/nmo/docs/eup/leaflets/standby-and-offleaflet.pdf>, [Accessed: 2014-01-15].
- [2] Company A, Project description, [2013-12-15].
- [3] N. Mohan; T.M. Undeland; W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, John Wiley & Sons, Inc., 2003.
- [4] B. Cordell, *Designing Audio Power Amplifiers*, McGraw-Hill, 2011.
- [5] Wikipedia, *Amplifier*, *Wikipedia*, available: http://en.wikipedia.org/wiki/Amplifier#Power_amplifier, Accessed: [2014-01-15].
- [6] D. Self, *Audio Power Amplifier Design Handbook*, Taylor & Francis, 2012.
- [7] J. Liu, Y. Allasasmeh, S. Gregori, B. Leesti, M. Snelgrove, *Envelope tracking H-bridged audio amplifier with improved efficiency and thd less than 0.1 %*, in: Computer Engineering (CCECE), 2012 25th IEEE Canadian Conference on, 2012, pp. 1–4.
- [8] C. W. Lin, B. S. Hsieh, *An anti-clipping protection system for multilevel class-D amplifier*, in: Electrical Engineering: Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2011 8th International Conference, 2011, pp. 129–132.
- [9] K. Jeppson, *Mikroelektronik*, Chalmers Tekniska Högskola, 2011.
- [10] A. S. Sedra; K.C. Smith, *Microelectronic Circuits*, sixth Edition, Oxford University Press, Inc., 2011.
- [11] Wikipedia, *Time Constant*, *Wikipedia*, Available: http://en.wikipedia.org/wiki/Time_constant, [Accessed: 2014-01-15].

- [12] DesignSpark PCB, Free-of-charge schematic capture and pcb layout program, RS Components and Number One Systems, [2014-01-21], [Online]. Available: <http://www.designspark.com/designspark/electronics/eng/page/designspark-pcb-home-page>, [Accessed: 2014-04-29].

- [13] H. J. Zhang, Linear Technology, *PCB Layout Considerations for Non-Isolated Switching Power Supplies*, [2012-09-20], Application Note, Available: <http://cds.linear.com/docs/en/application-note/an136f.pdf>, [Accessed: 2014-04-29].