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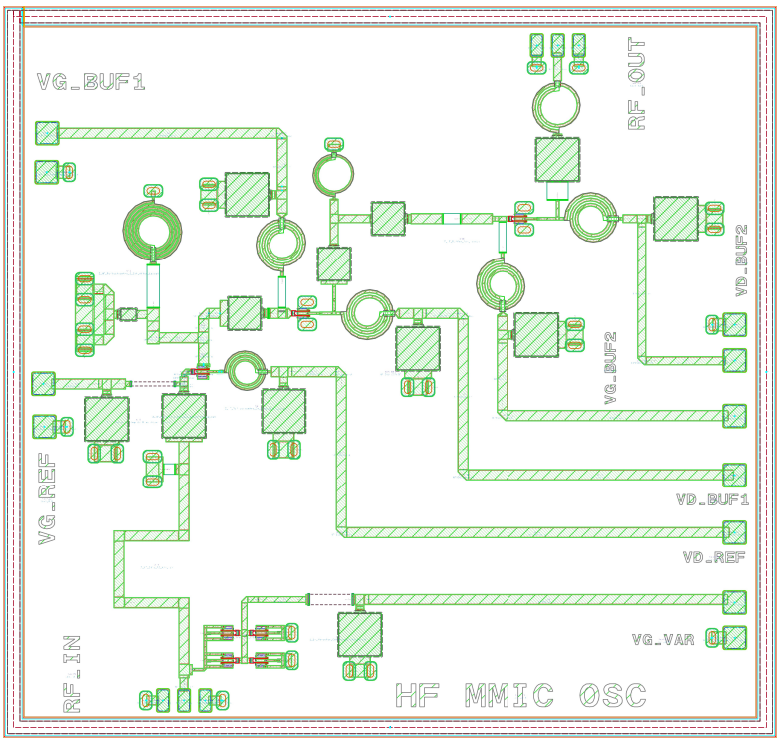

GaN MMIC Oscillator Design for Low Phase Noise Using a Tunable Cavity Resonator

Master's thesis in Wireless, Photonics and Space Engineering

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Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
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Cover: The designed reflection amplifier for 13.3 to 14.7 GHz.

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Abstract

One of the main limiting factors that prevents higher data rates in the communication systems of today is the phase noise of oscillators. To reach lower phase noise, the most effective improvement is to use resonators with higher quality factor (Q). On-chip resonators typically have poor quality factor so an external resonator is preferred from a performance perspective. Another way of lowering phase noise is to increase the power inside the oscillator, e.g., by using a high-power device technology.

This thesis presents simulation and design of two Gallium Nitride (GaN) MMIC based reflection type oscillators with integrated phase shifters, designed in the WIN Semiconductors NP15 GaN HEMT technology. The integrated phase shifter can be used for compensating interconnect parasitics as well as phase locking with a PLL. The designs are intended for high-Q mechanically tunable cavity resonators for two different frequency bands, 11.6 to 13.0 GHz and 13.3 to 14.7 GHz.

The thesis also presents transistor-model port de-embedding, required to extract a three-port transistor model from the two-port common-source model available in the design kit.

Simulations based on WIN's design kit, the de-embedded device model, and simulated cavity S parameters indicate minimum phase noise of -142 dBc/Hz at 100 kHz offset for the low-frequency band and -133 dBc/Hz at 100 kHz offset for the high-frequency band.

Keywords: GaN oscillator, GaN, Reflection oscillator, Cavity resonator, MMIC, High Q ocillator

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Johan Karlsson, Usman Shehryar, Gothenburg, June 2020

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1

Introduction

In order to increase the data rates in wireless communication systems, the communication moves to higher and higher frequencies where more bandwidth is available. Low phase noise frequency generation is difficult at the high frequencies that will be used in next generation wireless systems. One of the main problems that limit data rates is the phase noise performance of the local oscillator (LO) in both transmitters and receivers [2]. Because of this, the frequency generation often takes place at a lower frequency and by using frequency multipliers, the wanted LO frequency is attained. This has the drawback of increasing the phase noise, which prevents higher data rates in wide-band systems [3].

There are two main strategies for lowering the phase noise. The first is to utilize a high quality factor (Q) low-loss resonator as a part of the oscillator. The second way of reducing the LO phase noise floor is to have more power in the oscillator [4, 5].

For large scale communication systems, monolithic microwave integrated circuits (MMIC) based system components are preferred. In a MMIC, active and passive circuit elements are combined on a semiconductor substrate. This enables the creation of complex high-performing systems, that can be mass produced reliably, in a small circuit footprint. A drawback of MMIC systems are their inability to be tuned after manufacturing. Thus it is very important to use good models during the design, that accurately describe the performance of a manufactured MMIC.

1.1 Microwave resonators

A simple microwave resonator can consist of only an inductor and a capacitor. When implemented in a MMIC the quality factor is poor, often around 40 [2]. A distributed element MMIC resonator have a similarly poor quality factor [2]. An off-chip resonator can have much higher Q than an integrated MMIC resonator and has the disadvantage of using much more space than an integrated resonator. The off-chip interconnects also constitute a problem at higher frequencies as their loss increases with frequency.

A fixed frequency cavity resonator can have a Q value of several thousand [2]. A cavity resonator with a tunable perturbation will have lowered Q, but with the upside of having a tunable resonance frequency [1].

Dielectric resonators (DR) also have a high quality factor, in the order of several

thousand. They can be tuned mechanically by either moving the DR or by having a moving metallic object near the DR [2, 6].

Yttrium iron garnet (YIG) resonators have both high Q, in the order of several thousand, and are tunable to large bandwidths. The main drawbacks of a YIG resonator are that they are difficult to manufacture, are expensive to buy and sensitive to vibrations [6].

1.2 Gallium nitride (GaN) transistor properties

Gallium nitride (GaN) high-electron-mobility transistors (HEMT) are good for high power applications, since they have a large band gap and thus can withstand higher voltages without breaking down. This enables smaller transistors that can handle high power levels, with breakdown voltages in the order of tens of volts even for small transistors. Thus the transistor can be made small enough to have a high maximum frequency.

GaN transistors have a major flaw for oscillator design. GaN-HEMT have large amounts of flicker noise that increases the phase noise [2]. A high power GaN reflection oscillator with a high Q resonator might be enough to get low enough phase noise, even though it has high amount of flicker noise. How to utilize GaN and an off-chip resonator has been researched by Mikael Hörberg, who has designed several GaN MMIC oscillators using high Q off-chip cavity resonators [2].

1.3 Aim

The aim of this thesis is to design and fabricate two GaN MMIC reflection amplifiers that utilizes two off-chip high Q mechanically tunable resonator cavities. The cavities are tunable from 11.6 GHz to 13.0 GHz and 13.3 GHz to 14.7 GHz [1]. The phase noise needs to be low, at least below the levels presented in Table 1.1, so that after six times multiplication it can span the telecommunication E-band, 71 to 76 GHz and 81 to 86 GHz, and increase the possible data rates.

Both oscillators need an integrated phase shifting mechanism to enable the use of a phase-locked-loop (PLL) to regulate their oscillation frequency. A buffer amplifier to isolate the oscillator from load variations and to provide output power control will also be implemented. The reflection amplifiers needs to have higher reflection gain than the resonator loss at resonance. The reflection gain needs to be controlled by the reflection amplifier bias voltage, in order to control the resonator coupling.

WIN semiconductors NP-15 GaN process will be used for the design and manufacturing of these oscillators.

1.4 Scope

The thesis will only consider the WIN NP-15 GaN process for the design. It will be limited to only cover simulations since the manufacturing tape-out is after the

Table 1.1: Wanted performance for the two oscillators divided into low frequency (LF) and high frequency (HF).

	LF Oscillator	HF Oscillator	
Frequency range	11.6-13.0	13.3-14.7	GHz
Phase noise (100 kHz)	<-135	<-130	dBc/Hz
Phase noise (100 MHz)	<-165	<-165	dBc/Hz
Output power	>5	>5	dBm
Harmonic suppression	>20	>20	dB

expected end of the thesis. Measurements to verify the oscillator will not be performed. The thesis will only use Pathwave Advanced Design System (ADS) 2019 v1.0 from Keysight for all the oscillator simulations. The two resonators are already designed and will not be changed or optimized in any way. Even though a goal is to phase lock the oscillators using a PLL, the PLL is left outside this work. All simulations presented assumes free-running oscillators. No package for the oscillator will be considered during the design, though bondwires are considered in the design.

1.5 Societal, ethical and ecological aspects

Today, the data consumption and data rates are increasing rapidly. An oscillator with better phase noise performance will enable higher data rates for a given output power level. The last power amplifier stage of a radio transceiver typically dominates the power consumption, so if less output power can be used, the total power consumption of the system is reduced. A lower power consumption is better for the environment, since less electrical energy need to be produced. A lower power consumption also lowers the running cost of the system. Lower running costs might also give more people access to high data rate internet. A lower output power reduces the electromagnetic interference generated by the system.

2

Oscillator Theory

An oscillator is a device that converts DC power to RF power. Ideally an oscillator generates only a single tone at one specific frequency, however due to noise, all oscillators have a small frequency bandwidth. These short term frequency fluctuations are called phase noise [7].

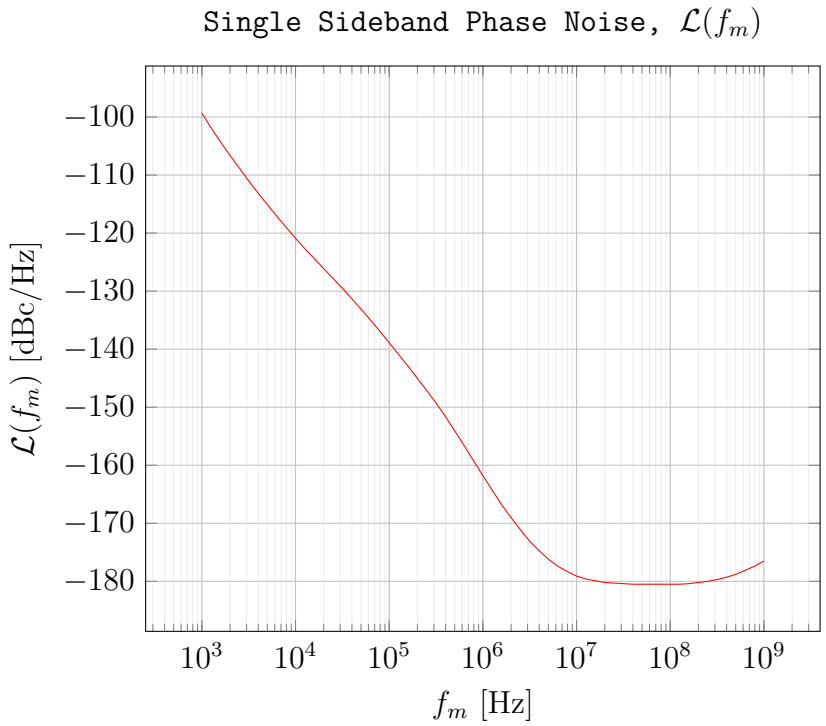

Figure 2.1: Single sideband phase noise for an oscillator.

Phase noise is symmetric around the center frequency, so often only one sideband is displayed. The single-sideband phase noise is denoted $\mathcal{L}(f_m)$ and has the unit dBc/Hz at a given frequency offset from the carrier (f_m) [8]. The single side phase noise is often displayed in a logarithmic plot, which is shown in Figure 2.1.

In the following section feedback oscillator analysis and reflection oscillator analysis will be presented. Phase noise and how to reduce it will also be discussed.

2.1 Feedback oscillator analysis

The most traditional view of an oscillator is that of an amplifier where the output is fed back to the input through a filter structure, as illustrated in Figure 2.2. The filter provides positive feedback to make the amplifier more unstable.

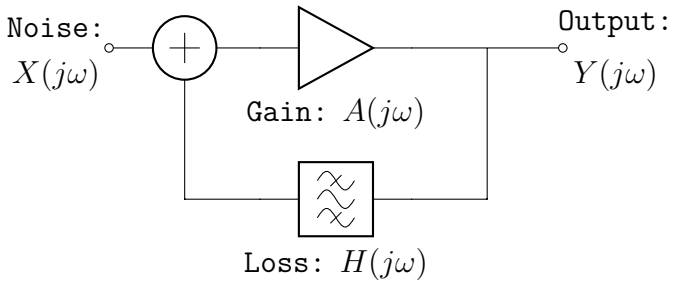

Figure 2.2: A model of a feedback oscillator. The filter provides positive feedback to make the oscillator more unstable so it can oscillate.

The output signal, $Y(j\omega)$, can be expressed by

$$Y(j\omega) = X(j\omega)\frac{A(j\omega)}{1 - A(j\omega)H(j\omega)} \tag{2.1}$$

where $X(j\omega)$ is the input signal, which is thermal noise in this case. $A(j\omega)$ is the gain of the amplifier and $H(j\omega)$ is the loss of the filter [8].

When the so called open loop gain $A(j\omega)H(j\omega)$ equals one, the circuit can oscillate [8]. The energy provided by the amplifier should be equal the energy lost in the filter for the oscillation amplitude to be stable. It is important that the phase shift around the loop causes the signal to add up in-phase. This is called the Barkhausen criterion.

$$A(j\omega)H(j\omega) = 1 + j \cdot 0 \tag{2.2}$$

A common way of writing this is

$$|A(j\omega)H(j\omega)| = 1 \tag{2.3}$$

together with

$$\underline{/A(j\omega)H(j\omega)} = 2\pi n, \quad n \in \{0, \pm 1, \pm 2...\}. \tag{2.4}$$

The Barkhausen criterion is not enough to determine if the oscillation will start since it does not disclose enough about the stability of the system. The stability is determined by the right half plane zeroes of $1 - A(j\omega)H(j\omega)$ [8].

The system is unstable and can oscillate if the loop gain, $A(j\omega)H(j\omega)$, in a complex polar plot passes $1 + j \cdot 0$ in a clock-wise manner. The steady state oscillation is reached when the loop gain passes through $1+j\cdot 0$ due to nonlinear gain compression

in the amplifier. This can be seen in Figure 2.3. This test to determine the stability of the system is called the Nyquist stability test. The diagram showing $A(j\omega)H(j\omega)$ is consequently called a Nyquist plot. [8].

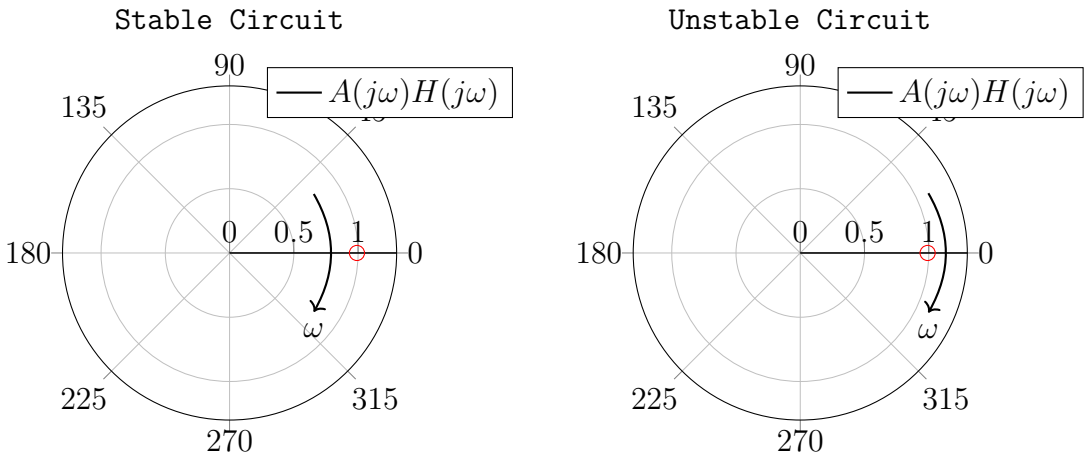

Figure 2.3: Nyquist criterion for a stable and an unstable circuit. If $1 + j \cdot 0$ is passed in a clock-wise manner, the circuit is unstable and will start oscillating.

2.2 Reflection oscillator analysis

A reflection oscillator, or as it is sometimes called, a negative resistance oscillator is another way of viewing an oscillator. Reflection oscillator analysis is common in microwave applications, where the internal capacitances of the transistor have a large impact on the design since they provide a large part of the feedback [8].

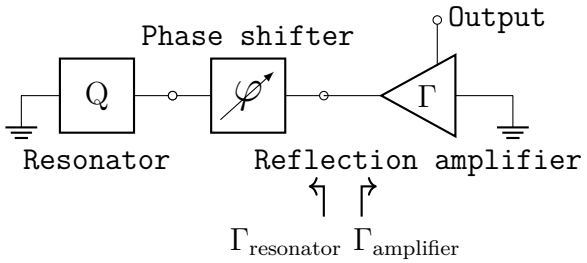

Figure 2.4: A reflection oscillator consists of an amplifier, a phase shifter and a resonator. The amplifier presents a negative resistance so its reflection coefficient is larger than 1.

A reflection oscillator consists of three main parts, as depicted in Figure 2.4. An amplifier that is unstable and presents a reflection coefficient ($\Gamma_{\text{amplifier}}$) larger than 1. A resonator that reflects ($\Gamma_{\text{resonator}}$) the wanted frequency and absorbs all other frequencies.

The amplifier needs to provide at least the amount of energy that is lost in the resonator, so that

$$|\Gamma_{\text{amplifier}}\Gamma_{\text{resonator}}| = 1 \tag{2.5}$$

For the oscillation to start, the product of $|\Gamma_{\text{amplifier}}\Gamma_{\text{resonator}}|$ needs to be larger than one. Due to nonlinear gain compression in the amplifier this will reduce so the product will equal one at a steady oscillation [8].

The third and last component is a phase shifter that ensures that the reflections adds up in phase so that

$$\angle\Gamma_{\text{amplifier}}\Gamma_{\text{resonator}} = 2\pi n, \quad n \in \{0, \pm 1, \pm 2...\} \tag{2.6}$$

Equation 2.5 and 2.6 are similar to the Barkhausen criterion, since they have the same physical interpretation. Just like with the feedback oscillator, these criteria do not fully describe the stability of the system. For a stable oscillation, the Kurokawa criterion needs to be satisfied [8]

$$\left(\frac{\partial R_{\text{amplifier}}(A)}{\partial A}\Big|_{A=A_0} \frac{\partial X_{\text{resonator}}(\omega)}{\partial \omega}\Big|_{\omega=\omega_0} - \frac{\partial X_{\text{amplifier}}(A)}{\partial A}\Big|_{A=A_0} \frac{\partial R_{\text{resonator}}(\omega)}{\partial \omega}\Big|_{\omega=\omega_0} \right) > 0 \tag{2.7}$$

where $R_{\text{amplifier}}(A, \omega)$ is the negative resistance presented by the amplifier and $X_{\text{amplifier}}(A, \omega)$ is the reactance of the amplifier. $R_{\text{resonator}}(A, \omega)$ is the equivalent resistance of the resonator and $X_{\text{resonator}}(A, \omega)$ is the equivalent reactance of the resonator. All of them have both an amplitude (A) and frequency (ω) dependence. A derivation of how a negative resistance can be presented by an active device can be found in [8] and [9].

2.3 Resonators

A resonator is a device that exhibits resonance at one or more frequencies. Resonance is when the impedance of the device reaches a minimum or maximum, while the reactance equals zero. The inductive reactance cancels the capacitive reactance of the device. The two simplest versions of electrical resonators are the parallel RLC resonator and the series RLC resonator, as shown in Figure 2.5. An ideal RLC resonator is resonant only for one frequency, ω_0 and consists of a resistor (R), an inductor (L) and a capacitor (C).

The losses of a resonator may be defined by the quality factor (Q) of the resonator [8]

$$Q = \omega \frac{\text{Stored energy}}{\text{Average power loss}}. \tag{2.8}$$

The higher the Q factor is, the more narrow banded the frequency response of the resonator is. Figure 2.6 shows the normalized impedance as a function of normalized angular frequency of both a parallel and series resonator with $Q = 10$. A higher Q gives a narrower impedance maximum/minimum. It can be shown that the following equation is another way of calculating Q [8].

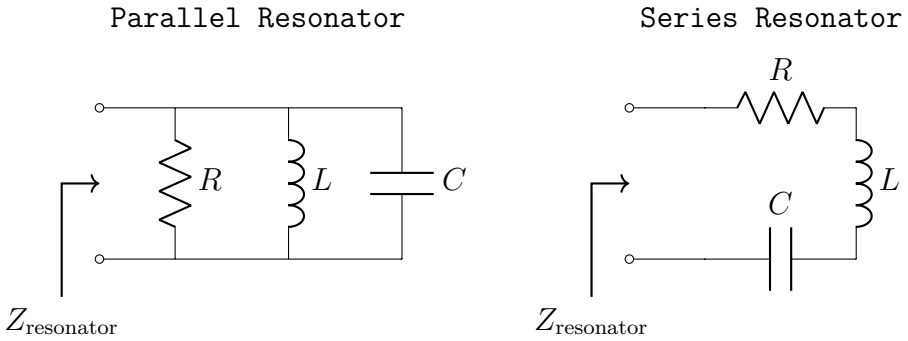

Figure 2.5: Circuit schematic of a parallel RLC resonator and a series RLC resonator.

$$Q = \frac{\omega_0}{\Delta\omega_{-3dB}} \tag{2.9}$$

Where ω_0 is the resonant angular frequency and $\Delta\omega_{-3dB}$ is the -3 dB impedance bandwidth between the two frequencies where the impedance has changed by 3 dB from the resonant value. That is the bandwidth between $|Z_{\text{resonator}}| = R/\sqrt{2}$ for a parallel RLC resonator and $|Z_{\text{resonator}}| = R\sqrt{2}$ for a series RLC resonator. Note that the $\Delta\omega_{-3dB}$ should not be obtained directly from S-parameters -3 dB bandwidth, since the scattering parameters are not a linear function of impedance.

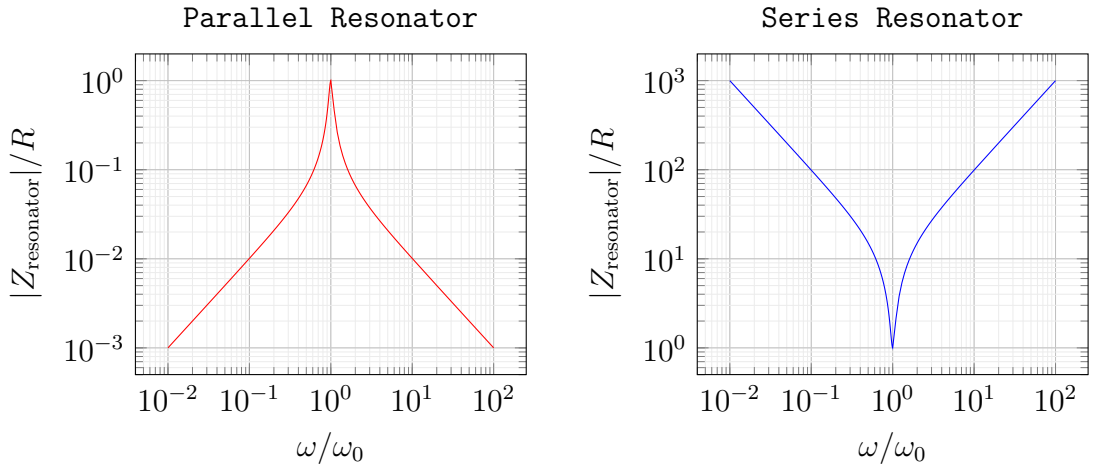

Figure 2.6: Impedance of a parallel RLC resonator and a series RLC resonator as a function of angular frequency where $Q = 10$ for both resonators.

The phase response of the resonator is also dependant on Q. The higher the Q, the faster the phase will change near the resonance frequency

$$\partial\omega = \pm \frac{\omega_0}{2Q} \partial \angle Z_{\text{resonator}} \Big|_{\omega=\omega_0} . \tag{2.10}$$

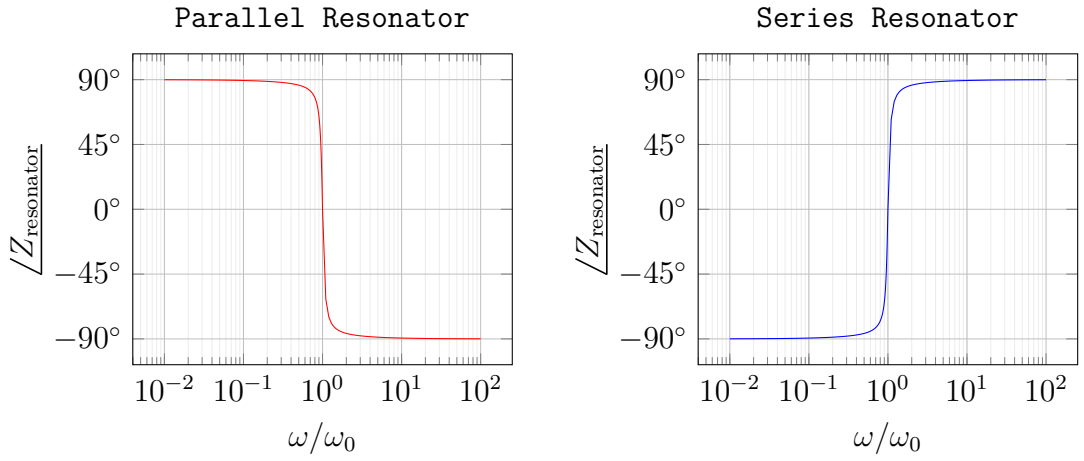

Figure 2.7: Phase response of a parallel RLC resonator and a series RLC resonator as a function of angular frequency where $Q = 10$ for both resonators.

This can be seen in Figure 2.7. This also means that at resonance, the frequency is only minorly affected by phase fluctuations caused by noise. This is why a high Q resonator is beneficial for reducing the phase noise in an oscillator [8].

Equation 2.10 can also be rewritten to form an expression for Q. It is a smooth function around the resonance frequency, which only gives the actual Q factor for $\omega = \omega_0$, the resonance frequency [8]. The smoothness of the function makes it usable for accurately calculating the Q factor from a set of measured impedances [1].

$$Q = \pm\frac{\omega_0}{2}\frac{\partial \angle Z_{\text{resonator}}}{\partial\omega}\bigg|_{\omega=\omega_0} \tag{2.11}$$

For a parallel resonator, a minus sign is required in both Equation 2.10 and 2.11 since the phase changes in the opposite direction of the frequency like shown in Figure 2.7.

When a resonator is coupled to any other circuit, the total Q factor will degrade. The resulting lower quality factor is called the loaded quality factor, Q_L. For the rest of the thesis, Q_0 will refer to the unloaded quality factor. Depending on how much the resonator is loaded, the Q_L will vary. β is the so called coupling coefficient that describes how much the resonator has been loaded. In Figure 2.8 the reflection coefficient as a function of β is shown [8].

$$Q_L = Q_0\left(\frac{1}{1+\beta}\right) \tag{2.12}$$

When β is smaller than 1, the system is said to be under coupled. When β equals 1, the system is critically coupled. When β is larger than 1, the system is over coupled [10].

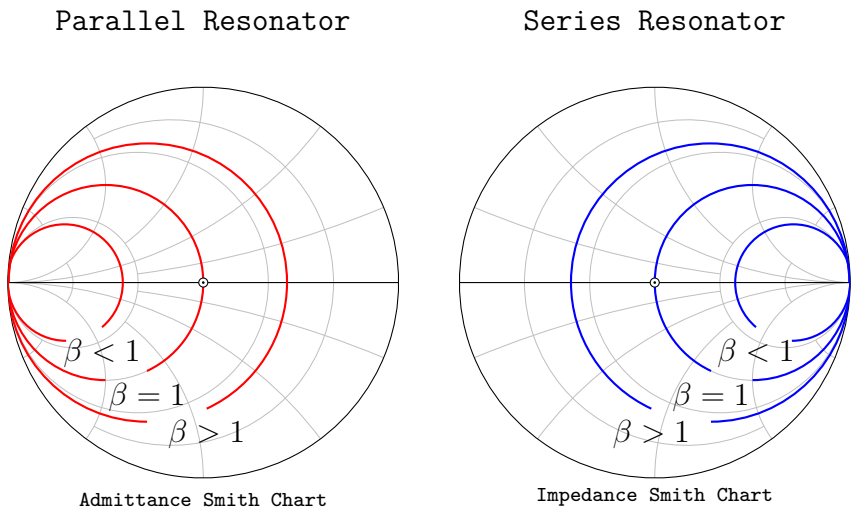

Figure 2.8: Reflection coefficient for a coupled resonator, with different coupling factors.

In a reflection amplifier, the amplifier loads the resonator so the load resistance equals $R_{\text{amplifier}}$. β can be expressed as [2]

$$\beta = \frac{|R_{\text{load}}|}{R_{\text{resonator}}} = \frac{|R_{\text{amplifier}}|}{R_{\text{resonator}}} = \frac{|\text{Real}(Z_{\text{amplifier}})|}{\text{Real}(Z_{\text{resonator}})} \tag{2.13}$$

where $Z_{\text{amplifier}}$ is the impedance seen when looking towards the amplifier and $R_{\text{amplifier}}$ is negative for a reflection amplifier.

To use the resonator, it needs to be coupled to the rest of the circuit. Low coupling (under coupling) to the resonator gives a higher Q_L but there is less power in the oscillator. High coupling (over coupling) on the other hand, increases the power in the oscillator, but lowers Q_L. How phase noise depends on these factors will be described in more detail in Section 2.5.

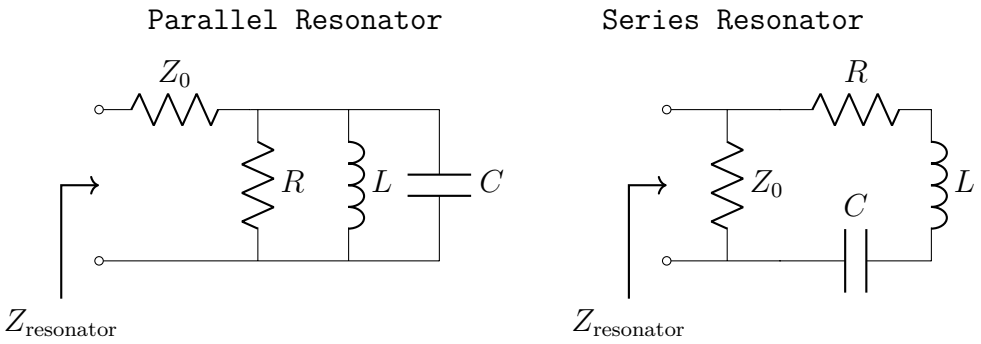

Figure 2.9: Circuit schematic of a parallel RLC resonator and a series RLC resonator terminated with characteristic impedance Z_0 to absorb power outside resonance.

When a resonator is terminated with the characteristic impedance Z_0, it will instead reflect power at the resonance frequency and absorb power for all frequencies outside

resonance. A schematic of this can be seen in Figure 2.9. Its frequency behaviour can be seen in Figure 2.10. The Q_L factor will be affected by adding this termination [10]

$$Q_L = Q_0 \left(\frac{1}{1+\beta}\right)\left(\frac{1}{1+\kappa}\right) \tag{2.14}$$

where

$$\kappa = \frac{|\Gamma_{\text{resonator}}(\omega_0)|}{1-|\Gamma_{\text{resonator}}(\omega_0)|} \tag{2.15}$$

and $\Gamma_{\text{resonator}}(\omega_0)$ is the reflection coefficient looking into the resonator terminated with characteristic impedance at the resonance frequency.

$$\Gamma_{\text{resonator}}(\omega_0) = \frac{Z_{\text{resonator}}(\omega_0) - Z_0}{Z_{\text{resonator}}(\omega_0) + Z_0} \tag{2.16}$$

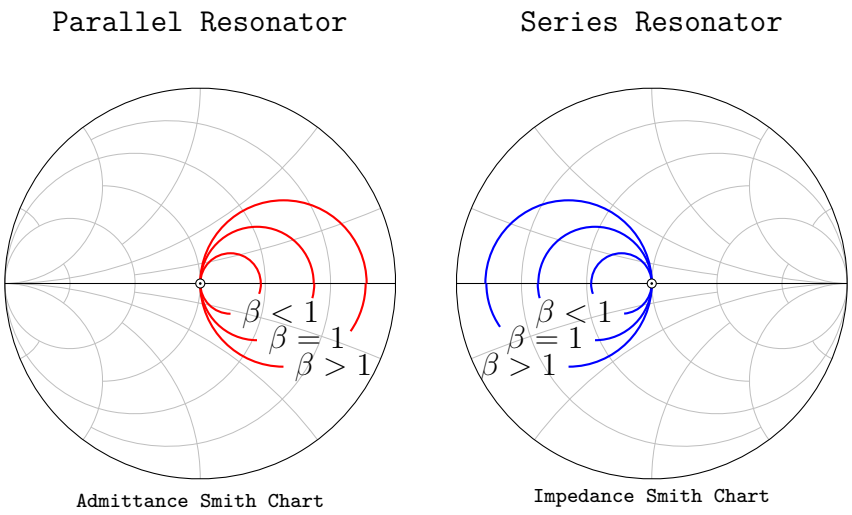

Figure 2.10: Reflection coefficient for a coupled resonator terminated with characteristic impedance Z_0, with different coupling factors. Smith chart is normalized to Z_0.

2.4 Oscillator performance measures

There are different performance measures that are important for an oscillator design. Depending on the application, some are more important than others. An oscillator is typically used as a so called local oscillator (LO) together with a mixer to translate the frequency content up or down in frequency. Most of the important performance criteria for an oscillator reflects on this. Typical performance goals for an oscillator is shown in Table 2.1.

Table 2.1: Typical performance goals for an oscillator

Parameter	**Typical value**
Oscillation frequency	Depends on application
Tuning range	Depends on application
Phase noise	Depends on application, e.g -110 dBc/Hz at 100 kHz offset is required for a 4 MHz channel bandwidth that uses 1024-QAM [2, 11]
Output power	0-10 dBm
Harmonic suppression	> 20 dB
Power consumption	As low as possible

Often, the most important part of the oscillator is that it oscillates at a certain frequency, or that it can span a certain frequency range. An LO with an incorrect frequency will cause upconverting mixers to convert the signal to the wrong center frequency, maybe even outside the frequency band that is supposed to be used for the application. A downconverting mixer will be affected by an incorrect frequency and will downconvert noise or even a different signal than the wanted one.

The tuning range of an oscillator that will be used in this thesis is defined as

$$\text{Tuning range} = \frac{(f_{\text{high}} - f_{\text{low}})}{(f_{\text{high}} + f_{\text{low}})/2} \cdot 100\% \tag{2.17}$$

where f_{high} is the highest achievable oscillation frequency and f_{low} the lowest.

The phase noise of an oscillator describes its short term frequency stability. Noise will distort the sinusoidal signal and cause it to have energy in frequencies beside the wanted central frequency [8]. In a system with a significant amount of phase noise, it is more difficult to separate signals with a small frequency separation. This can be seen in Figure 2.11 and 2.12. Phase noise will also distort the transmitted signal by adding a random phase rotation [8]. This behaviour can be seen in Figure 2.13.

A high phase noise floor will impact performance, especially when the oscillator will be used together with frequency multipliers, as the frequency multipliers raise the noise floor [3]. How to model phase noise will be discussed in Section 2.5.

An oscillator used in conjunction with a mixer must provide enough output power to drive the mixer. Mixers typically require between 0 dBm to 10 dBm of oscillator

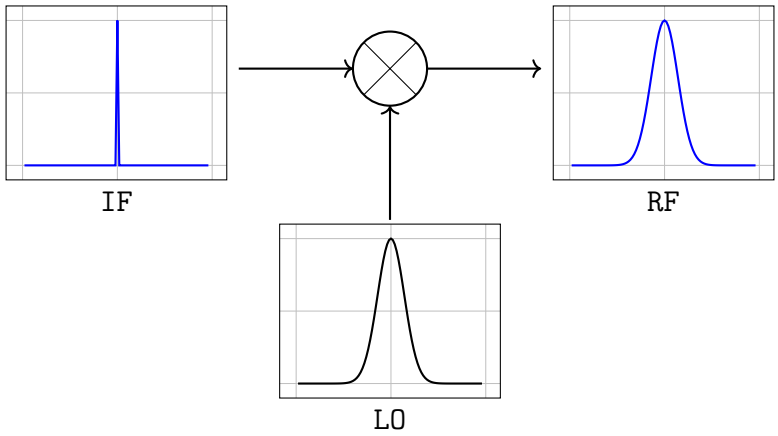

Figure 2.11: Phase noise will broaden the frequency spectrum of a single tone.

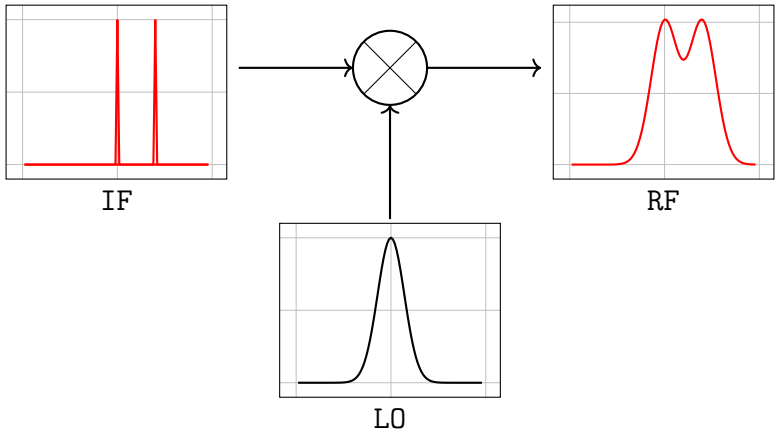

Figure 2.12: When two tones close to each other in frequency enter the mixer, they will interfere with each other when there is significant LO phase noise. It is difficult to separate the information from the two tones.

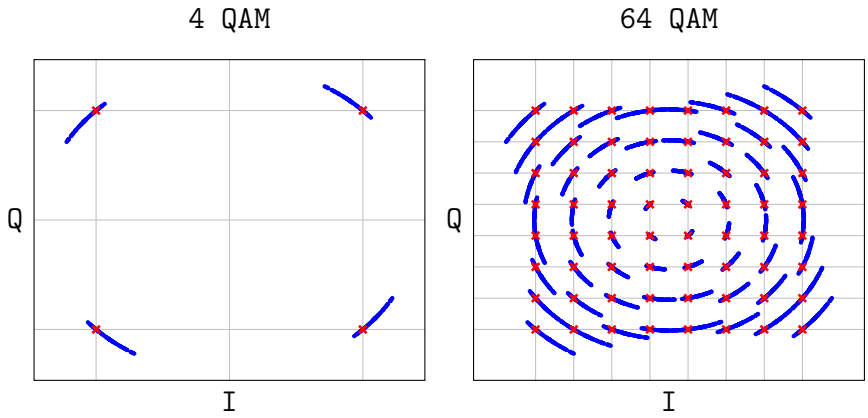

Figure 2.13: How phase noise affects a transmitted signal constellation. Red is the transmitted signal constellation without phase noise. Blue is the signal when it is affected by phase noise.

power [2, 11]. If unwanted frequencies enter a mixer with enough power, those frequencies will also contribute to frequency mixing in an unwanted way. Thus an oscillator needs to suppress harmonics and spurious frequencies beside the main frequency.

A low power consumption and a high efficiency are important for an oscillator, since it wastes less energy and thus is better for the environment and lowers the running electricity costs.

Wagnemans DC power and frequency scaled Figure-of-Merit (FoM) will be used as a performance measure to decide how well the oscillator performs [2].

$$\text{FoM} = -\mathcal{L}(f_m) + 20\log_{10}\left(\frac{f_0}{f_m}\right) - 10\log_{10}\left(\frac{P_{DC}}{1\text{ mW}}\right) \tag{2.18}$$

The best possible FoM is only a function of resonator Q_0 [2].

$$\text{FoM}_{\text{MAX}} = +174.6 + 20\log_{10}(Q_0) \tag{2.19}$$

2.5 Phase noise modelling

An ideal oscillator should have a stable amplitude, frequency and phase over the desired frequency range. However, practical oscillators have a time varying behaviour due to several different effects. Temperature changes result in a significant frequency shift. Component ageing result in a frequency drift with the passage of time. These frequency drifts are more predictable long term phenomena [8].

Oscillators can be modelled as linear time-varying systems, even though amplitude stabilization is caused by nonlinearities. Depending on where in the oscillation cycle the noise is injected into the oscillator, there will be short term amplitude and phase deviations. Since noise is a random process, unpredictable amplitude and phase deviations will be present [7].

$$v_0(t) = A(t)\cos[\omega_0 t + \phi(t)] \tag{2.20}$$

For a sinusoidal signal $v_0(t)$ with oscillation frequency ω_0, $A(t)$ is the amplitude modulation noise (AM noise) and $\phi(t)$ is the random phase variation, which modulates the frequency of the oscillator (FM noise) [8]. The phase variation will affect the oscillation frequency since the instantaneous angular frequency is

$$\omega(t) = \frac{d}{dt}\left[\omega_0 t + \phi(t)\right] = \omega_0 + \frac{d\phi(t)}{dt} \tag{2.21}$$

This short term frequency instability is called phase noise and is a result of random noise generated in the component technologies.

Amplitude noise is often of less concern due to gain compression in active devices, which attenuates amplitude noise [7]. A phase noise measurement with a phase

noise plateau can be a sign that there is significant amplitude noise [7]. Figures 2.11, 2.12 and 2.13 show how FM noise affects the transmitted signals. AM noise would add time varying amplitude to all graphs. This will affect the constellation in Figure 2.13, by adding random amplitude variations, which can cause even more signal decoding errors [8].

2.5.1 Leeson's phase noise model

Leeson's phase noise model is a linear time-invariant phase noise model for feedback style oscillators [4]. Even though it is a time invariant model, it describes what needs to be considered when designing for low phase noise

$$\mathcal{L}(f_m) = 10\log_{10}\left(\frac{FkT}{2P_{in}}\left[1+\left(\frac{f_0}{2Q_L f_m}\right)^2\right]\left[1+\left(\frac{f_{1/f^3}}{f_m}\right)\right]\right) \tag{2.22}$$

where F is the empirical noise figure, k is Boltzmann's constant, T is the ambient temperature in Kelvin, P_{in} is the input power to the amplifier, f_0 is the oscillation frequency and f_{1/f^3} is the flicker noise corner. The noise floor power is

$$\mathcal{L}(\infty) = \frac{FkT}{2P_{in}} = -177 \text{ dBc/Hz for } P_{in} = 0 \text{ dBm and } F = 1 \tag{2.23}$$

When the expression for Q_L in Equation 2.12 is inserted into Leeson's phase noise model, and differentiated with respect to β, the phase noise is minimised for a critically coupled resonator, $\beta = 1$ ($\frac{Q_L}{Q_0} = \frac{1}{2}$).

2.5.2 Everard's phase noise model

Everard's phase noise model is a linear time-invariant phase noise model for all kinds of feedback, including negative resistance oscillators, and how different models affect the optimal coupling. The model does not take flicker noise into account [5].

$$\mathcal{L}(f_m) = 10\log_{10}\left(\frac{FkT}{8Q_0^2(\beta/(1+\beta)^3)P_{RF}}\left(\frac{f_0}{f_m}\right)^2\right) \tag{2.24}$$

P_{RF} is the power delivered by the reflection amplifier.

When Everard's phase noise model is differentiated with respect to β, the phase noise is minimised for an under coupled resonator with $\beta = 0.5$ ($\frac{Q_L}{Q_0} = \frac{2}{3}$).

2.5.3 Optimal resonator coupling to minimize phase noise

Strong resonator coupling will increase the power in the resonator, which lowers phase noise. On the other hand, strong resonator coupling will lower the quality factor, which increases the phase noise. Thus the resonator coupling, β, is important to optimize in order to minimize phase noise. Leeson's model predicts that $\beta = 1$ is

the optimal resonator coupling to minimize phase noise. However Everard's model predicts that $\beta = 0.5$ is the optimum.

From measurements it has been shown that a β closer to 1, where the loop gain approaches 0 dB is the optimum [2]. This is due to nonlinear time-variant upconversion of noise that is not well described by linear time-invariant models [2].

Phase noise far from the carrier is well predicted from linear, time invariant models, since the flicker noise affects the near carrier phase noise more than the phase noise far from the carrier [2]. Hence the time-invariant models will be used for this work. These models agree that in order to achieve low phase noise the power and Q needs to be as large as possible.

2.5.4 Oscillator phase error

If an oscillator has a non ideal phase criterion at the resonance frequency of the resonator

$$\underline{/\Gamma_{\text{amplifier}}(\omega_0)\Gamma_{\text{resonator}}(\omega_0)} = \phi \tag{2.25}$$

the oscillator will oscillate, except the actual oscillation frequency (ω) and the resonance frequency (ω_0) will differ, since it will oscillate at

$$\underline{/\Gamma_{\text{amplifier}}(\omega)\Gamma_{\text{resonator}}(\omega)} = 0 \tag{2.26}$$

and not at the resonance frequency of the resonator. It has been shown that the phase noise will be degraded proportional to the phase offset from the ideal phase criteria for a feedback oscillator [12].

$$\mathcal{L}(f_m, \phi) \propto \frac{\mathcal{L}(f_m, \phi = 0)}{\cos^4(\phi)} \tag{2.27}$$

This behaviour can be interpreted as the effective Q factor for the resonator is lowered when there is a phase error, since the phase slope of the impedance is lower at the actual oscillation frequency, as explained in Equation 2.11.

3
Transistor Modelling

The aim of the thesis is to create an reflection type oscillator. The GaN technology that will be used for the oscillator design, WIN-NP15, does not have a three-port transistor model. The supplied transistor model always has a grounded source. WIN-NP15 is a power amplifier technology, and thus there typically is no need to have components connected to the source. For a reflection amplifier, the wanted topology requires an RLC network on the source which will be discussed in Chapter 4. Because of this, the two-port transistor model needs to be converted into a full three port transistor model before the design could start. This three port model will use the Angelov transistor model [13].

To model a transistor, measurement data is necessary to verify that the model agrees with the measured performance. Neither measurement data nor transistors that could be measured were available for this modelling. Thus the implemented Angelov model is based on WIN's supplied transistor models in their ADS design kit. This is not an ideal solution as it introduces more modelling errors.

WIN's transistor model has inaccuracies in the order of a couple percent compared to WIN's measurements. And the measurements have an unavoidable measurement inaccuracy that is method and equipment limited. The implemented Angelov model will also have inaccuracies, and thus the total uncertainty of the model is increased. The transistor to be modelled is a two finger (two transistors in parallel), 150 nm gate length (l), 50 µm gate width (W) GaN HEMT. A two finger transistor will be used to remove as few vias as possible from WIN's model.

A 2 finger 200 µm gate width transistor was modelled at first, but WIN updated their design kit just after the first transistor model was finished. The updated design kit did not allow this size of transistor to be manufactured. Thus the transistor modelling had to start over with the smaller 2 finger 50 µm gate width transistor that is used in this thesis.

3.1 The Angelov transistor model

The Angelov model is an empirical transistor model based on tanh functions to describe transistor behaviour [13]. This thesis will use the version of the model that is implemented in ADS 2019 v1.0. The transistor equivalent circuit schematic is shown in Figure 3.1.

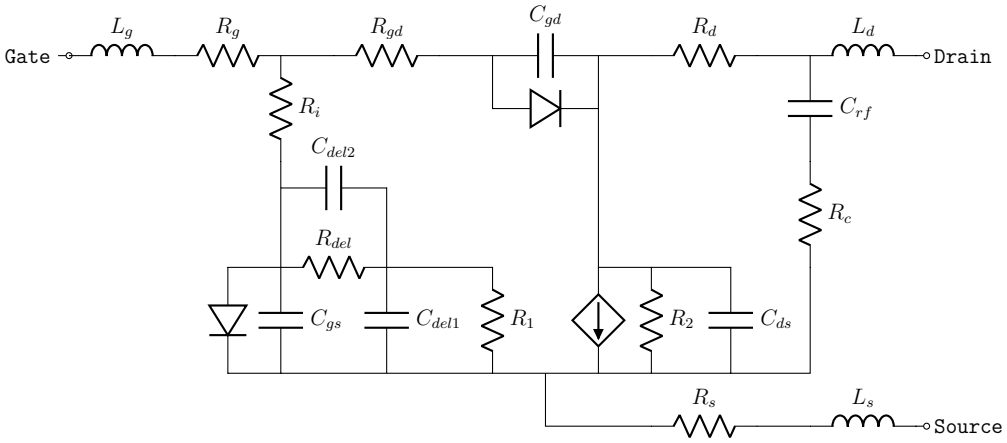

Figure 3.1: Angelov GaN HEMT equivalent circuit model. Subscript $_{del}$ denotes dispersion modelling components, R_c and C_{rf} model the frequency dependent output conductance. R_1 and R_2 are a part of ADS voltage controlled current source component.

To simulate the WIN model and create an equivalent Angelov model the setup described in Figure 3.2 was used, where the DC-parameters, S-parameters and noise performance was simulated in ADS. The model required a shift in reference plane, so transmission lines were added to compensate for this in the Angelov model. Since the source was grounded in WIN's model, no information regarding the reference plane on the source could be determined. This might be a source of deviation between the simulated performance and the actual transistor performance. 10 MΩ resistors were added between the gate and the drain and between the gate and the source to make the model converge a bit easier. This can be seen in Figure 3.3.

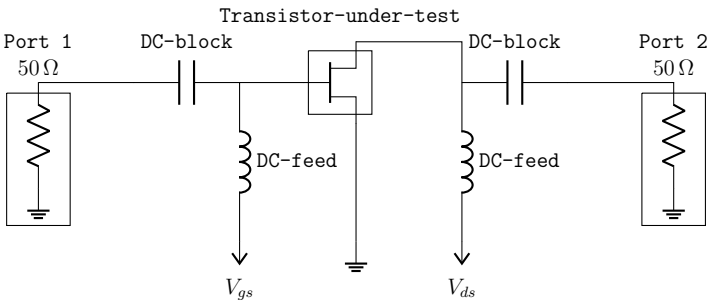

Figure 3.2: DC-parameter and S-parameter simulation setup to extract transistor parameters. Ideal DC-blocks and DC-feeds were used in ADS. For the noise modelling a Harmonic Balance simulation was performed with port 1 replaced with a P1tone component.

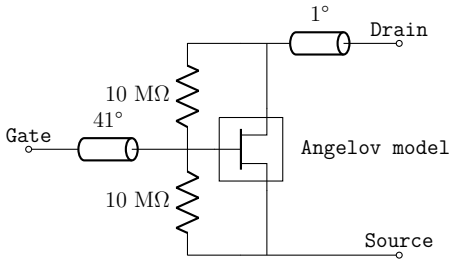

Figure 3.3: Final transistor model with shifted reference planes. The electrical lengths are at 13 GHz. The source reference plane is not changed since no information about it could be obtained from WIN's two-port grounded source transistor model.

3.2 Extraction of on resistance

To start the parameter extraction, the on and off resistance will be simulated. This is the ability for the gate voltage V_{gs} to control the channel resistance, $R_{channel}$. This is done by having a small, constant V_{ds} in the linear region, and sweeping V_{gs} [14]. For this simulation $V_{ds} = 1\,\mathrm{V}$ and V_{gs} was varied from $-3\,\mathrm{V}$ to $1\,\mathrm{V}$.

$$R_{ds} = \frac{V_{ds}}{I_{ds}} = R_d + R_{channel} + R_s \tag{3.1}$$

A simulation of the on and off resistance can be seen in Figure 3.4.

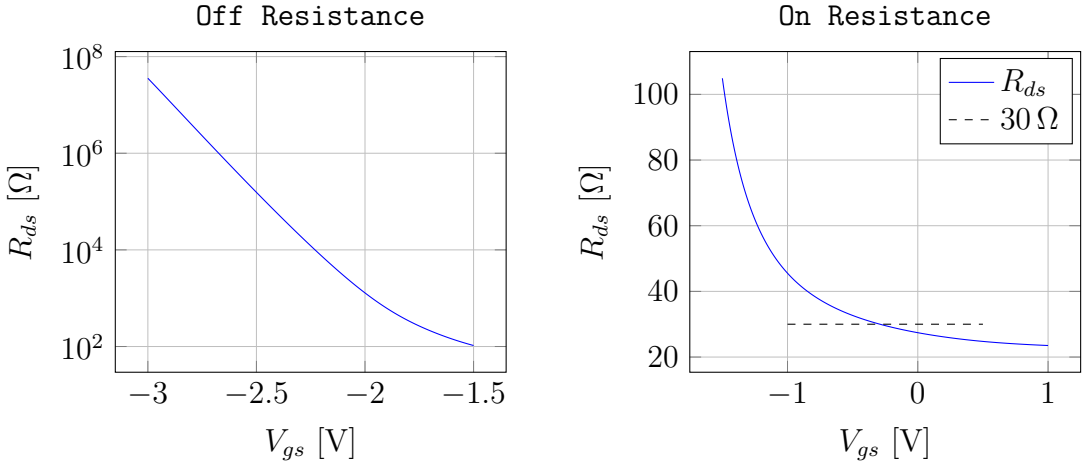

Figure 3.4: On and off resistance simulation. This transistor turns on at around $V_{gs} = -1\,\mathrm{V}$. The transistor will be used between $-1\,\mathrm{V}$ and $0.5\,\mathrm{V}$ so that range is used for the on resistance measurement. Above $V_{gs} = 1\,\mathrm{V}$ the transistor starts to have a rapidly increasing gate current.

When the gate is positioned symmetrically in the middle of the source and the drain, which is the case for the WIN-NP15 process, the following approximation can be used.

$$R_s \approx R_d \approx R_{channel} \approx \frac{R_{ds-ON}}{3} = \frac{30\,\Omega}{3} = 10\,\Omega \tag{3.2}$$

3.3 Gate current parameter extraction

Approximate values for V_{jg} and I_j can be extracted directly from an I_{gs} simulation, which is shown in Figure 3.5. V_{jg} is the threshold voltage for the gate current, and $V_{jg} = 0.9\,\mathrm{V}$ is the default value. I_j is the gate current at V_{jg}, $I_j = I_{gs}(V = V_{jg})$ [14].

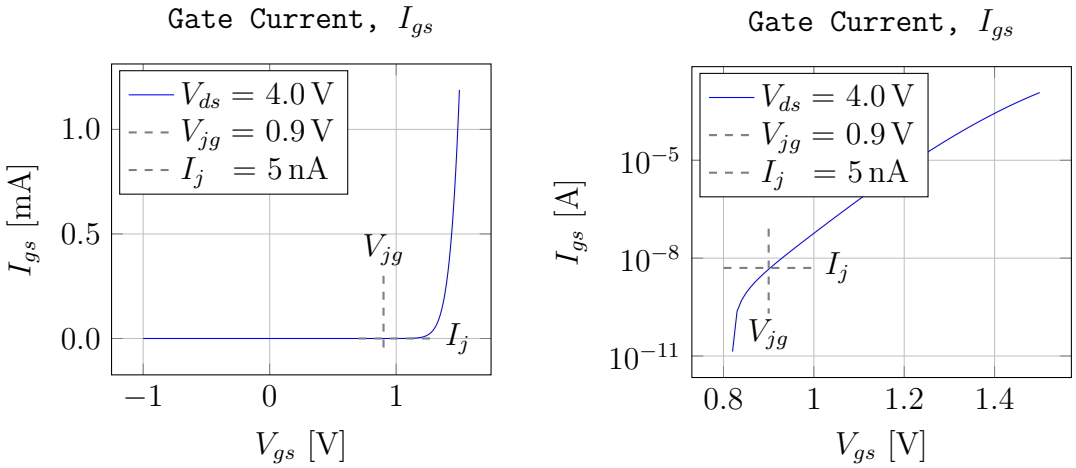

Figure 3.5: Gate current simulation. Above V_{jg} the gate has a rapidly increasing current so when operating the transistor $V_{gs} < V_{jg}$ is preferred.

P_g is a fitting parameter that together with Ne, the schottky diode ideality factor, describes the slope of the current I_g. $P_g(N_e)$ is a function of N_e so only one of the parameters is needs to be determined. $P_G = 18$ will be used as a starting value for the parameter optimization.

3.4 Drain characteristics parameter extraction

The drain-source current is complicated to model, since it depends on several different physical phenomena at the same time [14]. The negative slope of the drain current for high V_{ds} and high V_{gs} is caused by self heating and will be considered later in the thermal modelling. The extraction of α_r, α_s and λ is shown in Figure 3.6.

α_r can be determined from the slope of the drain characteristics (I_{ds} versus V_{ds}) at $V_{ds} = V_{knee}$, where the linear region and the saturated region meet at low V_{gs} [14]. α_s can be determined from the slope of the drain characteristics at $V_{ds} = V_{knee}$, at high V_{gs} so the drain current is large [14]. λ can be determined from the slope of the drain characteristics at high V_{ds}, in the saturated region, and low V_{gs} so there are less self-heating effects [14].

$$\alpha_r \approx \frac{\partial I_{ds}}{I_{ds}\partial V_{ds}} \qquad \alpha_s, \approx \frac{\partial I_{ds}}{I_{ds}\partial V_{ds}} \qquad \lambda \approx \frac{\partial I_{ds}}{I_{ds}\partial V_{ds}} \tag{3.3}$$

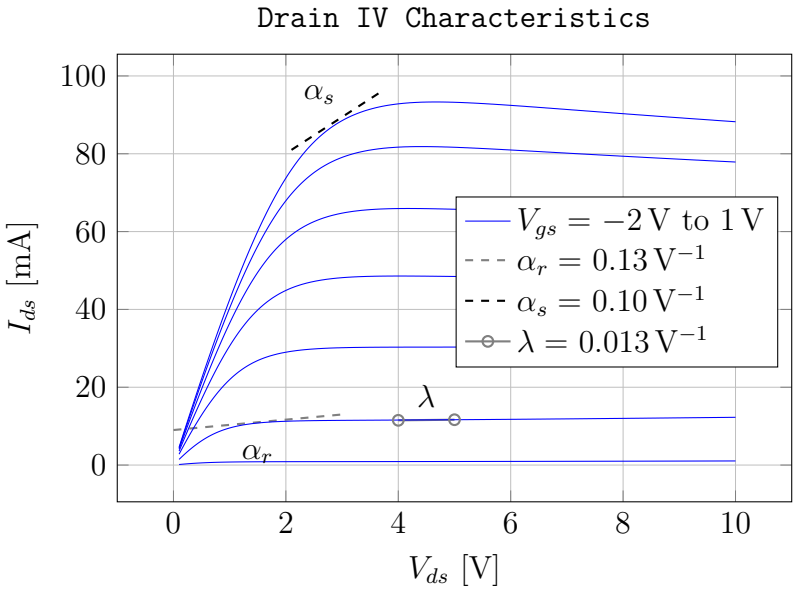

Figure 3.6: I_{ds} versus V_{ds} characteristics of WIN's transistor model. How to derive α_r, α_s and λ from this graph is shown in Equation 3.3

3.5 Transfer characteristics parameter extraction

The transconductance, $g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$, describes the transfer characteristics of the transistor. The transconductance is shown in Figure 3.7. When g_m is simulated, there are several discontinuities in the data. g_m is discontinuous around $V_{gs} = 0$. The I_{ds} model implemented in WIN's transistor model is not a smooth function but is instead split into two cases, $V_{gs} > 0$ and $V_{gs} < 0$. The drain current characteristics of WIN's transistor model is shown in Figure 3.8

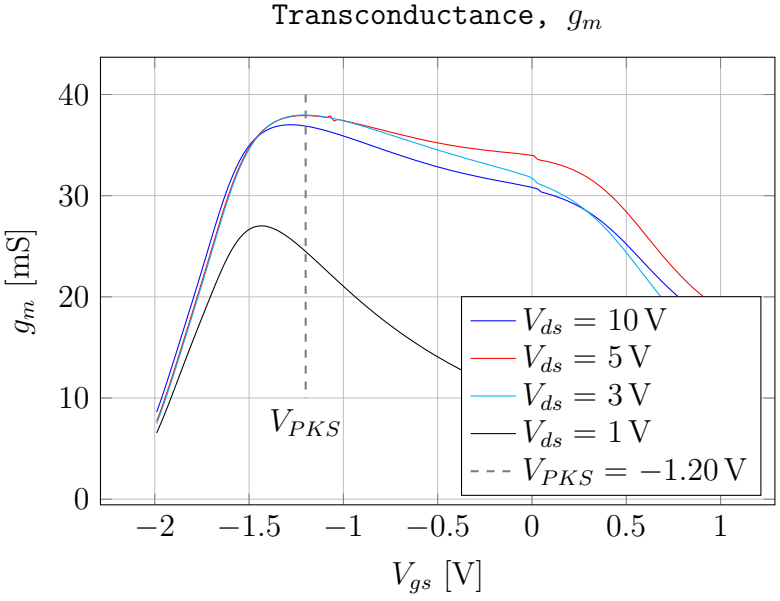

Figure 3.7: Transconductance characteristics of WIN's transistor model. Notice the discontinuity at $V_{gs} = 0\,\mathrm{V}$ and at $V_{gs} = -1.1\,\mathrm{V}$. The I_{ds} implementation in WIN's model is not a smooth function and is split into two cases, $V_{gs} > 0$ and $V_{gs} < 0$. V_{PKS} is the gate voltage for the highest g_m.

The Angelov model uses a bell-curve shaped g_m with its maximum at V_{PKS} [14] which results in the saturation current $I_{dss} \approx 2I_{pk0}$. Since the measured transconductance does not have the shape of a bell-curve, the extracted parameters will likely change during the IV optimization. $\Delta V_{pks} = 0.3$. The unsaturated coefficients for P_1 and P_2, $B_1 = 0.3$ and $B_2 = 3.0$ use the default values for GaN and will be used as the starting values for the IV optimization [14].

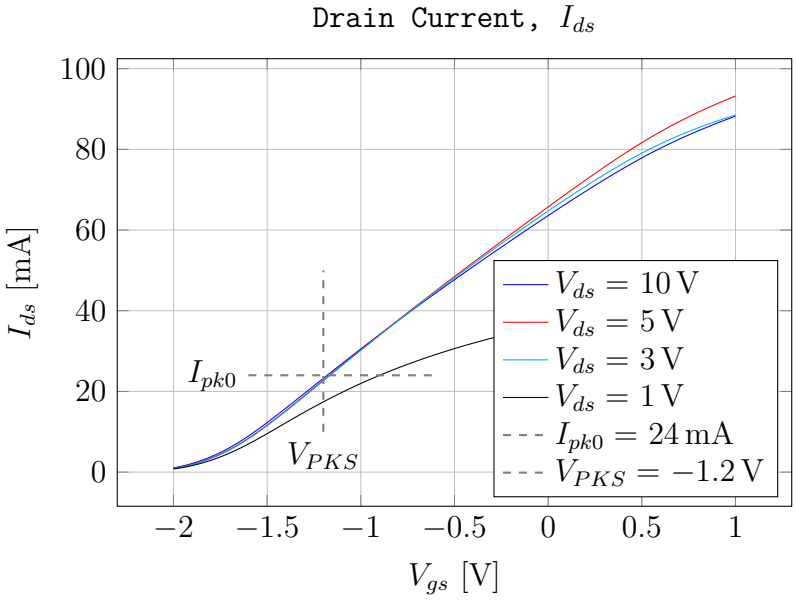

Figure 3.8: I_{ds} vs V_{gs} characteristics of WIN's transistor model. According to the Angelov model, I_{pk0} should be close to $\frac{I_{dss}}{2}$ which is not the case in this simulation. This caused some problems with the P_1 extraction.

3.6 Extraction of second derivative and third derivative parameters

P_1, P_2 and P_3 are polynomial coefficients to model the channel current [14]. To determine if these coefficients are necessary the function Ψ_1 is used to test how good the drain current model fits the data [14]. If the model is accurate, Ψ_1 will be a straight line with its derivative equal P_1. Ψ_1 for GaN is [14]

$$\Psi_1 = \operatorname{arcsinh}\left(\operatorname{arctanh}\left(\frac{I_{ds}}{I_{pk0}} - 1\right)\right) \tag{3.4}$$

Ψ_1 was then fitted to a third order polynomial, which is shown in Equation 3.5. Since the function arctanh(x) is defined for the domain of -1 to 1, $I_{pk0} \leq \frac{I_{dss}}{2} = 47\,\mathrm{mA}$ was required to get real valued coefficients.

Both Ψ_1 and Equation 3.5 are plotted in Figure 3.9. For this step $P_1 = 1.21$, $P_2 = -0.316$ and $P_3 = 0.133$ will be used as starting values for the optimization.

$$\Psi_1 \approx -0.541 + 0.972(V_{gs} - V_{pks}) - 0.316(V_{gs} - V_{pks})^2 + 0.133(V_{gs} - V_{pks})^3 \tag{3.5}$$

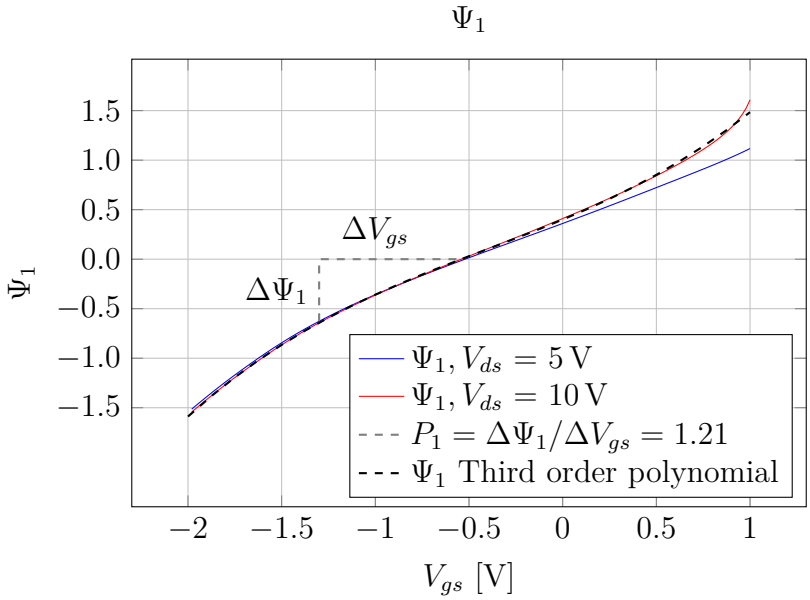

Figure 3.9: Graph of simulated Ψ_1 and Equation 3.5. $V_{ds} = 5\,\mathrm{V}$ were used as the basis for the derivative extractions since that is in the middle of the voltage span used for the modelling.

3.7 Thermal resistance fit

In a transistor, most physical effects have a temperature dependence. To model the self-heating, it is common to use thermal resistance and thermal capacitance to model the power flow similar to current flow through a circuit. The thermal resistance, $R_{th} = 85\,\mathrm{K/W}$, is given by WIN's models together with the thermal capacitance, $C_{th} = 590\,\mathrm{nWs/K}$, so these values are used as starting values for the optimization. All other temperature coefficients used the default values as a starting point for the optimization. How to extract the temperature behaviour is described in [14].

3.8 IV characteristic optimization

The model settings for the IV optimization are `Idsmod` = 1, `Igmod` = 0. The parameters where tuned and optimized to give an accurate IV fit. Since this is not the last step of the modelling process, the final IV curves are presented in Figure 3.10, 3.11, 3.12 and 3.13 instead of the ones derived during this stage of the modelling. The model agreement is not that good since the noise performance and RF performance were prioritized over the IV performance. The internal resistances in the Angelov model are too high.

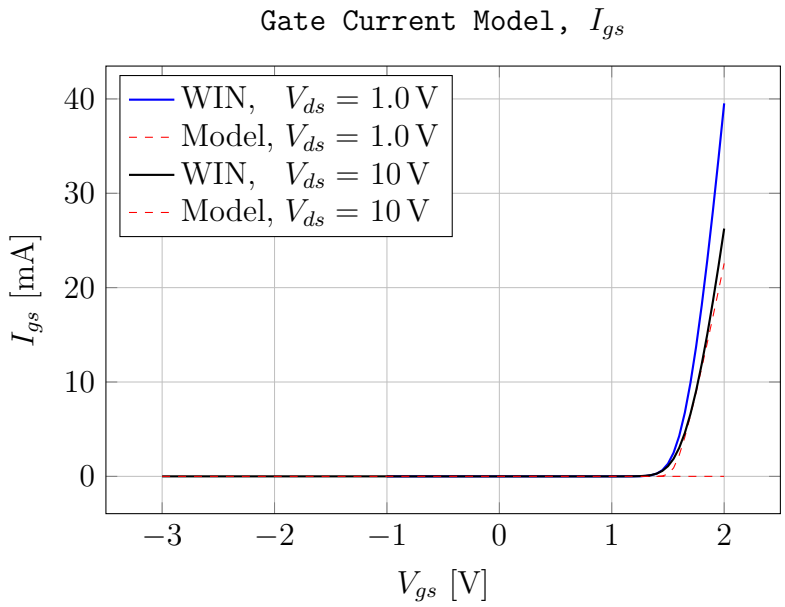

Figure 3.10: Gate current characteristics of the modelled transistor. The transistor will not be operated above $V_{gs} = 1\,\mathrm{V}$ since it has a breakdown at around 1.2 V to 1.4 V. For $V_{gs} \ll V_{ds}$ the gate current is small and negative for the model.

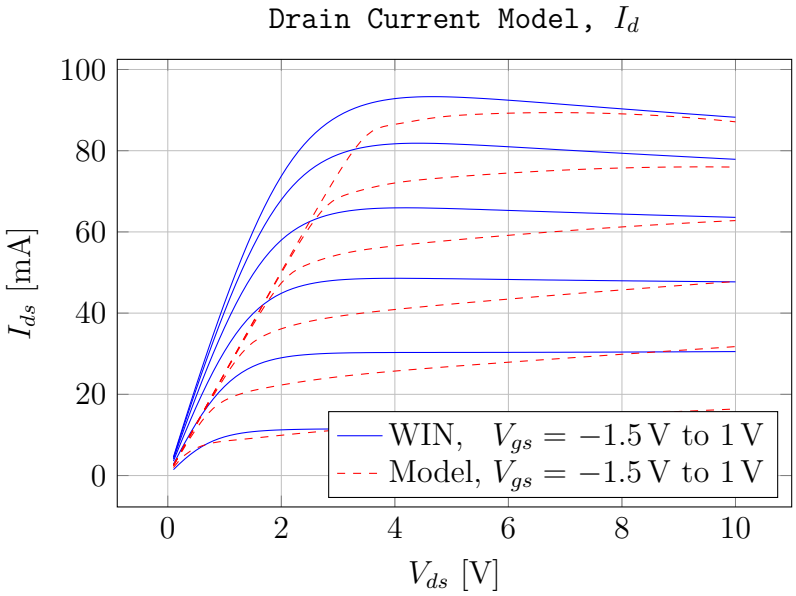

Figure 3.11: The output IV characteristics of the modelled transistor. The internal resistances are high, which cause sharp knee and lower slope in the resistive region, in order to better fit the thermal noise which will be explained more in Section 3.11.

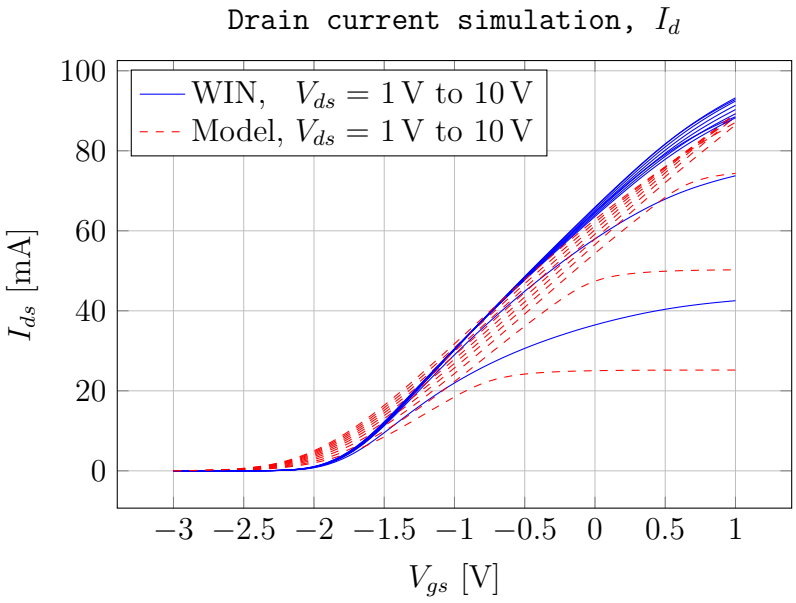

Figure 3.12: The transfer IV characteristics of the modelled transistor. The internal resistances are high, which reduce the slope of the IV curve, in the same way as in Figure 3.11.

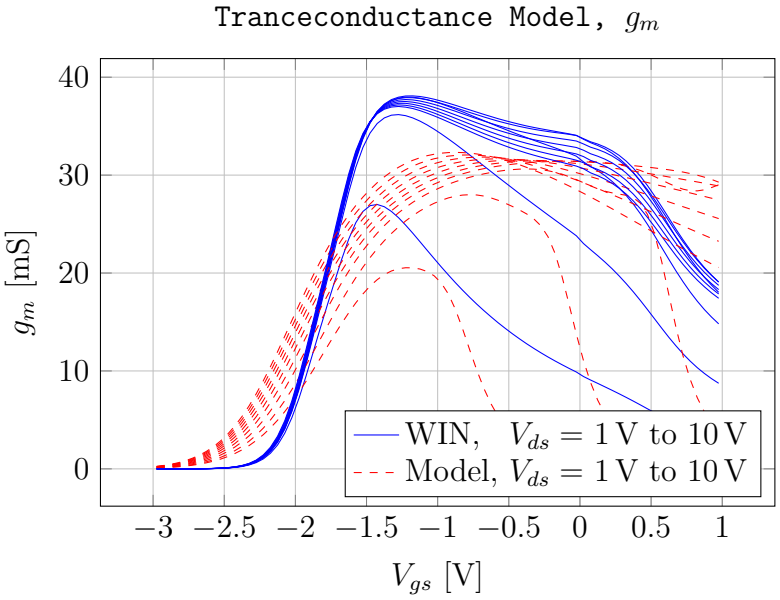

Figure 3.13: The transconductance characteristics of the modelled transistor. The internal resistances are high, which lower g_m.

3.9 Nonlinear capacitance and intrinsic parameter extraction

After the IV characteristics have been optimized and fitted to WIN's model, the values of the nonlinear capacitance and intrinsic parameters in the model need to be derived. The capacitance model `Capmod` = 2 is used, which is a bias dependent charge type model implementation [14], based on the equality in Equation 3.6.

$$\frac{\partial C_{gs}}{\partial V_{gd}} = \frac{\partial C_{gd}}{\partial V_{gs}} \tag{3.6}$$

For a symmetrical device like the one that is modelled, the nonlinear capacitance parameters are $P_{11} = P_{41}$, $P_{10} = P_{40}$, $P_{20} = P_{30}$ and $P_{21} = P_{31}$. The following values were used as starting points for nonlinear capacitance parameters, $P_{10} = -V_{pks}/P_1$, $P_{11} = P_1$, $P_{20} = 0.1$ and $P_{21} = \alpha_s$ [14].

3.10 S-parameter optimization

All parameters extracted so far were optimized to achieve similar performance as WIN's transistor model. The final small signal model can be seen in Figure 3.14. The starting point for the parameter values for the capacitance parameters, resistance parameters, inductance parameters and dispersion parameters were values found for a similar GaN HEMT in an example in [14]. The thermal resistance was kept higher than the earlier extracted value, as an attempt to predict the change in thermal performance that comes from moving the source vias. The final parameter values for the model are presented in Appendix A.

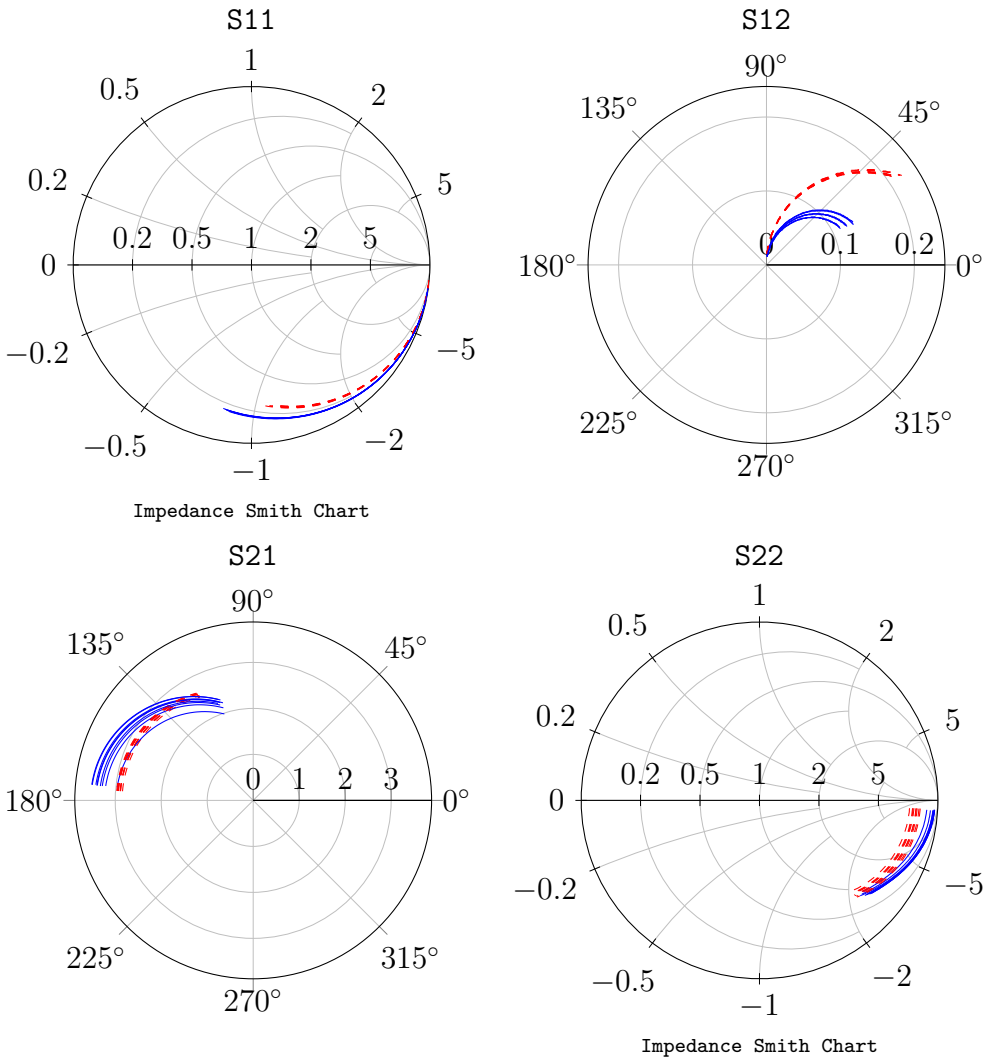

Figure 3.14: The final S-parameters of the transistor. Red traces are the implemented Angelov model and blue are the WIN model. The frequency is swept from 1 GHz to 16 GHz, V_{gs} is between −0.75 V and −0.25 V and V_{ds} is between 4.0 V and 6.0 V. For S_{22} and S_{12} the output resistance is too high for the Angelov model compared to WIN's model. The high resistances were necessary to achieve at better noise model fit.

3.11 Noise modelling

The noise of the transistor was modelled using the model parameter `Noimod` = 0, which uses the noise parameters described in Table A.10 in Appendix A. WIN's transistor model had large amounts of low frequency noise (LFN), which was difficult to model accurately using the Angelov model. Most difficult to fit was the thermal noise floor. Since it scales inversely proportional to the internal resistances, the internal resistances were increased to a point which ruined the IV fit. The thermal noise power is described by [14]

$$\frac{< i^2 >}{\Delta f} = \frac{4kT}{R} \ [\mathrm{A}^2/\mathrm{Hz}]. \tag{3.7}$$

So by increasing all internal resistances, the noise at a large offset was reduced. The final noise model can be seen in Figure 3.15.

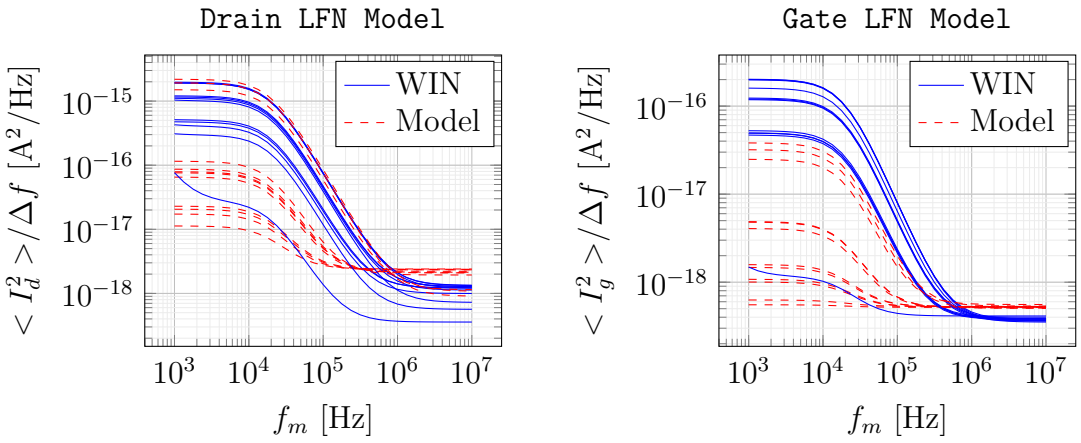

Figure 3.15: Low frequency noise simulation. WIN's transistor model has large amounts of noise. V_{gs} is varied between -1 V to -0.2 V and V_{ds} is varied between 2 V to 6 V. The noise at offsets larger than 1 MHz is lower for WIN's model compared to the implemented Angelov model. The drain current is much larger than the gate current and therefore causes more noise.

4

Oscillator Design

For the oscillator to be used in a system, it is important that it is phase locked to prevent frequency drift. The phase locking is handled by a Phase-locked-loop (PLL), which is a control loop that regulates the frequency of the oscillator by comparing it to a very frequency-stable crystal oscillator. Since the resonators are mechanically tuneable, they provide the large scale frequency tuning. The PLL requires much faster frequency control than what the cavity can provide, so some kind of small-scale fast voltage controlled frequency tuning is necessary. A varactor based frequency shifter will be implemented in the phase shifting network, to enable fast voltage-controlled tuning of the oscillation frequency.

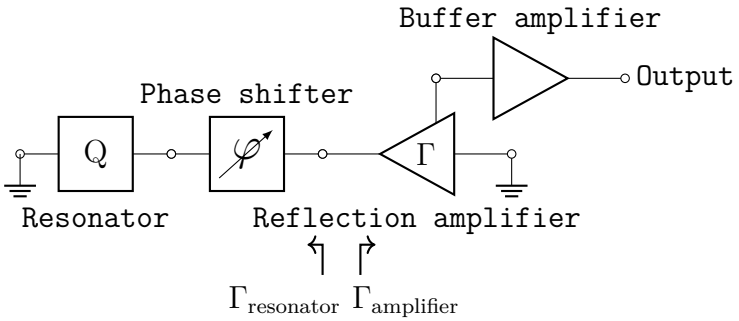

Figure 4.1: Block schematic of the designed oscillators. A buffer amplifier is connected to the source of the reflection amplifier in order to extract the signal from the oscillator.

In this Chapter, the design of the different components required for a complete oscillator will be discussed. The off-chip resonators that will be used are described in Section 4.1. The reflection amplifier design is presented in Section 4.2. The phase shifter design is presented in Section 4.3. Both oscillators will have the same block diagram, which is shown in Figure 4.1. $\Gamma_{\text{amplifier}}$ is the reflection coefficient looking towards the reflection amplifier and $\Gamma_{\text{resonator}}$ is the reflection coefficient looking towards the phase shifter and resonator connected together.

4.1 Resonator model

The resonators that will be utilized for the oscillators are two different size mechanically tunable cavity resonators [1]. They have already been designed, outside the scope of this thesis, and will not be changed in any way during the design process.

An image of the resonator with and without its cover can be seen in Figure 4.2. By moving the external screw, the resonant frequency of the resonator is tuned. A probe is lowered into the cavity in order to couple power to and from the resonator. The probe behaves as a capacitive connection to the resonator.

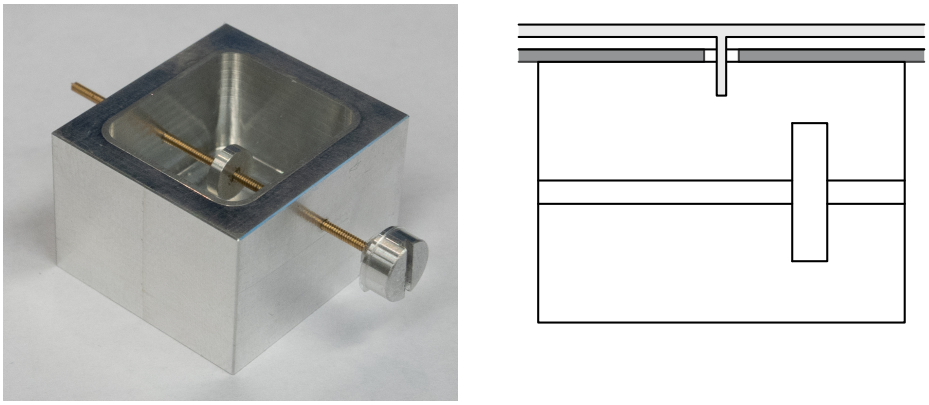

Figure 4.2: Images of the cavities. The two cavities look the same but have different internal dimensions. In the lid of the resonator is a probe which extends into the cavity. It couples the power in and out of the cavity. From [1]. Reproduced with permission.

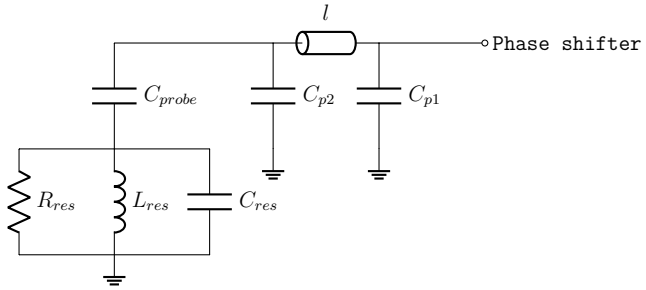

Figure 4.3: Equivalent circuit model for the tunable cavities. The cavities exhibit the behaviour of a parallel resonator at resonance. The model was extracted from EM-simulated S-parameters.

Both resonators are modelled with an equivalent circuit model, which can be seen in Figure 4.3, but with different component values. R_{res}, L_{res}, C_{res} and C_{probe} vary as a function of the tuning position of the cavity. The oscillator design used the equivalent resonator circuit models instead of simulated and extrapolated S-parameters in order to have less convergence problems during the Harmonic Balance

(HB) oscillator simulations. The unloaded quality factor of the two resonators are displayed in figure 4.4.

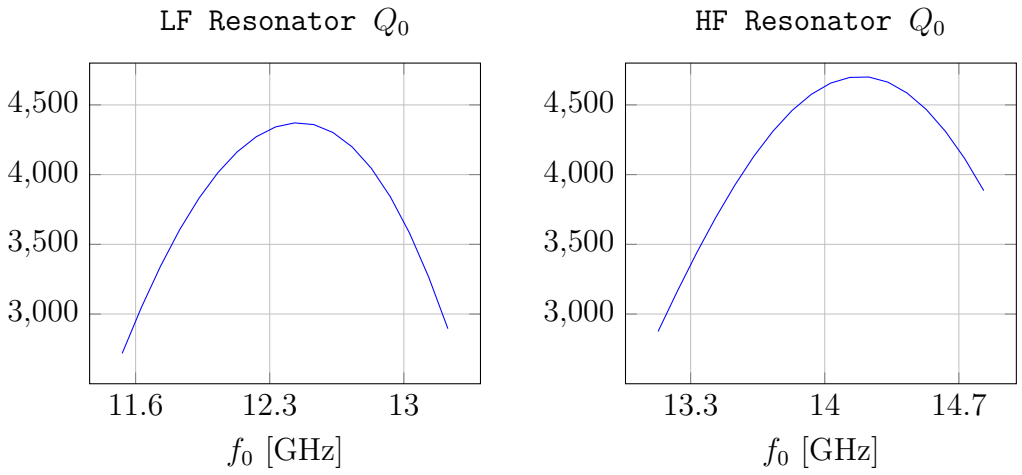

Figure 4.4: The unloaded quality factor for the LF and HF cavities as the resonator is tuned for different resonant frequencies. The Q_0 is lower at the limits of the mechanical tuning.

4.2 Reflection amplifier design

The reflection amplifier needs to be carefully designed. It needs enough gain to enable oscillation over the wanted frequency range, while not having too high gain, which causes the resonator to become too strongly coupled to the amplifier. To ensure that the amplifier together with the phase shifting network creates the optimal resonator coupling is of utmost importance for the oscillator phase noise performance [2]. Both amplifiers use the topology shown in Figure 4.5. This topology has been used to achieve low phase noise, with minor variations in [15, 16, 17, 18]. The amplifier uses the transistor modelled in Chapter 3.

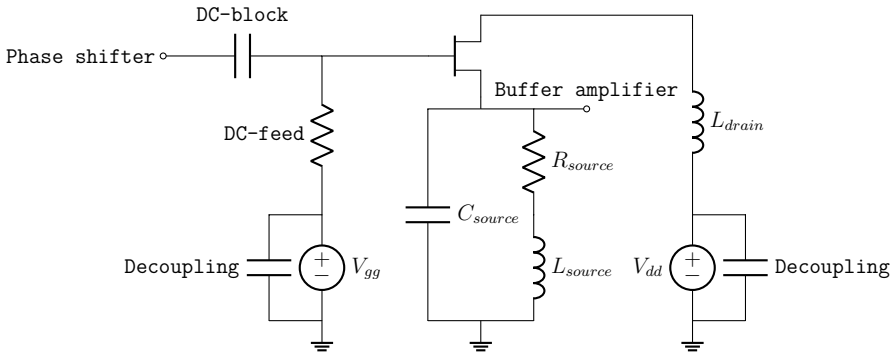

Figure 4.5: The reflection amplifier circuit schematic. The buffer amplifier is connected to the source of the main transistor in order to extract the signal from a node that a large amount of power, and where the buffer amplifier will only minorly affect the oscillation.

The drain is terminated inductively with L_{drain} to make the transistor unstable and create reflection gain at the gate. The value of L_{drain} is the inductance makes the transistor most unstable at the wanted peak gain frequency.

The RLC circuit connected to the source controls the shape and amplitude of the reflection gain. R_{source} and L_{source} controls the reflection gain amplitude and C_{source} controls both the shape and amplitude of the reflection gain. The drain was biased through L_{drain} and the gate was biased through a resistor, since the gate current is low. C_{source} is a small capacitor, less than 1 pF for both amplifiers. If less than four ground connecting vias were used, the reflection gain was strongly decreased, since the total behavior of the shunt capacitor turned inductive due to the via inductance. To change the capacitor to an open stub is a possible different design, which might have been beneficial. This problem could also have been solved by making C_{source} even smaller, but a smaller C_{source} would increase the risk of having parasitic capacitances dominate the source termination behaviour.

The reflection gain of the two amplifiers are presented in Figure 4.6.

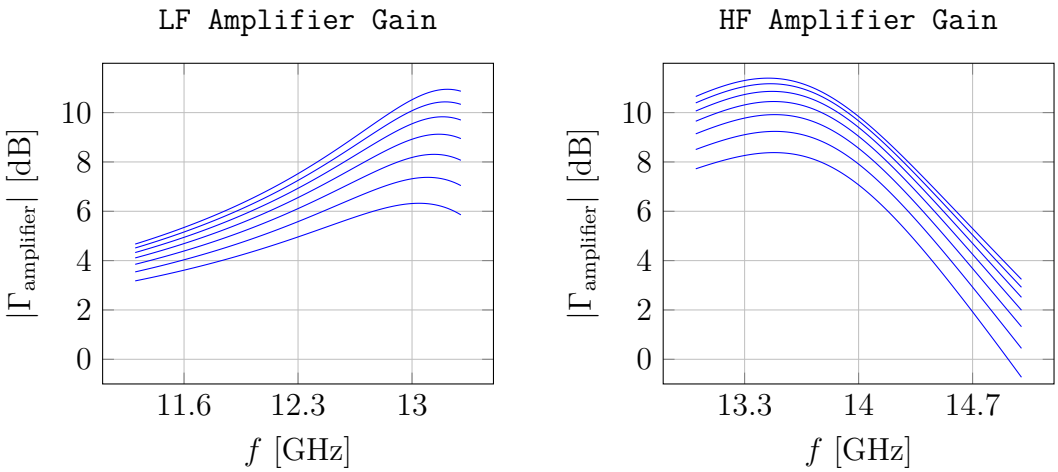

Figure 4.6: The reflection gain of both designed amplifiers. The gain can be controlled by changing the gate and drain bias. Simulated for $V_{dd} = 7.0\,\text{V}$ and V_{gg} from $-1.3\,\text{V}$ to $-0.1\,\text{V}$. The gain increases with increasing V_{gg}.

The phase of the reflection gain is presented in Figure 4.7. At the gain peak, the phase of the reflection has an inflection point, and the largest phase slope. Since the phase slope is largest at the peak and the phase behaviour is different depending on which side of the peak the oscillator operates, the gain peak is to be avoided. This makes it more difficult to design high bandwidth reflection amplifiers. The gain slope on the higher side of the gain peak was limited by parasitic capacitances in L_{drain} as the inductor approaches its self resonance frequency. To find this behaviour it is important to EM-simulate the inductor since the amplifier is sensitive to inductance variations and parasitic capacitances. Since the gain has a lesser slope at frequencies below the gain peak, having the gain peak at a higher frequency than the maximum wanted oscillation frequency was beneficial. The phase shift required for the phase shifter is dominated by the phase of the reflection amplifier. Thus the requirement on the LF phase shifter is less strict than for the HF phase shifter and the LF

oscillation frequency will be more easy to control.

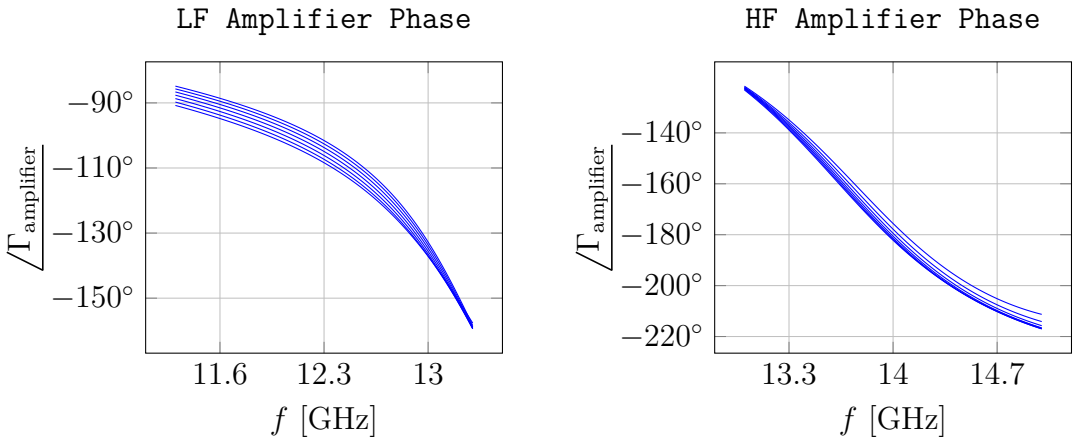

Figure 4.7: The phase of the reflection amplifiers for the same gate and drain bias as in Figure 4.6. The phase have different behaviour depending on if the gain peak is above or below the frequency band. Simulated for $V_{dd} = 7.0\,\text{V}$ and V_{gg} from $-1.3\,\text{V}$ to $-0.1\,\text{V}$.

The shunt decoupling capacitors were chosen as large as possible, to provide an efficient low impedance RF-ground. This is to prevent a feedback path through the DC supply as much as possible. The series DC blocking capacitors were also chosen as large as possible to have a low series impedance at RF.

4.3 Phase shifter design

Since two reflection amplifiers have been designed to provide enough reflection gain for oscillation to start, two phase shifting networks are designed to ensure that the oscillators phase condition, Equation 2.6, is fulfilled. The phase shifting networks also need to absorb all frequencies outside the resonance frequency of the resonator, to prevent oscillation at the wrong frequency. A single phase shifter that could span both LF and HF frequency bands were investigated, and deemed difficult to design. Two phase shifting networks were designed as an attempt to reach better phase noise performance since the phase noise degrades with phase error, as described in Equation 2.27.

The phase condition is fulfilled by a static phase shifter, that handles the majority of the phase shift, and a tunable phase shifter that fine-tune the phase. The phase shifter determines the oscillation frequency, where the the phase condition is fulfilled If the oscillator is to be used with a PLL, a tunable phase shifter is required in order to lock the oscillation frequency of the oscillator.

The LF and HF phase shifters use almost the same topology, which can be seen in Figure 4.8. The static phase shift is handled by transmission line l_1 and l_2. The total length of the transmission lines is the length that minimizes the phase error over the entire frequency range. It is important that the bondwire that will be used to connect the resonator is taken into account during simulations, as it is inductive

and will affect the total phase shift depending on its geometry.

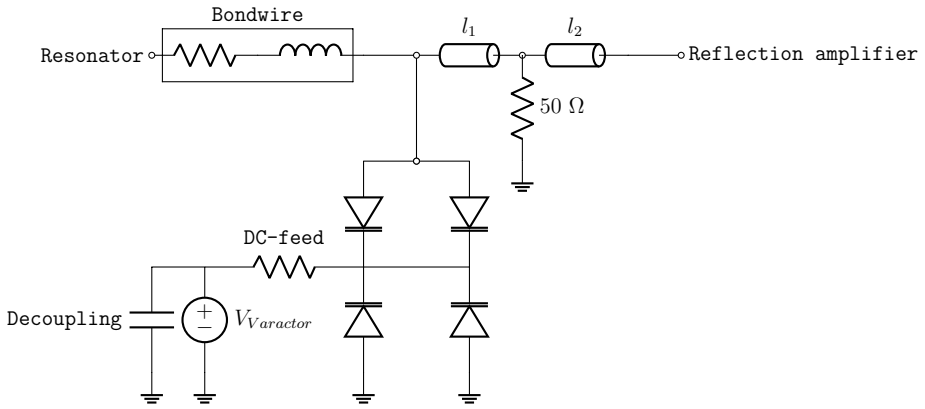

Figure 4.8: The phase shifter circuit schematic. The static phase shift is accomplished by l_1 and l_2. The bondwire, varactors and l_1 act as a quarter wave impedance transformers in order for the 50 Ω resistor to terminate all frequencies outside the resonant frequency of the resonator.

The bondwire, varactors and l_1 also act as a quarter wave impedance transformer to enable a 50 Ω shunt resistor to absorb all frequencies outside the resonance frequency. The LF phase shifter has more phase shift from l_2 after the termination in order to fulfil the phase criterion. The transmission line lengths that was used for the designs can be seen in Table 4.1. The total phase shift of the phase shifter depends on the varactor capacitance and the bondwire geometry.

Table 4.1: Transmission line lengths, and electrical length at 13 GHz

	l_1 [µm]	l_2 [µm]	l_1 [°]	l_2 [°]
LF	1540	910	66	39
HF	1340	0	57	0

The tunable small scale phase shift is provided using four varactors connected as close to the resonator as possible, using the topology described in Figure 4.8. The WIN NP15 design kit lacks a diode model to use as a varactor, so the modelled transistor had to be used as a varactor with the drain and the source shorted together. The negative voltage bias is applied to the gates in order to control the junction capacitance.

All tuning circuitry will cause distortion and modulation noise that will degrade phase noise [2]. This thesis uses two parallel anti-series varactors in order to reduce distortion and modulation noise [19]. The junction capacitance of a varactor depends nonlinearly on the reverse bias voltage [20]. Varactors typically have high losses, and thus a poor quality factor

$$Q_{\text{varactor}} = \frac{1}{\omega C_{total} R_{series}} \tag{4.1}$$

where C_{total} is the total varactor capacitance and R_{series} is the total series resistance of the varactors. The capacitance and quality factor is shown in Figure 4.9 as

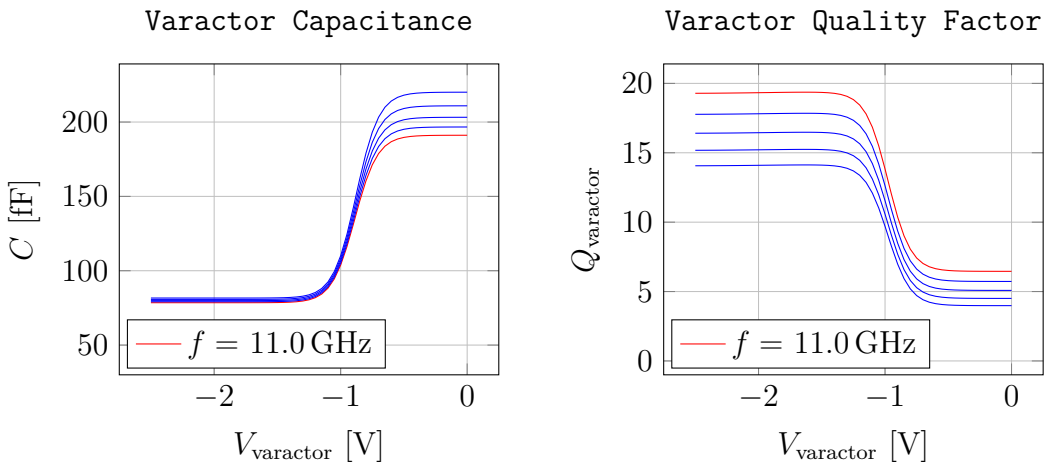

Figure 4.9: The CV characteristics and quality factor of the varactor implementation as a function of varactor bias. Both vary with frequency, so the frequency is simulated between 11.0 and 15.0 GHz

functions of the varactor bias. This poor Q_{varactor} will increase the losses and lower Q_0 for the phase shifter connected with the resonator. To achieve a wide tuning bandwidth, a low capacitance value and a high quality factor is required. The voltage handling of the varactor limits wide-band tuning. The voltage swing across the varactor increases with a stronger coupling to the resonator. The voltage level can exceed the reverse bias of the varactor, which degrades the quality factor [2].

For a wide band of oscillation frequencies, like in this work, more phase shift is typically required than what can be provided by a simple transmission line phase shifter. One method is to use several different phase shifters, and have transistors acting as switches to switch to the phase shifter that works best at each frequency [21]. A switch based phase shifter was not an option in this semiconductor technology, since WIN strongly recommends against using the NP15 technology for switches.

Figure 4.10 shows the resulting reflection coefficient ($\Gamma_{\text{resonator}}$) of the resonator connected with the phase shifter for both LF and HF oscillators. Red curves are the losses of the resonators at all resonant frequencies, i.e. at different cavity positions. The reflection amplifiers need to provide at least gain equal to $\Gamma_{\text{resonator}}$ to enable oscillation. The $50\,\Omega$ resistor absorbs power for frequencies outside the resonance, to suppress the non-resonance frequencies.

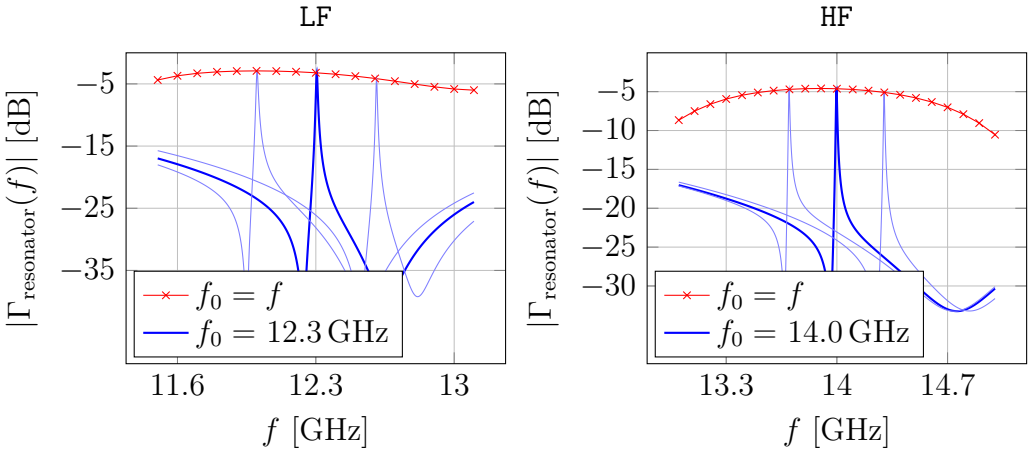

Figure 4.10: The reflection coefficient ($\Gamma_{\text{resonator}}$) of the resonators connected with phase shifters. The red curve is $|\Gamma_{\text{resonator}}(f = f_0)|$, the reflection from the resonator at resonance. while the thick blue curve is $|\Gamma_{\text{resonator}}|$ for a fixed cavity position with the resonance frequency 12.3 GHz and 14.0 GHz.

The designed phase shifter gives a phase shift of 15° to 25° over the entire frequency band when the varactor bias is varied, which is shown in Figure 4.11

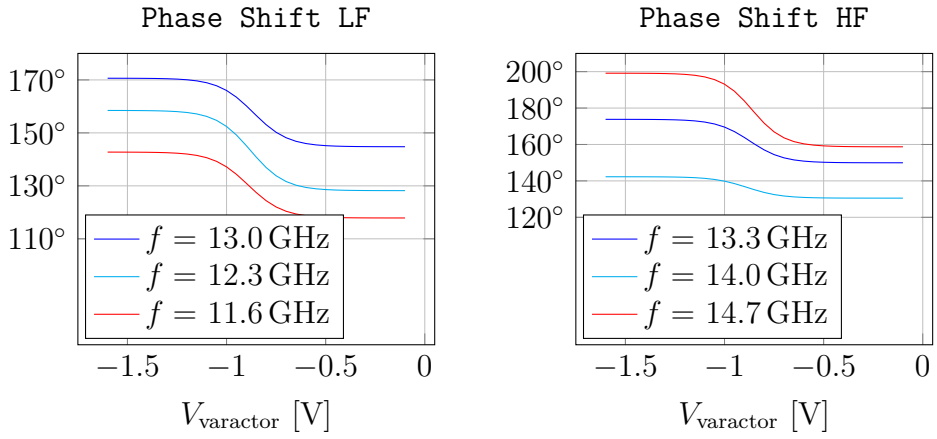

Figure 4.11: The possible phase shift for the phase shifter connected to the resonator. Between 15° and 25° phase shift is possible.

For all these simulations, the bondwire was simulated using the Philips-TU Delft Bondwire Model implemented in ADS [22]. A 500 µm long bondwire was deemed a reasonable size and used for simulations. In Figure 4.12, the extra phase shift introduced by changing the bond wire length is displayed. Approximately 10° phase shift variance can be expected. Since the varactor can control the phase to a greater extent, the oscillator is robust with respect to the bondwire length.

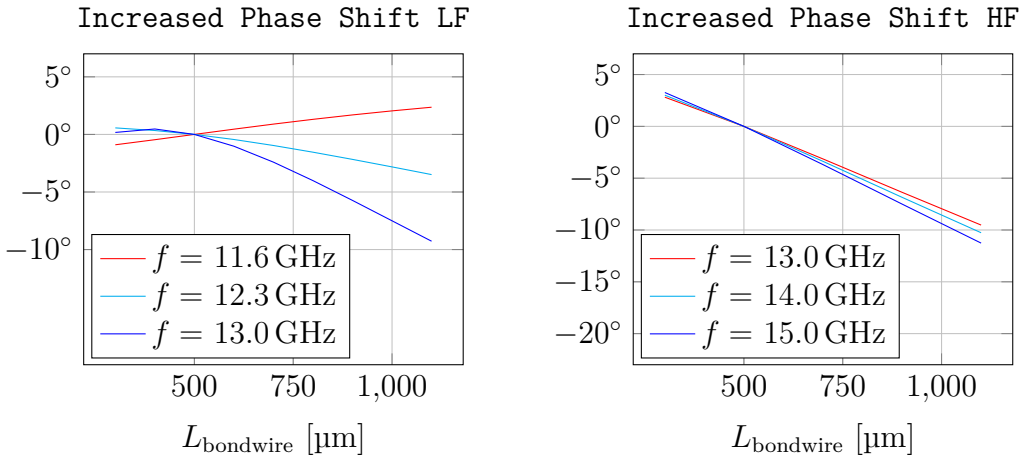

Figure 4.12: Extra phase shift introduced when the bondwire length is varied. The varactor is biased at −1.6 V

In Figure 4.13, the tuning sensitivity of the oscillator is displayed. The total tuning range is between 1.2 MHz and 4.8 MHz. A typical PLL has around 100 kHz bandwidth, so this tuning range should be enough phase lock the oscillator.

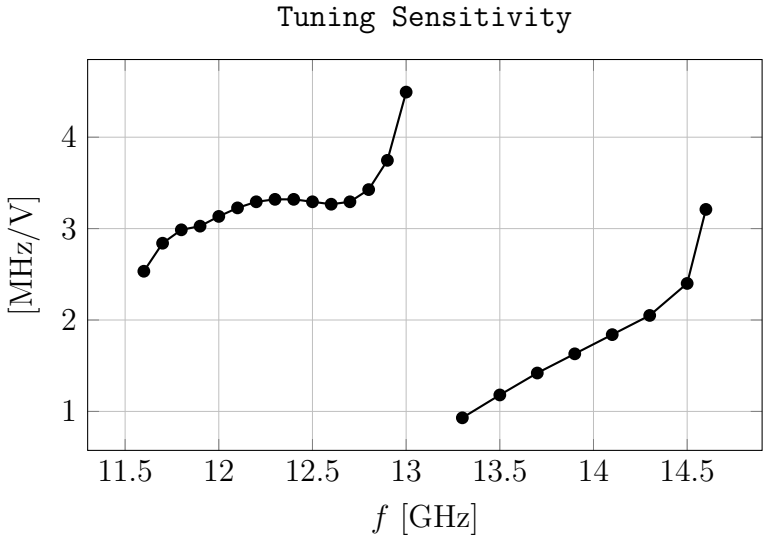

Figure 4.13: Tuning sensitivity of the final oscillator. The varactor bias is swept from 0.5 V to 1.2 V. The total tuning range is between 1.0 MHz and 4.5 MHz.

The Nyquist plot, $\Gamma_{\text{amplifier}}\Gamma_{\text{resonator}}$, is displayed in Figure 4.14 for varying varactor bias. As the varactor bias is varied, the resonance frequency changes. The Nyquist plot shows the small signal performance of the oscillator. When the oscillator is large signal simulated $\Gamma_{\text{amplifier}}\Gamma_{\text{resonator}}$ equals one due to gain compression.

The phase shift in the signal path does not degrade the Q-factor of the resonator [2]. A phase shift in the signal path may cause the phase condition to be fulfilled for a frequency where Q is not the maximum (the maximum phase slope of the impedance). This will degrade performance [2].

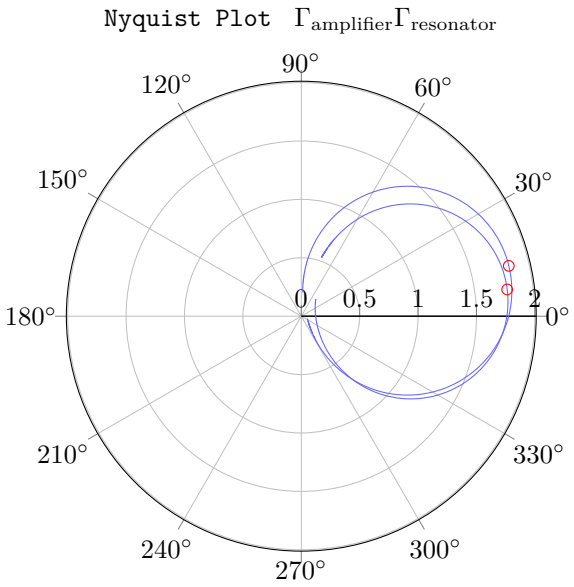

Figure 4.14: Nyquist plot for $f_0 = 13.8\,\text{GHz}$ using the varactor biased at $-1.6\,\text{V}$ and $-0.1\,\text{V}$. The phase shift is almost 10°, which corresponds to a frequency shift of 2.1 MHz.

Excessive phase shifting using this topology will limit the tuning bandwidth due to out of band oscillations. The impedance transforming transmission line will cause the $50\,\Omega$ termination to be less effective at suppressing frequencies far from the resonance frequency of the resonator, which can be seen at the edges of the frequency bands in Figure 4.10.

The reduction of Q_0 with variation of varactor bias for both LF and HF resonators are plotted in Figure 4.15. Q_0 is calculated using Equation 2.11, where $Z_{\text{resonator}}$ is the impedance looking into the phase shifter and resonator as shown in Figure 4.1. For the LF resonator Q_0 is degraded for all varactor biases and heavily degraded when the varactor is biased close to 0 V. For the HF resonator Q_0 is degraded less when the varactor is pinched-off, and heavily degraded when the varactor is biased close to 0 V. The only difference between the LF and HF phase shifter is the transmission line lengths. Thus the varactor is positioned in a way that affects the quality factor less for the HF phase shifter, even though the varactor has more loss at higher frequencies. A large Q reduction comes from the 50 ohm termination, it lowers Q with around 50% for the LF resonator and 25% for the HF resonator.

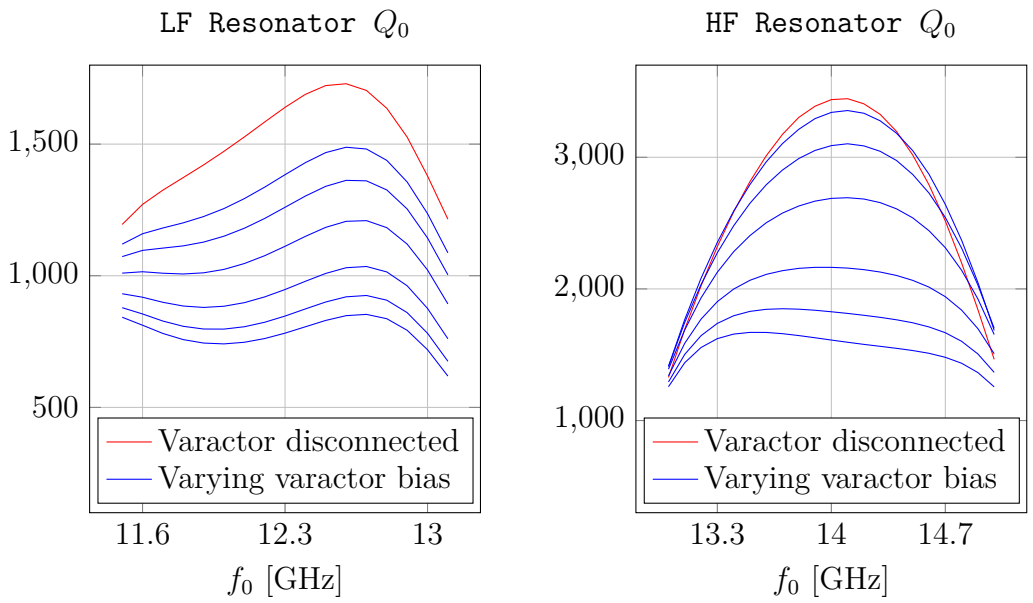

Figure 4.15: The Q_0 for the resonator (at resonance) together with the phase shifter and 50 Ω termination, when the varactor bias is varied. The main Q reduction comes from the 50 ohm termination.

4.4 Buffer amplifier design

The goal of the buffer amplifier is to isolate the load from the oscillator, while also providing a somewhat constant output power. To improve the isolation, a two stage transistor amplifier was designed. It needs to be able to isolate the output from the input while providing enough output power to meet the specifications. The buffer amplifier was designed with WIN's provided transistor model, since a grounded source topology is used for the buffer amplifier.

It is important that the input of the buffer amplifier is designed in a way that affects the reflection amplifier as little as possible, while still coupling as much power as possible from the oscillator in order to keep the phase noise floor low. The reverse transmission (S_{12}) needs to be as low as possible, so load variances affect the oscillator as little as possible. The gain needs controllable to make sure that the output power is constant even when the resonator power varies. The output needs to be matched to a 50 Ω characteristic impedance. With these design goals in mind, one buffer amplifier for both frequency bands were designed. Its circuit schematic is shown in Figure 4.16. It is important that the buffer amplifier is stable, and the result of the stability analysis is shown in Figure 4.17. The simulated S-parameters are shown in Figure 4.18. The gain (S_{21}) is lower for higher frequencies due the output inductor and the bondwire inductance. The output inductor is required to match the output.

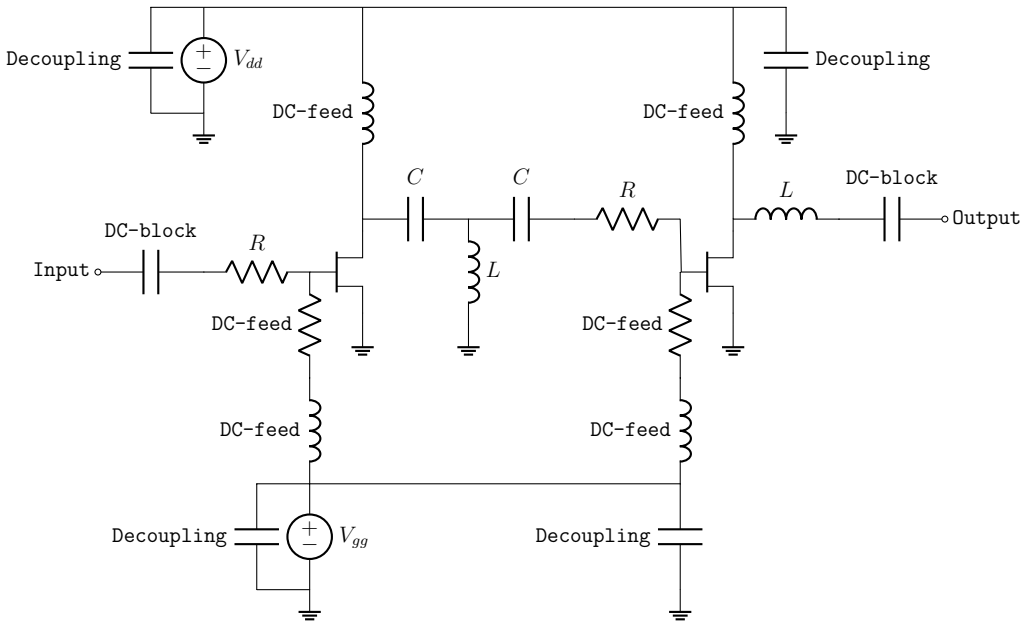

Figure 4.16: Schematic of buffer amplifier. The inter-stage matching network contains resistance to further stabilize the amplifier. The inductance at the output is for matching purposes.

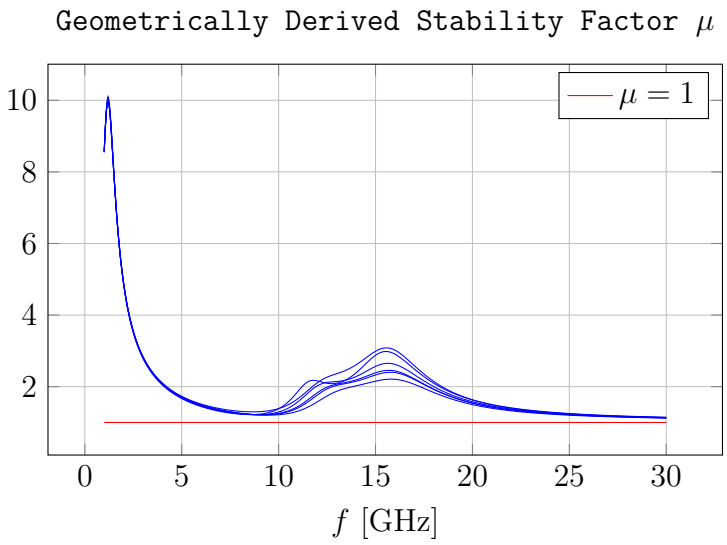

Figure 4.17: The buffer amplifier is unconditionally stable for all bias points up to the wanted maximum bias.

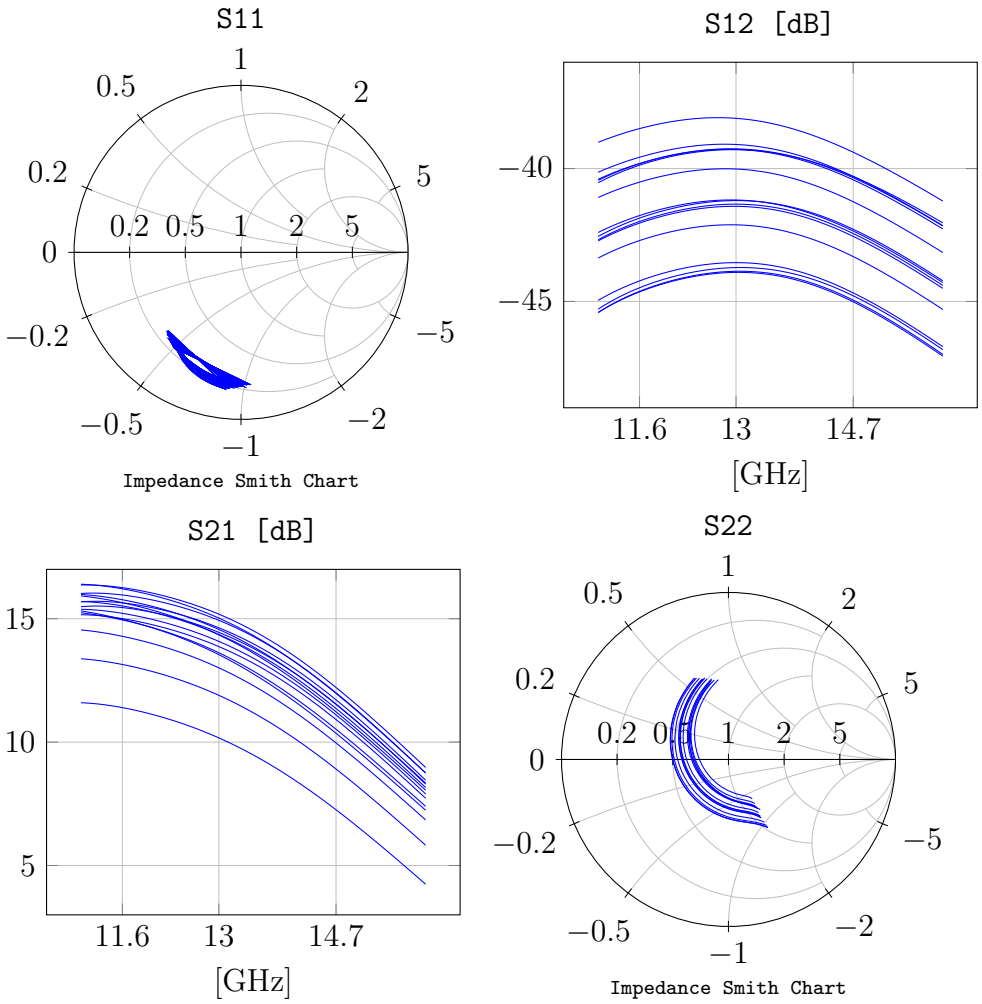

Figure 4.18: Buffer amplifier S-parameters for varying gate and drain bias. The gain is controllable to regulate the output power, while the isolation is good for all biases

4.5 Complete oscillator

A layout for each oscillator was created. Since the MMIC will be manufactured, a Design Rule Check (DRC) was required. The DC and RF pads were placed on separate sides to make it possible to test the circuit using probes.

The finished layout can be seen in Figure 4.19 for the LF oscillator and in Figure 4.20 for the HF oscillator. The DC-bias pad pitch is 200 µm and the RF pad pitch is 100 µm. All inductors were EM simulated for increased accuracy.

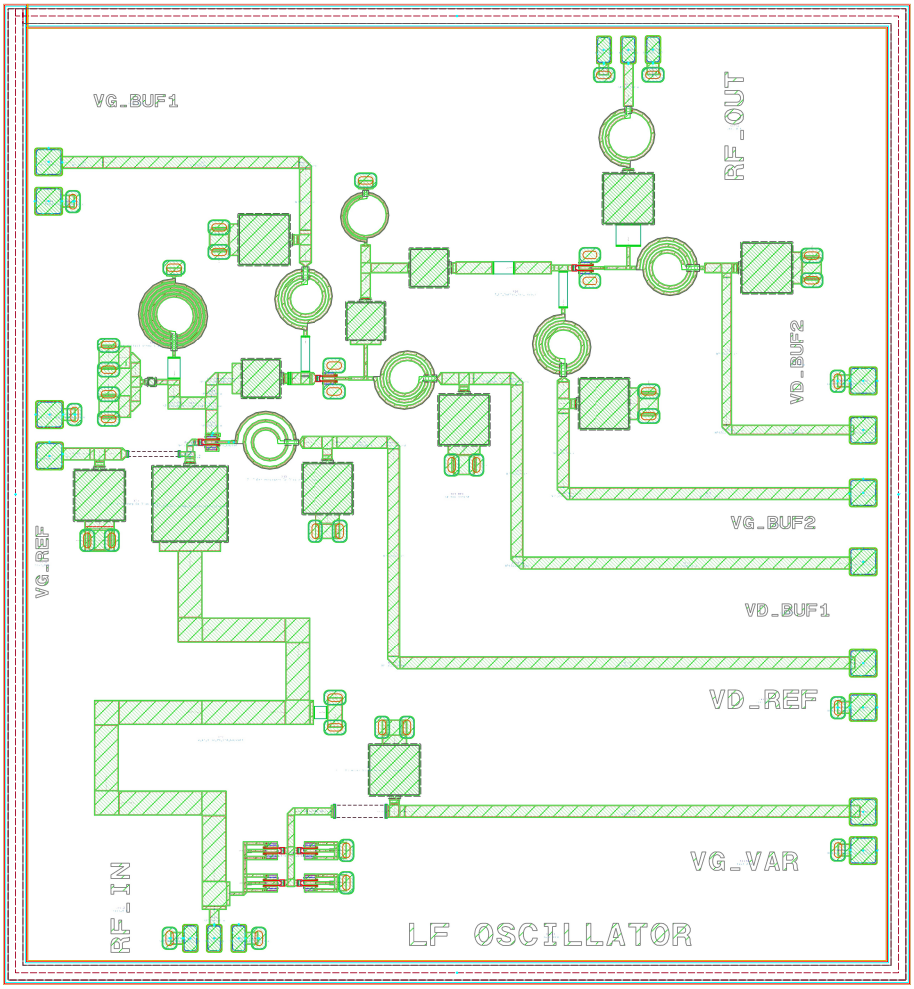

Figure 4.19: The layout of the entire LF oscillator. The size of the LF MMIC is 3.90 x 3.60 mm

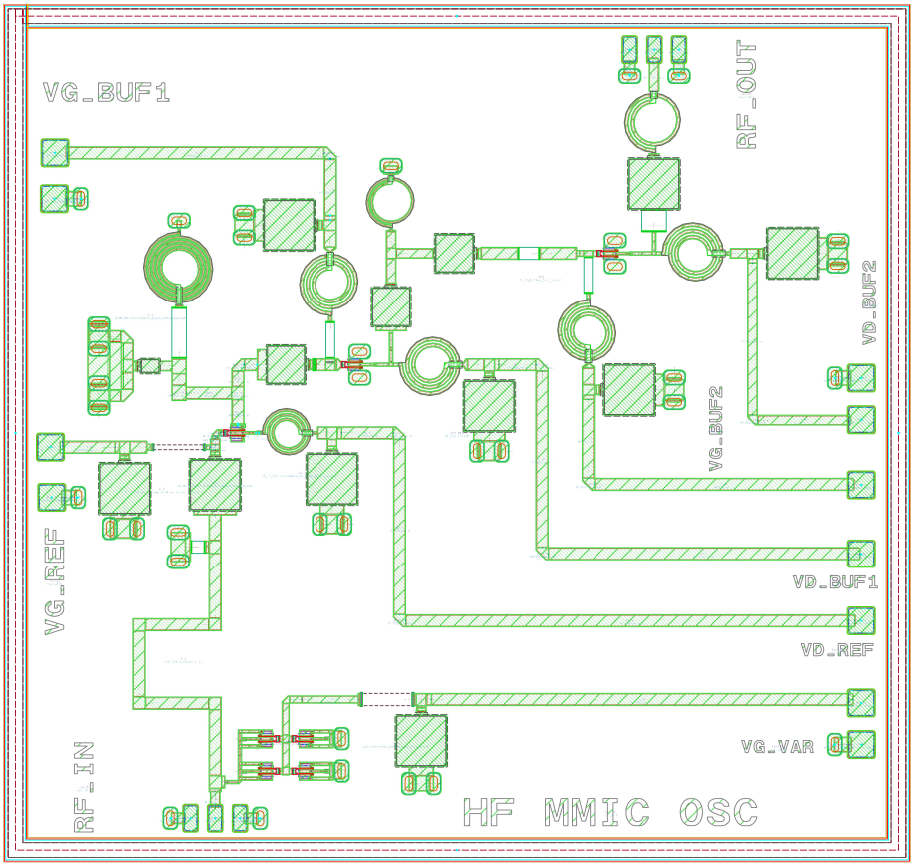

Figure 4.20: The layout of the entire HF oscillator. The size of the HF MMIC is 3.40 x 3.60 mm

5

Results

The best achieved simulated phase noise performance for the entire oscillator, measured at the output of the buffer amplifier, is shown in Figure 5.1. The lowest achievable phase noise was using $V_{\text{varactor}} = -1.6\,\text{V}$, since the Q is the highest when the varactor is more negatively biased. The quality factor at $V_{Varactor} = -0.9\,\text{V}$, the middle of the tuning range, is lowered by approximately 20% to 25%. At 12.3 GHz this corresponds to a change in Q_0 from 1380 to 1110, which can be seen in Figure 4.15.

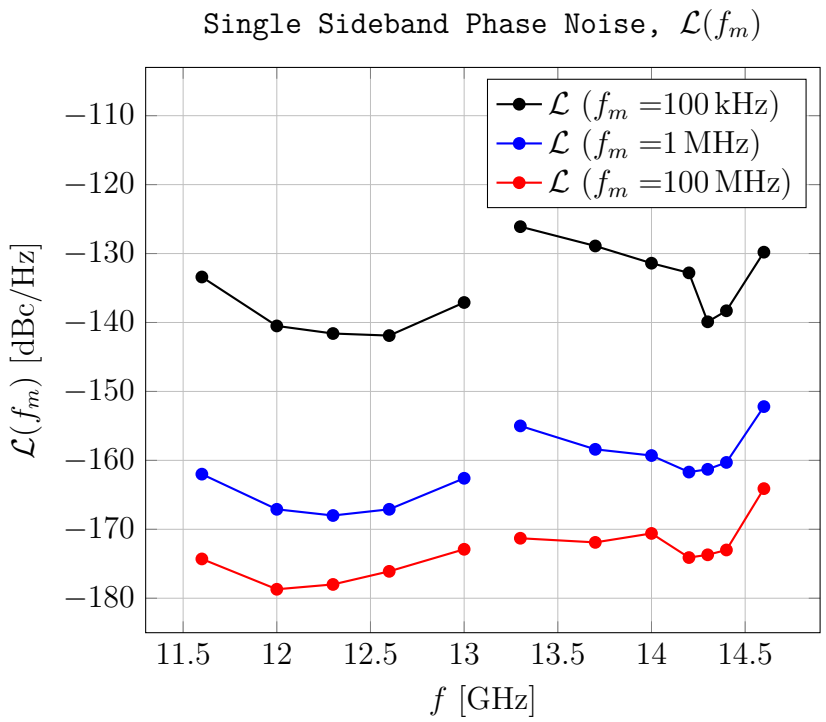

Figure 5.1: Lowest achievable phase noise per frequency for the two oscillators. At frequencies above 14.3 GHz, the phase noise behaviour changed from -30 dB per decade to -20 dB per decade.

At frequencies above 14.3 GHz, the phase noise behaviour changed from a slope of -30 dB per decade to -20 dB per decade. The phase noise floor, at 100 MHz offset, is dependent on the resonator power level. A higher loop gain ($|\Gamma_{\text{amplifier}}\Gamma_{\text{resonator}}|$) increased the power in the resonator and thus lowered the phase noise floor. The HF oscillator was optimized for a lower drain bias than the LF oscillator, which makes

it oscillate with less power in the resonator. Less power in the resonator combined with a lower buffer amplifier gain causes the HF output power to be lower than the LF output power.

The phase noise as a function of gate and drain bias is displayed in Figure 5.2. As the drain voltage increases, the minimum phase noise moves to larger gate biases.

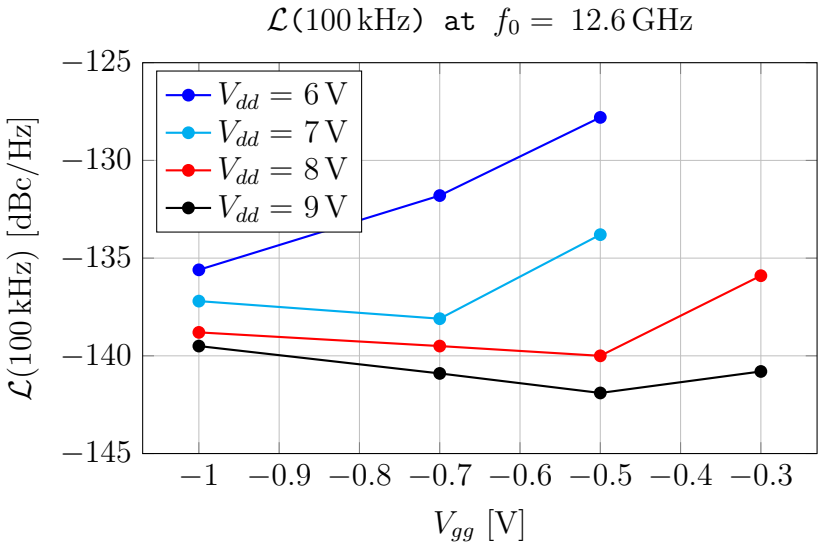

Figure 5.2: Phase noise as a function of gate and drain bias at 12.6 GHz. For a varactor bias of −1.6 V

The output power as a function of gate and drain bias is displayed in Figure 5.3. For a constant buffer amplifier bias. The higher the resonator power, the higher the output power.

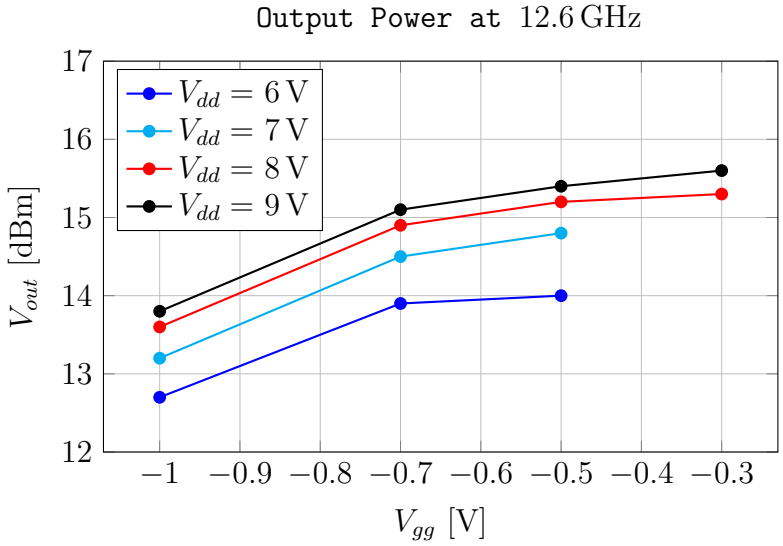

Figure 5.3: Output power as a function of gate and drain bias at 12.6 GHz. For a varactor bias of −1.6 V

In Figure 5.4, the same reflection amplifier bias and varactor bias is used as the resonator is swept from 14.2 GHz to 14.4 GHz. For 14.2 GHz and 14.4 GHz, the phase noise has a -30 dB per decade slope, but at 14.3 GHz it has a -20 dB per decade slope. This behaviour appears at all bias points for 14.3 GHz, although only for some bias points above 14.3 GHz. From the LFN modelling in Figure 3.15, the phase noise is expected to have a -30 dB per decade slope down to around 1 MHz offset.

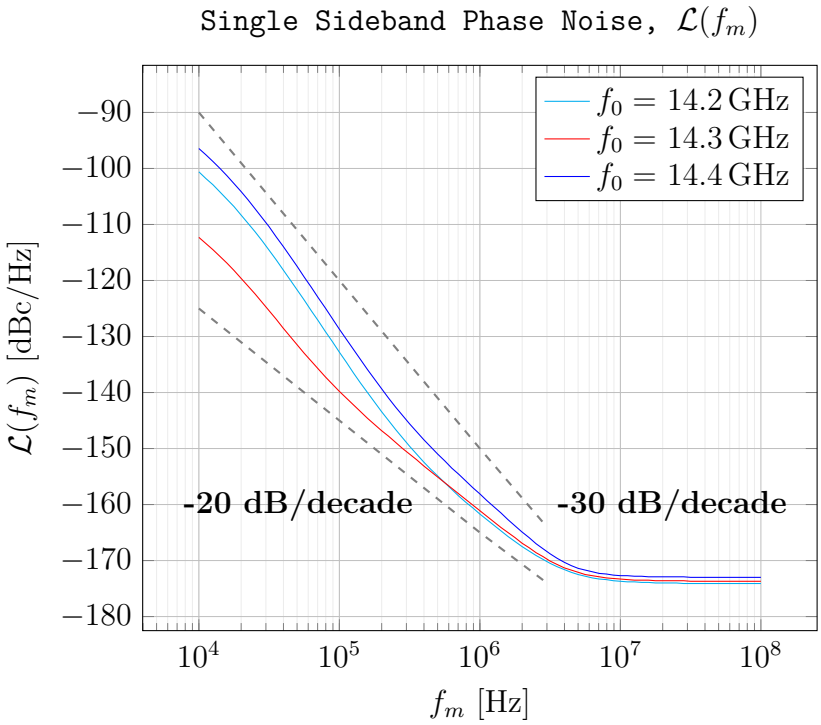

Figure 5.4: Phase noise when the bias of the reflection amplifier is kept constant but the resonance frequency is varied for the cavity. The phase noise should not differ as much in shape as it does. -30 dB/decade and -20 dB/decade trendlines are added for clarity.

In Figure 5.5, a plateau in the phase noise appears around 1 kHz offset. Everard's phase noise model is plotted in the same graph for comparison. This behaviour might be caused by high amounts of AM noise [7]. This behaviour appears even when the noise of the modelled transistor is turned off. The curves show bias points where the behaviour is visible, and does not show the bias points which minimize the phase noise.

In Figure 5.6 and Figure 5.7, the resonator voltage and output voltage is shown. In the resonator, harmonics are present and the waveform is somewhat distorted. The harmonic content varies with varactor bias. The buffer amplifier suppress the harmonics and thus the output signal is a clean sinusoidal with sufficient harmonic suppression.

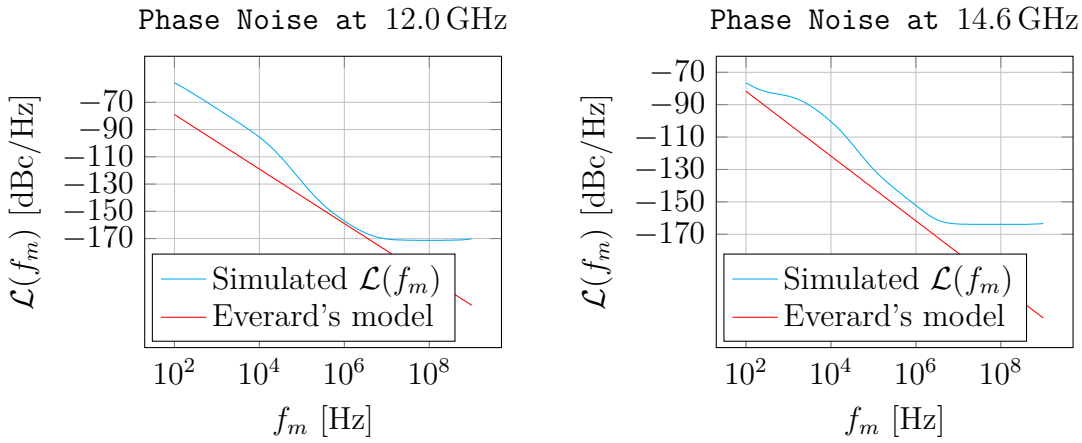

Figure 5.5: Everard's phase noise model compared to simulated phase noise ($F = 1$). Phase noise performance for bias points which show the plateau behaviour and agree well with Everard's model.

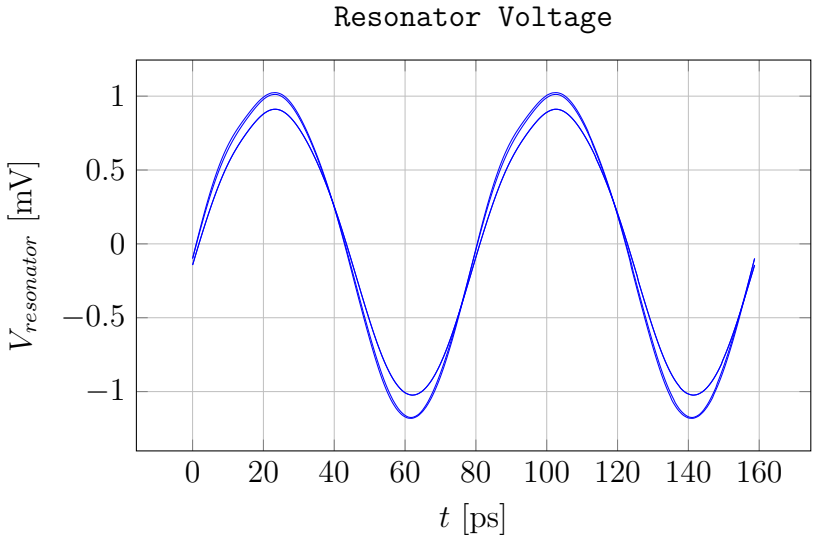

Figure 5.6: Resonator voltage waveform for the LF oscillator at 12.6 GHz. Varactor bias is swept from −1.6 V to −0.1 V

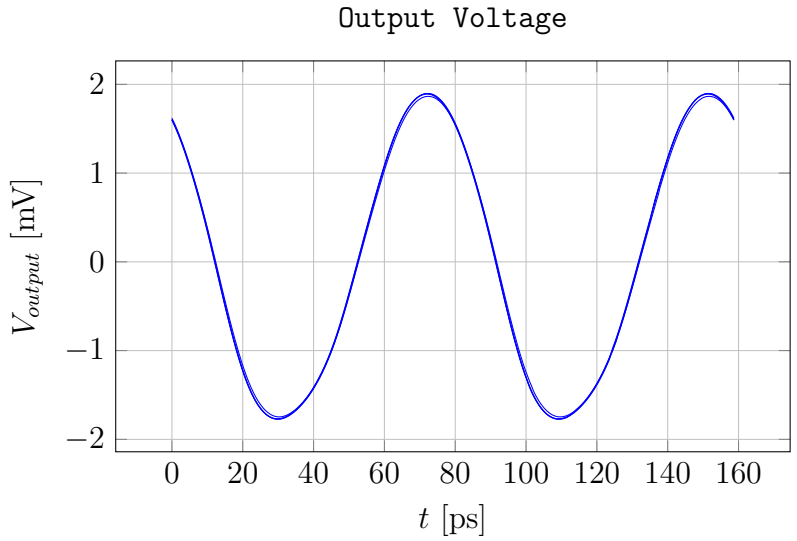

Figure 5.7: Output voltage waveform for the LF oscillator at 12.6 GHz. At the output of the buffer amplifier, the harmonics are suppressed. Varactor bias is swept from −1.6 V to −0.1 V

The phase shifter is unable to tune the phase shifter enough, so a phase error exists, as the oscillator oscillates a small step away from the resonance frequency of the cavity. The phase error at the best achieved phase noise levels are shown in Figure 5.8.

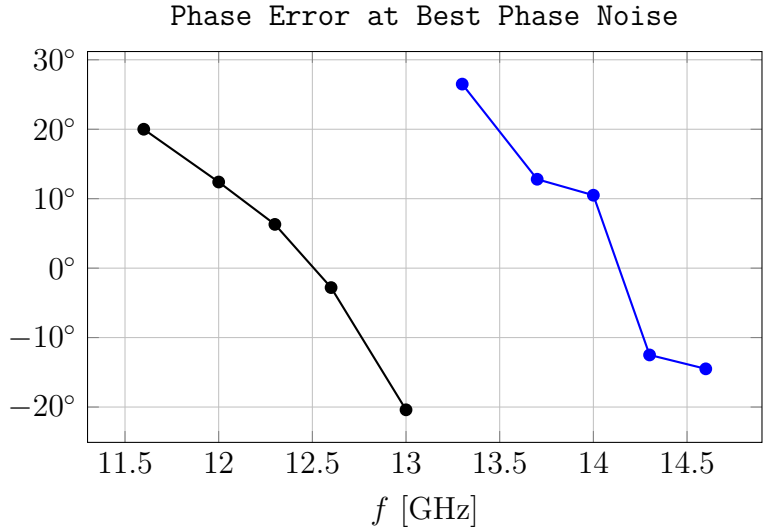

Figure 5.8: Phase error at the bias points that yields the lowest phase noise.

The different oscillator performance measures are presented in Table 5.1. The difference between FoM_{MAX} and FoM shows that there is room for improvement in the oscillator design. It is possible to achieve lower phase noise using the specified resonators.

Table 5.1: Performance of the two designed oscillators, FoM calculated for the best achieved phase noise per oscillator. The output power is controllable by changing the buffer amplifier bias.

	LF Oscillator	HF Oscillator	Unit
Frequency range	11.6-13.0	13.3-14.6	GHz
Tuning range	11.4%	9.3%	
Phase noise (100 kHz)	-141.9	-139.9	dBc/Hz
Phase noise (1 MHz)	-168.0	-160.3	dBc/Hz
Output power*	13-16	3-11	dBm
Harmonic suppression	> 24	> 35	dB
DC Power consumption	48-195	48-195	mW
FoM (100 kHz)	222.9	223.1	
FoM (1 MHz)	226.9	223.5	
FoM_{MAX} (100 kHz)	243.5	244.9	
FoM_{MAX} (1 MHz)	242.9	244.9	

* For a constant buffer amplifier bias.

The designed oscillators are compared to the state-of-the-art. In Table 5.2 and Table 5.3 is a comparison between the designed oscillators and published GaN cavity oscillator measurement results. The performance of the two designed oscillators need to be measured after manufacturing to verify their accuracy with the simulations presented in this thesis.

Table 5.2: Best achievable phase noise comparison between the results in this thesis and published measurement results for GaN cavity oscillators

	Frequency range [GHz]	Phase noise [dBc/Hz] (100 kHz offset)
Simulated results		
LF Oscillator	11.6-13.0	-141.9
HF Oscillator	13.3-14.6	-139.9
Measured results		
[17]	9.8-10.3	-140
[18]	9.9	-144
[23]	9.9-10.1	-118

Table 5.3: Phase noise comparison, for the entire tuning range between the results in this thesis and published measurement results for tunable GaN cavity oscillators

	Frequency range [GHz]	Tuning range	Phase noise [dBc/Hz] (100 kHz offset)
Simulated results			
LF Oscillator	11.6-13.0	11.4%	< -133
HF Oscillator	13.3-14.6	9.3%	< -126
Measured results			
[17] Setting 1	9.8-10.3	5%	< -129
[17] Setting 2	9.4-10.6	12.3%	< -123
[23]	9.9-10.1	1.6%	< -111

6

Conclusion

A complete three-port transistor model is required for accurate oscillator design. This three-port model should be based on and verified with measurement data.

The derived three-port model in this thesis is based on the two-port model in the WIN NP-15 design kit for ADS. WIN's transistor model is verified by measurements. In order to extract a three-port model, the parameter extraction is based on WIN's two-port transistor model. Since no measurement data is available, this increases the model uncertainty and subsequently the entire oscillator design uncertainty.

Both oscillators are close to the required oscillator performance. The LF oscillator sweeps the intended frequency band and achieves the phase noise goal for most of the resonator resonance frequencies. At 11.6 GHz the minimum phase noise is -133.4 dBc/Hz, 1.6 dB higher than the aim. The output power is high (13-16 dBm) while keeping a sufficient harmonic suppression ($>$ 24 dB). The LF reflection amplifier has its gain peak above the highest wanted LF oscillation frequency. This causes the phase response of the reflection amplifier to vary less with frequency. As a result the phase condition depends less on the reflection amplifier and subsequently the phase is more easily controlled.

For the HF oscillator, the phase noise at 100 kHz is close to the aim of -130 dBc/Hz. The harmonic suppression is good ($>$ 35 dB). The output power varies significantly (3-11 dBm). The reason for this variation is that the HF oscillator is optimized to fulfil the phase condition for lower drain voltage than the LF oscillator. The HF oscillator stops oscillating for frequencies above 14.6 GHz since the gain condition is not fulfilled for the highest wanted oscillation frequency. The gain peak for the HF reflection amplifier was below the lowest wanted HF oscillation frequency. The parasitic capacitances in L_{drain} causes the gain peak to shift to lower frequencies and lowers the reflection gain of the reflection amplifier significantly at the higher parts of the HF oscillation band.

A change in the design of the HF reflection amplifier where the gain peak is above the highest wanted oscillation frequency similar to the LF reflection amplifier would yield a better overall oscillator performance. Since the phase response of the HF reflection amplifier would be easier to control.

The PLL requires fast electronic frequency tuning. The MMIC varactor implementation in this thesis offers a wide tuning range but has high losses. The tuning range achieved in this work might be excessive so an off-chip varactor with lower losses might be an improvement.

The buffer amplifier isolate the load from the oscillator and provide more constant output power. The gain of the buffer amplifier may be too high, as the output power of the oscillator is well over 10 dBm. This high gain is advantageous since it keeps the phase noise floor low and subsequently preserves the high oscillator signal to noise ratio. The high power might cause further problems depending on the specifications of the connected mixer.

The optimal coupling for low phase noise is found for β between 2.0 and 2.5. This is due to having more power in the resonator. This does not agree with linear phase noise theory, Section 2.5.3, which suggest optimum coupling is $\beta = 1$. GaN has high amounts of flicker noise which might affect the optimum coupling.

A larger gate-width transistor would likely have been a better choice for the oscillator, since it would be capable of larger power levels that reduce the far from carrier phase noise.

6.1 Further studies

Some further studies in order to reach the minimum possible phase noise using a GaN reflection oscillator with high Q resonator are the following.

Usage of a transistor technology with modelled varactors and three port transistors would more reliably predict the performance of the transistor and the reflection amplifier. There is research [11] describing how to manufacture a GaN transistor in order for it to exhibit less flicker noise. A technology where there is LFN information depending on the transistor sizes would be beneficial.

A reflection amplifier with better gain control in order to find an optimal coupling coefficient over a wide frequency band is an alternative to be investigated, which might give better performance over a larger frequency span.

An investigation if a mechanically tunable dielectric resonator is a viable option for these purposes would be interesting, since dielectric resonators typically have higher Q than cavity resonators.

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A

Extracted Transistor model parameters

Table A.1: Angelov model modifiers in ADS

Parameter	Value	Description
`Idsmod`	1	Select Ids Current Model
`Igmod`	0	Select gate diode model
`Capmod`	2	Select capacitance model
`Noimod`	0	Select noise model

Table A.2: Angelov model gate current parameters

Parameter	Value	Unit	Description
I_j	5.00	[µA]	Gate forward saturation current
P_g	15.0	[-]	Gate current parameter
N_e	-	[-]	Gate p-n emission coefficient
V_{jg}	0.70	[V]	Voltage for gate junction current I_j

Table A.3: Angelov model drain current parameters

Parameter	Value	Unit	Description
I_{pk0}	0.07	[A]	Drain current for maximum g_m
V_{pks}	-0.80	[V]	Gate voltage (V_{gs}) for maximum g_m
D_{Vpks}	0.38	[V]	Delta gate voltage at maximum g_m
P_1	1.30	[1/V]	Polynomial coefficient for channel current
P_2	-0.14	[1/V^2]	Polynomial coefficient for channel current
P_3	0.10	[1/V^3]	Polynomial coefficient for channel current
α_r	0.15	[1/V]	Saturation parameter
α_s	2.00	[1/V]	Saturation parameter
λ	0.12	[1/V]	Channel length modulation parameter
Lvg	0	[-]	Coefficient for Lambda parameter
B_1	0.37	[-]	Unsaturated coefficient for P1
B_2	3.00	[1/V]	Unsaturated coefficient for P2

Table A.4: Angelov model breakdown model parameters

Parameter	Value	Unit	Description
Lsb0	0.21	[-]	Soft breakdown model parameter
Vtr	60.0	[V]	Threshold voltage for breakdown
Vsb2	1	[µV]	Surface breakdown model parameter
Ebd	0.2	[1/V]	Surface breakdown model exponent parameter
Kbdgate	1.0	[V]	Gatejunctions breakdown parameter
Vbdgs	10.0	[V]	Gate source breakdown voltage
Vbdgd	100	[V]	Gate drain breakdown voltage
Pbdg	0.5	[1/V]	Gate breakdown exponent

Table A.5: Angelov model capacitance parameters

Parameter	Value	Unit	Description
Cds	38.0	[fF]	Zero-bias D-S junction capacitance
Cgspi	19.9	[fF]	Gate-source pinch-off capacitance
Cgs0	21.8	[fF]	Gate-source capacitance parameter
Cgdpi	22.7	[fF]	Gate-drain pinch-off capacitance
Cgd0	21.8	[fF]	Gate-drain capacitance parameter
Cgdpe	2.60	[fF]	External gate-drain capacitance
P10	5.00	[-]	Polynomial coefficient for capacitance
P11	5.61	[-]	Polynomial coefficient for capacitance
P20	-0.10	[-]	Polynomial coefficient for capacitance
P21	0.71	[-]	Polynomial coefficient for capacitance
P30	-0.10	[-]	Polynomial coefficient for capacitance
P31	0.71	[-]	Polynomial coefficient for capacitance
P40	5.00	[-]	Polynomial coefficient for capacitance
P41	5.61	[-]	Polynomial coefficient for capacitance
P111	0	[-]	Polynomial coefficient for capacitance
P222	0	[-]	Polynomial coefficient P222 for capacitance
P10pk	0	[-]	Polynomial coefficient P10pk for capacitance [-]
m	0	[-]	Coefficient for capacitance [-]

Table A.6: Angelov model resistance parameters

Parameter	Value	Unit	Description
Rg	2.63	[Ω]	Gate ohmic resistance
Rd	19.0	[Ω]	Drain ohmic resistance
Rd2	0.23	[Ω]	Variable Drain ohmic resistance (Bias dependent)
Ri	4.41	[Ω]	Input ohmic resistance
Rs	19.0	[Ω]	Source ohmic resistance
Rgd	19.0	[Ω]	Gate-drain resistance

Table A.7: Angelov model inductance parameters

Parameter	Value	Unit	Description
Lg	10.0	[nH]	Gate ohmic inductance
Ld	2.56	[nH]	Drain ohmic inductance
Ls	40.0	[pH]	Source ohmic inductance

Table A.8: Angelov model dispersion parameters

Parameter	Value	Unit	Description
τ	0.16	[ps]	Internal time delay
RCmin	8.00	[kΩ]	Minimum value of Rc resistance
Rc	19.0	[kΩ]	R for frequency dependent output conductance
Crf	2.00	[fF]	C for frequency dependent output conductance
Rcin	500	[kΩ]	R for frequency dependent input conductance
Crfin	2.00	[fF]	C for frequency dependent input conductance
Rdel	1.00	[kΩ]	R for input delay modelling
Cdel	1.00	[fF]	C for input delay modelling
Kbgate	1e-15	[1/V]	back-gate feedback voltage modeling
Krfdc	1	[-]	division between Ids and Dispersion IdsRF current

Table A.9: Angelov model thermal parameters

Parameter	Value	Unit	Description
Rth	150	[K/W]	Thermal resistance
Cth	10	[µWs/K]	Thermal capacitance
Tcipk0	-0.001	[1/K]	Temperature coefficient of Ipk0 parameter
Tcp1	-0.0013	[1/K]	Temperature coefficient of P1 parameter
Tccgs0	0.002	[1/K]	Temperature coefficient of Cgs0 parameter
Tccgd0	0.002	[1/K]	Temperature coefficient of Cgd0 parameter
Tclsb0	0.0001	[1/K]	Temperature coefficient of Ipk0 parameter
Tcrc	0	[1/K]	Temperature coefficient of Rc parameter
Tccrf	0	[1/K]	Temperature coefficient of Crf parameter
Tcrs	0	[1/K]	Linear temp coefficient for Rs
TcRtherm	0	[1/K]	Linear temp coefficient for Rth
TcVpk	0	[1/K]	Linear temp coefficient for Vpk
TcVjg	0	[1/K]	Linear temp coefficient for Vjg

Table A.10: Angelov model noise parameters

Parameter	Value	Unit	Description
Fnc	400	[Hz]	Flicker-noise corner frequency
Kf	5e-6	[-]	Flicker noise coefficient
Af	1	[-]	Flicker noise exponent
Ffe	2	[-]	Flicker noise parameter
Tg	25	[°C]	Gate equivalent temperature
Td	300	[°C]	Drain equivalent temperature
Td1	2	[-]	Drain equivalent temperature coefficient
Klf	3e5	[-]	Flicker noise coefficient
Fgr	20	[kHz]	G-R frequency corner frequency
Np	1	[-]	Flicker noise frequency exponent
Lw	0.1	[mm]	effective gate noise width
Tnom	25	[°C]	Parameter measurement temperature

Table A.11: Unused Angelov model parameters (Default values used/parameter not used in ADS 2019 model)

Parameter	Description
Vkn	Knee voltage (obsolete)
Lambda1	Channel length modulation parameter only used with `Idsmod`=3
NoiseR	Gate noise coefficient [-] only used with `NoiMod`=2
NoiseP	Drain noise coefficient [-] only used with `NoiMod`=2
NoiseC	Gate-drain noise correlation coefficient [-] only used with `NoiMod`=2
Tmn	Noise fitting coefficient [-] only used with `NoiMod`=1

A.1 Parameter scaling equations

All parameters were converted to scaling equations that scales with the device size, W_{tot}, which can be seen in Table A.12. This was done to enable easier modelling of different size transistor if there was a need to. It also makes it easier to compare parameter values between different GaN technologies.

$$W_{tot}[\text{mm}] = \#\ \text{Fingers} \cdot W_{finger} = 2 \cdot 0.05\,\text{mm} = 0.1\,\text{mm} \tag{A.1}$$

Table A.12: The implemented scaling equations for the transistor modelling

C_{ds}	=	$C_{dsw} \cdot W_{tot}$	[fF]	R_{d2}	=	$0.001 + R_{d2w}/W_{tot}$	[Ω]
C_{gspi}	=	$1 + C_{gspiw} \cdot W_{tot}$	[fF]	R_{gd}	=	$0.001 + R_{gdw}/W_{tot}$	[Ω]
C_{gs0}	=	$1 + C_{gs0w} \cdot W_{tot}$	[fF]	R_{therm}	=	$0.1 + R_{thermw}/W_{tot}$	[K/W]
C_{gdpi}	=	$1 + C_{gdpiw} \cdot W_{tot}$	[fF]	L_g	=	$0.001 + L_{gw} \cdot W_{finger}$	[pH]
C_{gd0}	=	$1 + C_{gd0w} \cdot W_{tot}$	[fF]	L_d	=	$0.001 + L_{dw} \cdot W_{finger}$	[pH]
C_{gdpe}	=	$1 + C_{gdpew} \cdot W_{tot}$	[fF]	L_s	=	$0.001 + L_{sw} \cdot W_{tot}$	[pH]
C_{rf}	=	$1 + C_{rfw} \cdot W_{tot}$	[fF]	I_{pk0}	=	$I_{pk0w} \cdot W_{tot}$	[A]
R_g	=	$0.001 + R_{gw}/W_{tot}$	[Ω]	I_j	=	$I_{jw} \cdot W_{tot}$	[A]
R_i	=	$0.001 + R_{iw}/W_{tot}$	[Ω]	R_{cmin}	=	R_{cminw}/W_{tot}	[Ω]
R_s	=	$0.001 + R_{sw}/W_{tot}$	[Ω]	R_c	=	R_{cw}/W_{tot}	[Ω]
R_d	=	$0.001 + R_{dw}/W_{tot}$	[Ω]	τ	=	$\tau_w \cdot W_{tot}$	[ps]