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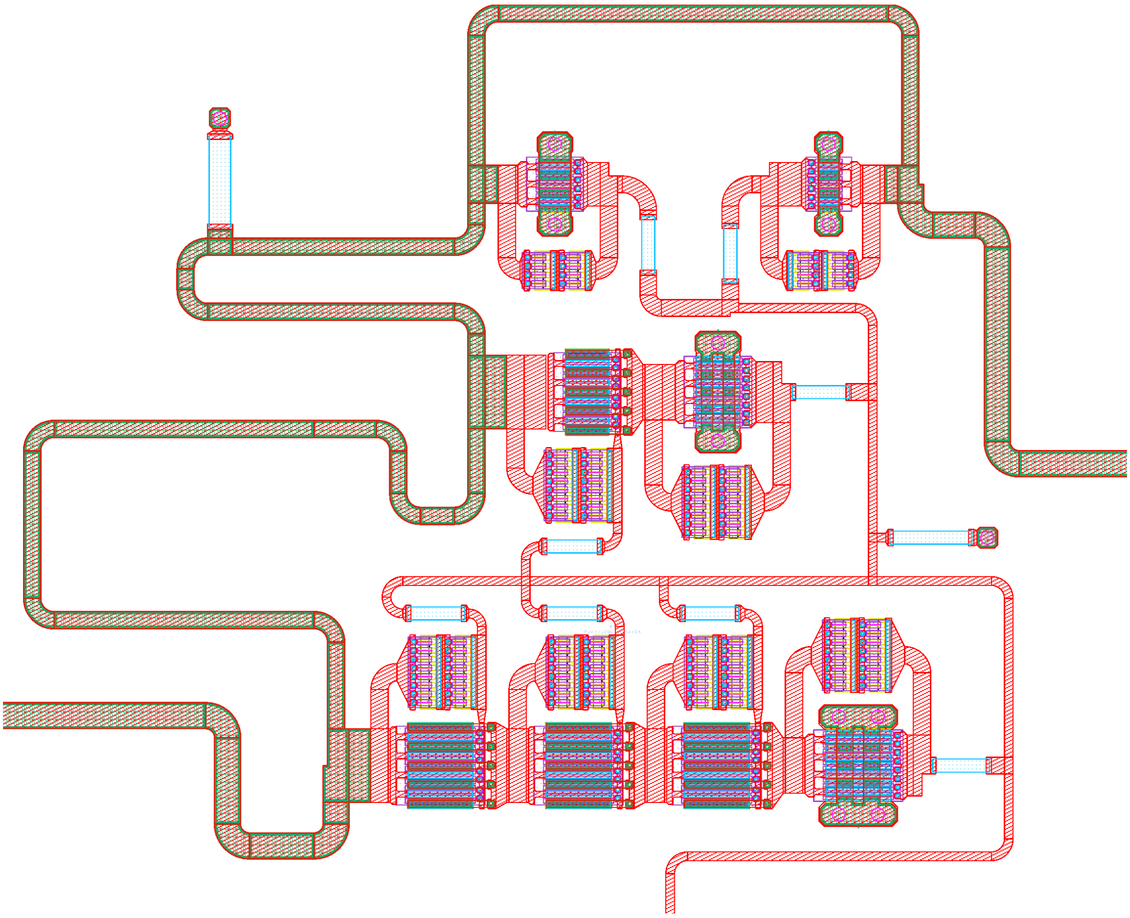

Wideband MMIC Power Limiters for Integrated Receivers

Design and Simulation

Degree project report in Wireless, Photonics, and Space Engineering

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Cover: Layout representation of a diode-activated limiter circuit, made in Keysight ADS.

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Abstract

This thesis explores the feasibility of designing wideband power limiter circuits that can be manufactured using monolithic microwave integrated circuit (MMIC) technologies, with a primary focus on gallium nitride (GaN). Three complete limiter circuits have been designed and simulated with different performances, along with one limiter needing external activation. No measurements of the circuits have been made. Three of the designs were made for a 0.15 µm GaN process, and the last for a GaAs process incorporating PIN diodes. The GaN-based limiters use switch-transistors to achieve the limiting behavior with different means of activation, and are designed to operate in the $2-6$ GHz frequency band. The minimum frequency is limited by the leakage power level, and the upper frequency by small-signal performance. The most promising complete GaN limiter keeps the leakage below 25 dBm for input powers up to 50 dBm. The GaAs limiter utilizes PIN diodes in an anti-parallel configuration to achieve limiting. It operates in the $2-18$ GHz range, making it a suitable option when this type of process is available. The leakage is below 17.5 dBm for input powers up to 48 dBm. It is, however, unclear whether the limiter itself will survive powers that large. Although the designs presented here seem to perform well in terms of power and bandwidth, the insertion losses are slightly higher than what is generally accepted.

Keywords: MMIC, Limiter, Wideband, GaN, Leakage, Protection, RADAR.

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Josef Jörgensen, Gothenburg, June 2025

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1 Introduction

In radar applications, where long range is one of the main requirements, the output powers are usually large. The more power transmitted from the system, the stronger the response one can hope to receive. In addition to more power, the sensitivity of receivers is improved to register weak signals. More power and better receivers allow for the detection of smaller targets at longer distances. If, however, a high-power signal reaches a system, it can cause damage to the sensitive devices. There are multiple scenarios where this can happen. If two systems operate in proximity, power from one could enter the other. There is also the risk of power being reflected from large nearby objects, such as buildings, which results in a significant portion of the transmitted power reaching the receiver. To avoid damaging the receiver, a protection circuit called a limiter is often introduced at the input. The limiter aims to leave low-power signals unaltered while attenuating potentially harmful signals. Traditionally, this has been accomplished using discrete diodes that are activated by the voltages resulting from the incoming signal, thereby reflecting the signal by introducing a low-impedance point [1]. The drawback to making these discrete circuits is that they can become rather large.

A large size becomes problematic when multiple receivers have to be closely packed in so called AESA (Active Electronically Scanned Array) systems, where each antenna element has its own transmitter and receiver. AESA radars are becoming more common since they reduce losses and enable instant beam steering [2], the requirements for size are increasing. The main solution to the size problem is the move towards integrated microwave circuits. In radar applications, GaN MMICs (Monolithic Microwave Integrated Circuits) are gaining popularity due to their excellent power-handling capabilities [3]. The optimal solution in terms of total circuit size would be to have the entire radar frontend on a single MMIC chip. It also reduces the need for external connections between components.

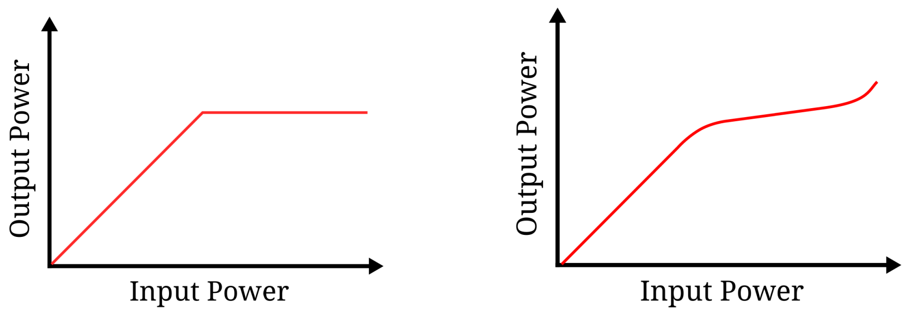
While circuits made in GaN can survive large powers, they are subject to trapping effects which reduce performance, and will at some point break down [4]. The need for a limiter circuit has thus not been eliminated by switching to GaN components. Most MMIC limiters found in the literature use PIN diodes to achieve the limiting behavior, just like in the case of discrete alternatives. The commercially available MMIC technologies with integrated PIN diodes are few and limited to GaAs, so for GaN, some other limiter topology is required. Instead of using diodes to achieve the limiting behavior, transistors can be configured to act similarly. The publications on this type of limiter are few [5], [6],[7], [8], and they are either narrow-band, needing external circuits to work, or cannot handle large powers. Narrow-band limiters are suitable for specific applications but must be adjusted for each design they are part of. In some surveillance applications, the primary goal is to listen over a wide range of frequencies, and therefore, the system's bandwidth is of great importance.

The goal of this thesis is to investigate and create wideband MMIC limiter designs using different topologies. This is done to determine the benefits and drawbacks of each topology, and to find the best alternative for a specified set of requirements. The primary technology used is GaN, but a limiter designed in a GaAs process with PIN diodes is also included for reference. First, a GaN limiter is presented, utilizing only transistors, which is relatively simple but has some performance limitations. Afterwards, a limiter building on the first one is shown, using Schottky diodes to improve the performance of the former. The drawback of this limiter is its larger size. A limiter topology found in literature, using both series and shunt transistors [6], is investigated for reference. This limiter requires a detection circuit for transistor activation and is thus more complicated. Lastly, an integrated PIN diode limiter is designed to get an idea of what performance benefits can be expected when using diodes over transistors as the limiting devices. The PIN diodes are part of a GaAs process, and the change of material for the receiver results in other requirements for limiter performance. All results in this thesis are based on simulation, and the designs have not been physically measured. A summary and comparison between the designs of this thesis and designs from previous works is presented to evaluate the results.

2

Limiter Fundamentals

The purpose of the limiter circuit is to prevent the power passing through it from exceeding a specified level. Figure 2.1a presents the desired input-output power relation. In this figure, there are two distinct regions. First is a linear region, where the output power is identical to the input. Since the limiter has no functionality when it comes to signal processing, ideally, all small signals should pass through it without any interaction. A low insertion loss is important for keeping the noise low, making it suitable to implement with an LNA [8]. Following the linear region is the flat region. At some point, the power should be limited to avoid damage to the trailing circuits. A perfectly flat response is not important, as long as the power does not exceed the specified value. For a physical limiter, one should expect a behavior similar to what is seen in Figure 2.1b, [8], [5]. The first thing to note is that the linear section is slightly shifted downwards due to losses in the limiter. When reaching activation, the flat, limited region sometimes has a slight slope. The transition between regions is also less sharp. Lastly, there is a point at which the limiting devices will have a problem handling the power, after which the limitation quickly deteriorates.



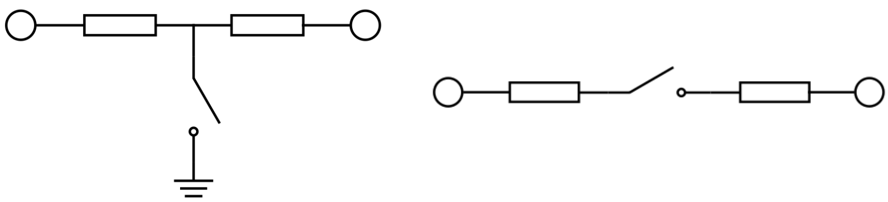
(a) Ideal input-output power relation

(b) Typical limiter power response

Figure 2.1: The large-signal power response of an ideal limiter alongside a graph showing the traits to be expected from a physical limiter.

The concept of most limiters is to have some component that provides a low-impedance path to ground. The idea is that power will be reflected by the low impedance point. Representing this component with an electrical switch, the concept becomes what is demonstrated in Figure 2.2a. The most straightforward way to achieve this behavior is to use diodes that start conducting when the voltage is sufficiently large [9]. When the limiter is constructed using discrete components, this is easy to do. An alternative is to use transistors as switching components. In integrated circuits, diodes are less common, so using FET (Field Effect Transistor) switches can be an alternative [6]. These can be activated by power detector circuits that turn them on when a certain level is exceeded, and keep them turned off otherwise [6] (later referred to as *detector-activated* limiters). They can also be activated more directly, similarly to the diodes, by taking advantage of the internal resistive and capacitive effects in the transistor (*self-activated*), or adding a diode between the signal and the gate (*diode-activated*) [5]. While it is possible to construct PIN diode limiters with different means of activation, using detectors, for example, only one type is covered here. It will be referenced as "PIN diode limiters", since most limiters of this type utilize PIN diodes as the limiting devices. The terms "self-activated", "detector-activated", and "diode-activated" always refer to transistor limiters in this work.

For detector-activated limiters, it is also possible to get limiter functionality using a series switch transistor that is turned on by default, and turned off when the power reaches a certain level, see Figure 2.2b. This type of limiter requires a dedicated bias network since a larger input power should result in a lower bias to the transistors. [6]



(a) Shunt Limiter **(b)** Series Limiter

Figure 2.2: Electrical concept for the most fundamental limiters.

In reality, limiter circuits have some limitations that prevent them from behaving in the ideal manner presented earlier. One important reason is that the limiter itself cannot handle unlimited input powers. The components that make up the limiter circuit have limitations in both the voltages and currents they can withstand, as well as in the thermal handling of the material, since some power will be dissipated in the switching components as heat. When discussing the performance metrics of a limiter, it is essential to specify the maximum input power for which it is designed.

2.1 Limiter Performance Metrics

There are three different metrics used in this thesis to describe the overall performance of limiters. The one that best describes the limiting behavior is leakage. The other two are insertion loss and maximum power. The bandwidth of the limiter is a result of all three. The values can be seen in the previously mentioned power response graph, as presented in Figure 2.3. Another property that is worth mentioning is the linearity of the limiter. For large signals, the harmonics generated in the circuit will be strong enough to become problematic in later stages of the receiver.

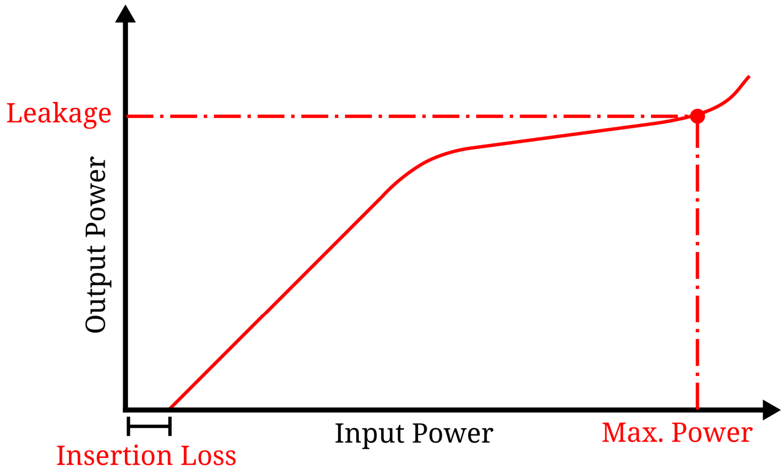


Figure 2.3: How the three performance metrics can be read from the limiter power response. The insertion loss is exaggerated for better visibility.

Linearity will, however, not be discussed further in this thesis, and no simulation results are presented.

The leakage will, for this work, be defined as the maximum output power of the limiter within the operating range of input powers. In Figure 2.1a, the leakage is the constant value that the limiter reaches after a certain input power. In practice, when the output looks as described in Figure 2.1b, specifying the maximum input power is needed to determine the leakage. In most cases, the maximum power is defined as a requirement based on what powers are reasonable to expect to reach the receiver. For transistor limiters, it is possible to adjust the leakage to some extent, as the bias voltages can be tuned. The minimum possible leakage for detector-activated limiters can be determined by applying the bias that fully activates the transistors and reading the output at maximum input power. This gives the maximum since the limitation depends on how well the devices are activated, and there is no way to make them perform better than by fully activating them. For self-activated and diode-activated limiters, the situation is more complicated, as the bias also affects the insertion loss.

The insertion loss shows how much of the incident power passes through the circuit when not limiting, and hence indicates the signal loss. Since loss in this network directly results in a reduced signal-to-noise ratio in the system, it has to be as low as possible. The components making up the limiter are frequency dependent, and as a result, the limiter itself is, so insertion loss will always be a limiting factor for the upper frequency of the limiter. Depending on the matching network, it might also set a lower limit.

If the bandwidth is not determined on the lower end by the insertion loss, it will be a result of the frequency dependence of the leakage. As will be described later, it is common to design limiters with multiple stages to improve performance. When the frequency is reduced, the effective electrical distance between the stages decreases for a given length of transmission line. Thus, the effectiveness of the later stages is also reduced, resulting in poorer limiting performance.

2.2 Design Requirements

The main goal of this thesis is to find wideband options, so the frequency bands are important to specify. For this work, two frequency bands were settled on. The goal bands are $2-6\,\mathrm{GHz}$ and $2-18\,\mathrm{GHz}$. The former gives good coverage over the S and C radar bands while the latter includes the S, C, X, and $\mathrm{K_u}$ bands [10] and is thus of high interest in radar applications.

Within the specified frequency bands, the insertion loss should be better than 1 dB from a 50 Ω system. When all other requirements are fulfilled, this is what should be optimized. Reducing the insertion loss works towards the goal of a transparent limiter that does not affect small signals. Connected to this is the return loss, which should be better than 10 dB.

The goal is to protect the receiver, and the leakage level is chosen thereafter. Exact values depend on material choice and the device sizes in the components following the limiter. The goal for power handling is set to 48 dBm. This means that the output power from the limiter, up to this input power, should be held below the leakage requirement. Some effort is made to ensure that the limiter itself can withstand powers above this value. Still, it has not been possible to verify this reliably through simulations. The limiter should be able to withstand this power for pulsed signals with a duty cycle of 10 %. The only reliable way to verify this is by measuring them, and that has not been done as part of this thesis. The goal itself, 48 dBm, is somewhat arbitrary, but something around 50 W-100 W is reasonable since it has been accomplished before [5], [11], and since radar outputs can become very large.

2.3 Material Considerations

In modern times, GaN MMIC technologies have gained popularity in the design of high-power microwave components. The main benefit of GaN components is that they can survive large powers because of the large band gap in the semiconductor, while still performing well in high frequencies using HEMT structures [3]. In previous research, it has been demonstrated that some GaN LNAs exhibit significant performance degradation when subjected to powers exceeding 28 dBm [12]. The recovery times increase with the power level, so a leakage below 25 dBm is a suitable choice.

It is reasonable to assume that a GaAs LNA can withstand 20 dBm of input power [13], [14]. The specific amount depends on both technology and LNA topology, so to keep some margin, it would be good to keep the leakage below 18 dBm. The heat dissipation is the main problem for the survivability of GaAs PIN-limiters because of poor thermal conductivity in the GaAs substrate [13]. It is therefore difficult to determine the required device sizes, as little information is available on how much they can handle and how this depends on their size.

2.3.1 Models

The development kit and models used for the GaN designs and simulations belong to the GH15 technology by UMS. While good models are provided for the transistors in steady-state operation, several other aspects are necessary to evaluate the limiter more effectively through simulation. The primary issue with capacity is limited knowledge about the power-handling capabilities of the transistors. Since thermal handling depends on the direct environment, the only reliable way to determine those properties is to perform measurements, and that has not been done for this thesis.

One challenge for both processes is predicting the activation behavior. Before the limiting devices are activated, there is a brief period during which the signal can pass through the limiter without being blocked, resulting in so-called spike leakage [15]. If this is large enough, the circuits might become damaged before the limiter has a chance to function. Transient simulations can help identify some crucial problems with the circuit, but having a good simulation result will not, however, guarantee that the circuit will behave well in practice.

2.4 Performed Simulations

Since all results in this thesis are derived from simulations, it is essential to specify how they were obtained. All simulations for this thesis were performed in Keysight ADS. Electromagnetic models for the passive networks were generated using the Momentum Microwave simulator. For the small-signal performance, S-parameter simulations were conducted. For the limiting behavior, harmonic balance simulations were used. For the GaN limiters, an order of seven was used, while only five was used for the PIN limiter.

It is worth noting that the harmonic balance simulations for the PIN limiter initially encountered difficulties converging. The problems mainly appear for some parameter values. The most important aspect was the size of the diodes. If the diodes of the first stage were too small, the convergence errors were more frequent. The problems mainly arose at the power levels where the limiting behavior begins, and at the levels where the diodes reach their maximum capacity. The presented PIN limiter design shows good convergence, however.

2.5 Topology choices

There are multiple ways to design a limiter, and each has its general benefits and disadvantages. There are two major decisions to make early in the design process. One is the principle of operation, that is, what mechanisms give rise to limitation. The second is the topology, in other words, how to arrange the limiting devices so that they perform as required. This section aims to discuss the latter since the former will be covered in separate chapters.

2.5.1 Using multiple stages

One concept common in literature is the use of multiple stages. The limiter is usually initiated by a main stage that handles the majority of the power and is completed by a so-called cleanup stage. In between, there can be intermediate stages if needed. In most designs where the limiter will be subjected to large powers, intermediate stages are required.

The reason for using multiple stages is that some power will leak through each stage. The following stage will then act as another low-impedance point, reflecting this power. At higher powers, more power is likely to leak into the next stage, and therefore, the requirements on the next stage are increased. If the leaked power is large enough, one cleanup stage may not be sufficient, and intermediate stages are added until the desired leakage is achieved.

The transmission line length, and thus the phase shift between the stages, is usually chosen to be a quarter wavelength for good activation of the devices [5]. In PIN diode limiters, the smallest and last stage will be turned on first, resulting in a voltage maximum at a quarter wavelength before it. Placing the preceding stage at this electrical point will thus introduce it to a higher voltage, turning it on faster [16]. This is likely the same effect seen in the transistor limiters. A quarter-wavelength transmission line between stages also increases the return loss [16], which is desired. This is not possible in a wideband application, since the phase shift will be vastly different for the different frequencies. In that case, it is better to choose the line lengths to get the optimum small-signal behavior.

One benefit of splitting the limiter into multiple smaller stages instead of one large first stage is that it makes matching easier. Each stage will act as a capacitor for small signals. The limiter will hence act as a low-pass filter, and the more stages in the limiter, the higher the order of the low-pass filter, resulting in a flatter frequency response. As a result, the insertion loss can stay below the maximum allowed value for longer.

2.5.2 Shunt Limiters

Shunt limiters are the most common limiter topology, and they can be made using either transistors or diodes as limiting elements. This type of limiter is what was presented in Figure 2.2a. All limiters presented in this work use shunt stages in some configuration.

There are several benefits to having the limiting elements in a shunt configuration compared to the series alternative. The first is that the requirements on small-signal behavior are loosened since no useful signal passes through the devices. They only conduct when limiting, and in that case, the signal is distorted either way. Another benefit is that it is easier to use the signals entering the limiter for activation of the limiting elements. Since a rise in voltage activates both transistors and diodes, the natural rise from strong signals can be used directly.

2.5.3 Multi-shunt Topologies

The multi-shunt topologies are special cases of shunt limiters. The idea is to have multiple shunt stages that work at the same electrical point. Although no designs have been developed in this thesis utilizing this concept, it is commonly found in the literature, particularly when authors aim for exceptional power handling. The benefit of doing this is that the power in the first stage is divided into two or more paths, significantly reducing the power that the devices have to withstand. This can be seen in both diode limiters [17], [11] and transistor limiters [5], [7].

The reason why this has not been used in the designs for this work is that adding more branches not only doubles the power handling of the design, but also doubles the capacitive effects of the transistors. The bandwidth suffers greatly from this. Previously, the benefit of dividing the capacitance into multiple stages was discussed, and this is effectively the opposite.

2.5.4 Combined Series and Shunt Topology

While limiters that use series stages are rare, they are possible to implement using transistors, and this has previously been done with good results [6]. The primary drawback is that this design requires both a detector and a bias network to operate. Some effort has been put into designing detectors for the GaN process as part of this thesis, but no useful results have been obtained. It is possible to create a circuit that produces an output voltage based on the signal strength, but comparing this with a reference and converting it into a signal that can activate transistors was not achieved. There are no useful designs presented in the literature for this either. Since both series and shunt transistors are used, the bias also needs two complementary outputs.

Another restriction to this topology is the size of the first stage. All power that enters the first stage will inevitably go through the first transistor, and so the survivability of the limiter depends on this. For the shunt limiters, it is possible to both add more transistors in series to reduce the voltage drop for each device and to transition into a multi-shunt topology for even better power handling.

2.5.5 Anti-Parallel Limiter

Shunt PIN diode MMIC limiters have been made since 1987 [18], and most of them use a sort of shunt topology. The topology is similar to the multi-shunt configuration, featuring two branches for each stage. One of the branches is reversed so that it starts conducting for large negative voltages, see Figure 2.4 for illustration. These limiters, therefore, better limit the signal in its entirety. This can, in turn, be combined with the multi-shunt presented earlier to further increase power handling [17].

From simulations, it appears that the diode size has little effect on limiting ability. The phase shift between the stages, on the other hand, makes a more significant difference. A PIN limiter is generally designed with a 90° phase shift between the stages. Since the limiting ability is reduced with lower frequencies, it is reasonable first to try to achieve a good enough limiting ability for the lowest

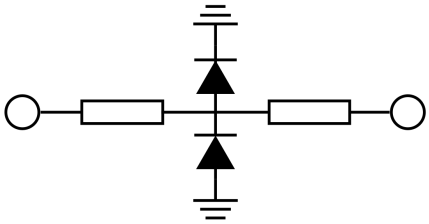


Figure 2.4: The fundamental version of an anti-parallel diode limiter.

frequency of the specified frequency range. From simulations, it becomes clear that longer transmission lines between stages worsen insertion loss. There is thus a tradeoff between insertion loss (and hence bandwidth) and the limiting ability.

3

Self-Activated Transistor Limiters

The most fundamental transistor limiter, which can be created in most GaN processes, uses only transistors with a constant bias applied. The parameters that determine limitation behaviors are transistor size and number, the number of stages, electrical spacing between stages, and the applied bias to the transistors. Intrinsic effects in the transistors allow them to be activated by themselves [8]. The performance of such a limiter is worse than what can be achieved in more complicated circuits, but its simplicity makes it worth investigating.

3.1 Principle of operation

In Figure 3.1, a conceptual schematic of the proposed limiter is presented. This type of limiter is interesting due to the ability to work without any advanced bias network for the transistors. The circuit could be described as a HEMT switch experiencing compression [19]. By choosing a suitable bias voltage, V_{bias} in the figure, the compression can be chosen to achieve the desired limiter functionality. The choice of bias is crucial for setting the leakage of the limiter, which becomes apparent in the simulation results.

The idea is that the signal presented on the drain terminal of each transistor will leak to the gate, raising the gate voltage and thus turning the transistor on. The intrinsic effects of a transistor can be seen as both resistive and capacitive [20]. The intrinsic capacitor between drain and gate should conduct better for the higher frequencies, thus resulting in better activation. Higher frequencies do indeed result in better limitation for this kind of limiter, but simulations indicate that this is mainly the result of the lines between stages being short, rather than a property of the transistors. When the same transistor configuration is used, with transmission line components representing a 90° shift at 2 GHz, the limiting region is significantly flatter, and the dependence on frequency is reduced.

The closer the transistor is to conducting, the quicker it starts limiting, resulting in lower leakage. For depletion mode transistors, which is the case here, this means having a higher bias voltage. On the other hand, having it close to conducting makes it less turned off for weak signals, resulting in a higher insertion loss. There is, in other words, a tradeoff between leakage and small-signal performance.

To ensure the limiter operates correctly in situations where the receiver is turned off and no bias voltage is applied, a pull-up resistor to ground ($R_{pull\text{-}up}$ in the figure) can be introduced, which is possible since the design utilizes depletion-mode transistors. The reason for having the bias in the first place is to keep the insertion loss as

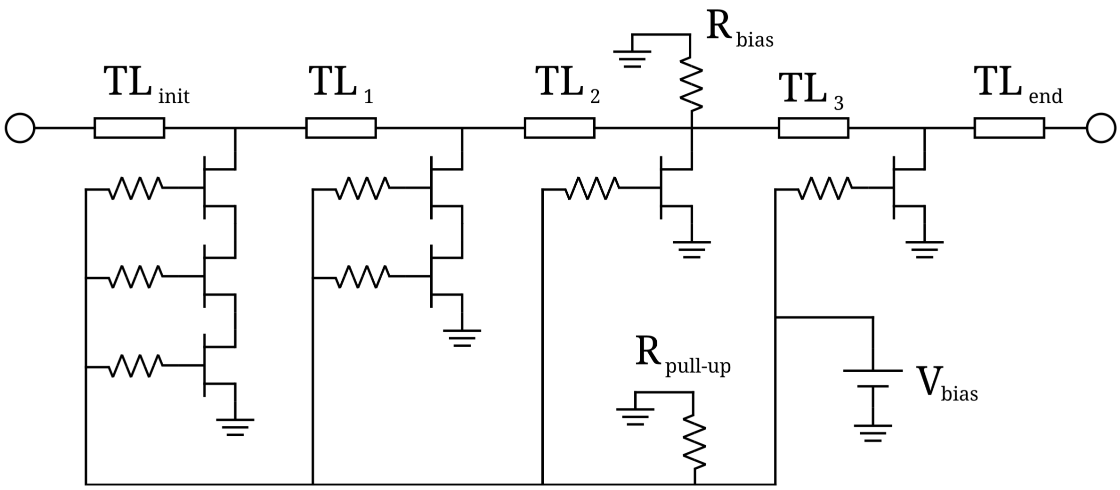


Figure 3.1: Schematic of the suggested self-activated transistor limiter.

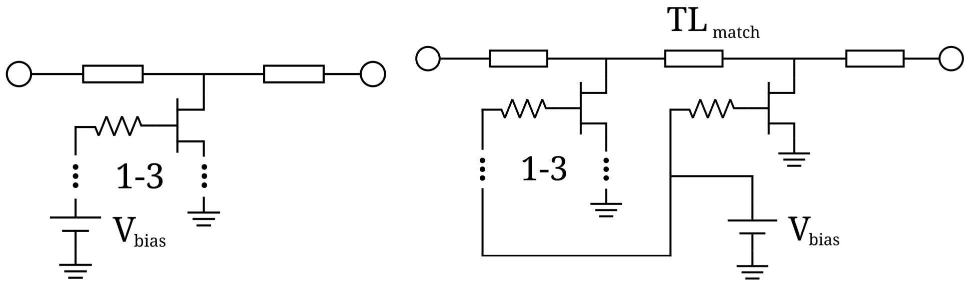
small as possible, but when the system is turned off, there is no need for small-signal performance. When the bias is turned off, the gate voltage is easily raised, and the transistors start limiting to their best ability. There will be a small current going through this pull-up resistor during normal operation, resulting in a constant power consumption. By keeping the resistance large enough, the power consumed should, however, be negligible compared to the power used for other parts of the system.

3.2 Choosing Transistor Sizes and Numbers

When it comes to choosing transistor sizes, there are multiple things to consider. The benefits of a larger transistor are twofold. A larger transistor with more fingers will result in a lower on-resistance [21], and will thus limit better, and be able to handle larger currents. An increase in size also means that a larger amount of power can be dissipated into heat before it burns. The drawback of larger devices is that they increase the capacitive effects, and as a result, the limiter becomes more narrowband.

While it should be obvious that a larger transistor can handle more power, there is some difficulty in determining how much. Usually, thermal handling is not part of the models provided by the foundry and is difficult to simulate. Thermal simulations are outside the scope of this thesis. Here, assumptions are made based on similar designs in papers, and thus have a low accuracy.

To better understand how much power is absorbed in each stage, simulations have been performed on simple shunt limiters with one and two stages as demonstrated in Figure 3.2. The first stage used one to three transistors in series. The transmission line length between the stages, TL_{match} in Figure 3.2b, was optimized in terms of small-signal insertion loss in the $2-6$ GHz band, and the simulations were performed in the ADS circuit simulator using transmission line models between the stages. Keeping all transistors the same size, it appears as if the amount of power absorbed in each stage remains constant regardless of the number of transistors in the stage or the addition of a second stage. With this in mind, it is easy to pick the number of transistors in the first stage in a way that should survive a certain amount of input power. A conservative choice would be to choose as many transistors as would be required if they were to absorb all the incoming power, but this will also reduce the efficiency of the stage, since less will be reflected. The drawback of adding more transistors in series in the first stage is that the total on-resistance increases. As a result, the stage becomes worse at limiting. Another benefit of having more transistors in series is that it reduces small-signal capacitance, which is beneficial for bandwidth.



(a) Single-stage **(b)** Dual-stage

Figure 3.2: Single and dual-stage self-activated limiters used for power simulations.

The power absorbed in the second stage is significantly lower than in the first, but could still prove important for strong signals. Making the stage out of two transistors seems to be the best option. Using more than this will reduce the effectiveness of the stage too much, and using just one large transistor would be too capacitive. To achieve the equivalent capacitive effects of two transistors in series, one transistor of half the size could be used; however, this approach may potentially lead to power handling issues. The remaining stages can be made small since no significant amounts of power will reach them, and the smaller size is beneficial both in terms of bandwidth and chip size.

3.3 Limitations on bandwidth

It was previously mentioned that the main reason for the circuits' small-signal frequency dependence is the intrinsic capacitances in the transistors. These capacitances can be altered for each transistor both by changing transistor geometry and the bias voltage. As described in the section above, transistor size directly affects limiting behavior and power handling, and the bias determines the leakage. To fulfill a specified power requirement, the choices for size and number are restricted, and the leakage restricts the bias choice. Obtaining a wideband small-signal behavior is thus mainly achieved through designing a suitable matching network. It is impossible to match capacitors for all frequencies, and the frequency response will inevitably become a low-pass filter. The best option is to make an LC network with many poles. For this reason, it is better to split the capacitances into multiple stages from a bandwidth perspective. Between the stages, slightly inductive transmission lines are placed with lengths optimal for bandwidth.

Since the bias voltage is a tradeoff between leakage and parasitics, and the leakage has to be low, it quickly became clear that the $2-6$ GHz band should be possible, but achieving higher frequencies is unlikely. What would be required is the implementation of a network that allows for significantly lower bias voltages when the limiter is turned off, which would enable higher frequencies. This being said, the frequency band $2-18$ GHz seems unlikely to be achievable for a GaN limiter that can handle large input powers, due to the requirements on transistor size.

3.4 Design Example

Now it is time to present an example of how a limiter like this can look. It starts with a stage featuring multiple large transistors that can withstand high powers, followed by a slightly smaller stage, and two smaller cleanup stages.

3.4.1 Schematic and functional description

The layout corresponding to the schematic in Figure 3.1 is presented in Figure 3.3, and gives a better understanding of the components' sizes and line lengths used. For reference, the transistors in the first stage are 150 µm wide, consisting of eight gate fingers. The design size is 2.2 mm by 1.9 mm.

The limiter is initiated and ended by 50 Ω transmission lines (TL_{init} and TL_{end}) since that is the impedance to which the limiter is matched. The exact lengths are not of much importance since they mainly provide a phase shift in addition to what is introduced by the lines within the limiter. The phase will have to be compensated either way, so this small addition should not make much difference. For convenience, they are made as short as possible. Between the stages, the lines (TL_{1-3}) are intentionally made thinner to increase their inductance, which helps with the matching of the limiter. The length of the lines has been chosen for minimum insertion loss within the $2-6$ GHz band.

The process of deciding transistor sizes starts in the first stage. The transistors are as large as possible to survive as much power as possible, and to reduce the on-resistance of the first stage. The number of transistors, three, was chosen based on the reasoning that adding more transistors would reduce the limiting ability too much, and as a result, the leakage would exceed the requirement. Fewer than three rises the capacitive effects, and reduces the power handling. While it is difficult to determine a specific power that the limiter can survive, it can be assumed that it should be able to survive around 100 W since a multi-shunt limiter with four branches with two transistors in each stage using the same technology can survive up to 450 W [5]. If a shunt-limiter with only one branch with two transistors were to be used, it can be assumed that it would be able to handle one-fourth of this power, or roughly 100 W. The referenced design does, however, use diodes for activation, similarly to what is used in the next chapter, which turns on the transistors more efficiently. In this self-activated limiter, the transistors become less turned on and are thus more resistive. More of the power can therefore be assumed to be dissipated, and the use of three transistors in series gives an additional margin. As seen in the results later, maximum power is not the primary shortcoming of the limiter. The second

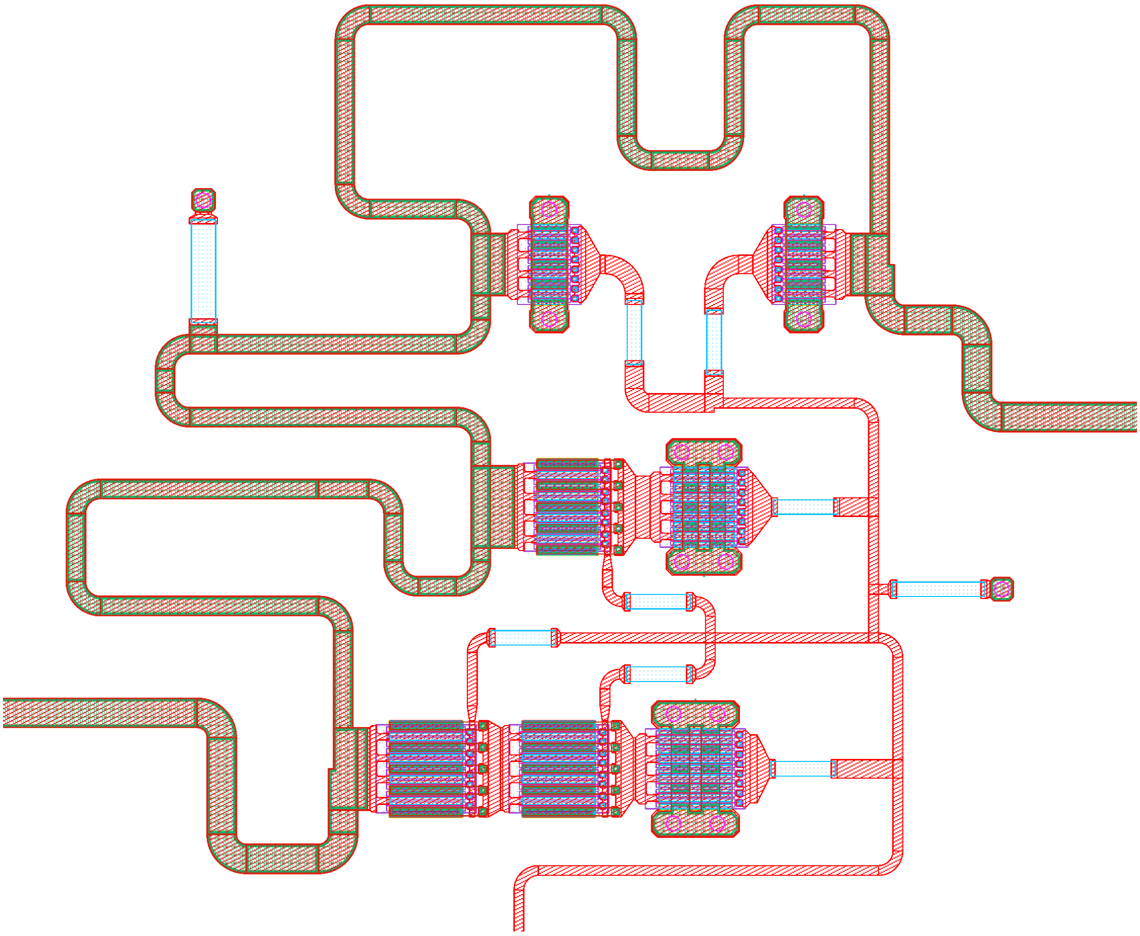


Figure 3.3: The layout of the suggested self-activated limiter.

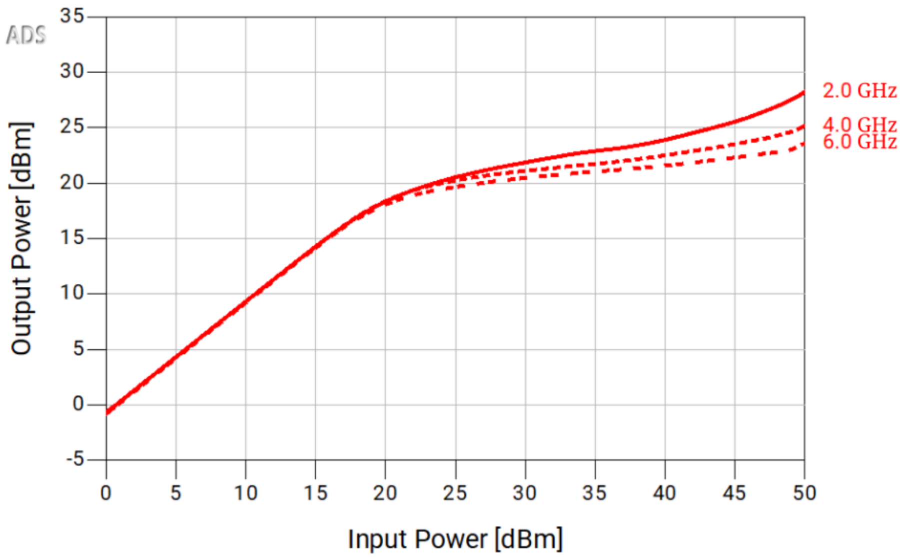


Figure 3.4: Leakage of the self-activated limiter for different frequencies.

stage uses two transistors to keep survivability without sacrificing the limitation too much. The last stages are introduced to make the power response flatter, thereby lowering the leakage. They are small to reduce the intrinsic capacitance. The bias voltage chosen for this limiter is $-4\,\mathrm{V}$.

3.4.2 Performance

The leakage of the self-activated limiter is presented in Figure 3.4. The most interesting thing to observe in this graph is the strong frequency dependence. The requirement of a leakage below 25 dBm is fulfilled for frequencies of 4 GHz, but for frequencies below this, the leakage is slightly higher. The main reason for this is the short electrical distance between the stages. For ideal limitation, the phase shift should be 90°, and the presented lines are much shorter. When the proper phase shift is added between the stages, the limiting performance is significantly improved for lower frequencies, at the expense of small-signal bandwidth. The initial choice of line lengths was made to keep the low-pass response of the turned-off limiter as good as possible for the specified frequency range, and this increase in line length reduces the cutoff frequency. Since the transmission lines are closer to 90° for the higher frequencies, the limitation improves, as observed in the figure. Another, less significant reason is the intrinsic capacitor that helps activate the transistor. Capacitors become more conductive at higher frequencies, and thus, a high-frequency signal will more easily reach the gate of the transistor. It should be possible to improve the activation of the transistors by adding additional capacitors between the drain and gate, but since the capacitive effects in the transistors are the main reason for a limited bandwidth, adding more capacitors would reduce the bandwidth further and has thus not been considered an option for this design.

The bias choice of $-4\,\mathrm{V}$ was determined to be the optimum given the presented requirements. To get a better understanding of why, the leakage of the limiter for a few bias voltages is presented in Figure 3.5. A stronger bias significantly raises the

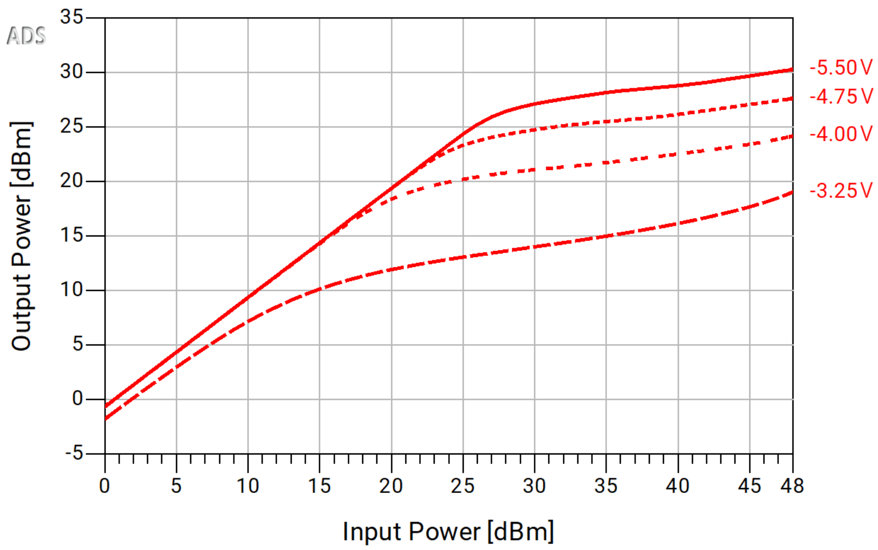


Figure 3.5: Power response of the self-activated limiter at 4 GHz for different applied bias voltages.

leakage, rendering the limiter less effective. The reason for not adding a weaker bias is seen in the linear region of the graph. The insertion loss increases quickly with a rise in voltage, reducing the usefulness of the limiter from a small-signal standpoint.

In Figure 3.6, the insertion loss for the limiter is presented. It fulfills the requirement of staying below 1 dB, but at both 3 GHz and 6 GHz, it is large enough to result in poor performance. In Figure 3.7, the return loss is presented. This fulfills the requirement with a good margin.

The transient response of the limiter is presented in Figure 3.8. It is clear that the leakage is slightly higher for the first 10 ns, but later settles on a constant value. This higher leakage is not large enough to cause problems with breakdown and is short enough to be negligible in terms of thermal handling. The models do not include all time-dependent effects in the transistors, such as the aforementioned trapping effects. Therefore, measurements would need to be made to obtain a good description of how it works in practice.

The conclusion is that the limiter does not fulfill the requirement of limiting ability within the entire frequency band. The insertion loss is within the specified requirement, but the margin is very small. These problems are solved by improving the activation of the transistors through the addition of diodes. This approach is presented in the next chapter. The only drawback to that design is that it requires a slightly larger total area; however, the performance is significantly improved.

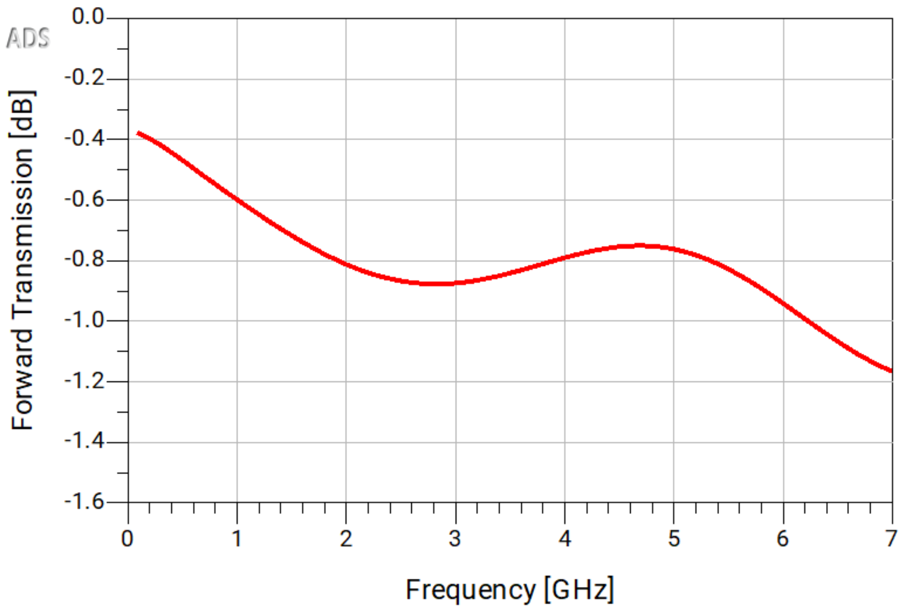


Figure 3.6: Insertion loss of the self-activated limiter.

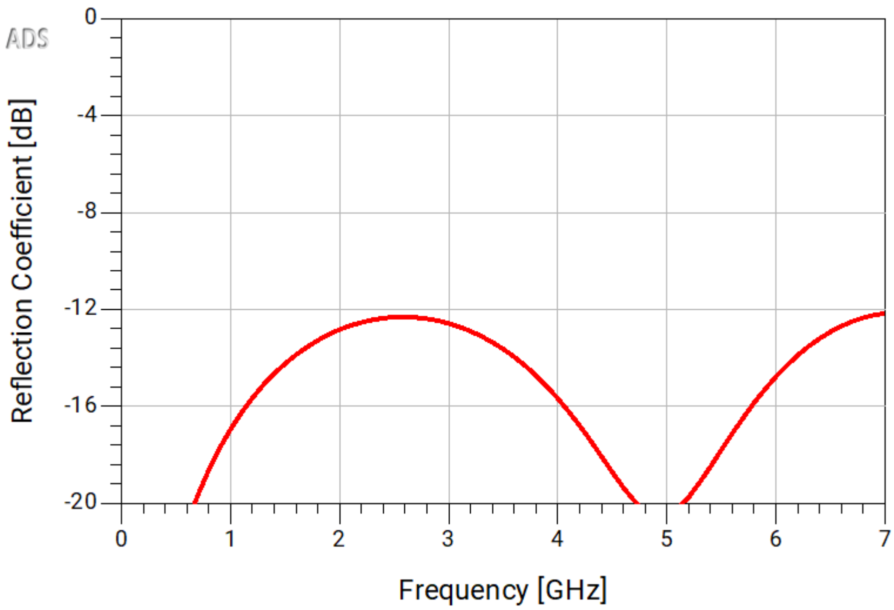


Figure 3.7: Return loss of the self-activated limiter.

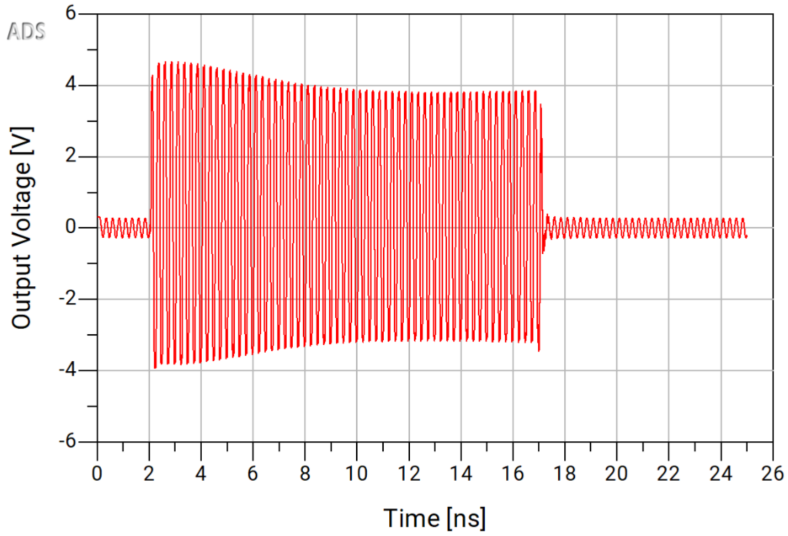


Figure 3.8: The transient response of the self-activated limiter for a 15 ns pulse of 40 dBm at 4 GHz.

4
Diode-activated Transistor Limiters

The limiters covered in this chapter are similar to the ones mentioned previously. While the activation process of the transistors in the self-activated case is entirely based on properties within the physical transistor, the diode-activated limiter uses an added Schottky diode between the drain and gate that gets activated for large enough signals. An illustration of this in its most fundamental form is presented in Figure 4.1 and has been used in previous works [5]. The diodes work in addition to the internal parasitics to more effectively activate the transistors, thereby achieving a better, flatter response.

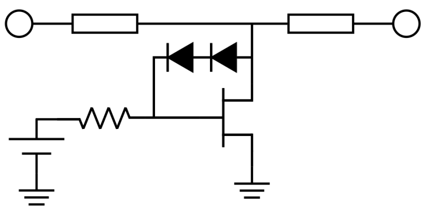


Figure 4.1: The simplest version of a diode-activated transistor limiter.

4.1 Design Considerations

In general, the process of dimensioning transistors and transmission lines is the same as in the self-activating case. In addition to this, there is a choice of diode number and size. The diodes used in this process are Schottky diodes. The gate lengths are made short to reduce size and parasitic capacitance. The powers passing through the diodes are small by design, so a small size should not be problematic from a thermal perspective.

The diode determines the possible bias voltages. From a DC simulation, it seems like the diode starts conducting at a forward bias of 2.8 V. If one diode is placed between the drain and gate, the bias at the gate can not be much lower than −2.8 V since DC would be conducted, leveling out the bias to this value. The threshold can be lowered by adding multiple diodes in series, each adding 2.8 V. Just like in the self-activating case, a lower bias means less parasitics from the transistors, but also a higher leakage. Thanks to the diodes, the bias can be lower without increasing the leakage as much. This effectively turns the transistors off, reducing capacitive

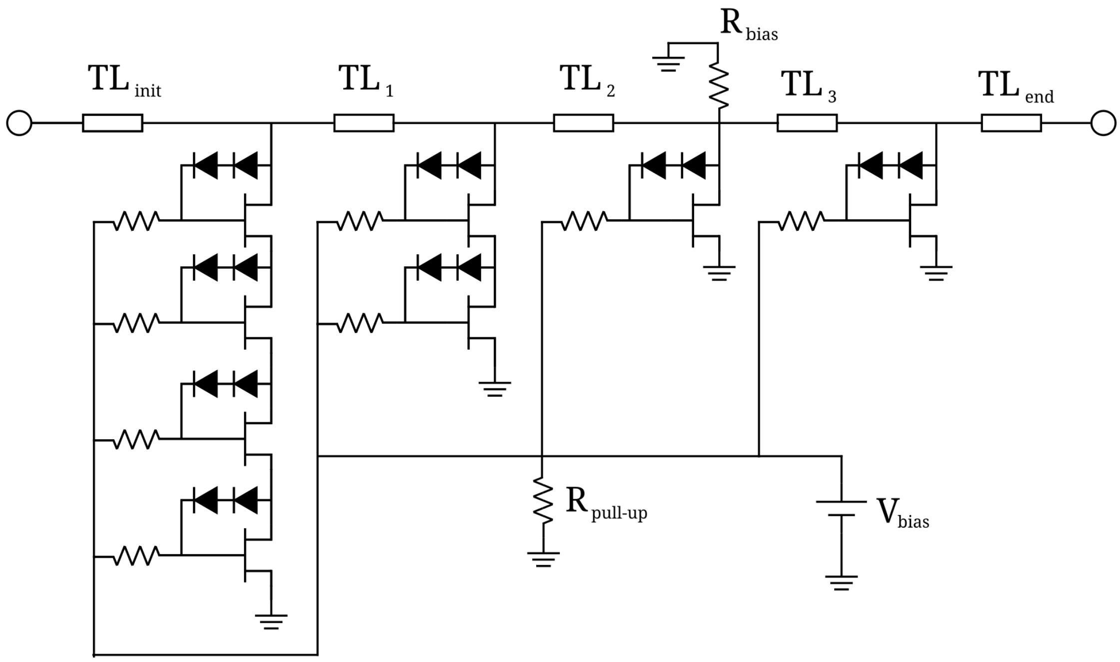


Figure 4.2: Schematic of the suggested diode-activated limiter.

effects. The diodes add to the parasitics, but the benefit of the lowered bias still makes it better than the self-activated limiter in terms of insertion loss.

4.2 Design Example

The design is similar to the self-activated limiter, but it requires a slightly larger area due to the presence of diodes. Since the activation of the transistors is improved, the size can be reduced while sustaining the amount of reflected power, which in turn reduces the transistor capacitances.

4.2.1 Schematic and functionality

The schematic of the proposed limiter is presented in Figure 4.2, and the corresponding layout is presented in Figure 4.3. Compared to the self-activated design, there are many similarities. The overall layout of the transistors and the number of stages are the same. The total size is 2.8 mm by 2.1 mm.

When it comes to transistor dimensioning, the main procedure is the same as for the self-activated limiter. The difference is that the transistors are activated more efficiently, and that the size of the transistors is of slightly less importance from a leakage standpoint. This is mainly noticed in the last two stages, where the transistors are smaller than in the self-activated case. In the first stage, it is also possible to add a fourth transistor while keeping the leakage below the required level. This allows for better survivability.

The bias is chosen to be -5.5 V, which is the lowest bias that is possible when using two diodes in series. Three diodes would raise the leakage too much. Another

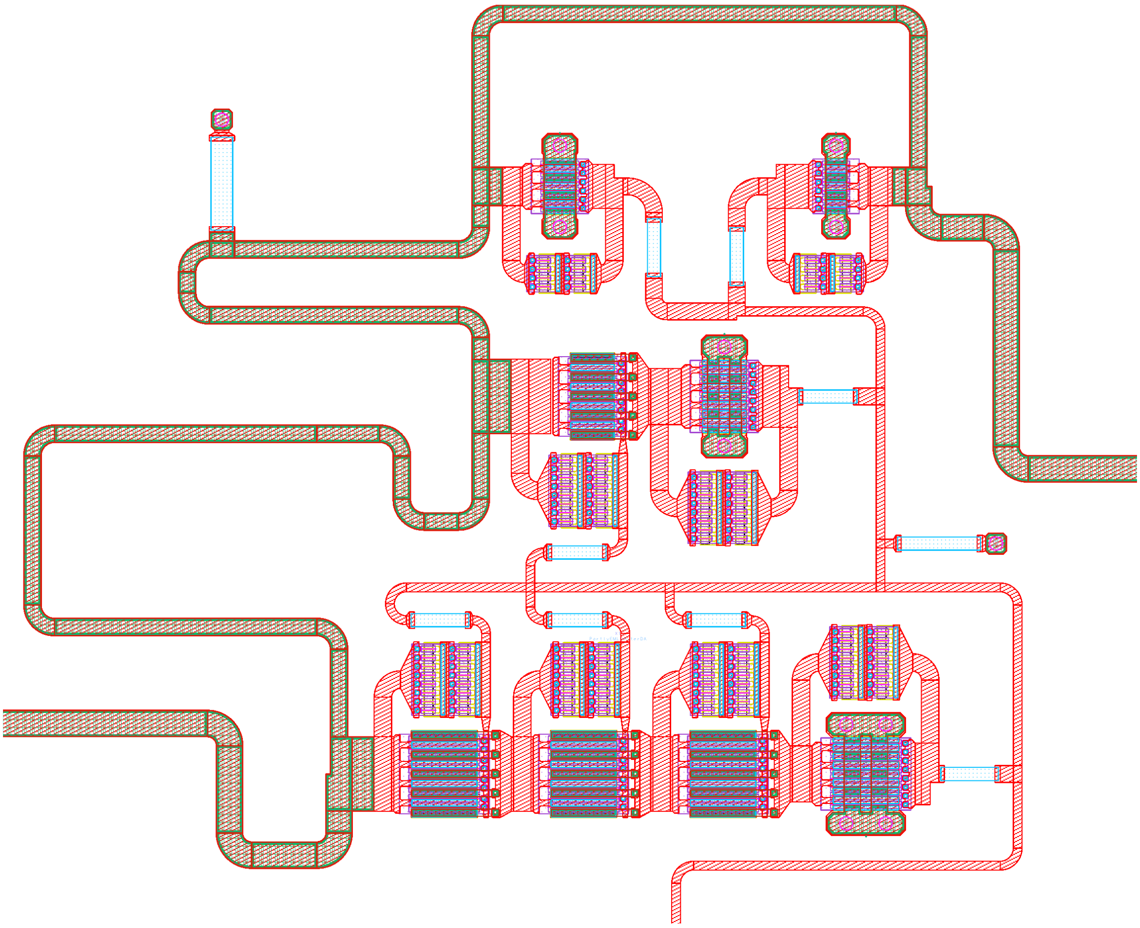


Figure 4.3: The layout of the suggested diode-activated limiter.

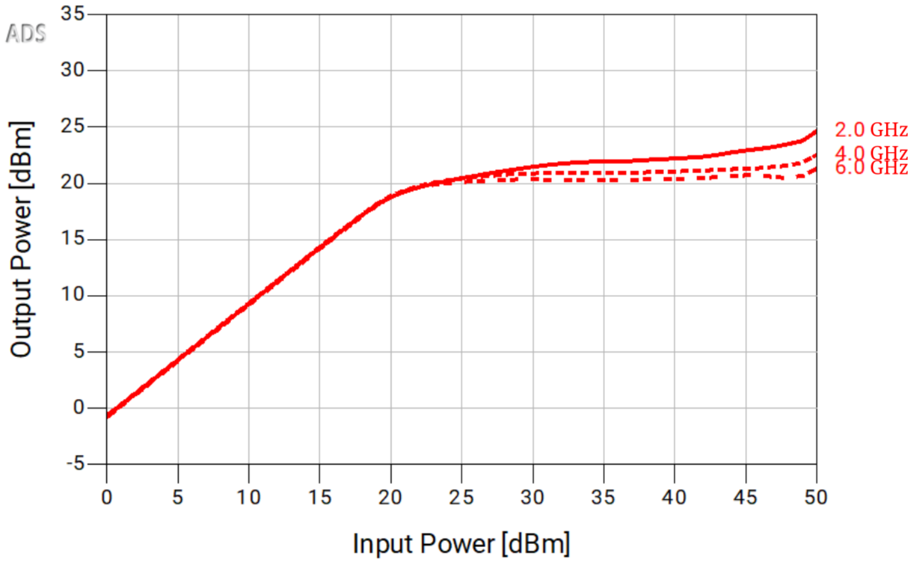


Figure 4.4: Leakage of the diode-activated limiter.

benefit of using two diodes is that they can be made the same total width as a maximum-sized transistor, and thus fit well in the layout.

4.2.2 Performance

In Figure 4.4, the leakage of the diode-activated limiter is presented. Compared to the self-activated limiter, this performance is superior. The response is flat, and below 25 dBm for up to 100 W. Using the same reasoning as in the previous chapter, the limiter is likely to survive powers above 100 W. The frequency dependence on the leakage is apparent, but significantly reduced compared to the self-activating limiter. The reason for the frequency dependence is, as before, the use of short transmission lines between the stages. These are well below quarter wavelength for 2 GHz, and thus the activation is less than optimal. While the diodes reduce the needed voltage rise for turning the transistors on, the longer electrical lengths for the higher frequencies will still result in better activation.

Similar to frequency, the bias dependence for leakage is much reduced compared to the self-activated case. As expected, decreasing the voltage below −5.5 V makes little difference due to the static voltage drop of the diodes. The same holds for small-signal performance, where no improvements are seen for stronger biases.

In Figure 4.6, the insertion loss for the limiter is presented. It is much better than the self-activated limiter. The return loss, however, presented in Figure 4.7 is slightly worse than for the self-activated. This reduction in insertion loss, despite an increase in reflection, indicates a decrease in losses due to dissipation. This is expected because of the stronger bias applied. The diode-activation allows for better turned-off devices, resulting in less current passing through them, which in turn reduces losses through the transistors.

The transient response of the limiter is presented in Figure 4.8. Similarly to the self-activated limiter, there is a brief period during which the leakage is slightly higher. For this circuit, however, the time is much shorter, and for a couple of

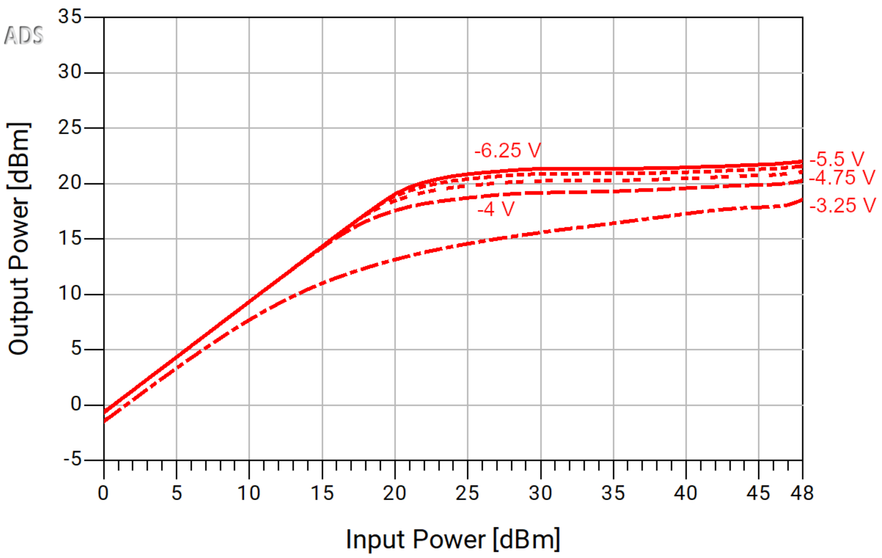


Figure 4.5: Power response of the diode-activated limiter at 4 GHz for different applied bias voltages.

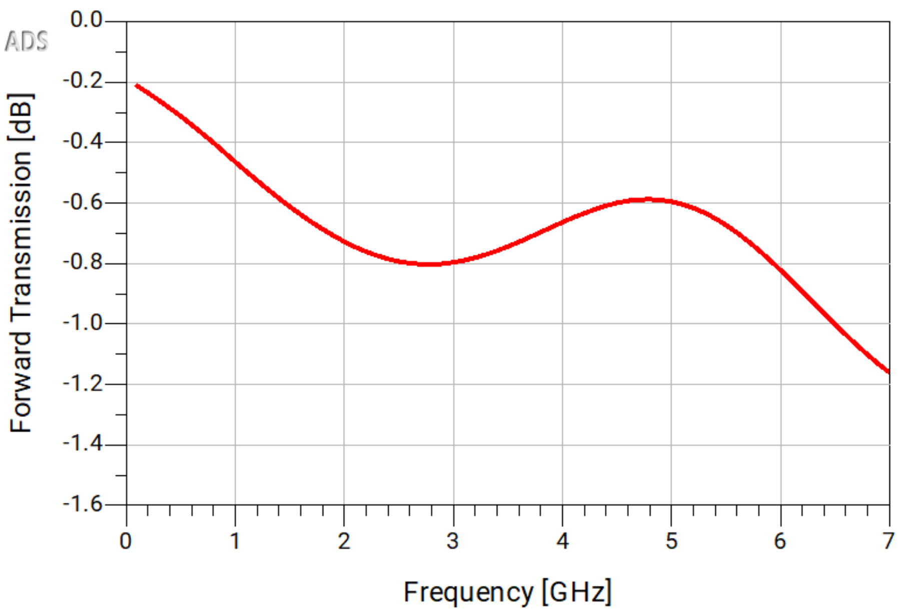


Figure 4.6: Insertion loss of the diode-activated limiter.

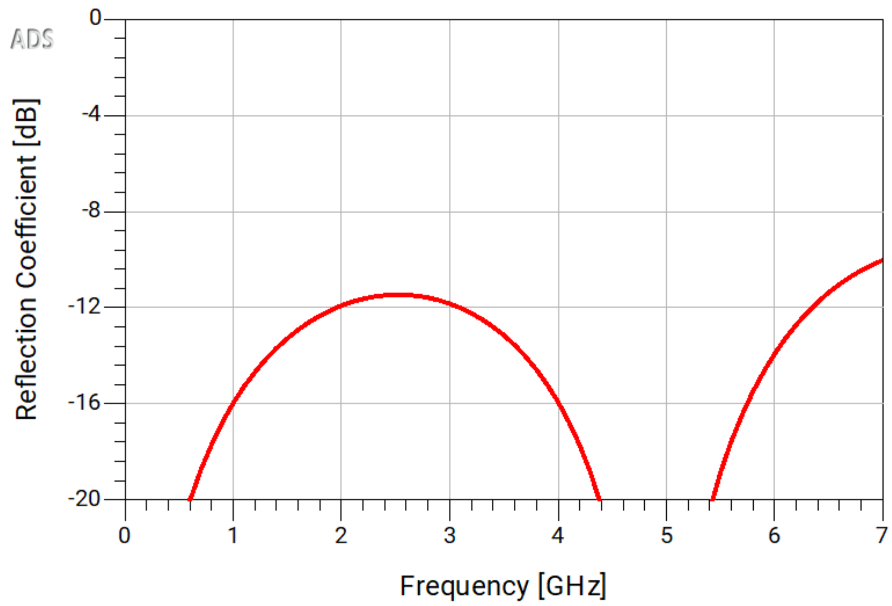


Figure 4.7: Return loss of the diode-activated limiter.

Table 4.1: The diode-activated limiter compared to previous MMIC limiters. The maximum power described is the power at which the leakage is measured.

Technology	Size [mm]×[mm]	Leakage [dBm]	P_{max} [dBm]	BW (max. IL) [GHz] [dB]	Source
GaN	2.8 × 2.1	24	48	2-6 (0.83)	This Work
GaN	2.1 × 1.1	25	46 (CW)	1-6 (0.5)	[6]
GaN	2.5 × 2	19	56	2.6-3.6 (0.6)	[5]

nanoseconds, the leakage becomes lower than the steady-state leakage. Again, the peak voltage is only slightly higher than the steady state, and the time is short enough to avoid thermal problems. Measurements would have to be carried out to verify this behavior. After the pulse, there are a couple of nanoseconds where the signal is lower than in steady state, similarly to when the pulse first reaches the limiter. The two behaviors are likely related since they are working at the same timescales, and neither of them is present in the self-activated limiter. However, no further analysis has been made to determine why these behaviors arise.

Out of the two complete GaN limiters presented in this thesis, the diode-activated alternative is better. To see how it holds up to the other GaN limiters found in literature, a comparison of the main parameters is shown in Table 4.1. An important comparison is between the diode-activated limiter designed in this work and the $1-6$ GHz detector-activated alternative found in [6]. That limiter offers much better insertion loss at a slightly better bandwidth. It can, however, not handle as much power, and the need for an external detector greatly increases the complexity. This is discussed further in the next chapter.

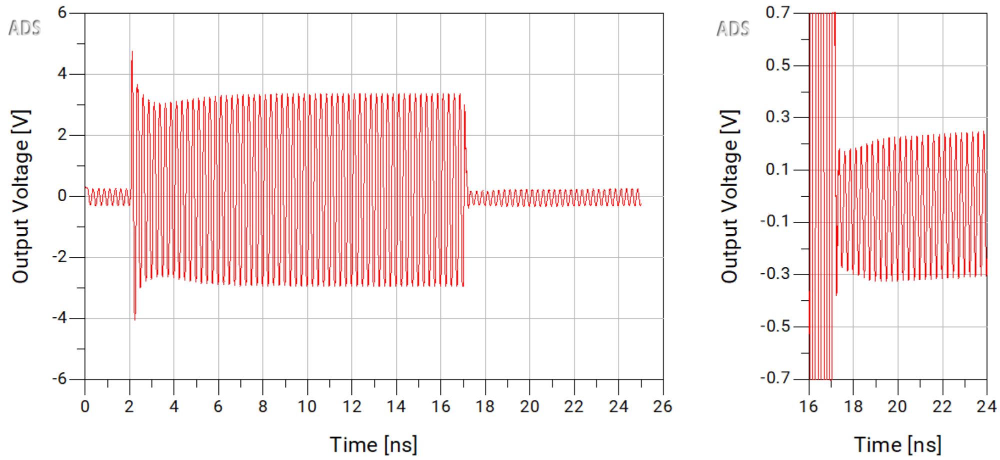


Figure 4.8: The transient response of the diode-activated limiter for a 15 ns pulse of 40 dBm at 4 GHz, along with a magnification of the response after the pulse.

5 Detector-activated Transistor limiters

By introducing external activation of the transistors, several improvements can be achieved over limiters that respond directly to the signal. One notable advantage of using detectors is the increased freedom in the choice of bias voltages. When limiting, the transistors can be completely turned on, increasing the amount of reflected power. Otherwise, the bias can be chosen to turn off the transistors as well as possible, enhancing small-signal performance. Additionally, this approach enables the implementation of series transistors that function as switches, turning off when the input power exceeds a predetermined threshold. The example circuit discussed here incorporates both series and shunt transistors.

5.1 Principle of operation

The design outlined in this chapter consists of three stages, the first being a series stage, while the subsequent two are shunt stages. This configuration is heavily influenced by the best-performing wideband GaN limiter known to the author [6]. Due to the different types of stages, two distinct biasing schemes are required. When the signal strength reaches a certain threshold, the series transistors must be turned off, while the shunt transistors need to be activated. Consequently, a bias network is necessary to process the output from the power detector, generating two complementary signals.

5.2 Detector considerations

There are two approaches to implementing the detection functionality. Either the detector is integrated on the same chip, using the same technology as the limiter, or it can be an external component mounted on the receiver circuit board. The external detector, however, is not a good option, as the primary reason for creating an integrated GaN limiter is to add more functionality to an existing chip. If more components have to be added, simply adding an external limiter offers greater flexibility.

The main drawback of the detector-activated limiter is the added complexity. The first problem is to read the power without interfering with the signal. The detection should, ideally, behave the same for all frequencies. It is difficult to couple part of the signal into the detector in a wideband manner. This reading of the signal will also degrade the small-signal performance. After the signal is detected and converted into DC, it should be amplified and shifted in a way that makes it suitable for biasing the transistors.

A performance issue is the detector's response time. A detector that generates a DC from a radio signal will likely take some time to adjust, both when rising and falling, which leaves room for potential spike leakage in the rise of the signal, and might render the receiver useless for some time after the signal has faded before the limiter is again turned off. Since no detector has been designed, no useful transient simulations can be performed, however.

5.3 Design

The presented design is not a complete limiter. It is merely a switch that can be turned on and off based on some detector output. The author has been unable to design a detector that can be used for biasing the transistors.

5.3.1 Schematic and functionality

A conceptual schematic of the limiter is presented in Figure 5.1. One can easily see the close resemblance between the last two stages and the self-activated limiter. This time, however, the bias to the transistors is not constant. While some self-activation may occur during operation, it should be negligible compared to the effect of changing the bias according to a detector.

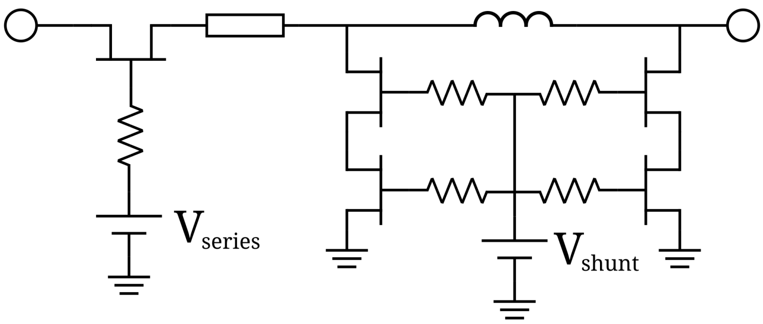


Figure 5.1: Schematic of the suggested detector-activated limiter.

The layout of the circuit is presented in Figure 5.2. The total design size is 2 mm by 1.2 mm. The first transistor is as large as the design kit allows. The reason for having it large is both to improve power handling and to reduce the on-resistance. The on-resistance in this limiter is of greater importance than for the previous designs. While a low on-resistance was important for the shunt limiters to improve the reflection while limiting, the on-resistance here directly corresponds to small-signal loss.

One potential limitation of this topology is self-activation behavior in the series transistor. If the signal strength becomes large relative to the bias, the same self-activation behavior that was seen before will happen here. While self-activation

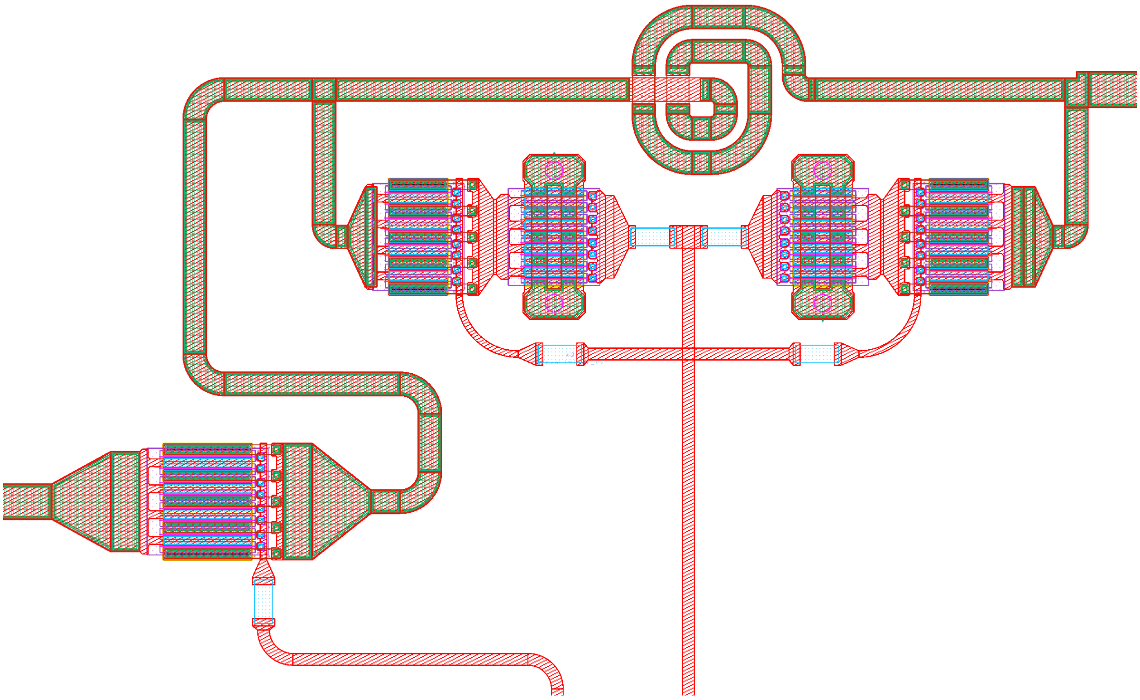


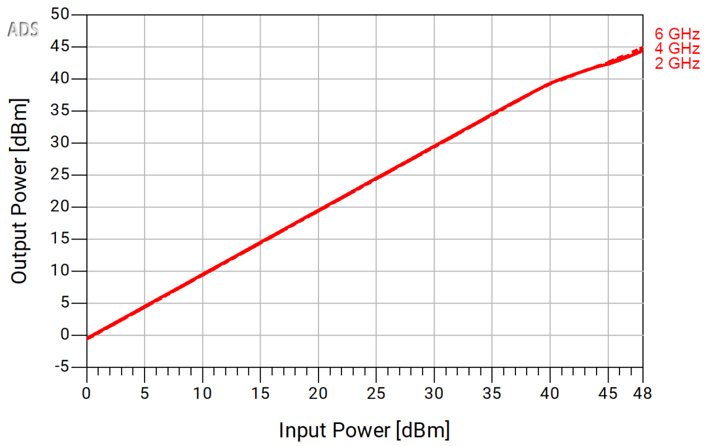
Figure 5.2: The layout of the suggested detector-activated limiter.

helps in a shunt limiter, turning the series transistors on for large powers when limiting would worsen the limiting effect.

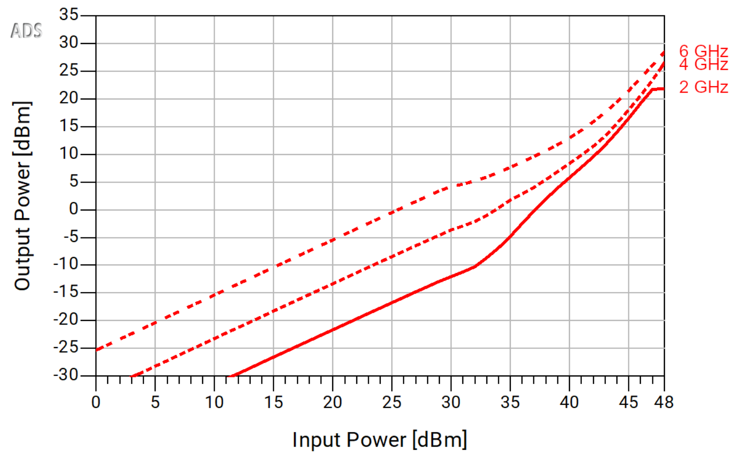
5.3.2 Performance

Since the detection network for this design is separate from the simulated circuit, it is not possible to present performance in terms of leakage. The power response directly depends on the detection and bias network, and can be shaped according to the designer's ability. However, by examining the power response of the limiter when turned off (Figure 5.3a) and activated (Figure 5.3b), it is possible to determine the physical performance limit. In the non-limiting case, the series transistor is biased at 0 V (V_{series} in Figure 5.1) and the shunt transistors (V_{shunt} in the figure) are kept at −12 V. In Figure 5.3a, there is no apparent large signal behavior until after 35 dBm. This is well above the 25 dBm leakage requirement, so there should not be any performance problems in this mode of operation.

When limiting, the bias voltages are switched, so that the series transistor is biased at −12 V and the shunt at 0 V. Here it is seen that the limiter exceeds the leakage requirement at around 47 dBm of input power. This is thus the maximum input power of this limiter. It is interesting to note that, contrary to the other limiters in this work, the highest frequency determines the leakage. This is likely the result of two aspects. First, since using an external biasing, the line lengths between stages do not affect the activation. Secondly, the shunt transistor, which is turned off while limiting, will conduct better for higher frequencies since it is slightly capacitive, resulting in worse limitation from this stage.



(a) Not Limiting



(b) Limiting

Figure 5.3: The large signal behavior of the detector-activated limiter when fully turned on and off.

Assuming the voltage for turning the transistors off is −12 V and for fully activating them is 0 V, the insertion loss is what is presented in figure 5.4 and the return loss is presented in figure 5.5. Since the insertion loss for the low frequencies is rather high, even though the return loss is very low, it indicates that there is a resistive loss in the system. The frequency response is flat within the frequency range, so if it is possible to reduce these losses, the insertion loss could be significantly improved. It is considerably worse than the original, published version [6]. One reason for this is most likely the use of smaller transistors. While the sizes of the series transistors used in the paper are left unsaid, the image of the fabricated circuit indicates that the transistors are larger than the $8 \times 150\,\mu\text{m}$ simulated here. There are likely other details that reduce the performance of the presented detector-activated limiter that have not been taken into consideration. No in-depth analysis has been conducted to optimize the concept's performance. Even if there is a way to improve the performance of this circuit, the design presented in the previous chapter was easier to implement with reasonable performance, with the benefit of being complete without the need for external circuitry, apart from the constant bias.

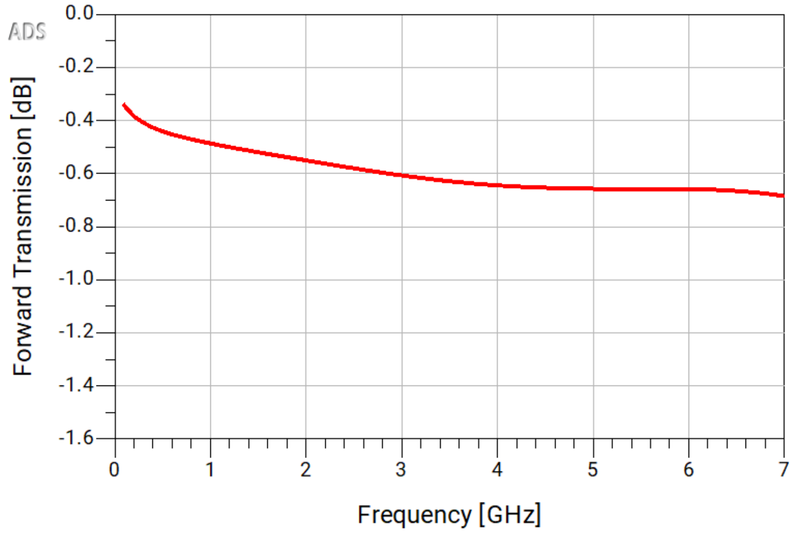


Figure 5.4: Insertion loss of the detector-activated limiter.

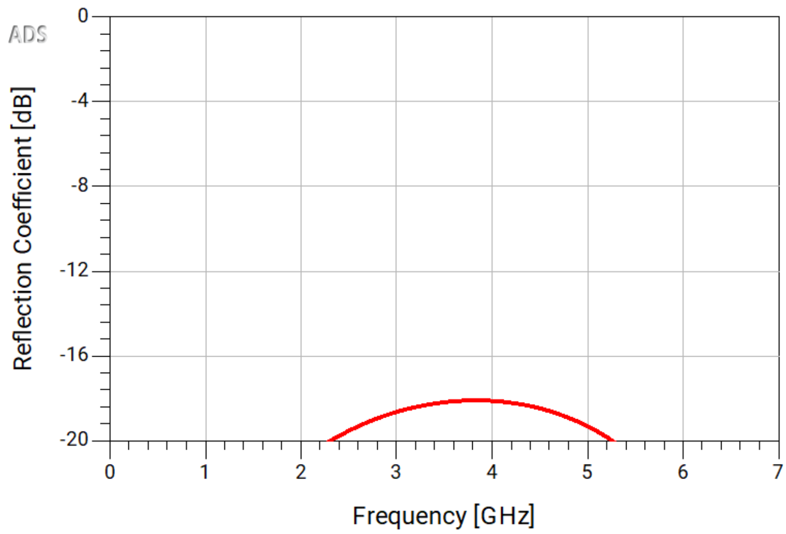


Figure 5.5: Return loss of the detector-activated limiter.

6

PIN Diode Limiters

Diode limiters are the most common type of limiters, both in integrated circuits and using discrete components. To gain insight into how the previously presented transistor limiters compare to their more traditional diode counterparts, an attempt has been made to design an integrated PIN diode limiter. To achieve the previously mentioned benefit of integrating the limiter with the LNA, a GaAs technology featuring both PIN diodes and HEMTs has been used, specifically WIN Semiconductors' PIH1-10.

6.1 Principle of operation

Diode limiters work much like the transistor shunt limiters. When the power is sufficient, the diodes begin to conduct. The main difference between the PIN and transistor shunt topologies in this work, apart from the difference in components, is that each stage has one branch that conducts for large positive voltages and one for negative voltages, as shown in Figure 2.4. It is thus better at limiting the signal.

Because of the lower on-resistance, the amount of absorbed power relative to the incoming signal strength is lower, reducing the requirement on thermal handling in the diodes. The specific amount of power that the diodes can handle is unknown. The maximum currents are specified, but it is difficult to determine the thermal behavior. GaAs is a poor heat conductor [13], so the diodes are likely to heat up fast when being used.

Compared to transistor limiters, the diode size does not significantly affect leakage because of its low resistance. The largest effect of diode size can be seen at 18 GHz, presented in Figure 6.1. At 2 GHz, where the leakage is the largest, the three diode sizes yield practically identical results. The main reason for increasing the size is to increase survivability. The increased size also affects the parasitics of the limiter. A larger diode is more capacitive, as was the case with transistors. What mainly affects the leakage and power handling in the PIN diode limiter is the electrical distance between the stages. In traditional, narrow band limiters, the distance between stages is a quarter wavelength to make them as effective as possible. Again, the concept of quarter wavelengths loses its meaning as the bandwidth increases, but simulations reveal that longer transmission lines between stages result in better limiting behavior. The drawback is that longer transmission lines reduce the bandwidth. Since the device size is of less importance, the design process of PIN diode limiters is simpler than that of a transistor limiter. The sizes cannot be ignored, however, since there is a requirement for maximum power. The diodes must

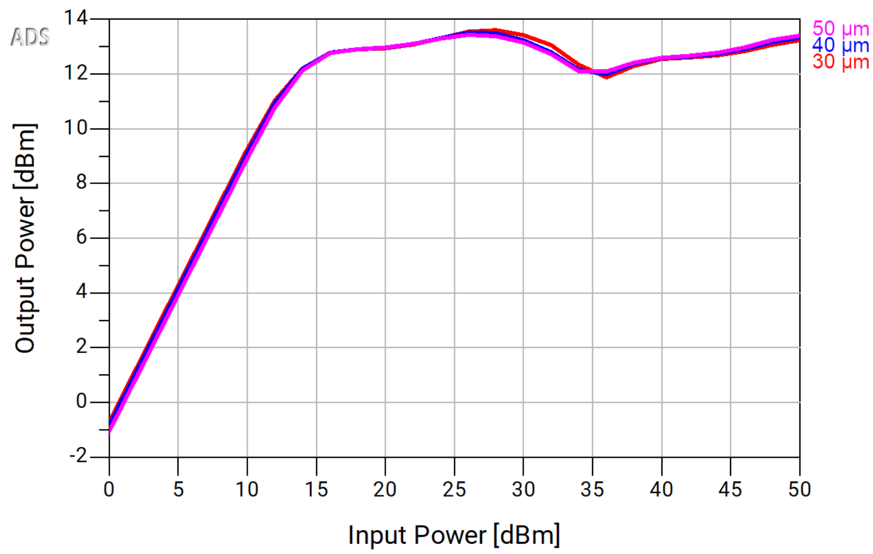


Figure 6.1: The power response of the PIN diode limiter at 18 GHz for square diodes in the first stage with side lengths of 30 µm, 40 µm, and 50 µm.

be scaled accordingly, and as a result, the bandwidth decreases when the limiter is designed for higher powers.

6.2 Design Example

A simple PIN diode limiter is presented. The purpose is both to assess its performance in terms of bandwidth and to understand how the design challenges differ from the transistor limiters.

6.2.1 Schematic and functionality

This limiter has been designed to operate in the wide $2-18$ GHz band, compared to the GaN limiters that were only designed for $2-6$ GHz. The schematic for the diode limiter is presented in Figure 6.2, and the layout is found in Figure 6.3. The design resembles traditional diode limiters. The primary difference lies in the addition of capacitors surrounding the second stage. The capacitors help to reduce the insertion loss more evenly across the wide frequency band, and are especially important for the higher frequencies. It increases the return loss for the lower frequencies that are blocked by the capacitors, but since the band was specified as a design requirement, achieving a good insertion loss for the higher frequencies is a higher priority than including the lower frequencies. The layout size is 2.4 mm by 0.65 mm. Looking at the figure, it should be obvious that this is by no means the most compact way of laying out the transmission lines, and that it should be possible to make it significantly smaller. The main reason for having the current transmission line shapes is to allow for easy evaluation of the effects of different length lines.

The reason why the capacitors help with the matching is currently unknown, but some observations can be made from simulations. The capacitors seem to move

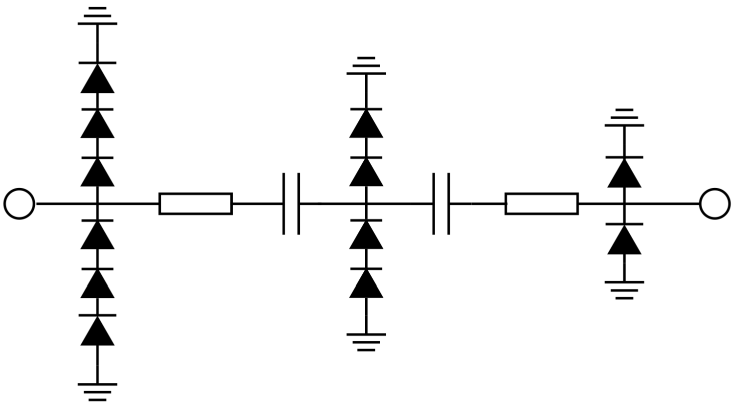


Figure 6.2: Schematic of the suggested PIN diode limiter.

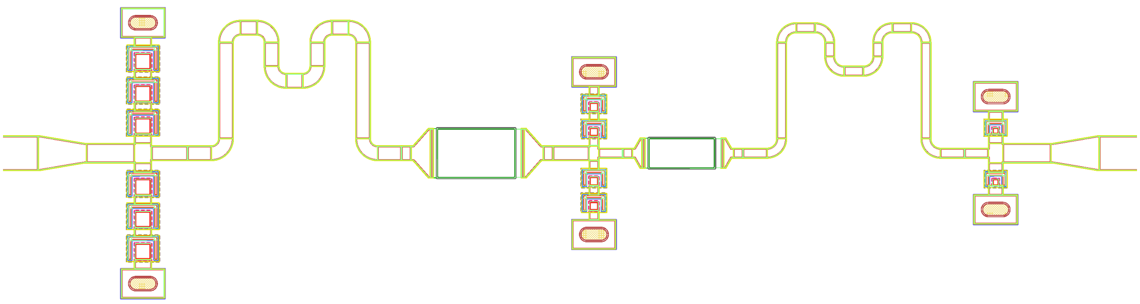


Figure 6.3: The layout of the suggested PIN diode limiter.

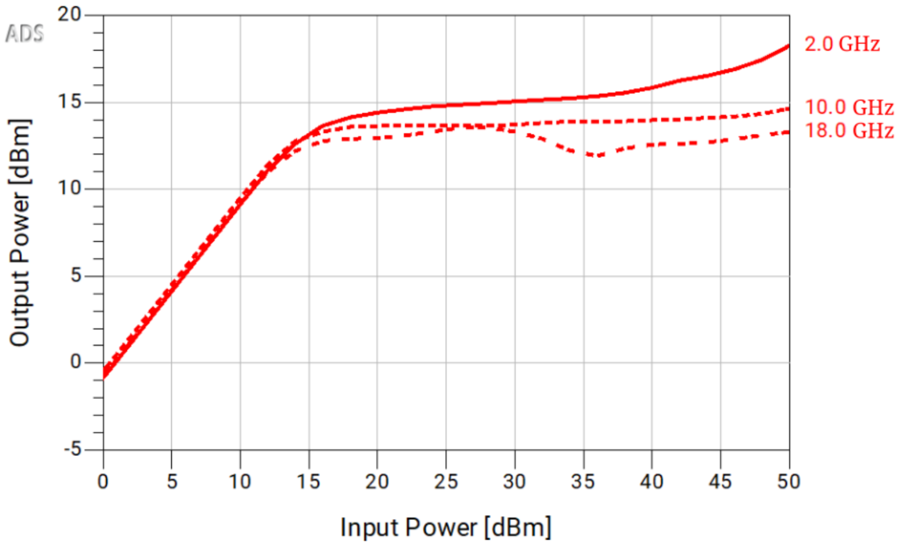


Figure 6.4: Leakage of the PIN diode limiter.

power dissipation from the first to the second stage while limiting. A larger capacitor yields a better (more even) frequency response, but the absorbed power in the second stage is also increased, resulting in either improved or degraded power handling, depending on how the stages have been scaled with respect to each other. A small enough value has to be picked to avoid too much power entering the second stage.

6.2.2 Performance

The Leakage from the PIN diode limiter is presented in Figure 6.4. It exhibits a flat power response and maintains the leakage below 18 dBm for input powers up to 48 dBm, which meets the specified requirement for a GaAs process. It is questionable whether the limiter itself can withstand such large powers, since no information is provided on this. In case it does, it has good coverage in terms of leakage.

In Figure 6.5, the insertion loss is presented. The goal of keeping the insertion loss below 1 dB is fulfilled with a good margin. To compensate for potentially optimistic models in higher frequencies, some margin is added above 18 GHz. The goal of keeping the return loss below 10 dB is unfortunately not fulfilled for the lower frequencies, which can be seen in figure 6.6. For higher frequencies, the insertion loss increases while the return loss is kept low. This suggests that there are losses in the system and that it is likely challenging to achieve higher bandwidths using the presented limiter topology.

The transient response of the limiter is presented in Figure 6.7. Surprisingly, there is no noticeable transient behavior for this limiter in the simulation. Some transient behavior is to be expected in all circuits, but in this case, that will have to be determined from measurements.

Similarly to the diode-activated limiter, the PIN diode limiter designed in this thesis is worse than what is found in literature in terms of insertion loss, which can be seen in the design comparison in Table 6.1. It does, however, offer an improvement in bandwidth and potentially in maximum power, depending on thermal behavior.

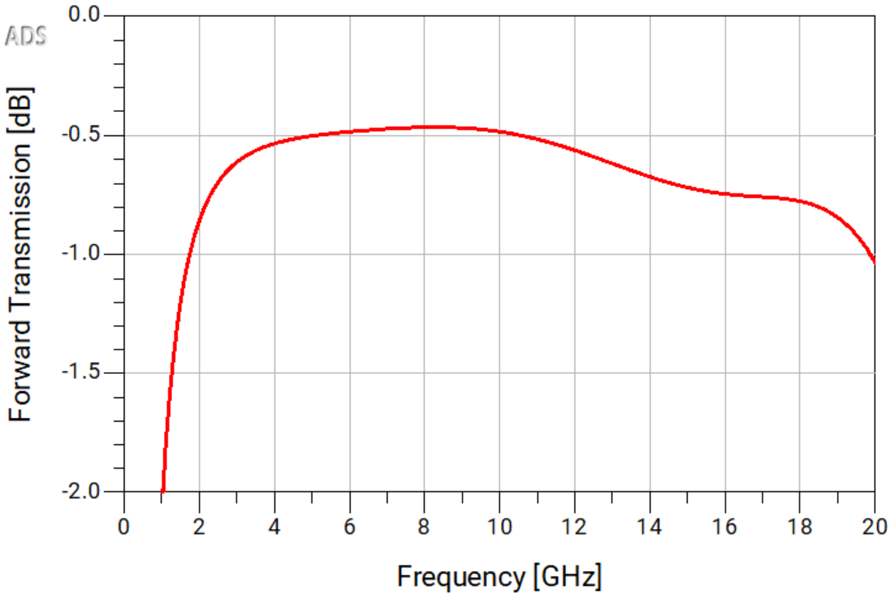


Figure 6.5: Insertion loss of the PIN diode limiter.

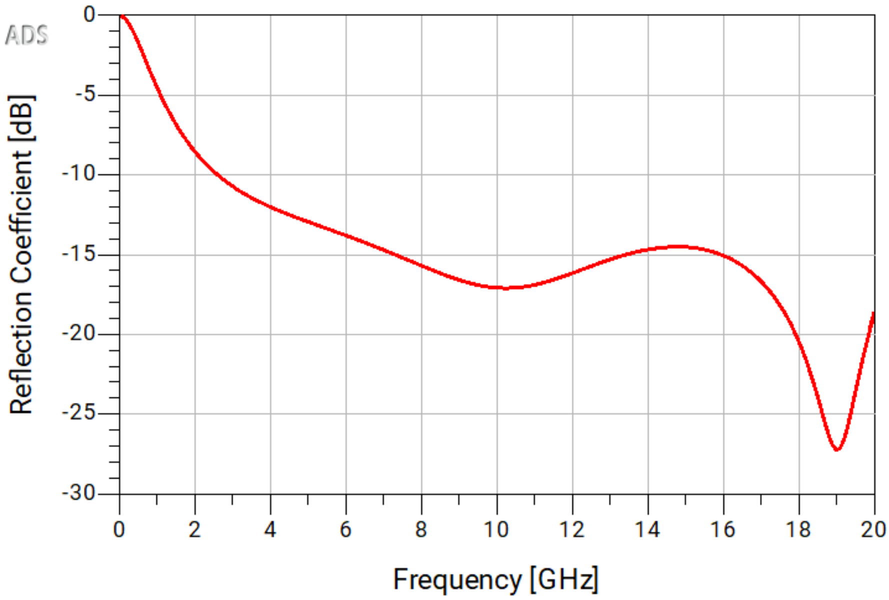


Figure 6.6: Return loss of the PIN diode limiter.

Table 6.1: The PIN diode limiter's performance in relation to similar MMIC limiters. The maximum power described is the power at which the leakage is read.

Technology	Size [mm]×[mm]	Leakage [dBm]	P_{max} [dBm]	BW (max. IL) [GHz] [dB]	Source
PIN+GaAs	2.4 × 0.65	17.5	48	2-18 (0.8)	This Work
PIN+GaAs	1.5 × 0.8	16	56	10-18 (0.55)	[11]
PIN+GaAs	1.1 × 0.7	15	40	0-18 (0.45)	[22]

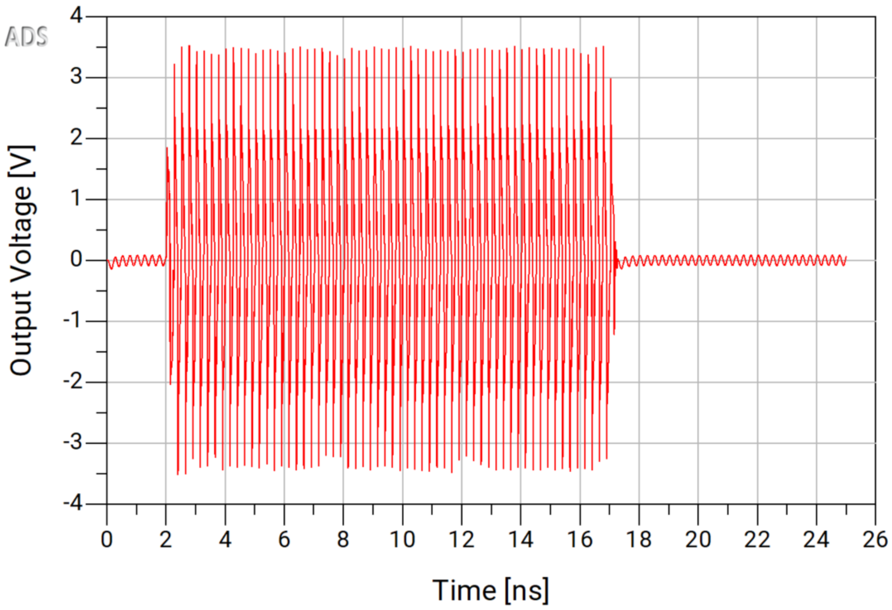


Figure 6.7: The transient response of the PIN diode limiter for a 15 ns pulse of 30 dBm at 4 GHz.

7

Conclusions

When designing a limiter, there are mainly three aspects that have to be decided upon. The first is how much power can be allowed to pass through the limiter, referred to as the leakage. Secondly, the worst acceptable small-signal behavior has to be determined. Since the limiter is introduced first in the receiver chain, it has a significant impact on system performance; therefore, this requirement must be set carefully. Being too strict on small-signal will, however, narrow down the possible achievable frequency band. Lastly, the maximum power capacity should be decided. Higher input power requirement calls for more and larger limiting devices, which in turn reduce the bandwidth. The bandwidth is a result of all other requirements. If the bandwidth does not meet system requirements, some compromise must be made with another requirement.

The designs presented in this thesis show promising results, as shown in Table 7.1. First, two similar and complete GaN limiters were presented. The first used internal effects in the transistor to achieve limiting. This design does not fulfill the given requirements, but still performs reasonably well. It can be compared to the second design, which is similar, with the main difference being that the transistors are activated using Schottky diodes. The addition of diodes improves activation, which both increases the limitation and allows for biases that better turn off the transistors, resulting in improved small-signal performance. The size increase resulting from the addition is relatively small compared to the performance improvement it brings. The limiters have acceptable small-signal behavior up to 6 GHz.

Another option is to activate the transistors using a dedicated detector. One limiter topology that requires a detector has been investigated. The results show that this limiter has the potential to perform similarly to the ones presented earlier, given an ideal detector. No design of a suitable detector has been presented, and it falls outside the scope of this thesis.

Table 7.1: The requirements and results of the four designed limiters.

	Max. IL [dB]	Min. RL [dB]	Bands [GHz]	Leakage [dBm]	Max. Input [dBm]
Requirement	1	10	2-6/2-18	25/18	48
Self-Activated	0.9	12	2-6	25	44
Diode-Activated	0.8	11	2-6	24	48
Detector-Activated	0.7	18	2-6	N/A	47
PIN Diode	0.8	8.5	2-18	17.4	48

Lastly, a limiter using PIN diodes was designed. This limiter outperforms the GaN transistors in all simulated aspects. The greatest improvement is seen in bandwidth, where this limiter works in the entire $2 - 18\,\text{GHz}$ band, although the lower frequencies show a slightly too high return loss. It is, however, likely that the limiter will be unable to withstand as much power before breaking. The required limiting behavior has been verified in simulation up to the specified maximum power, but whether the limiter will survive that power is questionable.

7.1 The Results' Role in Society

The designs presented in this work do not, in themselves, enable something that cannot be achieved in other ways, and therefore, the impact on society will be minimal. From an environmental viewpoint, it should be unimportant. If it were to be used, it would replace something that already exists, so the use of resources would not change significantly.

SAAB funds the thesis project, and the rights to all designs and results obtained as part of it are automatically transferred to the company. The primary business area of SAAB is defense materiel, and if the results of the master's thesis are to be used, it will be part of the defense industry. As a result, what is produced in this thesis may be used in products resulting in harm to people, buildings, or the environment, or in the prevention of it, depending on how it is used.

7.2 Future Works

To get the most out of this work, what should primarily be done is to have the circuits fabricated and measured. It would also be an option to first fabricate simple test circuits consisting of single limiter stages to determine what powers the devices can handle and validate the limiting behavior. Doing this could indicate whether anything is wrong and needs to be changed in the design. This would also be useful for future designs, since it would give a better understanding of each part of the design.

As mentioned in the sections on performance metrics, the linearity of the circuit is important from a signal standpoint. In-depth simulations and measurements will have to be made before the circuits are integrated with an amplifier. The results should be compared to the equivalent figure for the LNA, since it is likely that the linearity of the LNA is worse than that of the limiter.

The models used for simulating the transistor limiters are created with switching applications in mind. While the limiter mostly behaves like a switch for small signals, the activation behavior is not used in switching applications, and is, in that case, an unwanted effect. It would be good to have models that focus on the activation behavior. If transient behavior can be adequately modeled, that would also be valuable in determining activation behavior.

One aspect to investigate is whether it is possible to create a power detector and bias network in GaN that can be used for activating a limiter. If this is achieved, it will unlock higher bandwidths for detector-activated GaN limiters. While the detector-activated limiter presented here did not allow for higher frequencies than 6 GHz, a pure shunt-limiter with a detector will probably work better, since the capacitive and resistive effects in the turned-off transistors would be much lower, and the signal would not have to pass through an on-resistance of a series stage.

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