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Investigation of Harmonic Content in Chain-Link STATCOM With a Non-Integer Frequency Modulation Index

Master's thesis in Electric Power Engineering

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Abstract

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by Sabina Mesic

The technology around multilevel converters has emerged in the past decades and many new topologies have been introduced. Many multilevel converter topologies are equipped with floating capacitors which, if not controlled properly, face serious voltage imbalance issues. These issues are a result of the harmonic distortion in the output current and voltage. By proper choice of modulation technique, the harmonic performance of a multilevel converter can be significantly improved. One of the modulation techniques that improves the harmonic performance is the PS-PWM. However, this method does not eliminate the voltage imbalance issue that cause the capacitors to deviate, which leads to a need for additional individual balancing controllers. It has been concluded that a non-integer modulation frequency index significantly improves the imbalance problem by slowing down the deviation process during non-ideal conditions and almost completely preventing it during ideal conditions. In this thesis, the affect of a non-integer modulation frequency index voltage balancing in a modular multilevel converter with PS-PWM has been investigated. The harmonic behavior has been derived analytically and verified through PSCAD simulations.

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Abbreviations

FACTS	**F**lexible **A**lrernating **C**urrent **T**ransmission **S**ystems
FFT	**F**ast **F**ourier **T**ransform
IGBT	**I**nsulated **G**ate **B**ipolar **T**ransistor
MPCC	**M**ulti **P**oint **C**lamped **C**onverter
MMC	**M**odular **M**ultilevel **C**onverter
NCC	**N**ested **C**ell **C**onverter
PWM	**P**ulse **W**idth **M**odulation
PD-PWM	**P**hase-**D**isposition **PWM**
PS-PWM	**P**hase-**S**hifted **PWM**
STATCOM	**STAT**ic (Synchronous) **COM**pensator
SSSC	**S**tatic **S**ynchronous **S**eries **C**ompensator
SVC	**S**tatic **V**ar **C**ompensator
SVG	**S**tatic **V**ar **G**enerator
TCR	**T**hyristor **C**ontrolled **R**eactance
TCSC	**T**hyristor **C**ontrolled **S**eries **Capacitor**
TCR	**T**hyristor **C**ontrolled **R**eactance
THD	**T**otal **H**armonic **D**istortion
VSC	**V**oltage **S**ource **C**onverters

Symbols

C	Capacitance	F (Farad)
e_a	phase supply voltage	V (Volt)
e_d	d component of phase supply voltage	V (Volt)
e_q	q component of phase supply voltage	V (Volt)
f_c	carrier frequency	Hz (Herz)
f_0	reference frequency	Hz (Herz)
i_a	phase-leg current	A (Ampere)
i_d	d component of 3-phase current	A (Ampere)
i_q	q component of 3-phase current	A (Ampere)
L_{ac}	AC inductance	H (Henry)
L_a	line inductance	H (Henry)
m_f	modulation frequency index	
M	modulation index	
p	active power	W (Watt)
q	reactive power	Var (Volt-ampere Reactive)
R	Resistance	Ω (Ohm)
v_a	phase-leg voltage	V (Volt)
v_{Bda}	phase voltage control adjustement voltage	V (Volt)
$\overline{v}_C$	mean dc capacitor voltage (3-phase)	V (Volt)
$\overline{v}_{Ca}$	mean dc capacitor voltage (single-phase)	V (Volt)
$\overline{v}_{Ca1}$	mean dc capacitor voltage (cell)	V (Volt)
V_{dc}	dc voltage	V (Volt)
v_d	d component of 3-phase voltage	V (Volt)
v_q	q component of 3-phase voltage	V (Volt)

ω_c	carrier waveform angular frequency	rad/s
ω_0	reference waveform angular frequency	rad/s
θ_c	carrier phase shift	rad
θ_0	reference phase shift	rad

Chapter 1

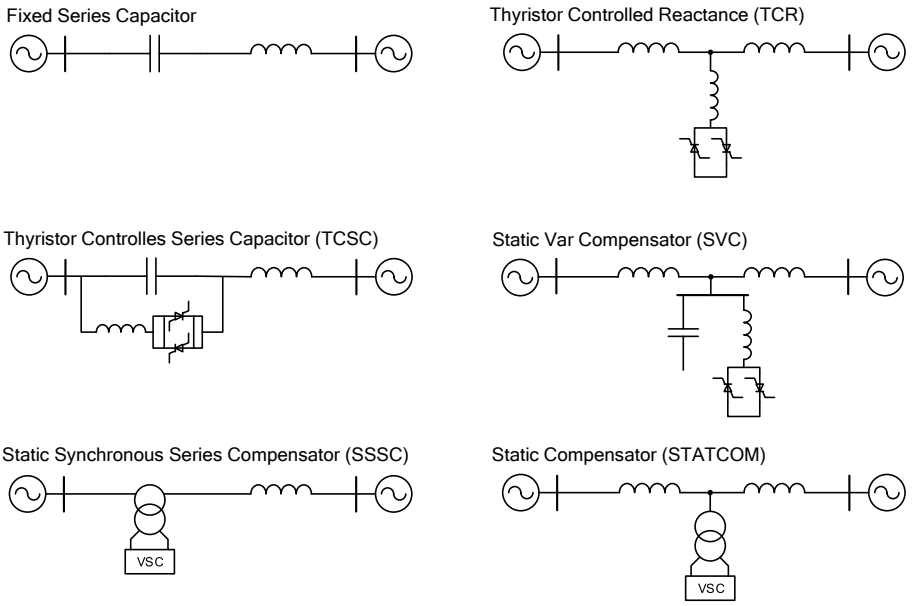
Background and Motivation

This chapter gives a brief introduction to the need for reactive power compensation and an overview of different kinds of compensation devices. Further, different topologies of converter based compensators are described and the main modulation strategies for these are given. Lastly, the aim of the thesis and main contributions are described.

1.1 Need for reactive power compensation in power systems

Electric power is usually generated, transmitted and consumed in AC form [1]. When transmitting AC-power both active and reactive power are transmitted, but it is only the active power that contributes to the energy consumed by the loads. The presence of reactive power in transmission lines does not only limit the amount of active power that can be transmitted, but it also affects the system stability. The transmitted reactive current can be either capacitive or inductive depending on the line loading.

A Flexible Alternating Current Transmission System (FACTS) is defined in [2] as "A power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability." FACTS devices can be connected in either series or shunt with the power line as shown in Figure 1.1. In principle, all the series connected FACTS devices inject voltage and all the shunt connected devices inject current to the transition line. The series compensation devices can have either fixed or variable impedance [1]. By



(a) Series Compensation (b) Shunt Compensation

FIGURE 1.1: The most common series and shunt compensation devices

adding a fixed capacitance in series with the transmission line, the line inductance is counteracted, which increases the transfer capability of the line and improves the angular stability. The series connected FACTS devices with a variable impedance instead, can be used whenever control of power flow is needed. If very good dynamic behavior is desired, a Voltage Source Converter (VSC) can be connected through a transformer in series with the line. Though, at transmission level, this is usually considered too expensive and complex and is therefore almost never used.

The shunt connected FACTS devices are connected in parallel with the transmission line Shunt compensation can be either static or dynamic. The static shunt devices consist mainly of shunt capacitors that are either permanently connected or switched on with thyristors or mechanical switches. The dynamic shunt compensation device consist of a VSC connected through a transformer in parallel with the line. This device is known as the STATic synchronous COMpensator (STATCOM). The main feature of this type of device is its ability to keep voltage profiles at desirable levels. By employing these devices, the transfer capability of the line can be increased and as consequence, the losses reduced.

The first prototype of a STATCOM was reported in 1981 [3] and constituted by several VSC through zig-zag transformers to reduce the total harmonic distortion (THD). In modern STATCOMs, the bulky zig-zag transformers have instead been replaced by multilevel converters. The basic concept of a multilevel converter is to obtain a sinusoidal voltage from multiple voltage levels typically provided by capacitors that can be either inserted or bypassed though power electronic based switches [4]. Introducing multiple voltage levels when generating the output waveform results in a more sinusoidal waveform with reduced THD. However, the control and modulation strategies for multilevel converters are often more complex and the increased voltage levels introduce voltage balancing issues which will be described later.

1.2 Actual trend for converter topologies

Multilevel converters can be divided into three main topologies which differ significantly in terms of implementation.
The Multipoint-Clamped Converter (MPCC), also referred to as the diode-clamped converter, is an extension of the three-level converter known as the neutral-point-clamped (NPC) converter. This converter consists of a number of series connected clamping diodes, composed in a quite complex physical layout.

In figure 1.2(a), the three-level MPCC is shown. The middle point of the two capacitors n is defined as the neutral point. The produced output voltage v_{an} has three levels; $+V_{dc}/2$, 0, and $-V_{dc}/2$. When switches S_1 and S_2 are on, v_{an} becomes $+V_{dc}/2$; when switches S_1' and S_2' are on, v_{an} becomes $-V_{dc}/2$; and v_{an} is 0 when switches S_2 and S_1' are on. What distinguishes this particular converter from the conventional two-level converter are the two diodes D_1 and D_2, that clamp the voltage to half the dc bus voltage. When switches S_1 and S_2 are turned on, the voltage across a and 0, i.e. v_{a0}, becomes $V_{dc}/2$. The voltage between S_1' and S_2' is balanced out by D_1' where S_1' blocks the voltage across C_1 and S_2 blocks the voltage across C_2.

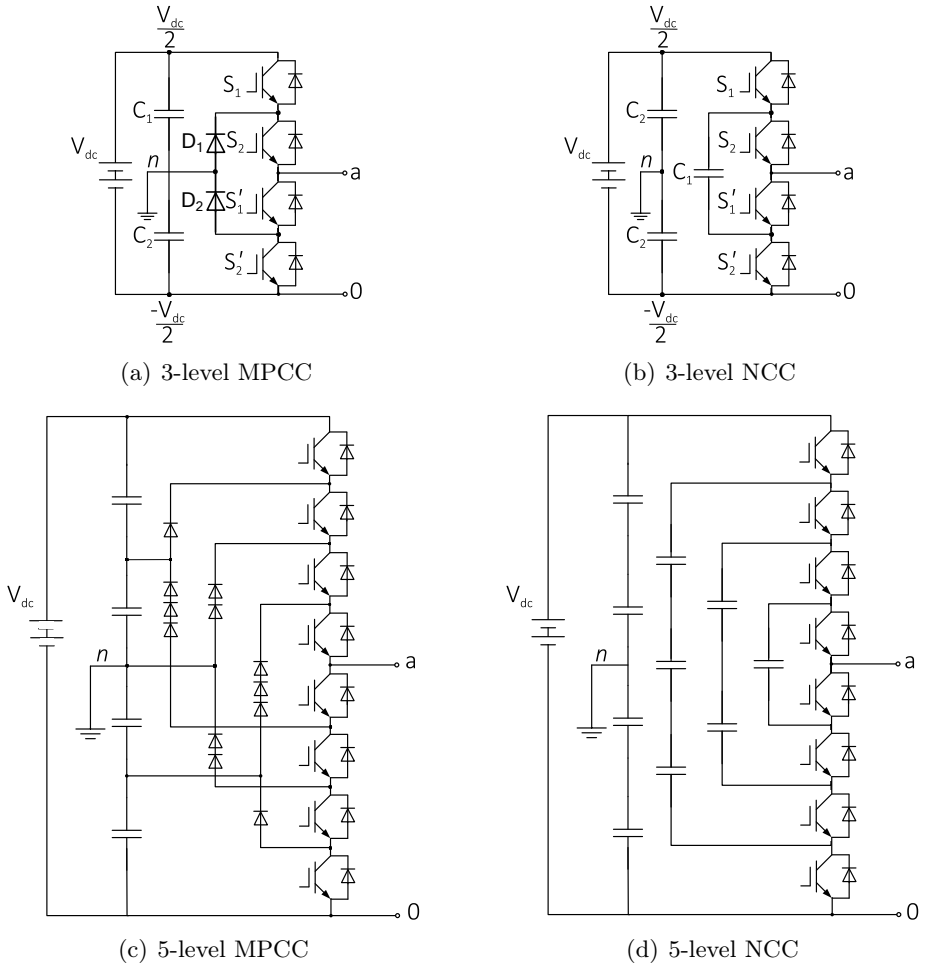
Figure 1.2(c) shows the schematics of a five-level MPCC and as can be seen in the figure, adding two voltage levels result in a much more complex construction . The complex

construction is what makes the MPCC unattractive for higher voltage levels than three. In addition to having a complex structure, voltage levels above three require external balancing circuits because the series-connected dc capacitors face voltage imbalance issues when using conventional modulation strategies [5]. To balance the capacitors in this case, higher dv/dt (more-than-one-level transitions) are required which will no longer give the classical multilevel staircase output.

The Nested-Cell converter (NCC), or the flying capacitor converter, is composed by a number of capacitors that can be switched on and off by transistors. The capacitors are not connected to the DC bus and therefore require higher switching frequencies in order to keep the capacitors properly balanced. In high-power applications however, high switching frequencies are not desirable due to the high switching losses and usually kept in the range of 500-700 Hz.

Figure 1.2(b) and 1.2(d) shows the schematics of the three and five-level NCC. This converter utilizes independent capacitors that clamp the bus voltage to one voltage level per capacitor. The output voltage v_{an} in the three-leveled converter varies between $+V_{dc}/2$, 0 and $-V_{dc}/2$. When S_1 and S_2 are switched on, v_{an} is equal to $+V_{dc}/2$; with S_1' and S_2' on, v_{an} equals $-V_{dc}/2$; and when either (S_1,S_1') or (S_2,S_2') are switched on, v_an is 0. The clamping capacitor C_1 is charged while (S_1,S_1') are on, and discharged while (S_2,S_2') are on. By proper selection of 0-level switching combinations, the voltage across C_1 can be balanced.

The Modular Multilevel Converter (MMC), also known as the chain-link converter or cascade converter has emerged both in industrial applications and academia since the early 2000s. It consists of a number of cascaded cells, each equipped with a floating capacitor. There exist many different configuration topologies of the MMC and an equal amount of cell topologies proposed. Some very common cell topologies are shown in Figure 1.4. The most commonly used cell topologies are the full-bridge cells and the half-bridge single-phase converters. The half-bridge composed MMC, shown in Figure 1.4(a), can only generate positive and zero voltages and must have an even number of cells, in order to generate an equal number of positive and negative voltage levels. Since it can only



(a) 3-level MPCC (b) 3-level NCC

(c) 5-level MPCC (d) 5-level NCC

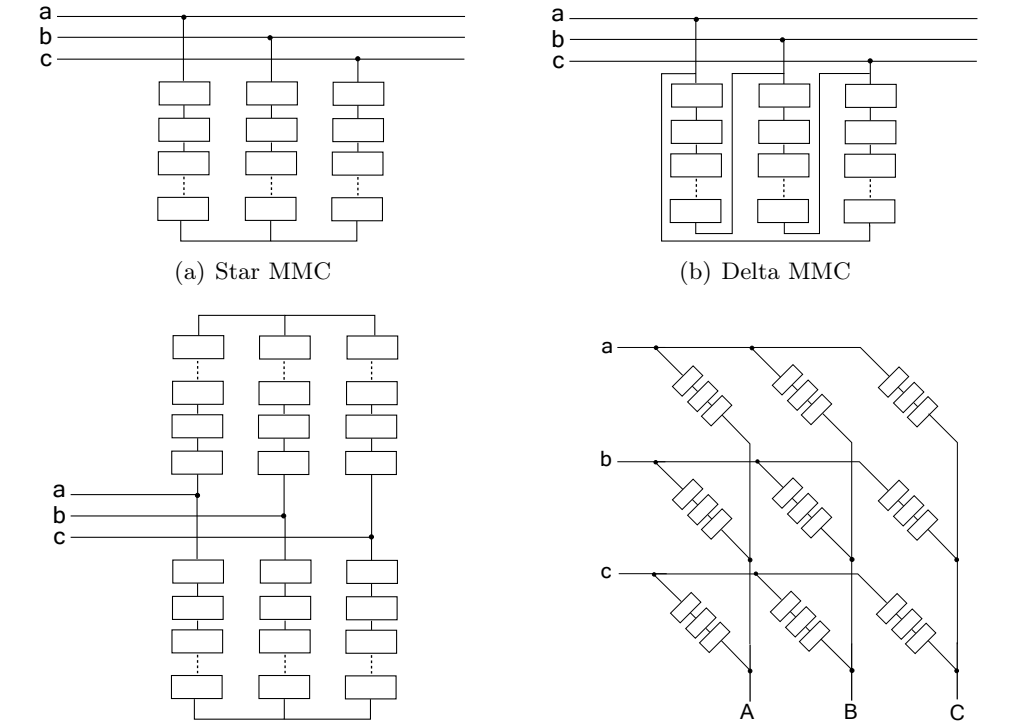
FIGURE 1.2: Circuit configuration of a MPCC and NCC

produce zero and positive voltages, there is inevitably a dc component and therefore it is only used in dc systems [6].

The full-bridge composed MMC, Figure 1.4(b), can generate both positive, negative and zero voltages which is why it is suited both for ac and dc systems.

In addition to these two common cell topologies, in order to increase the efficiency, the cells can be substituted by multilevel cells such as the NPC or the flying capacitor, shown in 1.4(c) and 1.4(d). For example, a 9-level MMC consisting of four full-bridge converters has four floating capacitors, which is described in [6]. By using two 3-level MPCCs instead of the four full-bridge converters, the same voltage level number is achieved but with fewer components and fewer floating capacitors. This improves the efficiency and also reduces the amount of required individual balancing controllers.

Figure 1.3 shows different circuit configurations of MMC. As can be seen in the figure, the cells can be constructed in a number of different ways, where the advantages and disadvantages are dependent on the application purpose.



(a) Star MMC (b) Delta MMC

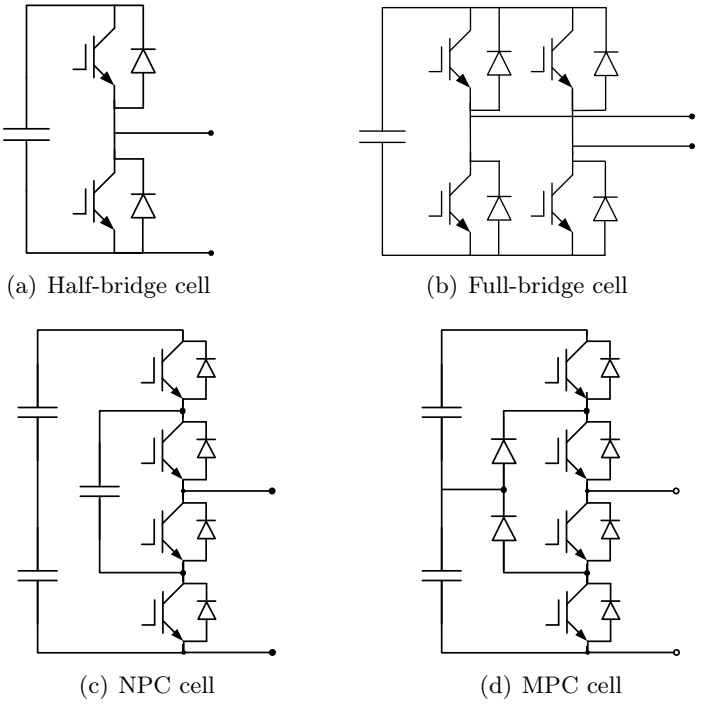
(c) Double Star MMC (d) Dual MMC

FIGURE 1.3: Configuration topologies of the MMC

The modular structure of the MMC makes it easy to introduce many voltage levels. As result, the MMCs is well suited for high power applications even with classic low-voltage semi-conductors. Furthermore, the high voltage-level number allows a significant reduction in switching frequency at cell level while still providing a high switching frequency in the resulting phase-leg voltage and current. This allows a reduction in switching losses while still moving the phase-leg voltage and current harmonics to higher frequencies which is desired for easier filtering. However, as with the NCC, floating capacitors still face the crucial issue of voltage imbalance, requiring additional voltage balance controllers to be added. A more detailed description of the control system will be provided in the next chapter.

The configuration topology shown in Figure 1.3(a) combined with the the cell topology shown in Figure 1.4(b) is what builds up the converter investigated in this thesis. Each sub-module toggles between three states; $+V_{dc}$, 0, $-V_{dc}$, and the total number of states

N_L achieved with this type of configuration are $N_L = 2N_H+1$ (where N_H is the number of cells). The resulting phase-leg voltage is given by the sum of the voltages generated by all the cells. In the case with 3 submodules, the phase-leg voltage will toggle between between $-3V_{dc}$ and $+3V_{dc}$. The current waveform is nearly sinusoidal even without filtering.



(a) Half-bridge cell (b) Full-bridge cell

(c) NPC cell (d) MPC cell

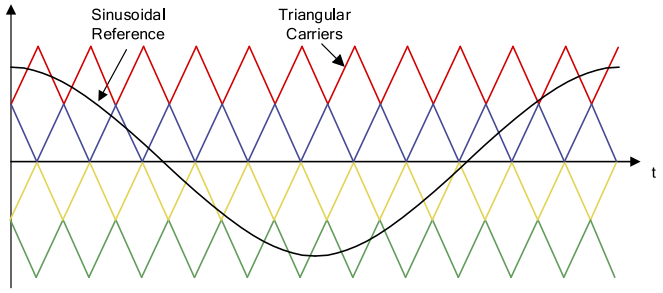
FIGURE 1.4: Cell topologies for the MMC

1.3 Multilevel Converter Modulation Strategies

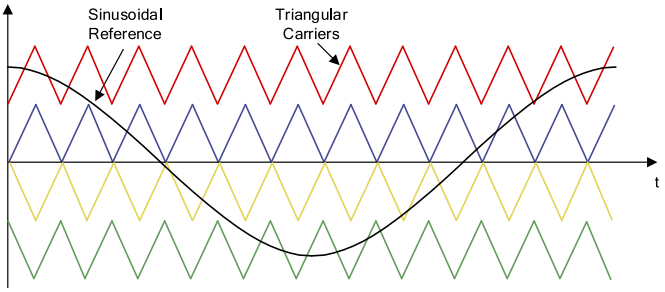
Modulation of multilevel converters is quite challenging there are many modulation strategies proposed in the literature to deal with the growing number of multilevel converter topologies [7]. Extending the modulation strategies for conventional converters to multilevel converters faces the challenge of not only having to control more power-electronics devices, but also the desire to explore additional degrees of freedom that can be gained from the increased number of switching states. As a result, there exists a large number of modulation strategies and algorithms to best fit a certain application and converter topology. In this thesis, the modulation strategies have been classified in to three groups; Carrier based Pulse-Width Modulation (PWM), Space Vector Modulation (SVM) and other modulation strategies.

1.3.1 Carrier-based PWM Strategies

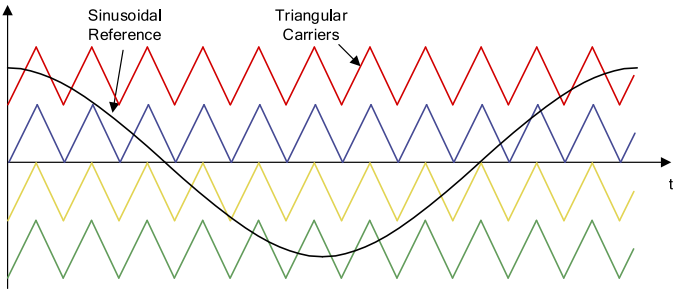
The two main carrier based PWM strategies for multilevel converters are the Level-Shifted PWM (LS-PWM) and Phase-Shifted (PS-PWM). The LS-PWM is the natural extension of bipolar PWM and it requires $N' - 1$ (where N' is the number of cells) to be applied to a multilevel converter. In this strategy, each carrier is associated to two voltage levels and thereby the same principles as for bipolar PWM can be applied for this method. The carriers span the whole amplitude range that the converter can generate and they can be shifted vertically. Variants of the LS-PWM, are shown in Figure 1.5.



(a) APOD



(b) POD



(c) PD

FIGURE 1.5: PD-PWM strategies for a five-level MPCC.

For the NPC and the MMC, where each cell can consist of two or three voltage levels and can be independently modulated using the same reference signal, the Phase-Shifted

PWM is a natural extension of the carrier-based PWM strategies. The PS-PWM strategy has N' carriers, each phase-shifted compared to each other. Introducing a phase-shift of $180/N'$ between the carriers, with the first carrier as a reference, results in a stepped waveform that gives the lowest distortion. This because the phase-shift results in calculation of all sideband harmonics up to $2N'$th carrier group. Since each cell uses the same reference, the switching is evenly distributed among the different cells. Another beneficial feature of this strategy is that the total output voltage has a switching pattern corresponding to N' times the switching pattern of each cell voltage.

1.3.2 SVM strategies

In the SVM strategy, unlike the previously mentioned methods, the switching pattern is obtained based on the three-phase space vector representation of the reference and the inverter switching states. All SVM-based techniques evolve around a modulation algorithm that can be divided into three stages. First, a set of switching states are selected, usually the three closest to the reference, second the duty cycles of each state is determined, and in the final stage the sequence in which the vectors are computed is determined. It has been reported that SVM-based strategies are able to achieve one or more of the following: a reduction in switching frequencies [8], lower THD compared to carrier based strategies [9], capacitor voltage balancing [10], feed-forward of dc-link ripple [11] etc. One of the big advantages of the SVM strategies compared to the carrier based PWM, is the reduced computational burden because the number of carriers does not increase with increased number of cells. However, in order to achieve a proper time average, the modulation period has to be small, which is comparable to high switching frequencies (above 1000 Hz) and this is undesirable for high power applications.

1.3.3 Other Modulation Strategies

Converters for high power applications are usually modulated with strategies that have switching frequencies below 1000 Hz. Using traditional carrier based PWM strategies with PS-PWM at these frequencies would result in low-order harmonics in the output voltage, which would increase the distortion and result in performance problems. One method that is developed to be used at low switching frequencies for high power applications is the Selective Harmonic Elimination (SHE) method. In this method, the harmonic

components of the switched waveform with unknown switching angles, are controlled to be equal to zero for the undesired harmonics, while the fundamental is controlled to the desired reference waveform.

For high power grid connected converters, a variation of SHE called Selective Harmonic Mitigation (SHM) can be used [12]. Here, unlike SHE, the undesired harmonics are not completely cancelled out, but instead limited to acceptable values.

For the modular multilevel converter topologies, there is one modulation strategy that has received a lot of attention recently and that is the sorting algorithm. This method uses the capacitor voltage increment during the last fundamental period as a basis to determine which of the carriers that charge the capacitors most or least. Consequently, the voltage increments are sorted in the descending order and the capacitor voltages are sorted in the ascending order. Then the carrier that charges the capacitors the most is applied to the capacitor with the lowest voltage and the carrier that discharges the capacitor the most will essentially be applied to the highest capacitor voltage. This method results in voltage balancing of the capacitor voltages. It can be further extended by using the previous information for predicting future voltage charging and preventing deviation.

Very recently, the use of model predictive control (MPC) has been introduced as a very promising alternative. This method has its base in a simple cost or quality function that has to be minimized. Unlike the traditional controllers, MPC based control does not require any modulator since the switching states are set directly from the controller and it has the benefit of allowing direct influence of several system variables simultaneously [13]. However, one major disadvantage of this control strategy is the computational burden for solving the switching states which is relatively high and increases exponentially for increased cell voltage numbers.

In this thesis, the aim was to investigate the PS-PWM method, so no attention has been paid to the other methods.

1.4 Aim of this thesis

This thesis aims to describe the essential principle of a cascaded multilevel converter and the voltage imbalance challenges that arise when these converter topologies are equipped with multiple separate dc links. Furthermore, the aim is to illustrate the effect of the frequency modulation index on cell voltage balancing in the modular multilevel converter modulated with PS-PWM.

1.5 Main contributions

The main contributions of this thesis is a detailed description of the harmonic contents in cell voltage and current with PS-PWM and a non-integer frequency modulation index. Further, the impact on cell voltage balancing has been investigated for different frequency modulation indices. The effect on harmonic content from integer versus non-integer indices has been studied and compared and the result show a significant improvement of cell voltage balancing with the latter.

Chapter 2

Principle of Modular Multilevel Converters

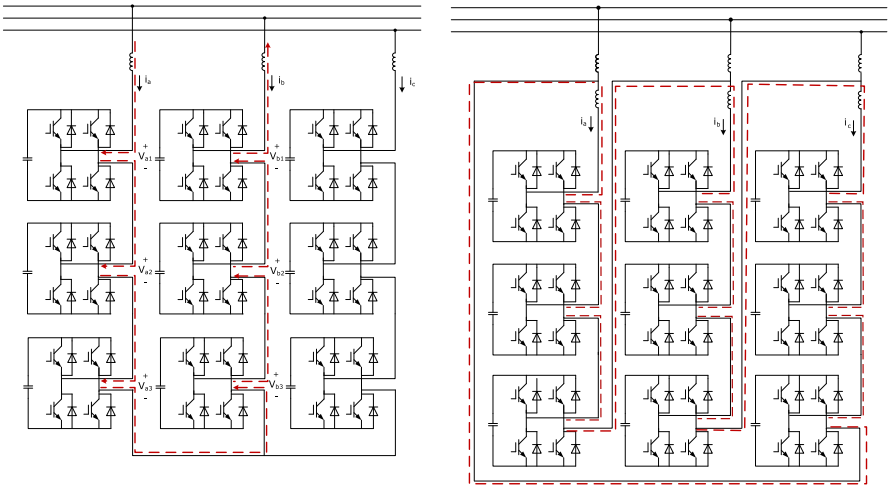
This chapter provides a short introduction to the MMC and some of the most common configurations of this converter topology along with their application purposes. Further, a detailed description of the investigated system is given along with the control and modulation strategy implemented in this work.

2.1 Modular Multi-level Converters and their applications

The first introduction of an MMC was reported in 1975 [14] based on series connection of full-bridge cells. In 2002, an alternative module was proposed by R. Marquardt, where half-bridge cells were used instead [15]. As mentioned in Chapter 1, there are many different configurations proposed today, depending on the performance requirements and applications. These can be classified as:

1. star-configured MMC;
2. delta-configured MMC;
3. double-star-configured MMC;
4. dual MMC.

When applied to high-power STATCOM systems, the MMCs are used to either inject or absorb reactive current. The current flow during compensation in the different topologies needs to be taken into consideration when choosing the specific converter topology. The current path for the star and delta configured MMC is shown in Figure 2.1.



(a) Current path in star configuration (b) Current path in delta configuration

FIGURE 2.1: Current path in star and delta configuration

The current path during compensation is different for different configuration topologies. In the star configuration, the current can flow from from one phase leg to another, leaving the third phase leg completely intact. As Figure 2.1(a) illustrates, the current can flow in a one direction through phase leg a, and in the opposite direction through phase leg b, which can charge or discharge the capacitors depending on which path the current flows through in the cells. The sum of active power transmitted between the phase legs must be equal to zero, to prevent active power exchange between the converter and the transmission lines. If active power is transmitted from phase leg b to phase leg a, the sum of the active power exchange is still zero, but the capacitors in phase leg a can be overcharged due to the lack of circulating current. In a delta configuration, on the other hand, the current circulates through all three phase legs, as illustrated in Figure 2.1(b), allowing a natural power distribution among the phase legs. However, in a delta connection the voltage is $\frac{1}{\sqrt{3}}$ of that in the line, so the power electronics must be rated $\sqrt{3}$, or additional cells must be added, compared to a star-configuration. Another shortcoming of the delta configuration is that the current is $\sqrt{3}$ times higher than the line current, which results in very high currents circulating in the converter.

In the double star configured MMC, shown in 1.3(c), the active power exchange is limited to the two phase-legs corresponding to each phase. This means that the power exchange between the line and the converter is limited to only reactive power which eliminates the voltage imbalance issue.

Another configuration of the MMC is the dual MMC, illustrated in Figure 1.3(d). This configuration type is a combination of the star and delta configurations and their advantages. Both the double-star and the dual configured MMCs are composed of two converters instead of one which increases the cost and footprint significantly. For compensation in large HVDC links, the star/delta configurations are more than adequate.

The main focus of this thesis is put on investigating the modulation index effect on voltage balancing of the MMC. The star configured MMC is the one most exposed to voltage imbalances and is therefore the topology investigated.

2.2 System Description

The considered MMC topology consists of series-connected full-bridge converters connected in star. These full-bridges are referred to as cells or submodules and they are normally controlled in such way that the dc capacitor voltages are kept close to their nominal value. Each cell capacitor acts as a voltage source that can be either inserted or bypassed. Each phase-leg has N cells and an AC inductance. Here, the investigated system consists of three cells per phase-leg, for a total of 9 cells.

Converter Ratings		
Rated Power	P	120 kV
Rated Voltage	V	33 kV
Fundamental Frequency	f_0	50 Hz
Cell voltage number	N	3
DC-link capacitor	C	4000 F
AC filter inductance	L_{ac}	4 mH

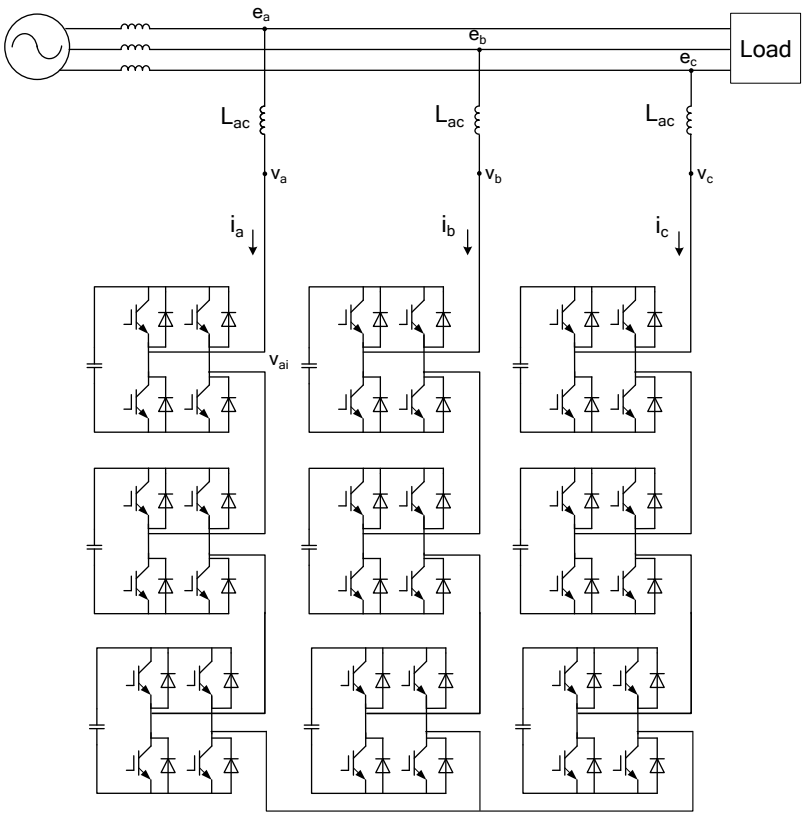


FIGURE 2.2: Schematics of the 3-phase, star-configured MMC investigated in this thesis

2.2.1 Design of main components

The energy stored in one cell can be calculated by:

$$E_{cell} = \frac{1}{2} C V_{dc}^2 \tag{2.1}$$

where V_{dc} is given by $\frac{V_a}{N} k$ and k is the factor that indicated the relation between the nominal cell voltage and the corresponding dc voltage. This means that the total energy stored in one phase-leg is given by:

$$E_a = \frac{N}{2} C V_{dc}^2 \tag{2.2}$$

Since the converter is rated at 33 kV and consists of 3 cells per phase-leg, each cell will have a nominal voltage rating of 11 kV. Because of the voltage imbalance issue, the capacitors need to be able to withstand higher voltages than the nominal value.

The ac filter inductance L_{ac} is chosen to be 0.1 p.u. and can be determined according

to:

$$X_{Lac} = 2\pi f_0 L_{ac} = 0.1 * Z_{base} = 0.1 * \frac{V_{base}^2}{S_{base}} \tag{2.3}$$

The maximum voltage that each semi-conducting device must be able to withstand can be find according to:

$$V_{rated} = \frac{V_{cell}}{N} k_{max} \tag{2.4}$$

where k_{max} is the value of the maximum percentage above rated value that is allowed, i.e. the maximum voltage ripple from the capacitors, and V_{cell} is the pole-to-pole dc link voltage.

2.3 Overview of control system

Figure 2.3 shows the control system of the investigated converter. The implemented control system is from [16] and consists of two sub-controls; current control that controls the active and reactive power and balancing voltage control for the submodules. Additionally, the balancing voltage control can be divided into the cluster controller, which controls the voltage in each cluster leg, and the individual balancing controller which controls each cell separately.

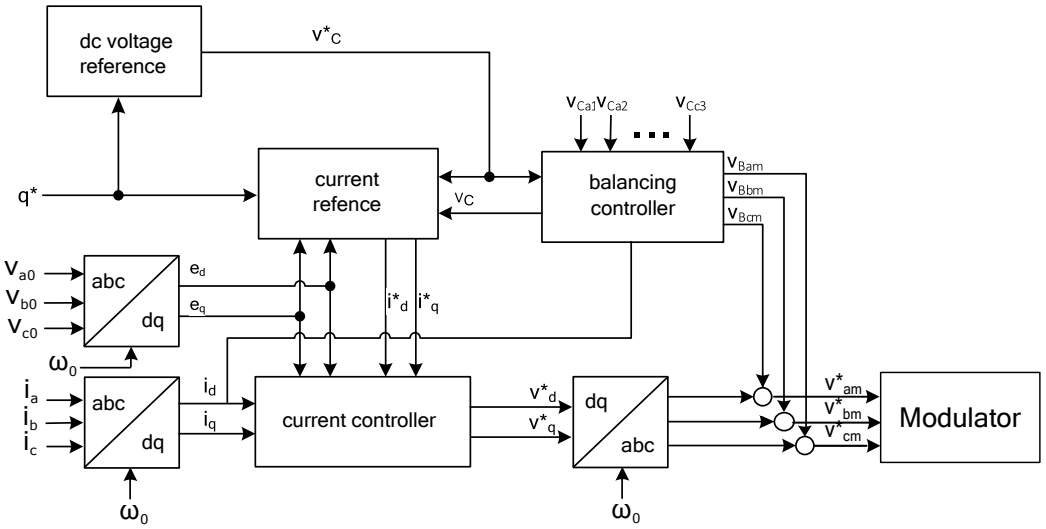


FIGURE 2.3: Overview of the control system implemented

2.3.1 Cluster control

The three phase voltages can be derived from Figure 2.2 to:

$$\begin{aligned} v_a &= e_a - L_{ac}\frac{di_a}{dt} \\ v_b &= e_b - L_{ac}\frac{di_b}{dt} \\ v_c &= e_c - L_{ac}\frac{di_c}{dt} \end{aligned} \tag{2.5}$$

where e_a, e_b and e_c are the three phase supply voltages. Equation (2.5) can be rewritten as the difference between the supply voltage and the three phase-leg voltages giving:

$$\begin{bmatrix} L_{ac}\frac{d}{dt} & 0 & 0 \\ 0 & L_{ac}\frac{d}{dt} & 0 \\ 0 & 0 & L_{ac}\frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} e_a - v_a \\ e_b - v_b \\ e_c - v_c \end{bmatrix} \tag{2.6}$$

Transforming (2.6) to dq-coordinates gives:

$$\begin{bmatrix} L_{ac}\frac{d}{dt} & -\omega_0 L_{ac} \\ \omega_0 L_{ac} & L_{ac}\frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} e_d - v_d \\ e_q - v_q \end{bmatrix} \tag{2.7}$$

where v_d, v_q and e_d, e_q correspond to the dq components of the cluster voltages v_a, v_b, v_c and the supply voltage e_a, e_b, e_c respectively.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} e_d \\ e_q \end{bmatrix} - \begin{bmatrix} 0 & -\omega_0 L_{ac} \\ \omega_0 L_{ac} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2.8}$$

The mean dc capacitor voltage of the three-phase system is given by

$$\bar{v}_C = \frac{1}{3}(\bar{v}_{Ca} + \bar{v}_{Cb} + \bar{v}_{Cc}) \tag{2.9}$$

and the mean dc capacitor voltages of the phase-legs are given by:

$$\begin{aligned} \bar{v}_{Ca} &= \frac{1}{3}(\bar{v}_{Ca1} + \bar{v}_{Ca2} + \bar{v}_{Ca3}) \\ \bar{v}_{Cb} &= \frac{1}{3}(\bar{v}_{Cb1} + \bar{v}_{Cb2} + \bar{v}_{Cb3}) \\ \bar{v}_{Cc} &= \frac{1}{3}(\bar{v}_{Cc1} + \bar{v}_{Cc2} + \bar{v}_{Cc3}) \end{aligned} \tag{2.10}$$

A P controller is used to adjust the current reference according to:

$$\begin{aligned} i_d^* &= K_1(v_C^* - \bar{v}_C) \\ i_q^* &= \frac{q*}{e_d} \end{aligned} \tag{2.11}$$

which gives the following equation for the voltage references:

$$\begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} = \frac{1}{3}\left(\begin{bmatrix} e_d \\ e_q \end{bmatrix} - \begin{bmatrix} 0 & -\omega_0 L_{ac} \\ \omega_0 L_{ac} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - K_2 \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} - K_3 \int \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} dt \right) \tag{2.12}$$

The supply voltage and voltage across the ac inductor are cancelled out by the first two terms on the right side of (2.12). The third term is a PI-controller for the d and q current.

The real and imaginary parts of the apparent power, i.e. the active and reactive power can be expressed as

$$\begin{aligned} p &= e_d \cdot i_d + e_q \cdot i_q = e_d \cdot i_d \\ q &= e_d \cdot i_q - e_q \cdot i_d = e_d \cdot i_q \end{aligned} \tag{2.13}$$

2.3.2 Individual Balancing Control

The cluster balancing control loop controls the mean dc capacitor voltage $\bar{v}_{Cj}$ (j representing the phase) with following loop

$$v_{Bda} = -K_4\{K_3(v_C^* - \bar{v}_{Ca}) - i_d\} \sin \omega_0 t \tag{2.14}$$

When $\bar{v}_{Ca} > v_C^*$, the reference balancing voltage v_{Bda}. This voltage is then added to the reference voltage as shown in Figure 2.3.
The individual balancing control loop is implemented similarly as the cluster control, and the control signal for the cell number i is given by

$$v_{Bqai} = \pm K_5(\bar{v}_{Ca} - \bar{v}_{Cai}) \cos \omega_0 t \tag{2.15}$$

To avoid interaction with the cluster control, the individual controller is designed to be slower than the cluster controller.

2.4 Overview of converter modulation

As mentioned in previous chapter, the PS-PWM is a very simple and reliable modulation strategy with a very good harmonic performance. It is a natural extension of the carrier based PWM methods used in conventional converters which is why it has been a popular choice in the industry [17].

Considering simpler modulation of the individual cell and for an N-level cascaded inverter, this strategy consists of N-1 carriers, each phase-shifted by 180°/N. The carriers have the same frequency ω_c and the same peak-to-peak amplitude E. The reference waveform is an arbitrary waveform with the frequency ω_0 and normalized amplitude M. This modulation strategy leads to full cancellation of harmonics up to 2N'th carrier group under ideal conditions.

The frequency modulation index is defined as the ratio between ω_c and ω_0 and it is essentially the impact on voltage balancing that this ratio has that is investigated in this work. As can be noticed, in this method, there are not a lot of parameters that can be influenced to improve the performance of the converter and as result the research around modulation strategies for multilevel converters is moving towards more complex modulation techniques that can potentially explore more degrees of freedom. There have been a lot of new strategies proposed that are superior to the PS-PWM but the reliability of the simplicity in this method might be a reason to why it is still widely used in the industry. The next chapter aims to investigate the voltage imbalance problem by analyzing the harmonic components in the cell voltages and current of the converter.

Chapter 3

Spectral Characteristics of Phase-Shifted PWM

In this chapter, a brief introduction to Fourier analysis is given and the harmonic content in a cell voltage for naturally and regularly sampled PWM is determined. Further, the harmonic content in the phase-leg voltage and arm current is derived. Finally, the impact that the produced harmonics have on the output voltage and cell-balancing during ideal and non-ideal conditions are determined.

3.1 Principles of Phase-Shifted PWM

The basis for modulation in power electronics is pulse-width modulation. PWM can take many different forms, few of which will be considered in this chapter.
The most common carrier types are

- the sawtooth carrier, associated with trailing edge modulation;
- the inverted sawtooth carrier, associated with leading-edge modulation; and
- the triangular carrier which is associated with double-edge modulation.

Trailing- and leading-edge modulation is often used in DC-DC converters while the double-edge modulation is more common in AC-DC and DC-AC converters [18]. This

because the double-edge modulation eliminates all even harmonics and centers the side-band harmonics around double the carrier frequency [19]. Even though even harmonics are cancelled out in trailing and leading-edge modulation in the line-to-line voltage, i.e. the output voltage from one fullbridge cell, it is better to cancel out harmonics in one phase leg than to rely on cancellation between phase-legs. Since the converter in this work is a DC-AC converter, double-edge modulation is used.

All fixed frequency open-loop PWM strategies can be divided into three categories [19], namely:

1. Naturally sampled PWM;
2. Regular sampled PWM;
3. Direct PWM.

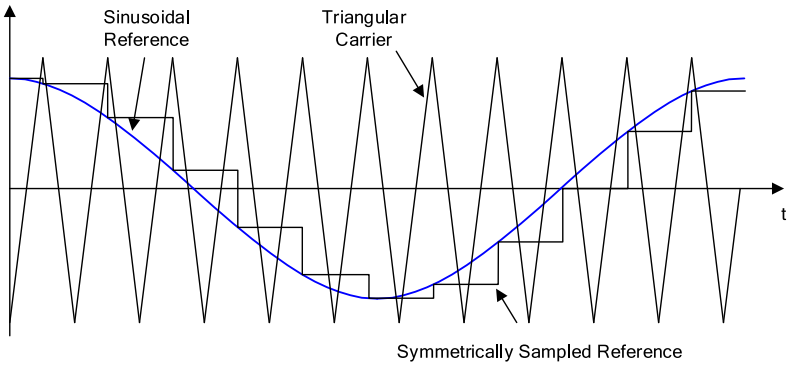
Naturally sampled PWM is used for analog implementation where the switching occurs at the intersection between the analog sinusoidal reference wave and the carrier wave. In digital implementation, on the other hand, the reference is usually sampled at regular time intervals and the reference waveform can be replaced by a clock/counter instead. The reference waveform in regular sampled PWM can be sampled either symmetrically or asymmetrically, as illustrated in Figure 3.1. As the figure shows, regular sampling introduces a relative phase delay, which can be compensated for with a phase advance. The phase advance is one half of the carrier interval for symmetrical and one quarter of the carrier interval for asymmetrical regular sampling. The sampled waveform is illustrated in Figure 3.1 and with the phase advance in Figure 3.2.

Direct PWM differs from the previous strategies and instead switching occurs when the integrated area of the target reference waveform over the carrier waveform is the same as the integrated area over the output [19].

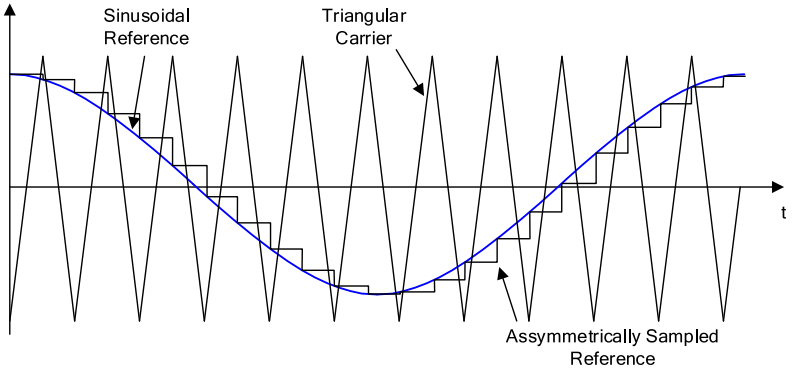
The equation describing the harmonic contents in the converter current and cell voltage waveforms have been carried out for naturally and regularly sampled PWM.

3.2 Double Fourier Integral Analysis

According to Fourier transform theory, a periodic function can be represented by a Fourier Series [19]. Fourier analysis can be performed on the PWM waveform if the ratio



(a) Symmetrical Regular Sampling



(b) Asymmetrical Regular Sampling

FIGURE 3.1: Regular Sampled PWM.

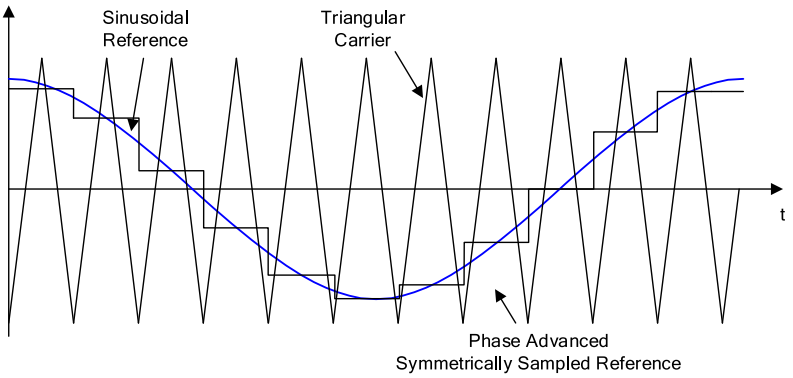
between the carrier frequency f_c and the fundamental f_0 is a rational number. If it also is an integer number, the Fourier analysis can be performed over one fundamental period $1/f_0$, since it is the periodicity of the waveform. For the case where the ratio is a non-integer value, the analysis must be performed on multiple periods of the fundamental, which will be explained later in this chapter. For analyzing the harmonic spectra in the output waveform of a converter, the Double Fourier Series method is used. In the Double Fourier Series method, there are two time-varying variables to consider. Namely the carrier frequency f_c corresponding to the duty cycle and the fundamental frequency f_0 corresponding to the periodicity of the square waves. Choosing $x(t) = \omega_c t + \theta_c$ and $y(t) = \omega_0 t + \theta_0$, where

$$\omega_c = 2\pi f_c \tag{3.1}$$

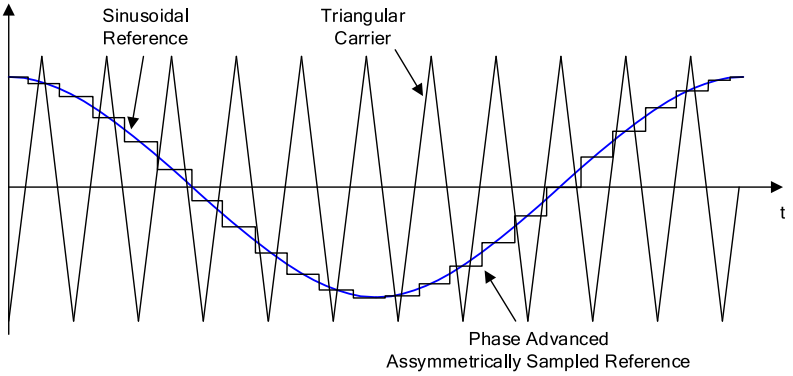
with

$$\theta_c = \text{phase offset angle for carrier waveform}$$

$$\omega_0 = 2\pi f_0 \tag{3.2}$$



(a) Phase-advanced Symmetrical Regular Sampling



(b) Phase-advanced Asymmetrical Regular Sampling

FIGURE 3.2: Regular Sampled PWM with Phase-advance.

with

$$\theta_0 = \text{phase offset angle for fundamental waveform}$$

Using the previous as the time-varying variables, the harmonic components can be expressed, according to [19], with a two dimensional Fourier Series as

$$\begin{aligned} f(x,y) = \frac{A_{00}}{2} &+ \sum_{n=1}^{\infty}[A_{0n}\cos ny + B_{0n}\sin ny] + \sum_{m=1}^{\infty}[A_{m0}\cos mx + B_{m0}\sin mx] \\ &+ \sum_{m=1}^{\infty}\sum_{\substack{n=1 \\ i\neq 0}}^{\infty}[A_{m0}\cos(mx+ny) + B_{m0}\sin(mx+ny)] \end{aligned} \tag{3.3}$$

where the coefficients are given by

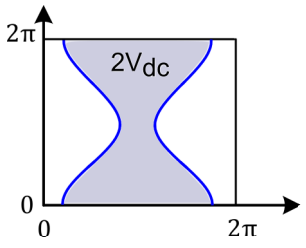
$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)e^{j(mx+ny)}dxdy \tag{3.4}$$

Replacing x and y with $\omega_c t + \theta_c$ and $\omega_0 t + \theta_0$ respectively, gives

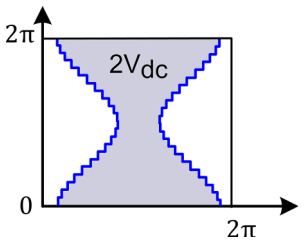
$$
\begin{aligned}
f(t) = & \underbrace{\frac{A_{00}}{2}}_{\text{DC offset}} + \sum_{n=1}^{\infty} \underbrace{\{A_{0n}\cos[n(\omega_0 t+\theta_0)] + B_{0n}\sin[n(\omega_0 t+\theta_0)]\}}_{\text{Fundamental Component \& Baseband Harmonics}} \\
& + \sum_{m=1}^{\infty} \underbrace{\{A_{m0}\cos[m(\omega_c t+\theta_c)] + B_{m0}\sin[m(\omega_c t+\theta_c)]\}}_{\text{Carrier Harmonics}} \\
& + \sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty} \underbrace{\{A_{m0}\cos[m(\omega_c t+\theta_c)+n(\omega_0 t+\theta_0)] + B_{m0}\sin[m(\omega_c t+\theta_c)+n(\omega_0 t+\theta_0)]\}}_{\text{Sideband Harmonics}}
\end{aligned}
\tag{3.5}
$$

where m is the carrier index variable and n is the baseband index variable. The angular frequency of each harmonic component of the output voltage is defined by m and n, as $(m\omega_c + n\omega_0)$. The baseband harmonics are defined by n alone with $m = 0$, and the sideband harmonics by m, with $n = 0$. A_{00}, with $n = 0$ and $m = 0$ corresponds to the DC offset. The Fourier coefficients depend on which PWM strategy used.

The value of the function $f(x, y)$ in (3.4) can be represented in topological form as shown in Figure 3.3(a), where the x and y-axes are scaled in radians corresponding to ω_c and ω_0 respectively. The intersections between the carrier and the reference waveforms are represented by the solution trajectory and have a slope equal to ω_c/ω_0. If both x and y are assumed to be periodic, the value of $f(x, y)$ can be represented as a Fourier series instead. This can be illustrated by repeating the unit cell in Figure 3.3(a) infinitely both in x and y, as shown in Figure 3.4.



(a) Unit cell for Naturally Sampled PWM



(b) Unit cell for Regular Sampled PWM

FIGURE 3.3: Unit cell representation of reference and carrier intersection with natural and regular sampling

The switching instants for naturally sampled PWM can be expressed by

$$x = 2\pi p - \frac{\pi}{2}(1 + M\cos\omega_0 t) \quad p = 0, 1, 2, ..., \infty \tag{3.6}$$

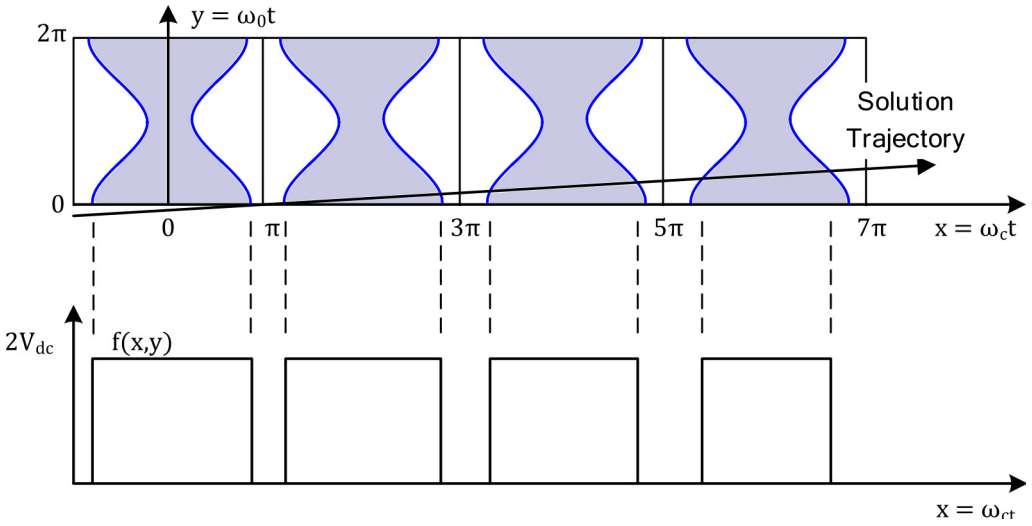


FIGURE 3.4: Switching pattern with double-edge PWM showing the intersections with natural sampling and the resulting output voltage

when f(x,y) changes from 0 to $2V_dc$, and

$$x = 2\pi p + \frac{\pi}{2}(1 + M\cos\omega_0 t) \quad p = 0, 1, 2, ..., \infty \tag{3.7}$$

when f(x,y) changes from $2V_{dc}$ to 0.

This means f(x,y) is only non-zero between (3.6) and (3.7), and is equal to $2V_{dc}$. By substituting the lower and upper limit of the inner integral from (3.4) with (3.6) and (3.7), (3.4) becomes

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1+M\cos\omega_0 t)}^{\frac{\pi}{2}(1+M\cos\omega_0 t)} 2V_{dc}e^{j(mx+ny)}\,dx\,dy \tag{3.8}$$

For $\underline{m = n = 0}$, the DC offset in (3.5) can be simplified to

$$A_{00} + jB_{00} = \frac{V_{dc}}{\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1+M\cos\omega_0 t)}^{\frac{\pi}{2}(1+M\cos\omega_0 t)} dx\,dy = \frac{V_{dc}}{\pi^2}\int_{-\pi}^{\pi}[\pi(1 + M\cos\omega_0 t)]\,dy = 2V_{dc} \tag{3.9}$$

which gives $A_{00} = 2V_{dc}$ and $B_{00} = 0$. For $m = 0$, $n > 0$, the coefficients of the baseband harmonics in (3.5) can be simplified to

$$\begin{aligned} A_{0n} + jB_{0n} &= \frac{V_{dc}}{\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M\cos\omega_0 t)}^{\frac{\pi}{2}(1+M\cos\omega_0 t)} e^{jny}\ dx\ dy \\ &= \frac{V_{dc}}{\pi^2} \int_{-\pi}^{\pi} [\pi(1 + M\cos\omega_0 t)e^{jny}]\ dy = \frac{V_{dc}}{\pi^2} \int_{-\pi}^{\pi} [e^{jny} + \frac{M}{2}(e^{j[n+1]y} + e^{j[n-1]y})]\ dy \end{aligned} \tag{3.10}$$

This can by further simplified given that $\int_{-\pi}^{\pi} e^{jny}\ dy = 0$ for all $n \neq 0$, which reduces to

$$A_{01} + jB_{01} = \frac{V_{dc}}{\pi^2} \int_{-\pi}^{\pi} \frac{M}{2}\ dy = V_{dc}M \tag{3.11}$$

since for all other values of n, $A_{0n} + jB_{0n}$ are equal to 0.

For $m > 0\ n = 0$, the coefficients of the carrier harmonics in (3.5) can be simplified to

$$\begin{aligned} A_{m0} + jB_{m0} &= \frac{V_{dc}}{\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M\cos\omega_0 t)}^{\frac{\pi}{2}(1+M\cos\omega_0 t)} e^{jmx}\ dx\ dy \\ &= \frac{V_{dc}}{\pi^2} \int_{-\pi}^{\pi} e^{jm\frac{\pi}{2}(1+M\cos\omega_0 t)} - e^{-\frac{\pi}{2}(1+M\cos\omega_0 t)}\ dx\ dy \end{aligned} \tag{3.12}$$

Using [19], the previous can be further simplified to

$$A_{m0} + jB_{m0} = \frac{2V_{dc}}{jm\pi} \left[e^{jm\frac{\pi}{2}} J_0\left(m\frac{\pi}{2}M\right) - e^{-jm\frac{\pi}{2}} J_0\left(-m\frac{\pi}{2}M\right) \right] \tag{3.13}$$

where J_0 is the Bessel function of first order. and $J_0(-\xi) = J_0(\xi)$ gives

$$A_{m0} + jB_{m0} = \frac{4V_{dc}}{m\pi} J_0\left(m\frac{\pi}{2}M\right) \sin m\frac{\pi}{2} \tag{3.14}$$

Finally for $m > 0$, $n \neq 0$, which represent the sideband harmonics in (3.5), the coefficients simplify to

$$\begin{aligned} A_{mn} + jB_{mn} &= \frac{V_{dc}}{jm\pi^2} \int_{-\pi}^{\pi} e^{jny} \left[e^{jm\frac{\pi}{2}(1+M\cos y)} - e^{-jm\frac{\pi}{2}(1+M\cos y)} \right] dy \\ &= \frac{V_{dc}}{jm\pi^2} \int_{-\pi}^{\pi} \left[e^{jm\frac{\pi}{2}} e^{jny} e^{jm\frac{\pi}{2}M\cos y} - e^{-jm\frac{\pi}{2}} e^{jny} e^{-jm\frac{\pi}{2}M\cos y} \right] dy \end{aligned} \tag{3.15}$$

According to [19] this can be rewritten as

$$\begin{aligned} A_{mn} + jB_{mn} &= \frac{2V_{dc}}{jm\pi} \left[e^{jm\frac{\pi}{2}} j^n J_n\left(m\frac{\pi}{2}M\right) - e^{-jm\frac{\pi}{2}} j^{-n} J_n\left(m\frac{\pi}{2}M\right) \right] \\ &= \frac{2V_{dc}}{jm\pi} J_n\left(m\frac{\pi}{2}M\right) \left[e^{jm\frac{\pi}{2}} e^{jn\frac{\pi}{2}} - e^{-jm\frac{\pi}{2}} e^{-jn\frac{\pi}{2}} \right] \end{aligned} \tag{3.16}$$

where J_n is the Bessel function of order n. With Eulers formula, the previous equation can be expressed as

$$A_{mn} + jB_{mn} = \frac{2V_{dc}}{jm\pi} J_n\left(m\frac{\pi}{2}M\right) \sin\left[(m+n)\frac{\pi}{2}\right] \tag{3.17}$$

The Fourier Series coefficients for the regular sampled PWM are derived in a similar manner, with different inner integral limits of (3.4). The inner integral limits of the regular sampled PWM can also be found by holding the solution trajectory shown in Figure 3.4 constant during each switching cycle. The unit cell representation of regular sampled PWM is shown in Figure 3.3(b). Figure 3.2 shows the repeated unit cell and the simplified version where the solution trajectory is held constant. The resulting Fourier Series coefficients for symmetrical regular PWM are described below.

For $m = 0$, $n = 0$, i.e. the DC offset is

$$A_{00} = 2V_{dc} \tag{3.18}$$

For $m = 0$, $n > 0$, the baseband harmonics can be derived with the same solution process leading to (3.11), but replacing m with $n(\omega_0/\omega_c)$, resulting in

$$A_{0n} + jB_{0n} = \frac{4V_{dc}}{\left[n\frac{\omega_0}{\omega_c}\right]\pi} J_n\left(n\frac{\omega_0}{\omega_c}\frac{\pi}{2}M\right) \sin\left(\left[n\frac{\omega_0}{\omega_c} + n\right]\frac{\pi}{2}\right) \tag{3.19}$$

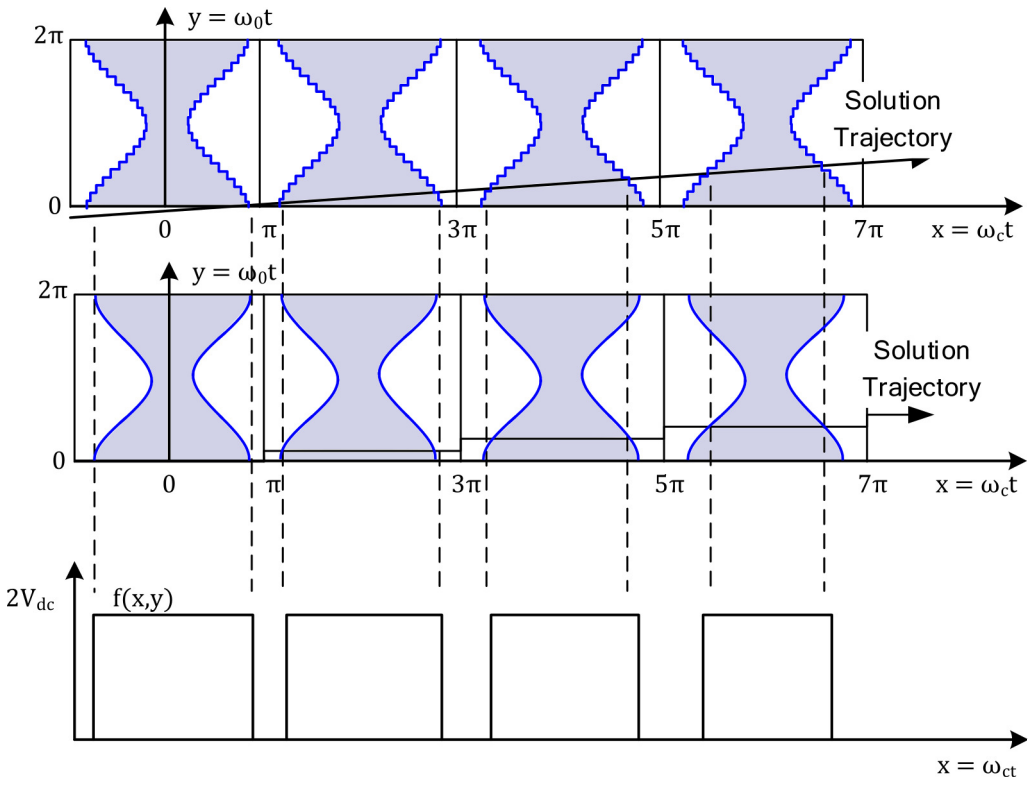


FIGURE 3.5: Switching pattern with double-edge PWM showing the intersections with regular sampling and the resulting output voltage

For $m > 0$, $n = 0$, with same derivation as for (3.14), the carrier harmonics are

$$A_{m0} + jB_{m0} = \frac{4V_{dc}}{m\pi} J_n\left(m\frac{\pi}{2}M\right)\sin m\frac{\pi}{2} \tag{3.20}$$

and finally for $m > 0$, $n \neq 0$, the sideband harmonics for symmetrically sampled PWM are derived as (3.17) but replacing m with $m + n(\omega_0/\omega_c)$, giving

$$A_{mn} + jB_{mn} = \frac{4V_{dc}}{\left[m + n\frac{\omega_0}{\omega_c}\right]\pi} J_n\left(\left[m + n\frac{\omega_0}{\omega_c}\right]\frac{\pi}{2}M\right)\sin\left(\left[m + n\frac{\omega_0}{\omega_c} + n\right]\frac{\pi}{2}\right) \tag{3.21}$$

The equations derived above represent the Fourier Series coefficients obtained with naturally and asymmetrical regular sampled PWM, which correspond to the harmonics of one leg of the full-bridge converter. The Fourier coefficients for the symmetrical regular sampled PWM have not been derived to avoid repetition, but can be found in [19].

3.3 Analysis of cell voltage harmonic content

A single-phase full bridge converter, illustrated in Figure 3.6, consists of two phase legs that are connected to a common DC bus, which for the system under consideration is a dc capacitor. Often the dc bus can be composed by two capacitors and the midpoint is denoted as z. The output voltage is the voltage between a and b [19]. The two phase-legs are switched with unipolar switching, which means one semi-conductor at a time is turned on or off as appose to bipolar switching where the two diagonal semi-conductors are controlled simultaneously. The phase-legs are modulated with 180° phase-shifted reference waveforms, and without any loss of generality the initial phase-shift can be chosen to 0 giving $\theta_0 = 0$ and $\theta_0 = \pi$. Based on the analysis presented in Section 3.2, the the full bridge phase-leg voltages are given as

$$v^*_{Az} = V_{dc} M \cos(\omega_0 t) \tag{3.22}$$

$$v^*_{Bz} = V_{dc} M \cos(\omega_0 t - \pi) \tag{3.23}$$

where M is the normalized output voltage magnitude, referred to as the modulation index, ranging between $0 < M < 1$. The fundamental output reference voltage is the difference between these

$$v^*_{AB} = v^*_{Az} - v^*_{Bz} = 2V_{dc} M \cos(\omega_0 t) \tag{3.24}$$

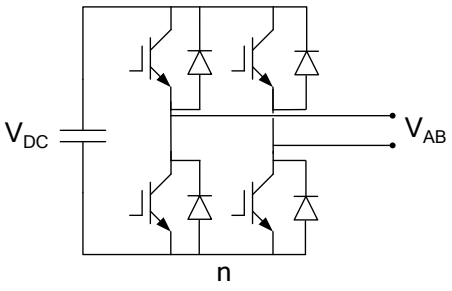


FIGURE 3.6: Circuit diagram of full-bridge converter (H-cell)

The actual output line-to-line waveform can thereby be calculated as the difference between output in phase-leg a and b. The carrier phase-angle θ_c can for simplicity be set to 0, and θ_0, as previously, can be set to 0 and $-\pi$ for phase-leg A and B respectively. The harmonic content in one phase-leg with naturally sampled PWM, can be derived by

combing Eq. (3.5) with Eq. (3.9), (3.11), (3.14) and (3.17), which gives

$$\begin{aligned} v_{An}(t) = \; & V_{dc} + V_{dc}M\cos(\omega_0 t + \theta_0) \\ & + \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}J_0\left(m\frac{\pi}{2}M\right)\sin m\frac{\pi}{2}\cos[m(\omega_c t + \theta_c)] \\ & + \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin[(m+n)\frac{\pi}{2}]\cos[m(\omega_c t + \theta_c) + n(\omega_0 t + \theta_0)] \end{aligned} \tag{3.25}$$

What can be noticed from the term $\sin\left[(m+n)\frac{\pi}{2}\right]$ in Eq. (3.25) is that if m and n are both even or odd simultaneously, the sideband harmonics are completely cancelled out. The harmonic solution for naturally sampled PWM can be expressed more compactly by expressing the voltage with respect to the DC bus midpoint instead as

$$\begin{aligned} v_{Az}(t) = \; & V_{dc} + V_{dc}M\cos(\omega_0 t) \\ & + \frac{4V_{dc}}{\pi}\sum_{\substack{m=0 \\ m>0}}^{\infty}\sum_{\substack{n=1 \\ n=-\infty}}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin[(m+n)\frac{\pi}{2}]\cos[m(\omega_c t + \theta_c) + n(\omega_0 t + \theta_0)] \end{aligned} \tag{3.26}$$

By inserting $\theta_c = 0$, $\theta_0 = 0$ and $\theta_0 = -\pi$ into (3.26) gives a harmonic solution for phase-leg a and b respectively. The voltage across phase-leg a is then given by

$$\begin{aligned} v_{Az}(t) = \; & V_{dc} + V_{dc}M\cos(\omega_0 t) \\ & + \frac{4V_{dc}}{\pi}\sum_{\substack{m=0 \\ m>0}}^{\infty}\sum_{\substack{n=1 \\ n=-\infty}}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin[(m+n)\frac{\pi}{2}]\cos(m\omega_c t + n\omega_0 t) \end{aligned} \tag{3.27}$$

and for phase-leg B

$$\begin{aligned} v_{bz}(t) = \; & V_{dc} + V_{dc}M\cos(\omega_0 t - \pi) \\ & + \frac{4V_{dc}}{\pi}\sum_{\substack{m=0 \\ m>0}}^{\infty}\sum_{\substack{n=1 \\ n=-\infty}}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin[(m+n)\frac{\pi}{2}]\cos[m\omega_c t + n(\omega_0 t - \pi)] \end{aligned} \tag{3.28}$$

using $\cos(\omega_0 t - \pi) = -\cos(\omega_0 t)$, the resulting voltage in both phase-legs is

$$\begin{aligned} v_{AB}(t) &= 2V_{dc}M\cos(\omega_0 t) \\ &+ \frac{4V_{dc}}{\pi}\sum_{\substack{m=0 \leftrightarrow \\ m>0 \leftrightarrow}}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin[(m+n)\frac{\pi}{2}] \\ &\times[\cos(m\omega_c t + n\omega_0 t) - \cos[m\omega_c t + n(\omega_0 t - \pi)]f] \end{aligned} \tag{3.29}$$

The second part of the term $\cos(m\omega_c t + n\omega_0 t) - \cos[m\omega_c t + n(\omega_0 t - \pi)]$ can be rewritten using trigonometry identities

$$\cos(\alpha - \beta) = \cos\alpha\cos\beta + \sin\alpha\sin\beta \tag{3.30}$$

Identifying α and β as $(m\omega_c t + n\omega_0 t)$ and $(n\pi)$ respectively, given that $\cos(n\pi) = (-1)^n$ and $\sin(n\pi) = 0$ gives

$$\cos(m\omega_c t + n\omega_0 t)(1 - (-1)^n) \tag{3.31}$$

The term above will be equal to 2 for odd values of n and 0 for even values. Since the term $\sin[(m+n)\frac{\pi}{2}]$ in (3.29) is only non-zero when (m + n) is an odd number and all even values of n are cancelled out by the previous term, m will only be even. This can be rewritten as $\cos[(m+n-1)\pi]$, giving the final expression as

$$\begin{aligned} v_{AB}(t) &= 2V_{dc}M\cos(\omega_0 t) \\ &+ \frac{8V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos[(m+n-1)\pi]\cos[2m\omega_c t + (2n-1)\omega_0 t] \end{aligned} \tag{3.32}$$

Similarly, by combining (3.18), (3.19), (3.20) and (3.21) and inserting into (3.5), the resulting phase-leg voltage with asymmetrical regular sampled PWM is given by

$$\begin{aligned} v_{An}(t) = \; & V_{dc} + \frac{4V_{dc}}{\pi} \sum_{n=1}^{\infty} \frac{J_n\left(n\frac{\omega_0}{\omega_c}\frac{\pi}{2}M\right)}{\left[n\frac{\omega_0}{\omega_c}\right]} \sin\left(n\frac{\pi}{2}\right) \cos[n(\omega_0 t + \theta_0)] \\ & + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0\left(m\frac{\pi}{2}M\right) \sin m\frac{\pi}{2} \cos[m(\omega_c t + \theta_c)] \\ & + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty} \frac{J_n\left[\left(m + n\frac{\omega_0}{\omega_c}\right)\frac{\pi}{2}M\right]}{\left[m + n\frac{\omega_0}{\omega_c}\right]} \sin\left[(m+n)\frac{\pi}{2}\right] \cos\left[m(\omega_c t + \theta_c) + n(\omega_0 t + \theta_0)\right] \end{aligned} \tag{3.33}$$

By rewriting Eq.(3.33) with respect to the DC bus midpoint instead, the equation can be further simplified to

$$v_{Az}(t) = \frac{4V_{dc}}{\pi} \sum_{\substack{m=0 \leftrightarrow \\ m>0 \leftrightarrow}}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_n\left[\left(m + n\frac{\omega_0}{\omega_c}\right)\frac{\pi}{2}M\right]}{\left[m + n\frac{\omega_0}{\omega_c}\right]} \sin\left[(m+n)\frac{\pi}{2}\right] \cos\left[m(\omega_c t + \theta_c) + n(\omega_0 t + \theta_0)\right] \tag{3.34}$$

and inserting θ_0 and θ_c as for (3.27) and (3.28) gives

$$\begin{aligned} v_{Az}(t) = \; & V_{dc} + V_{dc} M \cos(\omega_0 t) \\ & + \frac{4V_{dc}}{\pi} \sum_{\substack{m=0 \leftrightarrow \\ m>0 \leftrightarrow}}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_n\left[\left(m + n\frac{\omega_0}{\omega_c}\right)\frac{\pi}{2}M\right]}{\left[m + n\frac{\omega_0}{\omega_c}\right]} \sin\left[(m+n)\frac{\pi}{2}\right] \cos\left(m\omega_c t + n\omega_0 t\right) \end{aligned} \tag{3.35}$$

for phase-leg a, while for phase-leg b, we have

$$\begin{aligned} v_{Bz}(t) = \; & V_{dc} + V_{dc} M \cos(\omega_0 t - \pi) \\ & + \frac{4V_{dc}}{\pi} \sum_{\substack{m=0 \leftrightarrow \\ m>0 \leftrightarrow}}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_n\left[\left(m + n\frac{\omega_0}{\omega_c}\right)\frac{\pi}{2}M\right]}{\left[m + n\frac{\omega_0}{\omega_c}\right]} \sin\left[(m+n)\frac{\pi}{2}\right] \cos\left[m\omega_c t + n(\omega_0 t - \pi)\right] \end{aligned} \tag{3.36}$$

Subtracting v_{bz} from v_{az} and applying the same simplifications as for (3.32), gives

$$v_{AB}(t) = 2V_{dc}M\cos(\omega_0 t) + \frac{8V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos[(m+n-1)\pi]\cos[2m\omega_c t + (2n-1)\omega_0 t] \tag{3.37}$$

This represents the total harmonic content in one converter cell.

3.4 Analysis of total phase-voltage and current

As mentioned in the previous chapter, in the PS-PWM, there is a phase-shift between each carrier corresponding to one cell. The principles of the PS-PWM for a three level, full-bridge composed MMC is illustrated in Figure 3.7. The desired carrier phase-shifts

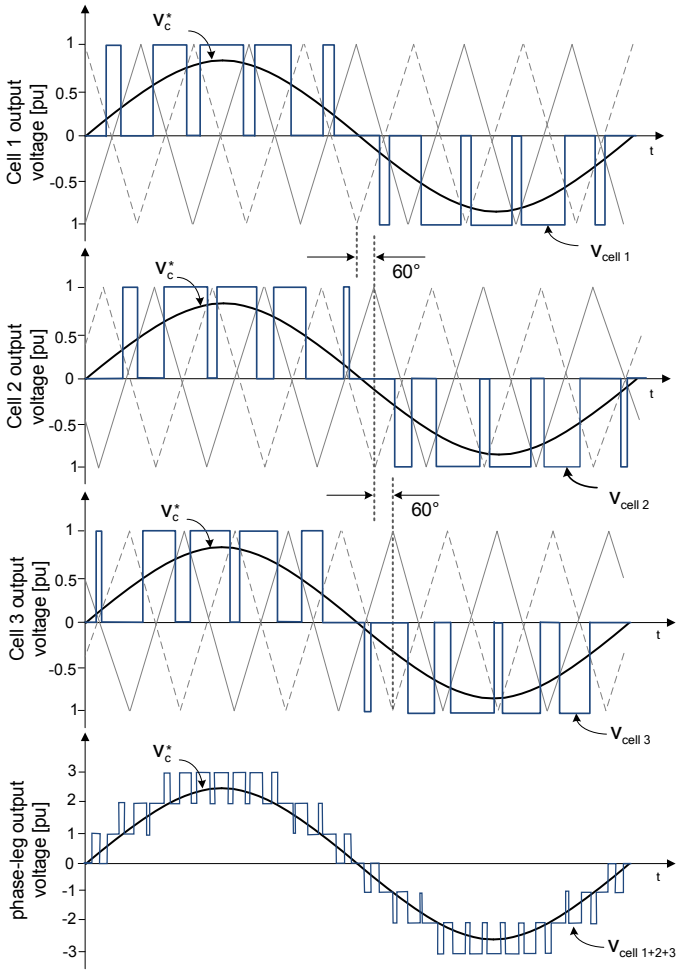


FIGURE 3.7: Figure of PS-PWM waveforms for a three-cell MMC

for an N-level converter are those that result in complete cancelation of carrier harmonics. The cancellation is achieved when the last term in (3.43) is added to zero for all cells. If the cell voltages are formulated in vector forms, cancellation is achieved when the sum of all vectors is equal to zero, as illustrated in Figure 3.8. The angles of the vectors are $2\theta_c$ from (3.43), thus the phase-shift in the carriers should be selected to half of that required to cancel the vectors out. The phase-shift for cell i can thereby be written as:

$$\theta_{c(i)} = \frac{(i-1)\pi}{N} \qquad i \in \mathbb{N}^+ \tag{3.38}$$

where N is the number of cells in one phase-leg and i is the cell-number.

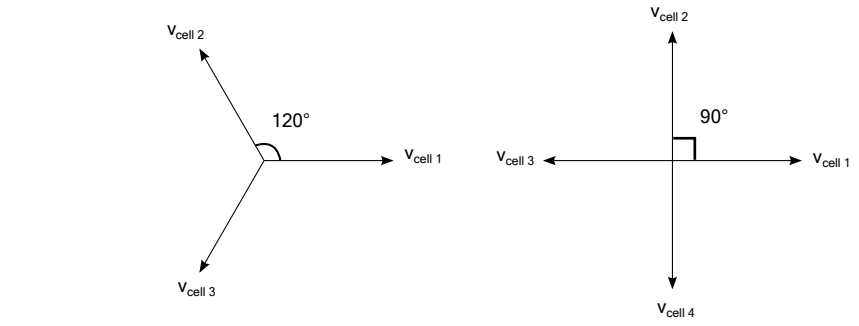


FIGURE 3.8: Phase-shift selection for a cell number of 3 and 4

The cluster voltage of a cascaded N-level MMC with PS-PWM and natural sampling, can be derived by adding the voltages of the individual cells:

$$\begin{aligned} v_{ab(i)}(t) &= 2V_{dc}M\cos(\omega_0 t) \\ &+ \frac{8V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos([m+n-1]\pi)\cos(2m[\omega_c t+\theta_c]+[2n-1]\omega_0 t) \end{aligned} \tag{3.39}$$

giving a total phase-leg voltage of

$$v_{az} = \sum_{i=1}^{N} v_{AB(i)}(t) \tag{3.40}$$

For simplification, the cell voltage v_{AB} in the continuation is referred to as $v_{a(i)}$, where (i) represents the cell number.

$$\begin{aligned} v_{az} &= NV_{dc}M\cos(\omega_0 t) \\ &+ \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos([m+n-1]\pi) \\ &\qquad \times \sum_{i=1}^{N}\cos\left(2m\left(\omega_c t + \frac{[i-1]\pi}{N}\right) + [2n-1]\omega_0 t\right) \end{aligned} \tag{3.41}$$

and since

$$\sum_{i=1}^{N}\cos\left(2m\omega_c t + [2n-1]\omega_0 t + \frac{2m[i-1]\pi}{N}\right) = 0 \tag{3.42}$$

for all $m \neq kN, k = 1, 2, 3...,$, the expression above cancels all harmonics up to $2N^{th}$ harmonic; (3.41) can be expressed as

$$\begin{aligned} v_{az}(t) &= 4NV_{dc}M\cos(\omega_0 t) \\ &+ \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos([Nm+n-1]\pi) \\ &\qquad \times \cos(2Nm\omega_c t + [2n-1]\omega_0 t) \end{aligned} \tag{3.43}$$

For the investigated system (N=3), the carrier phase-shifts θ_c can be calculated using (3.38) to 0, $\frac{\pi}{3}$ and $\frac{2\pi}{3}$ respectively, and sideband harmonic cancellation will be achieved up to $2mf_cN = 6mf_c$.

The analytical solution for the phase-leg voltage with asymmetrical regular sampled PWM is given by

$$\begin{aligned} v_{az}(t) &= 8V_{dc}M\cos(\omega_0 t)\sum_{n=1}^{\infty}\frac{1}{n\frac{\omega_0}{\omega_c}}J_n\left(n\frac{\omega_0}{\omega_c}\frac{\pi}{2}M\right)\sin n\frac{\pi}{2}\cos(n\omega_0 t) \\ &+ \frac{8V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{q'}J_{2n-1}(q'\pi M)\cos([Nm+n-1]\pi) \\ &\qquad \times \cos(2Nm\omega_c t + [2n-1]\omega_0 t) \end{aligned} \tag{3.44}$$

with

$$q' = 2Nm + [2n-1]\frac{\omega_0}{\omega_c} \tag{3.45}$$

The first summation term in (3.44) represents the baseband harmonics and the second summation term represents the sideband harmonics.

As described in Chapter 2 the instantaneous current in phase a can be expressed as:

$$i_a(t) = \frac{1}{L_{ac}} \int e_a(t) - v_a(t)dt \tag{3.46}$$

which means that the current harmonics are determined by the phase-leg voltage and not the individual cell-voltage. Assuming that the grid voltage e_a is ideal, it will only contain a fundamental component and will not introduce harmonic pollution in the current. Therefore, " " harmonic components different than the fundamental, the grid can be represented as a short circuit to ground. For simplification, the converter output voltage v_a can be used for analyzing the harmonic components in the current.

3.5 Impact of harmonics on cell-voltage balancing under ideal conditions

As derived above, each of the harmonic spectral models contains a fundamental component that is in phase with the sinusoidal reference waveform. Under unipolar switching, there is also a DC component in the PWM output waveform. The carrier related harmonics can be divided into two groups, which are

1. Carrier frequency harmonics, located at $f = mf_c, \forall\ m \in \mathbb{Z}^+$
2. Sideband harmonics of the carrier harmonics, located at $f = mf_c + nf_0, \forall\ m \in \mathbb{Z}^+,\ n \in \mathbb{Z}$ and with an amplitude of

$$\frac{2}{m\pi} J_n(\frac{m\pi M}{2}) \tag{3.47}$$

When the carrier frequency, f_c, is chosen to twice the fundamental frequency, f_0, the frequency of the sideband component for $m = 1$ and $n = -1$ is

$$f = f_c - f_0 = 2f_0 - f_0 = f_0, \tag{3.48}$$

which is the same as the fundamental frequency. The amplitude of this component can be calculated to

$$\frac{2}{\pi}J_{-1}(\frac{\pi M}{2}) \times \cos[m(\omega_c t + \theta_c) + n(\omega_0 t + \theta_0)] \tag{3.49}$$

In general, sideband harmonics will appear whenever the following is fulfilled

$$f_0 = \frac{mf_c}{1-n} \qquad \forall\ m \in \mathbb{Z}^+,\ n \in \mathbb{Z} \tag{3.50}$$

The amplitude of the sideband component is determined by the Bessel function which is proportional to

$$\frac{x^{|n|}}{2^{|n|}n!},$$

and the effect from such interaction is negligible for higher values of n. More specifically, the only values of n that would actual have a large impact are $n = 0$ and $n = -1$. Which means the claim above can be limited to

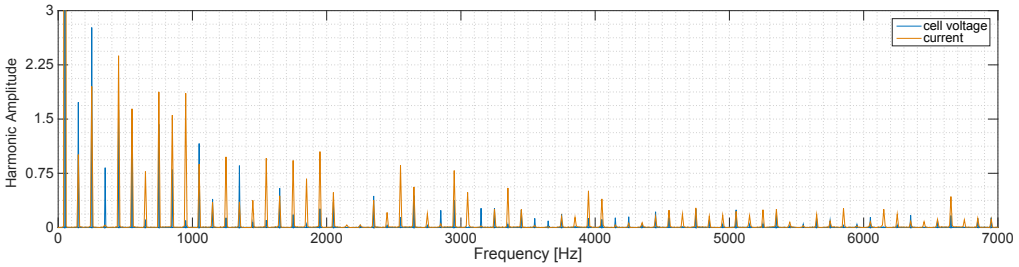
$$f = \frac{mf_c}{2}, \forall\ m \in \mathbb{Z}^+, \tag{3.52}$$

The result of a sideband harmonic appearing at the fundamental frequency is an interaction between cell voltage and current harmonics, which might result in active power production. This power production will, unless the current harmonics either leads or lags the voltage harmonics by 90°, have an active power component. Depending on the polarity of the active power produced, this will result in the capacitors either getting charged or discharged. If this occurs repeatedly, the capacitor voltages will deviate. To counteract this, each capacitor must be equipped with an individual balancing controller that prevents the capacitor voltages from deviating outside of their rated values.
The capacitor voltages can be calculated by

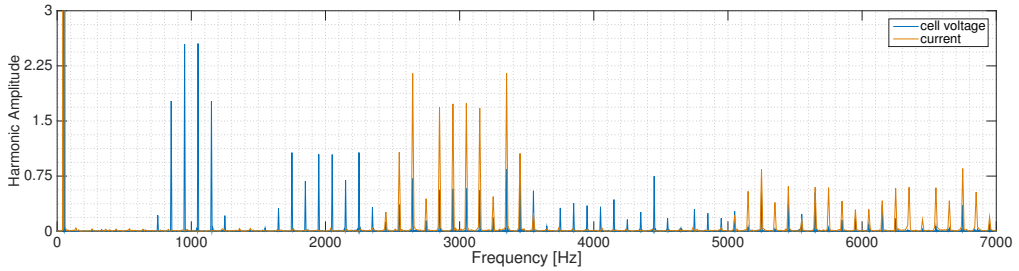
$$v_{ac}(t) = v_{dc}(t)v_{pwm}(t) \tag{3.53}$$

where v_{ac}, v_{dc} represent the AC, DC side cell voltages respectively, and v_{pwm} is the switching pattern derived above. If the DC voltage is constant, v_{ac} will be proportional to v_{dc}.

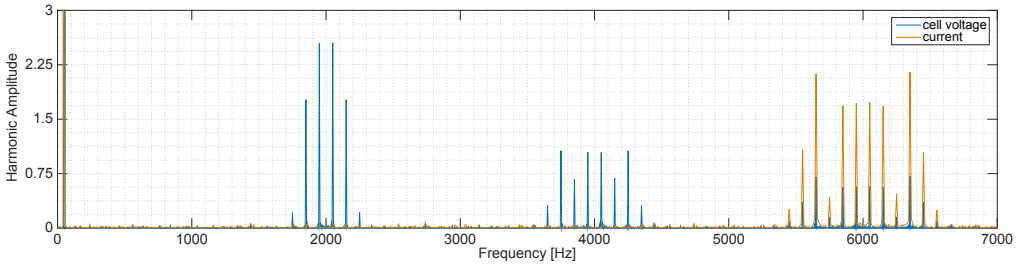
Figure 3.9(a) shows the sideband harmonic locations for different modulation indices, more specifically for $m_f = 2$, $m_f = 10$ and $m_f = 20$.



(a) $m_f = 2$



(b) $m_f = 10$



(c) $m_f = 20$

FIGURE 3.9: FFT analysis of cell and phase-leg voltage for various values of m_f.

As can be seen from the figure, by increasing the switching frequency, the impact of the interaction can be prevented. Another alternative is increasing the cell-number, which decreases the amplitude of the harmonics and thus the impact of the interaction. At high switching-frequency, around 1000 Hz, the interaction between the current fundamental and voltage sideband harmonics will occur for $(m = 1)$ at $(n = -19)$, which is insignificant.

In practice, the converter is designed to give a as sinusoidal current waveform as possible. This means that if the switching frequency is low, the cell number is chosen to be high and vice versa. Since a cell number of three is chosen in this work, the frequency should be high. Although this is not realistic for STATCOM applications due to the high power ratings and the rating limitations in todays semi conductors.

3.6 Impact of harmonics on cell-voltage balancing under non-ideal conditions

As mentioned earlier, when the STATCOM is connected to an infinitely strong grid, the current harmonics are determined by the phase-leg voltage. With PS-PWM, the phase-leg harmonics are cancelled up to $2Nf_c$ if double-edge modulation is used (Nf_c for single-edge modulation). This is however only true under ideal conditions. If, for example, there is a difference in dc bus voltages, or if the phase-shifts among the different cells are non-ideal, which is often the case, adding the harmonics in one phase-leg will not lead to a complete cancellation. As a result, current harmonics will appear at frequencies below $6f_c$ and might interact with the voltage sideband harmonics. As in the case of low switching frequency, the interaction will not result in the same active power production in the different cells. Consequently, the cells will be unevenly charged or discharged causing the voltages to deviate. The harmonics will have the same impact on the balancing of the dc capacitors as the baseband harmonics for the low switching frequency case. However, the amplitudes of the sideband harmonics are significantly smaller than the fundamental. This results in a much slower deviation process but, over time, an individual balancing controller is still required.

Considering for example that the dc capacitor voltages in the three cells in one cluster are unequal, the three cell voltages are given by

$$v_{a1}(t) = 2V_{dc1}M\cos(\omega_0 t) + \frac{8V_{dc1}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos([m+n-1]\pi)\cos(2m\omega_c t + [2n-1]\omega_0 t) \tag{3.54}$$

$$v_{a2}(t) = 2V_{dc2}M\cos(\omega_0 t) + \frac{8V_{dc2}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos([m+n-1]\pi)\cos\left(2m\omega_c t + \frac{2m\pi}{3} + [2n-1]\omega_0 t\right) \tag{3.55}$$

$$v_{a3}(t) = 2V_{dc3}M\cos(\omega_0 t) + \frac{8V_{dc3}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos([m+n-1]\pi)\cos\left(2m\omega_c t + \frac{4m\pi}{3} + [2n-1]\omega_0 t\right) \tag{3.56}$$

Adding (3.54), (3.55) and (3.56) gives

$$\begin{aligned} v_a = {} & 2M\cos(\omega_0 t)(V_{dc1}+V_{dc2}+V_{dc3}) \\ & + \frac{8}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\times\cos([m+n-1]\pi) \\ & \times[V_{dc1}\cos(w)+V_{dc2}\cos(w')+V_{dc3}\cos(w'')] \end{aligned} \tag{3.57}$$

where

$$w = (2m\omega_c t + [2n-1]\omega_0 t) \tag{3.58}$$

$$w' = \left(2m\omega_c t + \frac{2m\pi}{3} + [2n-1]\omega_0 t\right) \tag{3.59}$$

$$w'' = \left(2m\omega_c t + \frac{4m\pi}{3} + [2n-1]\omega_0 t\right) \tag{3.60}$$

Due to the term $[V_{dc1}\cos(w)+V_{dc2}\cos(w')+V_{dc3}\cos(w'')]$ in (3.57), with $V_{dc1}\neq V_{dc2}\neq V_{dc3}$, a 120° phase-shift between the cosine terms will not add up to 0 for harmonics located around $2f_c$ and $4f_c$, as in the ideal case. Since the current harmonics are located at the same frequencies as the phase-leg voltage harmonics, the harmonics that are not eliminated in the phase-leg voltage harmonics will inevitably interact with corresponding cell voltage harmonics. This means there will be an interaction between the sideband harmonics of the current and cell voltage. The consequences of these interactions can lead to active power production which can, depending on the direction of the current, lead to charging or discharging of the dc capacitors. The result of an interaction between the non-ideally cancelled current harmonics and cell voltage harmonics in cell number 1 can be determined by

$$V_{dc1}\cos(w) * (V_{dc1}\cos(w)+V_{dc2}\cos(w')+V_{dc3}\cos(w'')) \tag{3.61}$$

3.7 Non-integer frequency modulation index and impacts on cell-voltage balancing

The problem with capacitor voltage deviation described above can be improved by selecting a non-integer frequency modulation index. For the low switching frequency, during ideal conditions, the impact of an interaction between current fundamental component and voltage sideband harmonics can be significantly decreased with a non-integer m_f. If m_f is a non-integer, there will be no interaction between the sideband harmonics and the current fundamental component for all non-integer values of $m * m_f$. Each cluster consists of three cells, all with different carrier phase-shifts. As discussed earlier, the phase-shifts of the carriers is what determines if the dc capacitors are charged or discharged. To evenly distribute the power among all cells in one cluster, the carriers should be swapped among the cells. However, swapping of carriers results in an abrupt change of phase-shift, which can have negative effects on the overall system performance. By choosing a non-integer m_f, that at the end of one reference wave period is phase-shifted compared to the reference by 60° (for a cluster consisting of three cells), a continuous carrier swap is achieved. If, for example, m_f is chosen to $20+\frac{1}{6}$, the phase-shift after one fundamental period cycle (one fundamental period) is equal to 0, $\frac{\pi}{3}$ and $\frac{2\pi}{3}$. After each cycle, the phase-shift in each cell is further shifted by $\frac{\pi}{3}$. Figure 3.10 shows the carrier and reference voltage in one cell, with an integer and non-integer m_f. The dashed grey lines represent the integer m_f and the blue one is the non-integer m_f, the red graph is the sinusoidal reference waveform.

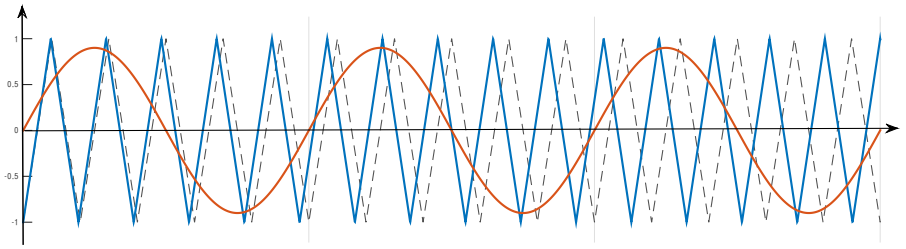


FIGURE 3.10: Figure of PWM with integer and non-integer m_fs

The result of such selection of m_f is a cell voltage output waveform that is no longer periodic in one fundamental period, but in three. In general, the non-integer m_f in such

way that the phase-shift is equivalent to carrier swapping after one fundamental cycle. For N' number of cells, the phase-shift is chosen to $\frac{360^\circ}{2N'}$.

To analyze the harmonic spectra for a non-integer m_f, an alternative method to the Double Fourier Series has been used. This method, presented in [20], is based on decomposing the output waveform into single square components. The pulse train function, $p_k(t)$ can represent any periodic PWM output waveform with a constant duty ratio. However, the duty ratio with a sinusoidal reference varies and each square wave can instead be given by a unit pulse function given as

$$w_k(t) = u(t-(k-1)T_s) - u(t-kT_s) \qquad k = [1, 2, ..., N'm_f] \tag{3.62}$$

where $u(t)$ is the unit step function, T_s is the carrier frequency and k is the specific pulse train number. Additionally, each $w_k(t)$ is assumed to be periodic with the fundamental period, T_0, or multiples of it incase of a non-integer m_f. With a non-integer m_f, that results in an output cell voltage waveform that repeats in 3 fundamental periods. The overall pulse train function can be expressed as

$$p(t) = \sum_{k=1}^{n} [w_k(t) \times p_k(t)] \tag{3.63}$$

where n must be a multiple of the periodicity of the output pulse train. Equation 3.63 can be extended to a more generic case, including a phase-shift in the pulse pattern, giving

$$p^{(\alpha_i)}(t) = \sum_{k=1}^{n} [w_k^{(\alpha_i)}(t) \times p_k^{(\alpha_i)}(t)] \tag{3.64}$$

where the phase-shift α is expressed as a fraction of the carrier period, i.e. a phase-shift of 180° corresponds to $\alpha = 0.5$. The two phase-legs of the full bridge cell can be expressed as

$$p_a(t) = \sum_{k=1}^{n} [w_k(t) \times p_k(t)] \tag{3.65}$$

$$p_b(t) = \sum_{k=1}^{n} [w_k^{(0.5)}(t) \times p_k^{(0.5)}(t)] \tag{3.66}$$

the full bridge voltage can by obtained by subtracting $p_b(t)$ from $p_a(t)$, through some simplification given in [20], the resulting pulse train pattern can be expressed as

$$p(t) = \sum_{k=1}^{n} w_k(t) \left[p_k(t) - p_k \left(t - 0.5T_s \right) \right] \tag{3.67}$$

where i represents the cell number.

Since both $w_k(t)$ and $p_k(t)$ are periodic with N' times the fundamental period, they can be represented by a Fourier Series as

$$p_k(t) = \sum_{i=-\infty}^{\infty} \{ P_k[i] e^{j2\pi i N' f_0 t} \} \tag{3.68}$$

$$w_k(t) = \sum_{i=-\infty}^{\infty} \{ W_k[i] e^{j2\pi i N' f_0 t} \} \tag{3.69}$$

The Fourier Series Coefficients $P_k[i]$ and $W_k[i]$ can be calculated by

$$P_k[i] = \int_0^{N'T_0} p_k e^{-j2\pi i N' f_0 t} dt \tag{3.70}$$

$$W_k[i] = \int_0^{N'T_0} w_k e^{-j2\pi i N' f_0 t} dt \tag{3.71}$$

According to [21], 3.70, 3.71 and 3.63, can be combined to

$$P[i] = \sum_{k=1}^{N'm_f} \left\{ \sum_{m=-\infty}^{\infty} W_k[m] \times P_k[i-m] \right\} \qquad \forall i \in \mathbb{Z} \tag{3.72}$$

To determine the current waveform, the patterns must be modified by the corresponding phase-shifts. The cell pattern with a 60° phase shift is given by

$$p(t)_2 = \sum_{k=1}^{n} w_k(t) \left[p_k \left(t - \frac{1}{6} T_s \right) - p_k \left(t - \frac{4}{6} T_s \right) \right] \tag{3.73}$$

and for 120° phase-shift

$$p(t)_3 = \sum_{k=1}^{n} w_k(t) \left[p_k \left(t - \frac{2}{6} T_s \right) - p_k \left(t - \frac{5}{6} T_s \right) \right] \tag{3.74}$$

The pulse patterns for the phase-leg voltage can be obtained by adding all the cell voltages, resulting in

$$p_{sum}(t) = \sum_{i=1}^{N'} p(t)_i \tag{3.75}$$

The Fourier representation can be derived similarly as for the phase-leg voltage.

This represents the phase-leg voltage and can, as explained in Chapter 2, be used to determine the harmonic components of the current. As oppose to using the double Fourier integral analysis, the pulse-train decomposition method does not requite that the frequencies of the carrier waveform is an integer multiple of the reference waveform.

Chapter 4

Impact of frequency modulation index on cell balancing

This chapter describes the PSCAD model used to investigate the effect of different frequency modulation indexes on the capacitor balancing. It is shown that proper selection of m_f allows certain improvement of the active power distribution among the different cells. Further, a brief discussion about the results is provided.

4.1 PSCAD model

The system described in Chapter 2 is the one that was implemented in PSCAD and used to perform the simulations. The main building blocks for the simulation models consist of a controller, a modulator and a converter model. The converter model is composed of 9 converter cells. Each cell is modelled with 4 IGBTs along with their anti-parallel diodes and a dc capacitor. The IGBTs are triggered with individual trigger signals (unipolar switching) that are obtained from the PMW pattern.

In addition to this, each cell capacitor is fed with an external voltage, to simulate a closed loop system. The voltage feeding the capacitors is obtained from a controller. The control includes a cluster voltage P-controller with an inner current PI-controller that regulate the average phase-leg voltage, and a individual balancing controller.

Figure 4.1(a) shows the PSCAD model of the converter, including the AC filter and the controller is shown in Figure 4.1(b).

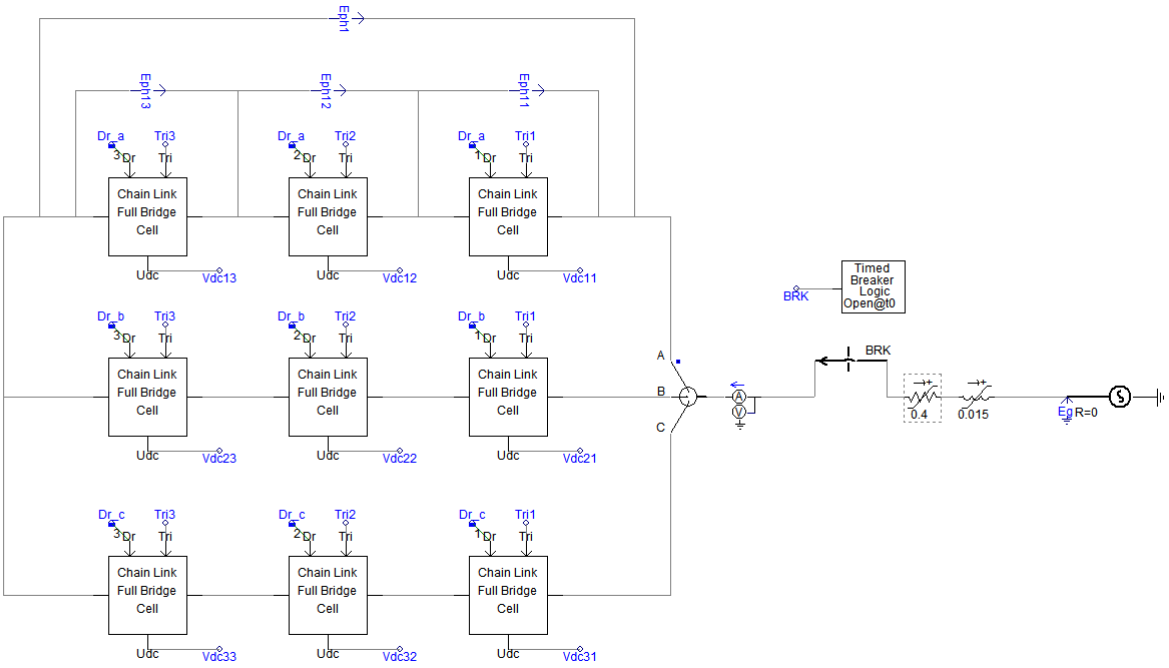
4.2 The role of the individual balancing controller

As discussed in Chapter 2, due to the voltage deviation issue, each capacitor voltage is independently controlled with a individual balancing control loop to keep the capacitor voltages within the desired voltage levels. The control loop in this model is a simple P-controller that calculate the error voltage, i.e. the difference between the capacitor reference voltage and the measured voltage. The P controller is used to control the error to 0. On the other hand, to investigate the voltage imbalance and the impact of m_f on the power distribution, the individual balancing controller must be removed. When removing the individual balancing controller, the dc capacitors are replaces with fixed dc sources. The modulation index is defined as $\frac{V_{dc}}{V_{ref}}$. The reason for this is if V_{dc} increases enough, the converter will be over-modulated, which could results in pulse-skipping. Figure 4.2 shows the pulse patterns and the intersections between the carrier and reference waveform with V_{dc} equal to $10kV$, $2kV$ and $11kV$. To compute an FFT analysis, the pulse patterns must be periodic. If the voltage levels change, the waveform will not be periodic so when computing the FFT analysis, the dc capacitors where replaced with fixed dc sources instead.

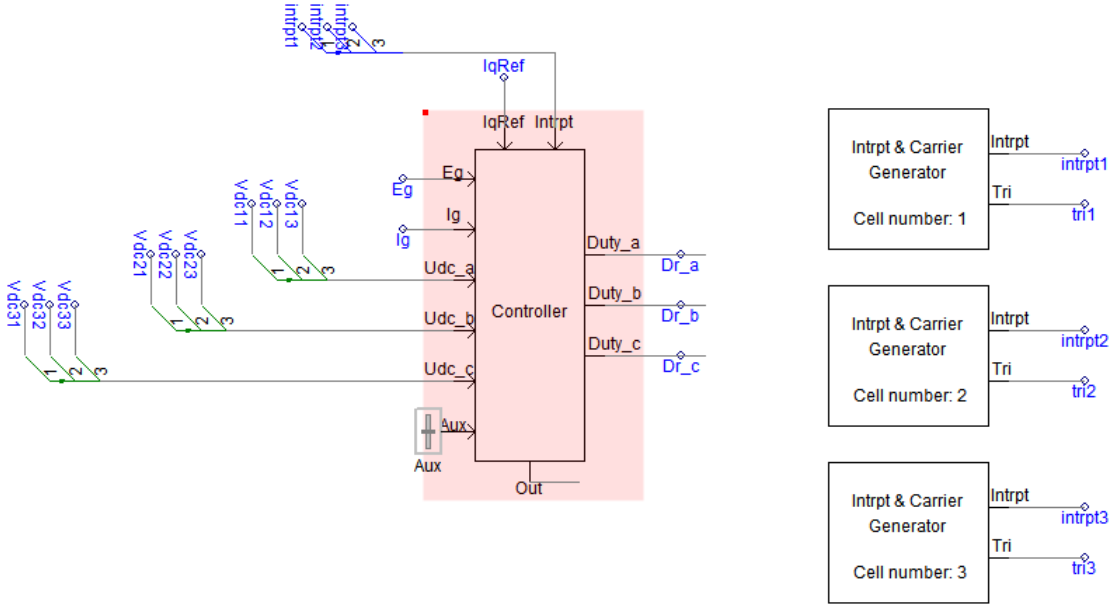
4.3 Simulation results with low switching frequencies

The simulations at low switching frequency are performed with a frequency modulation index of 7, and their non-integer equivalents 7.16, which correspond to switching frequencies of 350 and 358.33 respectively. Figure 4.3 shows the capacitor voltage deviation with a integer vs non integer frequency modulation index. As can be seen in the figure, the voltage ripple is significantly decreased with a non integer frequency modulation index and the deviation is prevented.

Figure 4.4 show the FFT analysis of the output cell voltages and the current. More specifically, it shows the current baseband harmonics and the voltage sideband harmonics.



(a) Converter model from PSCAD



(b) Controller from PSCAD

FIGURE 4.1: Model of the converter and controller in PSCAD

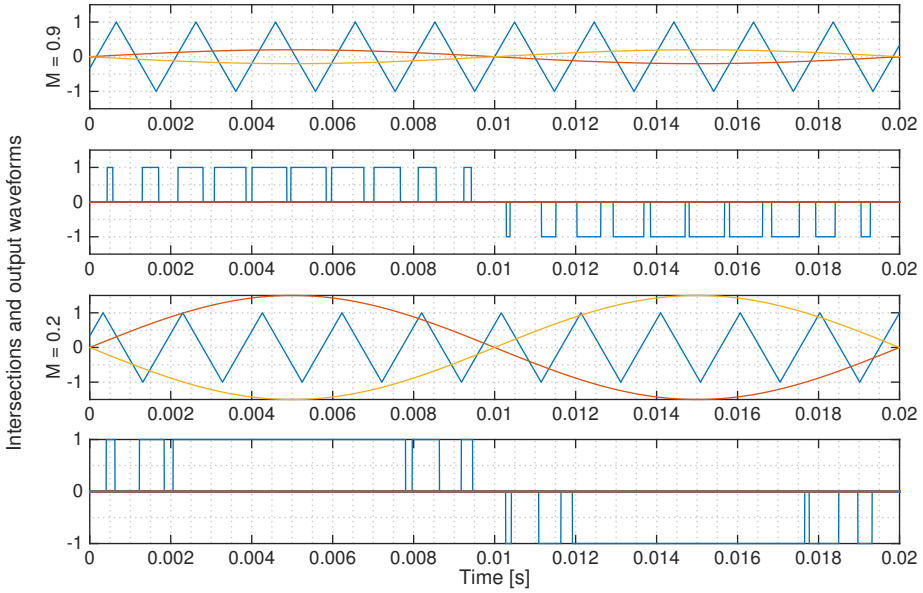
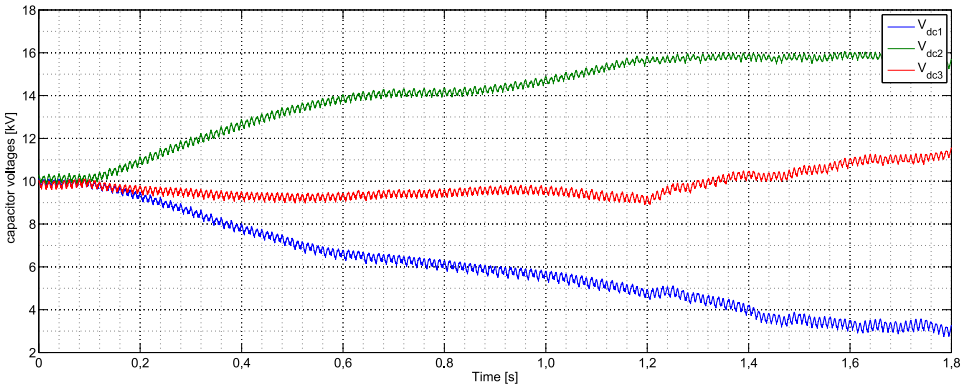
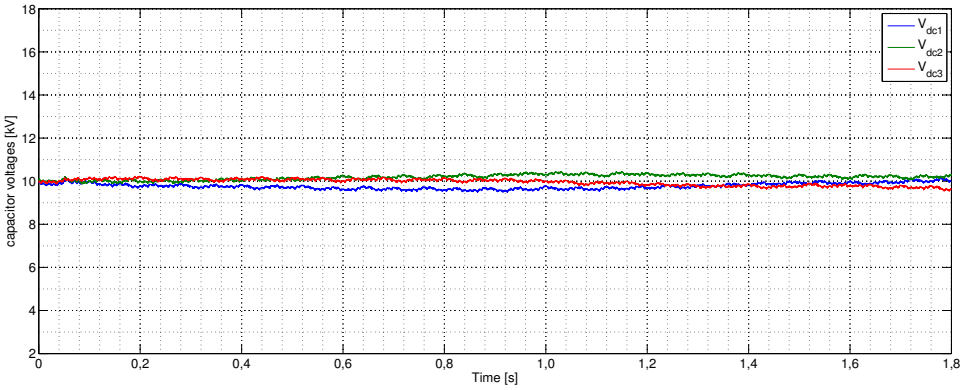


FIGURE 4.2: Switching intersections and the resulting output voltage



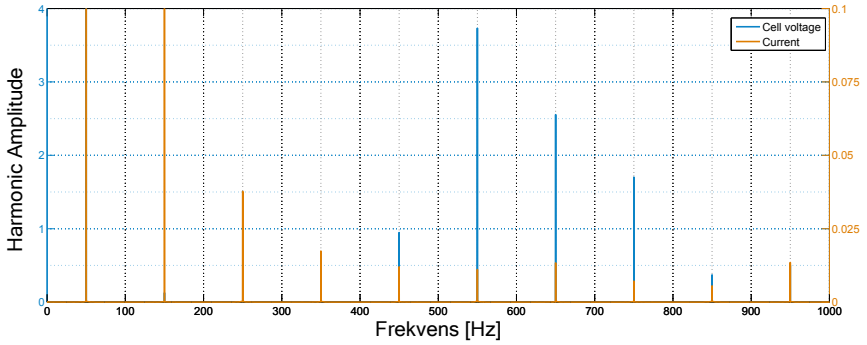
(a) Capacitor voltages with $m_f = 7$



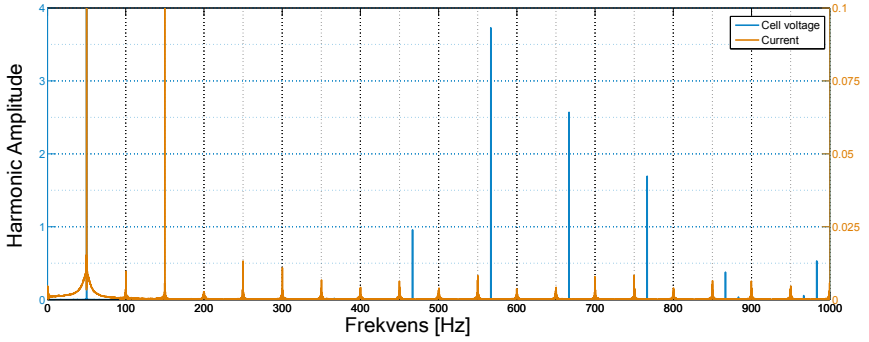
(b) $m_f = 7.16$

FIGURE 4.3: Capacitor voltages with $m_f = 7$ and $m_f = 7.16$

As seen in the figures, there is an interaction between the cell voltage harmonics and the current harmonics with the integer m_f but not with the non-integer m_f . The effect of an interaction between current and voltage harmonics will result in an active power production that will either charge or discharge the capacitors depending on the phase of the power. The FFT was computed with fixed dc capacitors and a duration of 5 seconds. By using fixed dc capacitors, the difference in harmonic spectra with different modulation indices can be studied without the effect from a voltage deviation.



(a) FFT cell voltage and current with $m_f = 7$

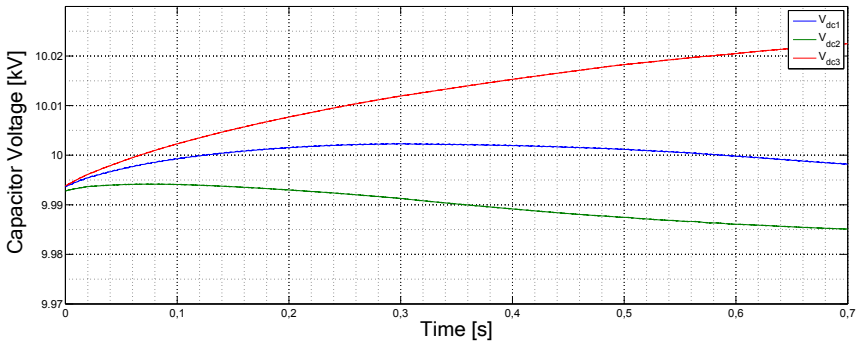


(b) FFT cell voltage and current with $m_f = 7.16$

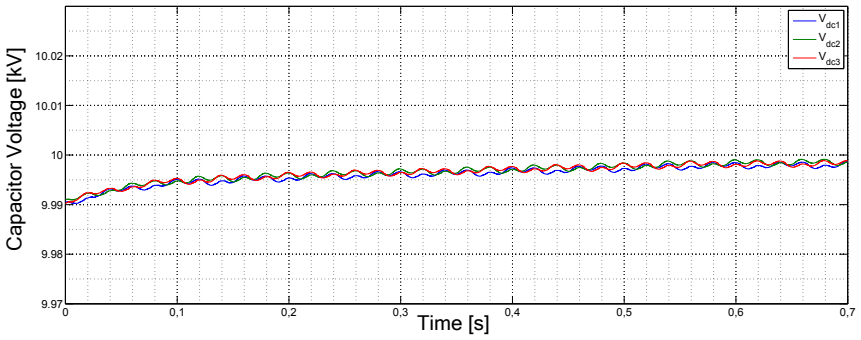
FIGURE 4.4: FFT of cell voltage and current with $m_f = 7$ and $m_f = 7.16$

4.4 Simulation results with high switching frequencies

The capacitor voltages with $m_f = 20$ and $m_f = 20.16$ are illustrated in Figure 4.5(a) and Figure 4.5(b) respectively. Similarly as for the low switching frequency case, the figures show that the capacitors quickly deviate from their nominal values with the integer m_f while for the non-integer, they are kept close to their nominal values.



(a) Capacitor voltages with $m_f = 20$

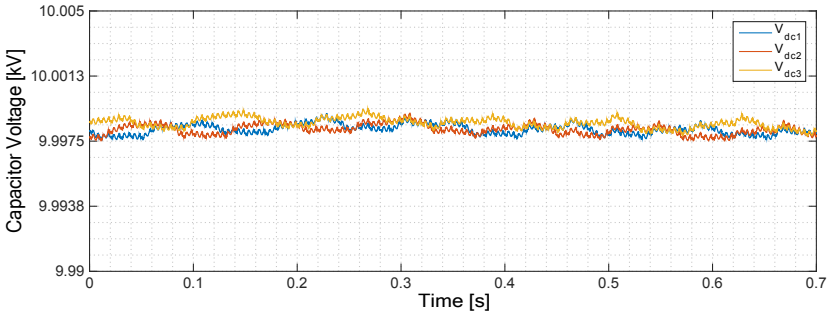


(b) $m_f = 20.16$

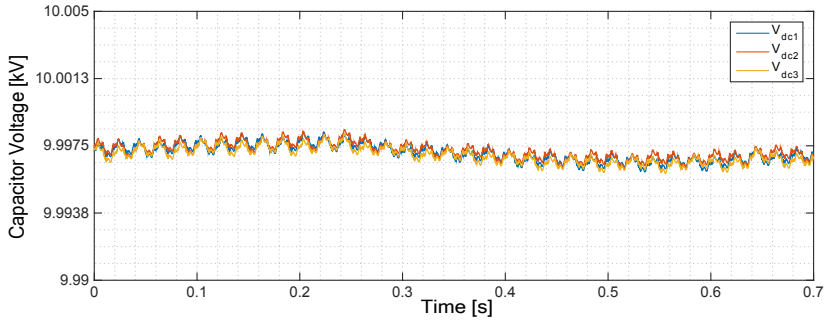
FIGURE 4.5: Capacitor voltages with $m_f = 20$ and $m_f = 20.16$

By introducing a non-integer m_f that gives an output cell waveform with a periodicity of 3 fundamental periods, the voltage deviation process is minimized. For comparison, the capacitor voltages with a $m_f = 20.083$ are shown in Figure 4.6(a) which is the equivalent of having 6 fundamental periods as the output voltage period. The results show that the voltage deviation is smaller for the non-integer modulation index with 3 fundamental periods as the output voltage period. Since the sum of the active power produced in one cluster during one cycle is 0, there is an equal amount of positive and negative power produced. This means that if one capacitor is charged, another one has to be discharged. By swapping the phase-shift of a carrier after one cycle, the capacitors will get both charged and discharged.

What should be noticed is that the capacitor voltage deviation is 300 times larger for the low integer case compared to the high switching frequency case, when a integer frequency modulation index is used. For the low switching frequency case, there is an interaction between voltage sideband harmonics and current fundamental component which has a significantly higher amplitude compared to current sideband harmonics.



(a) Capacitor voltages with $m_f = 20.083$



(b) $m_f = 20.16$

FIGURE 4.6: Capacitor voltages with $m_f = 20.083$ and $m_f = 20.16$

When computing the FFT analysis, two cases are considered. In the first case, the FFT was computed on 20 carrier periods, and repeated 10 times to increase the resolution of the FFT. In the second case, the waveform analyzed with the FFT corresponded to 250 fundamental periods (5 seconds) instead.

The results, Figure 4.7(a) and Figure 4.7(b), show that the cell voltage and current harmonics are located around the same frequencies regardless of how many fundamental periods the FFT considers. For $m_f = 20.16$ instead, the FFT analysis with a 20 carrier periods and 5 seconds are shown in Figures 4.7(c) and 4.7(d). As can be seen in the figures, the current harmonics are not located as the same frequencies when looking at 20 carrier periods compared to computing a FFT of the entire simulation of 5 s. This is a consequence of using a non-integer frequency modulation index, where harmonic cancellation can be achieved over multiple fundamental periods. As result, it is no longer sufficient to look at only one fundamental period to determine the harmonic behavior in the current. When using the non-integer frequency modulation index, the current harmonics get a new periodicity that is three times the switching period. As a result,

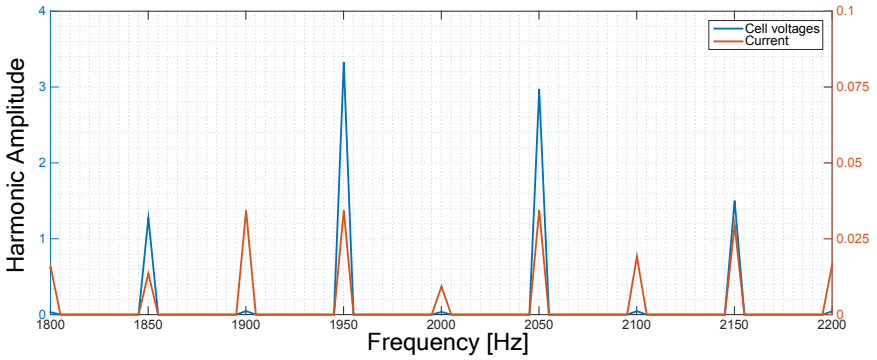
additional harmonics will appear corresponding to one third of the switching frequency. This can be seen in Figure 4.7(d). The new harmonic spectra, where a FFT analysis has been computed on multiple periods, does not have an interaction between current and voltage sideband harmonics at 2 and 4 f_c and thus removing the voltage deviation.

When the periodicity of the pulse pattern analyzed is increased, the harmonics are located at corresponding frequencies, i.e. at multiples of $1/N'th$ (N' being the number of fundamental periods of the new periodicity) of the fundamental frequency. An $m_f = 20.16$ corresponds to a periodicity of 3 times the fundamental in the cell voltage waveform, thus N' will be equal to 3, and harmonic components around multiples of 50/3 Hz appear.

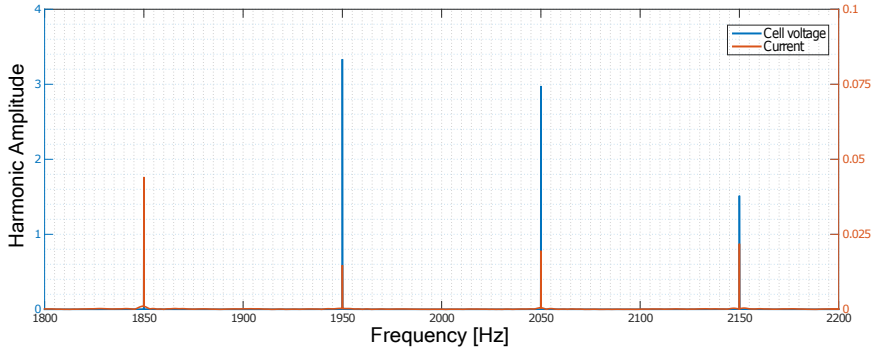
In Figure 4.8 the current and cell harmonics are shown for a $m_f = 20.083$ instead. As seen in Figure 4.8, similarly as with $m_f = 20.16$, harmonics appear at multiples of $1/N'th$ of the fundamental frequency, N' being 6 in this case, so new harmonics appear around multiples of 50/6 Hz.

The explanation behind the difference in frequency location of the harmonic component can be found by looking at the phases of these components. The harmonic components of the cell voltage share the same amplitudes for all periods of the fundamental, but the phases inherit a phase-shift from the corresponding carriers. As a result, despite there not being a complete cancellation in one fundamental period, harmonic cancellation, when summing the cell voltages together, can be achieved over a number of fundamental periods instead. This is the main advantage of the non-integer compared to the integer m_f.

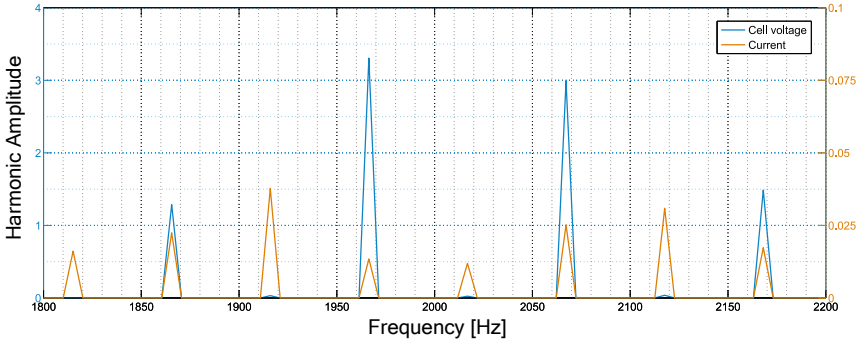
When there is a difference between capacitor sizes or in the series resistors of the capacitors, the non-integer frequency modulation index does not result in completely even voltage distribution and the simulations show a small improvement of the voltage deviation. This can be seen in Figure 4.9. The results are what should be expected since the individual cells are decoupled from each other, and if there is any asymmetry among the submodules the non-integer frequency modulation ratio cannot compensate for that. It can only compensate for differences in phase in the power produced by changing the phase of the carriers.



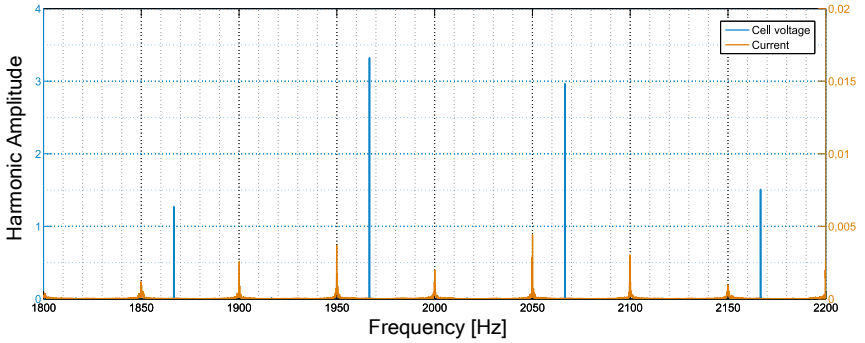
(a) Cell voltage and current harmonics with $m_f = 20$, 20 carrier periods



(b) Cell voltage and current harmonics with $m_f = 20$, 5 seconds

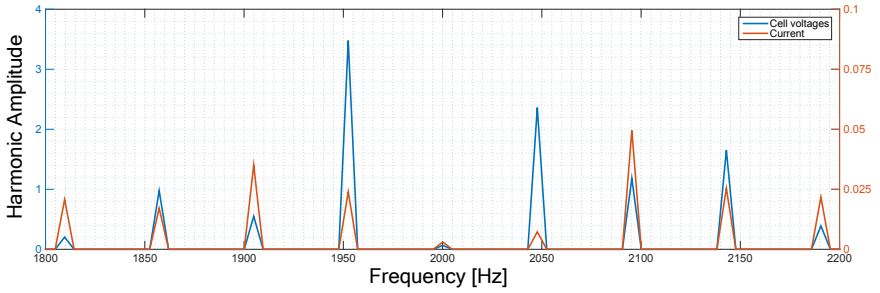


(c) Cell voltage and current harmonics with $m_f = 20.16$, , 20 carrier periods

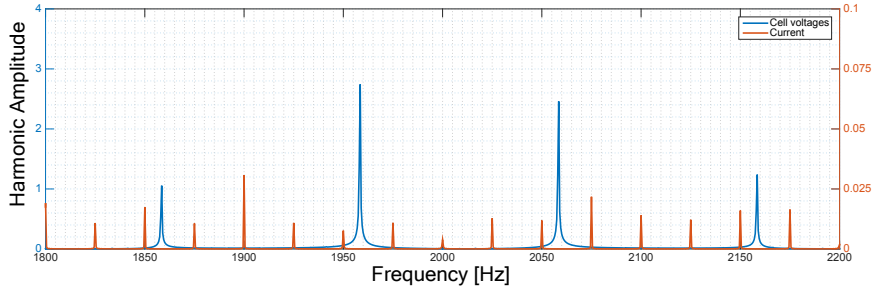


(d) Cell voltage and current harmonics with $m_f = 20.16$, 5 seconds

FIGURE 4.7: FFT of the cell voltages and current with $m_f = 20$, $m_f = 20.16$

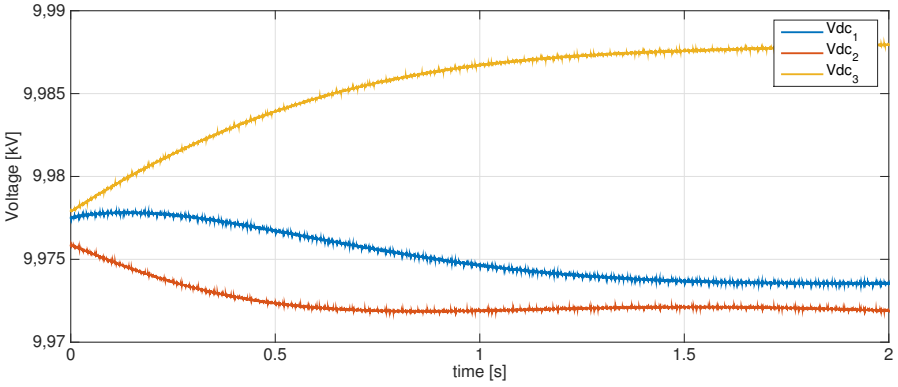


(a) Cell voltage and current harmonics with $m_f = 20.083$, 20 carrier periods

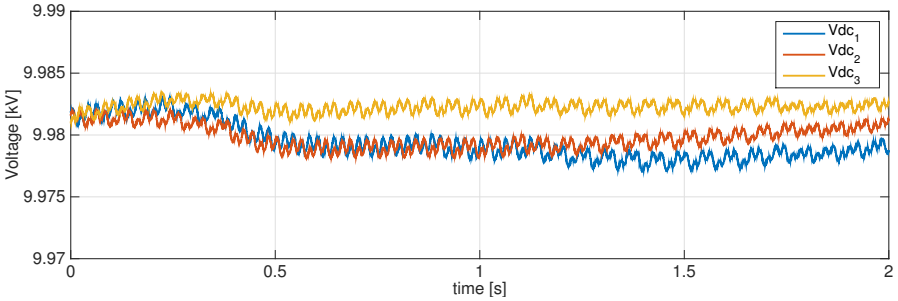


(b) Cell voltage and current harmonics with $m_f = 20.083$, 5 seconds

FIGURE 4.8: FFT of the cell voltages and current with $m_f = 20.083$



(a) Capacitor voltages with different capacitor values integer m_f



(b) Capacitor voltages with different capacitor values non-integer m_f

FIGURE 4.9: Capacitor voltages with $V_{dc1} = 3.2mF$, $V_{dc2} = 34mF$ and $V_{dc3} = 4.2mF$

Chapter 5

Conclusions and future work

This chapter aims to summarize the results and conclusions made from the investigations and some suggestions for future work in this fields are provided.

5.1 Conclusions

This thesis has investigated the impact of frequency modulation index on cell voltage balancing in a modular multilevel converter. The first two chapters offered a brief overview of different multilevel converter topologies and modulation techniques and a overview of the system investigated in this work. The system has been investigated both analytically and through PSCAD simulations at different carrier frequencies. The simulations have been carried out both for low and high switching frequencies. The results showed that the capacitor voltages deviated slower at high switching frequencies. It has been shown that selecting a non-integer frequency modulation index results in a natural balancing of the cell capacitors and prevents voltage deviation. The simulations showed that by introducing a non-integer index, the interaction between current and cell voltage harmonics was minimized. The results also showed that the non-integer index introduced other harmonic components located at other frequencies that are non-existing with the integer ratio. Increasing the cell numbers gave similar results as increasing the frequency. For the non-ideal case, when implementing unequal dc capacitors, the non-integer modulation index, although significantly improving the deviation process, did not prevent the voltages from deviating.

5.2 Future Work

The area of multilevel converter has evolved significantly in the past decade and there is many research being done around different control and modulation strategies. In this thesis, the main focus was on illustrating the difference between the integer and the non-integer frequency modulation index resulting from modulation with PS-PWM. This method is an extension from the PWM methods used for conventional 2-level converters. Multilevel converters have a different nature than the conventional converters and therefore, a modulation technique should be specifically designed that best suit the multilevel converters. In a future work, perhaps a different modulation technique should be studied. As mentioned in Chapter 2, a very popular choice currently is the sorting algorithm. There are also several papers that are investigating employing Model Predictive Control (MPC) algorithms for 3-leveled MMCs, however, a generic method for N number of cells is yet to be developed due to the high computational burden. A very interesting future project would be to compare the loss distribution and the overall performance of the converter with other modulation techniques.

For a future work focusing on PS-PWM, the phase-shift selection should be further investigated. Selecting the proposed phase-shifts, results in complete cancellation of current harmonics up to $6f_c$, since each contributing cell harmonic is phase-shifted by 120°. However, the harmonics around $6f_c$ are instead all in phase and result in an amplitude that is 3 times greater than each contributing harmonic. Perhaps a different phase-shift, that does not necessarily completely cancel out the harmonics below $6f_c$ but also doesn't add up to 3 times the amplitude around $6f_c$ is a better choice.

In the background, several different cells where mentioned, a comparison of the harmonic distortion for different cell-types could be interesting to investigate. Especially the performance of the MMC with the resonance/inductive cells.

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