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# Combined Tx/Rx Path

Master's thesis in Communication Engineering

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CHALMERS UNIVERSITY OF TECHNOLOGY

Gothenburg, Sweden 2024

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## Abstract

Over the last decade, advancement in the field of hardware development has resulted in designing efficient wireless communication systems. This has led to both the structuring of new systems and modification of existing ones. Among the various existing techniques, time division duplex (TDD) is a communication link where up-link and down-link are separated by using different time slots in same frequency band. It is an advantageous method when there is an asymmetry of up-link and down-link data rates and it is also the selected method for many commercial communication systems. TDD systems also gives a possibility to optimize the utilization of hardware, as same parts can be used for both up-link and down-link. This further reduces cost, size and possibly power consumption as well. Developing such transceivers (Tx/Rx) is the aim of this thesis project.

**Keywords:** Transceiver (Tx/Rx), Time Division Duplex (TDD), uplink, downlink.



# Acknowledgements

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Grish Kanna Malar Vijayakumar, Gothenburg, June - 2024



# List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

AC	Alternating Current
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog To Digital converter
ADS	Advances Designed System Software
AGC	Automatic Gain Control
AIR	Antenna-Integrated Radio
B2B	Board to Board
BPF	Band Pass Filter
CBW	Carrier Band Width
CP	Compression Point
DAC	Digital To Analog converter
DC	Direct Current
DFB	Distributed-feedback laser
DPD	Digital Pre-Distortion
DSA	Digital Step Attenuator
DUT	Device Under Test
EM	Electro Magnetic
EMI	Electro Magnetic Interference
EVM	Error Vector Magnitude
FDD	Frequency Division Duplex
FP	Fabry Perot laser
IF	Intermediate Frequency
IIP3	Input Third order Intercept Point
IP3	Third order Intercept Point
LNA	Low Noise Amplifier
LO	Local Oscillator
MAU	Media Access Unit
MB	Main Board
NF	Noise Figure
NR	New Radio
OIP3	Output Third order Intercept Point

---

PA	Power Amplifier
PAAM	Phased Array Antenna Module
PCB	Printed Circuit Board
RF	Radio Frequency
RX	Receiver
SBPS	Symbol Based Power Save
SMA	Sub Miniature version A
SNR	Signal to Noise Ratio
SP3T	Single Port Triple Through
SPDT	Single Port Double Through
TBD	To Be Determined
TDD	Time Division Duplex
TL	Transmission Line
TRX	Transmitter and Receiver
Tx/RX	Transceiver
VDD	Voltage Drain to Drain
VSCEL	vertical-cavity surface-emitting laser
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Network





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# 1

## Introduction

### 1.1 Purpose of the Project

Over the last decade, advancements in the field of hardware development has resulted in designing wireless communication systems with exceptional efficiency. This has paved way to both modification of existing systems and designing of new ones. The main purpose of this project is to build and evaluate a transceiver that operates at intermediate frequencies (around 5 GHz) utilizing Time Division Duplex (TDD) characteristics. These transceivers are constructed using the same set of hardware for both up-link (UL) and down-link (DL) communications, hence reducing the overall number of components on the main board. Among the many existing techniques, TDD is a communication link where UL and DL are separated by using different time slots in the same frequency band. Unlike Frequency Division Duplex (FDD), TDD has an advantage of not needing a suitable paired spectrum as both UL and DL uses the same channel for communication. Whereas having a paired spectrum has a drawback of wasting the spectrum when it is not used and moreover the guard bands that are used in FDD to avoid interference between UL and DL are wasted as they are not used for useful traffic. Here communication link to receiver is known as UL and communication link to transmitter is known as DL. It is an advantageous method, when there is an asymmetry of UL and DL data rates and also a widely chosen method for many commercial communication systems. In TDD as the channel propagation is same at both the directions, same parameters can be used to transmit and receive. This factor allows us to use channel reciprocity in TDD, whereas in FDD usage of different frequencies results in the channel having different characteristics on both directions. TDD systems also provide the possibility to optimize the utilization of hardware, thus using same parts helps to reduce cost, size and possibly power consumption. Developing such transceivers is the main motive of this thesis project.

The resultant transceiver design was developed based on link budget specifications and this modeled design was evaluated by analytical simulations. Advance Designed System software (ADS) was used to implement the basic design and evaluation work. Based on the design simulation results, a combined Transmitter/Receiver (Tx/Rx) path was developed. The thesis was concluded with a result presentation for both the Ericsson design team and the university, stating the performance outcomes of the project.

## 1.2 Objectives of the Project

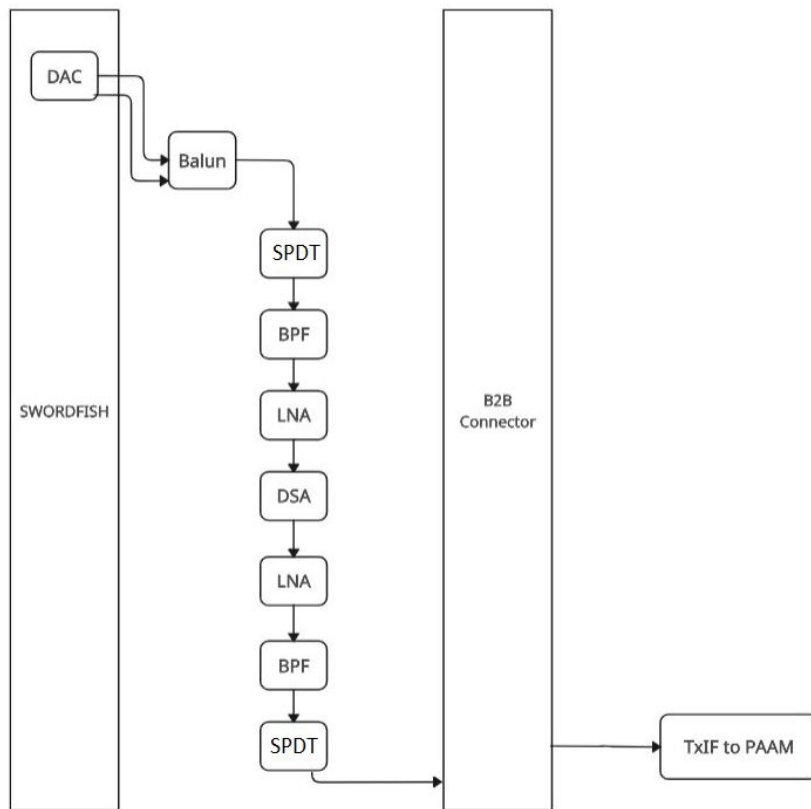
The following steps are envisioned as the objectives of the thesis work:

- Investigate the possibility to replace dedicated up-link and down-link hardware blocks with a common block used for both UL and DL communications.
- Systemize and design a transceiver based on block requirements and conclusions obtained from the investigation.
- Build and evaluate the transceiver performance in ADS.

## 1.3 Overview

Block diagram of the transmitter used in this project can be seen in Fig.1.1, where the signals from Digital to Analog Converters (DAC) are feed through a balun to the Single Port Double Through (SPDT) switch before it passes a palindrome series of components Band Pass Filter (BPF), Low Noise Amplifier (LNA), Digital Step Attenuator (DSA)) and enters the Board to Board (B2B) connector. This signal is later transmitted via Phased Array Antenna Module (PAAM) for communication. Figure 1.2 shows the block representation of the receiver used over the project, where the signals received from the PAAM is feed via a balun component. After the signal passes the palindrome series, it passes through an SPDT switch before it enters the balun and then the Analog to Digital Converter (ADC) were the received signal is converted.

As both the transmitter and receiver uses the same series of the palindrome components except few additional elements, they were both combined together to form a single Tx/Rx path (transceiver). Block representation of this transceiver can be seen in Fig.1.3, where we can observe that the SPDT switches have been replaced with Single Port Triple Through (SP3T) switches in order to support the new design. As a result of having a combined path, the number of components used before have been cut into half. Having such a combined path also paved way for reducing the size of the design and the overall cost as well. However, having such a combined path for Tx & Rx has its own challenge of compromising either the transceiver's linearity or noise. This was the reason why such a combined path was not designed from the beginning.



**Figure 1.1:** Block Representation of Transmitter Layout

# 1. Introduction

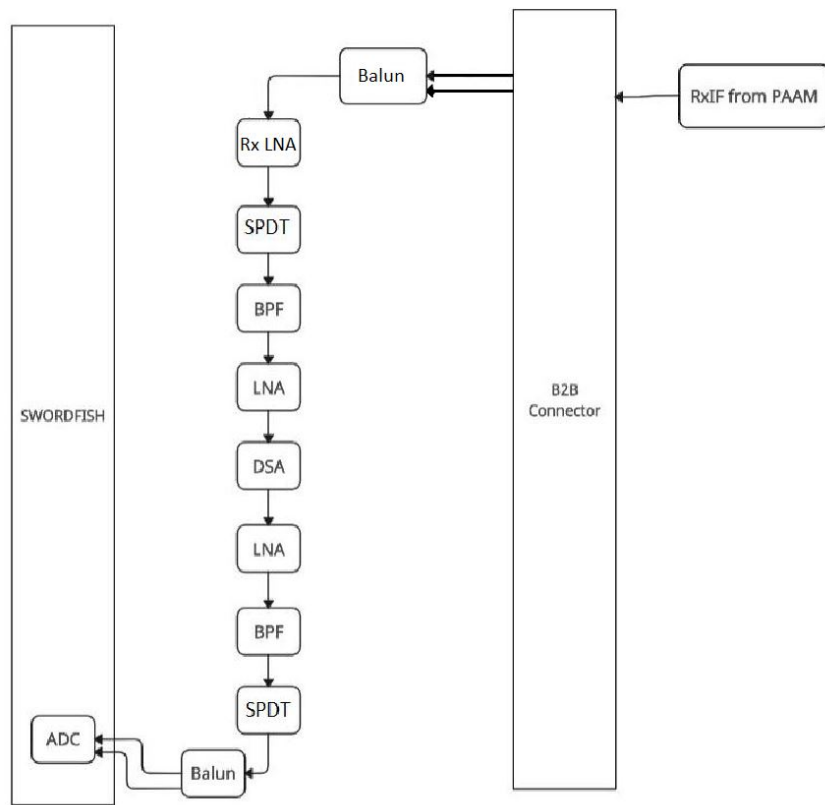


Figure 1.2: Block Representation of Receiver Layout

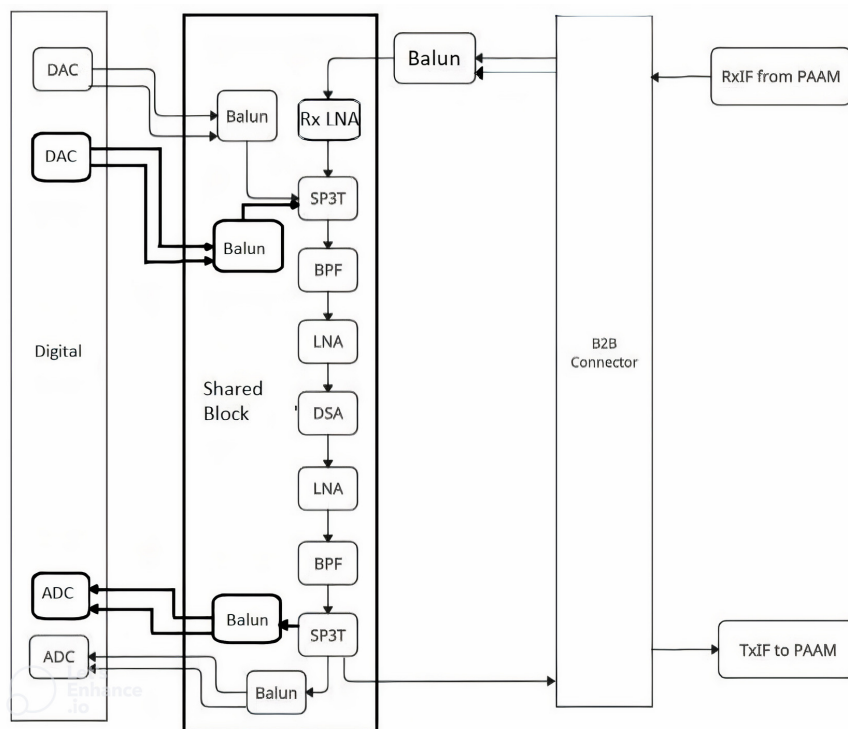


Figure 1.3: Block Representation of Transceiver Layout

# 2

## Theory

### 2.1 Radio Transceiver

A transceiver is a combined form of transmitter and receiver in a single package, thus, the operations of both transmitter and receiver can be single-handedly performed by a transceiver. This is used in wireless communication devices like cordless telephone sets, cellular telephones, radios, etc.

A transceiver can work in either half-duplex or full-duplex mode. In a half-duplex mode, it is not possible to receive and transmit signals at the same time. While in the full-duplex mode, transceivers can receive and transmit simultaneously without disrupting neither of the functions. FDD and TDD are the two different forms of full duplex. In FDD, the down-link and up-link frequencies are different for both Tx and Rx to process data. Whereas in TDD the down-link and up-link frequencies are the same, but they process data in different time slots. In our radio transceiver design, TDD is the duplex method used. As soon as the transmitter starts to transmit signals, the receiver will be silenced. This is achieved using an electronic switch, which lets the transmitter and receiver to be connected to the same antenna but in the mean time they can function individually. The transmitter and receiver operates on different time slots, so that the transmitter signal does not interfere with the receiver.

#### 2.1.1 Types Of Transceivers

Transceivers are classified into different types as the following examples:

- Radio Frequency (RF) Transceivers
- Fiber-optic Transceivers
- Ethernet Transceivers
- Wireless Transceivers

##### 2.1.1.1 RF Transceivers

These transceivers can be used in any wireless communication system by arranging them in between base-band modem as well as Power Amplifier (PA) or LNA. RF transceivers are used to transmit data in the form of audio or video over the wireless medium [1]. They are also used to convert intermediate frequencies (IF) to RF and for transmission & reception of TV signals in satellite communication, Zigbee and wireless local-area network (WLAN).

### 2.1.1.2 Fiber-optic Transceivers

This device uses fiber optic technology for data transmission. It is an essential element in optical network devices, which includes electronic components to encode or decode the information into light signals. After which these signals can be transmitted as electrical signals through another end. Here the data can be transmitted in the form of light which uses a light sources like vertical-cavity surface-emitting laser (VSCSEL), Distributed-feedback (DFB) laser and Fabry Perot (FP) laser.

### 2.1.1.3 Ethernet Transceivers

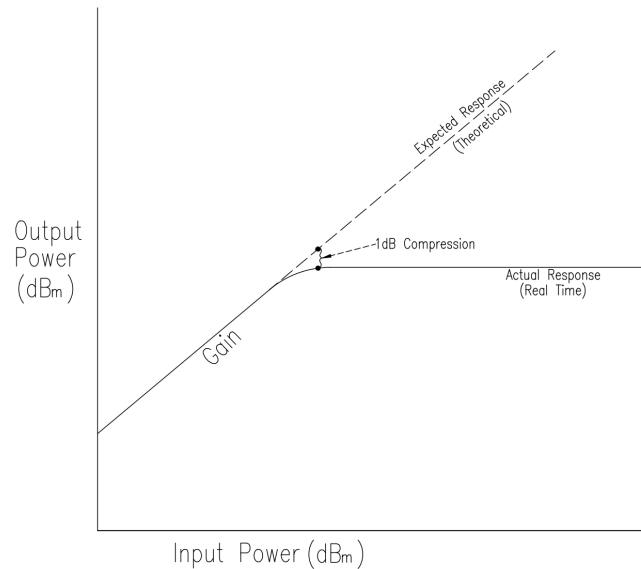
An ethernet transceiver is used to connect electronic devices or computers in a network to transmit & receive messages. An alternative name for them is media access unit (MAU), which is used in the specifications of IEEE 802.3 & Ethernet. Ethernet is the physical layer component in the ISO network model and it is mainly used for detecting a collision, conversion of digital data and Ethernet interface processing.

### 2.1.1.4 Wireless Transceivers

A wireless transceiver is a vital component in the wireless communication system and the quality of them can be determined by their efficiency as well as their data delivery rate. This includes two functional layers, known as physical layer & media access control layer. Where the physical layer includes an RF front end and a baseband processor, which changes a bitstream to a collection of symbol flow for data transmission. The MAC layer gives link traffic control used by the transmitter to contact the wireless links, evade collisions & enhance data throughput.

## 2.2 Performance Parameters

- Gain - Gain is the logarithmic expression for the ratio of output power to the input power, which also refers to the magnification of voltage (where  $P = V^2/R$ ) or current (where  $P = I^2R$ ). Passive components are known to have negative gain and dB is the unit in which gain is measured.
- Signal to Noise Ratio (SNR) - It is defined as the ratio of received signal power to noise power, expressed in dB scale (3.13). A high SNR is beneficial, as high SNR means that the signal is clear and easy to detect or interpret, whereas if it tends to be low, distinguishing noise from the desired signal becomes hard during communication.
- Compression Point (CP) - The point where the output power starts to saturate (without increasing along with gain) as the input power increases is known as compression point [2]. Figure 2.1 shows the 1 dB compression point, where the gain decreases by 1 dB from its constant value. It is until this point that we consider an amplifier to operate linearly. Once a device reaches its CP it undergoes compression and becomes a non-linear device, producing distortion, harmonics and inter-modulation products.
- Noise Figure ( $N_f$ ) & Noise Factor (F) - Noise figure is a term used to express the performance of an amplifier, receiver, mixer or other circuit blocks.  $N_f$  is



**Figure 2.1:** 1 dB Compression of Actual Response from Theoretical Response

expected to be low, in order for the system to have high performance and it is expressed in terms of dB. The noise factor of the system is determined by the ratio between input SNR and output SNR.

- Error Vector Magnitude (EVM) - EVM is used to measure how accurately a wireless system can transmit and receive symbols within its constellation, without the signal being degraded (filter distortion, I-Q imbalance, phase noise, etc) [3]. In an ideal case the transmitted and received symbols are present at their ideal positions (in their constellation diagram) but in real case scenario they tend to deviate due to imperfections. This is when they produce magnitude error along with vector error on the measured vector (deviated symbol). They are usually expressed in percentage but they can also be measured in dB scale, based on the following relation:

$$\text{EVM (dB)} = 20 \log_{10} \frac{\text{EVM}\%}{100}. \quad (2.1)$$

- Scattering parameters (S-parameters) - These set of parameters describes the input/output relationships among the ports of an electrical system. During higher frequency ranges it is vital to describe a network in terms of waves rather than voltage or current [4]. These parameters are used to determine both reflection co-efficients and transmission gains from the port ends of a network. S11 (input return loss), S12 (reverse transmission gain), S21 (forward transmission gain) & S22 (output return loss) are the matrix parameters for a 2 port network. These concepts are used in determining gains, losses and voltage standing wave ratio (VSWR).

- Adjacent Channel Leakage Ratio (ACLR) - ACLR is defined as the ratio of transmitted power on the assigned main channel to the power received in the adjacent radio channel (after a receive filter). The adjacent channels are located at different frequency offsets based on standards [5]. ACLR is also known as Adjacent Channel Power Ratio (ACPR).
- Third order intercept point (IP3) - IP3 is a hypothetical point where the power level of the third-order harmonics will reach the power level of the fundamental signal [6]. Once the device reaches its 1 dB compression, these two power levels become parallel to each other (device becomes saturated) and they never intersect. The input power level at this point is known as input IP3 (IIP3), and the output power is known as the Output IP3 (OIP3). IP3 is also co-related with linearity of the system.

### 2.3 Low Noise Amplifier

LNA is an important element of communication systems, which has the main role of amplifying weak signals by maintaining the noise low. Its performance can be measured using different factors like noise figure, gain, impedance matching, return loss and so on.

In general, normal amplifiers increase the power of both signal and noise present at their input, but they also tend to introduce additional noise to the system. Whereas LNAs are designed to minimize that additional noise, [7]. LNA provides voltage levels which are appropriate for analog to digital conversion and other analog processes. They are also used to increase the amplitude of weak RF signals.

### 2.4 Band-Pass Filter

BPF is a type of electronic circuit that is used to pass certain bands of frequency without them being attenuated. The particular band of frequency that passes by the BPF is known as pass-band. They are used over wireless communication in order to constrain the signal bandwidth, as it helps with accurate data transmission along with high speed. In the transmitter section, it limits the signal and prevents it from interfering with other systems [8]. Similarly in the receiver section, BPF only selects the desired pass-band and rejects others. They are characterized into narrow pass-band (high Q-factor) and wide pass-band (low Q-factor) by means of their Q-factor (reciprocal of fractional bandwidth).

An ideal BPF is assumed to possess a flat pass-band characteristic by completely passing only the desired frequency and omitting the remaining bands. However no such ideal filter exists in practical case, as complete rejection of frequency band outside the pass-band is not possible by the filter. This is known as roll-off characteristic of a filter and is expressed in terms of dB.

## 2.5 Switch

The need for RF switches have increased rapidly as the demand for wireless communication with high frequency and wide bandwidth increased. These switches are used to route high frequency signals to one or more signal paths for the purpose of data transmission. The parameter that defines the efficiency of a switch is its switching speed, as the name implies its the time taken for changing its state from on to off and off to on [9]. Insertion loss and isolation are the other parameters, were the former is the transmission loss when the switch is in its on state (considered crucial as it can add to system's noise level) and the later is the attenuation at the ports when the switch is at off state.

## 2.6 Digital Step Attenuator

An RF digital step attenuator is a device that is used to apply a controlled amount of attenuation to an RF signal and also where this applied attenuation is controlled digitally [10]. It is distinguished into three different types based on the implementation levels, such as:

- Integrated circuits, which are used for tight integration into high volume products. It requires detailed hardware and software integration.
- Digital attenuator modules, used for integration at system level and requires less engineering effort.
- Stand-alone digital step attenuator, typically including multiple independent channels and covering a wide range of applications.

Irrespective of its application or selected implementation, the digital attenuator is characterized by a set of parameters such as operating frequency range, minimum and maximum attenuation, attenuation step-size and accuracy. Different applications require different parameters as well as selection of control interface. These interfaces are divided into serial and parallel interface. LNAs have no constant gain, as they vary with respect to different parameters like frequencies, temperature and so on. Thus, a DSA helps to achieve a constant gain, desired by the user via attenuation.

## 2.7 Balun

Balun (balanced-unbalanced) is a device used to transform a balanced transmission line into an unbalanced one for long distance communications. This is due to the fact that differential signaling on the balanced lines are immune to cross-talk or noise. Baluns are used to sort out the flow of Alternating Current (AC) signals and make impedance transformation between coaxial cable and other interfaces [11]. They distribute and control common mode currents.

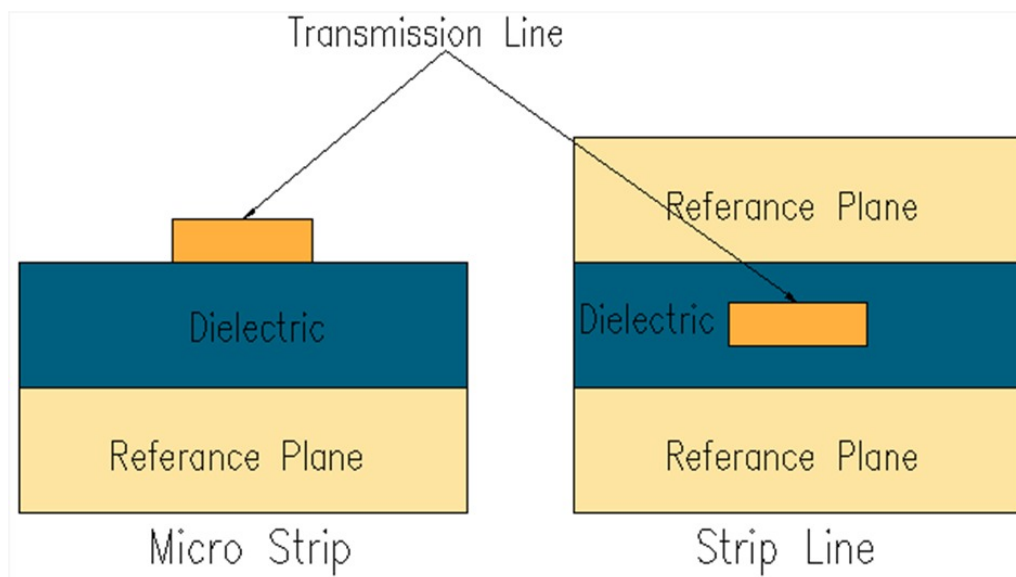
In RF circuits they are used as common mode chokes in order to avoid feed line radiation, which occurs when the coaxial cable at the feed point starts acting as antenna and radiates power. There are two main divisions of baluns, current balun (it forces equal current through the two sides of a balanced load) and voltage balun

(it forces equal voltage across the two sides of a balanced load). Voltage baluns are inefficient in preventing the coaxial cable shield. These baluns are mainly used over our transceiver in order to transform the 100 ohm input feed-lines into 50 ohm transmission lines.

## 2.8 Transmission Line

Transmission lines (TL) are the conductors that serve as a path for the transmitted electrical waves or RF energy to pass through them. They form a connection between transmitter or receiver with the antenna in order to permit signal transmission. They are divided into "Balanced" and "Unbalanced" transmission lines, where the balanced transmission lines are made of two parallel conductors spaced using insulator spacers. They have same amount of current flowing in them with reference to ground, but being  $180^\circ$  out of phase with each other. Whereas in unbalanced lines, the current carrying conductor is above ground and the return path of the conductor is grounded producing unequal impedance.

In Printed Circuit Boards (PCB) the transmission lines are built using two conductors: a trace for the signal and its return path (ground) in a reference plane, being separated by a dielectric plane [12]. To ensure it has same impedance throughout the line, the width of the trace and height between the two conductors are calculated. Transmission lines used in PCB are divided into two categories (Fig.2.2):



**Figure 2.2:** Micro-strip & Strip-line

- **Micro-strip** - A single uniform trace placed on the outer layer of the board and adjacent to a single conducting reference plane is known as micro-strip. The trace and reference planes are separated by PCB dielectric layer. It is used to provide return path for the signal.
- **Strip-line** - A uniform trace placed in the inner layer of the board, having reference planes on both the sides of the PCB dielectric layer is known as a

strip-line. Thus, it has two current return paths.

## 2.9 Matching Networks

Matching networks (impedance transformer) are used to enable proper impedance matching between source and load. Impedance matching must be performed to prevent standing waves and also to transfer efficient power. They only use reactive components (capacitors and inductors) that stores energy rather than resistive components that dissipate energy (resistors) [14]. This is done in order to ensure maximum power transfer from source to load without energy dissipation. Wide-band matching networks are hard to design, due to the fact that capacitors and inductors have impedance that is dependent on frequency. Thus, change in frequency over signals passing through matching networks degrades its efficiency.

## 2.10 $\pi$ Attenuator

$\pi$  attenuators are passive components that are used to reduce the source power without distorting the signal waveform. They are widely used in radio communication and microwave transmission lines in order to weaken stronger signals and provide impedance matching. These  $\pi$  type attenuators are unbalanced circuits, which does not have equal impedance over its two transmission lines. Throughout the transceiver design we use 0 dB  $\pi$  attenuators in between every component blocks in order to provide breakpoints over the transmission lines. Break points formed by these attenuators makes slicing of the strip-line much easier and accurate while calculating line-losses. These 0 dB attenuators are also used as placeholders in case the gain is needed to be adjusted.

## 2.11 Parasitic Capacitance

The result of virtual capacitance formed between two traces separated by a dielectric is known as a stray or parasitic capacitance. When current carrying traces run in close proximity, the potential difference between them ends up producing this unwanted signal or power integrity termed as parasitic capacitance [15]. These are prominent in high frequency PCBs, which affects the performance by leading to cross-talk, noise or signal coupling and Electromagnetic Interference (EMI) coupling. Impacts of these parasitic capacitance can be reduced in PCBs by avoiding parallel routing, increasing space between adjacent traces, impedance matching and so on. How this capacitance was calculated and its impacts were reduced on our design will be discussed in detail on chapter 5.

## 2.12 Unit Terms

- dB - Decibel (dB) is a logarithmic unit used to measure sound levels and a way of describing ratios (ratio of power, sound, voltage, etc).

## 2. Theory

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- dBm - Decibel milli-watts (dBm) refers the logarithmic unit that expresses power relative to 1 mW, it is used to define signal strength or intensity in RF engineering.
- dBc - Decibel relative to carrier (dBc) is the ratio of input signal power to the carrier signal power.
- dBi - Decibel relative to isotropic (dBi) describes the power an antenna transmits in a single direction compared to the isotropic radiator.

# 3

## SYSTEM MODEL

### 3.1 Link Budget Designing

Link budget designing was a vital part of this project, where the power gains and losses that a signal experiences in a communication system are accounted. In other terms it can be stated as an equation that gives output power of a signal after it has been exposed to attenuation due to propagation, antenna gains, feed-line losses, amplification and so on from the input power, as it propagates from Tx to Rx.

It is a design aid that is mainly used to calculate the output power while building a communication system, in order to make sure whether the passed information is received intelligibly with sufficient SNR. A simplified link budget equation (3.1) can be expressed as,

$$\text{Output power (dBm)} = \text{Input power (dBm)} + \text{gains (dB)} - \text{losses (dB)}. \quad (3.1)$$

Initial step for building a link budget starts by arranging various components or elements that have been chosen for the design in an orderly manner, similar to schematic block representation. Following this comes the measurement of various parameters (loss, gain, SNR, noise). Various combinations of components were also used, in order to find the optimal way to build the transceiver design.

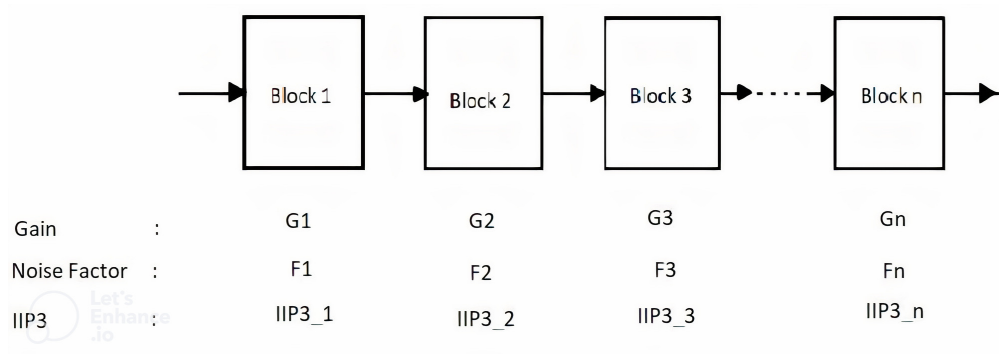
Link budget of this project was built on Excel, as it contains several features that makes the building process less time consuming. First the basic version of a receiver was designed after which it was examined and calculations were made. Following this the combined path of Tx/Rx was built using the same mechanism. Graphs were generated to compare the progress of noise, SNR, gain for various combinations of different components from this link budget. This gave a clear picture on the results we obtained after running multiple tests and what design requirements that were yet needed to be met.

#### 3.1.1 Formulas and Implementation

Several formulas were used on designing the link budget of the transceiver, in order to study various characteristics of the components used. Lets see them in a brief manner as follows:

- Gain ( $G$ ) & Linear Gain ( $A_l$ ) : The gain of various components were directly obtained from their respective data sheets, which were given in dB. For the purpose of calculation the values in dB were converted to linear scale using,

$$A_l = 10^{(\text{Gain}/10)} \quad (3.2)$$



**Figure 3.1:** Block-wise representation of parameters

and the total gain  $G_T$  for the system was calculated using the formula,

$$G_T = G_1 + G_2 + G_3 + \dots + G_n, \quad (3.3)$$

where,  $G_1, G_2, G_3, G_n$  are the gains of the blocks ranging from 1<sup>st</sup> block until  $n^{th}$  block, Fig.3.1.

- Noise Factor ( $F$ ): Noise factor is expressed as the ratio of SNR at the input to the SNR at the output. From this, cascaded noise factor of several blocks of components was calculated using Friis equation [16] as,

$$F_t = F_1 + \frac{F_2 - 1}{A_{l1}} + \frac{F_3 - 1}{A_{l1}A_{l2}} + \dots + \frac{F_n - 1}{A_{l1}A_{l2}A_{l3}\dots A_{l(n-1)}}, \quad (3.4)$$

where,  $F_t$  is the cascaded noise factor,  $F_1, F_2, F_3, F_n$  are the noise factor of the 1<sup>st</sup>, 2<sup>nd</sup>, 3<sup>rd</sup> and  $n^{th}$  stages respectively.  $A_{l1}, A_{l2}, A_{l3}, A_{ln}$  are the linear gains of the corresponding stages, Fig.3.1. High gain at the previous stage reduces the noise factor of the present stage and noise factor of the 1<sup>st</sup> block dominates the total noise figure.

- Noise Figure ( $N_f$ ): These values were directly obtained from the data sheets. The dB to linear conversion of them were done as same as that of gain with respect to eq.3.3. The noise figure is defined as the dB of noise factor,

$$N_f = 10\log(F), \quad (3.5)$$

here,  $F$  is the noise factor and  $F_t$  will be used in the place of  $F$  to calculate cascaded  $N_f$ .

- Thermal Noise (N): The thermal noise was obtained by using the formula

$$N = -174 + (10 * \log(B)), \quad (3.6)$$

where,  $B$  is the channel bandwidth and -174 is the amount of power in a 1 Hz bandwidth that a thermal noise source has at the room temperature in terms of dBm/Hz. The thermal noise in terms of power level is expressed as  $N = kTB$ , where  $K$  is Boltzmann's constant ( $1.3803 * 10^{-23} J/K$ ),  $T$  is the temperature in degrees Kelvin (e.g., 295 K) and  $B$  is the emission bandwidth of the device in Hertz.

- IIP3 & OIP3 : The values of IIP3 were only stated for switches on the data sheets, were-else the values for other components were obtained using the following relation,

$$IIP3 = OIP3 - G. \tag{3.7}$$

IIP3 is expressed in terms of dBm, where  $G$  is the gain in dB. The OIP3 values were also pre-defined on the components data sheets.  $OIP3_T$  or the total OIP3 value can be derived by the relation between  $IIP3_T$  and  $G_T$  as, (3.7)

$$OIP3_T = IIP3_T + G_T, \tag{3.8}$$

where,  $G_T$  is the total gain in dB and the  $IIP3_T$  is the total IIP3 of the system which is expressed using the following equation,

$$IIP3_T = \left( \frac{1}{IIP3_1} + \frac{A_{l1}}{IIP3_2} + \frac{A_{l1}A_{l2}}{IIP3_3} + \dots \right)^{-1}, \tag{3.9}$$

where,  $IIP3_1, IIP3_2, IIP3_3, ..$  are the input IP3 of the 1<sup>st</sup>, 2<sup>nd</sup>, 3<sup>rd</sup> stages respectively as shown in Fig.3.1.

Though the formulas used are same for both Tx and Rx in calculating the link budget, the number of component blocks differ. Desired Tx and Rx path results were generated by adding or neglecting certain component blocks during calculation as per requirements. This can be seen in Fig.3.2, where a separate option called "Transmission" is used to select between the two paths, each having their own component blocks.

DSA atten	10,00		BW	1E+08		Transmission	Tx
			Total Gain	9,55			Rx
			Total NF	10,68			
Freq	Case 3	3	Noise_thermal	-94,00			
Temp	25,00		OIP3(T)	2,43			
			IIP3(T)	-7,12			

Figure 3.2: Specifications & Path selection

### 3. SYSTEM MODEL

Overall view of the designed link budget for the transceiver can be seen in Fig.3.3. The components also have a selection list on the link budget which helps in understanding the impact of various combinations of components on the design's performance, which can be seen in Fig.3.4. The dB to linear and linear to dB conversions along with cascaded  $N_f$  and OIP3 can also be seen in individual rows of the link budget.

		1	1	3,00	2
	TL	Rx_LNA	Balun1	SW3	BPF2
Model			100AHF	SKY465LF	LFBD114
GAIN	-4,50	0	-0,7	-1	-1,5
Gain_lin	0,35	1,0	0,85	0,79	0,71
NF	4,50	0,0	0,7	1	1,5
NF(dB-L)	2,82	1,0	1,17	1,26	1,41
NF_cas	2,82	2,8	3,31	4,17	5,89
NF_cas(L-dB)	4,50	4,5	5,20	6,20	7,70
OIP3	1000,00	0,0	0	6,2	1000
OIP3_cas(Rx)	1000,00	4,5	-1,3187948	-1,93	-1,93
OIP3_cas(Tx)	1000,00		4,50	2,525981494	2,525981494
CP1		0			0

6		6	1	3,00	1,00	
LNA6	DSA	LNA6	BPF1	SW3	Balun1	TL
HMC8413		HMC8413	LFBA183	SKY465LF	100AHF	
19,5	-15	19,5	-1,5	-1	-0,7	-4,5
89,13	0,03	89,13	0,71	0,79	0,85	0,35
1,9	15	1,9	1,5	1	0,7	4,5
1,55	31,62	1,55	1,41	1,26	1,17	2,82
9,12	11,14	12,29	12,30	12,31	12,32	12,40
9,60	10,47	10,90	10,90	10,90	10,90	10,94
33	1000	33	1000	53	1000	1000
-1,93	-1,93	-1,93	-1,93	-1,93	-1,93	-1,93
2,52	2,52	2,52	2,52	2,52		2,52
21,5		21,5	0			

Figure 3.3: Designed Link Budget

		1	1	1,00	2
	TL	Rx_LNA	Balun1	SW1	BPF2
Model				SW1	
GAIN	-4,50	0	-0,7	SW2	-1,5
Gain_lin	0,35	1,0	0,85	SW3	0,71
NF	4,50	0,0	0,7	SW4	1,5
NF(dB-L)	2,82	1,0	1,17	SW5	1,41
NF_cas	2,82	2,8	3,31	SW6	5,86
NF_cas(L-dB)	4,50	4,5	5,20	SW7	7,68
OIP3	1000,00	0,0	0	6,18	1000
OIP3_cas(Rx)	1000,00	4,5	-1,3187948	-1,93	-1,93
OIP3_cas(Tx)	1000,00		4,50	2,518665679	2,518665679
CP1		0			0

Figure 3.4: Link Budget with selection option

### 3.1.2 Thermal Noise Propagation

Thermal noise propagation was one of the important parameters that was analyzed along with the link budget calculation. Calculating the thermal noise and knowing the value can help in improving the system performance and also in adopting the best approaches to do so. This propagation was studied with respect to both the noise as well as the components that were used on the design, where the thermal noise moves through the blocks by being multiplied with the gain of that specific component block. This total thermal noise is given as,

$$\text{Total Thermal noise} = (((N * A_{l1}) * A_{l2}) * A_{l3}) * \dots * A_{ln}), \quad (3.10)$$

where,  $A_{l1}, A_{l2}, \dots$  are the linear gains of various blocks through the path it propagates, Fig.3.1. The individual response of thermal noise on the components such as transmission lines, LNAs, Balun, etc can be expressed as,

$$\text{Propagated Noise} = (((N * (NF_1 - 1) * A_{l1}) * A_{l2}) * \dots * A_{ln}), \quad (3.11)$$

Here,  $NF_1$  just specifies the noise figure of the first block (Fig.3.1) and this changes with respect to what component we study the response of thermal noise.

The total and individual noise propagation studied on the different component blocks can be seen in Fig.3.5. The rows showcases the noise propagation throughout the specified blocks, whereas the columns shows the summation of noise values of various blocks in the particular column. All these values are in milli-Watt (mW) which are converted into dBm. The signal power throughout the propagation is also calculated in a separate row named as "Pin", using the formula,

$$P_{out} = (((Pin + G_1) + G_2) + \dots + G_n), \quad (3.12)$$

Here, the value of Pin can be changed between -40 to -5. These signal values along with previously obtained total noise values are combined to obtain SNR by the relation,

$$\text{SNR} = \frac{\text{Signal power}}{\text{Noise power}}. \quad (3.13)$$

As the signal and noise values we use as input are in dB, subtracting them provides the SNR of the link budget. This is based on the fact that division of normal numbers is equivalent to subtracting logarithmic values. Figure 3.6, shows the SNR calculation for the designed link budget.

### 3. SYSTEM MODEL

	TL	Rx_LNA	Balun1	SW4	BPF2	LNA6
Thermal noise	4,0E-10	1,4E-10	1,4E-10	1,2E-10	9,5E-11	6,8E-11
TL_N		2,6E-10	2,6E-10	2,2E-10	1,7E-10	1,2E-10
Noise_amp1 (mW)			0,00E+00	0,00E+00	0,00E+00	0,00E+00
Balun (mW)				5,93E-11	4,71E-11	3,33E-11
SW (mW)					8,19E-11	5,80E-11
BPF (mW)						1,16E-10
Noise_amp2 (mW)						
DSA (mW)						
Noise_amp3 (mW)						
BPF (mW)						
SW (mW)						
Balun (mW)						
TL_N						
Noise total (mW)	4,0E-10	4,0E-10	4,0E-10	4,0E-10	4,0E-10	4,0E-10

NA6	DSA	LNA6	BPF1	SW3	Balun1	TL
6,0E-09	1,9E-10	1,7E-08	1,2E-08	9,5E-09	8,1E-09	2,9E-09
1,1E-08	3,5E-10	3,1E-08	2,2E-08	1,7E-08	1,5E-08	5,2E-09
0,00E+00	0,00E+00	0,0E+00	0,0E+00	0,0E+00	0,0E+00	0,0E+00
2,97E-09	9,39E-11	8,4E-09	5,9E-09	4,7E-09	4,0E-09	1,4E-09
5,17E-09	1,63E-10	1,5E-08	1,0E-08	8,2E-09	7,0E-09	2,5E-09
1,04E-08	3,28E-10	2,9E-08	2,1E-08	1,6E-08	1,4E-08	5,0E-09
1,9E-08	6,2E-10	5,5E-08	3,9E-08	3,1E-08	2,6E-08	9,3E-09
	3,9E-10	3,4E-08	2,4E-08	1,9E-08	1,6E-08	5,8E-09
		1,9E-08	1,4E-08	1,1E-08	9,3E-09	3,3E-09
			1,2E-10	9,2E-11	7,9E-11	2,8E-11
				8,2E-11	7,0E-11	2,5E-11
					5,9E-11	2,1E-11
						2,6E-10
5,5E-08	2,1E-09	2,1E-07	1,5E-07	1,2E-07	1,0E-07	3,6E-08

Figure 3.5: Thermal Noise Propagation

	TL	Rx_LNA	Balun1	SW4	BPF2	LNA6
Noise total (mW)	4,0E-10	4,0E-10	4,0E-10	4,0E-10	4,0E-10	4,0E-10
Noise total_dbm	-94	-9,4E+01	-9,4E+01	-94	-94	-94
Pin	-10,00	-10,00	-14,50	-14,50	-15,20	-16,20
SNR	84,00	79,50	79,50	78,80	77,80	76,30

LNA6	DSA	LNA6	BPF1	SW3	Balun1	TL
5,5E-08	2,1E-09	2,1E-07	1,5E-07	1,2E-07	1,0E-07	3,6E-08
-72,6	-86,7	-66,8	-68,3	-69,3	-70,0	-74,5
1,80	-13,20	6,30	4,80	3,80	3,10	-1,40
74,40	73,53	73,10	73,10	73,10	73,10	73,06

Figure 3.6: SNR Calculation

## 3.2 Block Requirements for Systematizing Transceiver

There are certain specific requirements for both transmitter and receiver that uses one common path for operating. The DL path selects the DAC, whereas the UL path selects the ADC with respect to operating transmitter or receiver in the same block.

### 3.2.1 General Requirements

The general requirements for both Tx and Rx includes frequency range, interface impedance, timing requirements, power supply and operating temperatures.

#### 3.2.1.1 IF Frequency Range:

- IF operating frequency range is  $5000 \pm 400$  MHz.
- IF linearization range is  $5000 \pm 800$  MHz, which is required by the digital pre-distortion (DPD).

#### 3.2.1.2 Interface Impedance:

- Transmitter: The input interface towards the DAC is  $100 \Omega$  balanced ac coupled with return loss better than 12 dB for the whole IF frequency range. The output interface towards the RF-block is  $50 \Omega$ , with return loss better than 12 dB for the whole IF frequency range and it is better than 8 dB for the linearization pass-band.
- Receiver: The input and output interface towards the RF-block is  $100 \Omega$  balanced ac coupled with return loss better than 12 dB for the whole IF frequency range.

#### 3.2.1.3 Operating Temperature:

- Minimum start up temperature for the components to operate is  $-40^{\circ}\text{C}$ , whereas the maximum range (including heating from the component itself) is  $+94^{\circ}\text{C}$ .

#### 3.2.1.4 Power Supply & Control Logic:

- Supply voltage available for the block is 5.5 volts and the Control logic for switches, etc is 1.8 V. Functionality for power down/power up of components shall be active high.

#### 3.2.1.5 Timing Requirements:

- At TDD the UL to DL transition shall be done in less than  $7 \mu\text{s}$ .
- At TDD the DL to UL transition shall be done in less than  $10 \mu\text{s}$ .

### 3.2.2 Receiver Requirements:

- Gain: The overall gain ranges from -10.6 dB to 27.2 dB, where the typical target gain (the expected gain at room temperature, mid frequency and in the center of the control range) is 10 dB. Transmission line and connector losses at input shall be 4.3 dB. Transmission line losses at output shall be taken as 4.9 dB.

The receiver gain shall be configurable with resolution better than 0.25 dB. The configurable gain will be used to compensate for the gain variations on the RF-block. The gain flatness within IF pass-band ( $5000 \pm 402$  MHz) shall be within  $\pm 1$  dB.

- Noise Figure: Noise figure at maximum gain shall be less than 5 dB in all conditions (all temperature and frequency ranges).
- EVM: Main board EVM shall be better than 1 % for a new radio modulated signal and the Carrier Band Width (CBW) will be 100 MHz.
- Linearity:
  - CP: The input CP 1 dB should be better than -20 dBm for a carrier width signal at maximum gain.
  - IP3: The input IP3 shall be better than -15 dBm at maximum gain.
  - Harmonic Distortion (HD3 & HD2) : The third harmonic shall be better than -60 dBc for the frequency ranging from 1533 to 1800 MHz at maximum gain. The second harmonic shall be better than -60 dBc for the frequency ranging from 2300 to 2700 MHz at maximum gain.
- Isolation: The isolation between Rx ports shall be better than 60 dB.

#### 3.2.3 Transmitter Requirements:

- Gain: The overall gain ranges from -10.6 dB to 27.2 dB, where the typical target gain (the expected gain at room temperature, mid frequency and in the center of the control range) is 10 dB. Transmission line and connector losses at input shall be 4.3 dB. Transmission line losses at output shall be taken as 4.9 dB.

The transmitter gain shall be configurable with resolution better than 0.25 dB. The configurable gain will be used to compensate for gain variations on the RF-block. Hardware gain ripple shall be better than 1.5 dB (peak-peak) anywhere within the IF pass-band. Within linearization bandwidth, the hardware gain shall have a symmetrical ripple better than 2 dB and tilt less than 1 dB.
- Isolation: The isolation between Tx ports shall be better than 55 dB.
- EVM: Main board EVM shall be better than 1.2 % with DPD off.

# 4

## DESIGN

### 4.1 Rules & Regulations in Selection

While selecting hardware components for a design, there are a number of criteria that needs to be satisfied. In particular when such procedures take place under an industrial organisation, there comes a huge importance to integrity, availability and confidentiality. Hardware for designs are only resourced from entities that are approved by the organisation. These entities are verified and also have signed a contract under a vendor confidentiality agreement for being entrusted with the dealership. Vendors are selected for a product supply mainly based on aspects such as:

- Cost
- Technology
- Geo Flexibility
- Quality
- Sustainability

An Organisation takes care of the expenditures of various projects it handles within the budget it has been allocated. This begins from the basic design kick start to the end product circulation on the consumer market. Component selection also comes under this process, where the components that are being selected have to be cost-efficient apart from being suitable to the design requirements. For example, when a design requires 100s of amplifiers, each LNA can not be expensive individually. This will affect a lot during the time of mass production, which may result in exceeding the allocated expenditure.

Choosing hardware that are less expensive does not mean that they can lack on technical features. In order to achieve this, detailed search for a suitable hardware should be done. Quality of these hardware comes into picture while defining the lifetime of a manufactured product. An highly advanced product with a reasonable price having a poor lifetime or of bad quality from a renowned company may degrade the company's integrity among the consumers.

Having suppliers all around the world with valid raw materials is a high privilege when competing towards achieving deadlines. This helps at the time of an emergency crisis such as lack of product stock or other ethical reasons to find alternative resources. This Geo flexibility helps on running a smooth production without causing delay.

Sustainability comes into focal point when there is a need to develop products for the future with the resources available in hand but at the same time without deploying

them. The products that are being built for future purposes are highly aimed to be sustainable as it reduces the negative impact on the environment, economy and society. These sustainably developed products have merits such as less power consumption, easy waste disposal, non-toxic production.

## 4.2 Component Selection

Once the link budget is being designed based on specified requirements, there is another process that takes place simultaneously known as component selection. This component selection is given a significant amount of priority as the whole design's functionality depends on it. Lets see about the selected hardware parts for the designed transceiver briefly.

- **Balun:** From the suppliers X and Y, baluns for the design were selected. Supplier Y's Balun had an insertion loss of 0.7 dB, whereas supplier X's balun had a loss of 1 dB, which is comparatively higher. Component size for both of them were of same dimensions, thus balun from supplier Y was selected based on its low insertion loss.
- **LNA:** LNA is considered to be the key component of our link budget. The LNA candidates for component selection were mainly chosen by focusing on their gain, NF, component size, 1 dB CP, and OIP3 values (Table 4.1). Supplier C being one of the short listed candidate was dropped out, as its power consumption was higher than expected and also its operating frequency range was only until 5 GHz, whereas we needed the pass-band to be of additional 400 MHz. The S-parameters were measured in lab with network analyzer for the LNAs from suppliers A and B. The measured values were found to be identical in accordance with the values of their data sheets, even when there was minor difference due to transmission line loss. Though both supplier A and B's LNAs had similar gain, based on flat gain characteristics and absence of matching components, supplier B was chosen. However an LNA from supplier A is used as an additional LNA in Rx. The performance comparison for these LNA combinations can be seen in Table 4.2.

Supplier	Freq.range	Gain	NF	OIP3	CP 1
A	0.6G – 6G	21.5	0.7	34	19
B	0.1G – 9G	19.5	1.9	33	21.5
C	1.8G – 5G	30.3	1.6	35.73	26.6

**Table 4.1:** Features of LNA candidates

- **BPF:** With respect to both frequency and design specifications, two BPF were chosen from the supplier M. This BPF had an insertion loss of 1.5 dB (max) and was of smaller dimension.
- **Switch:** In our design, we are using SP3T switch instead of SPDT, which was used in the previous model of AIR. These switches are used to control the path switch over for Tx and Rx. As per our link budget, we have two SP3T

Amp 1	Amp 2	Tx Gain (dB)	Rx Gain (dB)
A	A	17.75	22.75
B	B	13.75	18.75
C	C	31.95	36.95
A	C	24.85	29.85
A	B	15.75	20.75
C	B	22.85	27.85

**Table 4.2:** Performance Comparison of LNA Combinations

switches in the designed model, for which the candidates were selected from Ericsson approved suppliers. During the investigation on component selection we found out that SP4T switches had good insertion loss and higher switching speed compared to SP3T switches, but they were expensive. Thus an SP3T switch with switching speed of 150 ns and gain of 1 dB was selected matching our requirements.

- DSA: DSA is considered to be the total gain controlling component for the design, used mainly to attenuate the system's gain as per our requirement. We are using the same DSA from the previous model of AIR. It works in a wide frequency range (9 KHz - 6GHz) and has flexible step attenuation varying from 0.25 dB, 0.5 dB, 1 dB up-to 31.75 dB.

### 4.3 ADS Verification

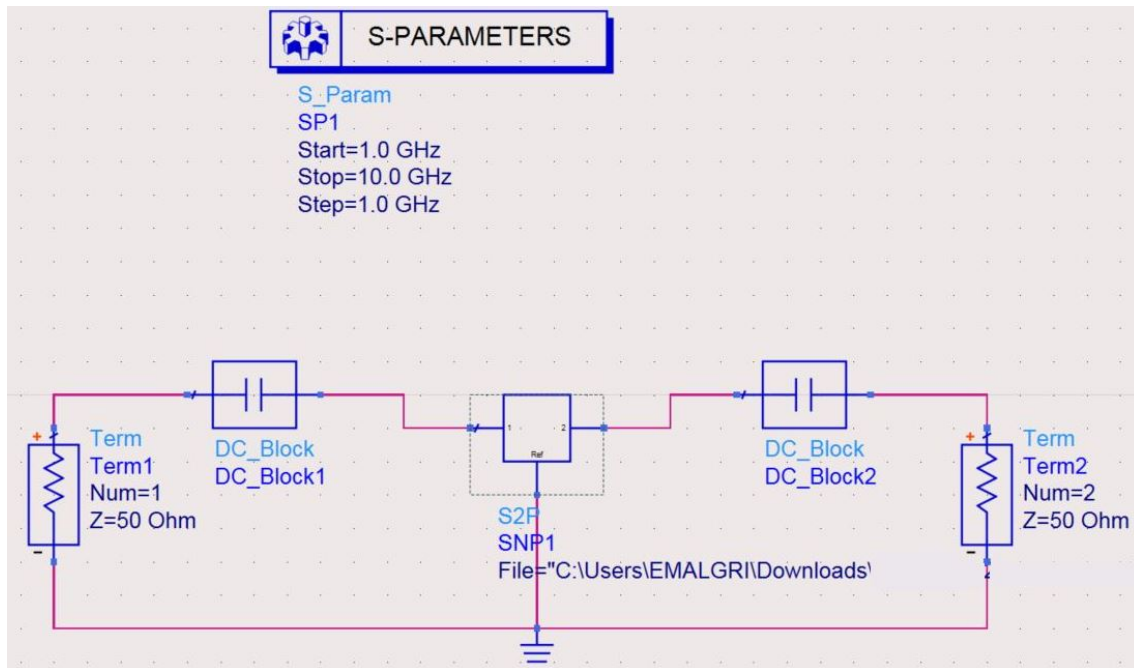
After completing component selection and link budget designing, there comes ADS simulation or verification. Every single component from the design was simulated using ADS within the frequency range of 1-10 GHz and its step size being 1 MHz, along with its S-parameters. In ADS simulation, we have used S2P file to save data from 2 port networks like LNA, BPF and DSA blocks. As we are using SP3T switch in our design which has 1 RF-in port and 3 RF-out port, we have used S4P file type. Same is for the balun, but it tends to have 2 imbalanced port and single balanced port. Thus, we used S3P file type for design verification in simulation of ADS.

#### 4.3.1 LNA

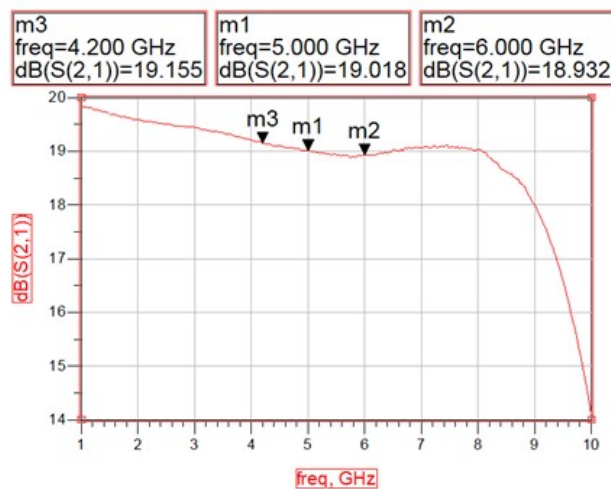
Evaluation kit for LNA was received from supplier B and supplier A's LNA was already available at the Lab. Thus, the lab testing of S-parameters for both the LNAs were done successfully using network analyzer. Both LNAs were given a 5 V supply and their power conception were noted to be same. Two DC block capacitors were used at both ends of the S2P for blocking the DC current and allowing RF signals to pass. Figure 4.1 shows the S2P block schematic for the LNA.

Figure 4.2 & 4.3 shows the difference in gain with respect to frequency change. Both graphs were observed to be identical and gain of the LNA from supplier B at lab test was narrowly lower (0.162 dB) than the data-sheet value. The gain was measured

## 4. DESIGN



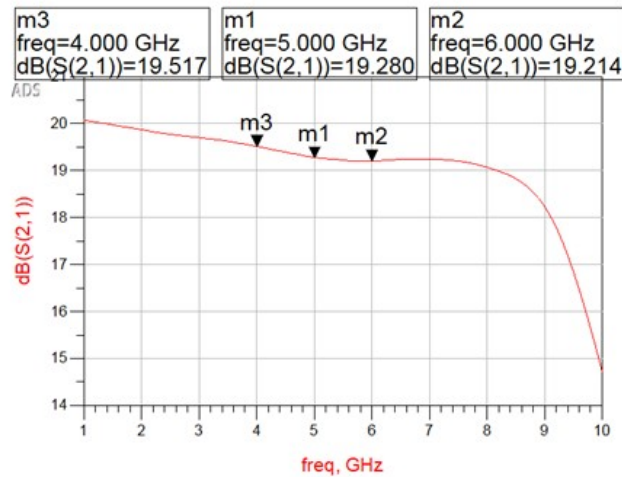
**Figure 4.1:** LNA (S2P) Schematic Block



**Figure 4.2:** Gain vs Frequency for supplier B's from Lab Test

including transmission line losses. Table 4.3 shows the difference in gain at three different frequency points.

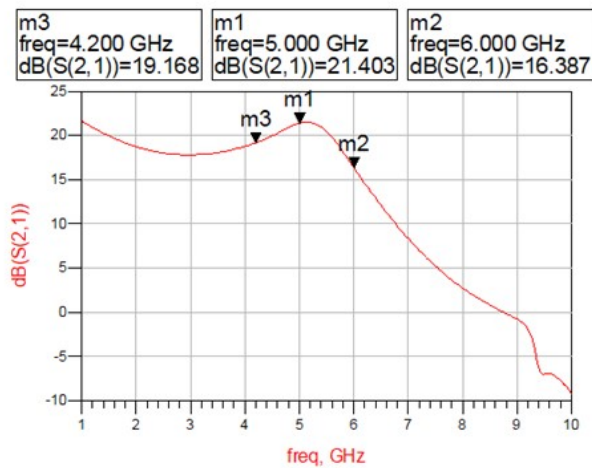
Figure 4.4 & 4.5 shows the difference in gain with respect to frequency change for supplier A's LNA. Both graphs obtained were nearly identical and gain of the supplier A's LNA at lab test was narrowly lower at 4 GHz and 6 GHz, but 1 dB higher at 5 GHz. Table 4.4 shows the difference in gain at three different frequency points.



**Figure 4.3:** Gain vs Frequency for Supplier B's from Data-sheet

Frequency	4GHz (dB)	5GHz (dB)	6GHz (dB)
S-parameter in Lab	19.155	19.018	19.124
S-parameter from Supplier	19.517	19.280	19.214
Difference	0.362	0.262	0.90

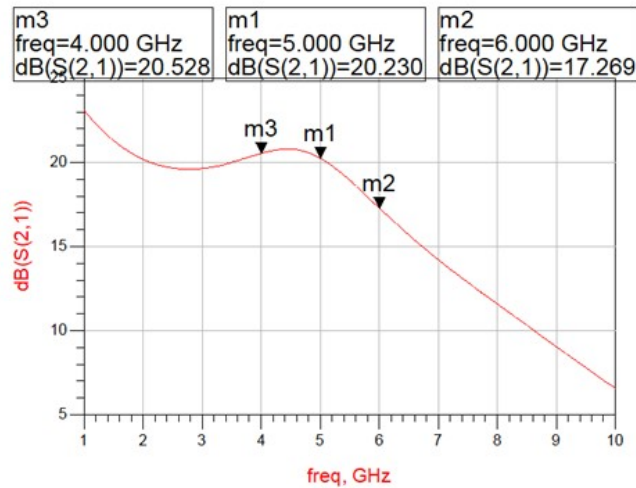
**Table 4.3:** Difference in Gain over 3 Frequency Points



**Figure 4.4:** Gain vs Frequency for Supplier A's from Lab Test

#### 4.3.1.1 DC blocking & RF choke

DC blocking is done in order to stop the flow of DC current into the system and for only allowing RF signals to pass through. These DC blocks works as a high-pass filter, as they allow the required RF frequencies to pass. These blocks are designed

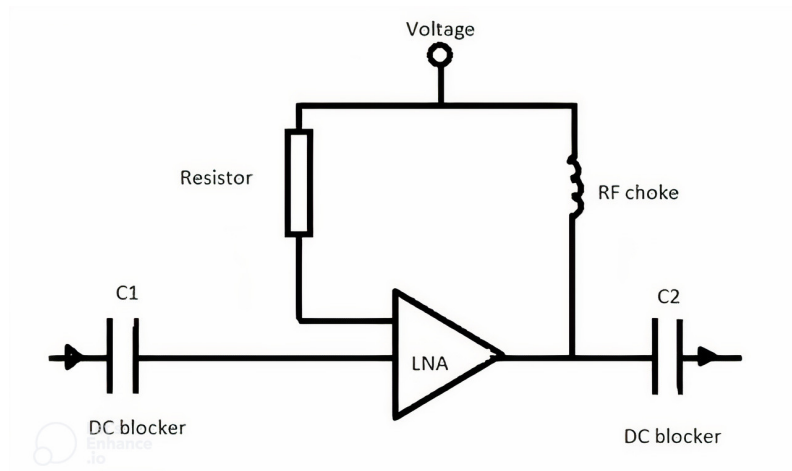


**Figure 4.5:** Gain vs Frequency for Supplier A's from Data-sheet

Frequency	4GHz (dB)	5GHz (dB)	6GHz (dB)
S-parameter in Lab	19.168	21.403	16.387
S-parameter from Supplier	20.528	20.230	17.269
Difference	1.36	1.173	0.882

**Table 4.4:** Difference in Gain over 3 Frequency Points

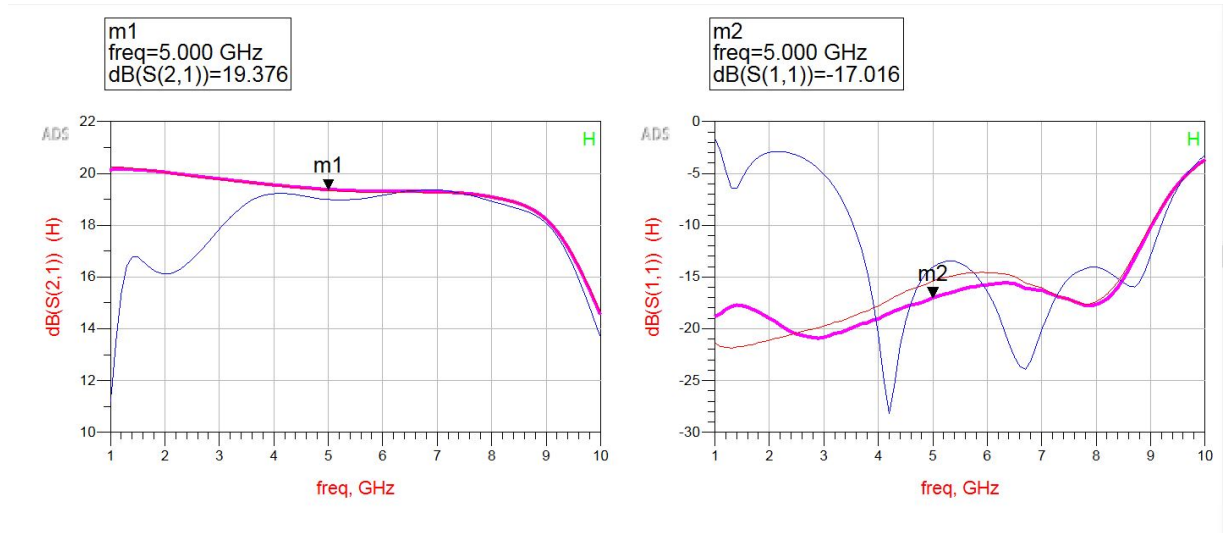
by placing capacitors in series to the transmission line, which can be seen in Fig. 4.6.



**Figure 4.6:** DC Block & RF Choke Schematic Diagram

Figure 4.7 (a) shows the DC blocking comparison for supplier B's amplifier (with respect to C1), where the pink line on graph indicates the gain while using a DC blocking capacitor of 5.6 pF (C1) at one side of the amplifier and 2.7 pF (C2) on the other side. The capacitance value at the rear end of an amplifier does not

have a huge impact over DC blocking, as the DC currents entering the amplifier needs to be stopped at the beginning of a system. Thus, C1 needs to perform as per requirement, whereas the red and blue lines indicate gain obtained while using capacitors of value 10 pF and 1 pF respectively (in place of 5.6 pF capacitor for the purpose of comparison).



**Figure 4.7:** DC Blocking Comparison on Amplifier from Supplier B

As we can interpret from the graph, DC currents are blocked properly from entering the system and interfering with the amplifier's performance over the desired frequency range (4 GHz - 6 GHz) when the capacitance is higher. If this capacitance value is minimized, the gain starts to fluctuate as a result of current penetrating through the DC block. The adjacent graph (b) shows the input return loss while using these 3 different DC blocking capacitors. The input return loss of capacitor 5.6 pF has a much higher reflection coefficient value of -17.01 dB compared with the other 2 capacitors having return loss of nearly -15 dB, where our system requirements need the return loss to be of 12 dB or better for both Tx & Rx. These factors show that using high capacitance for DC blocks helps the system to perform well and for our case we have used 5.6 pF at C1.

Another important component used are the RF chokes, as the name indicates it is used to block the RF signals passing through and only allows the DC current along with some low frequency AC. These chokes are used to provide supply voltage or VDD to the system without allowing RF signals to interrupt with the VDD line and directing them to flow out of the system. These RF chokes are nothing but inductors which are shunt connected to the transmission lines on the path of VDD, Fig. 4.6. These RF choke and DC blocking concepts are similar for both the amplifiers that were selected for the transceiver design.

### 4.3.2 Balun

Simulation of S-parameter for balun was different from other components. A transformer was used to match impedance, isolate DC currents between circuits, and perform current or voltage step-up or step-down. An ideal transformer was used, whereas the turn ratio was  $T = \sqrt{2}$ . Figure 4.8 shows the schematic block of balun and Fig. 4.9 & 4.10 are the graphs of insertion loss vs frequency comparison based on both data-sheet and lab measurements.

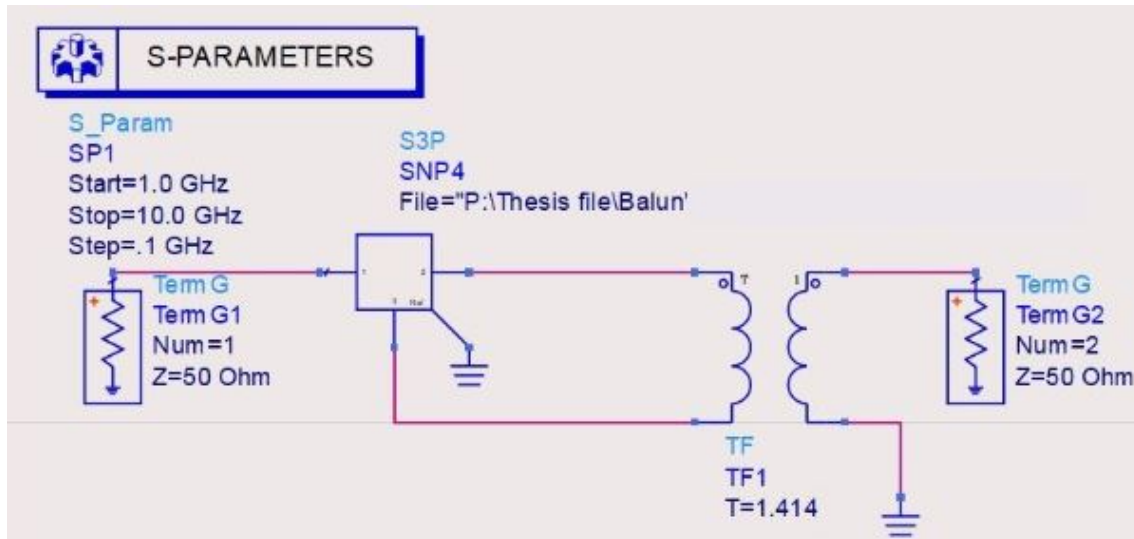


Figure 4.8: Schematic Block of Balun

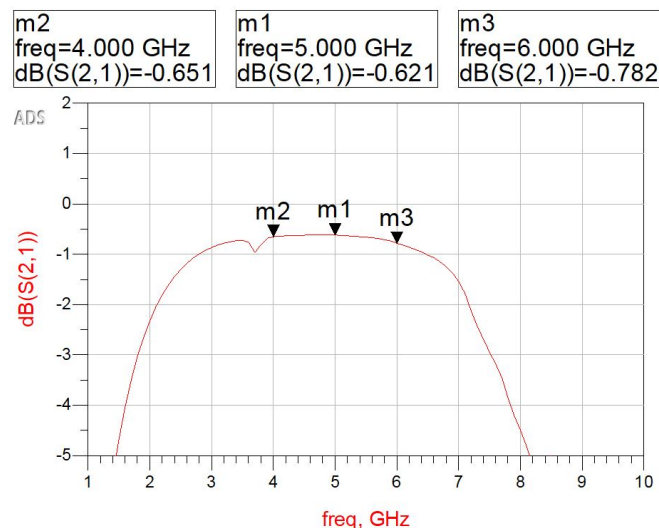


Figure 4.9: Insertion Loss vs Frequency based on Data-sheet

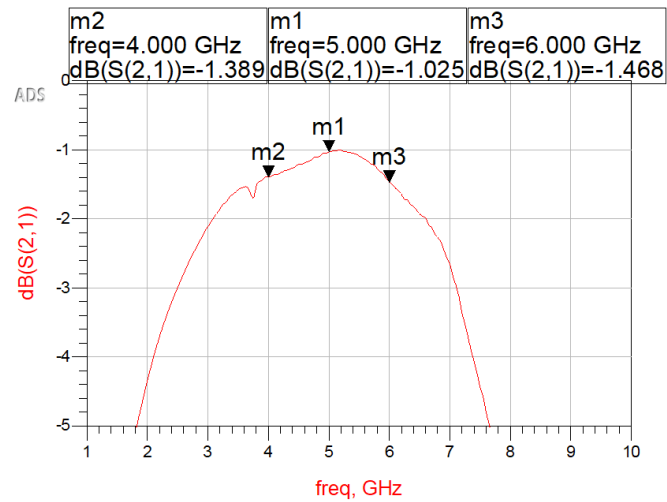


Figure 4.10: Insertion Loss vs Frequency from Lab

### 4.3.3 Band-Pass-Filter

Evaluation board for BPF that was finalized on the link budget was already available at the lab. Operating frequencies for BPF were set at a range of 4.6 GHz to 5.4 GHz but the S-parameters were measured at a range of 1 GHz to 10 GHz, in order to compare all the blocks at same frequency range. Insertion loss was supposed to be 0.7 dB at 5 GHz according to the data sheet but the S-parameter values which were given by the supplier was observed to be different. S-parameter values measured at lab were also found to differ. At 5 GHz we received 1.27 dB insertion loss and this loss included transmission line losses. Figure 4.11 & 4.12 are the graphs showcasing the insertion losses for lab tested S-parameters and supplier provided S-parameters.

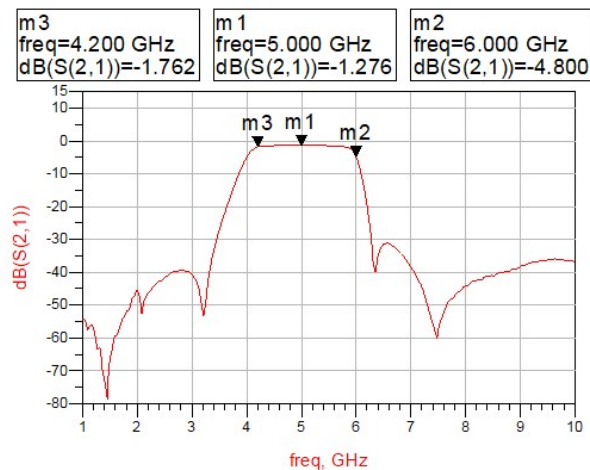
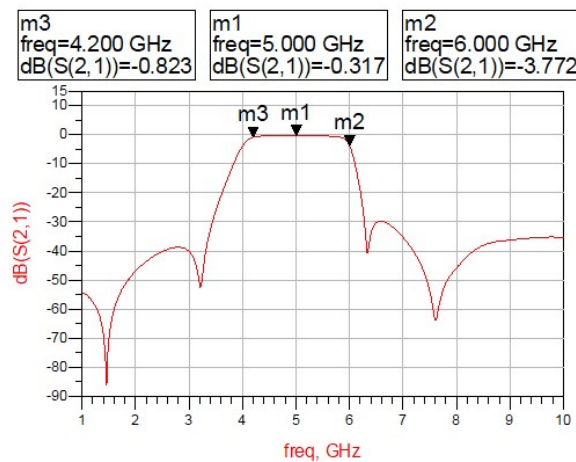


Figure 4.11: Insertion Loss of BPF in Lab



**Figure 4.12:** Insertion Loss of BPF from Supplier S2P File

#### 4.3.4 Combined Tx and Rx Path

Though we have a single combined path for Tx and Rx, line analysis were done on Tx and Rx separately for design verification. As per the link-budget, overall gain obtained was of 9.3 dB (where DSA value was -15 dB and transmission line loss at both ends were 9 dB, 4.5 dB for each end). However, higher gain was required in Rx compared with the Tx. This lead to addition of an extra LNA after the balun at Rx. Supplier A's LNA had a dedicated ON/OFF pin, unlike supplier B's amplifiers. Due to this extra shut-down pin, supplier A's LNA with 15 dB  $\pi$  attenuator was used to improve Rx gain by 5 dB. The overall gain received at the end was of 13.6 dB (Table 4.5) .

Gain	TL (dB)	Without TL (dB)
Tx	8.3	17.3
Rx	13.6	22.6

**Table 4.5:** Gain Comparison for Tx & Rx

Tx and Rx had NF of 10.93 dB and 9.7 dB respectively, which were higher than the specified requirement (NF should be below 5 dB). 50 dB gain was obtained from previous block which tends to reduce the total NF of the transceiver significantly (according to Friis equation). At the end, overall gain was mainly focused while designing the link budget of the transceiver. The line analysis of Rx can be seen in Fig. 4.13 and the graph showing the gain and input return Loss Vs frequency can be seen in Fig. 4.14. Table 4.6 shows the gain comparison for Tx and Rx with respect to link-budget and simulation results.

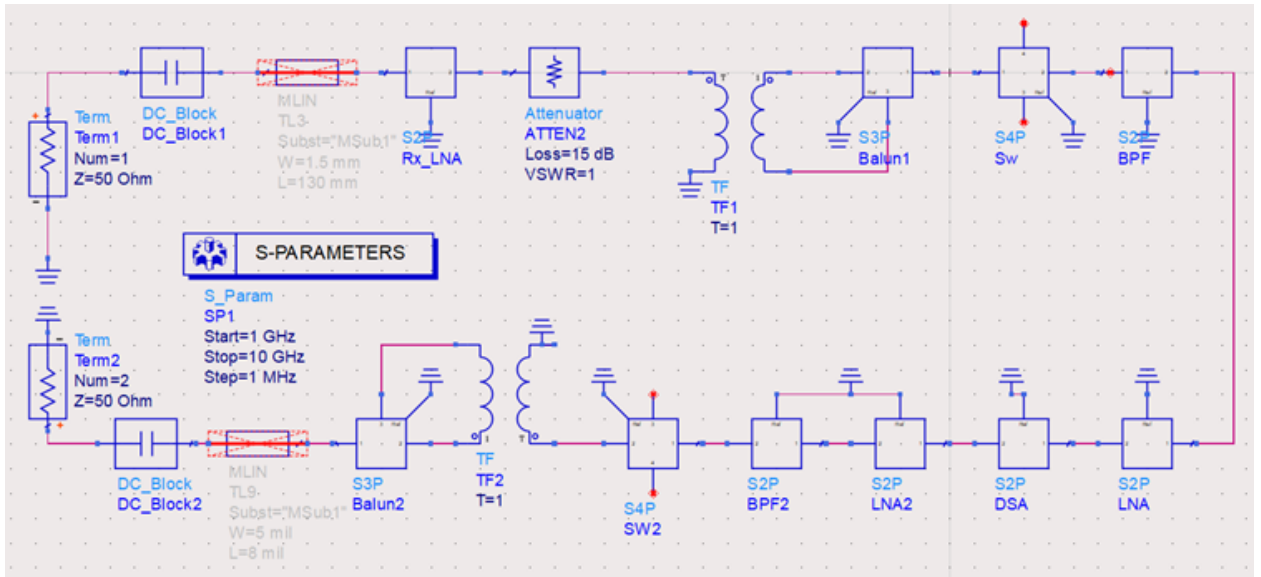


Figure 4.13: Rx-Line Analysis

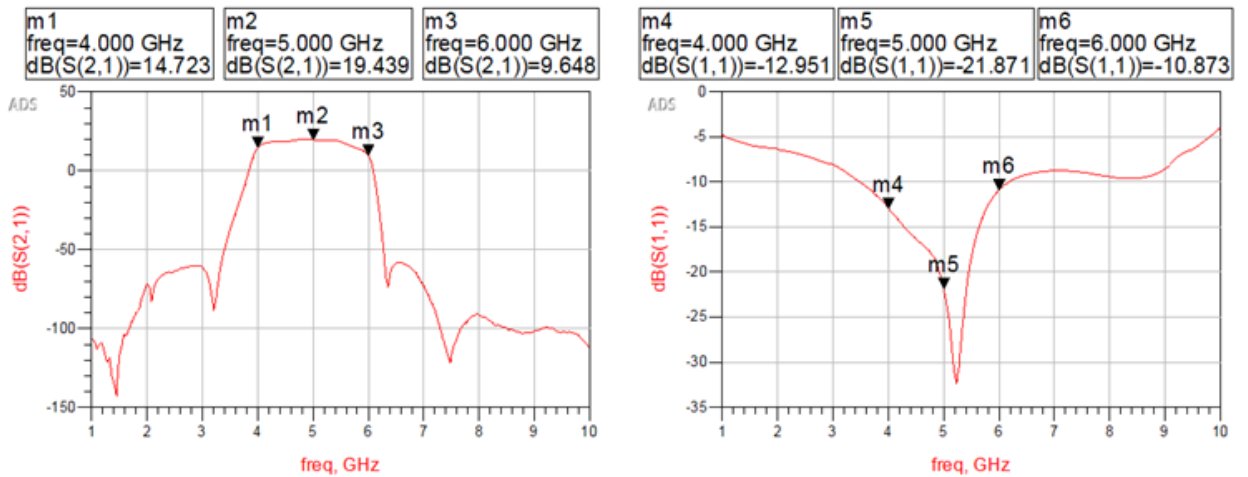


Figure 4.14: Rx Gain & Input Return Loss Vs Frequency

Gain	Link-Budget	Simulation (Lab s-para)	Simulation (Supplier S-para)
Rx	22.6	19.49	22.37
Tx	17.3	14.47	17.18

Table 4.6: Gain Comparison for Tx & Rx

## 4.4 PCB layout Designing

Once the components were verified using ADS, schematic designing of PCB was done using Cadence platform (Ericsson approved platform). Unlike ADS, PCB schematic

can be designed on Cadence using its in-built component footprints. Whereas in ADS, footprints of each and every components have to be drawn manually along with RF transmission lines (with fixed dimensions). These in-built component blocks had their own matching components and also parameters like transmission line impedance were setted manually by us. Cadence made the layout designing into a less time consuming process, where the components were chosen as per their package size and fitted along the transceiver path. Figure 4.15 shows the schematic diagram built on Cadence and this schematic layout was used for Electromagnetic (EM) simulation and transmission line-loss measurements after being uploaded and converted in ADS, which can be seen in Fig.4.16.



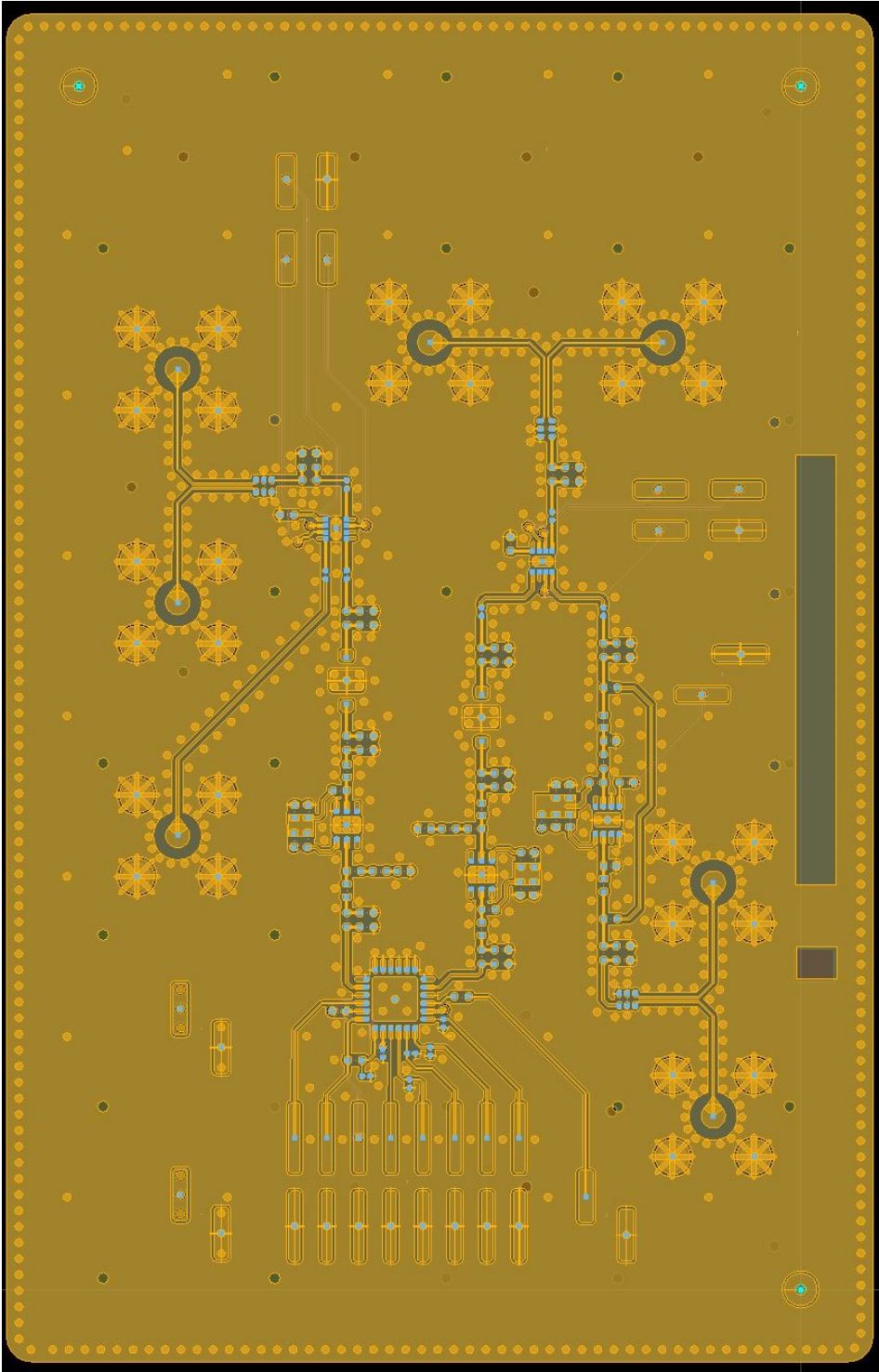


Figure 4.16: PCB Layout (ADS)

# 5

## Evaluation

### 5.1 EM simulation

Electromagnetic or EM simulation is carried out in-order to analyze the propagation of electromagnetic wave and also for the measurement of design's signal strength. EM simulation has always been an integral part of RF design and while performing this in ADS (which already has two key electromagnetic simulators integrated within its working environment), it reduces the need to use multiple designing environments.

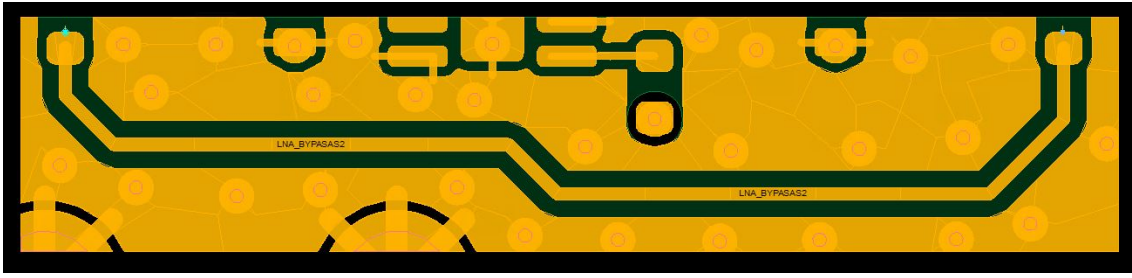
Transmission line-loss of the transceiver was calculated with this EM simulation over the desired frequency ranges with respect to the design specification. Once the line-loss of all the 50  $\Omega$  transmission lines over the PCB layout are calculated, the S-parameters of all the components will also be included in schematic analysis of the transceiver.

#### 5.1.1 Transmission line-loss Measurement

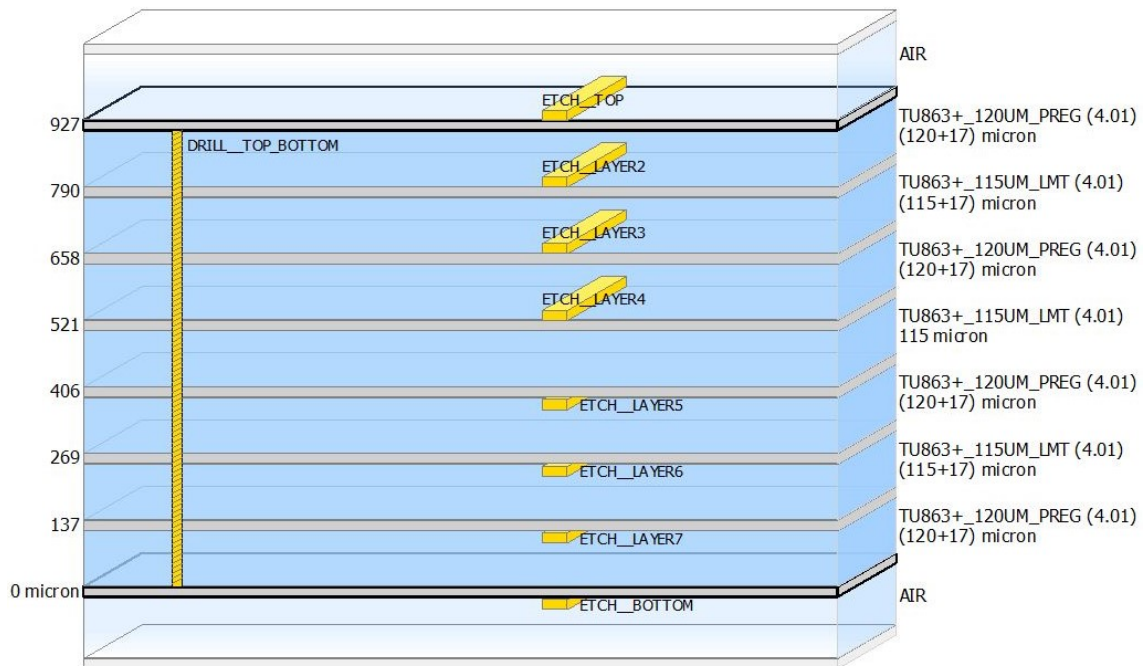
Initially the designed PCB layout was imported in ADS for line-loss calculation, where the whole layout was fragmented into individual sub-blocks for approaching the line-loss of 50  $\Omega$  lines in an accurate manner. One of such fragmented layout can be seen in Fig.5.1, where a by-pass line used on the receiver is shown. Input/output ports are placed on both ends of the transmission lines (including the pads) as P1 and P2 respectively. Figure 5.2 shows the 7 layer substrate model of the PCB before any modification and the 2 layer substrate model of the PCB consisting of only the TCP layer and the ground plane can be seen in Fig.5.3.

EM simulation settings option is accessed to generate an EM setup view for the fragmented layout. Inspection of the ports was carried out by accessing the ports option on the setup window, which was done to verify whether the ports were properly connected to the layout. Frequency range was set ranging between 4 GHz and 6 GHz on the frequency plan section. EM simulation was ran after saving the modified EM setup, which opens two task bars: a job manager (displays job simulation status) and momentum simulation status (displays simulation status and the frequency points used to achieve the converged results).

Once the job manager indicates the status as "Done", the simulation data opens showing the graphs for S11, S12, S21 & S22 in terms of dB. These graphs consist of both discrete frequency points and adaptively fitted points (shown in Fig.5.4), where a marker inserted at 5 GHz of S21 plot displays the loss as -0.597 dB at that particular frequency (center frequency of the design). The total length of this



**Figure 5.1:** Fragmented Transmission-line Segment



**Figure 5.2:** 7 layer Substrate Model of PCB

transmission line was obtained by inserting a ruler, which measured as  $17,551 \mu\text{m}$  (with respect to Fig.5.1). With both the obtained total length of transmission line and the loss at 5 GHz, line-loss of the transmission line was calculated to be  $-0.034 \text{ dB/mm}$  by the relation,

$$\text{Transmission line loss (dB/mm)} = \frac{\text{loss(at 5 GHz)}}{L(\text{total line length})} * (1 * 10^{-3}). \quad (5.1)$$

The same procedure was repeated for all the other fragmented transmission lines, which resulted in showing line-losses throughout the design ranging between  $-0.031 \text{ dB/mm}$  to  $-0.201 \text{ dB/mm}$ . While measuring the transmission line length of the design, some of the  $50 \Omega$  lines measured to be of same length (as they are identical

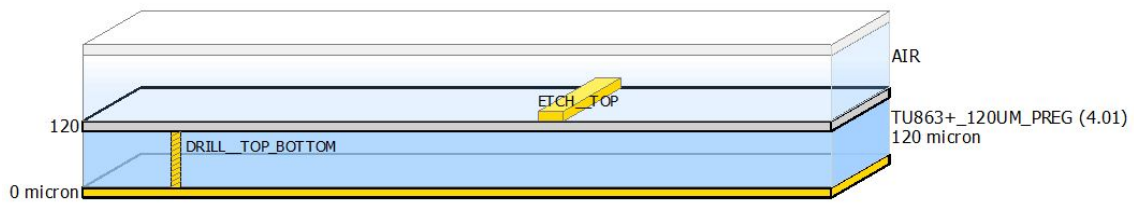


Figure 5.3: 2 layer Substrate Model of PCB

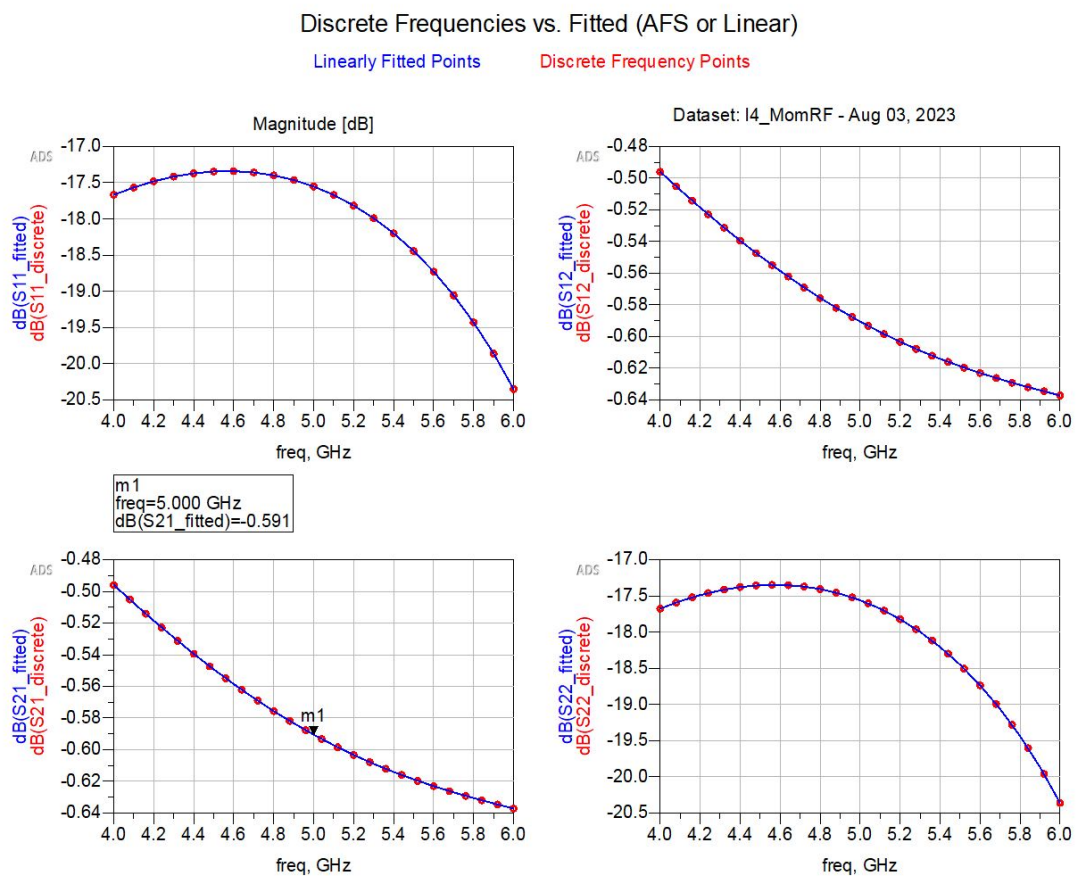
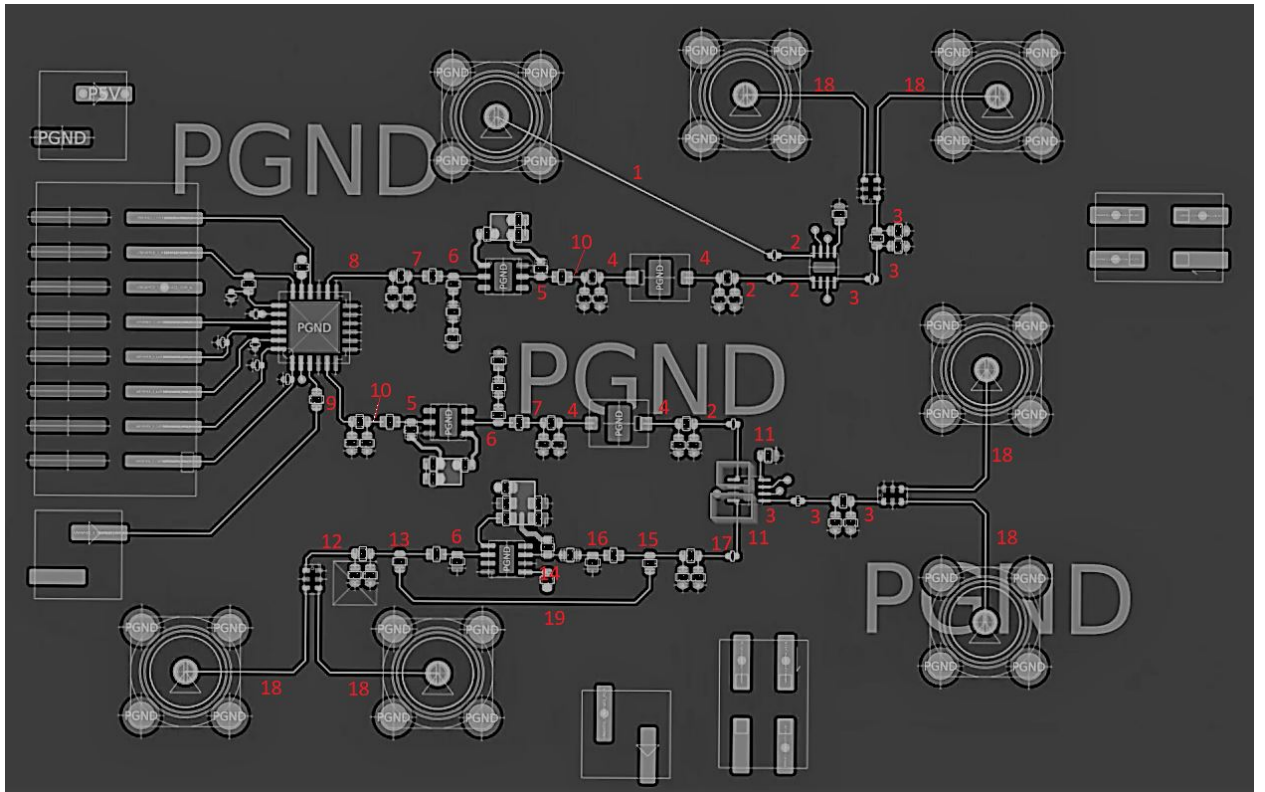


Figure 5.4: Discrete Frequencies Vs. Fitted

lines, they also have same characteristics). Thus, in order to avoid confusions they were grouped and labeled together. This gave us 19 different micro-strip line types, whereas there was a total of 41 main  $50 \Omega$  transmission lines (exclusive of shunt and matching) over the PCB layout. All these transmission lines can be seen in Fig.5.5, where they are numbered as per their type and Table 5.1 displays all the strip-line types along with their total line length ( $\mu\text{m}$ ), losses at 5 GHz and the calculated transmission line loss (dB/mm). In this table we can notice that the transmission



**Figure 5.5:** Labelled Micro-strip Lines

line types 7 & 10 have higher losses when compared with the transmission lines having higher length than them (eg. line type 2 & 3). The main reason behind this is that these small transmission lines are connected with RLC components and those RLC component's pad size is larger compared to the total line length, causing bouncing and reflecting of signals leading to higher loss.

## 5.2 Comparison with Link Budget

These obtained simulation values were compared with the link-budget (discussed in chapter 3), in order to evaluate the outcomes of the design. By setting the DSA's attenuation as -15 dB, we got a transmitter gain of 9.7 dB and a receiver gain of 14.7 dB (with additional 5 dB Rx LNA), shown in Table 5.2. The collective transmission line loss at both ends was -9 dB (-4.5 dB on each side).

In Table 4.6 we already compared the gain from our link budget along with lab measured S-parameter and the supplier's S-parameter, where the Tx gain with respect to link-budget was of 17.3 dB. Whereas the gain from ADS simulation with supplier provided S-parameter was 17.18 dB, which was quite near to our designed link-budget's gain. However, we obtained approximately 2.8 dB lesser gain from the lab measured S-parameter. This maybe due to the fact that the evaluation boards of hardware components came with a  $50 \Omega$  transmission line and RLC components

Micro-strip Line	Line Length ( $\mu\text{m}$ )	Loss at 5 GHz	Loss in dB/mm
1	20569	-1.558	-0.076
2	2254	-0.079	-0.035
3	2155	-0.081	-0.038
4	2472	-0.409	-0.165
5	2446	-0.167	-0.068
6	3148	-0.173	-0.055
7	1418	-0.266	-0.188
8	5206	-0.229	-0.044
9	4891	-0.248	-0.051
10	1325	-0.266	-0.201
11	5188	-0.159	-0.031
12	3991	-0.226	-0.057
13	3850	-0.296	-0.077
14	2788	-0.154	-0.055
15	4025	-0.295	-0.073
16	2080	-0.174	-0.084
17	2079	-0.198	-0.095
18	4200	-0.164	-0.039
19	17551	-0.597	-0.034

**Table 5.1:** Micro-strip Line Types & Their Losses

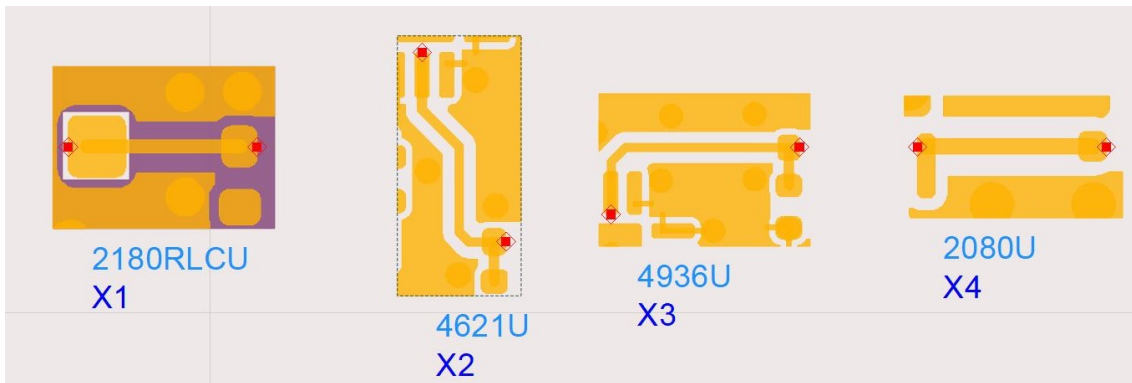
Gain	Tx (dB)	RX (dB)
With TL	9.7	14.7
Without TL	18.7	23.7

**Table 5.2:** Gain Comparison for Tx & Rx

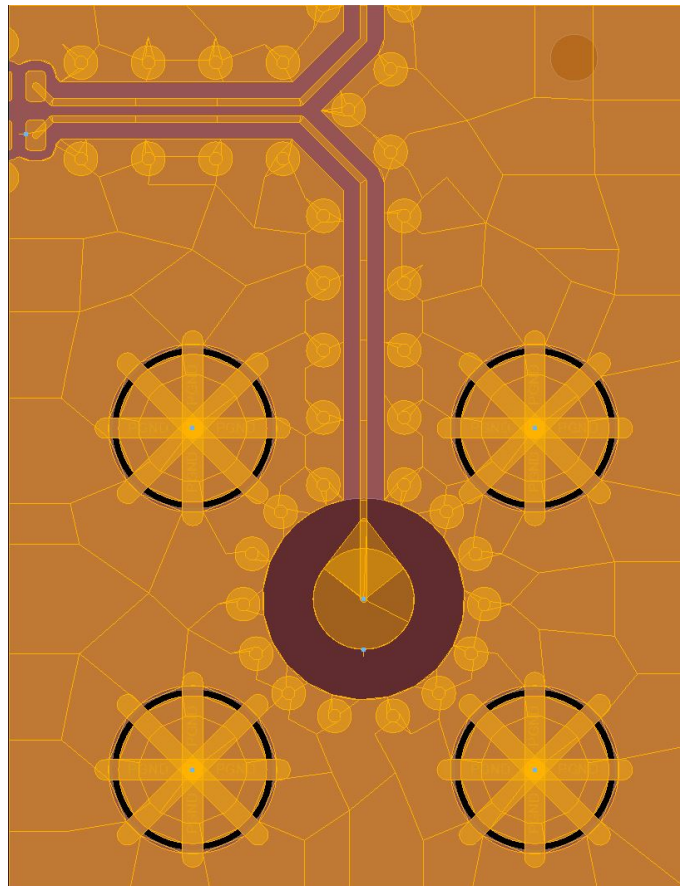
attached in it. In addition to that, the measuring cables have their own losses as well. Figure 5.6 shows some of the 50 ohm transmission lines from the layout, where transmission lines with their connecting pads can be clearly seen (the red dots represents the connecting ports).

At the receiver line we got a gain of 19.49 dB with an average loss of -0.08 dB/mm, where initially transmission line type 18 (Fig.5.5) was used, which had a high insertion loss of -2.5 dB at 5 GHz. These were the 100  $\Omega$  lines present on the layout, which all had an individual length of 11947  $\mu\text{m}$  and -0.21 dB line loss per mm. These lines had a 45° angle bend which can be seen in Fig.5.7, causing the signals to bounce over the path leading to increase in losses. They were cut into transmission lines of length 4200  $\mu\text{m}$  (shown in Fig.5.8), as they were not part of the actual design. The 45° angle bend and Sub-Miniature version A (SMA) ports were only used for the test boards.

Another transmission line connected with BPF that had an impact over the signal's pass-band (causing ripples) was line type 4. On the design, filters from supplier M were used which had connection pads larger than the pads of other components. These larger connection pads resulted in creating parasitic capacitance, which is



**Figure 5.6:** 50 ohm Transmission Lines

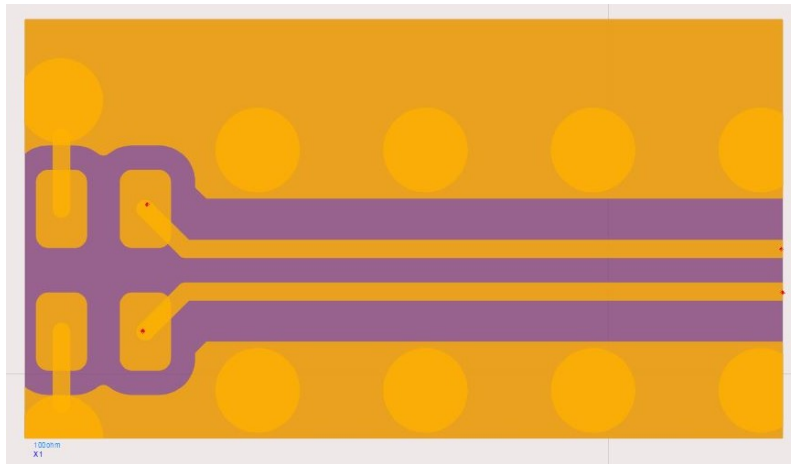


**Figure 5.7:** Transmission Line type 18

both unwanted and unavoidable in PCBs. This capacitance is directly proportional to the difference between area of a trace ( $a$ ) and distance amidst 2 traces ( $d$ ),

$$C \propto \frac{a}{d}. \quad (5.2)$$

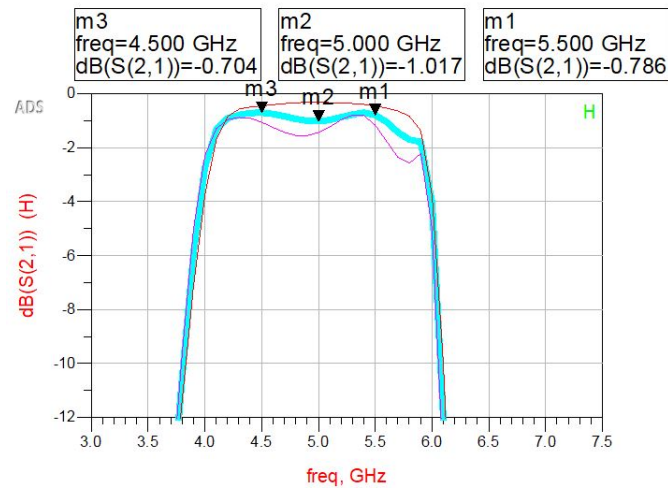
Here,  $a$  is the pad's area and  $d$  is the distance between pad and PCB layer. As



**Figure 5.8:** Modified Transmission Line type 18

per eq.5.2, these pad sizes increases the capacitance and they cannot be altered as they are of fixed dimensions. So, the height between the PCB layer and the pads was increased in-order to improve the design's performance. This was achieved by removing 4 layers beneath the pad and making it closer to the ground plane. By removing an intermediate layer, the height increases twice its original value. Thus, at the end of modification by removing 4 layers the height was increased to  $600 \mu\text{m}$  from the original height of  $120 \mu\text{m}$ , where the distance amidst a single layer was of  $120 \mu\text{m}$ .

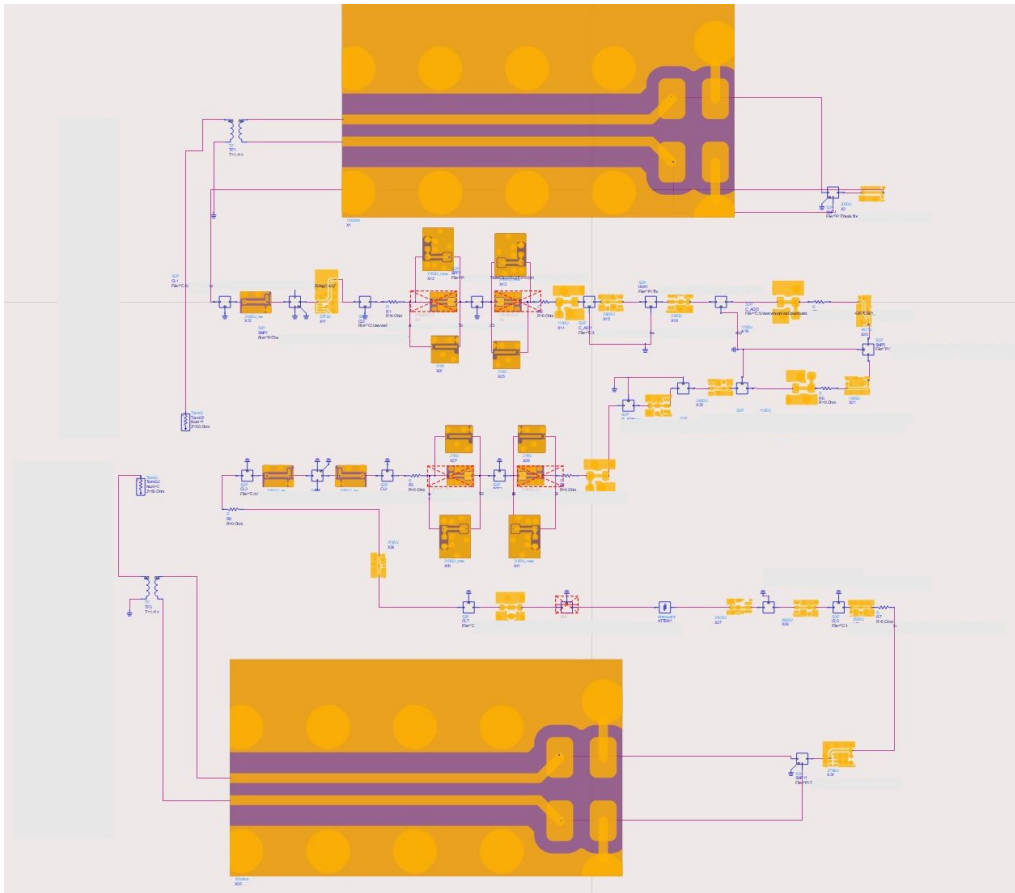
Figure 5.9 shows the comparison of pad's impact on the BPF, where the red line indicates its pass-band when connected with a  $50 \Omega$  transmission line without connecting pads. Here there is no ripple to be seen over the band. Meanwhile the blue line represents the pass-band of BPF when connected with a transmission line along with its pads. In this case, 4 layers under those connecting pads were removed. Pass-band of BPF when connected with transmission line along with its pads, where no underneath layers were removed is indicated using the purple line. This particular scenario creates the parasitic capacitance and we can also notice the ripple on its pass-band significantly.



**Figure 5.9:** Comparison of Pad's Impact over BPF's Pass-band

### 5.3 Results

Four different cases were ran in ADS to simulate and compare the results. Since our BPF's pass-band range is 900 MHz, all the simulations were run over the range of 4.5 GHz to 5.4 GHz. The designed PCB layout was ran on ADS, where the S-parameter files of all the components were uploaded and connected with transmission line and RLC components. Figure 5.10 and 5.11 shows the schematic representation of the receiver's and transmitter's transmission lines respectively.



**Figure 5.10:** Receiver's Transmission Line (ADS Simulation)

### 5.3.1 Case 1 : Without Transmission Lines

The first case was to simulate without transmission line, which gave us a gain of 21.56 dB at 5 GHz (receiver). Both the obtained gain and the link-budget estimated gain were more or less the same. Thus, it can fulfil our link-budget requirement.

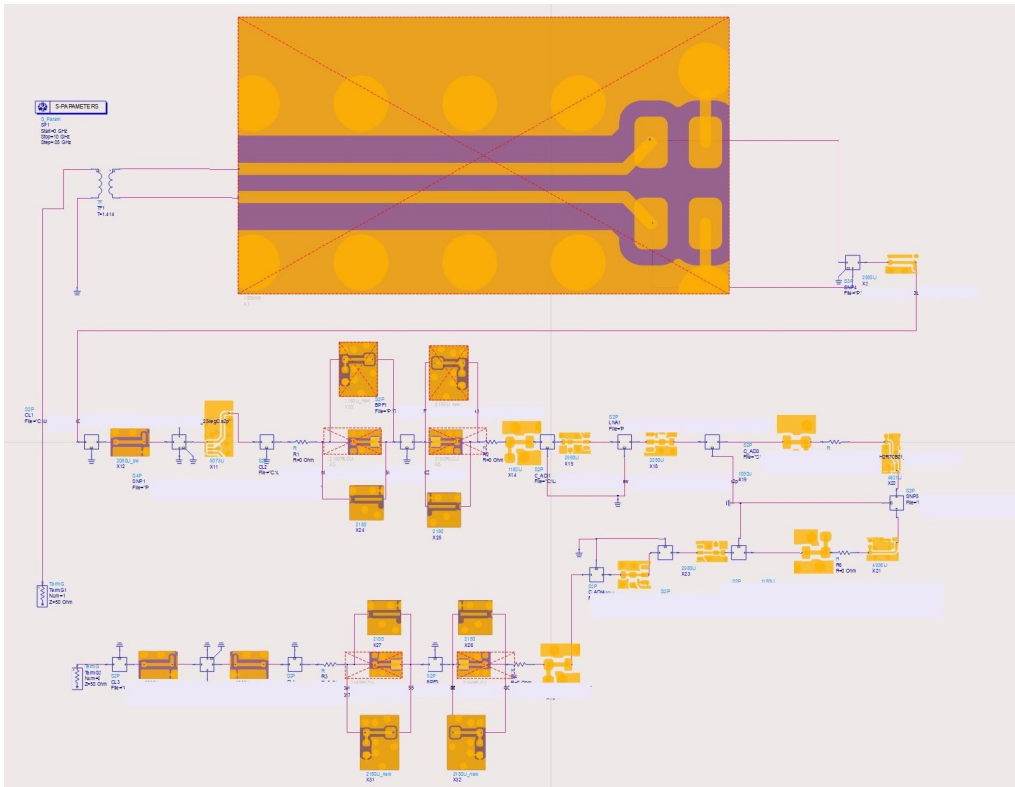
Figure 5.12 and 5.13 shows the total gain of receiver and transmitter simulated without transmission lines. Receiver's pass-band has a gain of 21.56 dB, whereas the transmitter has a gain of 18.04 dB. These gains are obtained without undergoing any transmission line losses.

### 5.3.2 Case 2 : With Transmission Lines

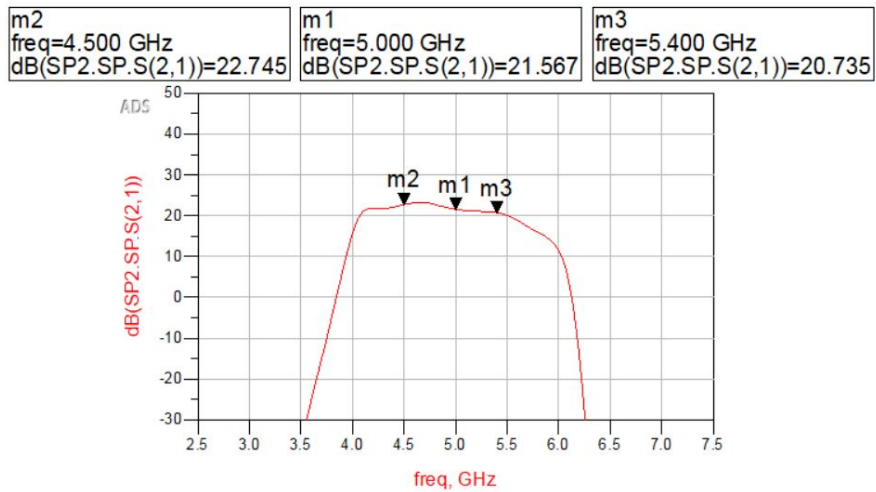
In this case, all the components were connected with the chopped 50  $\Omega$  transmission lines. Due to the impact of BPF's large pad size, ripples were formed on the pass-band and the gain obtained for this case was of 18.99 dB (receiver). Whereas the link-budget estimated gain was of 22.6 dB at 5 GHz. However this gain starts to decrease approximately 1.8 dB for the receiver and nearly 1 dB for the transmitter at 5.4 GHz.

Figure 5.14 and 5.15 shows the total gain of receiver and transmitter simulated with the transmission lines. Receiver's pass-band has a gain of 18.99 dB, whereas the

## 5. Evaluation



**Figure 5.11:** Transmitter's Transmission Line (ADS Simulation)



**Figure 5.12:** Receiver without Transmission Line

transmitter has a gain of 15.11 dB. These gains are quite low compared to the gains obtained in case 1, due to the presence of transmission line losses.

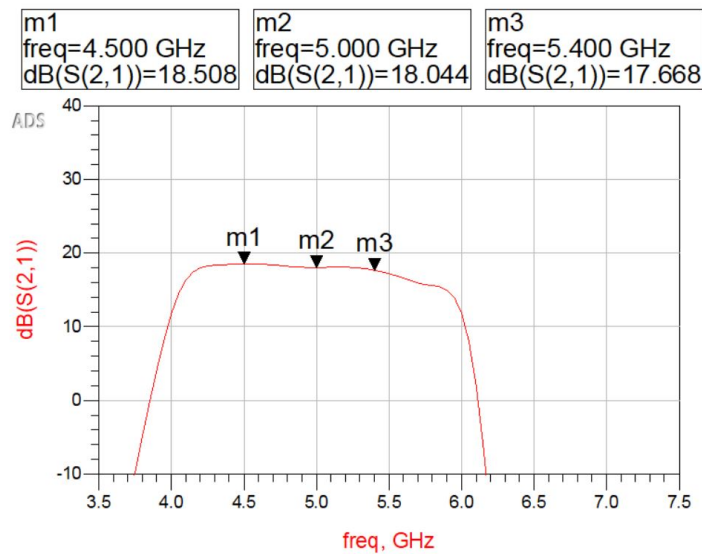


Figure 5.13: Transmitter without Transmission Line

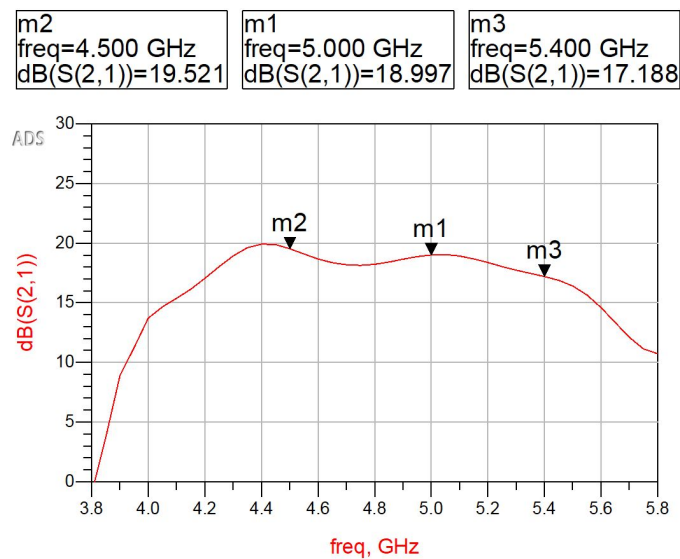


Figure 5.14: Receiver with Transmission Line

### 5.3.3 Case 3 : With Connecting Pads in BPF

Case 3 was executed by running simulations with the regular transmission line set-up, where the BPFs were connected along with their connecting pads. In this connection, a ripple was observed over the pass-band which impacted the gain by fluctuating it nearly 2 dB for both Tx and Rx.

Figure 5.16 and 5.17 shows the total gain of receiver and transmitter simulated with the BPF's connecting pads. Receiver's pass-band shows a significant ripple giving a gain of 15.83 dB, whereas the transmitter has a gain of 12.74 dB. These gains are comparatively 6 dB lesser to the gains obtained in case 1 and 3 dB lesser than the

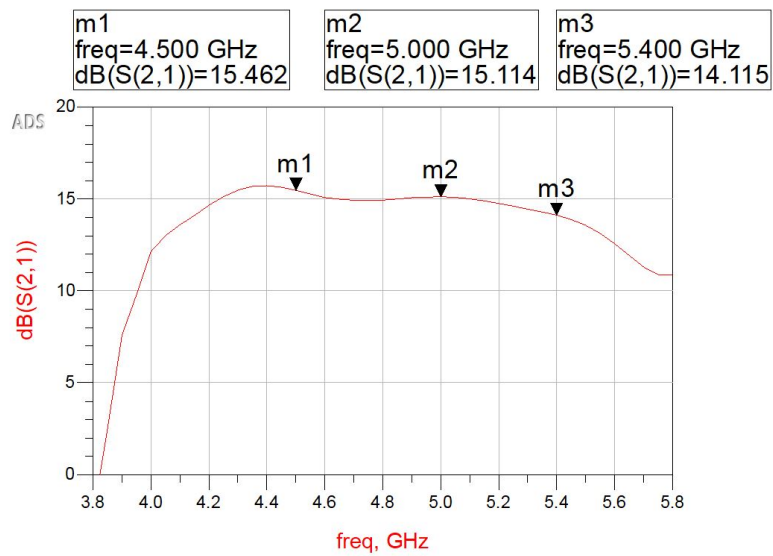


Figure 5.15: Transmitter with Transmission Line

gains of case 2.

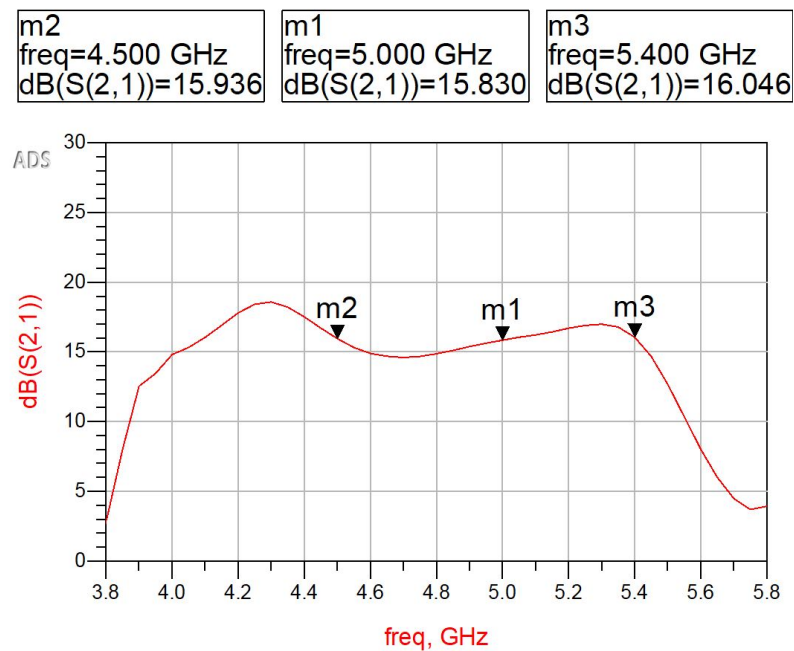
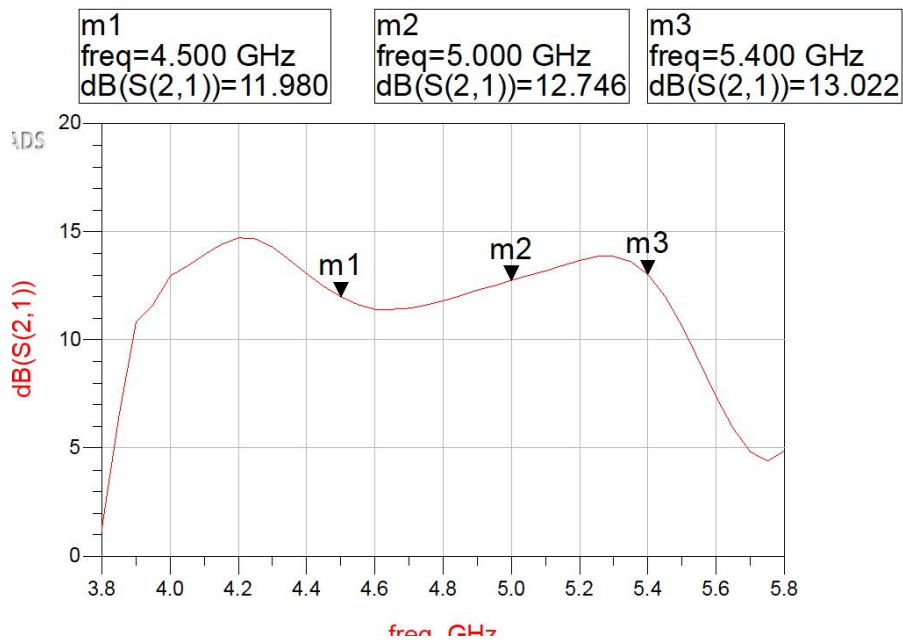


Figure 5.16: Receiver with BPF's Pad

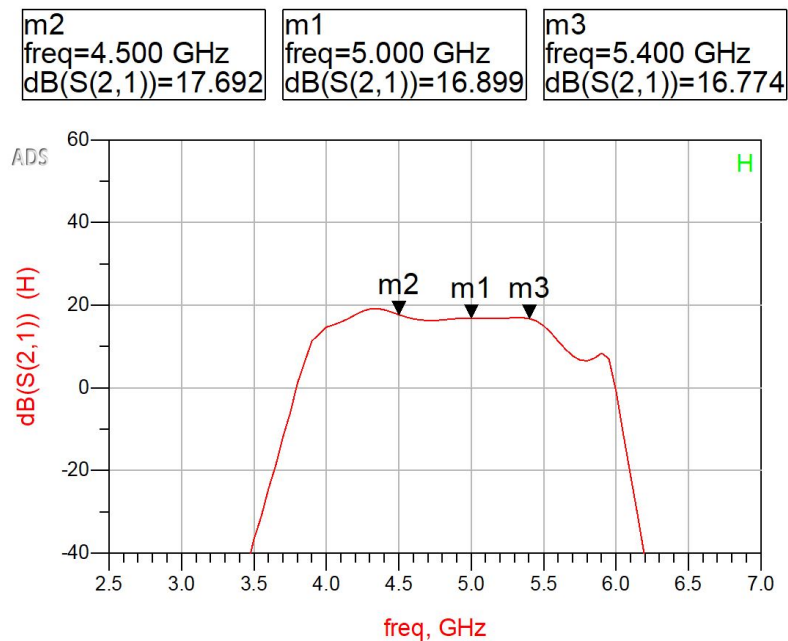
### 5.3.4 Case 4 : With Modified Connecting Pads in BPF

In this case, the overall gain of the design was improved by removing 4 intermediate substrate layers on the BPF's connecting pads. This helped with rectifying the fluc-



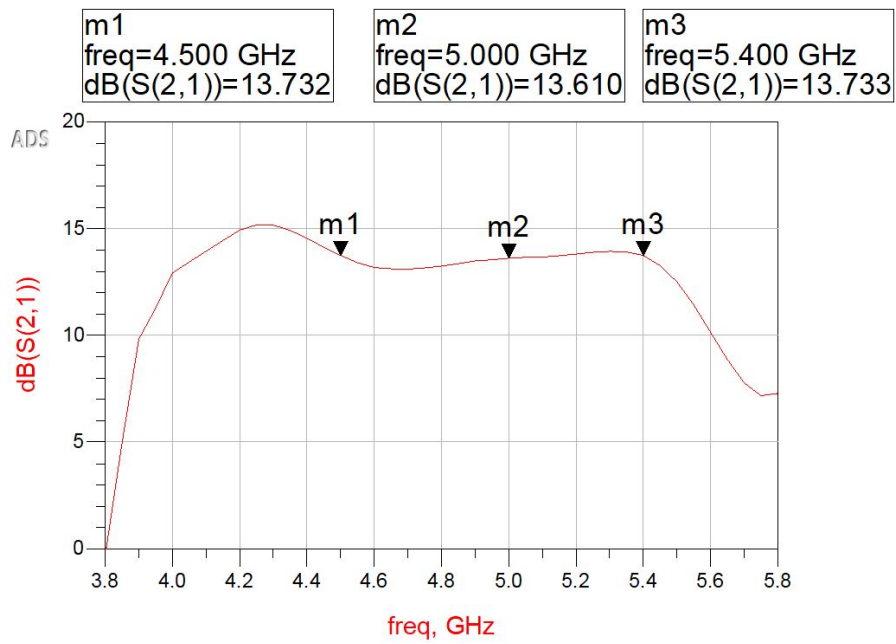
**Figure 5.17:** Transmitter with BPF's Pad

tuations found on the pass-band and avoiding the impacts of parasitic capacitance (formed due to the large connecting pads on the BPF).



**Figure 5.18:** Receiver with Modified BPF Pads

Figure 5.18 and 5.19 shows the total gain of receiver and transmitter simulated with the BPF's modified connecting pads. Receiver's pass-band shows a significant ripple giving a gain of 16.89 dB, whereas the transmitter has a gain of 13.61 dB.



**Figure 5.19:** Transmitter with Modified BPF Pads

These gains of transmitter and receiver seems to have been improved by 1 dB when compared with case 3.

# 6

## Conclusion

A new transceiver was designed and evaluated at intermediate frequencies around 5 GHz, which will help in replacing the existing model of separate Tx and Rx. This combined structure helped in fulfilling the main objective of this thesis project by using a common block of hardware components instead of separately dedicated up-link and down-link. This helped in minimizing the cost, size and number of hardware components used all over the system, while enhancing the efficiency. Such a transceiver layout was designed on Cadence based on the components chosen from a link-budget, developed from scratch making sure it fulfilled all the existing block requirements (such as gain, noise figure, thermal noise propagation and so on).

S-parameters of all the hardware components were tested in laboratory and their performance were studied by verifying those S-parameters using ADS. The impacts that DC blocking and RF chokes had on amplifiers were also studied in ADS. In the end, analysis of combined Tx/RX path was also done and the gains of transmitter and receiver were compared and studied with respect to the estimated link-budget gains. What primarily was supposed to be a manual testing of manufactured PCB at laboratory (designed from the Cadence), turned into evaluating them on software. This was to rectify the time constrain we had from waiting for the PCBs to be produced, followed by debugging the errors in them. Simulations of the transceiver layout were ran using ADS software, where all the transmission line losses were studied using EM simulation over the desired frequency range. After fragmenting the entire PCB layout, line-losses of all those 50 ohm and 100 ohm transmission lines were calculated at 5 GHz. Simulations using all these line-losses were done in order to compare their results with the ideal link-budget values. The same procedure that was done during ADS verification was repeated but including the transmission line losses and RLC components produced a new set of simulation results, which totally varied from the results of previously used transmission scenario.

The large connection pads of BPF ended up producing unwanted and unavoidable parasitic capacitance, which disrupted the performance of the transceiver (generated ripples over the pass-band). However its impact was reduced by eliminating few PCB substrate layers beneath those pads, which correspondingly reduced the distance in between pads and the ground plane trace. Four different scenarios were used in comparing those results, which concluded that removal of substrate layers under the large connecting pads of BPF improved the gain when compared with the simulations obtained while using those pads as it was. Though these results were differing from the initial link-budget results, it was mainly due to the reason that ideal performance of a system is not possible in real time due to presence of transmission line losses, losses in connecting probes, noise, parasitic capacitance, etc. In the end, design and

## 6. Conclusion

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evaluation of a combined Tx/Rx path was executed successfully, were the results obtained satisfied all the initial requirements we had and for the case of future work, all these software simulated results can be tested and compared manually in laboratory using hardware PCBs over a wide range of scenarios as desired.

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