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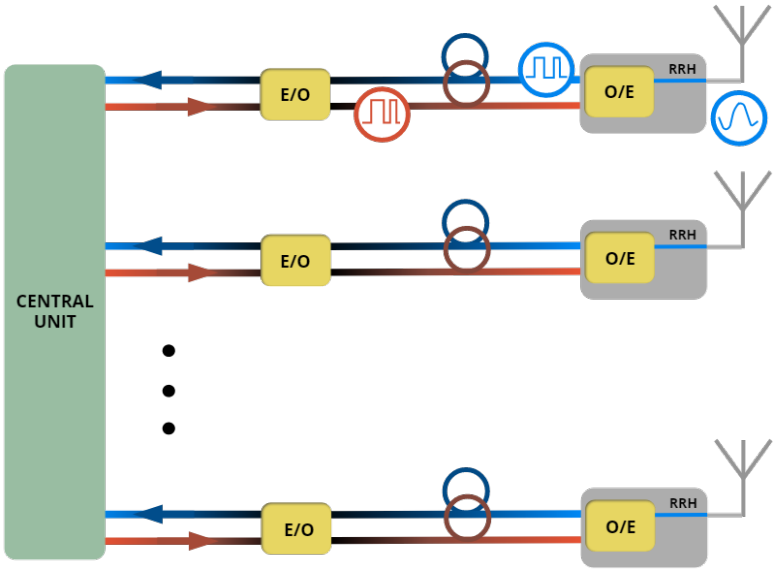

Realization of a 1-bit RF receiver

An implementation method for distributed MIMO over fiber

Master's thesis in Wireless, Photonics and Space Engineering

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Department of Microtechnology and Nanoscience
Chalmers University of Technology
Gothenburg, Sweden 2019

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Abstract

Development of wireless networks enforce research on new system designs, always in profit of improving certain features. A distributed MIMO network is defined by moving the antennas away from the base station, gaining spatial degrees of freedom. This technique has proven to meliorate some of the experienced difficulties in a collocated MIMO system, inspiring further research. In profit of understanding the capacity and limitations of such a network it is advantageous to enable actual measurements by building a testbed. Further, 1-bit receiver technology is promising in reducing analog system complexity, migrating as much as possible to digital domain at the central unit. This project entails research on the implementation of a distributed MIMO 1-bit RF receiver, including measurements and hardware analysis. It proves that such a system is in fact realizable with off-the-shelf components, although demands further development to gain flexibility.

Acknowledgements

I have had the fortune to work on an inspiring project with very inspiring people. With special thanks to Ibrahim Can Sezgin and Sven Jacobsson, providing both inspiration, hours of support and a good time meanwhile. I have truly learnt more from you than I have in any course during my years at the university. Further I would like to thank my examiner Christian Fager and Mikael Coldrey at Ericsson Research for the encourage and contribution with your great expertise.

Lise Aabel, Gothenburg, May 2019

Abbreviations

ADC	Analog to Digital Converter
BER	Bit Error Rate
CFO	Carrier Frequency Offset
DAC	Digital to Analog Converter
DSP	Digital Signal Processing
FPGA	Field Programmable Gate Array
ISI	Inter-Symbol Interference
MIMO	Multiple Input Multiple Output
MSE	Mean Squared Error
OFDM	Orthogonal Frequency-Division Multiplexing
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RRH	Remote Radio Head
SDR	Signal-to-Dither Ratio
SFP	Small Form-factor Pluggable
SNR	Signal-to-Noise Ratio
STO	Symbol Time Offset
VCSEL	Vertical-Cavity Surface-Emitting Laser

Contents

1 Introduction

1.1 Background

In the constant pursuit of higher data rates in wireless communication systems, many different techniques are being considered in 5G development. The invention of multiple-input multiple-output (MIMO) systems revolutionized the field of wireless communication. A MIMO network is able to support multiple channels simultaneously, enabled by using many antennas in one base station. At its invention it offered a vast capacity extension, which widened the bottleneck limiting the data rate. The advantage of MIMO is overpowering the competition, making it the most implemented type of communication system today.

Designing a multi-antenna system opens up a number of choices and trade-offs, since some profits come at the cost of others. One feature to consider is the spatial distribution of the base-station antennas. The optimum choice of layout depends on the application, but collocated base-station antennas is the most popular design. In that case the antennas are all located in a pattern at a common spatial location. Collocation has advantages in several situations, i.e. in system design and coherency. But under certain circumstances a collocated system faces challenges regarding shadowing and outage. For example, in urban areas the rich multipath environment can increase the probability of outage. An alternative design to collocation involves distributing the antennas, which may improve the capacity where the collocated system is deficient. The main advantage is that the area of visibility can be vastly enlarged. Distributed MIMO is a promising research area, and as the niche to this project a unique solution will be presented as a receiver implementation for this type of network.

Part of the physical network will now be separated from the central unit, where everything was located in the collocated network. The front ends, where the distributed antennas are located, will further be called *remote radio heads (RRHs)*. As a profitable solution in several aspects, the RRHs would advantageously be constructed in the simplest way possible. Migrating as many functions as possible to the central unit makes the system less vulnerable and simplifies the design. With this in mind, the interest is germinating for 1-bit receiver technology. The core to this idea is that commercially available analog-to digital converters (ADCs) are reaching higher capacity in sampling rate. A high sample rate can diminish the need of down-conversion, hence eliminate the common requisite mixers. There is just one problem to this notion: at high sample rate and high resolution, the ADC becomes heavily power consuming. 1-bit receiver technology proposes a receiver layout using high sample rate ADCs at low resolution, circumventing a high power consumption. Combining the idea of distributed MIMO and 1-bit reception, a unique idea for the realization of a testbed is proposed in this report. A testbed enables real measurements and further understanding of system performance and limitations.

The entrance to this project is founded by a prior research project; a *distributed MIMO sigma-delta over fiber* testbed for downlink has been built at the department of Microtechnology and Nanoscience, MC2, at Chalmers University [1], [2]. The publication proposes a solution for a similar network, and requires the realization of an uplink for completeness. As will be explained in this report, for a low resolution quantized signal, the restoration is highly noise-dependent. One of the main technical challenges is hence to solve the requirement on noise-control. Further, to get a high data stream between the RRH and the central unit, fiber cable provides a robust point-to-point link and allows for antenna distribution.

1.2 Previous work

Several studies on different aspects of 1-bit receiver technology have been published prior to this project. For instance, the study in [3] treats simulations for a massive MIMO uplink using 1-bit ADCs at each antenna, focusing on different detection techniques and the effect on channel estimation. Such studies are informing regarding signal processing, but do not attend system implementation and antenna distribution. Further, the study in [4] regards an uplink solution using 1-bit quantization at a remote radio-head, similar to what is presented in this report. However, the implementation in [4] is strictly limited in flexibility by the proposed hardware implementation, using a demodulation technique fully dependent on a known reference signal, aggravating the implementation of a testbed. No previous work with the same system proposal antecedent to this project has been reported.

1.3 Aim and contribution

The aim of the project is to develop a realizable uplink solution to a distributed MIMO over-fiber testbed by implementing 1-bit quantization, and accordingly study its key features. In collaboration with MC2 and the research department at Ericsson, the result shall provide all parts with valuable practical insights on the chosen type of system design.

1.4 Scope

In early stages of research projects the purpose demarcation is decisive for a coherent work process and to present results true to the context. The primary focus has been the understanding of the proposed system, rather than an actual implementation. With this entry the project will not include component design, but the relevant components will be commercial off-the-shelf. Further the RRH will not be tested as an integrated unit, but in a measurement environment. A proposed design of a complete receiver is presented in this report, but tests are performed at a measurement setup imitating the same functionality. Focus for tests has been on development and measurements of a single link, denoted a single-input single-output (SISO), with the ability of single-input multiple-output (SIMO) extension. A total system evaluation including both uplink and downlink is beyond the scope of this project, with the focus on the technical solution of the uplink.

1.5 Problem definition

Can a distributed MIMO uplink system be realized using 1-bit over-fiber technology? Is the chosen distributed MIMO over-fiber uplink technology a profitable solution compared to a classical MIMO setup? What are the limitations/difficulties in such a design?

2 Method

To understand the functionality of a 1-bit receiver architecture, a literature study ran in parallel with the digital signal processing construction to familiarize with signal processing as a subject, as well as the new type of network. Part of the work included establishment of instrument setup; to build a complete measurement environment enabling analog signal transmission and reception. Instrument communication as well as signal processing has been performed in

MATLAB. The majority of studies were performed in a lab environment, to get realistic insight in how to realize the actual system. A major part of work included comprehension of analog 1-bit quantization components. Assembly, construction and testing was performed at the Chalmers' laboratory. During all processes of the project, constant feedback meetings were held to progress as efficiently as possible.

3 Design concept

The profits of MIMO systems are well proven, making development of MIMO technology of high interest. In addition, distributed MIMO is proven to meliorate some of the deficiencies of a collocated MIMO system [5], [6]. In the pursuit of low power consumption and economically profitable solutions, interest germinate for low resolution networks, which makes the niche of this project. Explanation and motivation of the key system elements follow in the sub-sections of this chapter.

3.1 Distributed MIMO

Indoor and urban environments interfere with signals through reflection, diffraction and scattering, causing multipath propagation. The consequence is a distribution of amplitude, phase, angle-of-arrival and polarization at the receiver [7]. In the presence of a line-of-sight component between a transmitter and receiver, the direction of the strongest signal path is known. In that case the signal-to-noise ratio (SNR) can be increased by increasing the antenna directivity, but in reality it is rarely that simple. In the absence of line-of-sight in a rich multipath environment, the SNR will generally not increase by increased directivity, since radiation is incident at a distribution of angles [7]. A solution to this problem is the diversity antenna system, using several receiving antennas. In its foundation this implies observing a signal from a number of different points and combining them, gaining SNR from the statistical benefit. The classical realisation of such a system is to collocate a number of antennas, commonly as a multi-port base station, where each antenna port is receiving a version of the signal. In addition to multiple ports, the antennas are often rather antenna *arrays*, adding a degree of freedom to the system in the form of beamforming [8]. Collocation is the common design of MIMO, it is profitable from a system point-of-view and facilitates coherency at the receiver. However, collocation entails problems such as spatial correlation and shadowing [5]. Spatial correlation implies that the channels are not *independent and identically distributed*, as is the ideal case for the diversity system. Regarding shadowing, this is simply a result from the spatial relation between the receiver and the user. One solution to overcome some of the difficulties of collocated MIMO is to spread the antennas to gain spatial degrees of freedom, called a *distributed* MIMO system.

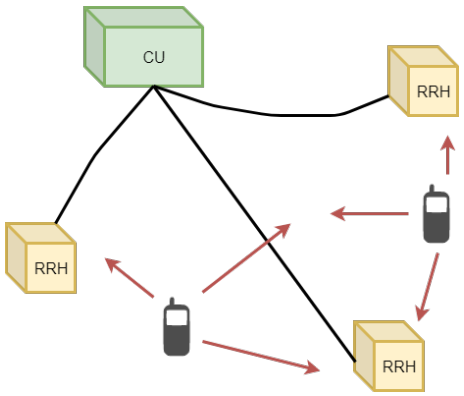


Figure 1: The layout of a 2x3 distributed MIMO receiver containing a central unit (CU), remote radio heads (RRH) and two users.

A distributed network structure discards the classical cell-layout, since the RRHs can be placed at an arbitrary distance from the central unit, as illustrated in figure 1. Spatially distributing the antennas reduces the probability of outage, becoming the springboard of the system benefit. The explanation is that the probability that a user has a good connection with one of the RRHs

is higher than connecting to one base station with collocated antennas. However, as with most technical solutions, distributed MIMO brings new challenges to the table.

A significant property of a receiver is its coherency, designating the aspect of keeping track of the relative phase of the received signals. With correct knowledge of the phase relations the signals can be constructively added at the receiver, in benefit of optimum decoding. Coherency is affected by many different features, and is challenging in the distributed MIMO network architecture because of the spatial distribution. This makes one of the design challenges in this new system topology.

3.2 1-bit RF quantization

To pick up an analog signal and process it digitally, it must be converted into digital *samples*, performed by an ADC. According to the well known Nyquist sampling theorem, the *sampling rate* of the ADC must be at a minimum two times the highest frequency component of the signal to sample. Traditionally, a receiver architecture includes one or several mixer stages performing down-conversion from RF to an intermediate or baseband frequency, due to limited ADC sampling rate. However, in pace with technology development, increased ADC performance allows for higher sampling rates. The higher the sampling rate, the higher the frequency that can be sampled for a correct read, thereby allowing sampling at a higher intermediate frequency. Accordingly, at a sufficiently high sample rate there would be no need for down-conversion. Eliminating the need of a mixer stage is advantageous, since mixers in practice raise system challenges, such as introducing frequency offsets. In a distributed MIMO network, mixers at each link would demand extensive synchronization efforts to keep the relative phases synchronized in profit of coherency. This fact makes the high capacity ADC very attractive in research on distributed networks.

When a signal is sampled, it is converted into *quantization levels*, defined by the resolution of the ADC. For example, an 8-bit ADC quantifies a signal into 2^8 different amplitude levels, which can be interpreted as the resolution of the sampled signal. A high sampling rate and high resolution ADC accordingly approaches an accurate read of an incoming signal, seemingly preferable. However, the energy consumption at high sampling frequencies increases with the number of quantization levels [9]. The envelope in figure 2 implies that the energy per conversion step is overall increasing at Nyquist sampling frequencies ($f_s/2$) above 1 GHz. Striving for minimum power consumption, the alternative is to either sample at a lower rate or at low resolution. This is what founds the motivation for the 1-bit quantization system proposed in this project: sampling at a high rate and low resolution.

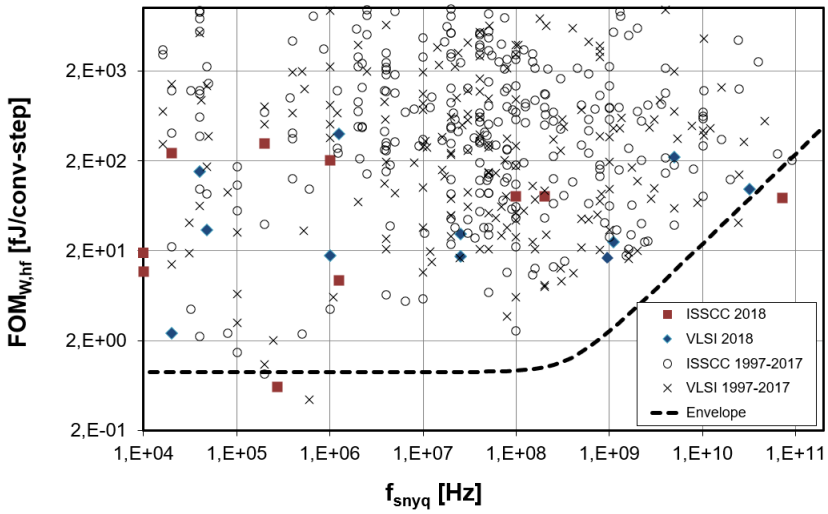


Figure 2: A plot of energy consumption per conversion-step for different ADC types. The figure of merit (FOM) has the unit fJ per conversion-step, and is plotted versus Nyquist sample frequency. The envelope represents the overall increased power per conversion step, increasing with frequency [9].

A 1-bit quantization converts a signal to the lowest possible resolution, since the 2^1 amplitude levels simply results in a high or low output value. The benefit of quantizing a signal at such low resolution is that the RF signal can be sampled avoiding down-conversion to an intermediate frequency and without consuming excessive amounts of power. However, this low resolution requires a new perspective on the nature of the sampled signal.

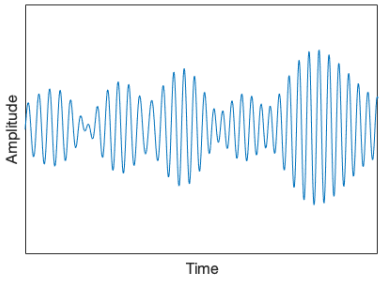
In wireless transmission, information is encoded into a transmittable waveform, commonly through amplitude and phase variations. When such a signal is sampled by a 1-bit ADC the digital samples takes only two quantized values. It is important to understand that the description in this chapter of how the method works is shaped merely to build an *understanding* of how information from a time domain signal can propagate through the low resolution sampling. The figures used to illustrate the method are not scaled with reasonable parameters other than for illustration purpose. With this in mind, the relation between a modulated time domain signal and the sampled version can be explained by the following approach.

For transmission, amplitude and phase encoded baseband information is modulated onto a carrier frequency, presenting itself as the envelope of the carrier signal. An incoming phase and amplitude encoded analog signal has a constantly varying amplitude over time, revealing the information it holds. As an example of a signal modulated onto a carrier, the blue curve in figure 3 (a) illustrates part of a transmittable signal in time domain. Observing this figure, it is clear that the carrier wave has a constantly varying amplitude over time. A 1-bit quantization of such a signal will convert it into merely two levels, as illustrated by the red curve in figure 3 (b). It is important to understand here that since an ADC is a device enabling digital processing, the blue signal could be thought of a signal *before* sampling, or equivalently with a *high* resolution for comparison. The red signal is what will be seen in digital domain by the receiver central unit, subject to digital signal processing.

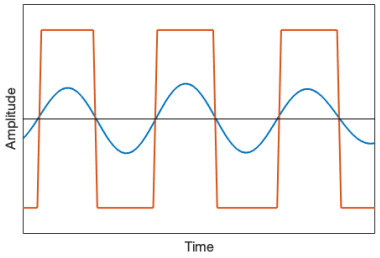
Since the information is present through amplitude variations in the analog signal, the quantization would intuitively seem to erase the signal content. However, under certain circumstances this proves to be quite wrong. Figure 3 (a,b) presents a noise-free signal, which is an ideal scenario that will never occur in an analog system, where additive noise is always present. When noise adds to a signal it will also affect the output after quantization, which is the key

to this approach. With additive noise, the analog signal will exhibit fluctuations as described by the blue curve in figure 3 (c). These fluctuations caused by noise will also produce high or low values in the quantization process, which can be depicted as a reproduction of noise in the output. Comparing figure 3 (b) and (c) the red curves show the differing outputs for the two cases, although the signal is the same. The only difference is the applied noise. Observing figure 3 (b) it becomes more clear that 1-bit quantization of a low-noise signal produces a digital signal similar to a clock sequence; forfeiting the signal information. In the right figure however, the noise produces flickering values. The flickers occur when the noise makes the signal sway about the *reference level*, deciding on the signal value being positive or negative. The more noise the signal contains, the higher signal amplitudes will be subject to a flickering output, making these flickers a depiction of the signal amplitude.

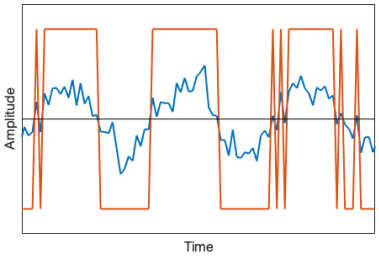
Noise flickering in the digital signal will depend on the signal amplitude; the lower the analog signal amplitude the larger impact the noise has in the quantization. When this relation is comprehended, it may be more obvious that the envelope of a signal, such as in figure 3 (a), will also affect the amount of quantized noise. With noise in the quantized signal as a measure of amplitude, signal information will propagate through the 1-bit quantization.



(a) A typical RF signal presenting the baseband data modulated onto a carrier frequency.



(b) A close-up on a modulated signal (blue), quantized into two levels (red).



(c) The same signal as in (b) but with additive noise.

Figure 3: An illustration of the noise dependence of 1-bit quantization, presenting input signals (blue) and their corresponding two-level version (red). Figure (a) illustrates what a modulated carrier may look like, aiming at the amplitude variations forming the envelope. The difference between (b) and (c) shows that noise on the input reproduces in the output, which is the key to demodulation of a 1-bit receiver.

The heart of this method is thus the reproduced noise, which is the key to demodulation. Comprehending the nature of the 1-bit quantization requires a new perspective, but may best be described by quantized noise as a measure of signal amplitude. To clarify, the noise reproduction in the digital signal is not measured or processed in any particular way, but this is rather a way to explain the propagation of information. With this in mind, the quantized signal can be seen as the footprint of an amplitude varying signal. To gain statistical reliability

to the method the signal is preferably highly oversampled. The higher the oversampling rate, the higher the resolution in time domain. When sampling at a high rate the statistical support for noise flickers (amplitude interpretation) then increases.

One question remains to enable control of this process: what is a good amount of noise? Considering the two extremes, a very high SNR would generate a digital signal similar to a clock sequence, and a very low SNR will drown the signal in noise. This simple analysis reveals that there must be a region or sweet-spot for which the SNR is optimum for decoding. In order to control the process in terms of noise reproduction, the method requires some type of SNR control. For this reason, the signal is preferably converted to a binary signal in a controlled analog environment before sampling at the 1-bit ADC. In this way the SNR propagation through the process can be observed and analyzed to ensure the correct signal is sampled.

3.3 SNR optimization

The SNR requirement on decoding capability calls for noise regulation prior to quantization, and consequently an analog implementation method. In a distributed MIMO system, an infinite number of antennas would mean an infinite SNR distribution among the received signals. In that case the system would theoretically always work, but this is of course not realistic. In purpose of studying the system from a single link, noise control is decisive. The analog solution for noise control is hence a decisive function for the entire system functionality.

A common error estimate of signal quantization is the *quantization error* denoting misreading of the signal value, e.g. the difference between the incoming signal and the quantized version. 1-bit quantization error means a high value is passed as a low or vice versa. These errors may be depicted as noise, founding the *quantization noise*, which often is correlated with the signal. Correlated noise is problematic in the sense that it may compromise the output, aggravating the ability to distinguish between noise and content. With the intention to randomize the quantization error, a *dither* signal can be added to the analog waveform before quantization [10]. The common entry to dithering is to introduce controlled random noise such that the misreadings become random and uncorrelated. In the proposed system topology, a wise choice of dither signal gives both the opportunity to correct the noise and make the quantization noise uncorrelated.

With the purpose of randomizing quantization noise, a dither signal is typically chosen as random noise. Although, for this specific system, there is nothing indicating this would be the optimum dither signal for the application purpose. In the proposed system topology for this project, the central unit is also used as a dither generator, which makes the choice of dither signal dependent on what signals the central unit can generate. Analog dithering is revisited in section 5.3.1, explaining the features of dither signal design.

Further, deployment of multiple RRH:s entails individual dithering at each link, since dithering must be applied prior to quantization. In a traditional wireless network a rule of thumb comprises high SNR, but this is no longer an impeccably accurate approach. The RRHs will in general receive signals with different SNR, where the one closest to the optimum SNR will make the dominant copy before dithering. As has been explained in section 3.2 the optimum SNR is not the highest. However, introducing dithering as a type of noise regulation, high SNR at reception is still preferable. Fundamentally because noise addition is far more applicable than noise reduction, to ensure operation at optimum conditions. The system presented in this report calls for a new perspective on the contemplation of power and noise. This insight prevails the project, and will be revisited repeatedly in according context.

4 Signal processing

Before moving on with the system design and studies of practical implementation, a first step is to verify the concept through simulations. In this way the proposed system can be observed in a controlled environment, giving further understanding of hardware requirements. Naturally following simulations is to move processes to analog domain and connect the results to theory. This chapter explains the construction and architecture of the digital signal processing used both for simulations and measurements. Results from simulations are presented in chapter 6, to closely serve as a comparison to analog measurements.

4.1 Structure

The digital signal processing described in this project is performed in MATLAB, and will here on be explained in chronological order; from transmitted bits to received bits. There are several ways to transmit a signal in terms of modulation technique, choice of carrier etc., which demands a motivated choice of digital system architecture prior to implementation. Firstly, a variable quadrature amplitude modulation (M-QAM) constellation is implemented, bringing flexibility in data rate for further tests. The modulation is explained in more detail later in this chapter. Secondly, one must consider the prevailing channel and what effect it has on the signal. A wide-band signal generally means the channel influence will be frequency dependent, aggravating channel estimation and equalization. A popular transmission technique to circumvent this is to use orthogonal frequency-division multiplexing (OFDM), which in comparison to single-carrier transmission uses a set of sub-carriers. Data is then divided between the sub-carriers, relaxing the symbol time, since less data is transmitted on each sub-channel. Orthogonality between sub-carriers means they are multiples of a fundamental frequency at baseband, which has some advantages. A key feature is that the sub-carriers can be transmitted simultaneously without interference, when perfectly orthogonal [11]. OFDM is robust towards inter-symbol interference (ISI) because of the relaxed symbol time, and since the fractional bandwidth typically is small each sub-channel can be presumed frequency flat [11]. A frequency flat channel means the channel is static within the fractional bandwidth. Figure 4 illustrates the implemented SIMO system from a digital signal processing (DSP) perspective, for which each step is explained in the sub-sections.

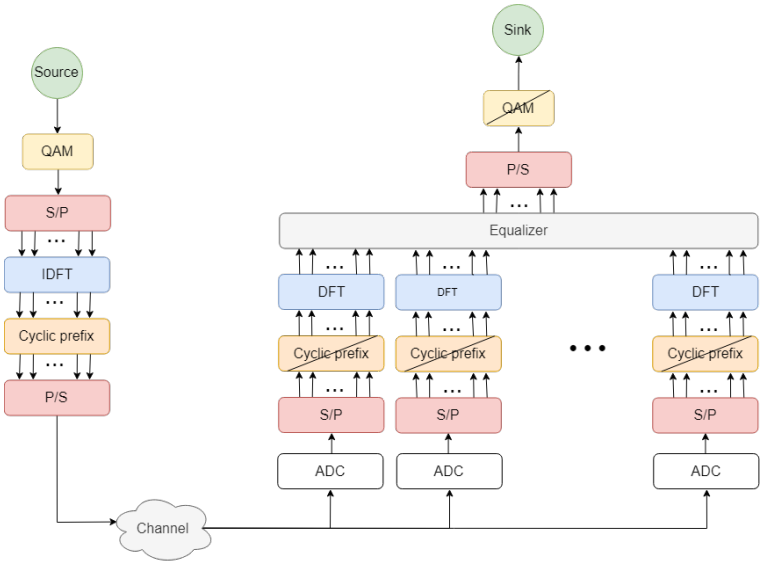


Figure 4: A block diagram describing the DSP structure for a single user and an arbitrary number of receiver antennas. A bit sequence is generated at the source, and at the sink the received information is again represented in bits. The yellow blocks present modulation/demodulation at a desired QAM map. Red blocks stand for serial/parallel conversion. Blue blocks stand for (Inverse) Discrete Fourier Transform. Cyclic prefix denotes padding/discarding of guard intervals. At the ADC blocks the 1-bit quantization is performed. The equalizer compensates for the channel and merges the received signals from multiple links.

4.2 Defining the user; signal construction

Starting with a series of bits at the source, the goal is to retrieve the same bits at the sink with a minimum loss of information. In purpose of system performance demonstration, the message for transmission is chosen as a random bit sequence of chosen length. To give bits a physical meaning in an efficient manner, they are translated into complex symbols. An M-QAM modulator defines a map of symbols, and what bits each symbol represents. The M denotes the number of symbols in the map, for which each symbol represents $\sqrt{M}$ bits. Complex symbols correspond to vectors, described by phase and amplitude. The technique is illustrated in figure 5, with In-phase (I) and Quadrature (Q) axes, presenting QPSK (4-QAM) modulation. Amplitude A and angle a defines the symbol vector. In general, the larger map of symbols used, the finer precision is needed to define them in analog domain.

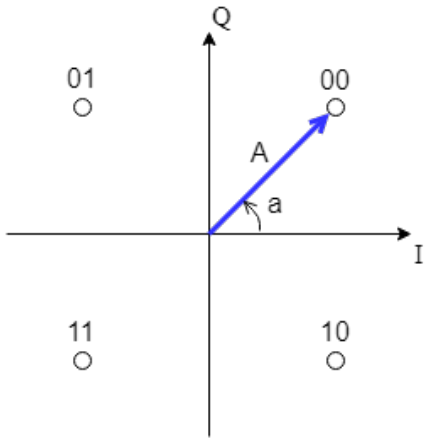


Figure 5: The modulation map for QPSK (4-QAM), presenting a symbol vector with amplitude A and angle a.

After modulation, the information is now contained in a vector of symbols. To create an OFDM signal, the symbols are divided into a number of parallel streams, i.e. the chosen number of *occupied* sub-carriers, to be processed separately. The occupied sub-carriers are hence those chosen to contain data. Assigning the number of occupied sub-carriers is a direct control of the total bandwidth, and hence depends on the system application. Bandwidth is related to sub-carriers as

$$\mathrm{BW} = \frac{F_{s,\mathrm{TX/RX}}}{N_{\mathrm{TX/RX}}} \cdot S, \tag{1}$$

where $F_{s,TX/RX}$ is the sample frequency at the transmitter or receiver, $N_{TX/RX}$ is the number of samples per OFDM symbol at respective side, and S is the number of occupied sub-carriers. Note that this sets a requirement on the sample rate at the transmitter (user) relative to the receiver, since the bandwidth is set at the transmitter. E.g. (1) shows that the ratio of sampling frequency and number of samples must be the same at both sides, since the number of sub-carriers is constant. At this stage the symbols are contained in the set of vectors defining the chosen signal bandwidth.

A common approach to get a signal to a transmittable frequency is to up-convert the signal in analog domain using mixers. In the pursuit of reducing analog system complexity, an alternative is to introduce *oversampling* in digital domain. The method implies an extension of the samples in frequency domain. The motivation of this method is explained by the property of the *Fourier transform*, giving one sample in time domain for each sample in frequency domain. Going back to the foundation of the Fourier series, the basic concept is that any signal shape can be created by a sufficient number of sinusoidal harmonics. An OFDM signal is constructed by a number of sub-carriers, creating some arbitrary shape when merged into an OFDM symbol. Consequently, the sub-carriers serve as the harmonics creating a signal shape through the Fourier transform. Adding harmonics (sub-carriers) will refine the signal shape; an increased number of frequency domain samples will increase the symbol resolution in time domain. In the reverse perspective it is intuitive that a larger set of samples in time domain will give a more accurately defined signal. Oversampling makes use of a larger set of sub-carriers in this case, but symbols are still only mapped to the chosen set of occupied ones.

Note that when the number of samples per OFDM symbol (N) in frequency domain increase, the frequency content will increase proportional to N, since the carriers are equally spaced when

using OFDM. This allows for placing the occupied carriers at higher frequencies, e.g. placing the symbols at higher frequencies. In this way it is possible to move the occupied sub-carriers up from baseband in digital domain. The limiting factor to how high in frequency the occupied sub-carriers can be placed is the sampling rate of the digital-to-analog converter (DAC), which determines the maximum output frequency. Even though the focus of this project is on the receiver, the reason for this note is the interest in system simplicity. In fact, for a sufficiently high sample rate DAC, the occupied carriers could be placed directly at carrier frequency, and additional up-conversion would not be needed. This method would eliminate the need of an analog up-conversion stage, which in practice generally contributes to frequency offset, higher order harmonics, etc. However, the method depends on the DAC being able to provide a sample rate of twice the carrier frequency and half of the signal bandwidth.

Since symbol mapping is performed in frequency domain, digital oversampling can be implemented by placing the symbols at the locations of the chosen sub-carriers in a zero matrix sized to the number of frequency samples. In this way only the a chosen sub-set contains information. An inverse discrete Fourier transform (IDFT) of the parallel streams gives a new set of complex vectors defining the symbols in time domain, defined by

$$x_n = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} \hat{x}_k e^{j\frac{2\pi nk}{N}}, \tag{2}$$

where N is the number of samples per symbol, k is the sub-carrier index and n is the sample index (i.e. the discrete time index). Mathematically the IDFT ensures orthogonality between the carriers, since the integer property of the indices guarantees multiples of a fundamental frequency. Furthermore, to ensure ISI robustness a *cyclic prefix* is placed in between the OFDM symbols, which is constructed by preceding each OFDM symbol with the tail end of itself. The prefix acts as a guard interval between the OFDM symbols and can be discarded at the receiver to retrieve the symbols with low ISI. After cyclic prefix padding, the parallel carriers of OFDM symbols are re-combined into a serial symbol stream, ready for transmission.

4.3 Channel influence

To have an idea of what the signal will look like at reception it is of utmost importance to know the channel it propagates through. During wireless transmission, a signal interacts with the environment, commonly through multipath propagation. This means the signal is partly or fully reflected by the surrounding environment before reaching the receiver. In general, the signal path length determines the attenuation of the signal; if it exists, the line-of-sight component will suffer least from attenuation. Accordingly, interaction with the environment will cause a delay spread between the shortest and longest propagation time.

A multipath channel is often frequency selective over a large bandwidth, because different frequencies generally interact differently with the surroundings. Since OFDM is used in this system the signal bandwidth is divided into a number of sub-channels assumed to be frequency flat, meaning that the channel is assumed constant over the fractional bandwidth. Never will this assumption be correct, but if sufficiently valid it vastly simplifies channel estimation. A model of the channel can be achieved by transmitting pilots constructed by a known set of data, where the difference between the original pilot and the received pilot reveals the channel.

4.4 The receiver; signal restoration

In principle the task of the receiver is to find the message and reverse the implementation of the transmitter and the channel. The ADC is the device sampling the signal, providing the digital samples that are processed according to the method described in this chapter. In the proposed system in this project, the 1-bit ADC described in section 3.2 provides a two-level signal in digital domain. The challenge presented to the receiver signal processing is to perform timing and frequency synchronization to an incoming signal and to estimate the channel influence, which is required for correct demodulation.

4.4.1 Detection and synchronization

The receiver is continuously listening to the channel, and needs a method to synchronize in time and frequency with an incoming signal. Two estimates are used in this matter, the symbol time offset (STO) and the carrier frequency offset (CFO). Perfect STO correction means the receiver is sampling at the exact right moment, in this case corresponding to a correctly placed N-point discrete Fourier transform (DFT) window. If the STO estimate has an offset, the received signal will exhibit a degree of ISI. CFO commonly originates from conversion oscillators, Doppler shift at the receiver [11] and sampling clock offsets. In this system no mixers are present, making the Doppler shift and clock offsets dominating the CFO. The reception of a wireless signal is generally very sensitive to CFO, and in an OFDM modulation the sub-carriers will also be subject to inter-carrier interference. Timing and frequency synchronization can be done by different methods, perhaps most intuitively by preceding the message with a known preamble that can be used for correction similar to a pilot. However, since a preamble will be subject to channel influence, the comparison to an unaffected copy would make the method itself highly sensitive to frequency offsets. The *Schmidl & Cox* algorithm [12] makes use of a periodic preamble, where the periodicity allows for detection through correlation with itself, and the result provides the timing and frequency offset estimates. In contrast to using a known preamble this method offers robustness to frequency offsets.

The correlation used for detection through the Schmidl & Cox algorithm is dependent on SNR, where a low SNR will generally reduce the correlation and aggravate the detection. The more noise reproduced in the quantization, the lower the correlation of the periodic preamble. In a distributed network the RRH with highest received SNR will be able to present the best signal detection, but will need the highest noise power for correction.

4.4.2 Channel estimation and demodulation

Upon signal detection a received signal y is a serial stream of samples in time domain, which is converted back into parallel streams for processing. The cyclic prefix serving as a guard interval for ISI has at reception served its purpose and may be discarded. A DFT converts the time domain samples back to frequency domain as follows:

$$\hat{y}_k = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} y_n e^{-j\frac{2\pi nk}{N}}. \tag{3}$$

$\hat{y}_k$ denotes the received samples at sub-carrier k in frequency domain and y_n is the corresponding time domain sample. At this stage the transmitted symbols $\hat{x}$ and the received symbols $\hat{y}$ differ by the channel frequency response $\hat{h}$ and noise $\hat{w}$ according to

$$\hat{y}_k = \text{sign}(\hat{h}_k \hat{x}_k + \hat{w}_k). \tag{4}$$

The *sign* operation here denotes the 1-bit quantization. Finding the best model of $\hat{x}$ requires a method for estimating $\hat{h}$. Approximating frequency flat channel responses for the sub-bands of an OFDM signal requires a channel estimate $\hat{h}$ for each sub-band, which are retrieved by preceding pilots. Mathematically the channel is estimated through the least squares method, minimizing the noise term for a sufficiently long pilot sequence. In intent of estimating the channel effect, $\hat{x}$ and $\hat{y}$ here represent the transmitted and received pilots, respectively.

$$\hat{h}^{\text{LS}} = \arg\min_{\hat{h}} ||\hat{h}\hat{\boldsymbol{x}} - \hat{\boldsymbol{y}}||_2 \tag{5}$$

In words, the least-squares estimate is the $\hat{h}^{\text{LS}}$ that minimizes the difference between $\hat{\boldsymbol{x}}$ and $\hat{\boldsymbol{y}}$ through the l2-norm, hence revealing the channel response. By solving (5) the minimizing $\hat{h}$ is found as:

$$\hat{h} = \frac{\hat{\boldsymbol{x}}^H \hat{\boldsymbol{y}}}{||\hat{\boldsymbol{x}}||^2}. \tag{6}$$

When the channel estimates are retrieved, equalization of the received signal is done through compensation with the achieved channel estimate. The distribution of multiple receiver RRHs demands as many channel estimations as there are RRHs, since all RRHs will experience different channels.

For an arbitrary number of RRHs the channel estimates and received signals can be combined through *zero forcing detection*. In comparison to other methods the zero forcing detection nulls the ISI through an inversion of the channel response, rather than optimizing the power through each channel [13]. The zero-forcing algorithm is defined by

$$\tilde{\hat{x}}_k = \frac{\hat{h}_k^H}{|\hat{h}_k|^2} \cdot \hat{y}_k, \tag{7}$$

where the channel weights $\hat{h}_k$ and received samples $\hat{y}_k$ denote content for sub-carrier k at all antennas. The resulting estimated samples $\tilde{\hat{x}}$ are finally converted back to a serial stream of symbols. According to the chosen algorithms the received symbols are at this point the estimation on what was originally transmitted. With ideal decoding the symbols would have the exact same phase and amplitude as the symbols in the QAM map they were modulated onto, but that will never occur in reality. The phase and amplitude values will have offsets, displaying a spread in the constellation diagram. The difference between the original symbol and the received symbol can be described by an *error vector*, denoting the amplitude- and phase difference, as seen in the following figure.

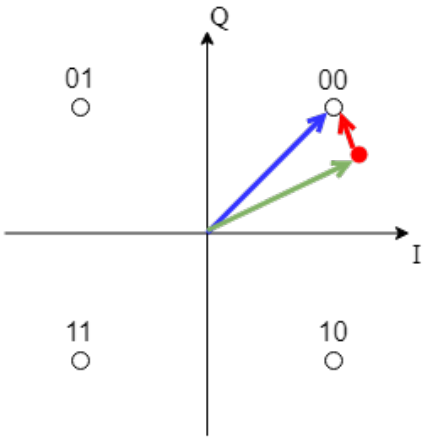


Figure 6: Illustration of the constellation at the receiver. A received symbol (red dot, green arrow) has an offset to the original symbol (blue arrow), denoted by the error vector (red arrow).

This error can be used as an estimation of the system performance, since it measures how close the estimation comes to the actual symbol. To get a pattern of bits at the sink the received symbols are mapped to the closest constellation points of the original constellation map. If a received symbol is mapped to a symbol different from what was originally encoded, bit errors will occur.

5 Hardware

After studying 1-bit receiver theory and the signal processing is defined, the next step is to find an actual implementation method. Regarding system competitivity, the key function in analog domain is the method used for noise correction, enabling decoding a signal when using a 1-bit ADC. Hence, the primary focus of hardware analysis is the method chosen for dithering. This chapter attends two different components regarding this; the comparator and the optical transceiver. An important aspect of the component is the behaviour of the output signal, to establish full control of the 1-bit ADC samples. The goal is to minimize the number of misreadings, introducing uncontrollable errors. A field-programmable gate array (FPGA) board will serve as central unit in the proposed design, and operate as a dither source, to control the noise during measurements.

5.1 The comparator

A comparator is a device that can be used to convert an RF waveform to a binary signal. In principle it compares an input signal voltage to a reference voltage, resulting in a *high* or *low* output depending on the relation between the two. The mathematical operation is described in equation 8. To circumvent the need of down-conversion the conversion rate of the comparator must be sufficiently high to operate at carrier frequency. Accordingly the carrier period time sets the requirement of rise- and fall time (t_R and t_F) of the comparator circuitry. The requirement is at a critical minimum $t_R + t_F < T/2$, such that complete pulses may be generated. Further, the reference voltage is what sets the logical level of the output signal, and must be chosen wisely. In purpose of pure conversion, the ideal reference would be the DC level of the incoming signal, to ensure equally probable output levels. However, the mathematical execution of the comparator enables output control through the reference

voltage, making studies of the reference quite interesting.

$$V_{\text{out}} = \begin{cases} \text{high}, & V_{\text{in}} > V_{\text{ref}} \\ \text{low}, & V_{\text{in}} < V_{\text{ref}} \end{cases} \tag{8}$$

Since the function of a 1-bit receiver is depending on the SNR of the signal, a decisive feature of hardware choice is to enable regulation of noise. A controllable amount of noise must be applied to the signal upon quantization, but there is no restrictive method of how. To rephrase, the requirement is rather that there must be a reproduced noise dependent on the amplitude of the signal, after quantization. In this regard the comparator operation gives the opportunity to control the output. Applying a controlled dither signal as reference will cause reproduction of that signal in the output, making the comparator fully capable to apply dithering. To achieve a controlled process it is still of high importance that the input signal voltage and the reference have the same average voltage level, such that it is equally probable to generate a high or a low output. An offset between the two would compromise the output, and imperil the reliability of the demodulation.

5.1.1 A high speed test device

For the purpose of studying analog dithering the comparator [14] in figure 7 was chosen, providing 9.3 GHz operating bandwidth and high phase preservation. The component has a combined rise- and fall time of $t_R + t_F = 40$ ps, theoretically enabling a maximum operating frequency of 25 GHz, providing a good margin for the application. Optimizing the employment of the comparator requires understanding of its functions, and their impact on the signal. For the chosen component, the reference signal and *latching* offers output control, making the decisive control signals.

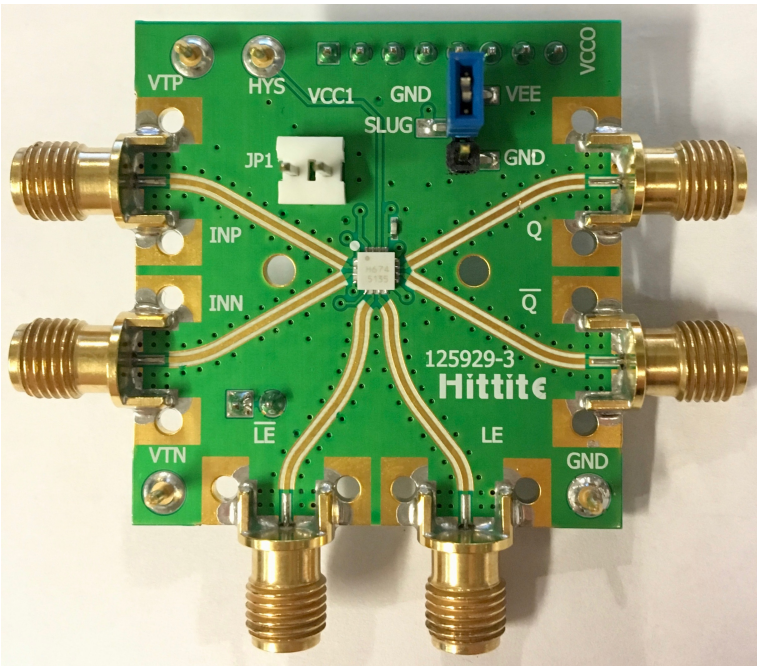


Figure 7: Comparator HMC674LC3C [14]

As seen in figure 7 the component offers six ports; differential inputs, inverting and non-

inverting output, and two ports for latch control. A latch is a logic circuit, enabling time controlled output pulses. The latch mode is also called "hold" mode, meaning the logical level of the input comparison is held just before the latch enable ($LE - LE_{bar}$) is going high. Apart from latch mode, the comparator can also operate in transparent mode. In that case the latch-enable ports are left floating, making the output continuously follow the logical value of the input comparison. Accordingly the output will continuously react to the mathematical execution. Because of the continuous tracking this method is more power consuming than the alternative [15], and during tests proved to generate an unstable output. Operating in latch mode the control signal in practice makes the component output sampled. According to the Nyquist sampling theorem the latch lock frequency (e.g. the sampling frequency of the comparator) must be at least double the carrier frequency, since the latch enable only goes high once per period. Choosing a clock rate marginally higher than what is required will ensure oversampling, profitable to sampling the signal correctly.

During operation the inverting output is terminated to 50 Ohm, and the latch is fed with a 2.5 GHz clock. The signal is applied to the INP-port, and the reference to INN. Operating conditions requires input voltages from -2 to 2 V, hence the reference signal can be shifted to the same level by a DC block to minimize any offset between the two.

5.2 Optical fiber and SFP+ transceivers

In the former project regarding downlink realization [1], [2] the conventional enhanced small form-factor pluggable (SFP+) optical transceiver [16] was used for electrical/optical conversion. Supporting 10 Gbps data rate it is a sufficiently high speed component also for the uplink realization. The SFP+ units are equipped with a 850 nm vertical-cavity surface-emitting laser (VCSEL), appropriate for short distance fiber transmissions. In addition it also provides internal quantization, ensuring a binary output signal. Since the SFP+ is a component with several integrated functions, the comparator [14] serve as a reference to confirm the logical execution and result. Amplification and quantization is located at the receiver section of the SFP+, ensuring a binary output at both ends.

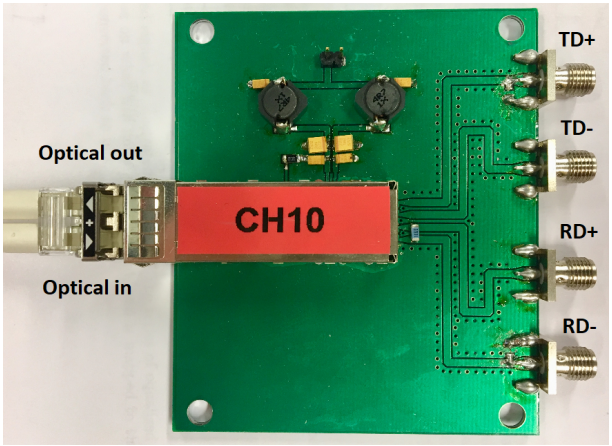


Figure 8: The SFP+ mounted on an evaluation board offering differential input and output. TD+/- represent the differential inputs and stands for Transmit Data. RD+/- similarly stands for Receive Data. Optical in/out represent the optical interface.

Providing differential input ports, mathematically the overall function of the SFP+ is a subtraction of the two inputs, followed by quantization. Denoting the transmit data TD^+ and TD^-, the receive data RD can be declared as

$$\mathrm{RD} = \mathrm{sign}(\mathrm{TD}^{+} - \mathrm{TD}^{-}), \tag{9}$$

rendering the function of the transparent comparator. The entirety of the device makes it advantageous for a demonstration of 1-bit over fiber transmission, since it offers joint quantization and optical interface.

A 30 meter long OM4 multi-mode fiber is used to merge with the SFP+ transceiver, where multi-mode fibers have a more robust connection to the source than single-mode, due to a larger core. The OM4 is generally low cost and is effective at short distances, since modal dispersion is limiting the propagation distance.

5.3 The FPGA as central unit

A field programmable gate array (FPGA) is, as the name indicates, a programmable integrated circuit enabling customized operations and applications. For this project the *Intel® Stratix® V GT Transceiver Signal Integrity (SI) Development Kit* [17] is used, offering an integrated FPGA mounted on an evaluation board. For convenience the complete unit is hereafter referred to as the FPGA. Providing full-duplex 12.5 Gbps transceiver channels routed to SMA connectors, it makes a good candidate as a central unit for the demonstration of a multi-channel receiver. In purpose of 1-bit quantization, the FPGA offers digital ports. The dual high-speed channels enable synchronized outputs, which can be used to provide a dither signal to use as reference in the conversion process. The bit transmitters are during operation continuously generating 5 Gbps signals of a customized bit pattern, which is used as the receiver response to add a dither signal to the process. Using the FPGA as a dither source requires further motivation and studies of the FPGA output, since it is a key feature to the proposed system. Description of the dither signal construction and its characteristics is presented in the following sub-section.

5.3.1 Dithering as binary noise control

As emphasized in section 3.2, optimal signal restoration requires optimal SNR, demanding a solution for noise control. An intuitive solution could be to adjust the transmit signal power, but such a solution would in practice require a feedback loop between the central unit and the user, seemingly inefficient. Applying a controlled dither signal at the receiver is more resource efficient, and requires no further response from the user. For this reason dithering at the receiver is an essential constituent in the proposed system. Dithering is fundamentally defined by adding noise to a signal prior to quantization, which is the requirement for analog implementation. This chapter describes the proposed method of dithering and the signal used in both simulations and measurements.

The dither signal will be applied at the differential input of the comparator/SFP+ as a reference, and the output binary signal will be a result of the difference between the input and dither. Both the comparator and the optical transceiver provide the mathematical execution to apply dithering according to (8) and (9). A random signal used as dither will appear as random binary values at the output, essentially providing output characteristics such as in figure 3 (c). In an ideal scenario the central unit would respond with an adjustable dither signal for correction, but the idea can be demonstrated by applying a stationary dither source in a controlled environment.

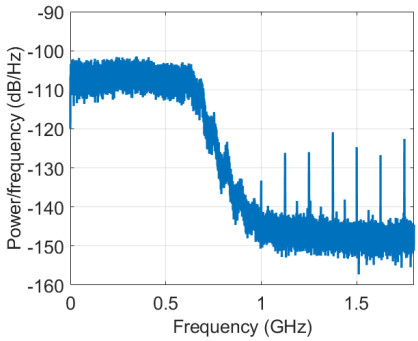
When mentioning SNR, it denotes the signal-to-noise ratio of the received signal at the RRH prior to dithering. In a realistic scenario there will be no SNR correction from the user, making the SNR of the received signal at each RRH stationary at the moment of reception. For this

reason the *Signal-to-Dither Ratio* is introduced, further denoted *SDR* (not to be confused with the common Signal-to-Distortion Ratio). This ratio describes the ratio between the received signal power and dither power. An important aspect to understand is that the signal already contains noise when dither is applied, since the received signal will have a certain SNR at reception. Since the SDR is the adjustable parameter, it makes the decisive factor for accurate decoding.

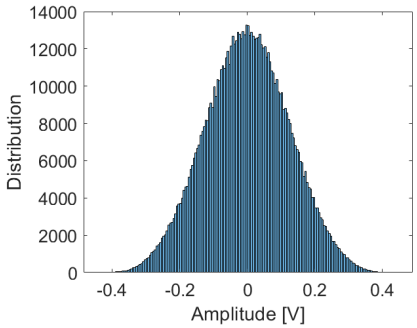
Further, choosing a dither signal may seem trivial at first, since random noise is commonly known to also randomize the quantization error, but will it provide the optimum reception conditions? The reference signal can in practice be arbitrarily chosen, making the study of dither signal optimization an extensive process. To grasp the functionality of the system a random sequence may serve as a reference to what can be achieved in terms of system capacity. According to the 1-bit quantization theory, random noise is capable to perform the necessary operation. The properties of a Gaussian amplitude distribution opens up for analysis, motivating system demonstration with a random Gaussian sequence for dithering. However, optimal dithering would provide gain in system performance, making the topic interesting for further research.

Using MATLAB to control the measurement environment, it is also used to provide the FPGA with a random bit stream. The built-in MATLAB function *randi* is used to generate a random binary pattern, providing uniformly distributed pseudo-random integers. The randomness of the bit stream is also something that can be affecting the performance of the dither signal, but this is left for further studies. According to the FPGA limitations, 240 000 bits was used as dither sequence, continuously transmitted on repeat from the FPGA. Due to a limited number of transmittable symbols by the lab equipment, the dither signal duration is still longer than the message sent.

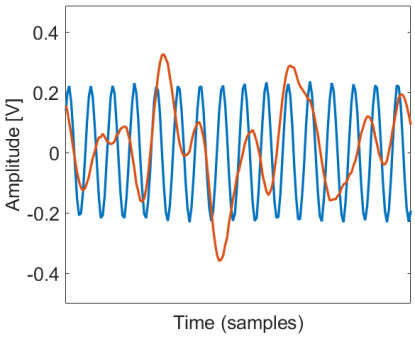
When using the FPGA as a dither source, one has to work with digital signals, in analog domain a binary sequence. A two-level signal can mathematically be described by the Fourier series; a sum of sinusoidal harmonics. The rich frequency content enables creation of other shapes using filters, allowing for an imitation of a Gaussian distributed random noise using a low-pass filter. When designing the dither sequence, one important aspect is the FPGA sample rate relative to the carrier; if the dither is relatively slowly varying the random nature will reduce in between samples. According to hardware restrictions described in section 6.1, measurements are made at a carrier frequency of 900 MHz. To generate a fast enough dither but not interfere with the signal itself, the low-pass filter was chosen as a 580 MHz LPF. Consequently, the highest frequency component of the dither will be in the order of 580 MHz, providing a margin to the carrier but still considered ”fast enough”. For the purpose a random binary sequence at 5 Gbps generated by the FPGA has the following characteristics after filtering.



(a) Power spectral density



(b) Amplitude distribution



(c) Signal and dither caption

Figure 9: A 5 Gbps random binary sequence generated by the FPGA presents the pictured characteristics after filtered with a 580 MHz LPF. Frequency spectrum (a) illustrates the characteristics of the filter, (b) presents the Gaussian amplitude distribution and (c) presents a close-up capture of an OFDM signal (blue) and the dither signal (red).

As depicted, the dither sequence is slower than the carrier frequency according to figure 9 (c), but has a very low power at 900 MHz. Figure 9 (b) presents Gaussian distributed amplitudes, and is considered a good enough random model for simulations and measurements for demonstration.

6 System realization and results

In purpose of proving the concept as well as monitoring component behaviour, hardware performance has been tested in a a lab environment. The approach is to bring validity to measurement results through comparison with simulation results, performing the same executions but in digital domain.

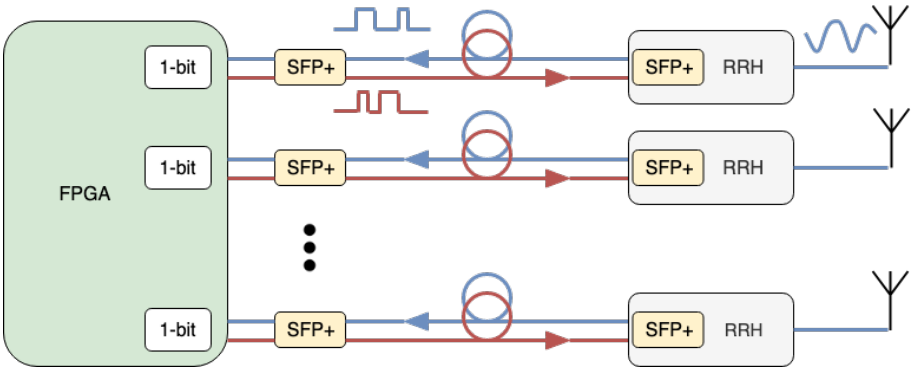


Figure 10: The proposed system design for an arbitrary number of remote radio heads (RRH), using the dual channels of the FPGA transceiver for reception (blue) and dithering (red) at each link. Electrical/optical conversion and quantization is performed at the receiver side of each SFP+ transceiver.

Figure 10 presents the proposed layout for a multi-antenna receiver testbed, with the FPGA serving as central unit. The duality of the FPGA and SFP+ units is used to transmit a binary signal from the FPGA over fiber, to use as dither at the RRH. The dither must be shaped at the RRH since the SFP+ has a binary output signal, and the amplitude variations of the dither is of utmost importance. Regardless of the desired dither properties, with the proposed system the shaping must be performed at the RRH, making it a critical constituent of the RRH design.

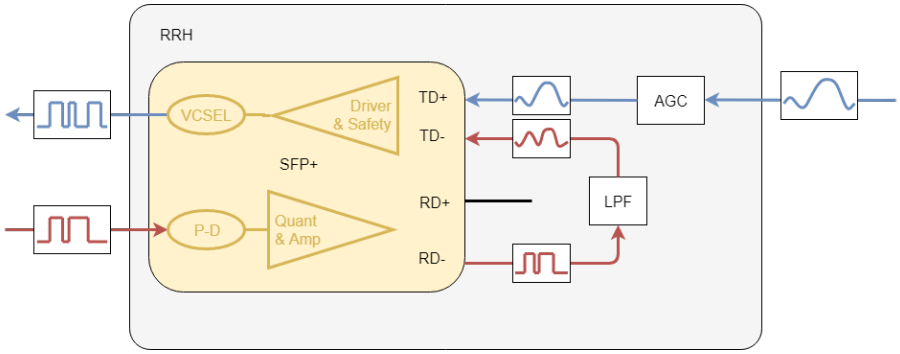


Figure 11: A conceptual illustration of the RRH with an integrated SFP+ transceiver. The SFP+ presents four ports; differential inputs (TD+/-) for transmit data and differential outputs (RD+/-) for receive data. The transmit side of the SFP+ is equipped with laser driver and safety circuitry and a VCSEL, and the receive side with a photo detector, quantization and amplification. Presented as the red link is the incoming binary signal from the FPGA that is shaped as the dither through the LPF. AGC stands for automatic gain control, responsible to regulate the power of the received RF signal to ensure the SFP+ input is driven at sufficient amplitude levels.

According to figure 11, a binary signal from the FPGA (red) is transmitted over fiber, received at the optical interface of the SFP+ at the RRH. This is the dither signal. The receiver side of the SFP+ is equipped with a photo-detector and internal amplification and quantization. For this reason the receive data is also a binary sequence. In the case of a Gaussian distributed dither the binary dither sequence is shaped through the LPF. After filtering, the dither is connected to the inverting input of the SFP+ to dither the signal as a reference. To make the SFP+ operate at optimum conditions the differential input must be assured to operate at proper voltage levels. Since there is no way to ensure the power of the received signal, an automatic gain control (AGC) is proposed to regulate the incoming signal, adjusting it to the

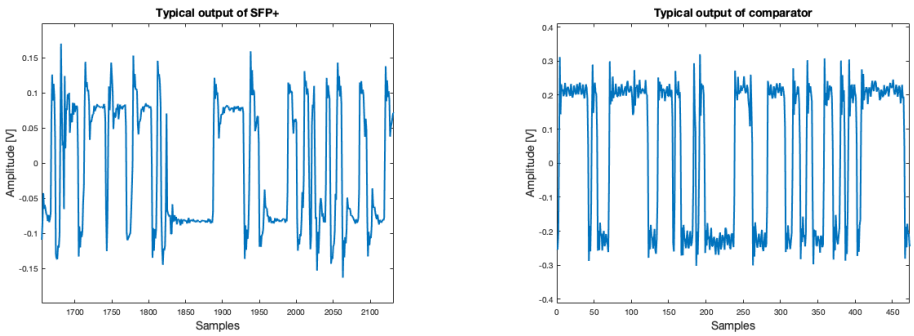
required input of the SFP+.

Due to the scope of the project, system measurements are not performed with the proposed system layout in figure 10, but in a test environment imitating the same functionality. First of all, the RRH PCB is not constructed, in purpose to rather study the realizability of a 1-bit receiver. To easily control the received signal power the wireless channel is replaced by cable, evading the AGC. SFP+ optical transceivers are well proven to operate with binary input, hence the dither is applied directly at the differential input to reduce all factors aggravating the study of the quantization process. The FPGA is only implemented as a dither source and is not finalized as a complete receiver.

The system performance is evaluated through the mean squared error (MSE) of the received symbols, chosen as a figure of merit. It is profitable to bit-error rate in the sense that the BER will be zero as long as all symbols are correctly mapped, but the MSE will always serve as a quality measure. MSE is defined as the mean value of the squared symbol error, and is presented in dB. To control the SDR at reception a constant dither power has been applied to the reference/inverting port, enabling sweeps of signal transmit power to find the optimal relation for reception.

6.1 Measurement layout

During all measurements the oscilloscope Agilent 54854A DSO [18] is used to capture the signal in time domain, offering a maximum sample rate of 20 GS/s and a 4 GHz analog bandwidth. With a finite number of samples in each signal capture this instrument is the bottleneck at measurements, limiting the number of symbols at each transmission. A maximum number of 1 025 000 samples in each capture makes the limit of the number of symbols for each transmission. Further, the bandwidth of the instrument restricts the carrier frequency during tests. A carrier frequency of 900 MHz was chosen to have a margin on the oscilloscope bandwidth. If the carrier is chosen too high, the carrier will be the only component seen by the oscilloscope, and the output will be sinusoidal. Lowering the carrier, square pulses will be observed, since higher order components will pass the oscilloscope bandwidth. At 900 MHz carrier frequency a binary output signal can be observed from the two devices tested, exhibiting characteristics as in figure 12.



(a) SFP+ **(b)** Comparator

Figure 12: Typical binary output characteristics from the SFP+ and the comparator.

One important aspect here, is that the sampled signal in the preceding figure has not been subject to 1-bit quantization. Since the oscilloscope captures the signal amplitudes at a rather fine resolution, it is in fact acting as a high resolution ADC. To justify the oscilloscope as a 1-bit receiver, the sampled signals will be enforced to 1-bit representation in post processing.

Observing the output in the figure, it is clear that the SFP+ exhibits a pronounced transient before settling at each level, and the comparator is more stable. If the transient oscillation is too vigorous, at times it will introduce additional noise. In post processing the sampled signal is 1-bit quantized by simply taking the *sign* of the signal presented by the oscilloscope. As long as the transient induced noise is sufficiently small, it will have a negligible effect on the system performance. If the transients however cross the zero-level, errors will occur. The sample rate used is 10 GS/s, the same as the proposed rate of the FPGA. A vector signal generator Agilent E4438C [19] is acting as the user equipment, and the dither signal is generated by the FPGA according to the description in section 5.3.1. Figure 13 illustrates the setup in the lab.

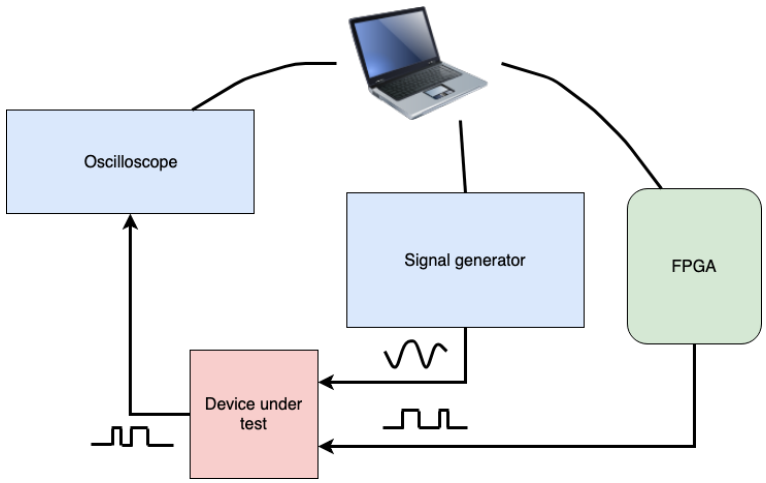


Figure 13: Measurement layout used when testing the comparator and SFP+. The signal generator is providing an OFDM signal, the FPGA is generating a random binary signal for dithering and the oscilloscope is sampling the output from the device.

6.2 SISO demonstration

Primarily the focus for measurements is to demonstrate the performance of a single link and compare the results to simulations. The performance of a single link will indicate the functionality of the method, and further motivate the functionality of a multi-antenna system. Measurements and simulations are only presented for QPSK modulation since the number of transmittable symbols are strictly limited to the instrument setup. For a higher order modulation the results would have a very low statistical support, requiring the FPGA to be implemented as a receiver.

6.2.1 Simulations and parameters

The theoretical system model using a simulated channel is the fundamental reference to the measurement results in analog domain, displaying the expected system behaviour. A simulated channel with known signal influence enables studies of isolating system parameter influence, as well as validating the system performance. What is important to emphasize about the results is that they are not general for this type of system. The results are highly dependent on the parameters set, and particularly the choice of dither signal. The results presented, i.e. figure 14, do not present optimum system performance, but rather what can theoretically be achieved with the specific settings and choice of dither.

Testing this type of system requires some motivation to specify all variable parameters. To

begin with, the dither signal used in simulations is implemented as the same dither used during measurements. Generated by the FPGA, a random bit sequence is filtered by a 580 MHz low-pass filter and sampled by the oscilloscope, possessing the characteristics presented in section 5.3.1. Using the same dither sequence in simulations and measurements warrants comparison to measurements more than a simulated dither, that could generate a different behaviour. Since single-link measurements are performed over cable, the channel during simulations is modelled as additive white Gaussian noise. The sample rate at the receiver is 10 GS/s for all simulations and measurements, and the signal is OFDM modulated.

Regarding the signal bandwidth and reception quality, figure 14 presents simulation results sweeping the signal power for a constant channel noise and dither power, at different signal bandwidths. The only parameter swept is thus the signal power. A sweep of signal power facilitates comparison with measurements, where the transmit signal power from the signal generator enables similar sweeps.

Observing figure 14, the prediction of a sweet-spot in signal to noise is confirmed. At this region the dither and the noise in the signal have together generated the sufficient amount of noise present in the 1-bit quantized signal. Over the entire sweep two extremes can be seen, one at low signal power and one at high signal power. At low signal power the dither and noise is dominating, erasing the signal. The result is a high MSE, corresponding to a large spread in the constellation diagram. As emphasized in section 3.2, the quantized signal at low noise is similar to a clock, forfeiting the signal information. Although, at high signal power the MSE is leveling out at about -10 dB. This is explained by the fact that a dither is applied to the process, such that although the SNR is high, noise is introduced through the dither.

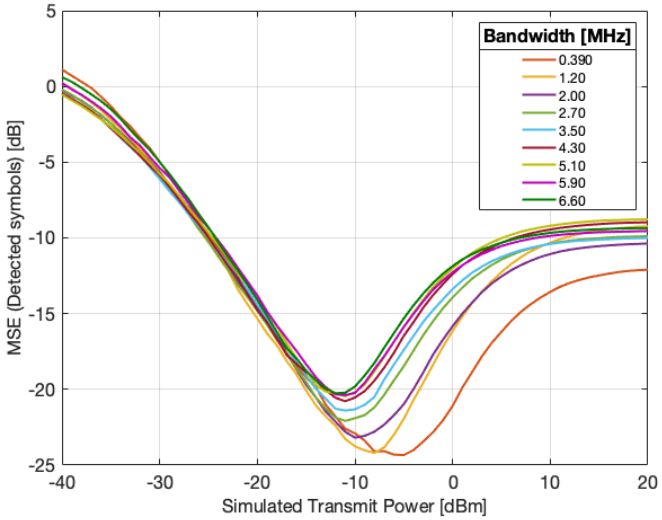


Figure 14: Achieved MSE of detected symbols from simulations, presenting a sweep over simulated transmit power for a constant noise and dither power. The different lines represent different signal bandwidths.

Further, the results show that received symbol MSE improves for a lower bandwidth. In OFDM modulation the bandwidth is proportional to the number of occupied sub-carriers, defining the frequency content of the signal envelope, e.g. the signal content. A larger bandwidth means the envelope can be shaped by more frequency components. In other words, a larger bandwidth would require a larger number of samples to achieve the same oversampling rate, refining the resolution. This explains the degradation of MSE at a larger bandwidth seen in figure 14. Choosing the operating bandwidth depends on the application and is a trade-off of a number

of features, such as hardware, MSE, SDR, data rate, ISI, etc.

The relation between MSE and oversampling rate implies that the MSE could be improved by simply increasing the oversampling rate, e.g. the sample rate of the ADC at the receiver. A decisive aspect of this is to consider the dither signal, which is producing noise in the sampled signal. If the noise generated by the dither is random in between samples, increasing the oversampling rate would improve the performance. However, the dither signal is also limited in frequency. In the specific dither design, it is slower than the signal itself. Although the dither is generated as a random sequence, it will in a sense not be random in between samples due to its rate of change. This fact makes one aspect of why dither signal design is a promising research area regarding improving the system capacity.

For demonstration a bandwidth of 2 MHz was chosen for measurements. Sampling at the rate of 10 GS/s, it is 11 times higher than the highest frequency component of the signal. The Nyquist rate is two times the highest frequency component of the signal, making the oversampling rate 5.5 at the particular settings. The number of transmitted symbols are, due to all set parameters and limitations, 36 in total. This makes 3 OFDM symbols for the 12 sub-carriers creating a 2 MHz bandwidth. For the measurements the data rate is then 4.5 Mbps for demonstration. No efforts have been made to increase the data rate at this project development stage. The minimum MSE at this bandwidth and the specific dither signal is according to the figure -23.2 dB. To get a better picture of the performance of the particular system settings, an infinite resolution ADC serve as the fundamental reference. At infinite resolution the MSE at the sweet-spot conditions is -38 dB. This is the theoretical best MSE that can be achieved with the digital signal processing design. The maximum capacity of the 1-bit receiver is unknown at this stage, since many aspects need further studies.

To get a depiction of SDR ratio, a simulation of different dither powers is presented in figure 15. The results show that an increased dither power requires a higher transmit power (SNR) to reach the optimum MSE. This behaviour is expected, as a higher SNR requires a larger noise correction, everything according to 1-bit receiver theory. This insight provides the scaling behaviour for dither adjustment in actual measurements.

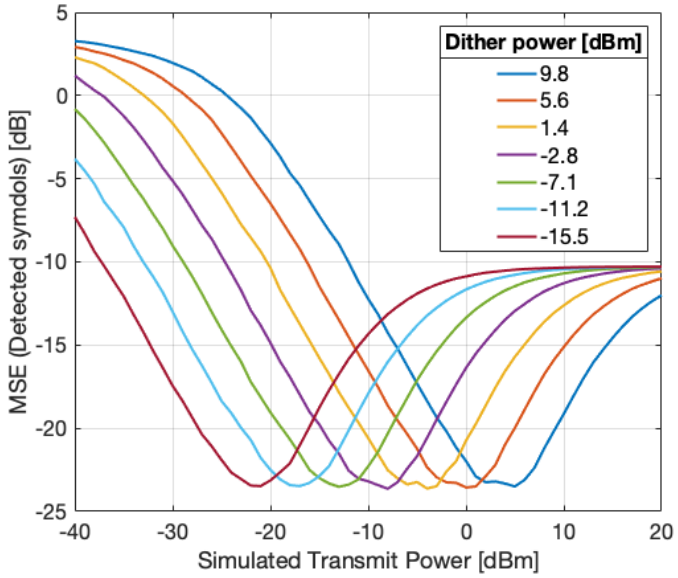


Figure 15: Achieved MSE of detected symbols from simulations, presenting a sweep over simulated transmit power for a constant noise and dither power in each individual simulation. Different lines represent different applied dither signal powers.

The optimum SDR is primarily dependent on the SNR of the received signal, since it is the total quantized noise that matters. Simulated dither powers in the figure are equally spaced with 4.2 dB, creating the same shift between the curves. This demonstrates the balance between signal power, noise power and dither power. To get a better picture of the power ratios, lets take a closer look at the purple curve in figure 15. A transmit power of -8 dBm appear to generate the optimum conditions, for which the SNR is found as 25 dB, and the SDR as -5.8 dB. First of all, from the SNR versus SDR, it is clear that the dither is dominating the total noise. Secondly, it appears that the SDR is negative for the particular dither. The fact that the dither power is higher than the signal power is highly dependent on the designed dither. Another dither design would most certainly generate a different result. Within the dynamic range of the measurement equipment, the optimum MSE can theoretically appear anywhere in the operating power region by adjusting the signal- and dither power. Accordingly, the dither power for measurements is adjusted to minimize the MSE in the middle of the dynamic range of the equipment.

6.2.2 Comparator results

In purpose of understanding the different devices used for dithering, a comparison between two components designated for the same task provides understanding of the output signal composition. The comparator function described in section 5.1, using the parameters found through simulations, provides the following results. Figure 16 illustrates a sweep over actual transmit power during measurements, using a dither signal average power at -5 dBm. Minimum achieved symbol MSE appear at a transmit in-band average power of -9 dBm, for which the power received by the comparator is approximately -8 dBm due to cable losses etc. This renders an SDR of -4 dB at the specific measurement. From simulations this implies that the operating SNR is in the same range as during simulations.

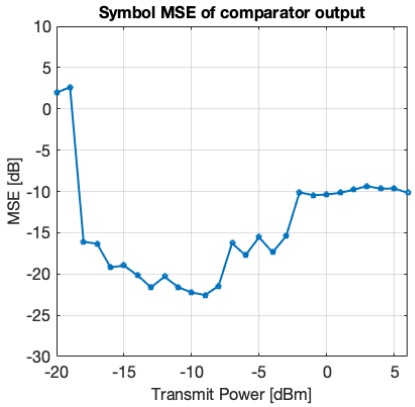
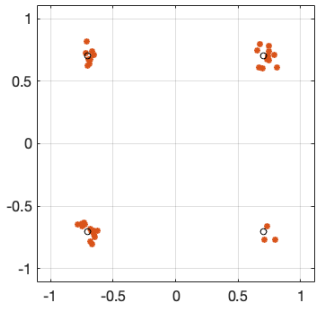


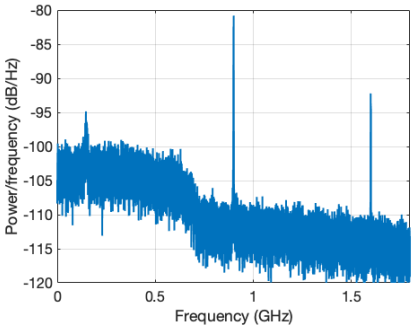
Figure 16: Achieved MSE of comparator [14] during tests, presenting a sweep over transmitted in-band power.

As figure 16 demonstrates, there is a clear region for which the dithered signal exhibit symbol MSE similar to simulation results. The minimum MSE obtained is -22.6 dB, that is 1 dB higher than simulated minimum. Similar to simulations the MSE is leveling out at -10 dB for high transmit powers. At low signal power there is a drastic increase in MSE, which may be explained by several factors. At low signal powers the noise drowns the signal, which is expected, but in analog domain there are other factors present as well. Possibly the rapid increase in MSE depends on the hardware sensitivity not being able to detect the signal at such low power levels. In a comparison between figure 16 and 15, the overall shape of the comparator output is similar to the theoretical curve, but at a smaller range of transmit

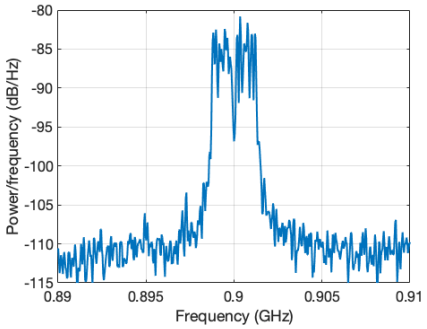
power. An important difference between simulations and measurements is that in simulations the channel noise is kept constant, but at measurements this can not be ensured. If the noise during measurements is dynamically changing with the operating power of the hardware, the range scale on the x-axis will be different. The overall jagged appearance of the curve is largely due to the limited amount of transmitted symbols used for each MSE calculation, but may also be affected by other system features. Figure 17 presents the constellation diagram and the spectrum for a transmission at minimum MSE.



(a) Constellation



(b) Frequency spectrum



(c) Close-up on frequency spectrum

Figure 17: Constellation diagram for transmission at minimum symbol MSE of -22.5 dB (a) and frequency spectrum of the corresponding received signal (b), presenting a close-up in (c) .

The constellation reveals the bottleneck to statistically supported results; the limited number of transmittable symbols due to the measurement equipment. Although, the results shall not be underestimated since repeated measurements provide similar results. What can be read from the frequency spectrum is that the dither signal design is profitable in the sense that the spectrum is clear at the carrier frequency. Apart from the signal itself, the spectrum in (b) shows two peaks within the interval, equally spaced from the signal. They prove to be the result of aliasing and harmonics, but do not disturb the signal at the carrier.

6.2.3 SFP+ results

Including the optical link, the SFP+ ought to generate similar results to the comparator, considering the logical task is essentially the same. According to figure 12, the behaviour of the output binary signal of the components differ. If the transients of the SFP+ pulses are inducing additional noise, it is a probable source to differences in measurement results. Power levels for dither and transmitted signal are equal to the comparator measurements. Figure 18 presents the received MSE. In the upper region of transmit power the curve is settling at -10

dB MSE, same as for the comparator and simulations. In the lower region there is again a rapid deterioration. Minimum MSE of -25 dB is achieved at -8 dBm transmit power, rendering the constellation in figure 19.

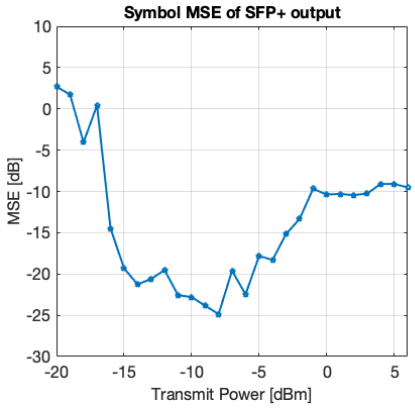
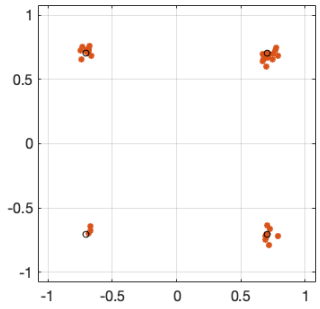


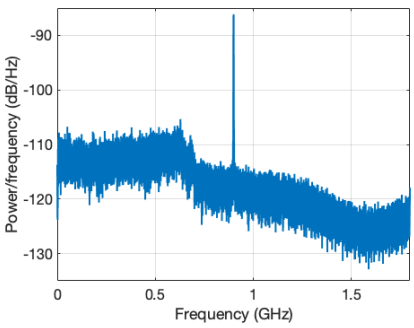
Figure 18: Achieved MSE of SFP+ [16], sweep over transmit power.

Firstly, the overall shape of the achieved MSE is similar to the theoretical model in displaying a maximum MSE at the lower interval above 0 dB and in the higher interval settling at -10 dB. Similar to the comparator, figure 18 presents the entire range in MSE as in figure 15, but over a much shorter interval. The SFP+ input range span an interval $[-0.3, 3.8]$ V, and the measurement transmit power generates peak-to-peak voltages $[0.063, 1.3]$ V, at the lowest making 1.5% of the operating interval. Two aspects are of importance to validating the comparison to theory; the sensitivity of the component and the system noise. If the component is provided too low input voltage, the output would be a pure quantized dither signal, since that power is constant. The output MSE would hence drop drastically when the voltage passes the threshold. Regarding the noise, a dynamic system noise would change the shape of the curve. Depending on the system that is measured, the shape will in a sense be characteristic to the device.

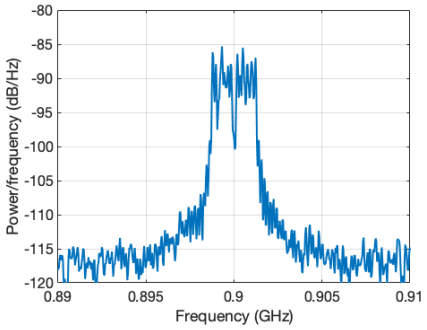
Further, some of the measurements actually give a better result than those presented from simulations. Many factors may be causing this behaviour, such as the quantization process or any fluctuations in noise or signal powers, but the most probable source is the limited number of transmitted symbols. The statistical distribution is again illustrated through the constellation.



(a) Constellation



(b) Frequency spectrum



(c) Close-up on frequency spectrum

Figure 19: Constellation diagram for transmission at minimum symbol MSE of -25 dB (a) and frequency spectrum of the corresponding received signal (b), presenting a close-up in (c) .

Figure 19 shows the spectrum of the received quantized signal for the optimum measurement at -25 dB MSE. At the lower frequency range the raised noise floor appear to be the result of the dither signal. Unlike the spectrum of the comparator there are no aliasing components or harmonics present in the visible region.

7 Discussion and conclusion

Regarding the tests that have been made, the proposed system is promising regarding the construction of a complete and functional testbed. The dither methods tested exhibit similar performance to that achieved in simulations. From the measurement results it is hard to motivate the exact conditions for optimum decoding, since the number of receivable symbols is strictly limited. Although, the results provide sufficient information to narrow down the conditions to ensure operation close to optimum.

Concerning the proposed design, dithering through the dual optical link provides a flexible implementation, reducing system complexity. One of the great challenges for implementation is to ensure operation at optimum MSE, since there are three fundamental powers affecting the output. For test purposes however, the proposed system would operate in a controlled environment and can still provide valuable insights without being flexible enough to cover all realistic scenarios. Still, the proposed AGC at the RRH requires further studies for motivation of the design.

As has been shown, the behaviour of the binary signal output of the dither component is decisive for receiver functionality. In this case the nature of the binary signal prove to be good enough

to demonstrate single link performance. However, the limited bandwidth of the oscilloscope used for signal capture restricts the resolution of the binary signal, and an instrument with higher capacity may reveal a different behaviour than displayed in figure 12. In this regard, a 1-bit ADC receiver as in the proposed design may benefit the reception, directly quantizing the analog binary signal into two levels.

7.1 Future work

The system proposed in this project has some advantages, but also brings several challenges demanding a new perspective on signal reception. There are many aspects that make interesting research topics, not least the study of dither signals. An imitation of Gaussian distributed random noise as dither sequence served as a foundation for system performance demonstration, but may theoretically be arbitrarily designed. Previous publications such as [4] show that the reference signal can be implemented in numerous ways, profited by post-processing. The main argument for a random sequence at this stage is the simplicity in implementation.

Future implementation of the FPGA as central unit would vastly extend the performance in terms of message length, number of ports, and not to mention the profit of using actual 1-bit ADCs for sampling. A first step to achieve a reliable model to connect to theory would be to implement the FPGA as receiver and further study the single-link performance using the SFP+ units as quantizers. To create a full link the design of a customized PCB, integrating circuitry for dithering and reception, would finalize a single link design. The number of ports available on the FPGA would then be the limit of the system extension in terms of RRHs.

Customized PCB design is in itself relatively simple, but a challenge for implementation is to control the signal power and dithering in a resourceful way. Knowing the fact that dither power versus SNR is decisive for reception, ensuring ideal operation could include an adaptive dither power as a response to received SNR. The signal detection algorithm implemented according to section 4.4 operates through a self-correlation of the periodic preamble, fully dependent on a sufficient SNR. In this regard the detection method could serve as an SNR estimate of the received signal, but demands further studies to motivate as an implementable solution. Implementation of such a solution would require feedback from the FPGA to the RRH. A more implementable solution could be to ensure a high SNR during tests, and in that case reduce the impact of signal noise. Then the dither would make the decisive noise control.

In order to implement a low-complexity distributed network, the SFP+ optical transceivers are profitable regarding the fiber connection enabling spatial distribution, as well as dithering through the dual optical link. Although the dither ideally would be applied with adjustable power, it may not be realistic for the proposed system design. The SFP+ units have a constant output power, demanding a feedback-controlled gain at the RRH, aggravating an actual implementation. However, if the testbed environment is controlled such that the received SNR is within an operating interval, the benefit of multiple RRHs would enable reception at a stationary dither power. Such a testbed would still provide valuable insight in this sort of system.

There are many aspects to consider in the realization of a functional testbed in a resourceful way, but the results presented in this report indicate that such a system is in fact implementable.

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