CHALMERS
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Modelling of Modular Multilevel Converter Using Input Admittance Approach

Chalmers University of Technology
Division of Electric Power Engineering

Master's Thesis in Electric Power Engineering

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Department of Energy and Environment
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Abstract

With increasing Distributed Energy Resources (DER) penetration and increased High Voltage Direct Current (HVDC) applications, Modular Multilevel Converter (MMC) is becoming an integral part of the power system due to its advantages in terms of scalability, harmonic performance and efficiency. One of the most challenging topics as with regard to MMC lies in its modelling as the detailed model offers computational challenge during transient simulations. Thus, the main purpose of this study is to derive an input admittance model that can be used for stability studies and controller designs.

In this thesis, the topology and operating principles of MMC are studied and an input admittance model is derived analytically. The derived input admittance is then compared with the input admittance of two level converter. Moreover, an average model of an MMC with four Sub Modules (SM) per arm is simulated in PLECS and used to validate the analytical model using frequency domain approach. Furthermore, the impact of different controller parameters, switching schemes and switching frequency variations on the derived input admittance is investigated.

It is found that the analytical and the simulated models agree very well for the entire frequency range with the exception of slight discrepancy at low frequency ranges (between 1 and 10 Hz). It is demonstrated that the input admittance model remains the same regardless of the changes in modulation schemes. Moreover, the derived input admittance is able to predict the changes in the input admittance of MMC due to control parameter variations.

Keywords: MMC, Input Admittance, MMC Modelling, Converter Control, PLECS, AC sweep analysis.

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Adulis Abun, Gothenburg, April 2016

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List of Acronyms

AVM Average Value Model
DEM Detailed Equivalent Model
HVDC High Voltage Direct Current
IGBT Insulated Gate Bipolar Transistor
MMC Modular Multilevel Converter
NLC Nearest Level Control
NVC Nearest Vector Control
PWM Pulse Width Modulation
PD Phase Disposition
POD Phase Opposite Disposition
APOD Anti Phase Opposite Disposition
PS-PWM Phase Shifted Pulse Width Modulation
PI Proportional Integral
SM Sub Module
SHE Selective Harmonic Elimination
SVM Space Vector Modulation
VSC Voltage Source Converter

1
Introduction

1.1 Introduction

With the trend of increasing in the penetration of distributed energy resources, the VSC (Voltage Source Converter) is becoming a key role player in integrating these renewable energy resources with the existing grid. Moreover, it is being used as a fundamental block in different power electronic based devices, to solve differ challenges in the power system; starting from integrating renewable energy resources to HVDC (High Voltage Direct Current) applications. However, to meet the rising demands of power capabilities and harmonic performance of converters, a VSC based technology, MMC (Modular Multilevel Converter) is emerging as an optimum solution for a wide range of applications.

The modular topology of MMC enables to build high voltage converters with a higher scalability and fault tolerance [7]. By increasing the number of voltage levels in the output using more sub modules, the power capability can be increased and the switching frequency can be effectively reduced. Furthermore, as the harmonics of the output voltage are reduced due to increased voltage levels, less filtering is required hereby improving the compactness of the system. The reduced switching frequency will also help in decreasing the switching losses significantly and thus leading to increased power ratings of the converter. Besides, as there is no direct series connections of the several semiconductor switches involved, problems related to simultaneous switching are also avoided [7]. Nevertheless, low order voltage harmonics at low switching frequencies put a larger energy storage requirement than as in traditional two level converters [6]. Thus, deriving a model that can completely describe the technical characteristics of the converter, including the internal dynamics of the SM capacitor voltages and currents circulating between the legs of the converter is of significant importance.

1.2 Background

The first MMC based HVDC transmission project, the Trans Bay Cable, was commissioned in 2010 by Siemens [1]. In addition to HVDC transmission applications, the MMC technology is being investigated for a wide range of applications such as railway feeding interties and medium voltage industrial drives [2] for its numerous benefits. Consequently, it is an active research area where investigations aiming at a deep understanding and optimum solutions for modeling, modulation schemes, con-

trol strategies, fault analysis... etc. are being carried out. As a model is the building block for all studies and analysis, this thesis will focus on modelling of MMC.

So far, different topologies of MMC have been proposed addressing specific concerns. A frequency domain model of MMC, for steady-state analysis of all operating point variables has been derived in [2] and [6]. In addition to mimicking the results of the detailed time domain computations, the model has a further advantage of clearly separating the dynamic and steady state effects. However, several assumptions in the model such as ignoring the switching harmonics, were made and thus it has a setback as it is not able to model the dynamics of the system. Consequently, it can't be used for further control system analysis, such as in the design and evaluation of the closed loop control systems.

One of the potential methods of representing the models of converters is to express the converter in terms of its input admittance matrix. In [4], a controlled three phase VSC is modelled using its input admittance. The main advantage of representing the VSC using this method its input admittance matrix is credited to the robustness of the model for different applications, such as studying the stability and grid interaction of the converter. Furthermore, the technique creates ease in modeling any change in the system, like modification of control schemes and parameters[4].

1.3 Outline of Thesis

After defining the scope of the thesis in the introduction, the theory of operating principle and topology of MMC is presented in Chapter 2 of the thesis. In Chapter 3, an analytical model for the input admittance of an MMC will be derived. Moreover, comparison of this input admittance model with that of a two level Converter (VSC) will be carried out in this chapter. Furthermore, the simulation model of MMC is discussed in Chapter 4. In this chapter, PLECS model of the MMC with the assumption of constant capacitor voltage is developed for verification purposes. Subsequently, changes in the input admittance with the changes in the controller parameters and modulation strategies used is investigated in Chapter 5. The Verification of the analytical model by comparing it with the simulation results is also be presented in this chapter. Finally conclusions and recommendations for future works are presented in Chapter 6.

2

Modeling of MMC

2.1 Topology and Operating Principle

As it can be shown in Figure 2.1, the circuit structure of MMC consists of three phase legs, each comprising of two arms connected in series between the dc-link. There are N number of Sub Modules (SM) in each arm in series with the arm inductor and resistor. The main objective of the inductor is to limit the surges in the arm current and also arm current harmonics; thus they are significant in the control of circulating currents. The resistances are operational variables, as they model the converter losses and the resistances of the inductor.

The SMs are the basic building blocks of the MMC and consist of either of the most popular configurations; half bridge or full bridge configurations. The half bridge configuration, which is the focus of this thesis, is depicted in Figure 2.2. It comprises of two switches, which dictates the charging and discharging of the capacitor. The switches consist of a controllable power switch (e.g. an IGBT) and an anti-parallel diode. When a switch is turned on, either the IGBT or the antiparallel diode in the same switch conducts. Only one switch is turned on at a time and thus there are three possible switching modes; inserted, bypassed and blocked. The SM is said to be inserted if switch S1 is turned on and the capacitor can be either charging or discharging depending on the direction of the arm current. If the arm current flows into the SM through the anti-parallel diode of S1, then the capacitor will be charged. However, if the current flows out of the SM through the IGBT of S1, then the capacitor will be discharged. Nevertheless, regardless of the direction of the arm current, the terminal voltage of the SM is the same as the capacitor voltage. The SM is operating in its bypassed mode if switch S2 is turned on. In this mode whichever the direction of the arm current is (either the IGBT or the anti-parallel diode will conduct depending on the direction of the arm current), the capacitor voltage remains constant and the terminal voltage of the SM is zero. The blocked mode of operation of the SM is when both the switches are turned off. This is impractical mode of operation as the capacitor can only charge (through the anti-parallel diode), but never discharge. As a result of the two practical modes, the SM can be controlled to provide either the capacitor voltage or zero output voltage. This way, the SMs are switched on and off generating stepped, near-sinusoidal waveforms.

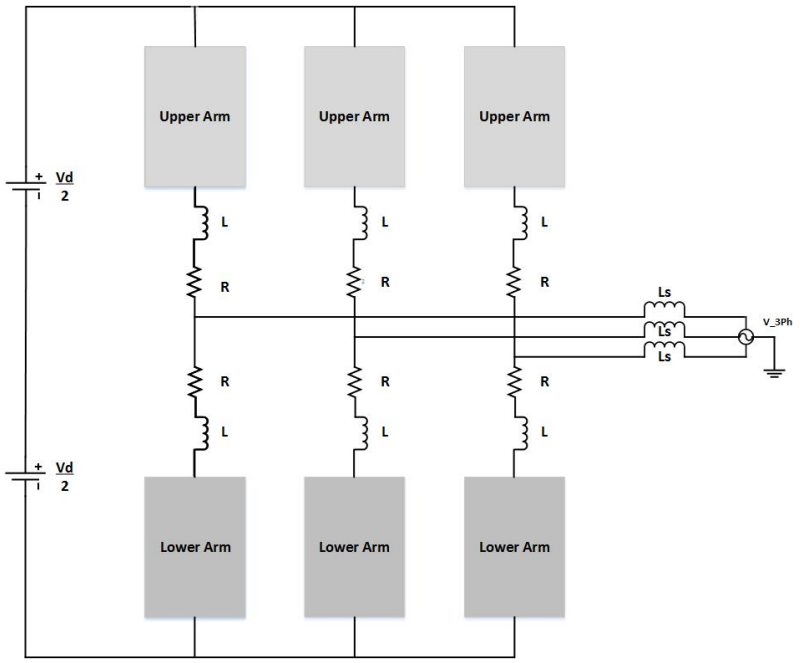

Figure 2.1: Schematic diagram of three phase MMC

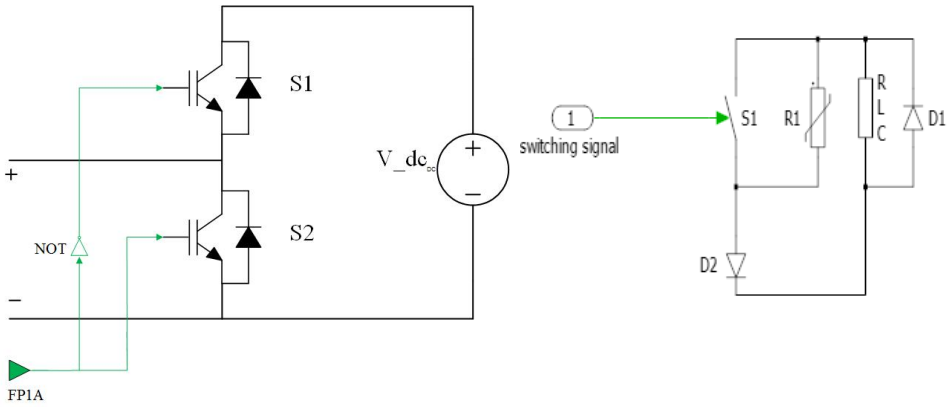

Figure 2.2: Figure 2-2 (a) Half-bridge SM (b) IGBT valve (detailed model)

2.1.1 Average Value Model (AVM) and Detailed equivalent models (DEM)

In [13], the performance of both the average value model (AVM) and detailed equivalent model (DEM) are analyzed. The proposed AVM assumes an ideally balanced capacitor voltages and ideal IGBTs. Moreover, the MMC characteristics are modelled using a controllable voltage source for the ac-side representation and controllable current source for the dc-side representation. On the other hand, the detailed model assumes the valves as ideal IGBT switch and the antiparallel diodes as nonlinear resistances. Detailed equivalent model treat each MMC arm as a Thevenin equivalent branch whose voltage and resistance is calculated each switching period.

Detailed models are far more accurate than the averaged models, but they are computationally challenging [9]. Even though the average model is able to replicate the dynamic performance of the converter accurately, unlike the detailed model, it cannot represent specific switching states. As a result, the average model cannot simulate different faults, such as SM failures or control system failures in the SMs as well as in the converter [9].

However, this thesis uses the AVM for simulating the MMC in PLECS. The AVM is selected due to its capability to model the dynamics of the converter accurately and its computational simplicity. The simulation of the MMC for validating the analytical model is discussed in Chapter 4 in detail.

2.1.2 MMC System Model Parameters

In order to validate the analytical input admittance using simulations, an MMC with 4 SMs is simulated in PLECS. The parameters of the MMC are given in Table 2.1. The dc-link voltage is selected to be 16 kV and thus the capacitor voltages are made to be 4 kV each. The selection of the control parameters and the choice of the switching frequency is discussed in chapter 4.

Table 2.1: Specification of MMC base parameters.

Parameter	Value	Parameter	Value
Arm inductance (L)	2mH	Output inductance (L_s)	2mH
Arm resistance (R)	0.1Ω	Current control bandwidth (α_C)	$0.2\omega_{sw}$
Grid voltage (v_g)	7kV	Feed forward Voltage bandwidth (α_F)	$0.1\alpha_C$
DC link voltage (v_d)	16kV	SM per arm (n)	4
Capacitor Voltage (v_{sm})	4kV	Switching frequency (f_s)	2075 Hz

2.2 MMC Internal Control (Dynamics)

The dynamics of the MMC is mainly associated with that of SM capacitor's dynamics. The internal dynamics mainly comprises of the SM capacitors' voltages and the circulating currents. To simplify the complexity of the model, it is proved in [14] that the sum of the capacitors voltage in an arm can be taken into consideration instead of separate capacitor voltage of the SM. This consideration is further used to derive the analytical model in chapter 3.

There is a nonlinear relationship between the circulating currents and the capacitor voltage variations. These variations in voltage when the capacitors are charged and discharged (insertion and bypassing of the SM), cause the circulating current harmonics. On the other hand, the circulating currents cause the capacitor voltage ripples [6]. This nonlinearity poses some challenges in deriving the frequency model [2], [6]. Thus, the analytical derivations carried out in this thesis assume perfectly

balanced capacitor voltages and as a result capacitor voltage balancing algorithm is not implemented in the simulations.

2.3 Modulation for Switching Pulse Generation

Numerous modulation and control schemes have been studyed in various literatures throughout the work of this thesis. The classification of the various types of modulation techniques based on switching frequencies is presented in [16]. For high switching frequency modulations, the carrier based modulation with phase shifted (PS-PWM) or level shifted (PD, POD, APOD-PWM) carrier and space vector modulation (SVM) techniques are suggested. Whereas for low switching frequency modulations, Selective Harmonic Elimination (SHE), Nearest Vector Control (NVC) and Nearest Level Controls (NLC) are recommended. The various techniques have also been presented in [15] and a choice is made based on the number of voltage levels. With the increase in the number of levels, PWM and SHE become computationally inefficient [15], SVM complexity increases exponentially [17], and thus NLC is proposed for higher number of levels. In practice PS-PWM is being used by ABB, while Siemens use NLC [18].

The modulation algorithm is responsible for obtaining the desired voltages at the outputs. In order to ensure the proper operation of MMC and to obtain the desired output waveforms, the capacitor voltages must be balanced and their variations maintained within a narrow band. The capacitor voltage balancing strategies can be based on the modulation techniques or control algorithms [10]. Three of these control methods are presented in [17] and it is proposed that the voltage balancing algorithm be integrated into the modulation scheme either by modifying the switching functions or the switching sequence. The principle of operation of these modulation strategies is to control the capacitor voltage within a narrow band by feedback control or by controlling the switching sequence of the SM. Thus, an ideal modulation technique depending on the latter strategy consist of a waveform generator technique and voltage balancing algorithm. The waveform generator technique decides the insertion ratio (the number of the SM in an arm to be inserted) by comparing the reference switching signal with the carrier and the voltage balancing algorithm determines the specific SM to be inserted or bypassed [10].

Conventional harmonic analysis methods for carrier based modulation is carried out in [12] and it is found out that the capacitor voltage will diverge, if the switching frequency is selected as an integer multiple of the fundamental frequency. However, it is observed if the carrier frequency (ω_c) is selected in such a way that $N\ \omega_c$ (where N is the number of SM in an arm) is an integer multiple of the fundamental frequency (ω_1), then the sub-harmonics and harmonics which are non-integer multiples of the fundamental frequency will be suppressed in the sum of the switching functions of an arm [12]. The ac-side voltage mainly depends on the difference of the upper and lower arm voltages, while the dc-link voltage depends on the summation these two voltages. Thus, if the switching harmonics of the upper and lower arm

voltages are in phase with each other, the ac-side harmonic content will be enhanced.

On the other hand, if the switching harmonics are out of phase the dc-link harmonic performance will be improved, as there is cancellation of the corresponding harmonic content. The phase angles of the switching harmonics are determined by the phases of the carrier waveforms, which can be optimized either for the dc-link or ac-side harmonic performance. The phases of the carrier waveforms of the SM can be determined on the bases of the selection of the harmonic performance that needs to be optimized. Thus, two kinds of PS-PWM modulation schemes $N+1$ and $2N+1$ were presented and they are summarized in Table 2.2. Moreover, it is found out that the mathematical model of the $2N+1$ level modulation is more complex than the $N+1$ level modulation. This is due to the fact that the upper and lower arm switching harmonics do not always cancel out. Thus, N+1 level modulation is preferred for further analysis as in [12], [10], [16].

Table 2.2: Comparison between $N+1$ and $2N+1$ $PS-PWM$ modulation.

	$N+1$ Modulation	$2N+1$Modulation
Harmonics performance	dc-link harmonics is enhanced	ac-side voltage harmonics is improved
Phase shift (β) of carrier waveforms in the upper and lower arms of a phase leg	π radians out of phase.(i.e $\beta = \pi$)	in phase (i.e.$\beta = 0$ when N is odd, and $\beta = \frac{\pi}{N}$ when N is even)
Insertion index for a phase leg	constant	Variable
Voltage levels of phase to neutral	$N+1$	$2N+1$

2.4 Switching Frequency

The selection of the switching frequency affects the switching losses, harmonics content, and voltage balance of the SM capacitors and the overall efficiency of the converter [11]. Moreover, there is a tradeoff between the capacitor voltage ripple and the switching frequency. To ensure high efficiency of the converter, the switching frequency is preferred to be as low as possible. On the other hand, the capacitor voltage balancing challenge increases as the peak to peak voltage ripple of the individual SM increases due to the significant reduction in switching frequency. Consequently, there is a lower limit of the switching frequency below which the peak to peak capacitor voltage ripple may cause voltage imbalance between individual capacitors and hence instability. The effect of switching frequency on the arm and line harmonics is also affected by the number of SMs per arm and the control strategies employed [11].

3

Input Admittance Analysis

3.1 Introduction

As the role of the grid-connected converters for various HVDC and FACTS applications increase, it is necessary to analyze the impact of the introduction of the converters into the grid. The converter can be interconnected with the grid easily, without causing instabilities, as long as its control system is designed in such a way that its input admittance is passive. This way, the system will dampen oscillations at any frequency [21].

In order to achieve passive input admittance for a VSC, Proportional-Integral (PI) based current controller in synchronous (dq) reference frame with dq decoupling and voltage feed-forward can be designed. In [4] and [21], expressions for the elements of the input admittance of a controlled two level VSC have been derived. The input admittance of the converter is then used as a tool for a closed-loop stability analysis of the converter-grid interconnection. With growing usage of MMC, the need for input admittance model of MMC also rises for the reasons mentioned above. This section focuses on derivation of input admittance model for an MMC.

3.2 System Model

3.2.1 Per-Phase Dynamics

In deriving the continuous-time model of the MMC, certain assumptions are made to ease the complexity. On the assumption that the switching frequency and the number of the SMs per arm are satisfactorily high, the discrete nature of the waveforms can be neglected. The impact of switching delay on converter characteristics is neglected by assuming a reasonably high switching frequency. Fixed SM capacitor voltage is assumed; thus no circulating current control and capacitor voltage control is employed. Furthermore, the three phase model can be transformed into a single phase, if the leg and filter inductances are assumed to be the same and if the grid is assumed to be balanced. As mentioned in 2.2, the sum of the capacitors voltage in an arm can be considered instead of individual SM capacitor voltages. Based on all these assumptions a per-phase model seen in Figure 3.1 is used for further analysis.

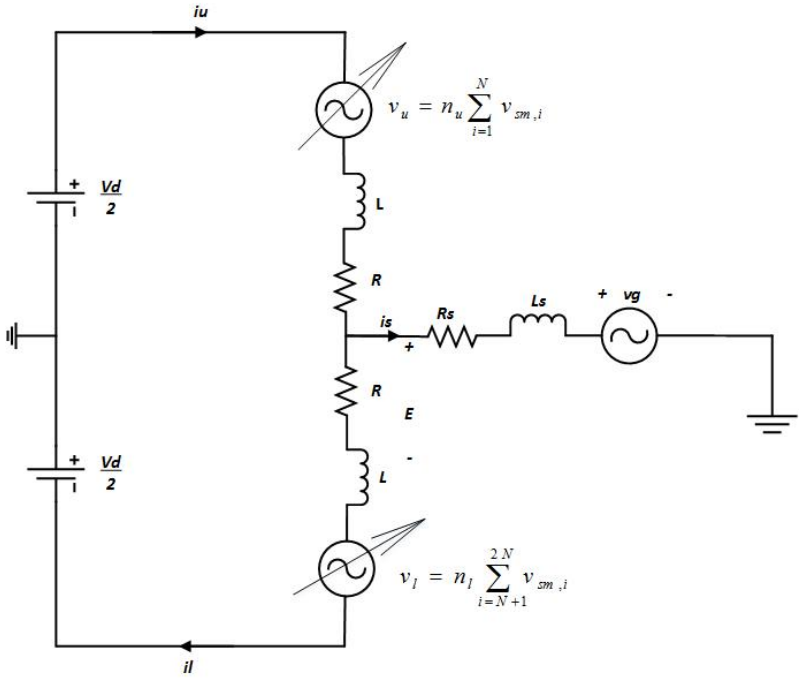

Figure 3.1: Per-Phase equivalent model of an MMC

With i_l representing the lower arm current and i_u the upper arm current, the ac-side current (i_s) and the circulating current between dc terminals (i_c) are given by

$$i_s = i_u - i_l \tag{3.1}$$

$$i_c = \frac{i_u + i_l}{2} \tag{3.2}$$

Similarly, the ac-side voltage driving ac-side current (v_s) and the internal voltage deriving the circulating current (v_c) are given by:

$$v_s = \frac{v_l + v_u}{2} \tag{3.3}$$

$$v_c = \frac{v_d - v_u - v_l}{2} \tag{3.4}$$

Where v_l is the inserted voltage in the lower arm, v_u is the inserted voltage in the upper arm and v_d is the pole to pole voltage of the dc-link.

Applying KVL, we can derive

$$\frac{v_d}{2} - Ri_u - L\frac{di_u}{dt} - v_u = E \tag{3.5}$$

where E is the voltage at the converter output. Similarly,

$$-\frac{v_d}{2} + Ri_l + L\frac{di_l}{dt} + v_l = E \tag{3.6}$$

Adding (3.5) and (3.6)

$$R(i_l - i_u) + L\frac{d(i_l - i_u)}{dt} + v_l - v_u = 2E$$

Putting in (3.1) and (3.3)

$$v_s - \frac{R}{2}i_s - \frac{L}{2}\frac{di_s}{dt} = E$$

Substituting $\frac{R}{2}$ and $\frac{L}{2}$ with R' and L', respectively, the expression is simplified to

$$v_s - R'i_s - L'\frac{di_s}{dt} = E \tag{3.7}$$

As shown in [14], the per-phase dynamics consisting of the internal dynamics of the SM capacitor voltages and the circulating current can also be expressed in terms of the internal control variables i_s, i_c, v_s and v_c as

$$\frac{dv_u}{dt} = \frac{N}{C}n_u\left(i_c + \frac{i_s}{2}\right) \tag{3.8}$$

$$\frac{dv_l}{dt} = \frac{N}{C}n_l\left(i_c - \frac{i_s}{2}\right) \tag{3.9}$$

where N is the number of SMs in an arm, n_u is the insertion index for the upper arm, n_l is the insertion index for the lower arm. In addition, the dynamics for the circulating current as,

$$\frac{di_c}{dt} = \frac{1}{L}\left(v_c - Ri_c\right) \tag{3.10}$$

Rearranging (3.7)

$$\frac{di_s}{dt} = \frac{1}{L}\left(v_s - E - Ri_s\right)$$

Moreover, the converter output voltage E and the grid voltage v_g can be related as

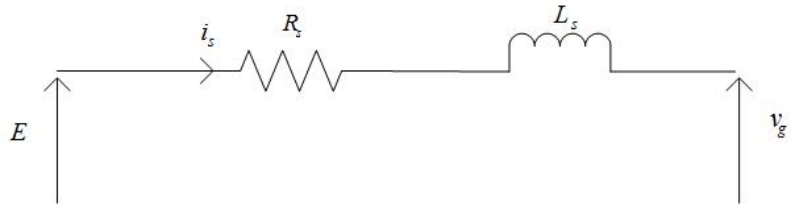

Figure 3.2: Ac-side parameters

$$E - v_g = L_s\frac{di_s}{dt} + R_s i_s$$

Thus, (3.7) can also be expressed as

$$\frac{di_s}{dt} = \frac{1}{L''}\left(v_s - v_g - R''i_s\right) \tag{3.11}$$

where $L'' = L_s + \frac{L}{2}$ and R" $= R_s + \frac{R}{2}$

3.2.2 Open-loop System

If the open-loop system represented by (3.7) is transformed into the *dq* reference frame, it can be expressed as

$$E_d = v_{sd} - \Big(R' + L's\Big)i_{sd} + L'\omega_1 i_{sq} \tag{3.12}$$

$$E_q = v_{sq} - \Big(R' + L's\Big)i_{sq} - L'\omega_1 i_{sd} \tag{3.13}$$

where ω_1 is the angular frequency of the reference waveform. Furthermore, this can be written as

$$v_{sd} - E_d = \Big(R' + L's\Big)i_{sd} - L'\omega_1 i_{sq}$$

$$v_{sq} - E_q = L'\omega_1 i_{sd} + \Big(R' + L's\Big)i_{sq}$$

Thus, if expressed in the matrix form it will be

$$\begin{bmatrix} v_{sd} - E_d \\ v_{sq} - E_q \end{bmatrix} = \begin{bmatrix} R' + L's & -L'\omega_1 \\ L'\omega_1 & R' + L's \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} \tag{3.14}$$

(3.12) and (3.13) can also be compiled to describe the open-loop system in terms of d-q space vectors, i.e. (3.12) + j*(3.13), then

$$E = v_s - \Big(R' + L'\Big(s + j\omega_1\Big)\Big)i_s$$

Solving for i_s,

$$i_s = \frac{1}{R' + L'\Big(s + j\omega_1\Big)}\Big(v_s - E\Big) \tag{3.15}$$

3.3 Control System Design and Input Admittance Derivation

3.3.1 Controller Design Principle

For MMC to operate properly, there should be a voltage difference between the dc-side voltage and the dc component of the output voltages of the SMs. The differential voltage generates a circulating current between the legs of the converter, which is responsible for the transfer of power between the sides of the converter. Moreover, the average SM capacitor voltage should be also maintained at a constant value to ensure that the average power transfer through an SM is zero.

These conditions are met by controlling the switching action of the power electronic switches of individual SMs. Regardless of the strategy used, the control system should achieve certain objectives such as:

- active and reactive power control.

- dc-side voltage control.
- circulating current control.
- arm capacitors voltage control.
- SM capacitor voltage balancing.

The typical control system have a cascaded structure consisting of inner loop and outer loop controls. The inner loop control involves current controller, while the outer loop control comprises of active power control and reactive power (terminal voltage) control as detailed in [4], [21] and [23]. However, in this thesis only the inner loop current controller is considered. It is implemented in the synchronous (dq) reference frame, which enables an independent control of the active and reactive power [20]. Moreover, capacitor voltage control is omitted as a constant capacitor voltages are considered. Furthermore, all the outer loop controllers are not included in the scope of this thesis.

3.3.2 Current Control Loops

The control method implemented for controlling the ac-side current is based on dq (synchronous) frame control and is depicted in Figure 3.3. This transformation from the stationary frame adds a cross-coupling term and to mitigate that a decoupling term is added in the control method in order to ensure independent control of the d and q components. As can be seen in Figure 3.3, the cross coupling effect cancellation is implemented by an inner loop of a positive feedback with a gain of $j\omega_1 L$. Moreover, a voltage feed-forward is also included for good dynamic performance. Furthermore, in case the voltage feed-forward option is unavailable due to difficulty in measuring the voltage E, active damping path might be added in the derivation [21].

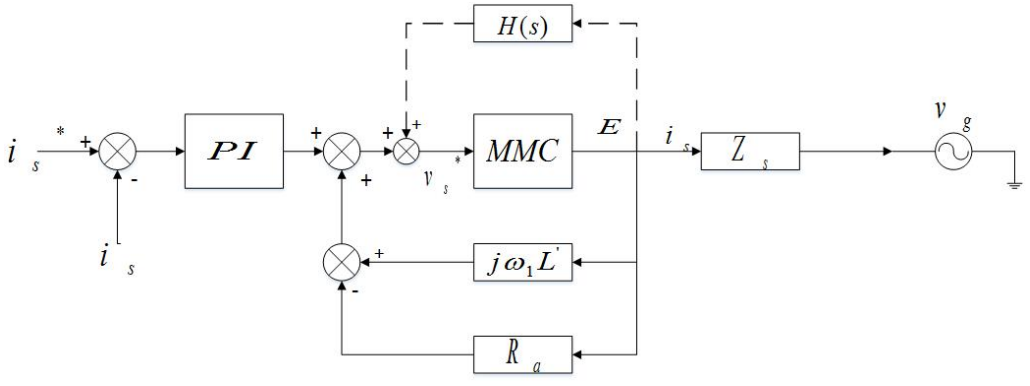

Figure 3.3: Output Current Controller

3.3.3 Choice of control laws

The input admittance of a converter depends on the control implementation. In this section PI controller of the ac-side current is used to calculate the expressions for

the input admittance of the ideal system; a system where the outer-loop controls is neglected. PI current controller with voltage feed-forward, dq-current decoupling and active damping is designed. However, further analysis of the input admittance is made by making the assumption that it is possible to feed-forward the voltage and thus the active damping resistance is neglected. Here, a standard PI controller will be considered to derive the input admittance. However, the choice of control laws is arbitrary and the model can be extended to include the circulating current controller based on the methods provided in [21].

3.3.4 Input Admittance Calculation

Here only the ac-side current controller is considered.

The open-loop system is given by (3.15) as,

$$i_s = \frac{1}{R' + L'\Big(s + j\omega_1\Big)}\Big(v_s - E\Big)$$

A PI current controller with *dq*-current decoupling, PCC voltage feed-forward and active damping results in the control law [21]

$$v^* s = \left[\Big(k_p + \frac{k_i}{s}\Big)\Big(i_s^* - i_s\Big) + \Big(j\omega_1 L' - R_a\Big)i_s\right] + H(s)E \tag{3.16}$$

where $H(s)$ is a first order feed forward filter, k_p is the proportion gain, k_i is the integral gain and R_a is the active damping term.

Assuming that the converter delay time (T_d), which comprises of the controller's computational delay and PWM switching times, then $v_s = e^{-T_d s} v_s^*$. However, neglecting the delay for simplicity, assuming $v_s = v_s^*$ and combining (3.15) and (3.16) results in

$$\begin{aligned} i_s\Big(R' + L'\Big(s + jw\Big)\Big) + E &= \left[\Big(k_p + \tfrac{k_i}{s}\Big)\Big(i_s^* - i_s\Big) + \Big(j\omega_1 L' - R_a\Big)i_s\right] + H(s)E \\ \Rightarrow i_s\Big(R' + R_a + k_p + \tfrac{k_i}{s} + L's\Big) &= \Big(k_p + \tfrac{k_i}{s}\Big)i_s^* + \tilde{H}(s)E \end{aligned}$$

where $\tilde{H}(s) = \tilde{H}(s) - 1$, which can be simplified to

$$i_s\Big(L's^2 + \Big(R' + R_a + k_p\Big)s + k_i\Big) = \Big(k_p s + k_i\Big)i_s^* + \tilde{H}(s)E \tag{3.17}$$

This can also be rewritten in another form as,

$$i_s = G_{ci}(s)i_s^* + Y_i(s)E \tag{3.18}$$

where $G_{ci}(s)$ and $Y_i(s)$ are the ideal inner closed-loop transfer function and input admittance respectively. These are referred as ideal because the outer control loops are neglected.From (3.17) and (3.18), $G_{ci}(s)$ and $Y_i(s)$ can be calculated as

$$G_{ci}(s) = \frac{(k_p s + k_i)}{L's^2 + (R' + R_a + k_p)s + k_i} \qquad Y_i(s) = \frac{s\tilde{H}(s)}{L's^2 + (R' + R_a + k_p)s + k_i} \tag{3.19}$$

3.4 Input Admittance Comparison of MMC and Two Level Converter

The input admittance model for a two level three phase converter (VSC) is derived in [4] and [21]. In [21] an input admittance expression of

$$Y_i(s) = \frac{s\tilde{H}(s)}{Ls^2 + (K_p + R_a + R)s + K_i} \tag{3.20}$$

is proposed; L being the input filter inductance, $H(s)$ feed forward Low pass filter, R_a active dumping Resistance, R input filter resistance, k_p and k_i proportional and integral control parameters. Moreover, as grid voltage is used in [4] and [21], (3.19) can be expressed in terms of grid voltage (v_g). Modifying (3.18) to replace E with v_g (3.19) can be expressed as

$$Y_i(s) = \frac{s\tilde{H}(s)}{L"s^2 + (R_a + K_p + R'')s + k_i} \tag{3.21}$$

Comparing (3.20) and (3.21) it can be easily seen that the expressions of the input admittance for MMC and that of a two level converter are the same with exception of the input filter inductance and resistance. In MMC, the input admittance comprises of the equivalent inductance of the input filter (coupling inductance) and half of the arm inductance in series, while in two level converter it is made up of the input filter (coupling) inductance only. Similarly, the resistive part of the input admittance in MMC includes half of the arm resistance in series with the filter resistance, whereas two level converter consists of the filter resistance only.

However, it is to be noted that the similarity obtained between the input admittances of a two level converter and that of MMC is only under the assumptions taken in this thesis work. Constant capacitor voltage and ideal converter without delay is considered in this thesis. Otherwise, had the internal dynamics of MMC been considered, different relationship between the input admittances of two level converter and that of MMC would have been expected.

4
Simulations

In this chapter, an MMC with four SMs per arm is simulated in PLECS. A single phase open loop system is designed from which a three-phase open-loop system is developed. After verification of the three-phase open-loop system, ac-side current control is implemented for the three-phase MMC and its closed-loop performance is verified.

4.1 System Design Strategy

A simulation model which is used to verify the mathematical model is prepared in PLECS. A balanced capacitor voltage and ideal IGBT switches are considered to simplify the simulation. To achieve the final MMC simulation model required to validate the analytical derivations, a single phase MMC with 4 SMs per arm and an open loop voltage control is initially modelled. After verification of this model, a three phase model with an open loop voltage control is implemented. Finally, a three phase model with ac-side current controller is simulated.

To verify the open-loop model of MMC is working as intended, a comparison of the measured and reference (fundamental) voltages is carried out. Moreover, as the main component of the open-loop system is the modulation part, it is used for validating the proper operation of the open-loop model. Since the total number of inserted SMs in N+1 modulation scheme remains constant during a period, it is also used as a verification tool for the modulation. Similarly, for the closed loop system, the performance of the controller is first analyzed by checking its ability to track reference.

4.1.1 Modulation

Modulation determines the instant at which individual switches change their states and is responsible for obtaining the desired voltage waveforms at the output. From the various SPWM based multicarrier modulation techniques, PS-PWM is selected in this thesis. This is mainly because PS-PWM is one of the widely used industrial standards for carrier based multilevel modulation [17]. In this scheme, multiple carriers with same amplitude and frequency but different phase shifts are compared with a reference waveform to generate the firing pulses as shown in Figure 4.1.

PS-PWM is not suitable for low switching frequencies. The lower the switching

frequency, the higher is the impact of the delay on the converter characteristics. Accordingly, a higher value of switching frequency is considered to reduce the impact. The switching frequency is decided by the carrier frequency and hence a higher carrier frequency of 2075 is selected. The carrier frequency is chosen to meet the conditions for good harmonic performance [12]. Consequently

- the switching frequency is made non-integer multiple of the fundamental frequency (f1), and
- The product of the switching frequency (f_s) and N (number of SM per arm) is selected as an even multiple of the fundamental frequency.

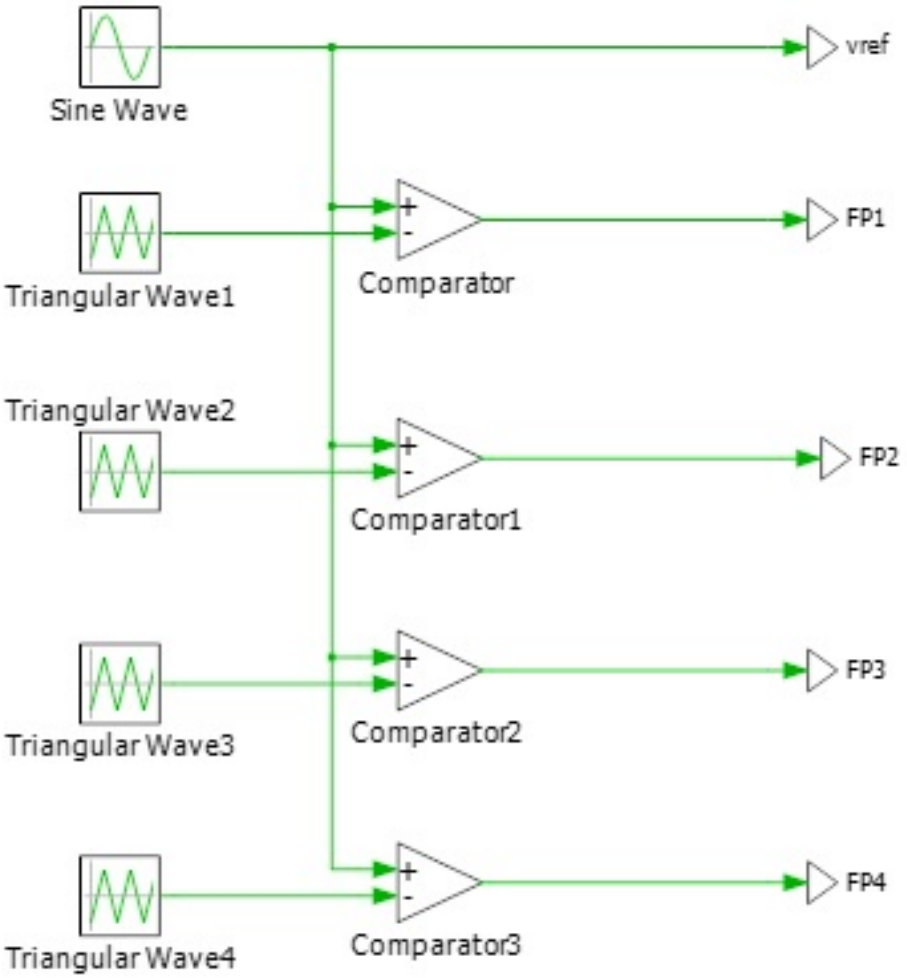

Figure 4.1: Upper arm PS-PWM modulation

Carriers for individual SM are generated and are phase shifted by $\frac{(360)}{N}$ degree, N being the number of SM per arm. The phase shift between the carrier waves is selected on the basis of harmonic performance and the type of modulation implemented. Here $N + 1$ level modulation is selected as it is simpler than the $2N + 1$ level modulation. Moreover, as discussed in 2.3, in $N + 1$ modulation the number of inserted SM per a phase leg is always constant (equal to N per phase leg) and thus can be used as a verification tool.

The reference waveforms for the upper and lower arms are 180° out of phase. A unity modulation index is used and thus the amplitude of the reference is selected to be equal to that of the carrier, which is in turn equal to the half of the dc-link voltage of $\frac{V_{dc}}{2} = 8kV$.

4.1.2 Control System

Controller Design

As can be seen in Figure 4.2, PI current controller of the output (ac-side) current with dq decoupling and voltage feed forward of the grid voltage (V_{gd} and V_{gq}) is implemented in PLECS. For the mathematical model derived in Chapter 3, a consideration of both with and without voltage feed forward is proposed and thus a feed forward of an active resistance is included in order to make the model robust. However, in the simulations only the approach with feed forward voltage is implemented and hence no active damping is included.

The feed forward filter $H(s)$ needs to have a static unity gain to ensure a perfect compensation of E (the voltage at the output of the converter) in steady state [21]. There are many possibilities to achieve this of which a first order filter implementation is the easiest. Therefore, $H(s)$ is selected to be,

$$H(s) = \frac{\alpha_F}{S + \alpha_F} \tag{4.1}$$

where α_F can be selected based on the mode of operation(transient or steady-state). It is recommended in [21] to select an α_F value of less than $0.1\alpha_c$ for steady-state operation and this will be considered in this thesis.

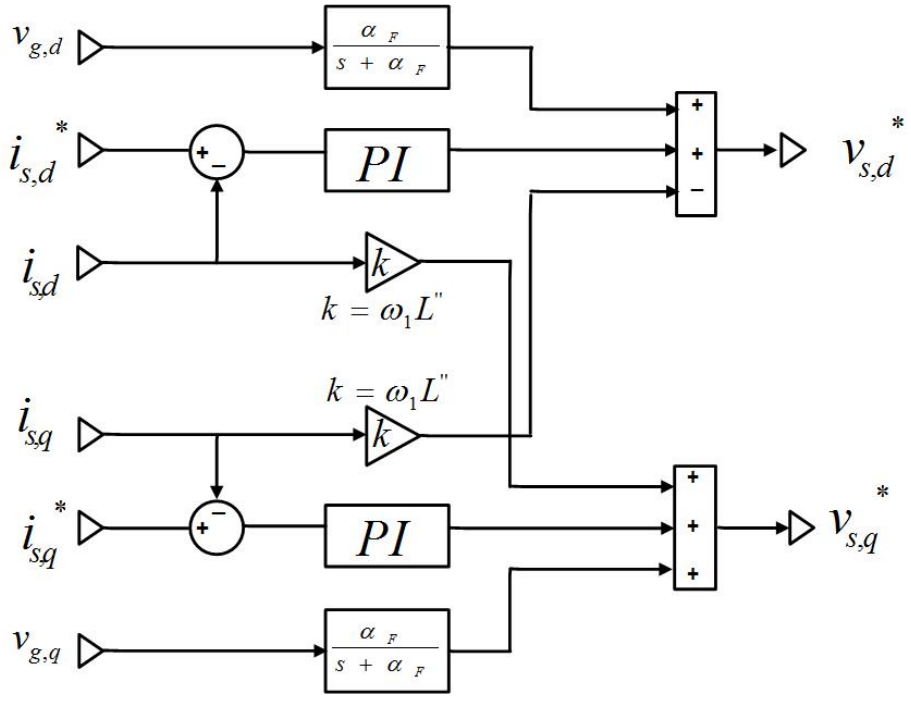

Figure 4.2: Output (ac-side) current controller

Parameter Selection
The maximum bandwidth of the output current controller is limited by the switching frequency [4]. However, the actual bandwidth to be selected is determined by the speed of the response desired. In [21], it is recommended that the bandwidth of the closed-loop current controller should be less than $\frac{1}{5}$ of the angular switching frequency. Hence $\alpha_c \leq 0.2\ \omega_{sw}$ is selected for the simulations as a base value. Moreover, the parameters of the PI controller are selected as $K_p = \alpha_c L''$, whereas K_i is tuned to remove the steady-state errors quickly. However, for analysis carried out in Chapter 5,K_i is selected as $K_i = \alpha_c R''$. Besides, the bandwidth of the voltage feed forward filter (α_F) is selected to be small ($0.1\alpha_c$) for normal mode of operation. Thus, the control block diagram depicted in Figure 4.2 is based on the control law expressed by (3.16) and parameters selected in this section.

4.1.3 AC sweep analysis

As can be seen in Figure 4.3, the perturbation injection to carry out AC sweep analysis is implemented by introducing a disturbance voltage in series with the grid. As PLECS doesn't support a three phase controlled voltage source perturbation (which represents the grid), it was difficult to make the AC sweep analysis of a three phase system. The disturbances in the three phases need to be balanced. In order to meet that condition, a *dq* approach is applied as shown in Figure 4.4. Accordingly, the perturbations are introduced into the dq components, which later are transformed into three phase balanced disturbances.

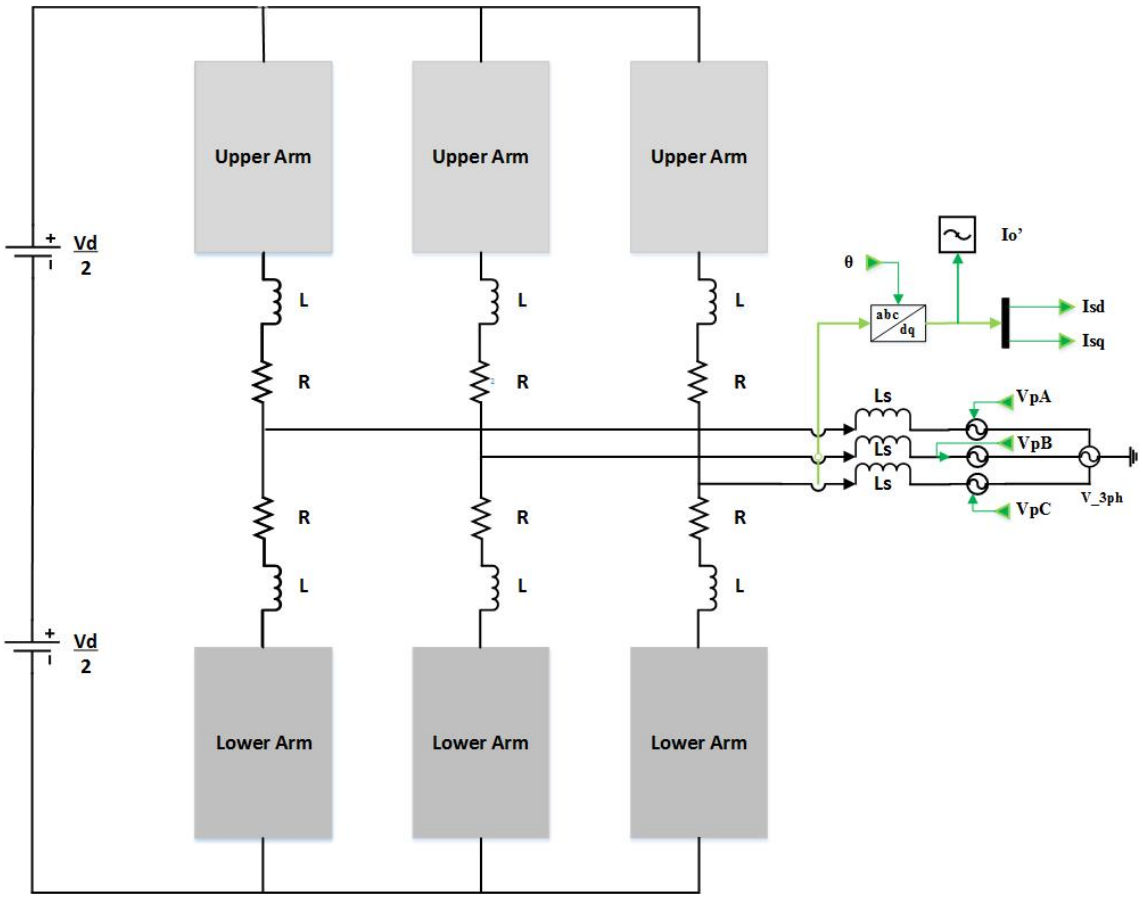

Figure 4.3: AC sweep analysis implementation

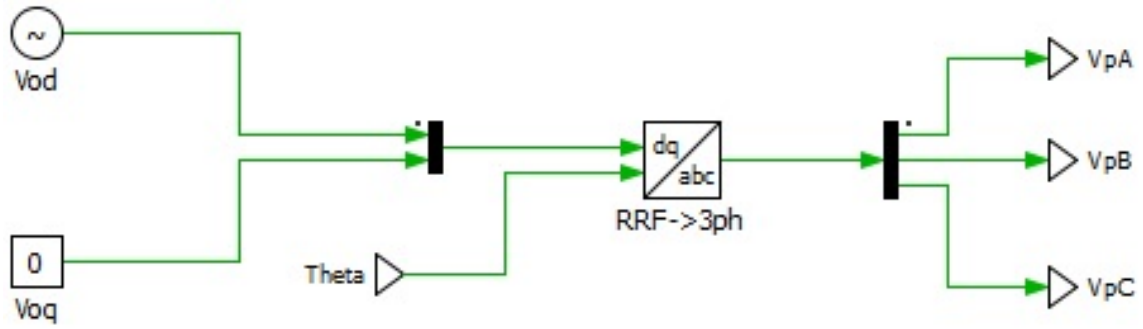

Figure 4.4: Perturbation injection

4.2 Simulation Results

4.2.1 Modulation

As can be seen in Figure 4.5, four phase shifted carriers are compared with a reference to generate the switching pulses for the SMs in the upper arm. Similarly, 4 phase shifted carriers are compared with a second reference which is phase shifted by 180° from the first reference, to generate the complementary firing pulses of the SMs in the lower arm. As shown in the diagram of Number of Inserted Cells (Upper Arm), each time a carrier crosses the reference, there is a change in the number of inserted SMs in the arm.

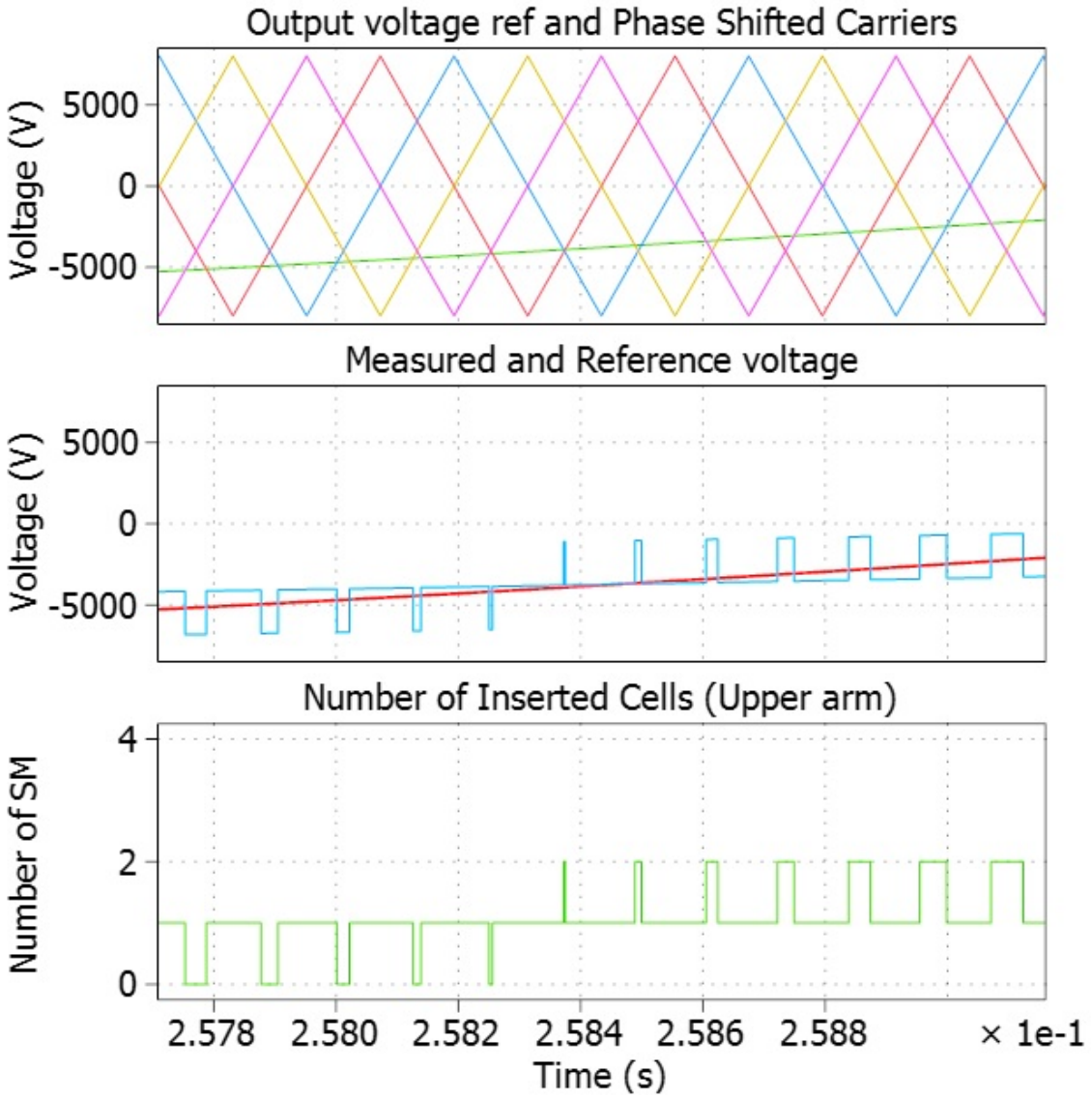

Figure 4.5: PS-PWM switching action for the upper arm

Moreover, as shown in Figure 4.6, the total number of inserted SMs during one period remains constant and is equal to the number of SM in an arm. This is in

accordance with the theory of the $N + 1$ modulation scheme discussed in section 2.3. It can also be noticed, in Figure 4.6 that the output voltage waveform has 5 levels proving the accurate implementation of the $N + 1$ modulation technique. Furthermore, from the second diagram of the same figure, it can be observed that the average of the output voltage coincides with the upper arm reference. This validates the mathematical model, as the simulation results of the output voltage comply with (3.3).

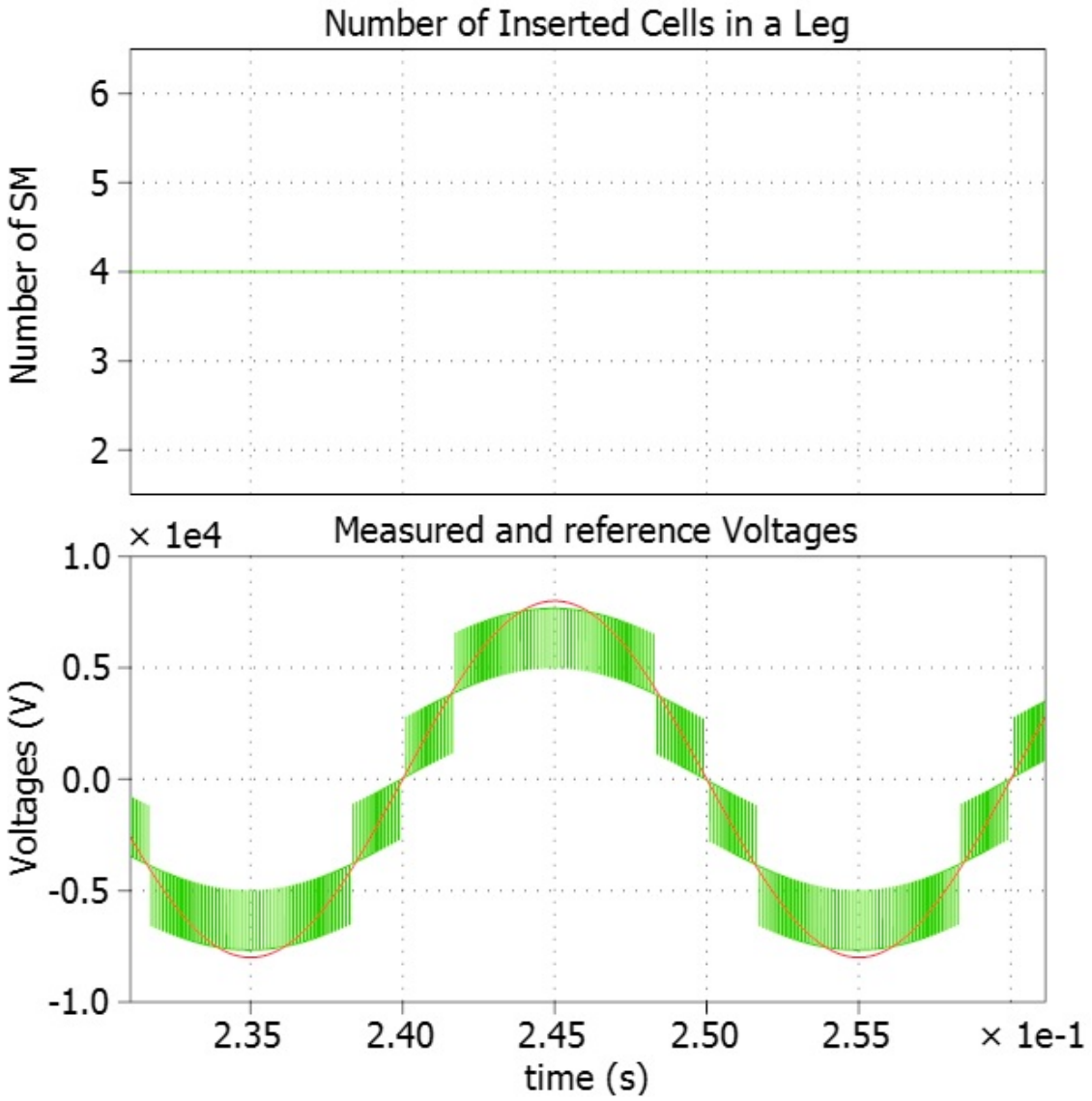

Figure 4.6: Modulation results for the upper arm

In addition, as shown in Figure 4.7, upper and lower arm currents are 180° out of phase. However, they have the same amplitude and frequency. The upper and lower arm currents are determined by the internal dynamics of MMC. Thus, their similarity and harmonic performance obtained in the figure, is the direct result of the presumed balanced capacitor voltage. The arm currents add up as per (3.1) and (3.2), and hence it can be concluded that the mathematical model is valid.

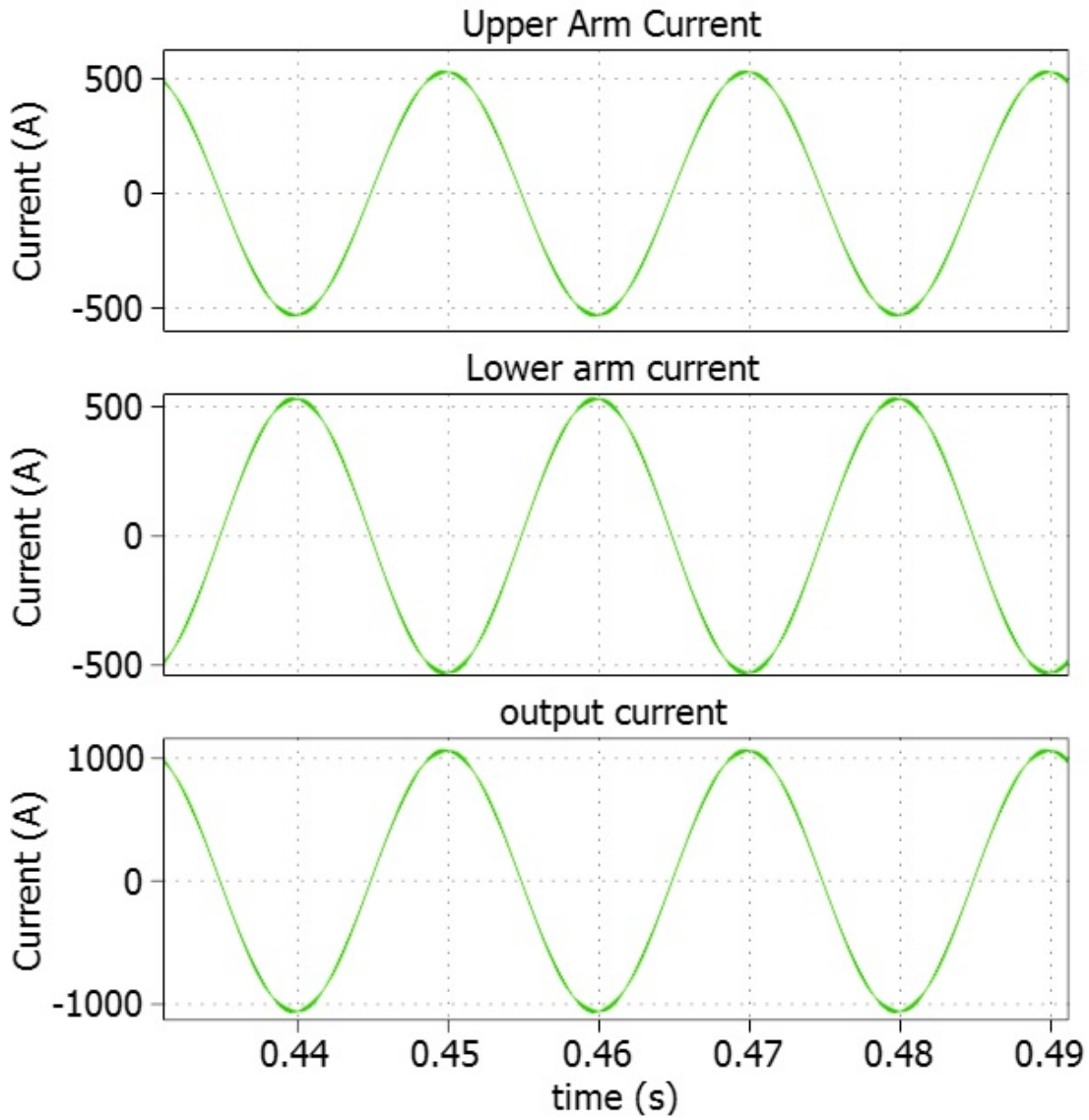

Figure 4.7: Arm and ac-side currents

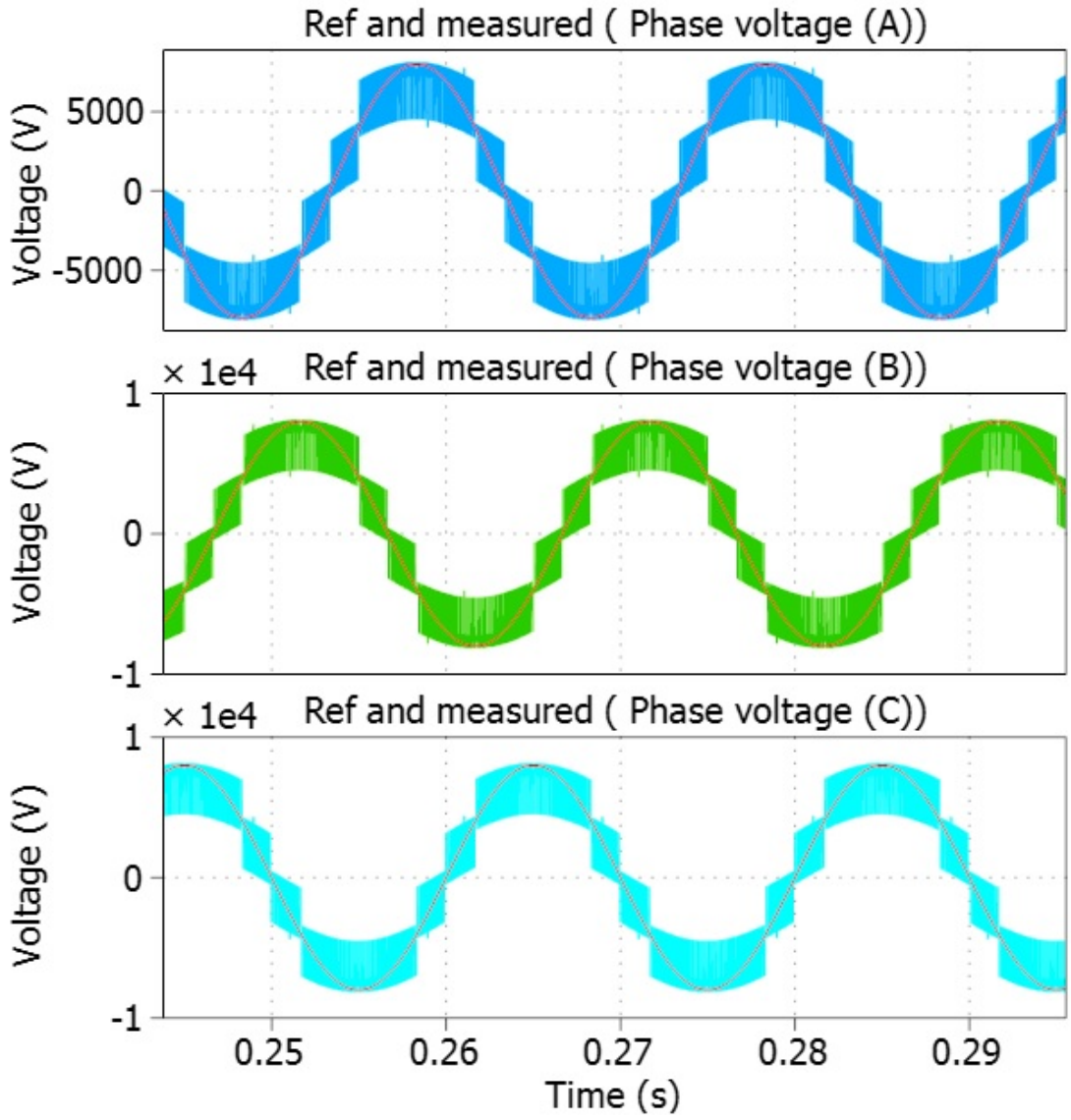

Figure 4.8: Reference and measured phase voltages of three phase model

The number of levels of the converter is governed by the number of phase voltage levels, but not by the load type or the number of phases [23]. In $N + 1$ modulation technique, the number of line to line voltage levels is given by

$$N_{L-L} = 2 * N_p - 1 \tag{4.2}$$

where N_p is the number of phase voltage levels. As can be seen in Figure 4.8 and Figure 4.9, the phase voltages have 5 levels and the line to line voltages have 9 levels, verifying (4.2).

Moreover, closer observation of Figure 4.8 shows the output phase voltages following their respected references. Besides, as can be observed from Figure 4.8 and Figure 4.9, the line to line voltages have higher amplitude and a better harmonic performance than the single phase model.

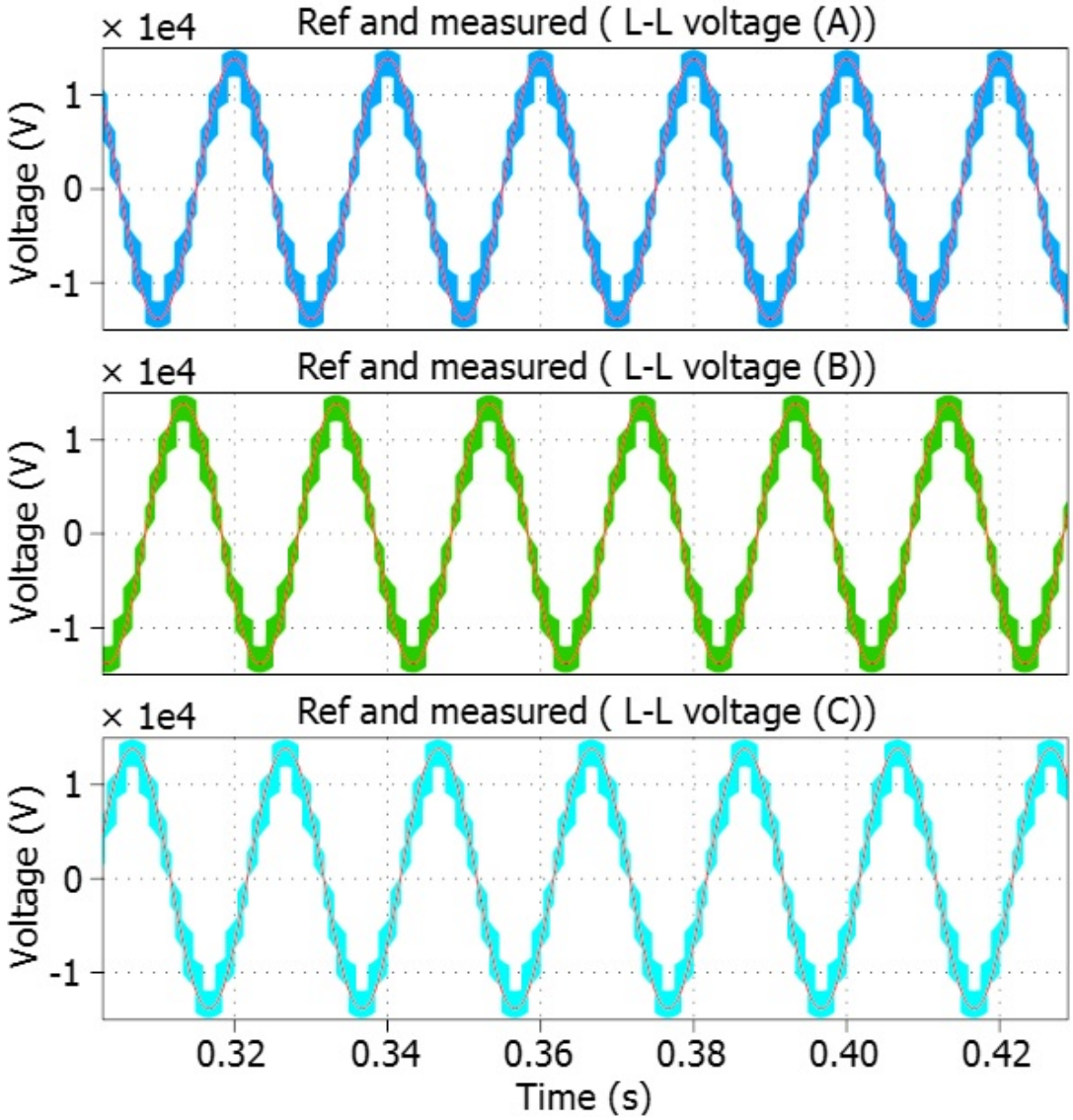

Figure 4.9: Line to line reference and measured voltages

Likewise, as can be seen in Figure 4.10, the output currents are sinusoidal with a balanced phase shifts. The upper and lower arm currents of a phase leg are 180° out of phase. Additionally, it can also be observed that the three phase currents have the same amplitudes.

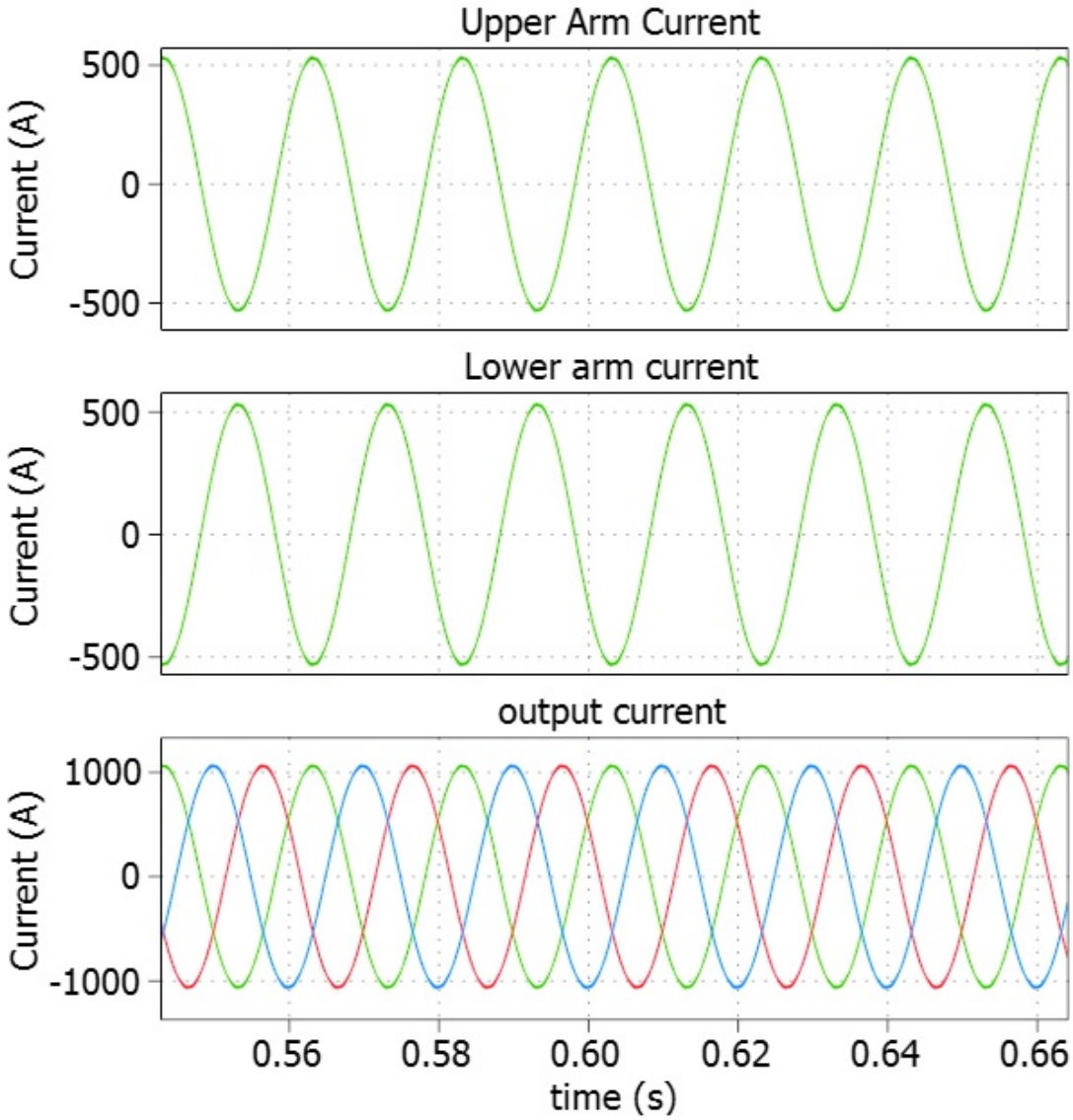

Figure 4.10: Arm and ac-side currents of three phase model

4.2.2 Control System

The dynamic response of the ac-side current controller can be seen in Figure 4.11. Independent steps for the d and q current components are applied at different instants and as can be observed from the figures the current controller tracks the step changes in the references. Moreover, the individual responses of the d and q currents to the respective steps confirm the realization of the decoupling of the synchronous components (dq) by the controller action in steady-state.

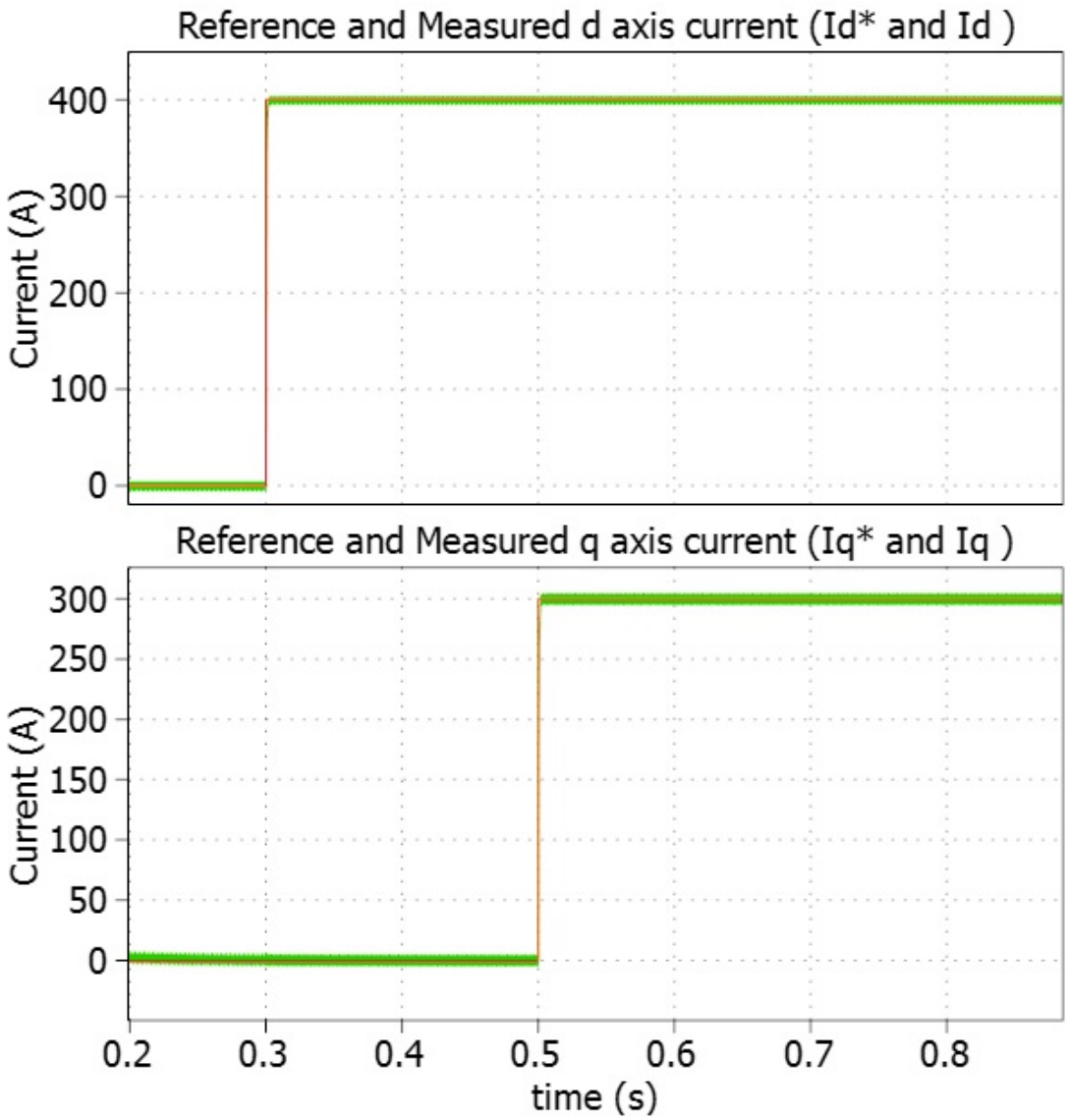

Figure 4.11: Dynamic Response of the output current controller

5

Model Validation

In this Chapter, the analytical results are validated through time domain simulations. To find the input admittances in the time domain simulation, AC sweep analysis is used. This is achieved by injecting a voltage perturbation at different frequencies. The input admittances are then calculated as a rate of the FFT of the current response to the voltage disturbances.

5.1 Impact of Parameter Changes on Input Admittance

In this section, the impact of change in control parameters, switching frequency and modulation scheme on the analytical and simulated models is studied. These studies aim at assessing the robustness of the analytical model to mimic the simulated model for various values of the control and modulation parameters. Therefore, comparisons between the two models under different parameters are made to verify the analytical derivations.

For these analysis, the analytical input admittance model is made to include the filter inductor. This is because the AC sweep analysis calculates the current response to the injected voltage, which represents the whole admittance including the filter. The AC sweep analysis is carried out using PLECS and the result is exported to MATLAB, where the comparison between the analytical and simulated model is carried out.

5.1.1 Effect of α_C

Three different cases have been studied to analyze the effect of the current controller bandwidth on the ability of the analytical model to represent the MMC model. The band width of the current controller is varied to be 10% ($0.1\omega_{sw}$) and 5% ($0.05\omega_{sw}$), of the angular switching frequency, from the base value of 20% ($0.2\omega_{sw}$). As can be seen in Figure 5.1, when α_C is selected as $0.05\omega_{sw}$the two models coincide for the entire frequencies with exception of small deviation below 10 Hz. Similarly it can be observed in Figure 5.2 and Figure 5.3, for $\alpha_C = 0.1\omega_{sw}$ and $\alpha_C = 0.2\omega_{sw}$, that the analytical model mimic the simulation results for the entire frequency ranges

with a very small deviation below 10 Hz.

As can be observed from the three cases (Case I, Case II and Case III) there is no significant difference as long as the ability of the analytical model to mimic the MMC's input admittance is concerned. It can be seen that the three models coincide for the entire frequency range with small deviation in the range below 10 Hz.

Case I For the band width of the current controller chosen as 5% of the switching frequency

α_C=$0.05\omega_{sw}$=651.6 rad/s
α_F=$0.1\alpha_C$=65.2 rad/s
K_p=$\alpha_C L''$=0.7
K_i=$\alpha_C R''$=32.6

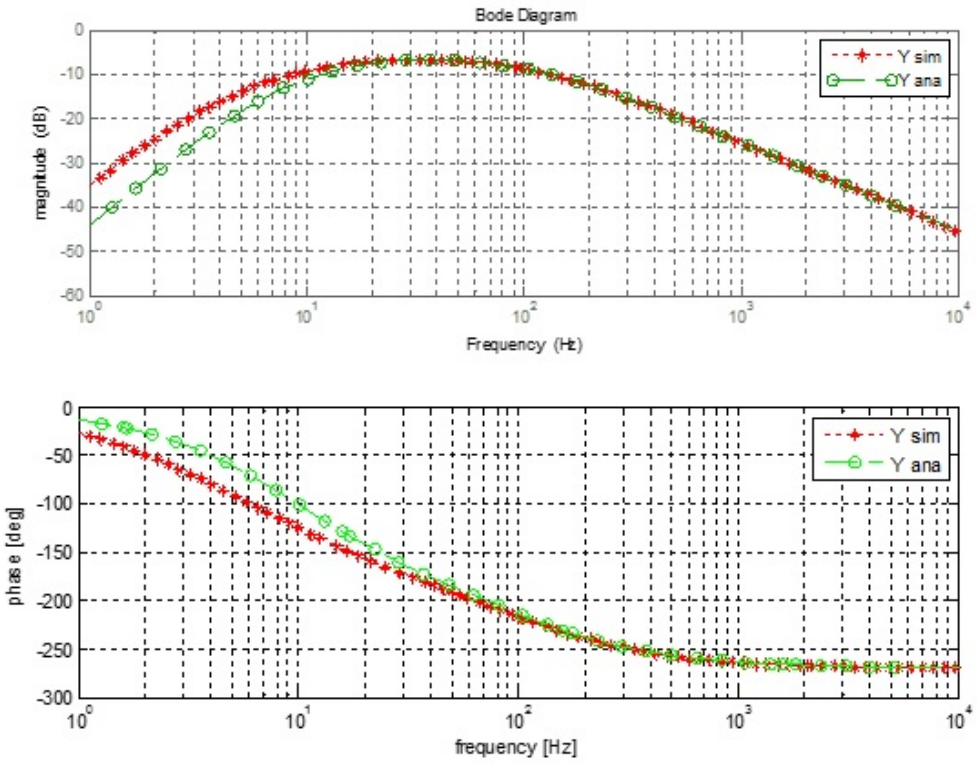

Figure 5.1: Simulation and analytical model input admittance for α_C=$0.05\omega_{sw}$

Case II For the band width of the current controller chosen as 10% of the switching frequency

α_C=0.1ω_{sw}=1303 rad/s
α_F=0.1α_C=130.3 rad/s
K_p=$\alpha_C L''$=1.3
K_i=$\alpha_C R''$=65.15

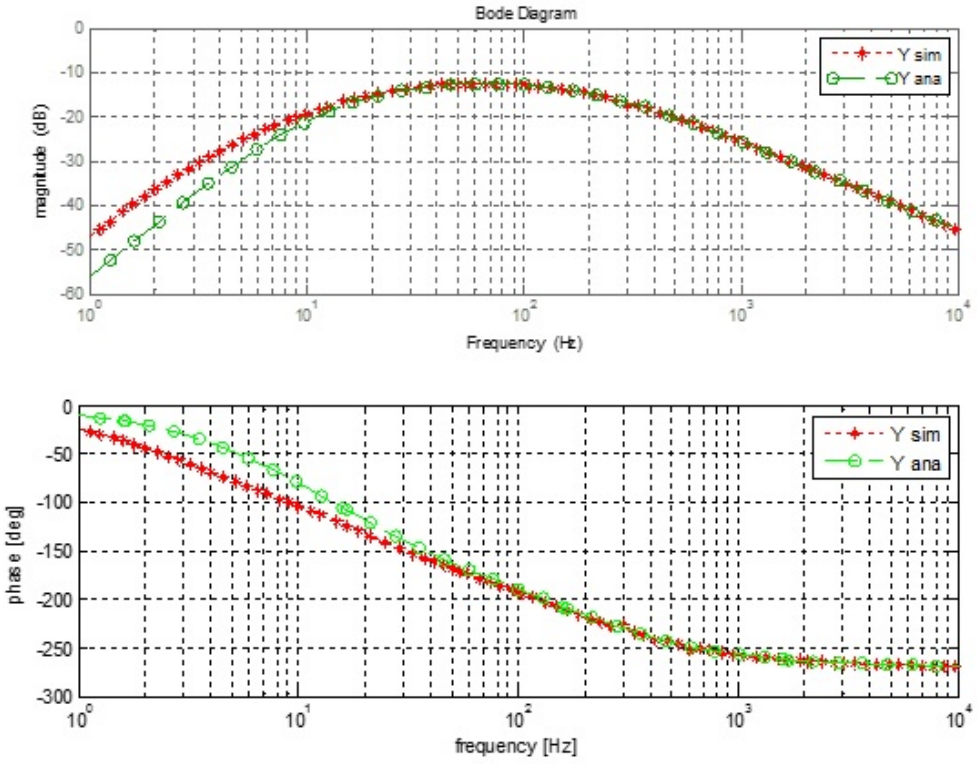

Figure 5.2: Simulation and analytical model input admittance for α_C=0.1ω_{sw}

Case III For the band width of the current controller chosen as 20% of the switching frequency

α_C=0.2ω_{sw}=2606.2 rad/s
α_F=0.1α_C=260.6 rad/s
K_p=$\alpha_C L''$=2.6
K_i=$\alpha_C R''$=130.3

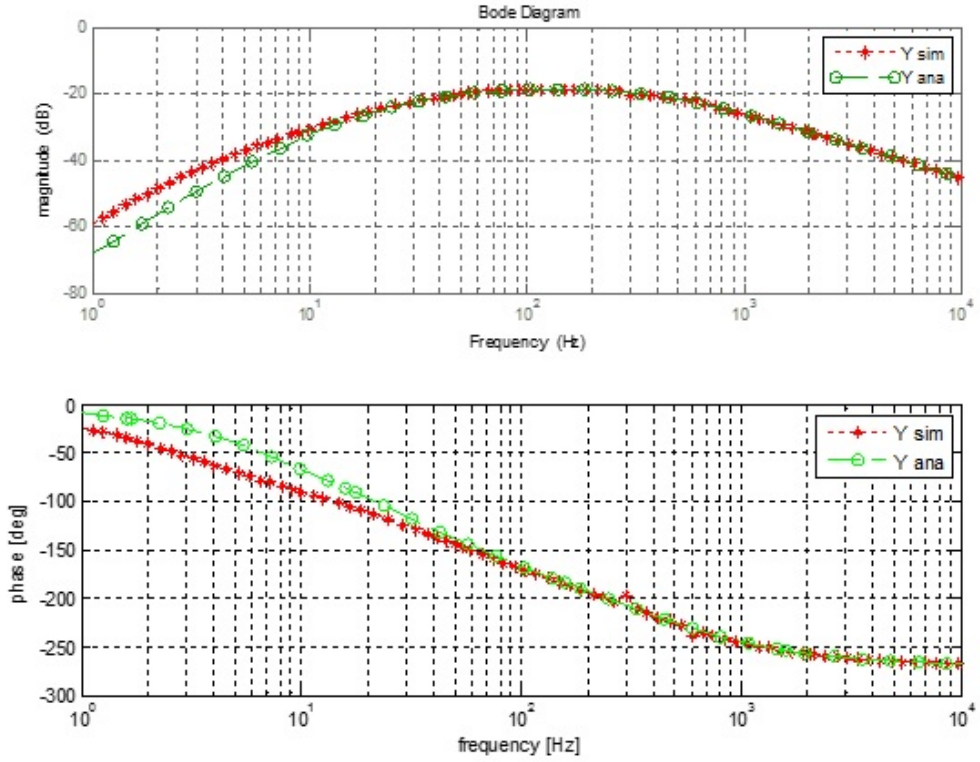

Figure 5.3: Simulation and analytical model input admittance for α_C=0.2ω_{sw}

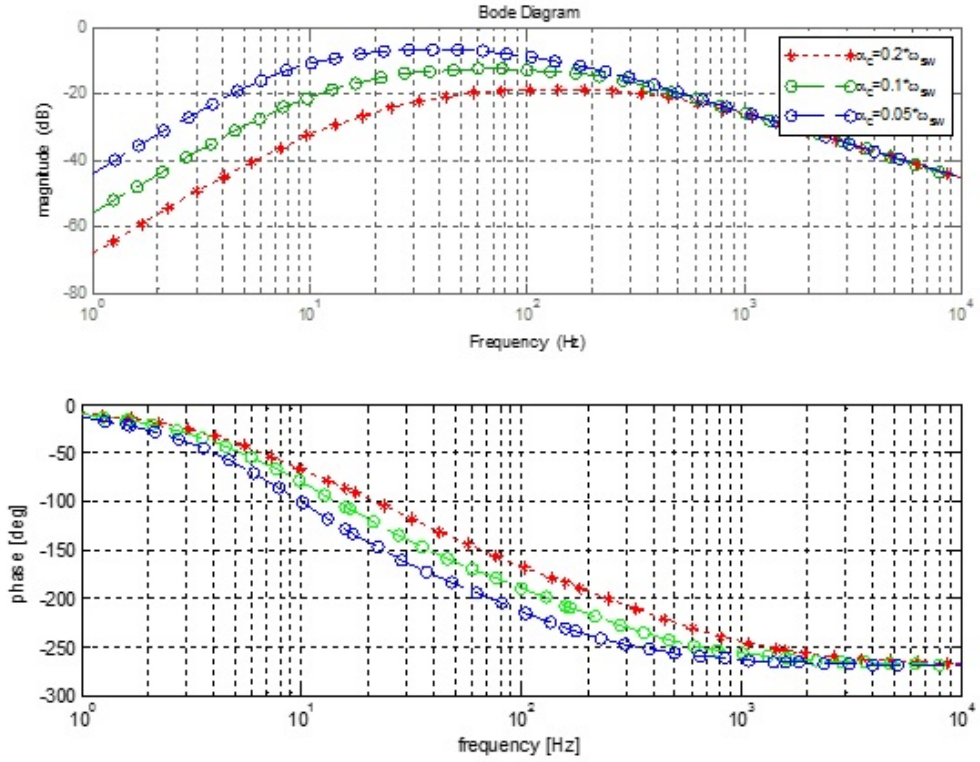

Figure 5.4: Analytical model input admittance for $\alpha_C = 0.2\omega_{sw}$, $\alpha_C = 0.1\omega_{sw}$ and $\alpha_C = 0.05\omega_{sw}$

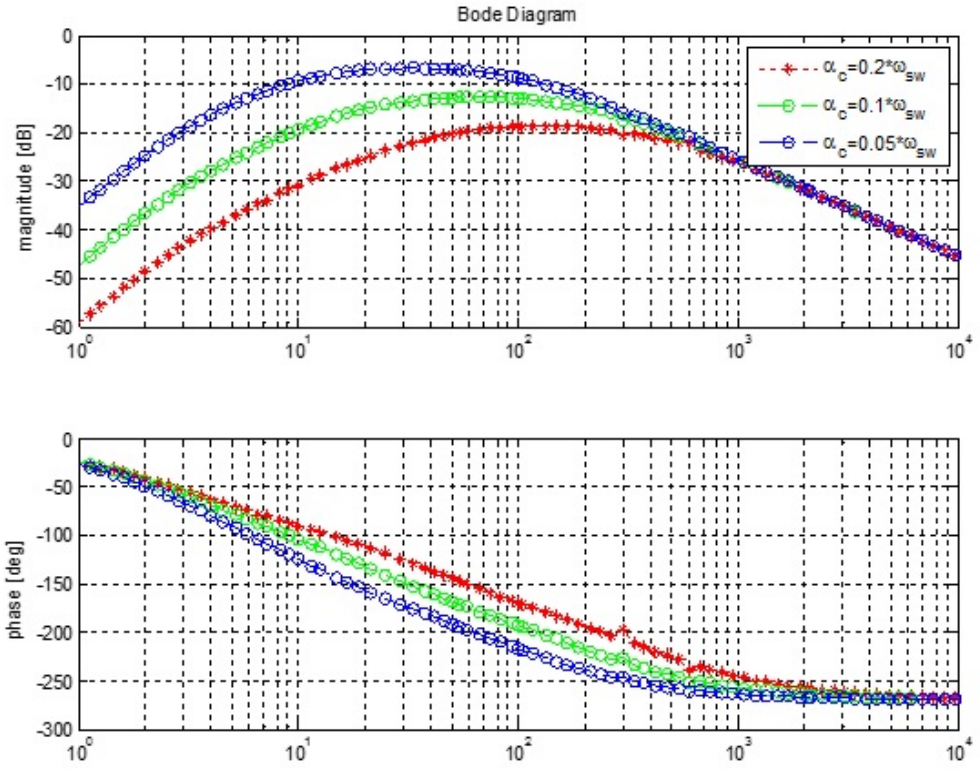

Figure 5.5: Simulation model input admittance for $\alpha_C = 0.2\omega_{sw}$, $\alpha_C = 0.1\omega_{sw}$ and α_C=$0.05\omega_{sw}$

It is found that both models have similar trend in their phase and magnitude plots with the change of α_C. As can be seen in Figure 5.4 and 5.5, both the simulation and analytical models' input admittance magnitude (gain) for higher frequency ranges do not vary regardless of the changes in α_C. Moreover, for lower frequency ranges similar behavior can be observed (i.e. higher magnitude for smaller bandwidth of α_C).

5.1.2 Effect of α_F

Three different values of α_F are simulated, keeping α_C at the base value ($\alpha_C = 0.2\omega_{sw}$). The band width of the feed forward is varied independently to be 1% (0.1 α_C), 5% (0.05α_C) and 1 (unity). It can be observed in figures of case IV- case VI (Figure 5.6-Figure 5.8), that the analytical model mimics the MMC's input admittance perfectly for all frequency ranges greater than 10 Hz, regardless of the changes in α_F. However, the input admittance of the analytical model deviates slightly from the simulated model for frequency ranges less than 10 Hz.

As can be deducted from (3.19) and (4.1), it is expected for the analytical model to vary inversely with changes in α_F. This can be easily proved by observing Figure 5.9. Moreover, as is illustrated in Figure 5.9 and Figure 5.10, with the decrease of

α_F, the input admittance gain increase for both the analytical and simulated models.

Case IV For the band width of the feed forward chosen as 1% of the current controller

α_C=$0.2\omega_{sw}$=2606.2 rad/s
α_F=$0.1\alpha_C$=$26.1rad/s$
K_p=$\alpha_C L''$=2.6
K_i=$\alpha_C R''$=130.3

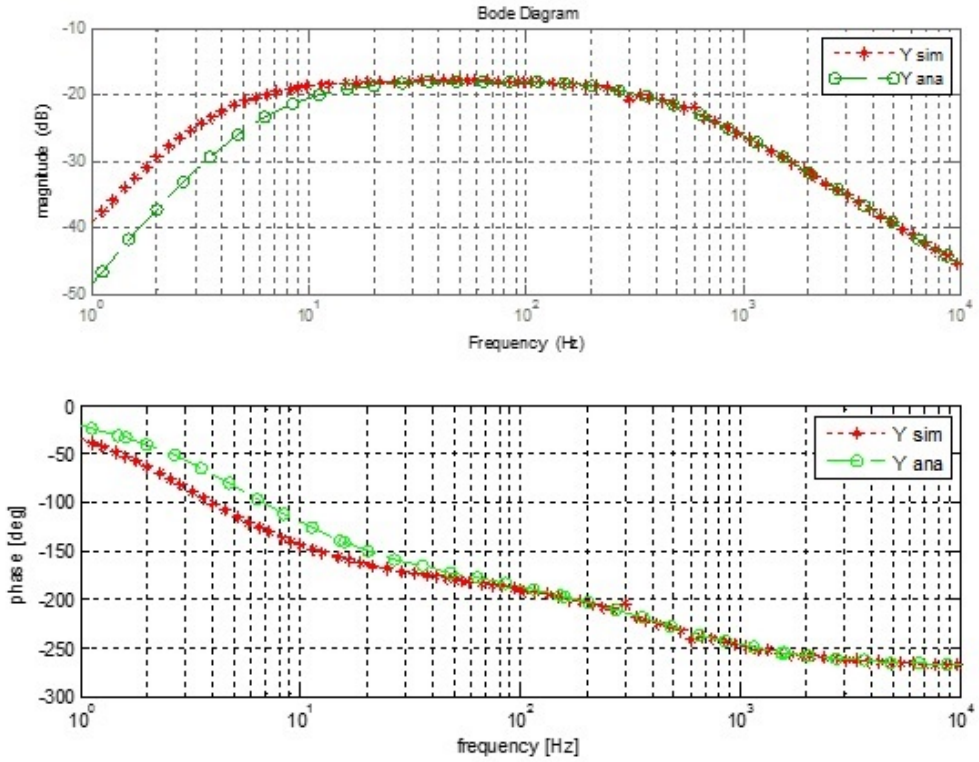

Figure 5.6: Simulation and analytical model input admittance for α_F=$0.01\alpha_C$

Case V For the band width of the feed forward chosen as 5% of the current controller

α_C=$0.2\omega_{sw}$=2606.2
α_F=$0.05\alpha_C$=130.3
K_p=$\alpha_C L'''$=2.6
K_i=$\alpha_C R'''$=130.3

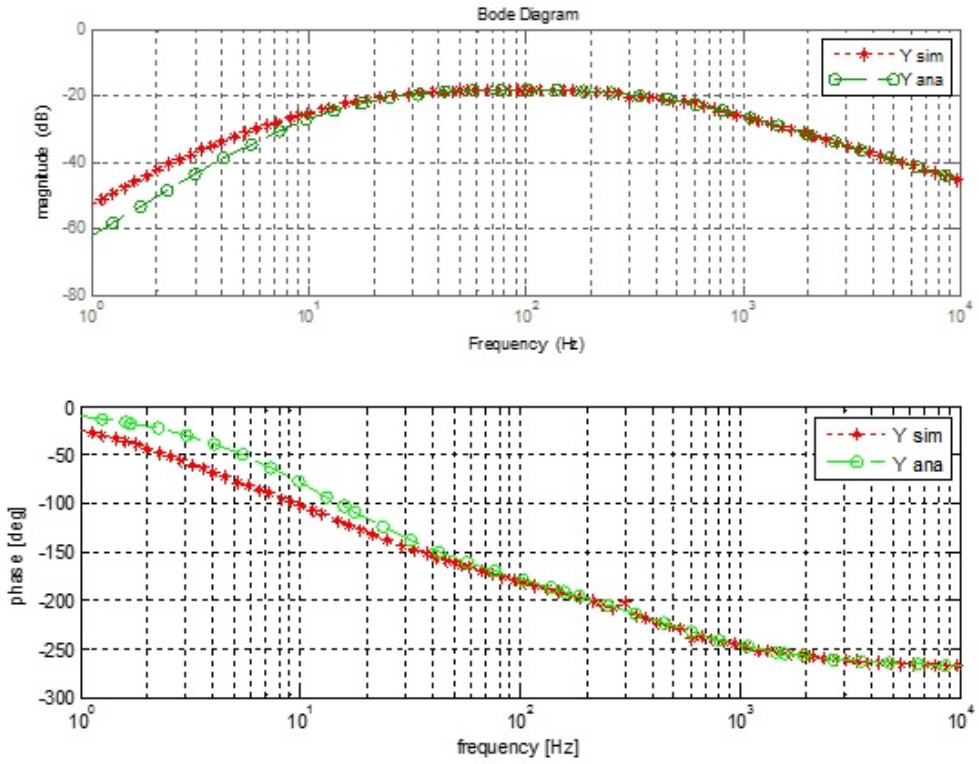

Figure 5.7: Simulation and analytical model input admittance for α_F=$0.05\alpha_C$

Case VI
For the band width of the feed forward chosen as unity

α_C=$0.2\omega_{sw}$=2606.2 rad/s
α_F= $1rad/s$
K_p=$\alpha_C L''$=2.6
K_i=$\alpha_C R''$=130.3

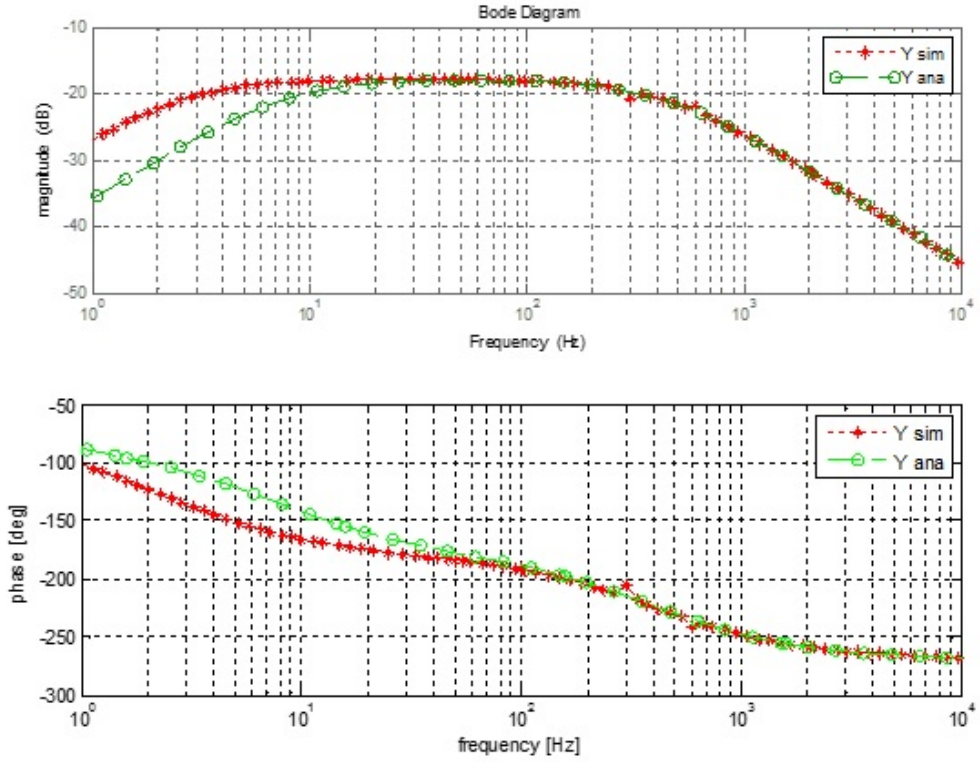

Figure 5.8: Simulation and analytical model input admittance for α_F=1

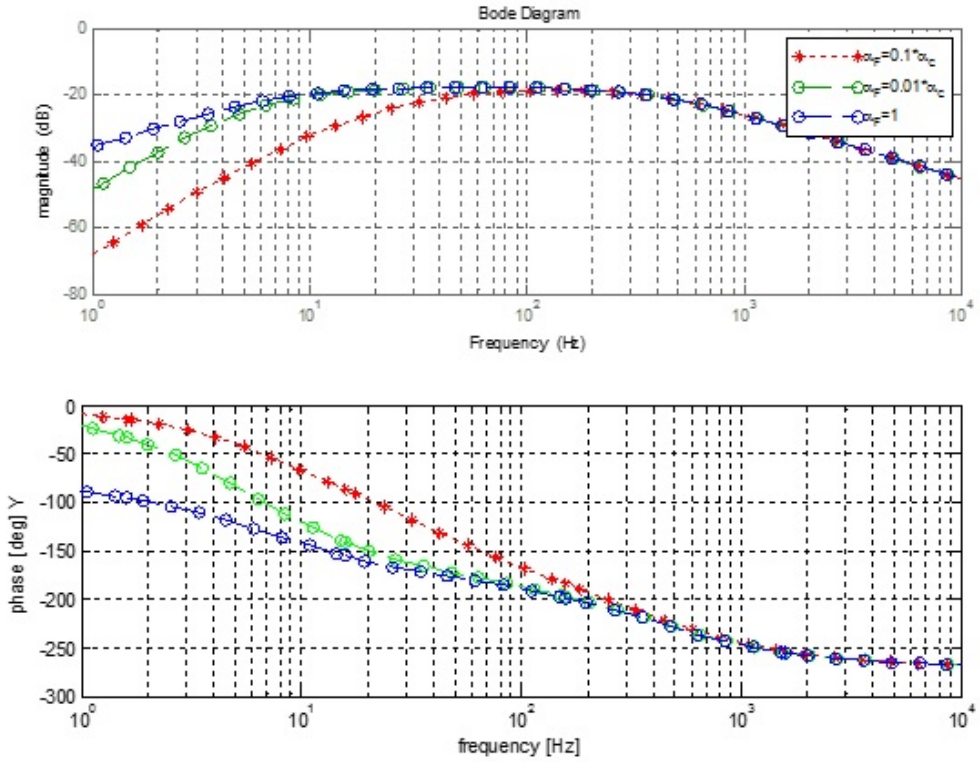

Figure 5.9: Analytical model input admittance for α_F=0.1 α_C, α_F=0.01α_C and α_F=1

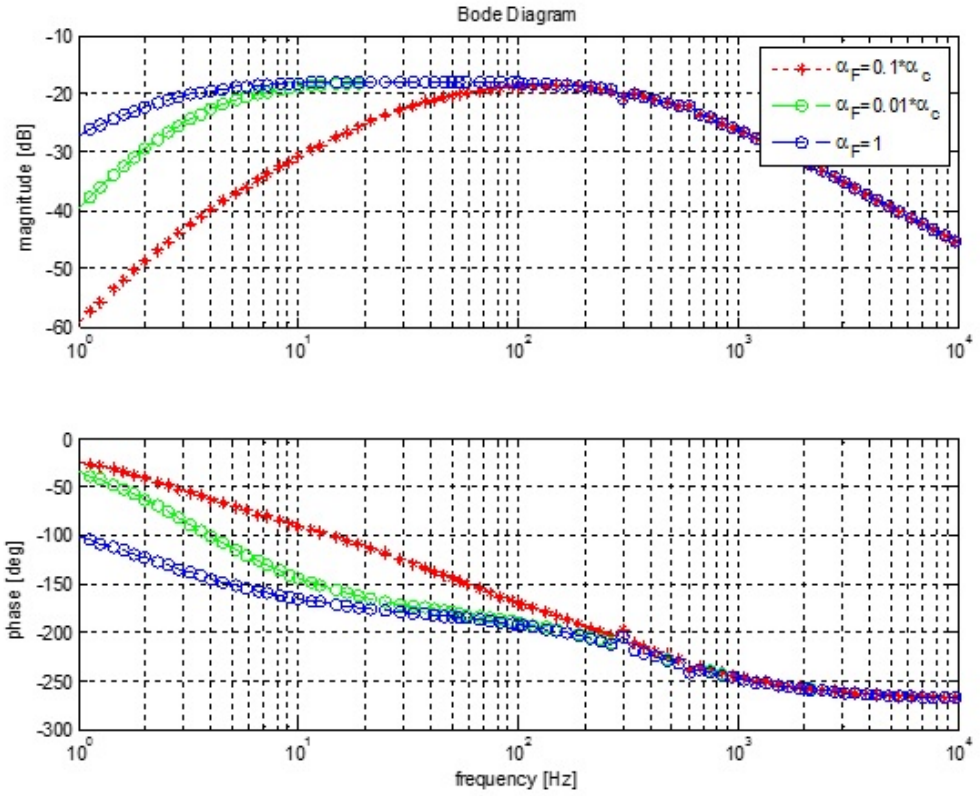

Figure 5.10: Simulation model input admittance for, α_F=0.1 α_C, α_F=0.01α_C and α_F=1

5.1.3 Effect of Switching Frequency

To study the impact of varying the switching frequency explicitly, two different values of switching frequency are analyzed. Only the switching frequency is varied separately keeping the current controller parameters at their base values (i.e. when the switching frequency is 2075 Hz, α_C=0.2ω_{sw} and α_F=0.1α_C). When all other parameters are kept constant, no change in the input admittance is expected as there are no parameters in the analytical derivations that directly depend on the switching frequency. This is mainly because the delay from the converter is ignored in the analytical derivations. Moreover, as higher switching frequency is used, the impact of switching frequency on the input admittance is negligible. In accordance with the analytical results, the simulations' input admittance also remains the same irrespective of the changes in the switching frequency. This can be easily verified by observing Figure 5.11. The results of the AC sweep analysis for the two different switching frequencies are plotted on the same figure and as can be seen, there is no change in the results regardless of the changes in the switching frequency.

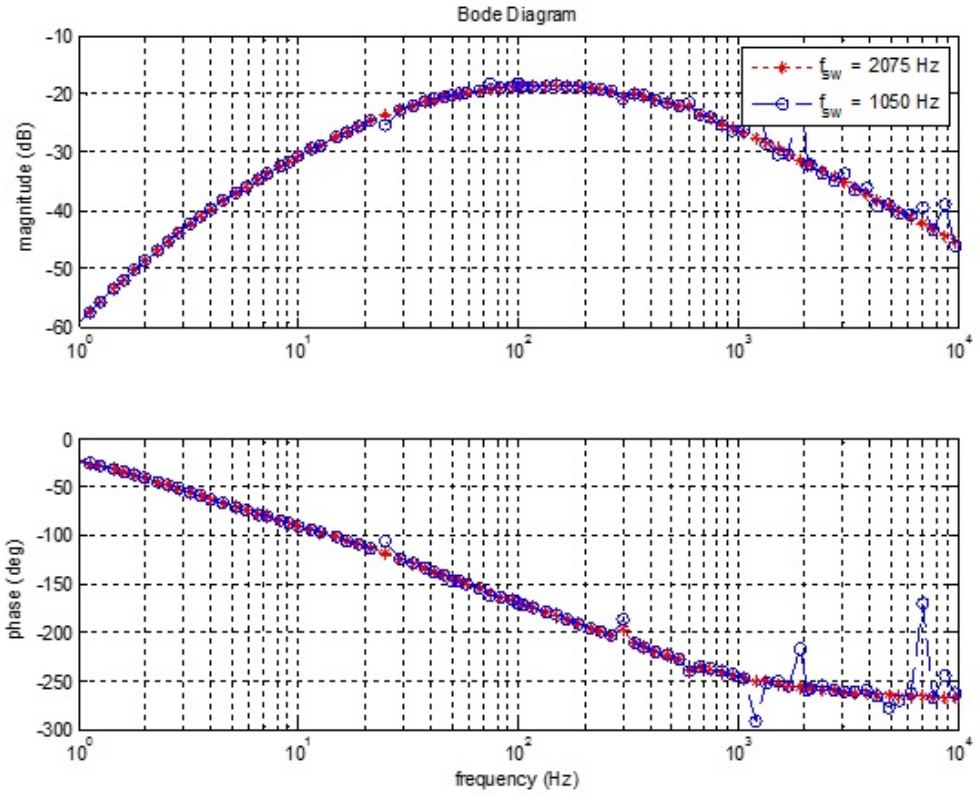

Figure 5.11: Simulation model input admittance for $f_s = 1050Hz$ and $f_s = 2075Hz$

5.1.4 $2N + 1$ Modulation scheme

In this section $2N + 1$ modulation scheme is implemented and the resulting input admittance model is compared with that of the $N+1$. To implement this modulation scheme, the phase shift between the carriers of an arm is made to be 45° ($\frac{180}{N}$) and similarly, the references of the upper and lower arms of a leg are made to be phase shifted by 180°. To prove that the modulation scheme is working as intended, the total number of inserted SM and the comparisons of the reference and measured voltages are observed. It is observed that the total number of inserted SM during a period varies in accordance with the theory in 2.3. Moreover, it can be observed in Figure 5.12 that the measured voltage is able to follow the reference voltages. As can be seen from Figure 5.13, there are no significant variations on the input admittances, when $N + 1$ and $2N + 1$ modulation schemes are used.

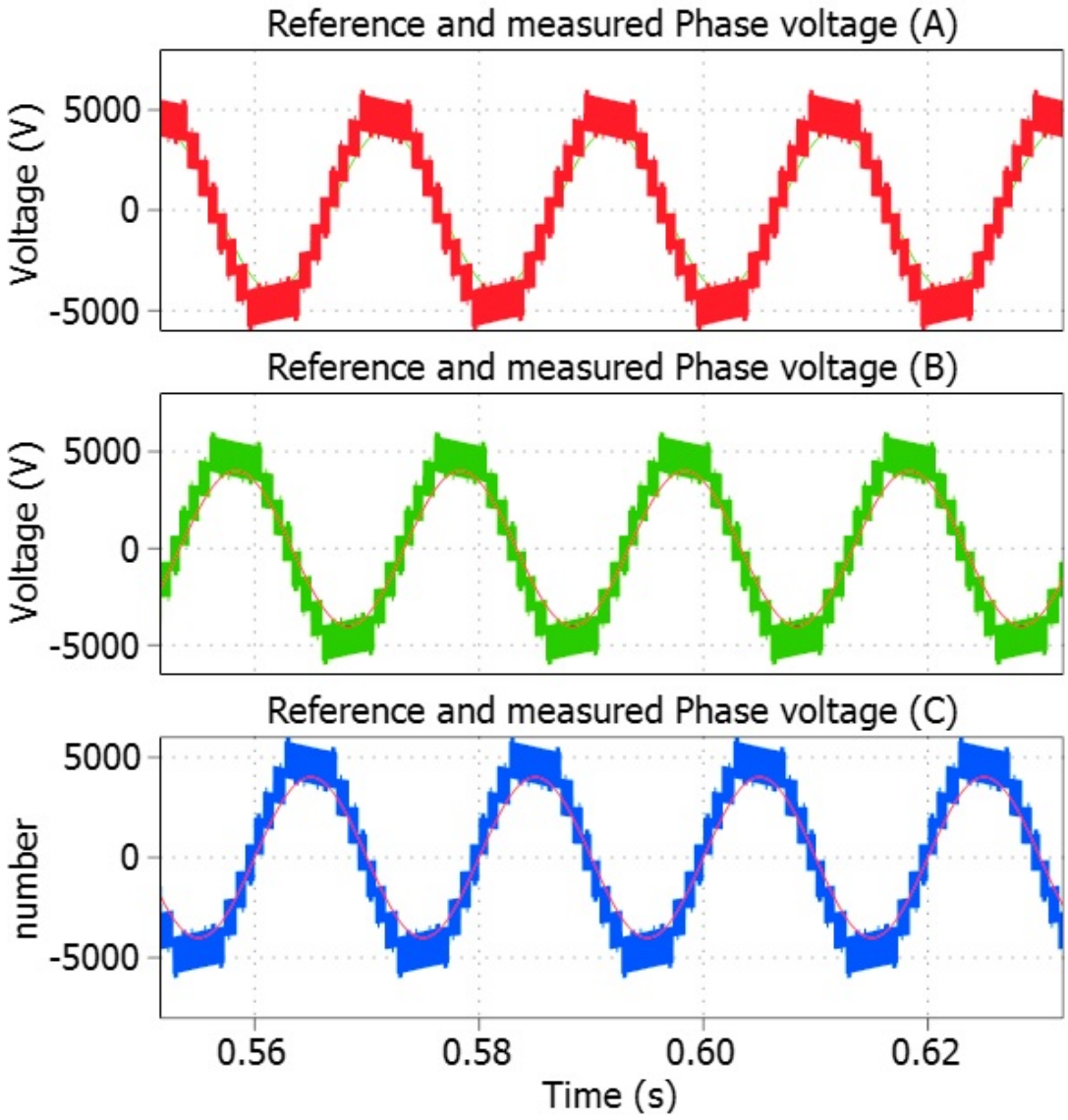

Figure 5.12: Reference and measured voltages for $2N + 1$ modulation

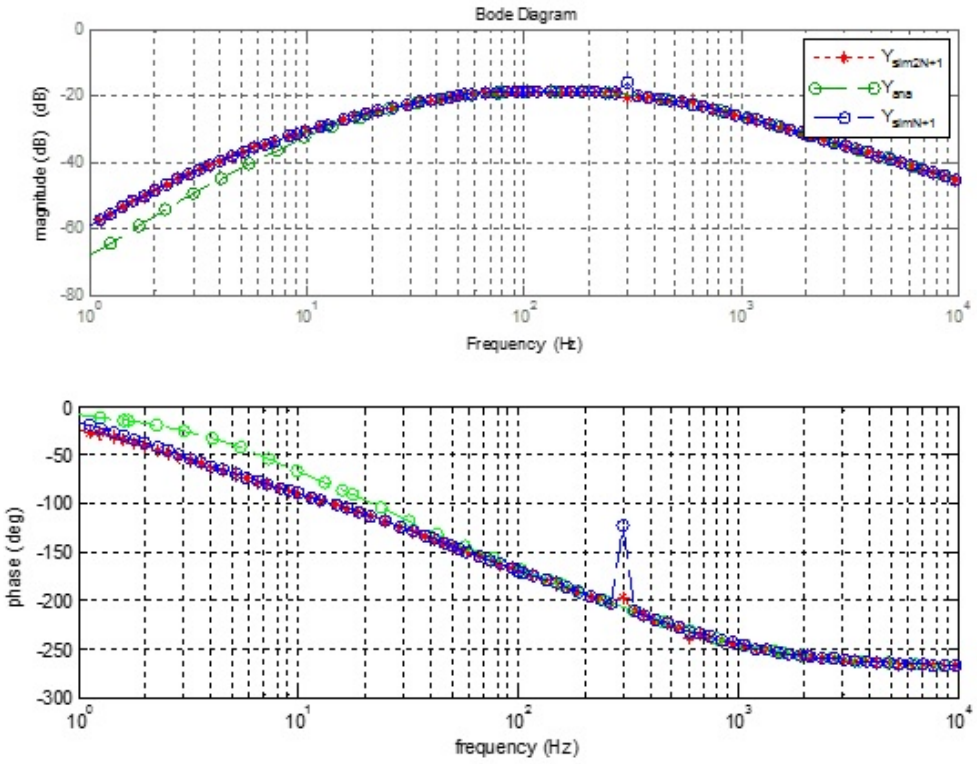

Figure 5.13: Comparison of input admittances for analytical, $N + 1$ and $2N + 1$ modulation schemes

5.2 Chapter Summary

The impact of different control parameters, switching frequency and modulation scheme, on the input admittance is studied in this chapter. AC sweep analysis is carried out for the individual case and the results are compared with the analytical model in MATLAB. It is found out that the two models (analytical and simulated) match perfectly for the entire frequency range, with exception of small discrepancy at lower frequencies (below 10 Hz). This discrepancy may be explained by computational errors due to the very small gains involved. Moreover, it is observed that the analytical model is able to imitate the simulated model regardless of the changes in the control and modulation parameters. Furthermore, it is observed in both the simulation and analytical models that the input admittance is not affected by changes in the switching frequency and modulation schemes.

6
Conclusion and Future Work

6.1 Conclusion

In this thesis work, an analytical input admittance model of MMC is derived. To verify this derived model, a five level MMC is simulated in PLECS. The simulation results from the AC sweep analysis in PLECS are then compared with the derived input admittance in MATLAB. Moreover, control and modulation parameters impact on the input admittance model of the MMC is analyzed. Besides, the input admittance expression of the MMC is compared with that of a two level converter.

For the typical system at the base values (case III), the derived and simulated models match entirely with the exception of slight discrepancy at low frequency ranges (below 10 Hz). Among all the parameters studied, it is found that the analytical model is able to mimic the simulated model regardless of the variations in the control and modulation parameters. It is also demonstrated that changes in switching frequency and modulation schemes do not affect the input admittance. Additionally, for an MMC with constant capacitor voltage assumption, it is observed that the input admittance of MMC has the same expressions as that of a two level converter (VSC) with an equivalent inductance and resistance resulting from a series connection of the arm inductor and the filter inductor.

6.2 Future Work

In this study an assumption of constant capacitor voltages is made. However, in practice the capacitor voltages are varying and it accounts for significant internal dynamics of MMC. Future works in representing the MMC with its input admittance model may include:

- the assumption of uniform capacitor voltages can be disregarded and more robust model can be derived by including the circulating current and capacitor voltage dynamics.

- in this model, only internal loops are included; however, a robust model can be designed by including the outer control loops of Alternating Voltage Control loop (AVC), Direct Voltage Control loop (DVC) and PLL dynamics.

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