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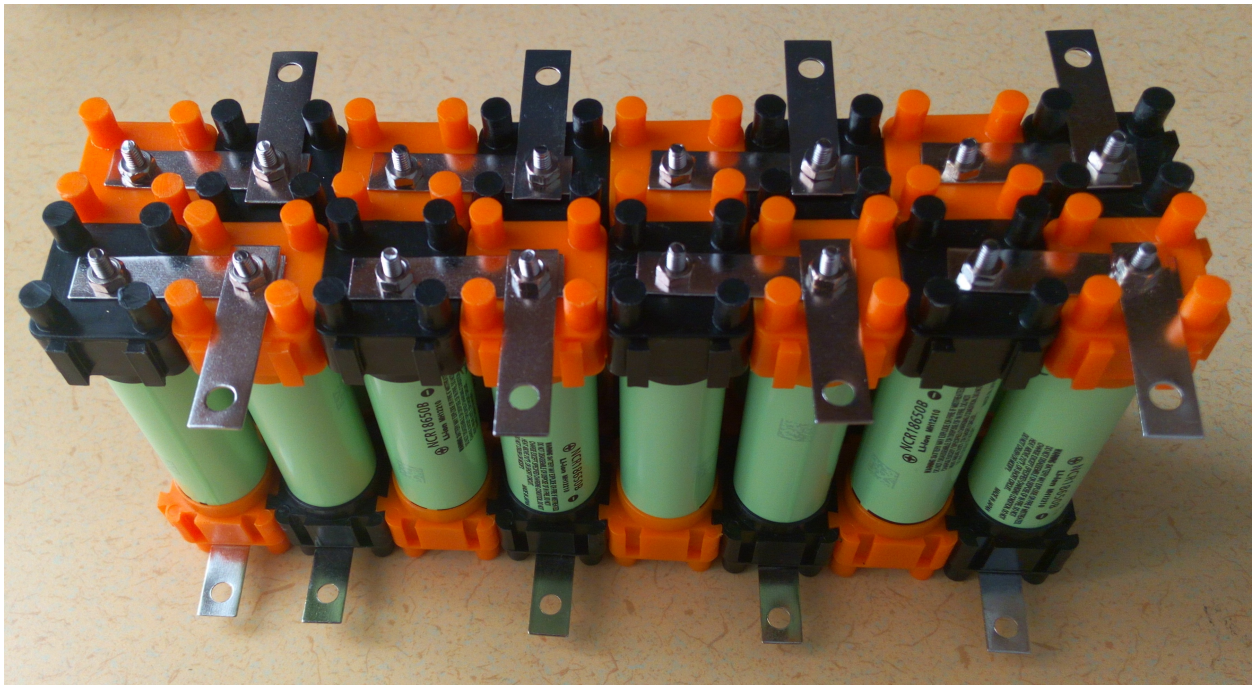

Design and Implementation of a Scalable Battery Management System

Master's Thesis in Computer Science and Engineering

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Abstract

Our society is facing significant challenges due to accelerated climatic change brought by increased carbon emissions (from cars, industries and power generation) leading to global warming. According to the 2018 Transport and Environment report on carbon emissions (CO_2 EMISSIONS FROM CARS: the facts), the transport sector is Europe's single biggest source of carbon emissions contributing 27% of the European Union's total carbon emissions with cars and vans representing more than two thirds of this percentage. Therefore, vehicle electrification is of utmost importance to provide an alternative to fossil fuel driven (internal combustion engine) vehicles. Improved technology coupled with tightened emissions legislation has continuously driven costs of vehicle electrification down making electric vehicles more accessible.

Battery electric vehicles mostly run on Lithium-ion batteries which have high battery capacity, very low memory effect and long lifetime. Battery Management Systems (BMS) primarily monitor lithium-ion cells for such parameters as voltage, current, temperature and battery states (*e.g.* state of; charge, health, function and power) to ensure that the batteries are safely utilised. Poor management of cell voltage, cell temperature or battery pack current damages the batteries and endangers the safety of vehicle users.

The major aim of this project is to design and implement a Scalable Battery Management System (SBMS) for the scalable electric drivetrain of the Generation-3 car platform prototype at Infotiv AB, Gothenburg, that allows re-usability, reconfiguration and extension rather than redesign. In this thesis, we analyse the scalability aspects of modular electric vehicle BMSs and incorporating these aspects in designing a prototype SBMS. In order to ensure a fully scalable system implementation we apply design layering. In design layering, the scalability of the BMS design is studied in the topological, functional, hardware and software perspectives. In addition to technical aspects, we also analyse the cost implications of implementing such a system.

A SBMS is implemented using a master microcontroller coordinating two module microcontrollers. Each module micro-controller controls a battery monitor, which in turn monitors eight cells. The layered design offers high flexibility not only in design and components, but also in cost estimation. The thesis is arranged as follows: it begins with introduction and theoretical sections, then design and implementation sections, and finally the analysis and conclusion sections.

Keywords: Electric Vehicle Batteries, Lithium Ion Battery Pack, Battery Management System, Cost Estimation, Scalability, Layered Design, Scalable Battery Pack, Battery State Estimation, Modular Battery Topology.

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Lastly, we want to take this opportunity to thank our family and friends for their love and support. Without their continued support, we would not have been able to finish this job.

Guhan Raj Sathyamoorthi and Talemwa Semanda Mubanda
Gothenburg, November 2019

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List Of Abbreviations

A/D Analogue to Digital

ACB Active Cell Balancing

ADC Analogue to Digital Converter

BEV Battery Electric Vehicle

BM Battery Module

BMS Battery Management System

BP Battery Pack

CAN Control Area Network

CC-CV Constant Current and Constant Voltage

CFGR Configuration Register Group

CM Characteristic Map

CMU Cell Monitoring Unit

DoD Depth of Discharge

ECM Equivalent Circuit Model

ECU Electronic Control Unit

EKF Extended Kalman Filter

EMI Electro-Magnetic Interference

HEV Hybrid Electric Vehicle

HV High Voltage

I^2C Inter-Integrated Circuit

IEP IES Education Platform

LAB Lead Acid Battery

LIB Lithium-Ion Battery

LIC Lithium-Ion Cell

LV Low Voltage

M/S Master/Slave

MCU Micro-controller Unit

MMU Module Management Unit

NHB Nickel-metal Hydride Battery

NTC Negative Temperature Coefficient

OCV Open Circuit Voltage

OV Over-voltage

PCB Passive Cell Balancing

PEC Packet-Error-Code

PMU Pack Management Unit

PTC Positive Temperature Coefficient

SBMS Scalable Battery Management System

SOA Safe Operating Area

SoC State of Charge

SoF State of Function

SoH State of Health

SoP State of Power

SPI Serial Peripheral Interface

UV Under-voltage

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1

Introduction

A Battery Management System (BMS) is a hardware and software system that ensures the proper and safe functioning of batteries in Battery Electric Vehicles (BEVs) and Hybrid Electric Vehicles (HEVs) [1]. Lead acid, nickel-metal hydride and lithium-ion batteries are the most common battery technologies used for BEV/HEV energy storage. However, most BEV/HEV manufacturers prefer Lithium-Ion Batteries (LIB) due to their higher energy and power density. Additionally, LIBs experience almost no *memory-effect*, meaning they can be charged to full capacity regardless of present charge [2]. However, Lithium-Ion Cells (LIC) are sensitive to operating conditions. They are very intolerant to over-charge or over-discharge and cannot be charged safely beyond a certain temperature range [3]. If LICs operate outside proper charge/discharge conditions, this can cause thermal run-away that can result in explosions or permanent damage to the cell. In this regard, a BMS enforces maximum charge or discharge currents and voltages at various temperatures to achieve the following objectives: maximise cell and battery lifespan, increase energy efficiency for extended driving range, and improve safety of the battery system. The necessary voltage, current, and temperature conditions for LIC/LIB operation are referred to as its Safe Operating Area (SOA) [4].

The BMS uses various sensors to measure Battery Pack (BP) current, cell voltages, and temperature at various BP points, in order to maintain battery SOA [5]. The BMS performs battery state estimation, and battery system information logging, in order to improve system efficiency [6]. Furthermore, it handles internal communication of its sub-components and external communication with other vehicle sub-systems. The BMS also performs cell balancing to equalise the charge on series-connected cells in the BP to prolong battery life [7]. It also controls several actuators to restore SOA, *e.g.* fans or refrigeration sub-systems (to cool the battery), and relays/switches (to control current flow). It also promotes overall battery system safety by ensuring that proper *galvanic isolation* is maintained, to prevent high voltages (usually 300–600 V) and currents (usually > 80 A) of the BP from damaging BMS control circuitry and other vehicle systems, or harming users [5].

During operation, BMS sensors measure the instantaneous current and voltage at various temperatures in different operating conditions. Certain parameters (such as the remaining battery capacity) are difficult to measure accurately while the battery is in use. Additionally, sensor measurements may contain errors introduced by electrical noise in the vehicle systems. Therefore, the BMS performs estimation using several methods based on different battery parameters to calculate the battery state [8]. For better state estimation, the BMS controller stores information about both the battery and system parameters. Besides internal sensory data, the BMS also receives data from external vehicle subsystems for improved battery modelling and state estimation. This data may include environmental temperature, current vehicle speed, and vehicle travelled distance [3].

BEV energy management technologies must promote safety and be environmentally friendly. In modern BMSs, an emerging trend is to monitor each cell in the battery to improve both safety and efficiency [9]. The *smart cells* have cell monitoring capabilities integrated together with the cell [3, 9]. One advantage of this approach is that safety of the overall system is maintained given that each cell is kept in SOA. Given that BEVs are expected to have such a high proliferation, the *second life* opportunities of such cells are much higher since all battery state information is stored together with the cell [9]. However, decentralisation of battery management to the cell level poses a scalability challenge. Increased per-cell monitoring functionality leads to rapid increase in complexity and subsequent development cost of BMS due to the substantial increase in the number of components. A more scalable approach is to divide the battery into modules. Modular BPs can easily scale without high increase in complexity since most SOA supervisory circuitry is confined to the module for a number of cells. The capacity of modules in a BP depends on the manufacturer and the vehicle's energy needs.

The BMS is usually designed to satisfy specific goals such as longer drive-range or fast-charging [10]. This leads to use of specific technologies such as communication standards. In order to fulfill requirements for a new system, the designer has to change both software and hardware. This leads to long design time and higher costs. BEVs consist of several *mechatronic* systems that require physical testing in the real-world for satisfactory results. Often BEV technologies are tested on prototype vehicles. Currently, the cost of building new prototype vehicles whenever testing scope changes can be quite high, whereas implementing changes to an existent design may unnecessarily increase complexity.

1.1 Motivation and Problem Statement

In order to fulfil client's requirements for BMSs, the designer has to change both software and hardware. This leads to long design time and higher costs. Therefore, to combat such challenges, a *scalable* BMS (SBMS) design allows re-usability and extension of current design instead of redesign. This provides flexibility while minimising design costs.

Infotiv AB is developing a scalable drivetrain for a model electric vehicle platform called IES Education Platform (IEP). The electrical drivetrain shall be scalable to support future development projects. To support the scalability of the drivetrain, implementation of an equally scalable BMS that *powers* it is paramount.

1.2 Purpose

There are several BMSs in use in BEVs today with many vehicle manufacturers employing custom solutions. Such BMSs cater to the requirements of particular vehicles. However, in this research we investigate implementation of a more flexible and scalable solution. We seek to answer a major question: *How can we implement a BMS for the IEP that can be easily scaled to other vehicles?* We attempt to answer this question with the following project objectives:

- Carry out a survey of current BMS designs to find out the requirements for designing a scalable BMS for BEVs/HEVs. Firstly, this will provide a deeper understanding of the factors that influence design of existent BMSs. Secondly, it will provide an understanding of the scalability requirements/considerations.

- Design and implementation of a SBMS based on the afore mentioned considerations according to the requirements from Infotiv AB. The SBMS design must demonstrate flexibility to support the IEP drivetrain and other vehicle types depending on their requirements.
- Analyse the resultant SBMS design and implementation in relation to the above two objectives. Demonstrate that its not only possible to implement a SBMS, but also affordable compared to a non-scalable alternative.

1.3 Thesis Structure

Chapter 2 gives the theoretical background to BMSs. It presents the properties of different cells, battery models, BEV BP structure, functions and requirements of the BMS, BMS topologies and scalability considerations for BMS development.

Chapter 3 looks at the design of the SBMS. It begins by describing the arrangement of project delivery activities, and continues to the overall system design, then further elaborates on the system design according to the topological, functional, hardware and software perspectives.

Chapter 4 talks about the implementation of the SBMS design. It presents a detailed explanation of the hardware design by describing the required hardware components and their specifications. Then, it describes the different software routines and management functions performed.

Chapter 5 presents the experimental setup and testing of the SBMS. It shows the setup of different hardware units and results obtained from testing both the hardware and software.

Chapter 6 presents an investigation of the design, implementation and experimental results in comparison with the theoretical concepts. It also presents a discussion on the scalability and cost analysis of the SBMS design.

Chapter 7 presents a summary of achievements of the project. In addition, it also presents suggestions of future improvements to the designed system.

2

Batteries, Battery Management Systems and Scalability

BMS is a wide topic encompassing several disciplines, however, in this chapter we cover some of the major aspects of BMSs concentrating on Battery Electric Vehicle (BEV) and Hybrid Electric Vehicle (HEV) battery systems. The first section discusses battery cells and their chemistry, mainly focusing on lithium-ion cells (LICs). The second section talks about physical arrangement of batteries and hardware components within a vehicle battery pack (BP). The third section talks about the BMS hardware and software. It focuses on the BMS requirements, functions, and topology. It further looks into the battery state estimation and modelling techniques used to manage batteries. The last section discusses the scalability and reconfigurability considerations for designing a Scalable Battery Management System (SBMS).

2.1 Battery Electric Vehicle and Hybrid Electric Vehicle Cells

There are several rechargeable battery types suitable for different applications. Different battery types have different properties and, therefore, exhibit differing performance characteristics. The most common battery technologies in BEVs/HEVs are Lead Acid Batteries (LABs), Nickel-metal Hydride Batteries (NHBs) and Lithium-Ion Batteries (LIBs). NHBs together with LIBs are the two leading types of batteries used in electric vehicle market to-date. BEV/HEV battery developments have a high emphasis on higher energy densities (to increase electric-driving range), safety, lifetime, reliability, and costs [11].

2.1.1 Lead Acid Battery

The LAB dominates the global rechargeable battery market to-date due to; low cost of raw materials, mature and cost-optimised manufacturing, robustness, low-temperature discharge power and heat tolerance. However, their use for BEV/HEVs is limited by: the relatively low specific energy and power, a low deep-cycle life, limited charge acceptance, and acid stratification and sulfation. Acid stratification and sulfation rapidly reduce LAB performance (when kept at low charge) and may result in permanent damage [12].

2.1.2 Nickel-metal Hydride Battery

NHB are predominantly used for the high-power, wide operating temperature range HEV applications due their ability to hold far more energy, offer much longer life cycle and lighter

weight when compared to LABs [13]. They can also deliver rapid power burst. However, the battery's cycle life reduces with repeated rapid discharges of high load while delivering rapid power burst. Therefore, this type of battery is more suitable for HEVs rather than BEVs since HEVs typically experience deep discharge cycles. NHBs also have a high self-discharge rate and suffer from *memory effect* [14].

2.1.3 Lithium-Ion Battery

LIC are preferred cell for BEV due to their higher energy density and voltage compared with NHB. Higher voltage allows connecting fewer cells together in series resulting in a lighter BP. LICs also have a lower rate of self-discharge and much better cycle life than NHB [13]. However, LIBs are more expensive to produce and operate since they require monitoring circuitry.

The LIC anode and cathode are separated by an electrolyte that is electrically isolating but can conduct Li^+ ions (Figure 2.1). When a load is connected to the battery, the electrons are transported from current collector at the anode, through an outer circuit to current collector at the cathode. The Li^+ ions are transported from the anode material to the cathode material through the electrolyte. Depending on which materials that are used in the anode and cathode, the cell will have different characteristics. Cells are usually limited by the cathode material, which sets the bounds for cell power and capacity [15]. The key requirements for considering materials that determine the battery's performance include; safety, manufacturing costs, lifetime stability, energy density, power density, and State of Charge (SoC) operating range.

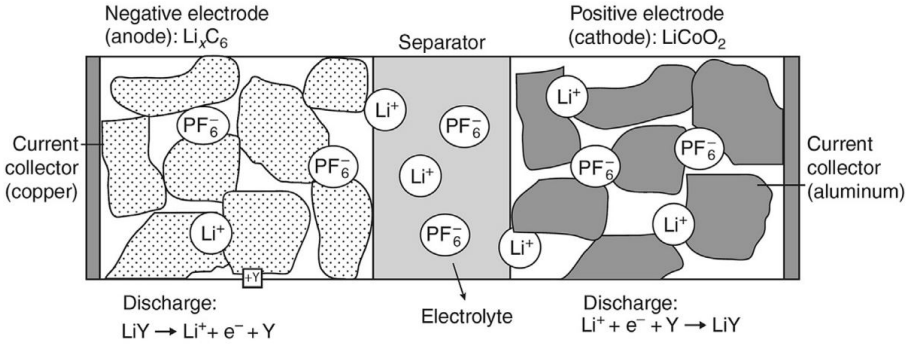
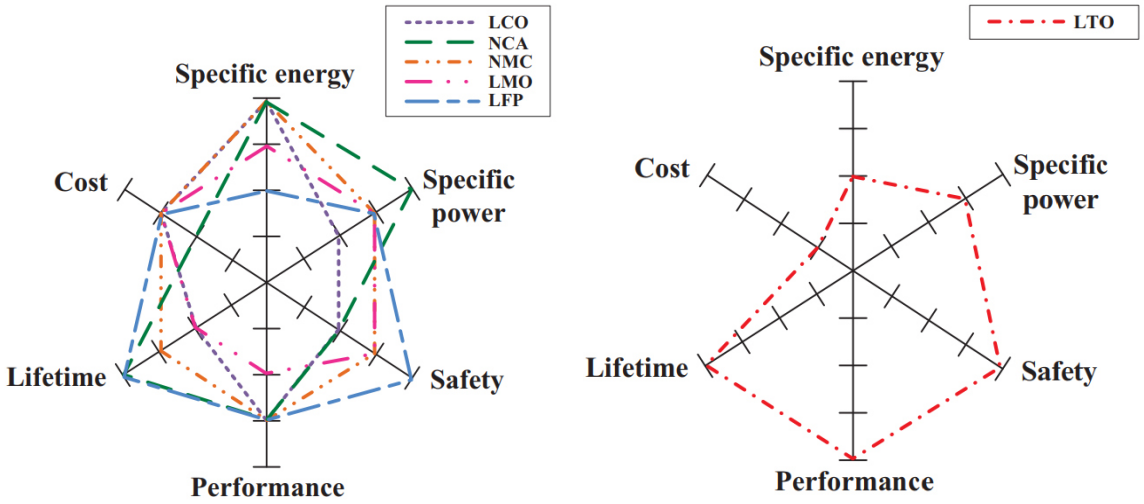


Figure 2.1: Lithium-Ion Cell Design [16]

Since no cathode material completely fulfils all BEV requirements, LIC electrodes in BEVs/HEVs usually use a mixture of different cathode and anode materials to complement the advantages and disadvantages of the respective materials. The most common cathode materials include: Lithium Cobalt Oxide (LCO), Lithium-Nickel-Cobalt-Aluminium (NCA), Lithium-Nickel-Manganese-Cobalt (NMC), Lithium-Manganese-Spinel (LMO) and Lithium-Iron-Phosphate (LFP). Anode materials include natural graphite, synthetic graphite, hard carbon, and Lithium Titanate (LTO) [11]. Figure 2.2 shows a comparison of the different materials according to the main BEV requirements of: safety, cost, lifetime stability, energy, performance and power density [17].

Different materials may be preferred for different applications. For example, NCA cells are preferred for BEV cars due to their high energy, but are less safe because they are more prone



(a) Various cathode materials

(b) LTO-based anode material

Figure 2.2: Requirements fulfilment of cell technologies [17]

to thermal runaway. LFP cells offer less energy and are preferred for household electronic appliances since they are less prone to thermal runaway and therefore are more safe. LTO and LFP cells may be preferred for use in electric buses in urban centres because they support deeper discharge cycles enabling the use of fast charging stations [18].

2.1.4 Cell Geometry

Battery cells are also differentiated by their geometry/format. Cell geometry has major influence on the design of BP housing, the cell interconnection system, and other components such as the cooling system [19]. There are three major types of cell geometry: cylindrical, prismatic and pouch cells [4, 19, 11].

In cylindrical cells, the anode, cathode, and separator are rolled up and sealed in a battery canister with an electrolyte [20]. The standard format for cylindrical LICs is 18650-type cells (18mm diameter, 65mm high). Recently, higher capacity 21700-type format (21mm diameter, 70mm high) has been adopted by industry [21]. The prismatic and pouch cells consist of stacked layers of anodes, separators, and cathodes sandwiched in between layers of the laminated film, however, prismatic cells have a hard-case housing [20]. The size of prismatic and pouch cells usually depends on the application.

2.2 Battery Packs and Modules

BEV/HEV BPs usually consist of several Battery Modules (BMs) as their primary components. These BMs output a relatively low output voltage usually less than 60 V that can be handled without any special precautions [5]. The modules are connected in series/parallel and monitored by the BMS. Figures 2.3 and 2.4 show schematic diagrams of the battery module and BP components respectively.

The BP is fitted with a *switch box* that contains high-voltage switches, contactors, and fuses that, when necessary for safety, disconnect the battery from the rest of the High Voltage (HV)

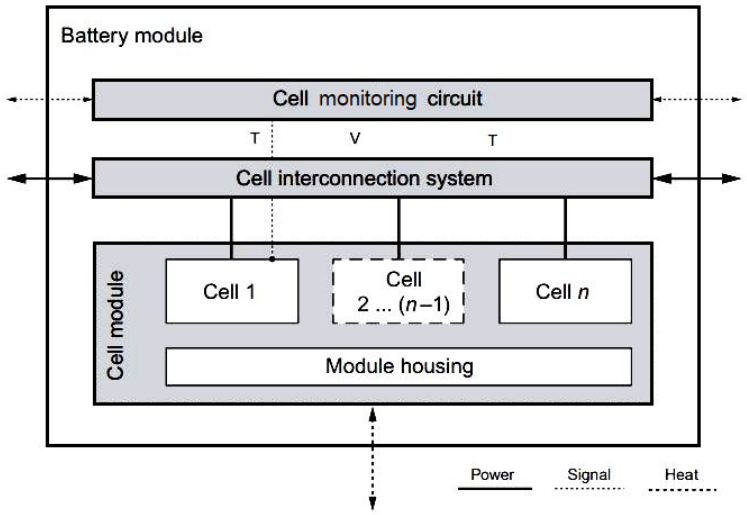


Figure 2.3: Schematic Diagram of battery module Components [5]

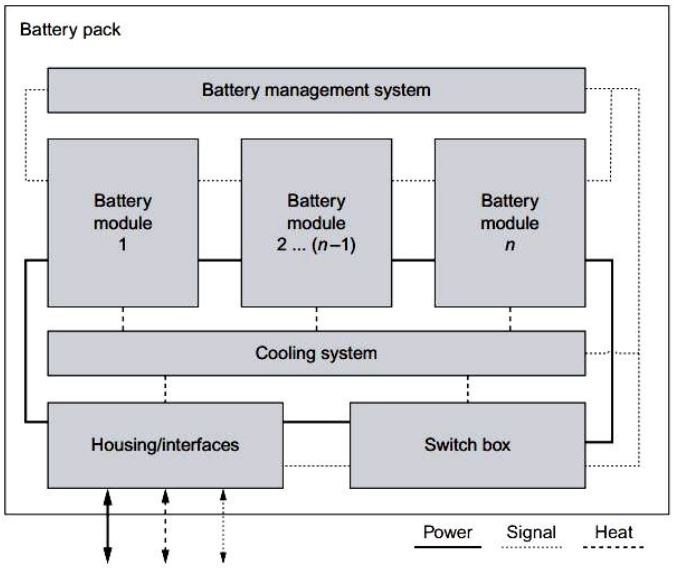


Figure 2.4: Schematic Diagram of BP Components [5]

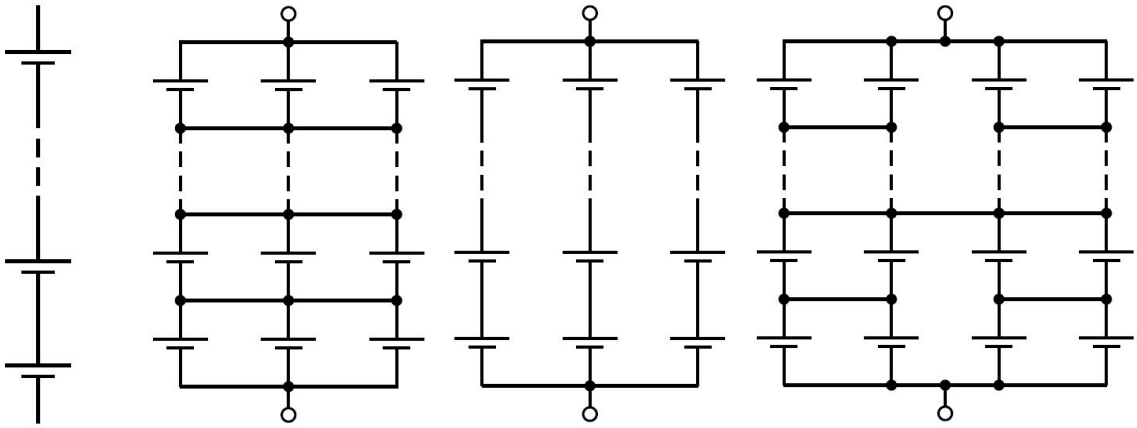
system. The power supply and communication interface of components/units that come in direct contact with the HV lines in the BP have to be *galvanically* isolated from the rest of the pack to avoid short-circuits or loss of insulation.

A cooling system maintains cells in safe operating temperature. The BP and its components are securely fitted onto the vehicle's body and enclosed in a housing that protects it for the entire vehicle life span. The housing provides mechanical strength and stiffness to support the BPs. It also contains all interfaces to the vehicle, such as the HV plugs, communication, and cooling interfaces.

2.2.1 Battery Configuration

There are various battery configurations of series (S) and/or parallel (P) cell connection (see figure 2.5) of cells in BPs [5, 22]. The type of battery configuration used may depend on the application requirements.

Connecting cells in series increases voltage but keeps capacity constant while connecting cells in parallel increases capacity but maintains the voltage [4]. For example, `8S` or `8S1P` (eight cells in series), `4S2P` (four cells in series, two cells in parallel) and `2S4P` (two cells in series, four cells in parallel) configurations all contain 8 cells but their respective BPs deliver different voltage and capacity [23, 4].



(a) Series **(b)** Fully Parallel **(c)** Parallel Batteries **(d)** Mixed

Figure 2.5: Battery Configuration Types [11, 4]

The fully parallel and parallel battery configurations are the most common configurations [22]. However, the two configurations lead to differing BP behaviour. In fully parallel, if one of the cells develops a soft short-circuit, the BP remains functional with a lower terminal voltage. However, in case of a short circuit in a cell in a parallel batteries configuration, the entire string cells are forced to operate at a higher voltage [22].

The fully parallel configuration is preferred over parallel battery configuration to improve BP robustness by reducing the parts count and the effects of cell-to-cell variations, resulting in a less expensive, more reliable, and better performing battery. With batteries in parallel, replacing defective batteries may seem safer but increases cost, introduces high inrush currents due to difference in battery voltages, and longer time to balance the new and old batteries [4].

2.2.2 Sensors

BMSs in BEVs usually measure cell and BP voltage, cell and/or BP temperature and BP current [4]. There are two ways of measuring cell voltage and temperature: distributed (one circuit per cell) or localised (a circuit shared among various cells). Since the cell temperature changes more slowly than voltage, it is common for the voltage measurement to be distributed and the temperature measurement to be localised.

Good voltage measurements are done using a decent Analogue to Digital (A/D) converter (typically 10–12 bits) [4]. Higher resolution of A/D converter measurements experience higher

noise which should be filtered out to maintain accuracy. BP voltage measurement may be added to identify faulty slave boards in a master/slave BMS (see sub-section 2.3.3.2) [3].

Common temperature sensors for the measurement of temperatures in BMS applications are of Negative Temperature Coefficient (NTC) or Positive Temperature Coefficient (PTC) types [24]. As temperature rises, the resistance of the NTC thermistor decreases while that of the PTC thermistor increases. In both thermistor types a temperature measurement is realised by capturing the voltage drop while a constant current is flowing. NTC and PTC thermistors provide high accuracy for automotive range temperatures (*i.e.* -40–125 °C) at low cost and complexity. Achieving similar accuracy with thermo-couples may require more complex electronics [24].

BP current sensors can be divided into two categories *i.e.* galvanically connected (*e.g.* shunt resistor current sensors) and isolated/contactless (*e.g.* Hall effect current sensors) [24]. Table 2.1 shows a comparison of the shunt based and Hall effect current sensors.

Sensor Type	**Hall Effect**	**Shunt Resistor**
Voltage Isolation	Yes	No
Output Offset	Yes	No
Cost	High	Medium
Susceptibility to EMI	Medium	Low
Linearity over measuring range	Poor	Good
Saturation/hysterysis	Yes	No

Table 2.1: Comparison of Hall Effect and Shunt Resistor Current Sensors [3]

2.2.3 Battery Pack Design Requirements

The design of the battery pack is highly influenced by the requirements of the BEV. These requirements can can be classified into four categories: mechanical, safety, service and cost requirements [5].

Mechanical requirements are generally covered by the battery housing/casing. It defines integration of battery modules, thermal management system, electrical and communication interfaces. A few of the important BEV requirements are: 1) BP must withstand crash loads, 2) the housing has to be as light as possible, 3) the housing should also protect the battery from corrosion, chemical, fire or road debris, and intruding objects, and 4) the BP must have proper isolation.

Safety requirements are directly linked to the mechanical requirements. Safety requirements are usually derived from development processes according to automotive standards.

Service requirements deal with exchange components in the BP. They also define how the maintenance activities should be carried out on the battery ensuring long battery lifetime while maintaining the battery in good condition for second-life applications.

Cost requirements ensure that the total BP cost is kept low. Considering the relatively high cost of LICs compared to other cell types, it important to keep the overall cost of other BP

components low.

2.3 Battery Management Systems

A BMS generally refers to any system responsible for the supervision, control, and protection of battery cells, either individually or connected to form battery systems. In modern BEVs/HEVs, BMSs are the main safety guard of a battery system for BEVs that ensure reliable and safe operation of battery cells connected to provide high currents at HV levels [3]. This section presents the requirements for design of good BMS. Then, it discusses an overview of BMS functions and topology. Finally presents a deeper study on the state estimation functionality and how the BMS models the battery to improve battery management.

2.3.1 Design Requirements

The first considerations when designing good battery systems for BEVs/HEVs is identifying and recording all requirements arising from the overall vehicle's type, design, and the environment in which it is to be operated [19]. The stringent operating conditions of LIBs and objective functions of the BMS, lead to a group of requirements that have to be met to achieve good BMS design [3].

2.3.1.1 Data Acquisition

Accurate measurement of battery parameters is of high significance. Typical accuracy is about 0.5–1.0% for voltage and current measurements [3]. Achieving longer battery life-time requires maintaining at most a 2–5 °C temperature difference among cells [25]. Additional parameters or values of supplementary sensors (*e.g.* humidity sensor) inside the BP or other application parameters (*e.g.* speed, power, environmental conditions) are also acquired using analogue or digital I/O.

2.3.1.2 Data Processing and Storage

The BMS carries out estimation of several battery states such as SoC, State of Health (SoH), State of Function (SoF) and State of Power (SoP). State parameters are calculated from battery parameter values by preconditioning or use of complex algorithms and models [3]. In addition to calculating battery state, the BMS processes external information from other vehicle subsystems as well as providing these systems information for user information or further processing.

2.3.1.3 Communication and Data Transfer

A BMS communicates with other embedded control systems of the vehicle or the application, off-board and on-board [3]. Transmitted information may include battery state information (*e.g.* SoC, SoH) or predictions (*e.g.* available power), while the vehicle may provide additional parameters to the BMS (*e.g.* environmental conditions, power requirements, location data) from external vehicle systems (*e.g.* that monitor or control remote sensors, actuators, displays, safety interlocks, and other actors).

2.3.1.4 Electrical Management

The electrical management is responsible for controlling the charge/discharge current and voltage based on the calculated battery states (*e.g.* SoC, SoH) and other input parameters [3]. In addition, electrical management equalises individual cell voltages. Further more, electrical management provides robustness against Electro-Magnetic Interference (EMI) [24] and ensures proper electrical isolation of HV from Low Voltage (LV) circuitry.

2.3.1.5 Thermal Management

Thermal management system in the BMS compensates for temperature gradients among cells to ensure that cells operate at relatively the same temperature. This is achieved through cooling or heating of the cells to restore optimum Safe Operating Area (SOA) temperatures. Operating cells within the required temperatures prevents thermal runaway and increases battery lifetime [3]. The cooling/heating system can be air-based (fans and heat sinks) or liquid-based (cooling fluid).

2.3.1.6 Safety Management

The BMS minimises the risks associated with the operation of LICs in BPs; supervision of battery voltage, current, and temperature protects cells from operating outside SOA [3]. Safety management ensures proper insulation of the vehicle HV from the user [24]. In addition, safety management also commences emergency shutdown of the BP in case of a crash.

2.3.2 Functions

The core concern of the BMS is to ensure that batteries are in proper operating condition. In BEVs, this concern has been extended to include other functions that mainly prolong the lifetime of the battery. BMS functions can be broadly categorised into protection, performance management, diagnostic, interface and auxiliary functions [1].

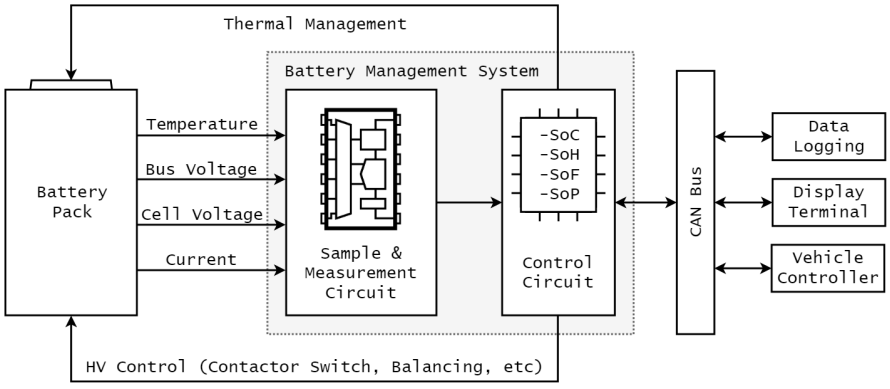


Figure 2.6: Generic Function of a BMS [8]

2.3.2.1 Voltage, Current and Temperature Monitoring

The BMS directly measures the voltage, current, and temperature of the cell or BP [1]. The measured values are used by the BMS to estimate battery state and detect that the

battery is charging/discharging within the SOA. Measurement sample frequency depends on the application, however, high sample frequency might be required to allow more precise measurements and state estimation. The most commonly used sampling frequencies are 1 and 10 Hz [26]. The BMS also validates that the sensors are taking accurate measurements by filtering out noise and compensating for deviations in measurements from sensors/devices.

2.3.2.2 Cell and Battery Pack Protection

The BMS ensures that the battery operates within accepted voltage, current and temperatures. Beside cell protection, the BMS also protects the BP from damage by disconnecting defective cells, modules or the whole pack to prevent damage to other cells or system components [1].

2.3.2.3 Charge and Discharge Control

The BMS ensures proper charging/discharging voltages and temperatures. More batteries are damaged by inappropriate charging than by any other cause. The discharge current of the battery is often expressed in terms of C-rate, in order to normalise against the battery capacity, which may be different among batteries. C-rate is a measure of the rate at which a battery is discharged relative to its maximum capacity. LICs are charged under Constant Current and Constant Voltage (CC-CV) conditions *i.e.* initially cells are charged with constant current as voltage rises to a set value (depending on cell chemistry), then the voltage is maintained as current drops [27, 6].

2.3.2.4 Cell Balancing

Imbalance among cells in a battery are caused by: charge/energy difference, total capacity difference due to manufacturing process variations, and internal impedance difference caused by the manufacturing process or uneven degradation of the cells in the pack [28]. Imbalance may result in over-charge or over-discharge or over-heating of one or more cells. Cell balancing operations ensure that all cells have similar operating conditions to maximise battery life. Cells are *equalised* using switches during charge and discharge. There are two major schemes for balancing: passive and active balancing.

In Passive Cell Balancing (PCB), energy is drawn from the most charged cell and is dissipated across a resistor (bleed resistor), whereas with Active Cell Balancing (ACB), energy is just transferred between cells [4]. There are two main modular approaches to ACB *i.e.* neighbour-only and nonneighbour-only [29]. Nonneighbour-only approaches allow transfer of charge between non-adjacent cells. There are four major ACB techniques *i.e.* cell to cell: energy is moved between adjacent cells, cell to battery: energy is taken from the most charged cell and sent to the entire battery, Battery to cell: energy is taken from the entire battery and sent to the least charged cells, and Bidirectional: employs either cell to battery or battery to cell depending on need [4].

2.3.2.5 State Estimation

States are the variables related to the battery system evolution, *i.e.* they capture a knowledge of the history of the system [30]. There are four major states estimated by the BMS; State of Charge (SoC) State of Health (SoH), State of Power (SoP), and State of Function (SoF).

2.3.2.6 Data Logging

The BMS monitors and stores the battery's history. Stored information is used for estimating SoC, SoH or SoP in order to increase the battery lifetime and compare healthy/expected state of the battery with the measured state to determine whether it has been subject to abuse. Parameters such as number of cycles, maximum and minimum voltages and temperatures, and maximum charging and discharging currents can be recorded for subsequent evaluation [1].

2.3.2.7 Communication

BMS has communication channels that link it to other systems interfacing with the battery for monitoring its condition or its history. Communications interfaces allow user-access to the battery for modification of BMS control parameters or diagnostics and tests. The most common communication channel in automotive systems is the Control Area Network (CAN) bus. Other channels include FlexRay for inter-system communication and analogue/digital I/O, Local Interconnect Network (LIN) for inter-component serial communication, Serial Peripheral Interface (SPI) for mainly internal digital communication and pulse width modulation signals for communication with sensors/actuators [3].

2.3.2.8 Demand Management

While not directly related to the operation of the battery itself, the objective demand management is *intelligent* minimisation of the current drain on the battery or regenerative braking currents when the SoC is already high, by designing power efficiency techniques into the applications circuitry and thus prolong the time between battery charges [1]. Battery models based on usage are created from both internal and eternal parameters which may include the driving pattern or the temperature conditions at a given time. These parameters are then fed back into the BMS for continuous evaluation.

2.3.3 Topology

BMS usually consist of three tiers: Cell Monitoring Unit (CMU), Module Management Unit (MMU) and Pack Management Unit (PMU) [3]. The CMU is attached to each cell and measures cell voltage, temperature, and other parameters at cell level and provides cell-level balancing. The MMU manages and controls a group of CMUs providing inter-cell balancing. Lastly, the PMU manages and controls all MMUs, communicates with external systems, measures battery pack-wide parameters such as pack current and voltage, and controls pack safety devices. There are three major types of BMS topology: centralised, master/slave and distributed.

2.3.3.1 Centralised Topology

Centralised BMS (see figure 2.7) have got the CMU, MMU and PMU functionality are combined into one system (controller). It is highly economical and can be used for small low-capacity devices such as electric bicycles. However, scaling such systems is difficult due to rapid rise in complexity in design and wiring. Centralised BMSs are not commonly used in BEVs and large BP applications.

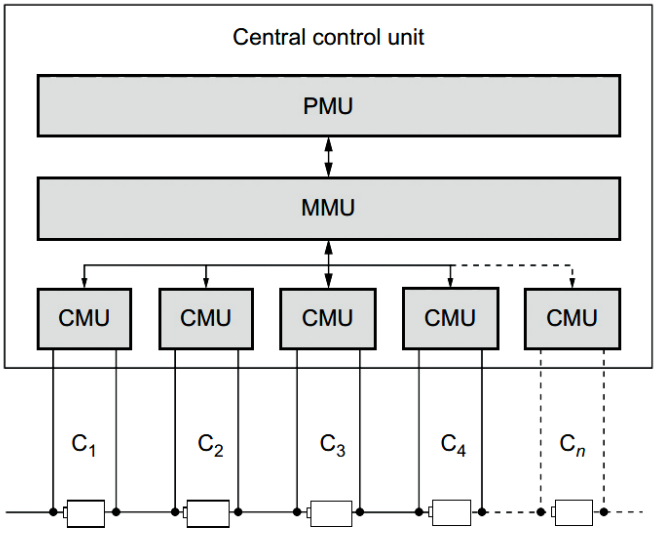


Figure 2.7: Centralised BMS Topology[3]

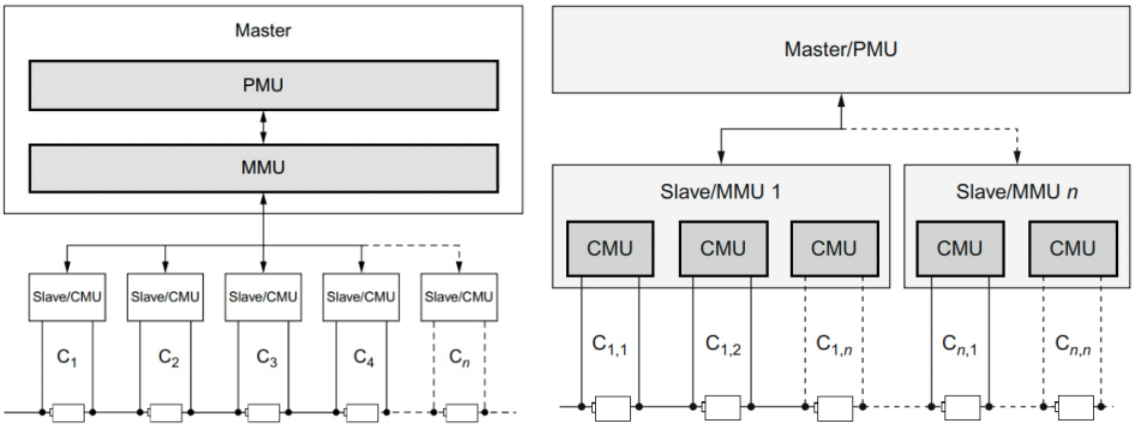
2.3.3.2 Master/Slave Topology

A Master/Slave (M/S) BMS topology has a central controller (master) connected to a slave unit(s) connected to a cell(s). M/S BMS offers reduced design complexity and higher flexibility with some functionality split between the master and the slave. M/S BMS are more expensive than centralised BMS but are more scalable. There are two configurations *i.e.* M/S BMS with separate CMU (M/S-1) and M/S with separate PMU (M/S-2).

In M/S-1 (see figure 2.8a), the PMU and MMU functionality are merged to form the master. This configuration poses a maintainability challenge due to high number of connections at increasing voltages. The CMU boards can be placed close to the cell. A *smart cell* has CMU functionality integrated together with the cell [9]. In M/S-2 or *modular* (see figure 2.8b), the MMU and CMU are merged to form the slave. This is the most common configuration for BEVs/HEVs allowing the separation of the BMS into smaller modules that are easier to maintain and assemble.

2.3.3.3 Distributed Topology

The distributed BMS does not require a central controller. The PMU, MMU and CMU functionality are all managed by a subsystem for one or more cells. When compared to the centralised and M/S topologies, they offer higher flexibility, high fault tolerance, easy fault isolation especially when using smart cells, light-weight modules due to the reduced communication wiring, and are highly maintainable due to support for *plug-and-play* installation [3, 2]. However, distributed topologies are highly complex and require advanced Electronic Control Units (ECUs) with flexible and safe communication infrastructure. Distributed systems are more commonly used in smart grids. Figure 2.9 shows a distributed BMS schematic diagram (the MCU contains the PMU and MMU).



(a) M/S-1 BMS Topology **(b)** M/S-2 or Modular BMS Topology

Figure 2.8: Master/Slave BMS Topology [3]

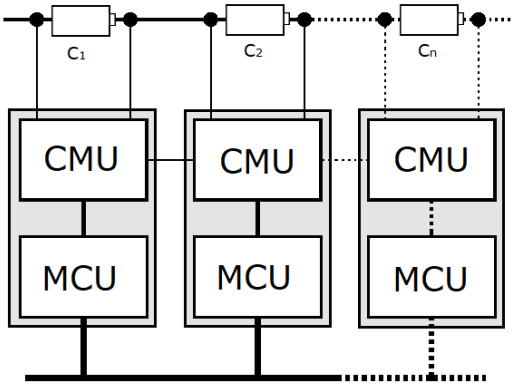


Figure 2.9: Distributed BMS Topology [2]

2.3.4 Battery State Estimation

The BMS depends on indirect methods to measure the battery states. Each of these methods has some limitations. The BMS employs several methods to obtain more accurate state estimations. The SoC is the most important since it shows amount of charge in the battery. It is usually calculated at short intervals. The SoH is measured over a longer period of time than the SoC. Power estimations provide information about the battery performance in relation to application expectations.

2.3.4.1 SoC Estimation

The SoC is the amount or quantity of charge available (releasable capacity, $C_{releasable}$) in the battery or cell at a particular point in time, in contrast with the total charge available when fully charged (rated capacity, C_{rated}) [4, 6]. When a battery is discharging, the Depth of Discharge (DoD) can be expressed as the percentage of the capacity that has been discharged by any amount of current (released capacity, $C_{released}$) relative to C_{rated} [6].

$$SoC = \frac{C_{releasable}}{C_{rated}} \times 100\% \tag{2.1}$$

$$DoD = \frac{C_{released}}{C_{rated}} \times 100\% \tag{2.2}$$

Without considering the cell's Coulomb efficiency (η) and battery ageing, the SoC can also be expressed as:

$$SoC(t) = 100\% - DoD(t) \tag{2.3}$$

Estimating an accurate value of the SoC is not obvious since battery charging involves complex chemical and physical processes. BMS performs SoC estimation of individual cells in the battery chain for both internal and external applications. For example, SoC is required to ensure optimum control of the charging process, while the user may require SoC to know the estimated remaining drive-range.

Cell SoC

Cell SoC estimation methods can be classified into four categories: look-up table, ampere-hour integral, model-based, and data driven [8].

With a look-up table, measured parameter values are compared against known discharge curve values. The look-up table can provide precise values of SoC if the battery is not actively charged/discharged for a while. This makes it a less practical method for real-time applications since measuring precise Open Circuit Voltage (OCV) would require disconnecting power for extended periods of time [8].

Ampere-hour integral (Coulomb counting) method [8, 6] provides more precise SoC during battery charge/discharge by integrating precise current flow over a period of time *i.e.* it calculates the remaining capacity simply by accumulating the charge transferred in or out of the battery [6]. By obtaining the initial SoC, the SoC values at any time during charge/discharge can be obtained using equation 2.4 below:

$$SoC(t_k) = SoC(t_0) - \frac{1}{Q}\int_{t_0}^{t_k} \eta I_L(t)dt \tag{2.4}$$

Where $I_L(t)$ denotes the load current of the battery, Q denotes the maximum available capacity and η denotes Coulomb efficiency. Some of the drawbacks of this method are: it experiences battery current measurement errors of due to random disturbances (*e.g.* electrical noise, temperature drift), and the required Q must be re-calibrated due to variations in operating conditions and ageing of the cell. Therefore, the ampere-hour integral method works better when used with other supporting techniques.

Model-based SoC estimation methods (see figure 2.10) express battery models as state equations. They can generally be classified into three types *i.e.* electro-chemical model, Equivalent Circuit Model (ECM), and electro-chemical impedance model. Several nonlinear state estimation algorithms and adaptive filters are employed to estimate or infer the internal

state of batteries *e.g.* Kalman filter, Luenberger observer, PI observer, sliding-mode observer [8]. Model-based estimation methods combine the ampere-hour integral and look-up table methods *i.e.* OCV look-up table values are used to correct the SoC obtained from current integration. Model-based methods provide much more reliable and accurate compared to ampere-hour integral but require much more development time and extensive domain knowledge [31].

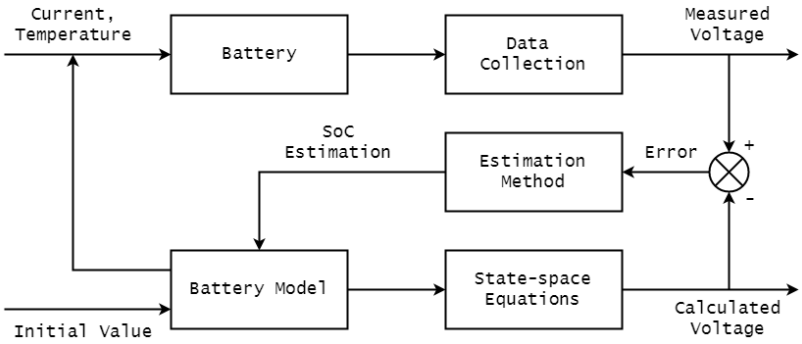


Figure 2.10: General Flow of Model-based SoC Estimation [8]

Data driven estimation methods depend on input-output data. These methods do not require accurate initial model parameters, and are, therefore, suitable where there is high uncertainty *e.g.* black-box models in combination with intelligent systems. Black-box models can effectively solve nonlinear state estimation [8]. However, data driven methods require large amount of data. Additionally, heavy dependence on the data may lead bias in black-box model's decision making [31].

A practical approach to SoC estimation is a data-model fusion method that merges the online data-driven method and the model-based method, where the data-driven method can identify the system parameter in real-time with the online measurements [8].

Battery SoC

Battery SoC estimation methods can be classified into three types: cell calculations based, screening process based and bias correction.

The cell-calculation-based method can be realised using three methods; big cell, short board effect, and one-by-one calculation. The big cell method regards the BP as one big cell taking the overall SoC. The short board effect method bases SoC calculation on the extreme cell *i.e.* the cell with the lowest SoC. Finally, one-by-one calculation method bases the battery SoC on the SoC of all individual cells.

The screening-process-based method chooses cells with similar characteristics (*e.g.* voltage, capacity) to construct a BP and then bases the SoC of the BP on one of the cells.

The bias correction method first builds a nominal model for the battery, then uses the online bias correction method to identify differences between the nominal model and the battery cell. SoC estimation is carried out using the corrected model.

2.3.4.2 SoH Estimation

The SoH is an *arbitrary* figure of merit of the actual condition of a battery or BP, compared to its nominal condition (*e.g.* when the battery is new), expressed in percent points [1, 4]. SoH of 100% means that the battery's condition meets the required specifications. As the battery is used, SoH is reduced. There is no particular industry standard measure of SoH and different manufacturers/users define it differently.

A simplified measure of SoH can be calculated by comparing the maximum capacity (C_{max}) of an in-use battery with a nominal value (*e.g.* battery's rated capacity — C_{rated}) stored in a nonvolatile memory [1, 6]:

$$SoH = \frac{C_{max}}{C_{rated}} \times 100\% \tag{2.5}$$

There are two approaches used to determine SoH: experimental and adaptive methods.

Experimental methods perform SoH estimation using the battery cycling history and preset parameters that influence the battery lifetime. The *life evolution* of a battery is determined by its capacity loss and the increment of its internal resistance. Therefore, SoH can be estimated using direct measurements of cell voltage and current, and the ohmic resistance of the cell at different temperatures. Linear methods *i.e.* data fitting, probabilistic method, current integration, support vector regression algorithm are commonly used, however, non-linear methods such as *big data* data-processing techniques are employed to augment the linear methods [32].

Adaptive methods determine the SoH through calculation from parameters that are sensitive to the degradation of the battery cell in much the same way as illustrated in figure 2.10. This necessary data is measurable or examined throughout the operation of the battery. Common adaptive methods include: Kalman filters, observers, fuzzy logic, artificial neural networks and least squares [32]. Kalman filters also include Extended Kalman Filter (EKF) and Unscented Kalman Filter.

2.3.4.3 Power Estimations

The ability of a battery to fulfil its required tasks are governed by both its SoC and power delivery/storage capability. Power capability prediction can be expressed using two metrics: SoP and SoF. Both SoP and SoF use the battery ECM to predict the maximum power the battery can deliver within the specified voltage limits [33].

SoF Estimation

In applications with specific power requirements, the SoF can be expressed as a *yes/no* parameter stating whether the battery has sufficient power capability to carry out a specified function (*e.g.* engine starting, speeding up, climbing) [33, 34, 35]. An SoF of `1` (yes) means the battery can carry out the function, while an SoF of `0` (no) means it cannot.

$$SoF = \begin{cases} 1 & if \quad v_{min} \geq v_{limit} \\ 0 & if \quad v_{min} < v_{limit} \end{cases} \tag{2.6}$$

v_{limit} is the minimum battery voltage allowed by manufacturer specifications, and v_{min} is the minimum voltage reached by the battery during the discharge profile [33]. However, applications with less specific power requirements, it would be preferred to define the SoF as:

$$SoF = \frac{P - P_{demands}}{P_{max} - P_{demands}} \tag{2.7}$$

where P is the possible power the battery could supply, the $P_{demands}$ means the demands of the power, and the P_{max} means the maximum possible supplied power of the battery (while the SoH and SoC equals to 0, and the operating temperature is at a specific temperature) [35].

SoP Estimation

In comparison to SoF, SoP is a *vernier* signal indicating how much power is available [33]. A battery's SoP is defined as the ratio of peak power to nominal power. SoP is a common indicator of the maximum charging and discharging power capabilities of LIBs and is crucial for both the battery management and vehicle supervisory control system [35]. SoP estimation methods can be broadly divided into: Characteristic Map (CM) based and ECM-based methods [36, 37].

CM-based methods use offline CMs (such as look-up tables) stored in BMS memory to calculate the SoP. These offline CMs mainly contain the static interdependence among the SoP, battery states (*e.g.* SoC, SoH at various temperatures) and battery parameters (*e.g.* duration of the power pulse, battery voltage). CM-based methods are simple and easy to implement.

ECM-based techniques differ mainly in the used ECM (*e.g.* Randle ECM) and methodology for parameter and battery states identification [37]. The SoP can be defined as:

$$SoP = \frac{v_{limit}(v_{OCV} - v_{limit})}{\sum r_{internal}}[W] \tag{2.8}$$

where $r_{internal}$ is the total internal resistance of the battery model. SoP is derived from the ECM and corresponds, for discharge conditions, to the power delivered at the battery terminals when the battery terminal voltage drops to v_{limit} for steady-state operation [33].

2.3.5 Battery Modelling

LIC behaviour results from various electro-chemical and physical processes. Battery models are based on the mathematical description of these processes and are a useful tool in optimising BMSs. By applying several external electronic and thermal stimuli to the model during simulations, the designer of a BMS can investigate the development of the battery voltage and temperature, and also the course of each of the various reactions that take place inside the battery [38].

2.3.5.1 Equivalent Circuit Model

ECM uses electrical circuit components such as resistors, capacitors and voltage source to build circuit networks that describe battery parameters. The ECM is widely used because

of its simplicity and ease of implementation for realtime applications with relatively high accuracy [8]. ECM techniques are used to model both electric and thermal battery parameters [30],

Electric Circuit Models

The simple ECM (see figure 2.11) is composed two parameters: voltage source and series resistance [30]. The OCV denotes the ideal battery voltage source without considering the battery's internal characteristics. The series resistance represents the internal voltage drop due to electrical resistance from various battery components or with accumulation and dissipation of charge in the electrical double layer [8].

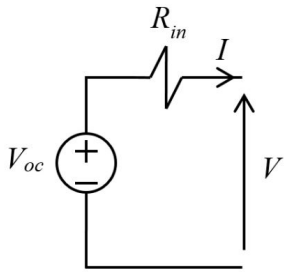


Figure 2.11: Simple ECM [30]

Thévenin Model

The Thévenin model (see figure 2.12) considers dynamic voltage behaviour and the mass transport effects such as the diffusion resistance (R_D) and diffusion capacitance (C_D). Several parallel RC branches represent dynamic behaviour. Using a higher number of RC branches may model battery processes better and subsequently improve accuracy.

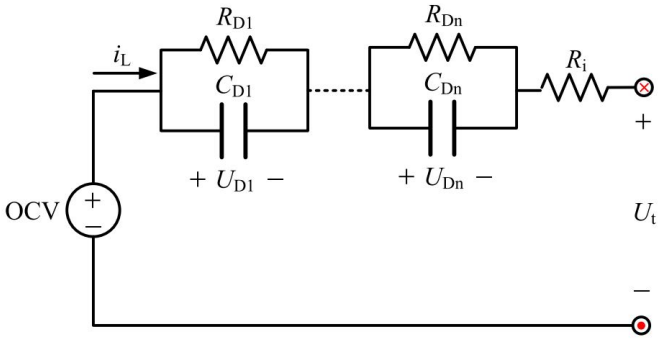


Figure 2.12: Thévenin ECM [8]

C_{Di} denotes the ith equivalent diffusion capacitance, R_{Di} denotes the ith equivalent diffusion resistance, U_{Di} is the voltage across C_{Di}, for $i = 1, 2, 3, 4, \ldots n$. Electrical behaviour of this battery model can be expressed by equation 2.9; where: i_L denotes battery load current and U_t denotes battery terminal voltage.

$$\begin{cases} \dot{U}_{Di} = -\dfrac{1}{R_{Di}C_{Di}}U_{Di} + \dfrac{1}{C_{Di}}I_L \\ U_t = U_{oc} - I_L R_i - \displaystyle\sum_{i=1}^{n} U_{Di} \end{cases} \tag{2.9}$$

OCV Recursive Estimation: OCV recursive estimation techniques are used to implement the Thévenin ECM. Since battery OCV shows a monotonically increasing trend with SoC, the SoC can be predicted in real-time through the online identified OCV. The commonly used algorithms for battery system identification are recursive least squares and the Kalman filter. The recursive least squares algorithm is easy to implement on-line and is computationally efficient. The Kalman filter achieves the accurate realtime parameters by minimising the root mean square error between the desired output value and actual output value based on its state equation [8].

Thermal Circuit Model

In the Thermal Circuit Model (see figure 2.13), the temperature is assumed to be uniform or piecewise uniform in the battery; it is possible to use lumped elements to describe the thermal behaviour of the battery itself. The same elements can be used to represent thermal resistances (the inverse of the thermal conductivities), thermal capacitances, and heat sources [30].

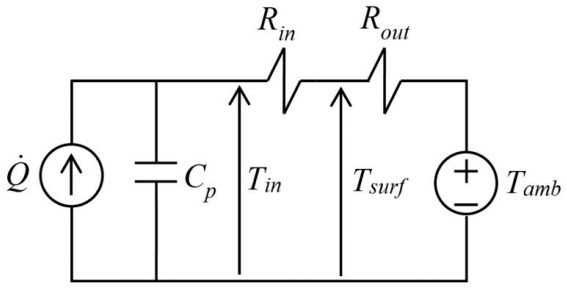


Figure 2.13: Thermal ECM [30]

2.3.5.2 Parameter Identification

Parameters refers to the characteristic quantities of the system, including chemical (solid phase conductivity, diffusion coefficients) and electric quantities (internal resistance, capacitance) [30]. Identification methods can be classified into: online and offline identification. Online methods allow parameter/state estimation during the normal operation of the battery, while offline methods are developed by testing the batteries with ad-hoc tests performed when the battery is not used for its application.

Online Identification Methods

The majority of online identification methods are applied to ECMs representing the electric behaviour of the battery. The online methods usually focus on SoC estimation during the normal operation of the battery. Since the SoC varies continuously during battery operation,

online estimation of the SoC offer more adaptable results. Some or all of the other parameters depend on the SoC, and their estimation can be online or offline.

Offline Identification Methods

Offline identification methods estimate parameters that are not estimated online and to obtain initial values for the parameters estimated online. Since the parameters of the ECM keep changing while the battery is in operation, highly accurate initial values (such as the actual OCV) can only be obtained when the estimation is done offline. In addition, there is reduced complexity of the estimation algorithm. One major drawback of offline methods is the difficulty of estimation in cases where parameter variation is necessary, *e.g.* characterising variation of the SoH and temperature.

2.4 Scalability and Reconfigurability

Scalability of systems is often hard to define precisely but rather can be specified in relation to requirements or considerations. Scalability is generally understood as the ability of a system to respond to increasing demand.

A reconfigurable architecture with respect to software and hardware components and their inter-relationship (since the software requires various data from the hardware for proper battery monitoring), maximises flexibility and reliability of the BMS. A well-designed, combined hardware-software architecture provides both cost-effectiveness and scalability [39].

A smart modular BMS results in a reconfigurable framework that provides trade-offs for different heuristics such as reliability, cost, size and volume, weight, and efficiency [39]. A SBMS can be achieved through the use of reconfigurable battery modules and a scalable and reconfigurable BP. Scaling a BMS requires high level flexibility to increase battery power and energy to fit a wider range of requirements. This section discusses some of the key scalability considerations for designing a SBMS.

2.4.1 Cells

As earlier mentioned (see sub-section 2.1.3), different cells have different characteristics that enable them to be used for specific applications. A BMS can be tailored to meet specific requirements *e.g.* the system can be set to a particular nominal cell voltage [3]. This reduces costs since the BMS is designed to the required accuracy and necessary processing power. However, this limits use to that particular cell chemistry.

2.4.2 Fault Tolerance and Reliability

It is not possible to remove all noise factors in a systems for complete reliability. However, reliability can be maintained to acceptable levels by making the system less sensitive to noise factors and more tolerant to faults. Since faulty cells can lead to thermal runaway, it is better to disconnect them from the module or disconnect the module. The BMS should have the capability to bypass weak/faulty cells or modules in such a way that the BP remains operational [39]. This is achieved through the use of switches connected to each cell to form a battery-cell reconfigurable array. System reliability is assessed based on the reliability of components and their connections since individual components directly affect reliability of the entire system.

2.4.3 Cost

The cost is a major consideration in realising a reconfigurable architecture. A low component count decreases costs. Highly decentralised battery systems may involve a high number of components since each cell has its own monitoring. High component count increases cost, volume, and weight while decreasing system efficiency [5]. Modular BPs can easily scale without high increase in complexity since most SOA supervisory circuitry is confined to the module for a number of cells [4]. A highly centralised system on the other hand makes cost estimation more complex with increase in components. A more scalable approach is to divide the battery according to functionality. This simplifies cost estimation since quantities of components involved in implementing a given functionality can provide costing for future improvements and reconfigurations much more uniformly [40].

Cost estimations are greatly improved by having more accurate information about the costs of different vehicle systems. A detailed cost analysis has to include the costs of the single components as well as the tooling and development costs [5].

2.4.4 Battery Pack Structure and Support

The design of the battery housing depends on several mechanical, safety, service, and cost requirements. For example as a mechanical requirement, the BP is designed to withstand occurring crash loads. Hence the required crash performance of the BP substantially influences the design and especially the weight of the housing and the whole system [5]. The BP should also be light-weight since the amount of energy used by a vehicle rises as weight increases.

Design requirements impose limits on the range of allowable design which may limit the scalability or reconfigurabilty of the BP. For example, the BP is usually positioned at the underbody and the centre tunnel of the vehicle ensuring a low centre of gravity for better driving dynamics. It is also not common to replace car battery cells, rather it is preferred to replace a module with defective cells or the entire battery [4].

2.4.5 Thermal

Besides preventing thermal run-away, maintaining LICs within optimal operating temperatures also extends their lifetime. Therefore, a good thermal management strategy must not only maintain safe operating temperatures but also maintain optimum operating temperatures. Designers have to carefully choose a thermal management strategy because it highly influences the physical structure of the BP. The effectiveness of thermal control also defines charge/discharge limits. For example, thermal system with refrigeration capability can easily support faster charging rates [19].

Higher power battery applications require a thermal management system that equalises temperature gradients between the cells much more effectively [3]. The cooling system can be air-based (fans and heat sinks) or liquid-based (cooling fluid). Air-cooled systems are simper to implement but are much less effective than liquid-cooled systems when evacuating heat from the batteries. Depending on the environmental conditions, a good thermal management system should have the capability to heat the cells to bring their temperature into the allowed operating window.

2.4.6 Electrical Isolation

In BEVs the number of cells connected in series is quite high resulting in large differences in voltage among components. In addition to user protection, component-to-component isolation also protects BEV hardware components from damage. For example, even on the same board, components whose functionality directly interacts with the batteries (*e.g.* current sensors, voltage sensors, relays) are isolated from the LV components such as micro-controllers and non-volatile memory. In this respect, the BMS functionality is divided according to isolation [41].

The level of isolation required depends on the peak operating voltage at a component's location in the BEV's battery or traction system. According to the ISO 6469-3:2018 standard [42], BEV voltages below 60 V are classified as low voltages (class A) while those above 60 V are classified as high voltages (class B) and require isolation coordination. Whereas the traction battery is in the HV range, battery modules are kept in the LV range [5].

There are two main types of isolation *i.e.* basic and reinforced [42]. Basic isolation is a single level of isolation which provides basic protection against electric shock. Reinforced isolation is a double level of isolation which provides higher protection against electric shock. Reinforced isolation provides supplementary protection such as functional isolation that protects against ground loops.

2.4.7 Communication

The BMS is usually designed to satisfy specific goals [10]. For example, a power grid BMS may require longer range communication links than those in a BEV BMS. This leads to use of specific technologies such as communication standards. Different communications standards are suitable for different applications. For example, SPI communications are cheap and sufficiently supports short distance inter-component communications on a circuit board while CAN is suitable for reliable communication of BEV components in different locations.

SBMS application designs must support several communications standards without requiring serious change to existing software. Addition of a communication layer to the overall BMS application stack [10] allows other BMS software and hardware to operate independent of communication standard used.

Communication in the BMS also contributes to the overall wiring harness. In a modular BMS, there are three major ways of connecting the master and slaves *i.e.* star, daisy-chain and hybrid topological connections [41]. The star topology is easy to implement but leads to increase in wiring harness since each slave has a direct connection to the master. With daisy-chain, the slaves share the same communication line to the master. Each slave is identified with a unique ID (or address). The hybrid topology is a combination of the star and the daisy-chain. For example, a relatively small number of slaves are grouped into clusters. Slaves in each cluster connect in a star topology and the clusters are connected with daisy-chain topology [41].

2.4.8 Hardware Topology

Good electrical architectures for balancing units of BMSs are governed by *imperative* design constraints. Imperative design imposes *modularity* and *localised control* constraints [43].

2.4.8.1 Modular Hardware Design

Modularity allows the connection of homogeneous units in a BP. Homogeneity ensures that BPs must contain the same cell/module configuration. Modular designs enable easy integration, increased safety by eliminating potential single points of failure, and reduced wiring harness decreasing complexity and weight [29].

2.4.8.2 Hierarchical Hardware Topology

A hierarchical architecture involves a global BMS, and local controllers that act as local BMSs. This is because as the number of cells increases, the amount of software processing and hardware complexity also increases requiring sharing of management functions across several units. A hierarchical organisation can be achieved through the use of switch-configuration management; cell-level arrangement (by the local BMSs) and array-level arrangement (by the global BMS). This approach promotes system scalability by effectively coping with large-scale battery cells [39].

2.4.9 Software Layering

BMS software is highly influenced by the topology [3]. For scalability, it is important to decouple the software architecture from the hardware design. Layering the software design according to functionality is an effective way of separating concerns in the BMS software. BMS software can be divided into 4 layers, *i.e.* low-, middle-, upper- and top-level [44].

The low-level contains device drivers and hardware interface routines. The middle-layer is responsible for implementation of communication protocols and interpretation of physical measurements. The upper-layer does high-level battery computations. Finally, the top-level makes decisions based on information from lower lying layers. Layering increases the reusability and maintainability of the software.

3

Battery Management System Design

In partial fulfilment of the second project objective, this chapter describes the design of a Scalable Battery Management System (SBMS). The first section describes the project delivery process, then follows a generalised view of the architectural design of the system, and the last sections give a detailed description of the topological, functional, hardware, and software design of the SBMS.

3.1 Project Delivery

Infotiv AB suggested a delivery process that divided the project into four *phases*. Phasing the project provides a clear follow-up on progress on activities to improve delivery. These phases are:

Literature survey: In this phase, we broadly investigate BEV/HEV BMSs and their scalability. The results of our investigation are written in theoretical part of the report (section 2).

BMS Development: This phase takes up biggest part of the project. During this phase we design, implement and test the system. It is divided into two sub-phases *i.e.* development of a scalable BP and development of the scalable BMS.

Documentation: In addition to this report, we carry out detailed technical descriptions of the system. These technical documents including circuit diagrams and operational manuals are bundled into education material for Infotiv AB

Presentation: In addition to documentation, we also present our research findings both at Chalmers University and Infotiv AB

When reasonable fulfilment of phase requirements is attained, that phase is *frozen* and development proceeds to the next phase. Within each phase, *agile-style* development techniques are used to continuously refine a solution through collaboration with both the supervisor, advisor and other Infotiv AB engineers.

3.2 System Design

In order to ensure a fully scalable system, the system scalability is explored in four perspectives. We called this strategy *design layering*. In design layering, the scalability of the BMS

design is studied in the *topological*, *functional*, *hardware* and *software* perspectives. Figure 3.1 shows how the different project layering perspectives interact.

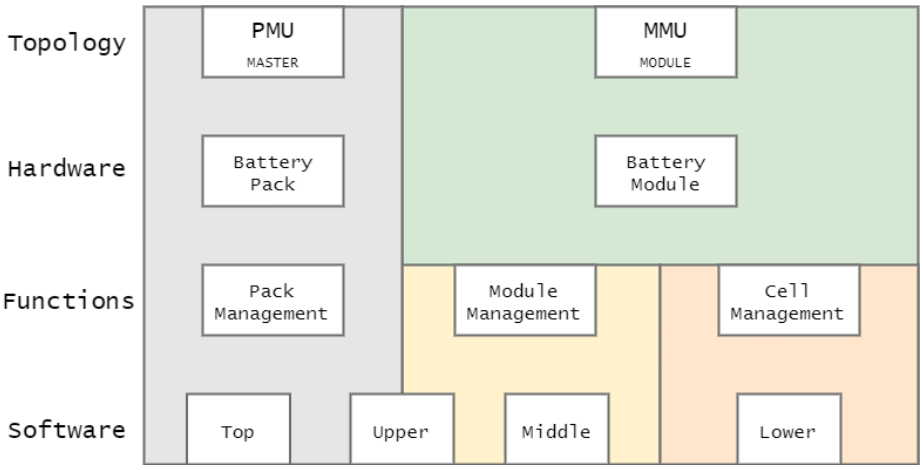


Figure 3.1: Project Design Layering

During system design, the modular topology was chosen for the project. The overall BMS is, therefore, divided into the Pack Management Unit (PMU) and Module Management Unit (MMU), each with a controller. The MMU controller acts as a *local* BMS while the PMU controller has the *overall* BMS view [39]. BMS functions are subdivided into cell, module and pack management. Pack management functions are handled by the PMU while the cell and module management is handled by the MMU.

With the layered hardware design, the BP is divided into battery modules. Each battery module is managed locally by the MMU. BP components (*e.g.* pre-charge, cooling) that affect other battery modules are managed by the PMU [5]. BMS software is divided into 4 layers, *i.e.* low-, middle-, upper- and top-level software layers. In the low-level, we have device drivers and hardware interface routines such as communication protocol implementation. The middle-layer is responsible for implementation of data handling/manipulation functions and interpretation of physical measurements. The upper-layer does high-level battery computations. Then, the top-level makes decisions based on information from the other layers [44, 10]. However, these four layers are implemented in both the PMU and MMU to varying degrees (see section 3.6). This means that the whole system is implemented as master BMS coordinating slave BMSs [39].

Modular/layered design delivers robust systems in shorter time compared to conventional code development. BMS algorithms are implemented to support plug-and-play integration while at the same time minimising single point of failure promoting a more scalable design. Additionally, failures can be easily localised and controlled. Layering increases the re-usability and maintainability of the software [9, 10].

3.3 Topological Design

Following the modular topology, the overall system is designed to have a master—PMU and several slaves—MMUs. The module controller manages individual battery cells and relays information to the PMU controller. Figure 3.2 shows the overall design[1].

[1]The design is implemented with two modules, however, four modules are shown here to illustrate scalability

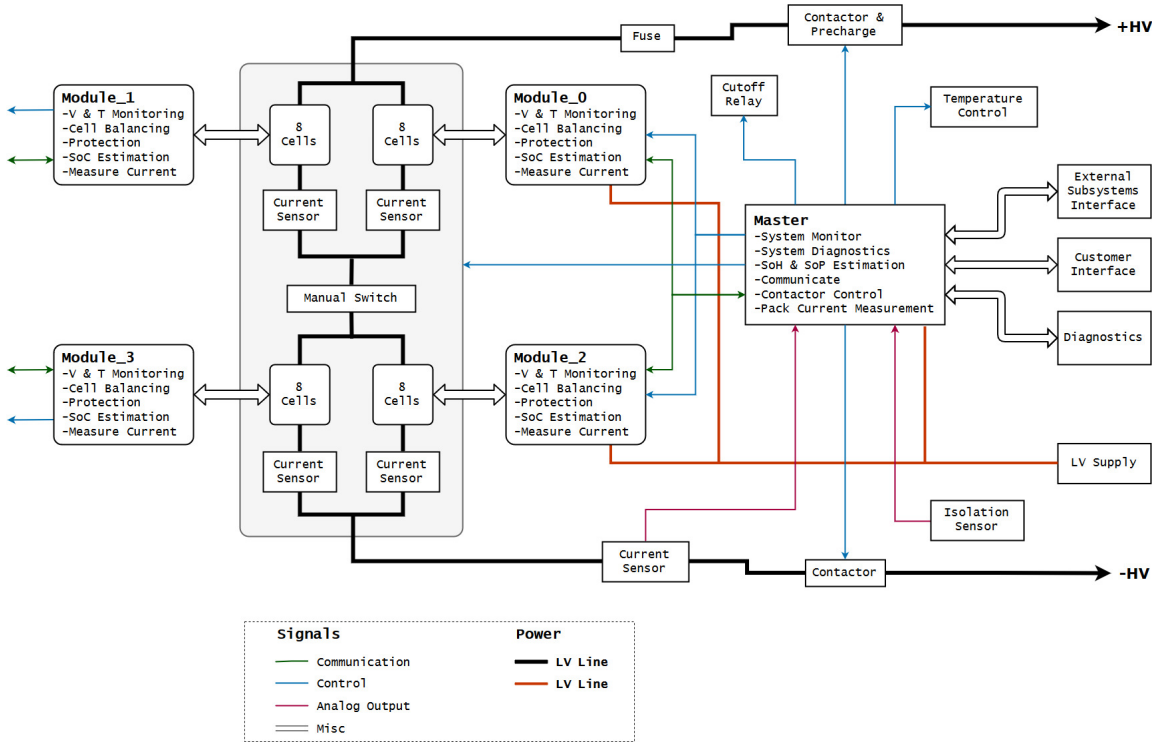


Figure 3.2: System Design Overview

3.4 Functional Design

Management functions are split between the modules and the master to varying degrees (see figure 3.2). Splitting functionality increases flexibility since the master and the modules are scaled independently of each other. Following the principle of layered design, management functions are divided into three parts *i.e.* cell, module and pack management functions. The master handles pack management functions while the modules handle cell and module functions.

3.4.1 Cell Management

These are the lowest level functions that are carried out mostly by the battery module in coordination with the module controller as shown in figure 3.3. Cell management mainly involves data acquisition (*i.e.* measurement) and cell protection (*i.e.* detection of operation outside SOA). These include:

- Cell voltage measurements
- Cell temperature measurements
- Cell balancing
- Cell fault detection *e.g.* when cell voltages or temperatures exceed operating limits (see Table 4.1)

3.4.2 Module Management

Module management functions are concerned with module functions that do not directly interact with the cells as shown in figure 3.3. The module controller carries out minimal data processing on parameters collected under cell management, such as calculation of the State of Charge (SoC) of the cells. This allows the module to act as a *mini-BMS*, thereby improving the overall scalability of the BMS. Module management functions include:

- Reading cell voltage and temperature measurements
- Measuring module temperatures
- Estimating SoC with low complexity algorithms
- Handling module level faults
- Communicating with master by sending requested data and report faults
- Measuring module level current (if enabled)

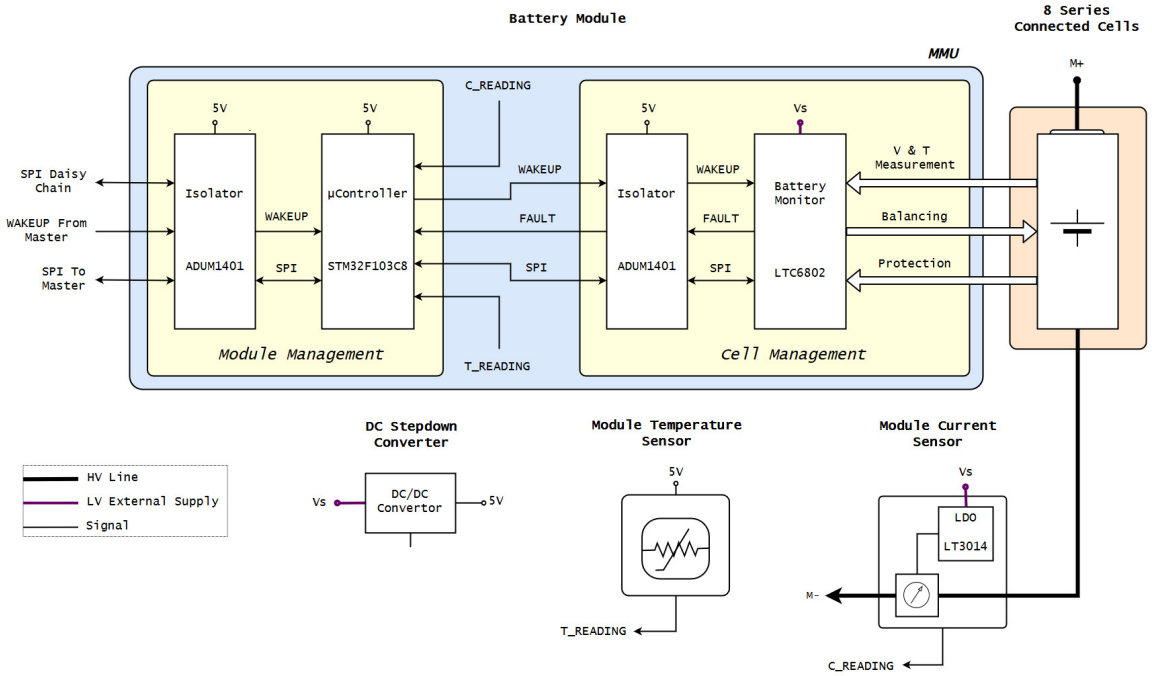


Figure 3.3: Module Design Block Diagram

3.4.3 Pack Management

Pack management functions affect the entire BMS. These functions are mainly carried out by the master controller since it carries out top decision making in of the BMS. The master controller does complex data processing and communication with external subsystems. Figure 3.4 shows the pack management (master) design. Pack management functions include:

- Initiating and configuring BMS components
- Diagnosing the system by ensuring the proper system hardware and software functioning

- Handling pack-level faults
- Logging and processing data (such as complex battery state estimation)
- Communicating with external system
- Controlling contactors and pre-charge
- Managing power (such as initiating low-power mode in module controllers)
- Monitoring proper electrical isolation
- Measuring BP current

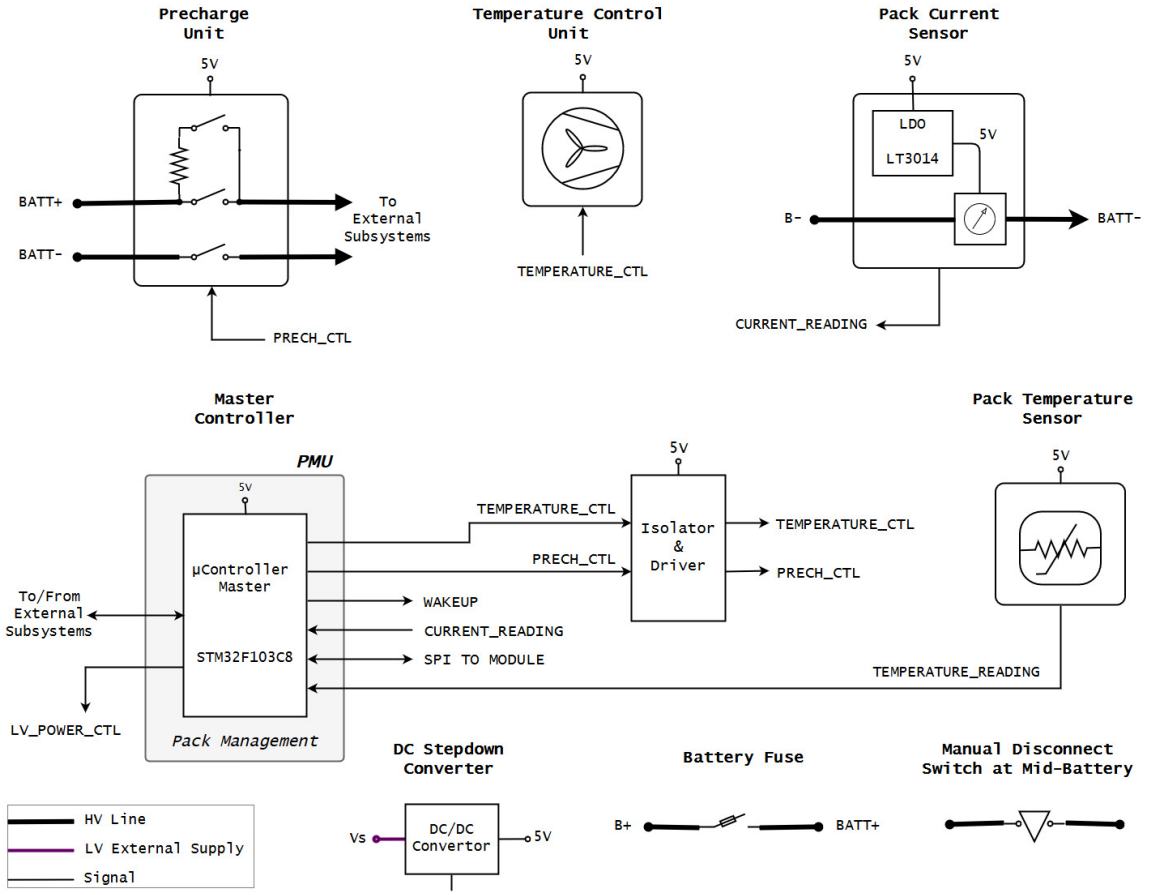
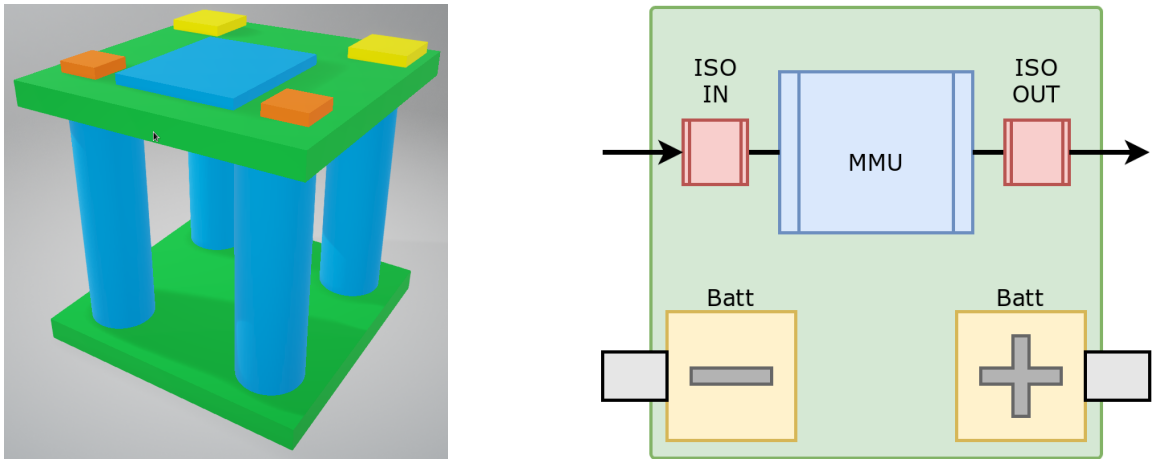


Figure 3.4: Master Design Block Diagram

3.5 Hardware Design

The BP consists of two battery modules, each with a nominal voltage of 28.8 V and consisting of eight lithium-ion cells (LICs) connected in series. These modules are connected in series to produce a nominal BP voltage of 57.7 V. Figure 3.5a shows a 3-D model[2] of the BM with 4 cells (Figure 3.5b is the top view).

[2]The image shows 4 cells, however, since the modules have even dimensions, an 8-cell modules can be constructed by combining two such modules



(a) Battery Module 3D Model **(b)** Battery Module Top View

Figure 3.5: Battery Module Hardware Design

To increase system modularity, the hardware components are grouped in *units* according to overall functionality. Table 3.1 shows these units and their overall functions. Figure 3.6 shows the arrangements of the units in the system.

Name	**Functions**
Battery Monitor	Measure cell voltage and temperature
Module/Monitor Isolator	Isolate/protect Low Voltage (LV) module control circuitry from High Voltage (HV) battery
Module Controller	Control and configure module components
Master/Module Isolator	Isolate the module from the master
Master Controller	Control and monitor whole BMS
Pre-Charge	Safely connect/disconnect battery HV to load
Current Sensor	Measure battery pack current
Temperature Control	Cooling/heating system for the batteries and components
Low Voltage Power Supply	External LV power supply to controller units
Isolated Low Voltage Power Supply	Step down voltage to component specifications
Disconnect Switch	Manual disconnection of battery power
Surge Protection (Fuse)	Automatic disconnection of battery power on surges

Table 3.1: System Hardware Units

Each cell is connected directly to the battery monitor which measures its voltage. Similarly, temperature sensors are placed at the cathode of each cell to measure its temperature. Temperature sensors are put on each battery module, pre-charge resistor, and BP. Sampled voltage and temperature values are converted to digital signals and stored.

The module controller, battery monitor, and sensors make up the *slave* (see figure 3.3). The module controller sets SOA limits in the battery monitor and reads measured cell temperatures and voltages. Each module controller in-turn is also controlled by the master controller. The master controller makes up the *master* (see figure 3.4). Due to the low computation complexity requirements, for simplicity of design, the same type of Micro-controller Units (MCUs) are used but implement differing functionality for the slave than the master.

BP current is measured by a current sensor and read by the master controller. However, each module can optionally do current measurement. The pre-charge unit contains three relay switches driven by N-MOSFET transistors controlled by the master MCU via an isolated interface. A high power toggle switch enables manual disconnection of battery supply.

All components are externally powered over a 12V LV line. The external power supply is stepped down to 6.1 V and 5 V to power relay switches and other LV circuitry (such as MCUs, current sensor) respectively. An isolated 13 V supply powers the battery monitor. The isolated line is also stepped down to 5 V powering the battery monitor regulator and other LV circuitry (such as multiplexer, amplifier). The battery monitor and the MCUs communicate using Serial Peripheral Interface (SPI) via magnetic isolation interfaces to ensuring galvanic isolation of the LV and HV power system. The HV line is fitted with a protection fuse.

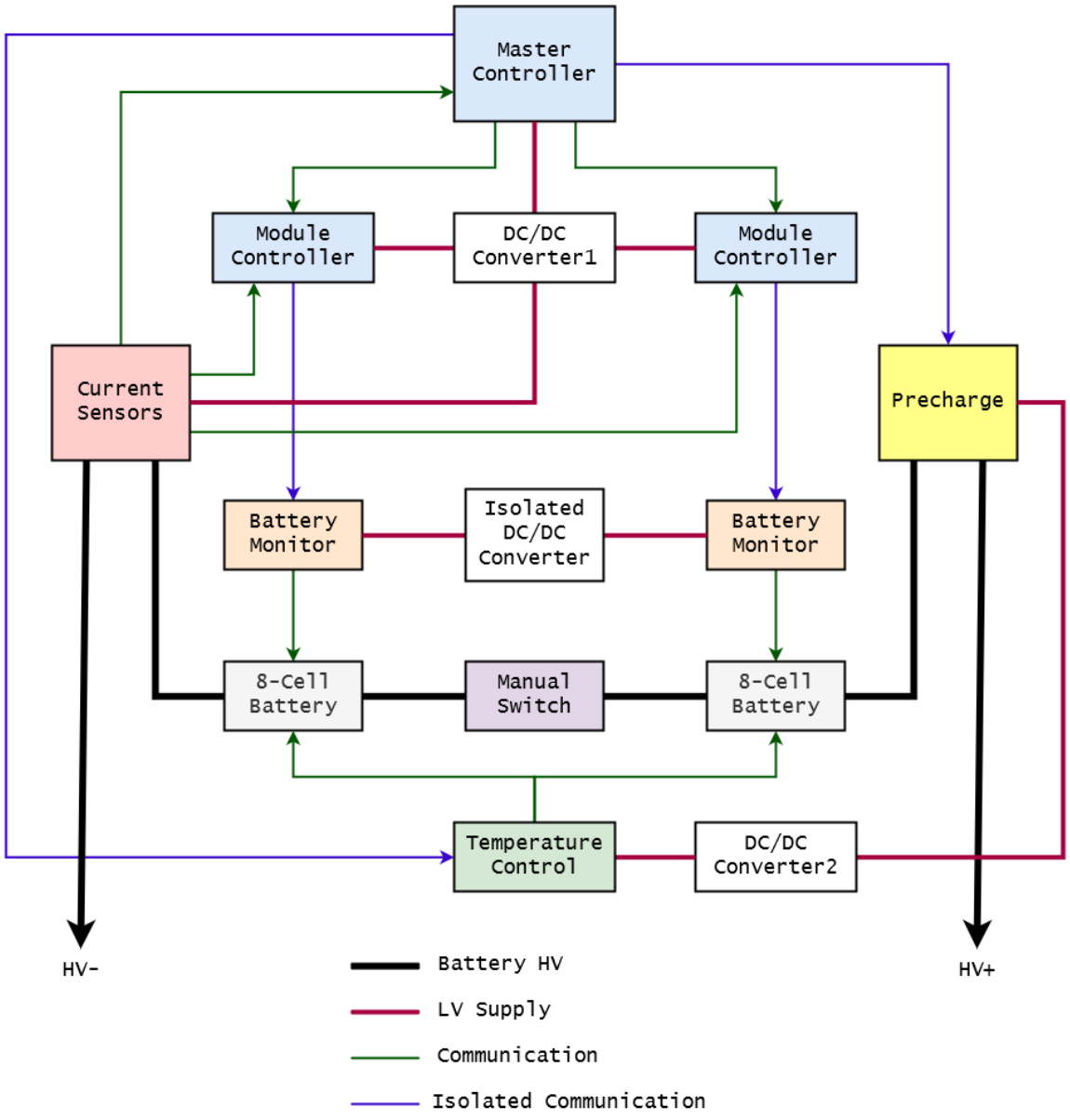


Figure 3.6: System Hardware Units Arrangement

3.6 Software Design

The system software functionality is implemented on the master and module controllers as a master BMS managing slave BMSs. The master and the slave implement the software layers to varying degrees. The master MCU mostly contains top, upper, middle layer software applications while the module MCUs mainly implement upper, middle and lower layer software (see figure 3.1).

Lower level functions run by the module MCU include:

- Hardware driver routines for configuring and reading battery monitor registers.
- SPI and I^2C communication routines.
- Analogue to Digital (A/D) conversion routines of sensor output values.

Retrieved data from these routines is stored in several variables in the program. Middle layer applications then use this data to implement monitoring functionality such as monitoring cell voltage and temperature. The upper layer applications do computations such as calculation of SoC. The top level organises the flow of the program on the module MCU. Since the module does not perform complex decision making, its top layer and upper layer are merged and any complex decisions are deferred to the master.

Lower level functions run by the master MCU include:

- SPI and I^2C communication routines.
- A/D conversion routines of sensor output values.

Similar to the module MCU, data from lower level routines is stored and used by middle layer functions and upper level applications organise the program flow. However, since the master MCU is expected to take major system decisions, the top layer also encompasses the upper layer.

3.6.1 Operation Modes

The overall system has 6 operation modes/states, *i.e.* Startup, Configuration, Monitor, Fault, Diagnosis and Standby. Figure 3.7 shows the operation state diagram illustrating transitions between different states.

The master controller keeps track of the overall system state. However, each module also implements these states. The MCU uses 2 state variables: `state` and `step`. The `state` variable indicates the overall state while the `step` variable denotes which level of the system is implementing a state. For example, there are 2 steps in startup mode, *i.e.* master MCU startup, and module MCUs startup. These state variables are always stored on non-volatile memory and are read at system initialisation.

3.6.2 Fault Mode

If the system encounters an unsafe condition that can lead to damage of cells or endanger safety of users, the system goes into the faulty state and remains there until the fault is cleared. When the system goes into fault status, current flow is automatically disabled, *i.e.*

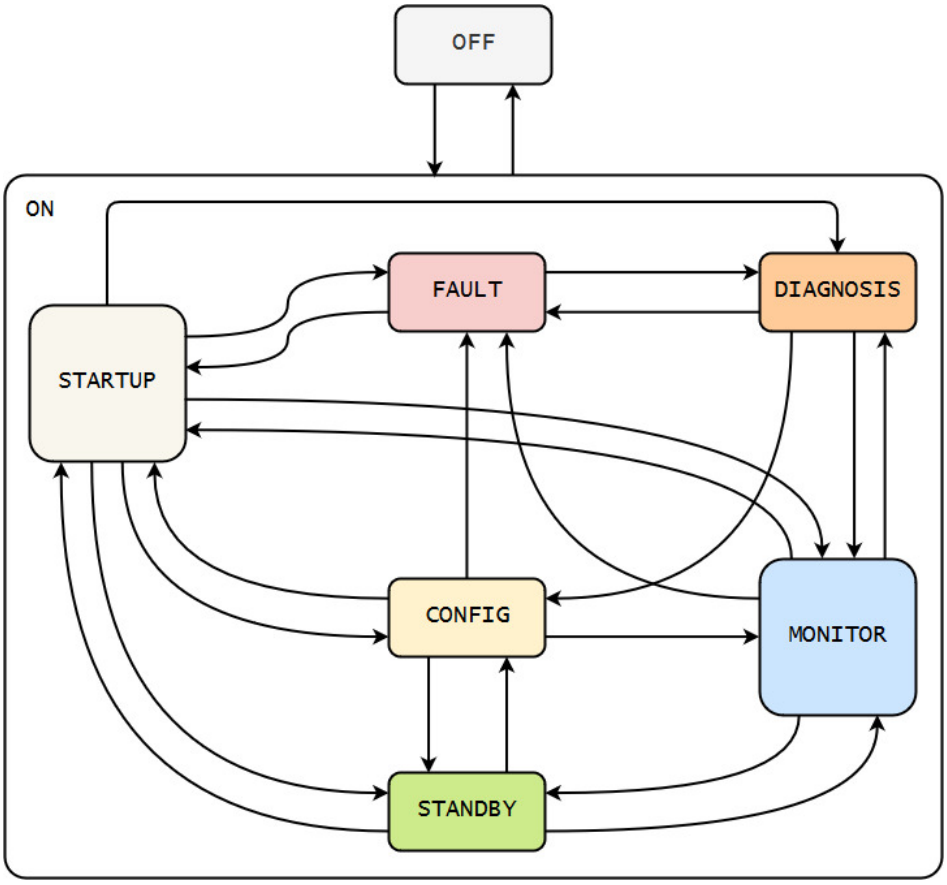


Figure 3.7: System States Design Overview

the contactors are opened. If the user wishes to solve the problem, the system is put in diagnosis mode.

3.6.3 Diagnosis Mode

In order to solve a fault, a diagnosis is carried out by sending the system into diagnosis state. Diagnosis is manually enabled. However, the system is expected to go into diagnosis mode on its own to try to solve a fault when it arises, however, this is not implemented due to limited time for development. In the diagnosis mode, the system may carryout startup and configuration activities but cannot close contactors. When a fault is successfully solved, the system proceeds to startup mode, otherwise it reverts back to the fault mode.

3.6.4 Startup Mode

When the system is powered up, it goes into the startup mode. In this mode it performs the following functions;

- The master checks that all its peripherals are attached and functioning, for example the modules must be able to establish SPI communication.
- Each of the modules present also checks that their peripherals are well connected and reports to the master.

- Each controller runs any necessary initialisation code.

In the startup, the MCUs also check for any previous errors that may be stored on non-volatile memory. In case of any error during startup the system transitions to the Fault status. Otherwise the system continues to the Configuration mode.

3.6.5 Configuration Mode

The configuration or config mode can also be viewed as an extension of the startup mode. After startup, the MCU begins configuration of system variables and peripheral components:

- Configure communication channels for MCUs and battery monitors
- Configure system timers in the MCUs
- Configure GPIO pins
- Configure the MCUs' A/D converters
- Set user limits, *e.g.* voltage, current and temperature limits, and other initial application values

The master initiates the configuration of modules. When the module controller has completed configuration, it signals the master that it is ready. The master proceeds to the monitor stage when all modules are successfully configured. In case of a fault, the system goes into the fault state.

3.6.6 Standby Mode

In standby mode, the MCU's peripherals are switched off but its random access memory is kept on and its contents maintained. Turning off peripherals conserves energy. Since the batteries need to be monitored while in use, the system can only go into this state when the contactors are open and batteries are not in use.

The master controller can respond to commands to *wake-up* from standby mode. The master controller also *orders* the modules to enter/exit standby mode. The system can be put into standby from monitor, config or startup modes. On exiting standby, the MCU returns to the previous state it was in before standby.

3.6.7 Monitor Mode

This is the major mode of the MCU where the LICs are monitored. The master MCU, module MCUs and battery monitors carry out their functions as described in the functional design (see section 3.4) while in the monitor mode. Sub-section 4.3.3 shows the system scheduling scheme used to execute different functions.

4

Implementation

This chapter describes the implementation of the Scalable Battery Management System (SBMS) design, in fulfilment of the second project objective. This chapter has three sections. The first section gives the IES Education Platform (IEP) specifications of the system. These specifications encompass constraints set by Infotiv AB and design constraints drawn from our prestudy in section 2. The second section gives hardware components required their respective configurations. The last section describes the major software functionality implementation.

4.1 IEP Specifications

The IEP BMS prototype design was built using two modules each managing eight NCR18650 cells [45]. Each cell has a maximum capacity of 3350 mAh, a maximum voltage of 4.2 V, and cut-off voltage of 2.5 V. Each module can deliver between 24–32 V, giving a BP voltage between 48–64 V. NCR18650 cells allow a maximum discharge rate of 2 C; meaning a maximum of 6.7 A can safely be drawn continuously. The system was built to be scalable to support a 400 V–100 A system (see table 6.1 that shows the necessary battery configuration for such a target system). Table 4.1 shows the main system specifications.

4.2 Hardware Components

In the implementation, several regular-sized discrete components were used which required more space that a conventional circuit board. While designing the circuits, we relied on initial manufacturer information, such as sample circuits from datasheet that we modified to fit our particular design. For example, the battery monitor is designed to work with twelve cells but we were able to modify the sample circuit to use eight cells [46]. The components were grouped into units (see table 3.1) and put on the same circuit board (bread board) if possible.

4.2.1 Battery Cells

The NCR18650B LICs from Panasonic are limited to operate within a 4–3 V range. This means the available capacity is 2,880 mAh which is approximately 86% of the original maximum State of Charge (SoC). The reason we choose this range is because the OCV-SoC curve behaves largely linearly within that range for the nominal operating temperature of 20 °C [45]. Since we are using air cooling, we restrict the maximum and minimum temperature far within the absolute limits to protect cells from getting out of SOA.

Type	Parameter	Value			Unit
		Min.	Typ.	Max.	
Cell	Absolute Voltage	2.5	3.6	4.2	V
	Operating Voltage	3	3.6	4	V
	Capacity	3250	3350	3350	mAh
	Rating		1	2	C
	Operating Current	0	3.25	6	A
	Absolute Temperature	−40	20	125	°C
	Operating Temperature	−10	20	55	°C
Module	Series Cell Count	8		8	
	Parallel Cell Count	1		4	
	Absolute Voltage	20	28.8	33.6	V
	Operating Voltage	24	28.8	32	V
	Battery Monitor Cell Count	6		12	
Pack	Absolute Voltage	40	57.6	67.2	V
	Operating Voltage	48	57.6	64	V
Isolation	Isolator Resistance	10^9			Ω
	Minimum Isolation @ 500 V	2×10^6			Ω/V
	Operating Isolation @ 500 V	2×10^5			Ω/V
Measurement Error	Voltage Measurement Error	8	9	10	mV
	Current Measurement Error	±0.24		±0.35	mV/A
	Thermistor Tolerance (NTC)		±1	±2	%

Table 4.1: System Specifications

4.2.2 Manual Disconnect Switch

A manual high power disconnect switch is inserted between the battery modules. This switch provides a safety mechanism to manually disrupt current flow. The manual switch accommodates a continuous current of 10 A at 72 VDC, which is well within our system power limits.

4.2.3 Battery Monitor

The LTC6811HG-2 is a 12 cell addressable multicell battery monitor [46] from Linear Technologies/Analog Devices. It measures voltages and temperature values and converts them to digital values using two 16-bit Analogue to Digital Converter (ADC) and stores them in registers. The ADC is a Delta-Sigma converter with built-in noise filter. It has low measurement error of less than 1.2 mV which is low enough for automotive applications. It draws

low maximum current less than 800 µA during measurement and tolerates supply voltages 11–75 V. The battery monitor also requires a regulated 5 V supply with a maximum current less than 13 mA. It can measure 6–12 cells with voltages ranging from 0–5 V.

4.2.3.1 Operation States

The operation of the LTC6811 is divided in a set of separate operating states as shown in figure 4.1:

SLEEP State: The reference and ADCs are powered down and the watchdog timer has timed out. The discharge timer is either disabled or timed out. The supply currents are reduced to minimum levels. A WAKEUP signal sends the LTC6811 the STANDBY state.

STANDBY State: The reference and the ADCs are off. The watchdog timer and/or the discharge timer is running. When a valid ADC command is received or the REFON bit is set to 1 in the Configuration Register Group (CFGR), the IC pauses for a certain time interval to allow for the reference to power up and the enters either the REFUP or MEASURE state. Otherwise, if no valid commands are received for that time (when both the watchdog and discharge timer have expired), the LTC6811 returns to the SLEEP state and resets register values. The watchdog usually expires within two seconds if no valid command is received.

REFUP State: To reach this state the REFON bit in the CFGR must be set to `1`. The ADCs are off. The reference is powered up so that the LTC6811 can initiate ADC conversions more quickly than from the STANDBY state. When a valid command is received, the IC goes to the MEASURE state to begin the conversion. Otherwise, the LTC6811 will return to the STANDBY state when the REFON bit is set to 0, either manually or automatically when the watchdog timer expires.

MEASURE State: The LTC6811 performs ADC conversions in this state. The reference and ADCs are powered up. After the ADC conversions are complete, the LTC6811 will transition to either the REFUP or STANDBY state, depending on the REFON bit.

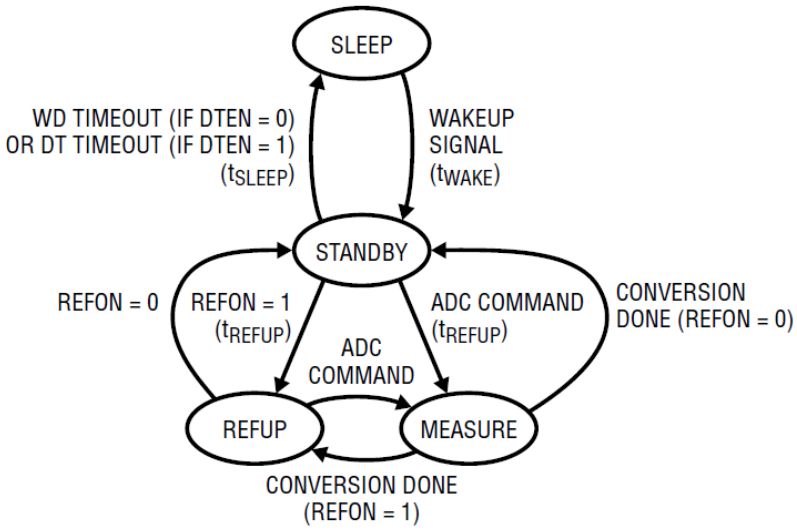


Figure 4.1: LTC6811 Operation State Diagram [46]

4.2.3.2 A/D Converter

The battery monitor has two ADCs that operate simultaneously when measuring cells. Only one ADC is used to measure the GPIO inputs. It has eight ADC operation modes that correspond to different oversampling ratios. Modes vary in accuracy and and conversion time The battery monitor is run in 7 kHz or normal mode since the ADC has high resolution and low total measurement error.

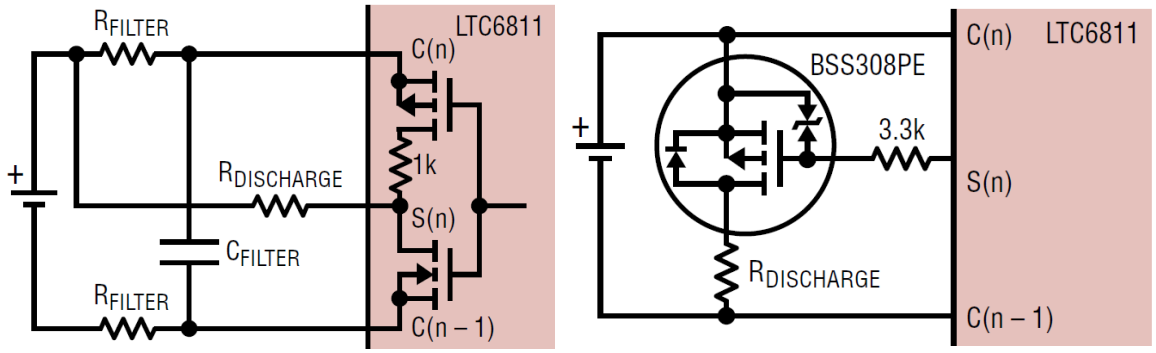
There are options regarding the number of GPIO to be measured as well as the desired ADC mode. The measurements are stored in the AVAR/AVBR (auxiliary) Register Group. Synchronous measurement of the cell voltages and GPIO ports with a single command allows consistent and time-stamped data collection. The reference voltage (V_{REF2}) is also measured and stored. V_{REF2} has a nominal voltage of 3 V. The voltage reference value is retrieved by the Micro-controller Unit (MCU) and used to perform thermistor temperature calculations.

When the cell voltage is measured, the results are compared to Over-voltage (OV) and Under-voltage (UV) thresholds that are stored in memory registers. If a cell's voltage exceeds these thresholds, its OV or UV flag bit in Status Register Group is set.

The battery monitor also supports carrying out self checks to ensure proper operations *i.e.* accuracy check: to verify the accuracy of a data acquisition system, multiplexer decoder check: to ensure the proper operation of each multiplexer channel and digital filter check to ensure proper percentage of 1s in a pulse density modulated bit stream. Additionally, an open wire check ensures no open wires between the ADCs and external cells [46].

4.2.3.3 Cell balancing

By default, the LTC6811 supports PCB. Each `S` pin output is connected to an internal N-channel MOSFET (see figure 4.2a) with a maximum on resistance of 25 Ω. The internal switches (MOSFETs) `S1` through `S12` are connected with external 100 Ω discharge resistor to passively balance cells with balancing current of less than 60 mA. For applications that require balancing currents above 60 mA, the `S` outputs are used to control external transistors (see figure 4.2b).



(a) Internal Discharge Circuit **(b)** External Discharge Circuit

Figure 4.2: Internal and External Discharge Circuits [17]

The discharge permitted (DCP) bit is kept high to allow discharge during cell since `S` pin discharge states do not change. If the DCP bit is low, `S` pin discharge states will be disabled while the corresponding cell or adjacent cells are being measured. The discharge N-MOSFET

is connected to an internal pull-up PMOS transistor with a low 1 kΩ series resistance that allows the external transistor to turn off during cell measurement.

4.2.3.4 Discharge Resistance Calculation

External discharge circuit ensures that the chip is not heated up due to cell balancing. An external balancing circuit is designed for a maximum discharge current of 80 mA since the FDV304P P-channel MOSFET is rated at 25 V, 350 mA. The system is set to tolerates a 3% imbalance in SoC. This imbalance is resolved in 2–3 hours. Taking a balance time T_D of 2.5 hours, the required balance current, I_D is given by;

$$I_D = \frac{SoC \times C_{releasable}}{T_D} = \frac{0.03 \times 3250}{2.5} = 39 \text{ mA} \tag{4.1}$$

Current discharge, I_D is directly proportional to the SoC multiplied by the battery capacity, $C_{releasable}$) and inversely proportional to the time taken to discharge (T_D). Given a nominal cell voltage, $V_{NOM} = 3.6$ V, discharge resistance is $R_{DISCHARGE} = {}^{3.6\text{ V}}/_{39\text{ mA}} = 92.3\ \Omega$. The P-channel MOSFET has a maximum on resistance, $R_{ON} = 1.5\ \Omega$ which reduces the required discharge resistance to 90.8 Ω. However, we use the much more available 100 Ω resistance which still gives us a discharge time less than 3 hours.

4.2.4 Temperature Sensor

NTC temperature sensitive resistors are used for sensing the temperature. They are connected to the battery monitor's `GPIO` pins. Each cell's anode has an NTC resistor attached to it. NTC resistors have a nominal resistance of 100 kΩ at 25 °C. A 100 kΩ resistor is connected together with the NTC sensor to form a potential divider as shown in figure 4.3 below.

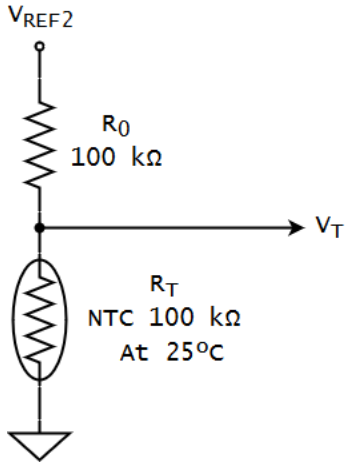


Figure 4.3: Potential Divider Circuit for NTC Temperature Sensor

The voltage drop across the divider is measured and stored by the battery monitor. The temperature is mapped using a temperature-resistance look-up table from the manufacturer's datasheet. Since the manufacturer does not include all temperatures, an interpolation function is applied to approximate the remaining temperature values.

The potential divider voltage output, V_T is calculated from: $V_T = V_s \times {}^{R_{REF}}/_{(R_T + R_{REF})}$. Given $R_{REF} = 100$ KΩ and supply voltage, $V_s = V_{REF2}$, The resistance, R_T of the NTC resistor at a given temperature is calculated by;

$$R_T = R_{REF} \times (\frac{V_{REF2}}{V_T} - 1)^{-1} \tag{4.2}$$

The battery monitor has five `GPIO` pins but we have 8 sensors *i.e.* 1 per cell. The output from each cell's temperature sensor is multiplexed using LTC1380 8-channel analogue multiplexer (see figure 4.4) [47]. Using pins `GPIO5` and `GPIO4` as `SCK` and `SDA` respectively, the battery monitor controls the multiplexer via Inter-Integrated Circuit (I^2C) communication to provide the voltage output from each thermistor into `GPIO1`. A low power operational amplifier, LTC6255, increases the multiplexer's output voltage. An alternative multiplexer is the SN74LV4051A-Q1 from Texas Instruments, however, we chose this design since it was simple (since it was clearly outlined in the datasheet) and could fulfil our requirements.

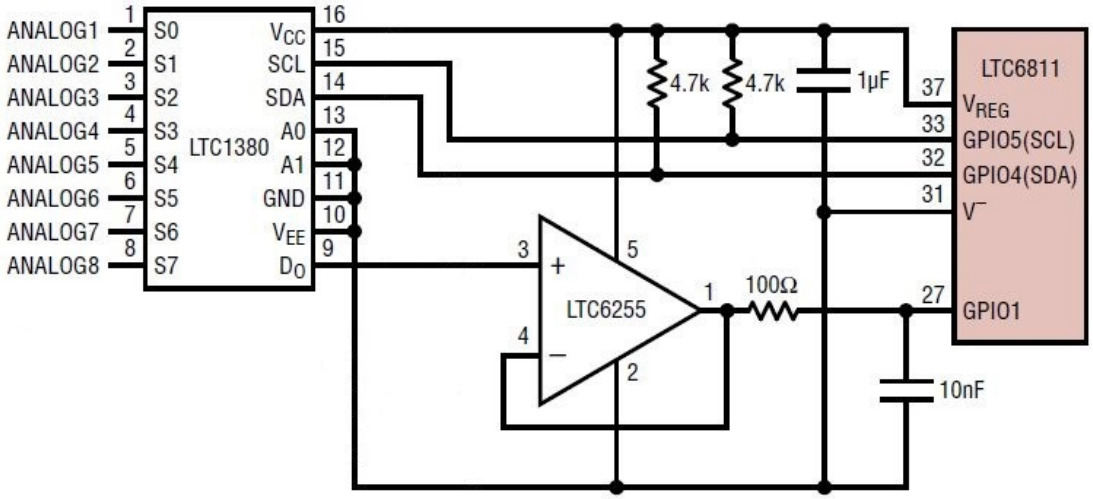


Figure 4.4: Temperature Sensor Multiplexer Design [46]

4.2.5 Micro-Controllers

The STM32F103C8T6 [48] MCU has ARM Cortex M3 architecture and can operate at 72 MHz. It has a 12-bit ADC offering high resolution and low total conversion error of 5 LSB. It also supports several communications interfaces such as USART, I^2C, SPI, and CAN communication. To simplify design, this same type of MCU is used for master and module controllers. Table 4.2 shows a summary of major MCU features:

The STM32F103C8T6 is a robust, low cost and high performance MCU. There are several development support resources, for example, the chip can be programmed using the popular Arduino software tools and libraries. It also supports CAN interface making it suitable for automotive applications.

Specification	**Value**
Supply Voltage Range	2 to 3.6 V
Supply Current Range	Max 50.3 mA in Run Mode (72 MHz, 105 °C)
	Max 32 mA in Sleep Mode (72 MHz, 105 °C)
Temperature Range	−40 to 125 °C
Communication Channels	CAN (2.0B Active)
	2 SPIs (18 Mbits/s)
Clock Frequency	72 MHz (max)
Standby Mode Current	5 µA
Sleep Mode Current	14.4 mA
Stop Mode Current	370 µA
Flash Program Memory	Size: 64 kB
	Endurance: 10,000 Cycles (−40 to 85 °C)
	Data Retention: 10 years (1000 cycle at 105 °C)
SRAM	20 kB
ADC	Number: 2
	Resolution: 12-bit
	Rate: 1 µs
	Channels: 16
	Range: 0–3.6 V
Processor Type	ARM Cortex M3

Table 4.2: STM32F103C8T6 ARM Micro-controller Specifications [48]

4.2.5.1 Micro-Controller Board

The *bluepill* is a breakout board for the STM32F103C8T6 MCU. It contains all essential connections for the MCU *e.g.* 8 MHz oscillator crystal, 3.3 V voltage regulator to allow use of a 5 V supply and micro USB port to power the board from a personal computer. Port `PC13` of the microcontroller is connected to to an indicator LED for easy prototyping. Appendix A.1 shows the board's circuit diagram.

4.2.5.2 Micro-Controller Replacement

Though the intention was to use the STM32F103C8T6 MCU, it was replaced with ATmega2560 [49] which was readily available. The ATmega2560 sits on the Arduino Mega 2560 breakout board. This change does not significantly affect the core application software since wrapper functions handle device initialisation (see sub-section 4.3.1). Execution time is also

not affected due to the low complexity of the application which allows us to operate the MCU at low frequency with satisfactory results. However, this change mainly affected the precision of program calculations mainly due to the lower resolution 10-bit ADC on the ATmega2560. We also replaced the M/S SPI communication with I^2C, since the ATmega2560 has only one 4-wire SPI port. Table 4.3 shows a comparison of the STM32F103C8T6 and ATmega2560.

Specification	**STM32F103C8**	**ATmega2560**
Supply Voltage Range	2 to 3.6 V, 3.3 V (nominal)	1.8 to 5.5 V, 5 V (nominal)
Supply Current Range	Max 50.3 mA in Run Mode (72 MHz, 105 ° C)	Max 12.4 mA in Active Mode (8 MHz, 85 °C)
	Max 32 mA in Sleep Mode (72 MHz, 105 °C)	Max 3.3 mA in Sleep Mode (8 MHz, 85 °C)
Temperature Range	−40 to 125 °C	−40 to 85 °C
Communication Channels	2 I^2C	1 I^2C
	2 SPIs (18 Mbits/s)	1 SPI (4 Mbits/s)
	CAN (2.0B Active)	-
Clock Frequency	72 MHz (max)	16 MHz (max)
Flash Program Memory	Size: 64 kB	256 kB
	Endurance: 10,000 Cycles (−40 to 85 °C)	Endurance: 10,000 Cycles
	Data Retention: 10 years (1000 cycle at 105 °C)	Data retention: 20 years at 85 °C
SRAM	20 kB	8,192 kB
Data EEPROM	-	4096 kB (Endurance: 100,000 Cycles)
ADC	Number: 2	1
	Resolution: 12-bit	10-bit
	Rate: 1 µs	Rate: 13–260 µs
	Channels: 16	16
	Range: 0–3.6 V	0–5.5 V
Processor Type	ARM Cortex M3	Microchip 8-bit AVR RISC

Table 4.3: Comparison of STM32F103C8 and ATmega2560 Specifications

4.2.6 Current Sensor

The ACS724LLCTR-30AB-T is a 30 A bi-directional Hall effect current sensor from Allegro microsystems [50]. It has a nominal sensitivity ($Sens$) of 66 mV/A and maximum total error, E_{TOT} of 5.5%. Its primary conductor has a low resistance of 1.2 mΩ. Differential sensing protects against common mode field interference making it highly resistant to Electro-magnetic Interference (EMI). An integrated shield greatly reduces capacitive coupling from current conductor to die. This reduced interference makes it suitable for high voltage automotive application. When the sensor has no current flowing through it, its output quiescent output voltage is, $V_{OUT(Q)} = {}^{V_{cc}}/_{2}$, where V_{cc} is the supply voltage. Since the current sensor has *ratio-metric* voltage characteristic, $V_{OUT(Q)}$ varies in direct proportion with V_{cc}. Given an output voltage $V_{OUT(IP)}$, the output current I_P is calculated by:

$$I_P = \frac{V_{OUT(IP)} - V_{OUT(Q)}}{Sens} \tag{4.3}$$

Hall effect current sensors encounter deviations during operation due to temperature changes and nearby magnetic fields and, therefore, require re-calibration after a period of prolonged operation. For example, the initial quiescent output voltage value at zero amperes is read off and any subsequent measurements have to be offset with that value. The biggest advantage of the Hall effect current sensor over a shunt-based current sensor is that it is inherently isolated with comparably similar sensitivity and accuracy [3]. This means there is no need for extra isolation components to protect the low voltage circuitry.

4.2.7 Digital Isolators

Digital isolators provide proper electrical isolation of the modules from each other and from the master. The LTC6811-2 battery monitor's SPI interface is already isolated. The digital isolators in this case are used to transmit control signals to other parts of the system such as control of relay drivers. The ADUM1400W, ADUM1401W and ADUM1402W [51] digital isolators from Analog Devices have a rated basic insulation of 2,500 V RMS and reinforced insulation for operating voltages up-to 400 V rms. These isolators operate at temperatures between −40 °C to 125 °C and support data rates between 2–90 Mbps. The ADUM1400W digital isolators have four channels in same direction hence suitable for driver isolation.

Digital isolators use magnetic coils to transmit digital signals over a barrier. The isolator works by encoding and decoding rising and falling edges of an input signal with 1 ns pulses *i.e.* two pulses for rising edge and one for falling edge. Each side of the isolator is independently powered. Digital isolators are preferred over opto-isolators due to their low power consumption, ability to support higher data rates, and lower degradation over time.

4.2.8 Pre-charge Contactor Relays

Due to the high cost of automotive relays, we chose to use printed circuit board high power relays for our contactors since they could well meet power limits (see table 4.1). The G2RL-1A-E-5DC relay's contacts are `open` when not powered *i.e.* normally-open configuration. Both the positive and negative battery terminals each have a contactor relay connected to them. A third relay is used for pre-charging the filter capacitor. The relay coil requires 5 V to close the contacts. The relay coil has a 62.5 Ω resistance requiring a minimum supply current of 80 mA.

Relays use an electromagnet to operate a mechanical switch. They ensure that the control circuit that operates the switch is not electrically connected to the switch itself thereby ensuring high protection. Mechanical relays are preferred over solid state relays due to their higher isolation resistance and absence of leakage current when contacts are open. Additionally, solid state relays generate high amounts of heat when used with high currents and voltages.

The relays would preferably be driven by MOSFET drivers due to their faster response. However, in this case we used the readily available NPN transistors (see figure 4.5). We added an allowance in the design so the transistor can be changed easily without need to change any other components. However, the voltage drop across the N-MOS or NPN will reduce the 5 V supply voltage by $\approx$ 0.2–0.9 V depending on the type of transistor used. NPN may have a lower voltage drop typically ≤ 0.2. Assuming a maximum voltage drop of about 1 V, a voltage supply of 6.1 V will result in a total voltage of $6.1 - 1 = 5.1$ V across the coils. This is sufficient to operate the relay coils.

4.2.9 Pre-charge Resistor and Filter Capacitor

A high power wire wound resistor is used for charging the filter capacitor to reduce the current flow when the positive contactor is connected. Wire wound resistors are tolerant to in-rush currents. The pre-charge time depends on the load resistance and capacitance. A 1 kΩ resistance and a 1 mF capacitance provide an estimated pre-charge time of 1 s.

The pre-charge resistor and filter capacitor form an RC circuit. The time constant of this pre-charge circuit is used to obtain the safe current for closing contactors. The time constant of the RC circuit is given by $\tau = R \times C$.

The voltage across the capacitor, V_c at any time, t during charging is given by $V_c = V_s(1 - e^{-t/\tau})$. At $t = 5 \times \tau$, the capacitor is almost fully charged and the voltage across the capacitor, $V_c = 0.98 \times V_s$ which drops the current through the resistor, I_t to 0.7% of it original value. For a nominal current of 3.25 A, the current flow at $t = 5\tau$:

$$I_{5\tau} = \frac{0.7}{100} \times 3.25 \text{ A} = 22.75 \text{ mA} \tag{4.4}$$

For a desired pre-charge time $T_{pre} = 1$ s with filter capacitance, $C_f = 1$ mF, we require a pre-charge resistance:

$$R_f = \frac{1 \text{ s}}{1 \text{ mF}} \times \frac{1}{5} = 200 \ \Omega \tag{4.5}$$

The total energy, E_f stored in the capacitor is:

$$E_f = {}^1\!/_2 \times C_f \times V_{batt}^2 = 0.5 \times 0.001 \times 67.2^2 = 2.258 \text{ J} \tag{4.6}$$

This gives a total power dissipation:

$$P_f = E_f / T_{pre} = 2.258/1 = 2.258 \text{ W} \tag{4.7}$$

and at the beginning of the pre-charge instantaneous power:

$$P_{if} = V_{batt}^2/R_f = 67.2^2/200\Omega = 22.58 \text{ W} \tag{4.8}$$

Wire wound resistors are designed to withstand such short spikes in power hence a 3 W pre-charge resistor is enough even at such a high instantaneous power. In addition to pre-charge time, the microcontroller also monitors the current flow using the current sensor to ensure that the current level is below the required limit. This ensures safety since variations in RC values lead to variations in pre-charge time. Figure 4.5 shows relay-driver circuit for the pre-charge circuit.

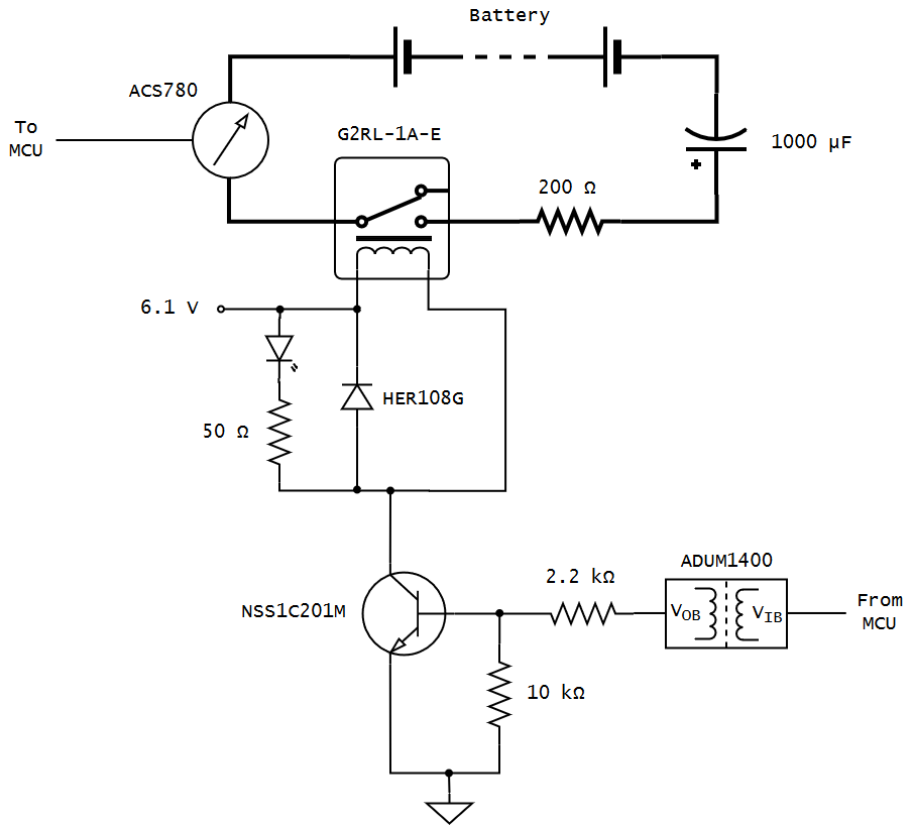


Figure 4.5: Relay and MOSFET driver Circuit for pre-charge

4.2.10 DC/DC Converters

The system design assumes an external main supply voltage of 12 V which is a standard voltage for Low Voltage (LV) circuitry in automotive applications. There are 4 major supply lines that draw from the main supply. This is achieved using LT8302 and LT3990 switching regulators. Switching regulators are preferred over linear voltage regulators dues to their low heat dissipation [52]. There are two non isolated lines and two isolated lines;

1. Line 1: 5 V supply for MCU and current sensor units
2. Line 2: 6.1 V supply for the pre-charge and contactor units
3. Isolated Line 1: Isolated 12 V supply for battery monitor units
4. Isolated Line 1: Isolated 5 V supply for the battery monitors' V_{REG}

4.2.10.1 Line 1: 5 V Supply

In our case, as part of design requirements from Infotiv AB, we assume that the 5 V supply is externally provided. Additionally, 5 V is a common transistor-transistor logic (TTL) supply voltage that could be part of the LV supply voltage lines in a BEV.

4.2.10.2 Line 2: 6.1 V Supply

Line 2 is achieved using LT3990 switching regulator (see Figure 4.6). The LT3990 is a constant frequency, current mode stepdown regulator [53]. It takes in an input voltage between 4.2–62 V.

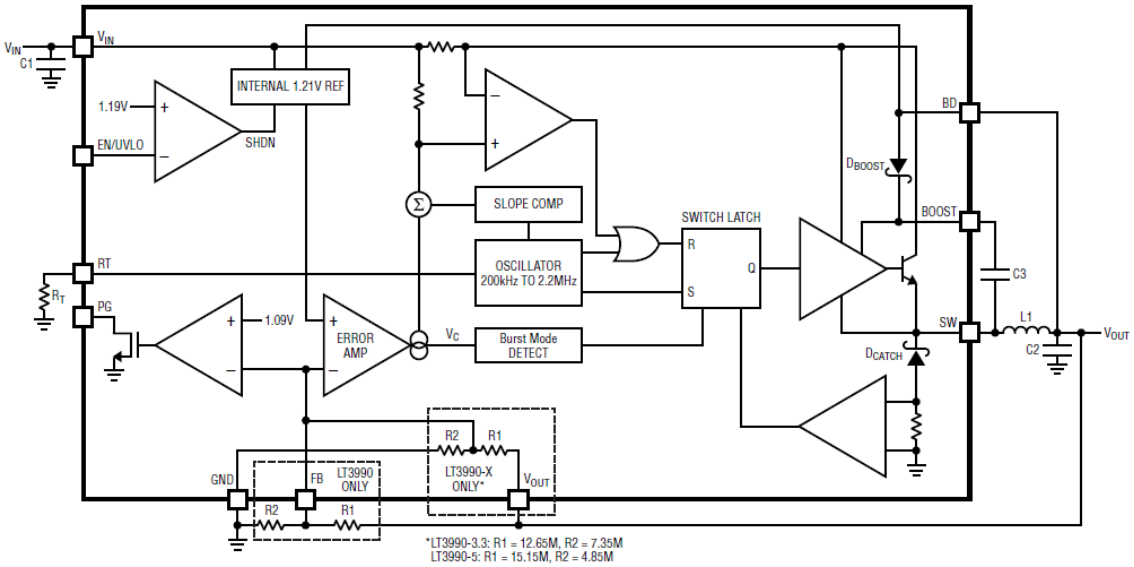


Figure 4.6: LT3990 Converter Block Diagram [53]

The LT3990 can be set to output any voltage by varying its feedback voltage . The feedback voltage is varied using a voltage divider *i.e.* changing R_2 while maintaining R_1 at 1 MΩ. R_2 value necessary to provide an output voltage of 6.1 V is chosen using equation 4.9:

$$R_2 = R_1 \times \left(\frac{V_{OUT}}{1.21} - 1\right)^{-1} = 1 \times 10^6 \times \left(\frac{6.1}{1.21} - 1\right)^{-1} = 247443.76 \approx 247 \text{ k}\Omega \tag{4.9}$$

LT3990 regulator uses a constant pulse-width modulation architecture that can be programmed to switch from 200 kHz to 2.2 MHz using a resistor, R_T tied from the `RT` pin to ground. R_T is set to 374 kΩ to give a frequency of 400 kHz.

The regulator setup (see figure 4.7) is simulated to ensure that it can provide the necessary voltage and current to drive the relays. The regulator is simulated using LTSpice software with input voltage varying between 6.2–60 V. The relay coils are represented by resistors with corresponding coil resistance.

Figure 4.8 shows the input voltage, V(vin), output voltage, V(vout) and output current, I(Coil1) flowing through one of the substitute coil resistances[1]. As can be observed the output current and voltage remain relatively stable enough to maintain the relay-coil in intended working condition *i.e.* V(vout) ≈ 6.1 V and I(Coil) ≥ 80 mA.

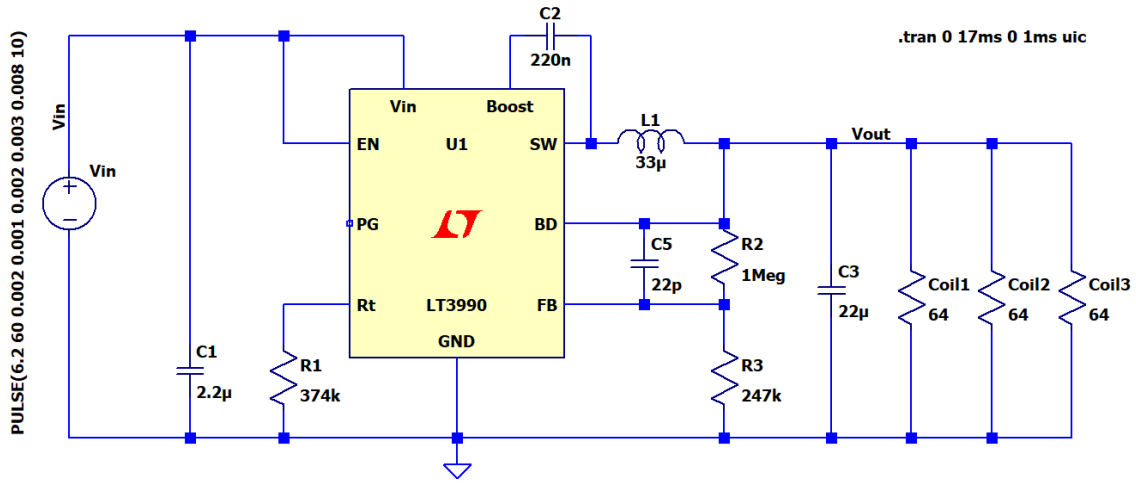


Figure 4.7: LT3990 6.1 V Output Simulation Setup

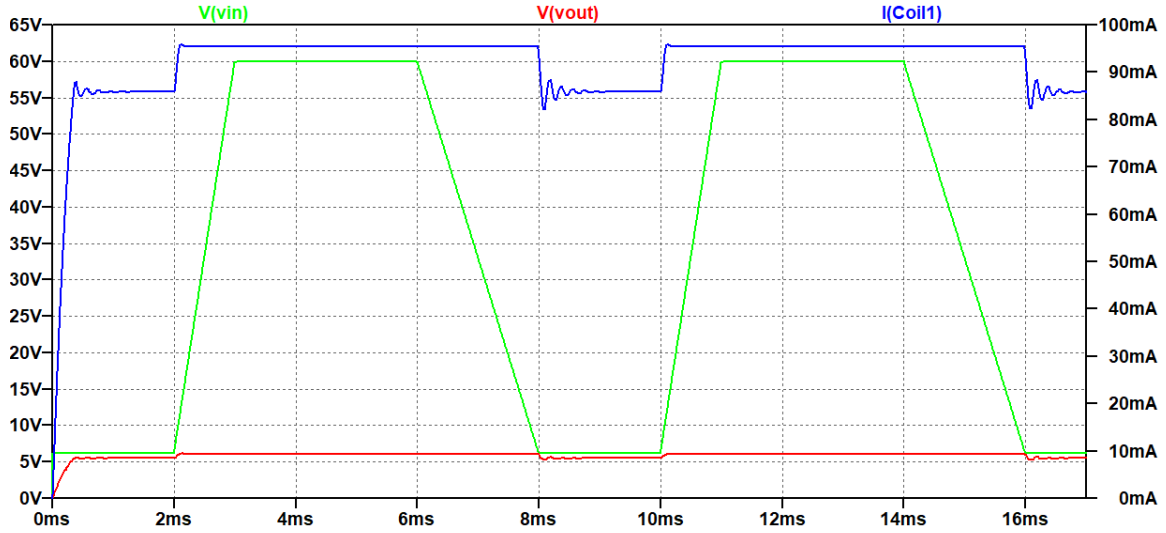


Figure 4.8: LT3990 6.1 V Output Simulation Results

4.2.10.3 Isolated Line 1: 12 V Supply

Isolated Line 1 voltage is achieved using a LT3802 switching regulator and transformer that form an isolated flyback converter (see figure 4.9) [54]. The LT8302 is a current mode switching regulator IC designed specially for the isolated flyback topology. It has an input voltage range of 3–42 V. The LT8302 samples the isolated output voltage through the primary-side flyback pulse waveform thereby requiring neither opto-isolator nor extra transformer winding

[1] A relay component for simulation with LTSpice could not be found. A resistor substitutes the relay coil resistance. The coil inductance is ignored since it is quit low and does not significantly affect simulation results. The coil inductance directly affects relay turn-on and turn-off delays that are accounted for in the design.

for regulation. The output voltage is always sampled on the SW pin when the secondary current is zero. This improves load regulation without the need of external load compensation components.

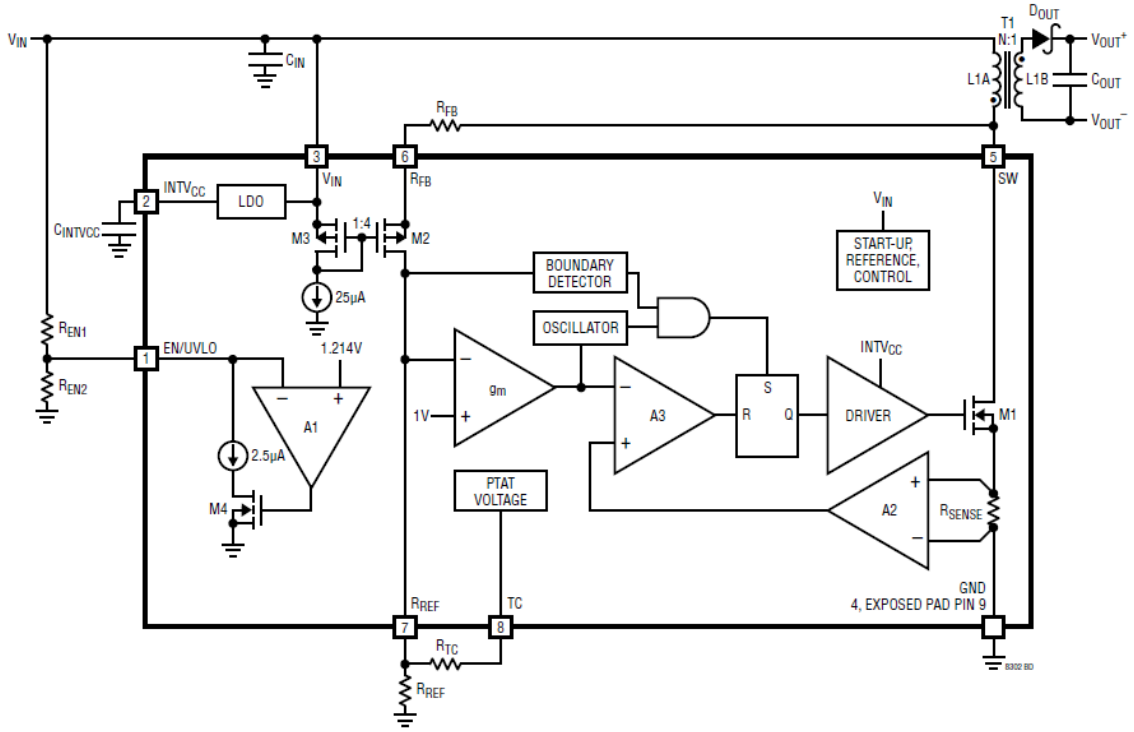


Figure 4.9: LT8302 Flyback Converter Block Diagram [54]

The LT8302 usually operates in two modes: Quasi-Resonant Boundary Mode Operation for heavy loads, and Discontinuous Conduction Mode Operation for light loads [54]. The R_{FB} and R_{REF} resistors are external resistors used to set the output voltage. When the power switch M1 turns off, the SW pin voltage rises above the V_{IN} supply. The amplitude of the flyback pulse, *i.e.* the difference between the SW pin voltage and V_{IN} supply, is given as:

$$V_{FLBK} = (V_{OUT} + V_F + I_{SEC} \times ESR) \times N_{PS} \tag{4.10}$$

where V_F is the output diode forward voltage, I_{SEC} is the transformer secondary current, ESR (Effective Serial Resistance) is the total impedance of secondary circuit and N_{PS} the transformer effective primary-to-secondary turns ratio [54]. The internal reference voltage, $V_{REF} = 1$ V, feeds to the non-inverting input of a sample-and-hold error amplifier. The relatively high gain in the overall loop causes the voltage at the R_{REF} pin to be nearly equal to the internal reference voltage V_{REF}. The resulting relationship between V_{FLBK} and V_{REF} can be expressed as:

$$V_{FLBK} = V_{REF} \times \left(\frac{R_{FB}}{R_{REF}} \right) \tag{4.11}$$

Combination of equations 4.10 and 4.11 yields an equation for V_{OUT}, in terms of the R_{FB} and R_{REF} resistors, transformer turns ratio, and diode forward voltage;

$$V_{OUT} = V_{REF} \times \left(\frac{R_{FB}}{R_{REF}}\right) \times \left(\frac{1}{N_{PS}}\right) - V_F \tag{4.12}$$

Transformer leakage inductance on either the primary or secondary causes a voltage spike to appear on the primary after the power switch turns off. In addition to the voltage spikes, the leakage inductance also causes the SW pin ringing for a while after the power switch turns off. To clamp and damp the leakage voltage spikes, an (RC + DZ) snubber circuit (see figure 4.10) is recommended. The RC (resistor-capacitor) snubber quickly damps the voltage spike ringing and provides great load regulation and EMI performance. The DZ (Diode-Zener) ensures well defined and consistent clamping voltage to protect SW pin from exceeding its 65 V absolute maximum rating.

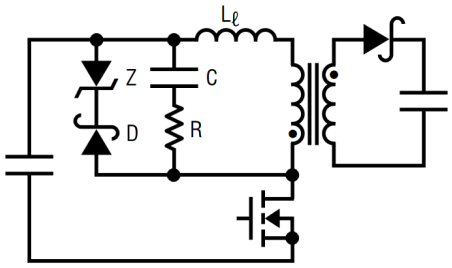


Figure 4.10: (RC + DZ) Snubber Circuit [54]

From equation 4.12 and other related design guidelines from the LT8302 datasheet, a setup of the flyback regulator is simulated using LTSpice software (see figure 4.11). In the setup, $R_{FB} = 178\ \text{k}\Omega, R_{REF} = 10\ \text{k}\Omega, N_{PS} = 1:1$, and $V_F = 0.81$ V to give a regulated output voltage of 12 V. The zener diode in the snubber circuit has a breakdown voltage of 24 V and the output zener diode clamps the output voltage to 13 V. The transformer coils have an inductance of 9 µH at a frequency of 10 kHz. The regulator has a maximum output current of 400 mA and switching frequency of 711 kHz.

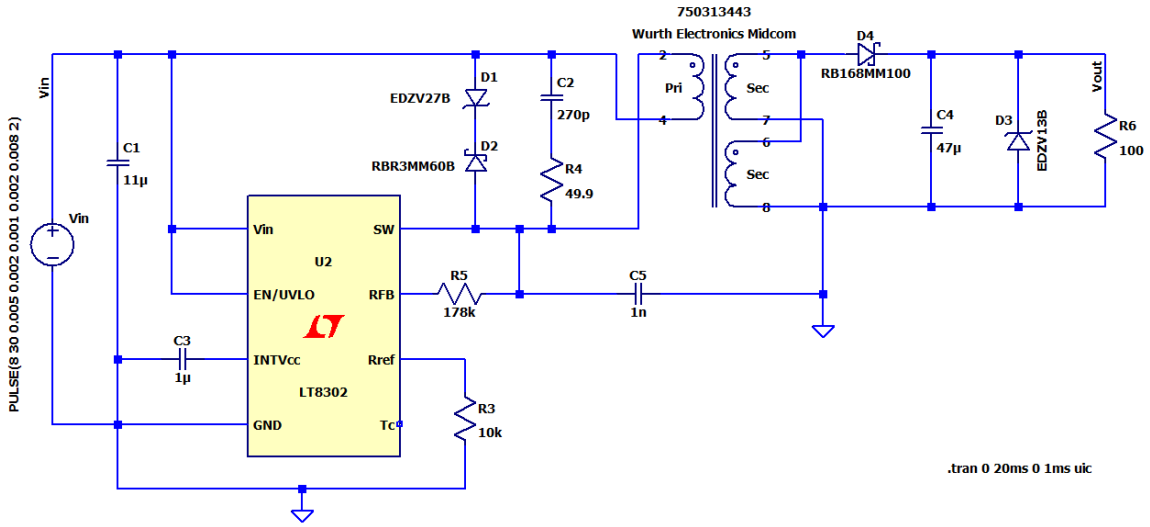


Figure 4.11: LT8302 Isolated 12 V Output Simulation Setup

Figure 4.12 shows the simulation results. Input voltage, V(vin), output voltage, V(vout) and

output current, I(R6) flowing through 100 Ω resistor. As can be observed, the output current and voltage remain relatively stable at *i.e.* V(vout) ≈ 12.5 V and I(R6) ≈ 134 mA, even with input voltage varying between 8.2–30 V. This is enough power output to reliably run the battery monitor.

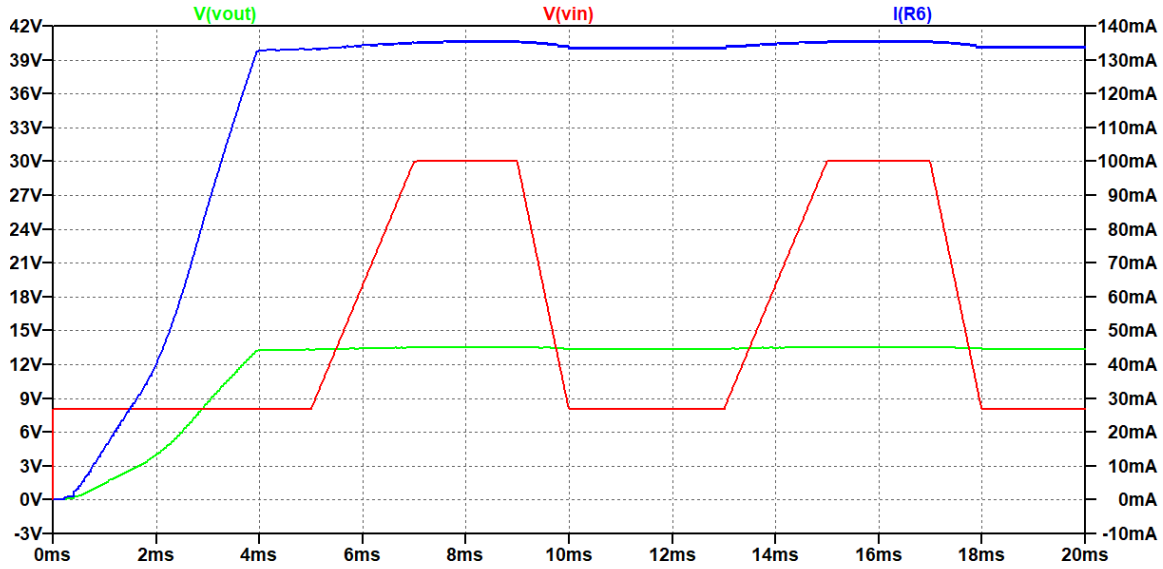


Figure 4.12: LT8302 Isolated 12 V Output Simulation Result

4.2.10.4 Isolated Line 2: 5 V Supply

Isolated line 2 is achieved using LT3990-5 switching regulator (see Figure 4.6). The LT3990-5 is a variant of the LT3990 that is set to an output of 5 V. Its feedback voltage divider resistances are internally set to $R_1 = 15.15$ MΩ and $R_2 = 4.85$ MΩ. This regulator is supplied by the isolated 12 V output. It therefore acts as a step-down stage for the isolated 12 V to 5 V. It powers the battery monitor `VREG`, multiplexer and operational amplifier.

4.3 Software Description

The software is written in C/C++ to run on all common MCUs. In order to cover a wide range of devices, the software presents generic interfaces to the application battery management logic through the use of wrapper functions to hide device dependent routines. The software is built with anticipation of scalable implementation and as such accommodates running of multiple devices. This is achieved by giving MCUs and battery monitors addresses. All commands include an address. The master and module controllers share some functions since both controllers are expected to operate to a certain degree as individual BMSs (see sub-section 2.4.8). Figure 4.13 shows the general program flow with startup, config, monitor and fault system states.

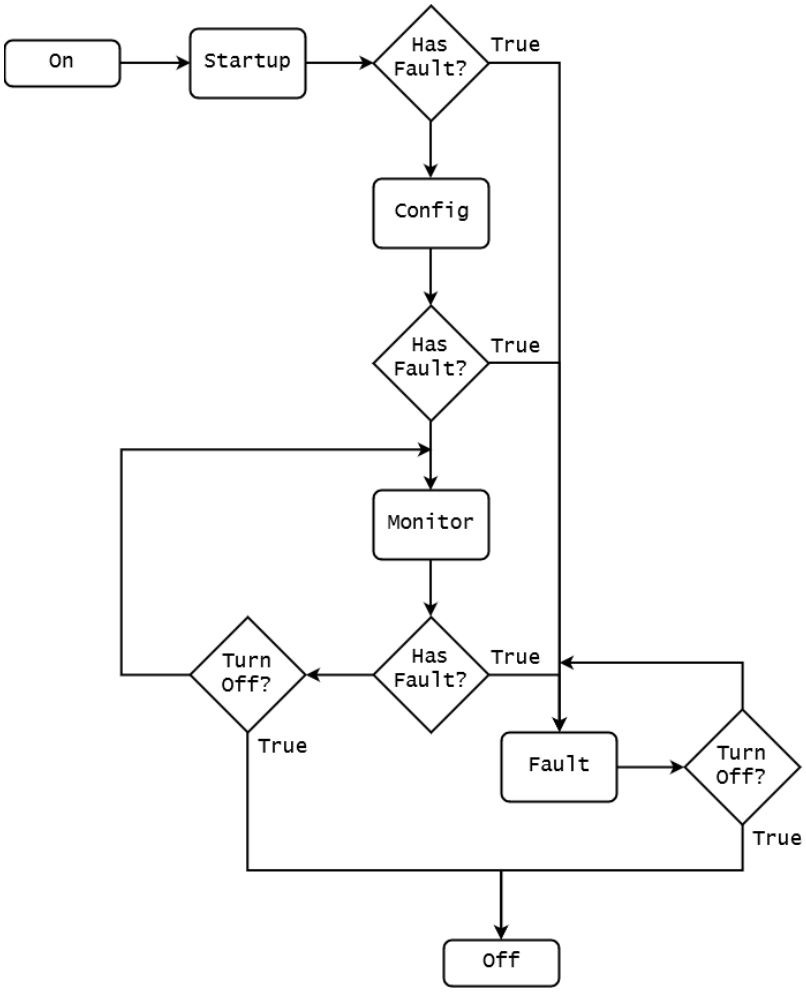


Figure 4.13: Program Flow With Startup, Config, Monitor and Fault Modes

4.3.1 Micro-controller Configuration

The MCU implements both the startup and config states at configuration. Since the same types of MCU is used for both the master and module controllers, the underlying MCU initialisation is the same. However, there some differences. For example, the master and module initialise different GPIO pins and the module MCU, unlike the master, also initialises the battery monitor at the application level.

Under startup the MCU performs device initialisation. MCU device initialisation involves configuration of communication interfaces (*i.e.* SPI and I^2C), GPIO pins, System timers and A/D Converter. In order to make the software more generic and scalable, wrapper functions have been built around the initialisation routines *i.e.* `init_spi()`, `init_gpio()`, `init_timer()`, `init_adc()`. The application simply calls these functions to initialise the device.

Under config, the MCU performs application initialisation and configuration. MCU application initialisation mainly involves setting system operating limits for voltage, current and temperature (see table 4.1) and initialising peripheral devices such as battery monitor and current sensor (*e.g.* calculating current sensor initial offset).

Since we were not able to use CAN or SPI (see sub-section 4.2.5.2), the MCUs were connected over an I^2C bus. I^2C protocol inherently supports M/S architecture and device addressing. Each MCU has its own address that which distinguishes its communications on the common I^2C bus. The addresses have a common offset and are simply consecutive numbers. The master only needs to know the number of MCUs available and it will be able to communicate to all of them.

4.3.2 Battery Monitor Configuration

The battery monitor has two types of registers: data and control registers. Data registers store the converted ADC values and different state values such as internal die temperature. Control registers store configurations that specify a required functionality. The registers are divided in register groups [46]. The CFGR stores the major configurations for the battery monitor (see figure 4.14). The MCU initialises the battery monitor by setting CFGR register values.

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGR0	RD/WR	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	REFON	DTEN	ADCOPT
CFGR1	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGR2	RD/WR	VOV[3]	VOV[2]	VOV[1]	VOV[0]	VUV[11]	VUV[10]	VUV[9]	VUV[8]
CFGR3	RD/WR	VOV[11]	VOV[10]	VOV[9]	VOV[8]	VOV[7]	VOV[6]	VOV[5]	VOV[4]
CFGR4	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGR5	RD/WR	DCTO[3]	DCTO[2]	DCTO[1]	DCTO[0]	DCC12	DCC11	DCC10	DCC9

Figure 4.14: Battery Monitor CFGR Registers [46]

The ADCOPT selects the ADC mode, GPIOx configures the GPIO pins (as input or output pull down on/off), VUV sets UV, VOV sets OV and DCCx configures cell discharge switches [46].

4.3.2.1 Communication

The module controller can read measured values from the registers by issuing commands on the isolated 4-wire 1-Mbps SPI. The 4-wire serial port is configured to operate using CPHA=1 and CPOL=1. To minimise errors during communication, error checking is performed on data sent over the SPI using Packet-Error-Code (PEC). The PEC is a 16-bit cyclic redundancy check value calculated with the initial PEC value of `0000000000010000` for all bits in a register group in the order they are passed and the characteristic polynomial: $x^{15} + x^{14} + x^{10} + x^8 +$

$x^7 + x^4 + x^3 + 1$ [46]. The PEC is calculated and sent in an SPI write command. A PEC is also calculated and sent back in an SPI read after read/write operations on the SPI.

4.3.2.2 Protocol Key Format

LTC6811-2 commands have a 16-bit command code: 11-bit command code that defines the command functionality, and 5-bit code for the addressing, as shown in figure 4.15. The battery monitor will respond to a command only if the address bits [6:3] match the physical address mapped by pins `A3-A0`. Since we use one battery monitor, all the address pins are grounded resulting in address `0`.

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	WR	1	a3*	a2*	a1*	a0*	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

Figure 4.15: Battery Monitor Address Command Format [46]

4.3.3 Scheduling Scheme

While in the monitor mode, the MCUs run the BMS application functionalities in a program loop according to scheduling scheme (see figure 4.16). All BMS functions are performed every second and spread out at 100, 200, 400, 600, 800 and 1000 ms. This gives a sampling frequency between 1–10 Hz (see sub-section 2.3.2).

For increased accuracy, voltage and current measurements are carried out every 100 ms. Both simulated and actual urban current and voltage driving profiles indicate low error rates at 10 Hz sampling frequency [26]. However, the SoC does not change much when measured at sampling frequency between 1–10 Hz, and thus can be safely calculated at 800 ms intervals. The temperature LICs changes much more slowly than voltage and can thus be safely sampled every 600 ms. Other activities such as checking limits are done after corresponding values have been measured. The MCUs store messages in send/receive buffers. The buffers are checked every 1 s for messages to send or process.

4.3.4 Voltage Management

The battery monitor stores voltage values as unsigned 16-bit values. To minimise the effects of noise during measurement, a moving average of the measured voltage, V_{Cx} is calculated as shown in equation 4.13. The total measured voltage of the battery is also computed and stored. Each cell's measured voltage is compared with the OV and UV limits set in the system. If any cell exceeds these limits, a system fault is generated and the system transitions to Fault mode.

$$V_{Cx}[t] = \frac{V_c[t-1] + V_c[t]}{2} \tag{4.13}$$

4.3.4.1 Voltage Equalisation

Due to the close correlation between cell voltage and SoC, the BMS ensures that the voltages of the cells are similar. Since we employ the short board effect battery SoC estimation method

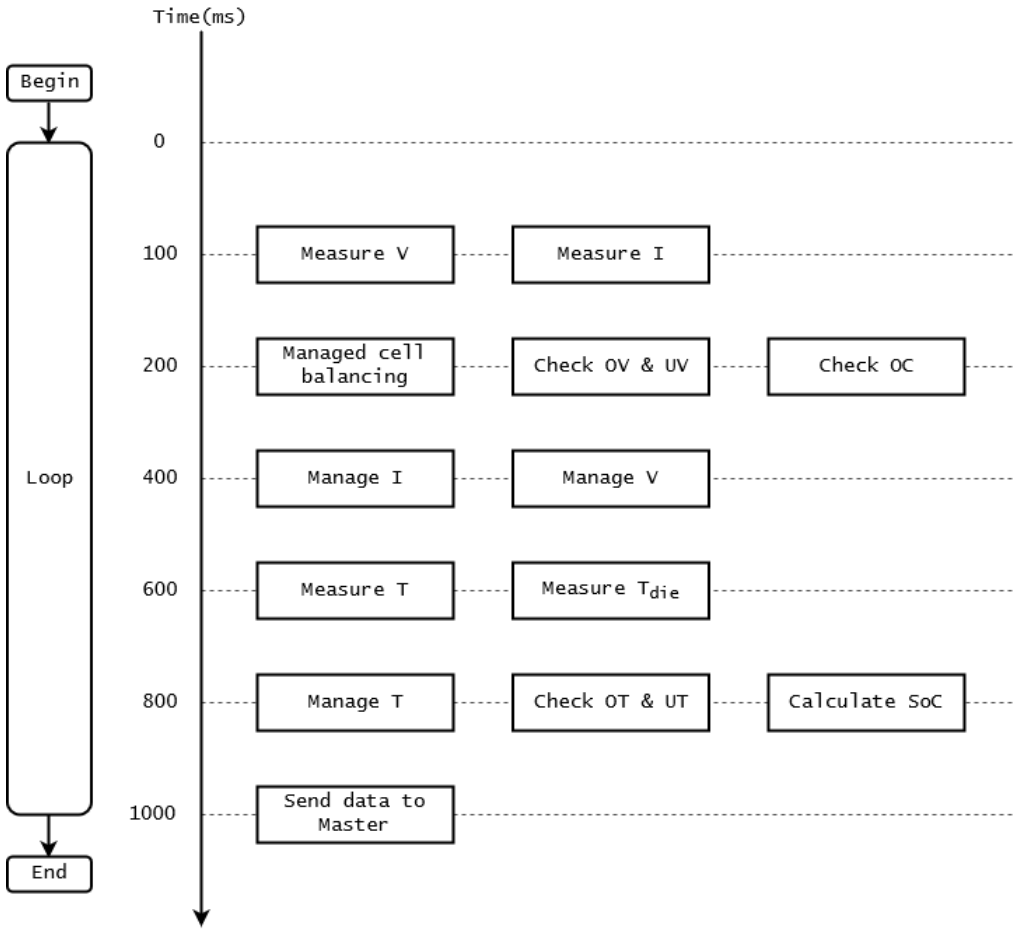


Figure 4.16: Monitor mode software schedule

(see 2.3.4.1), all cell voltages are kept close to the most discharged cell. Each cell's voltage, V_{Cx} must be within a small $\Delta V = \pm 500$ mV deviation from the lowest cell voltage, V_{LO} *i.e.* $V_{Cx} - V_{LO} < \Delta V$. Figure 4.17 shows the equalisation flowchart for a cell.

If a cell's voltage is above $V_{LO} + \Delta V$ the MCU configures the battery monitor to switch on that corresponding cell's `S` pin for the calculated *bleed* period. A log of currently balancing cells is maintained to avoid re-configuring pins that are already discharging. If the cell's voltage is equalised before the bleed period expires, then the MCU simply configures the battery monitor to stop the bleed.

4.3.5 Current Management

Current is measured using MCU's A/D conversion of the current sensor's output. Over time, the current sensor's quiescent offset shifts. Therefore, the current sensor's quiescent output voltage $V_{IOUT(Q1)}$ is calculated by taking the average of 10 successive ADC readings before current begins to flow through the sensor.

While the current is flowing, the supply voltage V_{CC} of the current sensor is also measured. The ACS724 has ratiometric sensitivity which varies with V_{CC}. Therefore, the MCU also reads the current sensor's supply voltage. The V_{CC} is measured using a potential divider

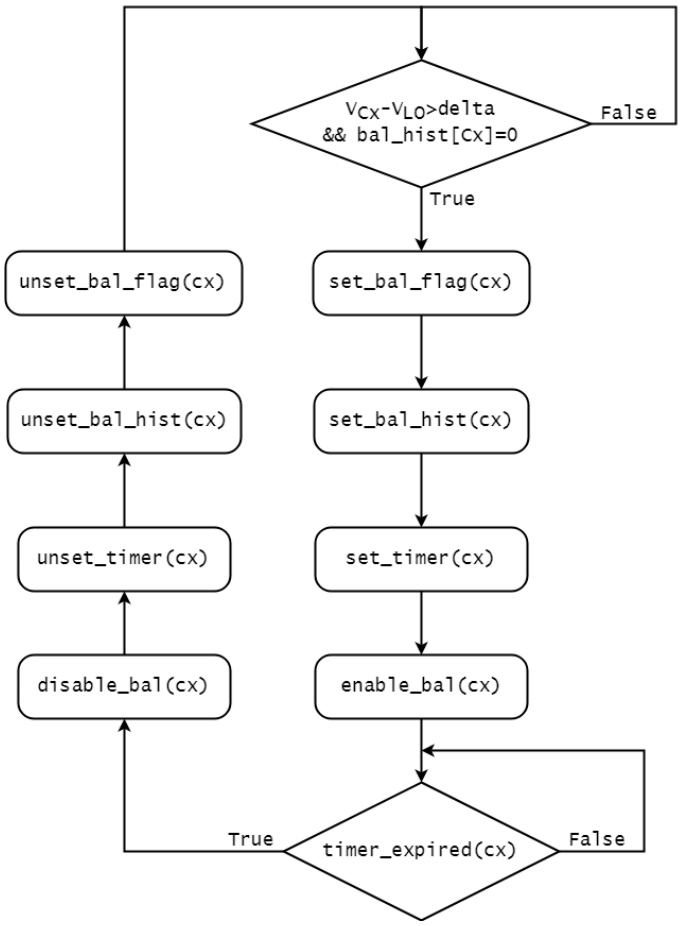


Figure 4.17: Cell Balancing Flow

with 2 MΩ resistors. The read value is simply multiplied by two to get the actual V_{CC}. Using the current sensor's ratiometric coefficient, $SENS\_RAT\_COEF = 1.3$, the sensitivity is calculated as;

$$SENS(V_{CC}) = SENS(5V) \times \left[1 + \frac{(V_{CC} - 5V) \times SENS\_RAT\_COEF}{5V}\right] \tag{4.14}$$

The actual current is calculated using equation 4.3. Eight successive current values are stored and used in SoC calculation. Each time the current is measured, it is compared with the maximum current limit. If the measured current is above this value, a system fault is generated and the system goes to Fault mode.

4.3.6 Temperature Management

The temperature sensor outputs are multiplexed via the battery monitor through an I^2C interface. When reading cells temperature, LTC1380 I^2C protocol commands are written to the battery monitor's COMM register group. The COMM register stores all data and control bits required for I^2C or SPI communication to a slave devices [46]. The protocol commands contain the multiplexer's address and selected multiplexer channel (see figure 4.18). Since a single multiplexer is used, its given address 0. The channels range from

0(`0b000`)–7(`0b111`). The MCU then commands the battery monitor to write the commands to the multiplexer through the I^{2}C interface. The multiplexer selects the specified channel and outputs the analogue temperature sensor voltage value to the battery monitor `GPIO1` pin. The MCU commands the battery monitor to perform A/D conversion of this value and reads the converted value from the auxiliary register group. The process is repeated for all eight channels corresponding to the eight cells.

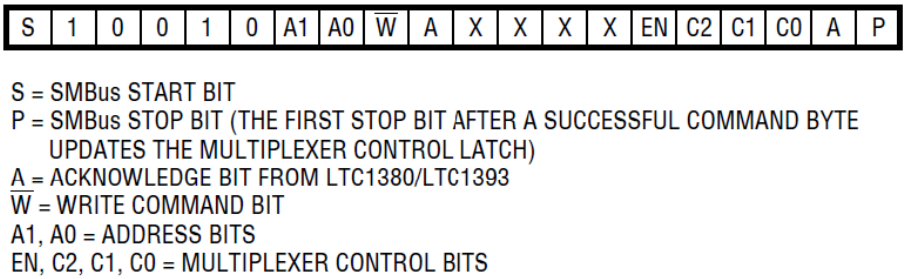


Figure 4.18: LTC1380 Multiplexer I^{2}C Send Byte Protocol [47]

Read temperature sensor voltages are converted to temperature using equation 4.2 and manufacturer's temperature-resistance look-up table, as outlined in sub-section 4.2.4.

4.3.6.1 Temperature Equalisation

Each cell's temperature, T_{Cx} is compared with the moving average temperature of all cells, $T_{AVG(MOVING)}$. Each cell's temperature must be within $\Delta T = \pm 2\,^{\circ}\text{C}$ of $T_{AVG(MOVING)}$. It is our intention to implement air cooling in the system, however, this is not possible. Therefore, the system is configured to generate a fault if any cell's temperature is outside $T_{AVG(MOVING)} \pm \Delta T$ or exceeds the set over-/under-temperature limits.

4.3.7 State of Charge Estimation

For simplicity, the SoC is estimated using two methods: ampere-hour integral (AmpHr) and EKF. Since OCV-SoC curve for the NCR18650B cells is largely linear between 4–3 V, we use AmpHr method for the first 85% of the nominal SoC (see figure 4.19). AmpHr has a much simpler implementation and provides accurate enough result. However, for closer inspection of the measurement, we use EKF algorithm for the SoC for last 15% of nominal SoC because the the OCV-SoC curve tends to become exponential at lower SoC [45]. More accurate measurement at lower SoC prevents accidentally over-drawing charge from the cell.

In order to use AmpHr method, the continuous integral function represented by equation 4.15 is converted to its discrete form; using a rectangular approximation for integration and a suitably small sampling period, Δt [55];

$$SoC_{k+1} = SoC_k - \left(\frac{\eta \Delta t}{C_n} i_k\right) \tag{4.15}$$

where SoC_k is the sample SoC, i_k is the sampled current and C_n is the nominal cell capacity. The Coulomb efficiency, $\eta \approx 1$. The terminal voltage and the current are measured at the same time. A small sampling period, $\Delta t = 100$ ms is chosen (see sub-section 4.3.3).

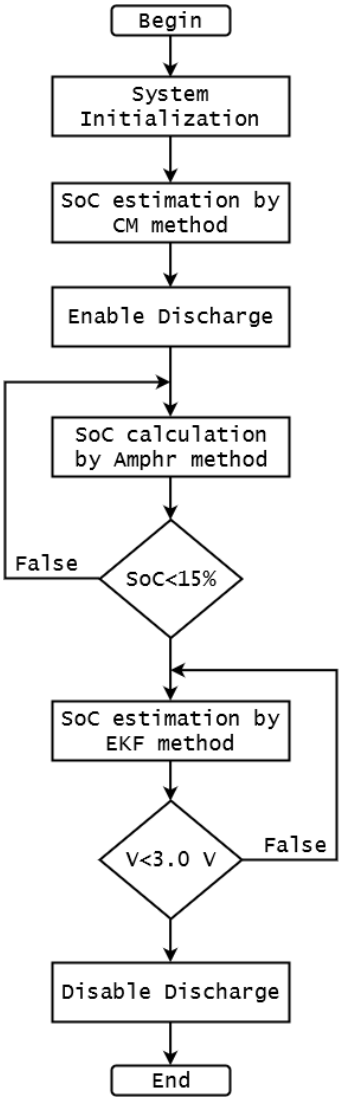


Figure 4.19: SoC Calculation Flow

4.3.8 Precharge Control

The master controls pre-charge relay contactors in simple sequence as described in table 4.4. The negative contactor is closed first. The pre-charge contactor is closed next. Two conditions must be fulfilled before the positive contactor is closed. The first condition is that the charge time should be equal to the maximum charge time, $T_{pre} = 1$ s. The second condition is that the current flowing through the filter capacitor, I_{Cf}, should be less or equal to the minimum current flow $I_{5\tau}$. Both conditions must be fulfilled for the positive contactor to close. Ideally $I_{5\tau}$ should be reached in $\approx T_{pre}$ seconds. After closing the positive contactor, the pre-charge contactor is opened after $k = 500$ ms. The value of k is greater than the manufacturer-defined time it takes to close/open the mechanical relay contactors. According to the datasheet this time is 15 ms.

Activity	**Contactor**			**Status**
	Negative	**Precharge**	**Positive**	
Connect HV	OFF	OFF	OFF	DISCONNECTED
	ON	OFF	OFF	
	ON	ON	OFF	
	`wait(`T_{pre} `AND` $I_{Cf} \leq I_{5\tau}$`)`			
	ON	ON	ON	CONNECTED
	`wait(`k`)`			
	ON	OFF	ON	
Disconnect HV	OFF	OFF	OFF	DISCONNECTED

Table 4.4: Pre-charge Control Sequence

5

Experimental Setup and Results

Hardware setup and software development are done simultaneously depending on the functionality that is being tested. It was not possible to do a wide variety of tests on the system such as the heat generated during operation or effects of EMI, due to the limited time for the project.

5.1 Hardware

In the hardware setup, several regular-sized discrete components were used which required more space that a conventional circuit board. The components were grouped into units (see table 3.1) and put on the same circuit board (bread board). Figure 5.1 shows the setup of the hardware components with one module and master.

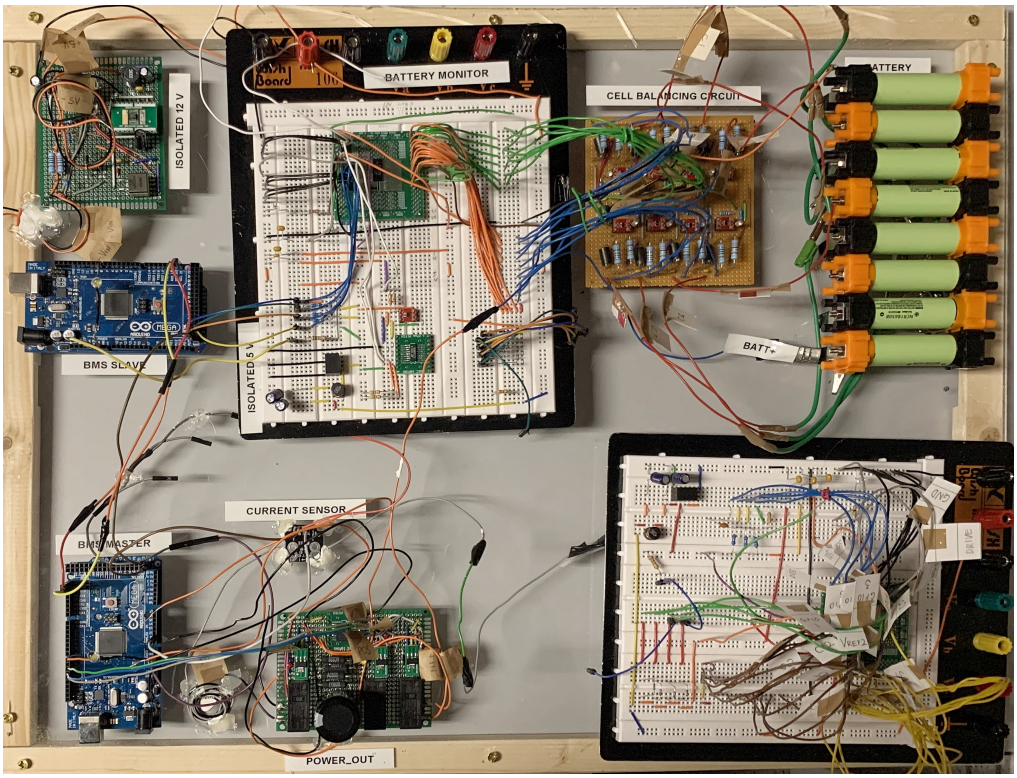


Figure 5.1: Final Assembled BMS Hardware

5.1.1 Battery Module and Battery Pack

Figure 5.2 shows the 8-cell BMs and figure 5.3 shows the BP. The cells are held by interlocking contacts/caps on both ends of the cell enabling the BP can take on different shapes. Each cell with caps is 22 mm × 22 mm × 93 mm. Subsequently, each BM has a total length of 176 mm resulting in BP dimensions of: 176 mm × 44 mm × 93 mm.

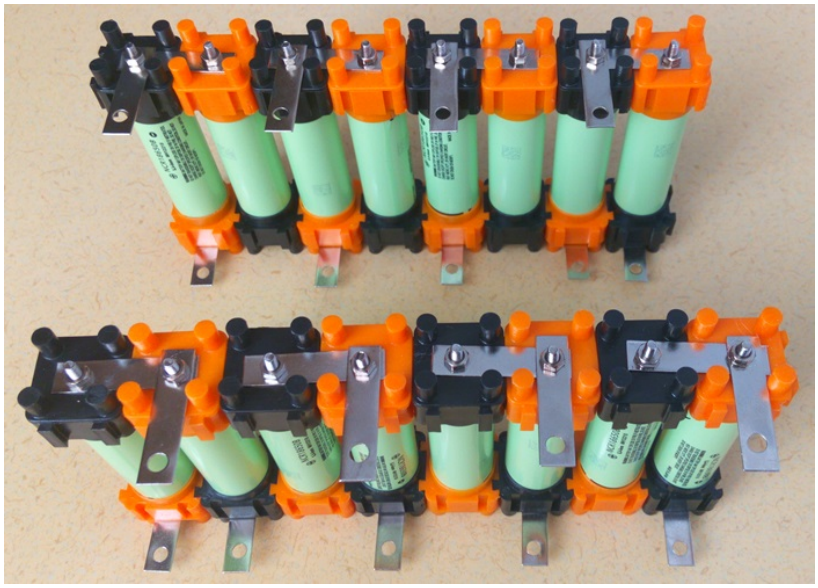


Figure 5.2: Battery Modules

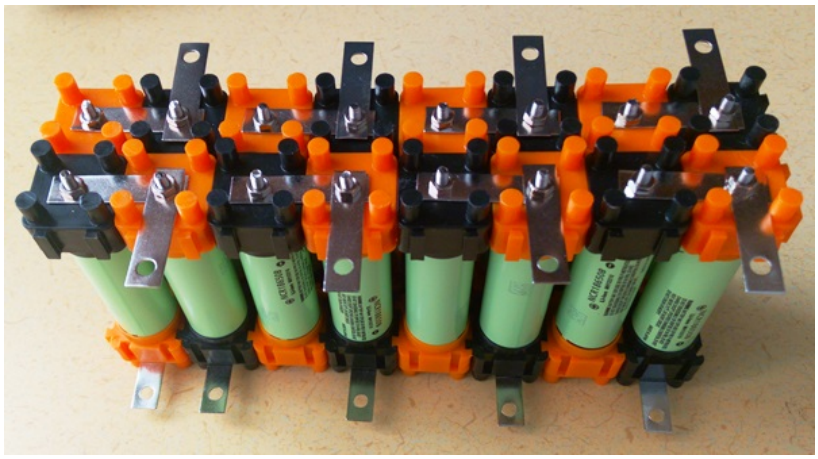


Figure 5.3: Battery Pack

5.1.2 Isolated Power Supply

Figure 5.4 shows the two isolated power lines were mounted on the same breadboard; the yellow rectangle shows the LT3990, the green rectangle shows the isolation transformer and the pink rectangle shows the LT8302.

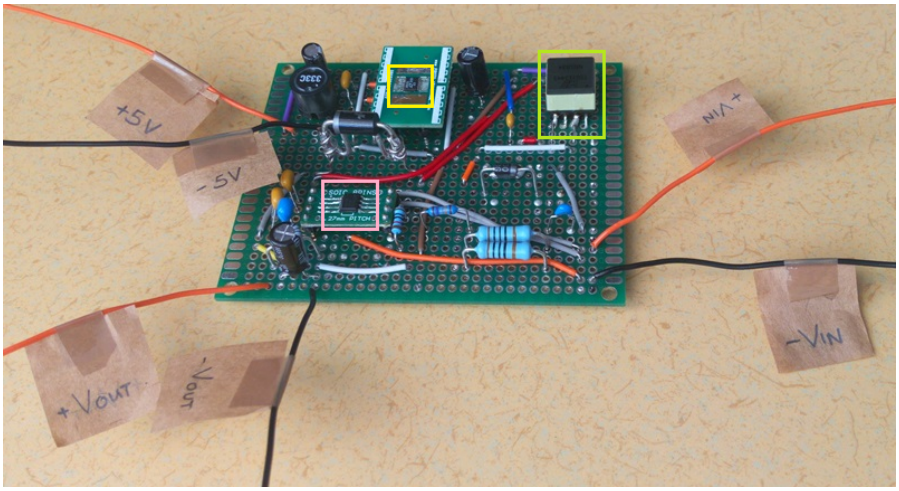


Figure 5.4: Isolated Power Supply Unit

5.1.3 Current Sensor

Figure 5.5 shows the current sensor; the grey wires connect to the current conductor, the orange wire is the power supply, the green wire sensor output and the black wire is the ground.

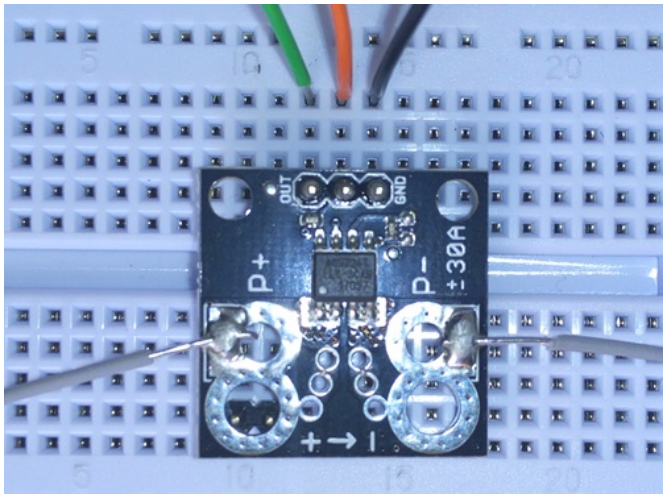


Figure 5.5: Current Sensor Unit

5.1.4 Precharge Unit

LEDs were added to the design in order to indicate which contactor is closed. Figure 5.6 shows the pre-charge unit setup; the blue rectangle shows the power supply to the pre-charge unit, the green rectangle shows power supply to the input-end of the digital isolator, the black rectangle shows the negative HV line and the red rectangle shows the positive HV line.

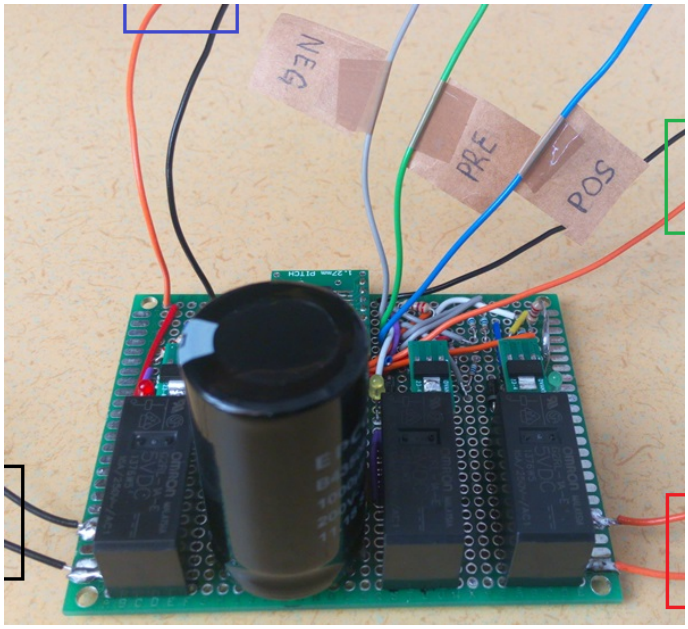


Figure 5.6: Pre-charge Unit Setup

The functioning of the contactors is tested and the results are displayed on an oscilloscope as shown in figure 5.7; the yellow signal is the capacitor voltage, blue is the pre-charge contactor control signal, violet is the positive contactor control signal and green is the negative contactor control signal. The pre-charge time is ≈ 1 s.

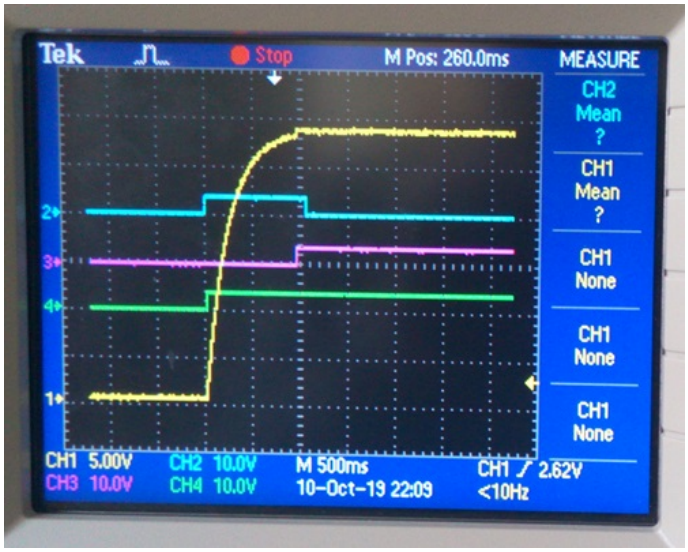


Figure 5.7: Pre-charge Unit Contactor Control Signals and Capacitor Voltage

5.2 Testing Challenges

Since the hardware was divided into units, we were able to test some of the system units. The minimum hardware required to test system functionality included: a module controller, battery monitor, current sensor, temperature sensing unit, isolated power supply unit, and pre-charge unit. We successfully tested the isolated power supply and pre-charge units hardware and software functionalities. However, due to the failure of other units it was not possible to perform certain integration tests and subsequently a complete system test was not could be carried out.

Testing challenges were caused mainly due to hardware errors that occurred in the LTC6811HG-2 battery monitor chip. Using the battery monitor self tests (see sub-section 4.2.3.2), we were able to find out that the chips had developed internal ADC and filter errors resulting in invalid voltage and GPIO readings. As a result, we could not perform tests on the temperature and voltage management functionalities since they were heavily dependent on the proper functioning of the battery monitor. Due to limited time, we could not investigate the cause of these errors.

We were able to do tests on the current sensors with low currents from laboratory power source to prove that the sensors functioned as expected. However, current measurements with the BP were difficult since we needed to monitor the batteries to reliably observe and record the current flow.

Another hurdle we faced was the limited time for all the project activities. As a result some activities overlapped further reducing the time. As a thesis project, we were academically constrained to finish the project with a fixed time. Additionally, it was not a strict requirement from Infotiv to fully finish the project. The major requirement from Infotiv was for us to come up with an implementable design which we have done.

6

Battery Management System Scalability Analysis

During design of the system, we sought to fulfil the objectives of the project outlined in section 1.2. The first objective was intended to increase our knowledge about BMS in order to implement a SBMS. We have been able to fulfil this objective in chapter 2. Under that chapter, we explored the scalability consideration which outlined the requirements for a scalable system. These considerations have been applied during the design and subsequent implementation of the system to accomplish the second objective. This chapter analyses scalability of the proposed Scalable Battery Management System (SBMS) design in fulfilment of the third objective.

6.1 Design Layering Analysis

As noted earlier, the design of the BMS depends on the designer's set requirements. Scalability is a multifaceted concept that can be explored in various ways according to designer's objectives. This is why we chose the design layering strategy to explore scalability in different realms to allow the designer ability to easily service different objective basing on our design and implementation. In this analysis we seek to answer two key questions:

1. *Can the SBMS allow addition of resources to cater for increased workload?*
2. *Can the SBMS cater for increased workload without increasing resources?*

Workload in our case mainly refers to the number of cells to manage and the subsequent increase in voltage or current. The resources encompass the software and hardware.

6.1.1 Topological Design

With regards to Question 1, the topology of the SBMS allows increase in the number of modules in response to increased number of cells. Depending on the design, the number of cells managed by the module can also be increased. When compared to a centralised topology, a single controller can manage a limited number of cells [4].

6.1.2 Functional Design

With regards to question 1, the functional design of the SBMS puts emphasis on different functions within the BMS to handle higher number of cells.

Similar to the topological design analysis, the Cell Monitoring Unit (CMU) and Module Management Unit (MMU) functionality can also be scaled by increasing the number of modules. For example, the number of sensors to measure the cells is increased by increasing the number of modules. Since Pack Management Unit (PMU) carries out more complex computations and decision making, its scalability is mainly handled in software perspective (see sub-section 6.1.3).

6.1.3 Hardware

With regard to question 1, we seek to know if more hardware units can easily be added to the system in order to cater for increased number of cells. Breaking up the hardware into units increases both flexibility and re-usability by allowing a designer to select sufficient parts to meet set requirements of a given application.

With regard to question 2, it is also possible to increase the number of cells without increase in the number of hardware units. The SBMS can safely monitor up-to four cells in parallel if they are initially well balanced. In so doing the capacity of the battery can be increased up-to four times. The current design uses eight cells yet the battery monitor supports a maximum of twelve cells. This leaves room for increase of the voltage on a module as long as it remains below 60 V.

6.1.4 Software

With regards to question 1, layering the software allows us to maintain flexibility even with increasing workload. For example, if we required an upgrade to the state estimation methods, we would not require changing the entire system due to the separations of concerns in the BMS software. We make changes to the upper-layer but leave the low-layer intact.

With regards to question 2, we seek to know if the system can accommodate increased hardware components without requiring changes to the software. This has been partly achieved by writing the software in anticipation of increased peripherals, *i.e.* several runtime variables such as the battery monitor data structure are stored as arrays in anticipation of more than one battery monitor. A user can update the number of battery monitors available and the system will automatically manage them. With Micro-controller Units (MCUs), each module controller posses an address and communicate with the master on that address. Adding a module controller only requires updating the master with that module MCU's address.

6.1.5 Communication And Timing

We were not able to fully analyse effect of different configuration on system timing. However, due to the relatively low sampling frequency and low data and software complexity, the system timing may not be adversely affected by addition of more hardware. According to the datasheet of the components, the communication and information processing can be carried out within 100–200 ms intervals set in the system schedule (see sub-section 4.3.3). Additionally, the current design is implemented with the slower ATMega2560 MCUs (with a maximum clock frequency of 16 MHz) which can be replaced with the faster STM32F103C8 MCUs (with a maximum frequency of 72 MHz) that were earlier proposed. This enables the design accommodate increased processing needs while maintaining system timing constraints.

6.1.6 Electrical Isolation

Components used during design are targeted to meet automotive standards. According to the ISO 6469-3:2018 standard [42], class B application are those that support more than 60 V. In order to scale our system to a class B application, we ensure proper isolation coordination to provide both basic protection and fault protection according to the ISO 6469-3:2018 standard. Isolation is performed on both power and communication lines in the system.

Each module is a class A application *i.e.* has a maximum voltage below 60 V [42]. This inherently maintains proper isolation coordination. The designer only has to worry about isolating the overall Battery Pack (BP) voltage/current in the system rather than individual modules.

6.2 Use-case Analysis

Different number of Battery Modules (BMs) can be combined to increase voltage or capacity. During design, we targeted a design that would scale to at least 400 V and 100 A. In a centralised system, this would require a `134S32P` cell configuration. This causes a design challenge if all these cells have to be connected to a single controller. In the SBMS modular topology, this would require a `17S32P` BM configuration. The SBMS is not only applicable to BEVs but can also be applied to other electronic devices as well. Table 6.1 shows the common use cases and different configurations of the BMs required. The configuration are based on the minimum operating cell voltage and BP voltages and the minimum cell capacity as shown in table 4.1. As can be observed, the design can be scaled to achieve the target system of 400 V and 100 A.

Use Case	**Requirements**			**Configuration**	
	Voltage (V)	**Capacity (Ahr)**	**Maximum Current (A)**	**Cell**	**Module**
Target Design	400		100	134S32P	17S32P
Gen 1 Car Platform[a]	14.8	5.2	5	5S2P	1S2P
Gen 3 Car Platform[b]	48	48.75	100	16S16P	2S16P
Uninterrupted Power Supply (UPS)	12	7.2		8S3P	1S3P
Electronic Kick Bike	48		14	16S5P	2S5P
Electric Vehicle	400	250	800 (peak)	134S123P	34S123P

Table 6.1: Cell and Module Configurations For Different Use Cases

[a] This is the first generation prototype vehicle for IEP
[b] This is the third generation prototype vehicle for the IEP that carries one human passenger

6.3 Cost Analysis

In the cost estimation, we begin by analysing the cost distribution according to the layered design. Figures 6.1, 6.2 and 6.3 show percentage distribution of costs from the topology,

functional and hardware perspectives. It can be observed from all 3 charts that the bulk of the cost goes to the battery monitor which is found in the topology slave and functional CMU. Even with much more expensive controllers, the battery monitor may still remain more costly. Since the system manages small number of cells, *i.e.* 1–4 cells, an increase in the number of cells requires more battery monitors. However, a controller can manage up-to 16 battery monitors if desired.

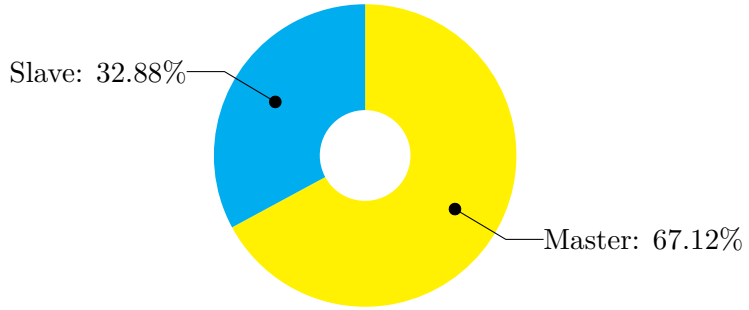


Figure 6.1: Topology Design Cost Distribution

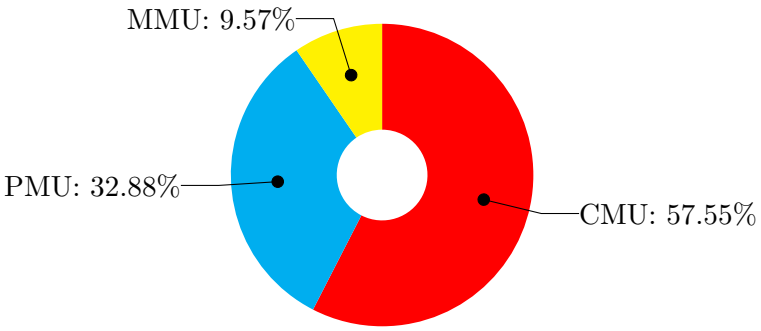


Figure 6.2: Functional Design Cost Distribution

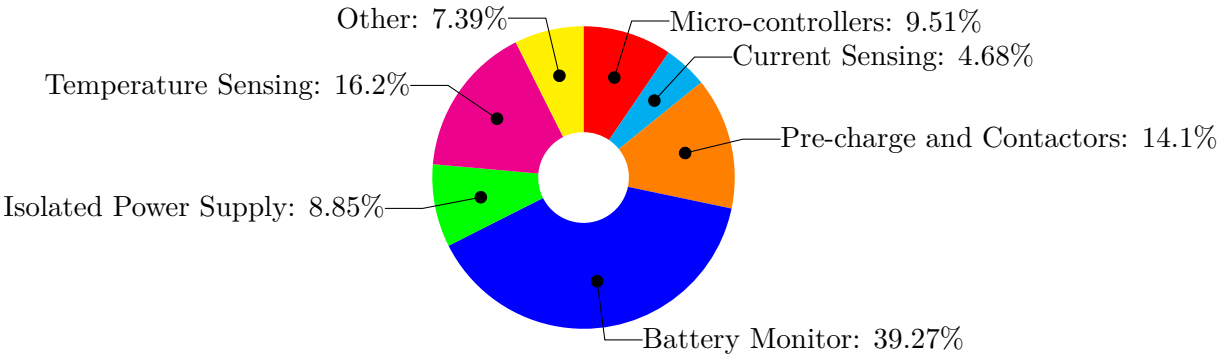


Figure 6.3: Hardware Design Cost Distribution

7

Conclusion and Future Work

In this report, we have demonstrated how a SBMS could be built. We have researched on the considerations required for scalability of a BMS, partly implemented a SBMS design, and then analysed the SBMS costs to show its viability. Since scalability is a multifaceted concept, design layering enables exploiting scalability opportunities of the design according to the four perspectives of topology, functional, hardware, and software. Additionally, the SBMS has been shown to not only exhibit scalability but also a high degree of reconfigurability and re-usability.

The topology perspective divides the design into a modular system with a master and several slaves. The functional perspective divides functionality into PMU, MMU and CMU. The hardware perspective groups the hardware components into units. The software perspective divides up the software into top, upper, middle and lower layers. Through a cost distribution analysis over the topological, functional, and hardware perspectives, we have shown that layers closer to the cells are more expensive that those further away.

There are several improvements that enhance the SBMS design that can be explored in the future. In order to improve communication reliability, CAN communication should replace I^2C protocol used for testing the design. Advanced algorithms such the improved model-based state estimation algorithms could replaces the low complexity functions applied in the design. The current system simply shuts-off current in case of a fault, however, it is desirable that a bypassing strategy be devised to eliminate only affected modules rather than the whole BP. Finally, an efficient cooling (Air or liquid) mechanism should be implemented to evacuate heat from the SBMS.

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A

Appendix

A.1 STMF103C8T6 Bluepill Schematic