

Balancing Asymmetrical Load Using a Static Var Compensator

Negative Sequence Assessments and Controller

Master of Science Thesis

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Department of Energy and Environment Division of Electric Power Engineering CHALMERS UNIVERSITY OF TECHNOLOGY Göteborg, Sweden 2014

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Abstract

In practical power systems, it is normally impossible to maintain perfect balance or symmetry in phase voltages and currents. The diversity of the load, such as single phase, arc furnaces and railway, enhances the amount of unbalance or negative sequence components. Alongside asymmetrical load, further increase in negative sequence components is introduced due to the network inherent asymmetry i.e. untransposed transmission. Thus, they are usually excessive and exceeds standards at weak nodes in the network. Utilities and customers have to comply certain code agreements to limit the degree of negative sequence components in the network. This is because that negative sequence components cause deterioration to the network equipments. For instance, higher loss, torque oscillation, speed reduction and excessive rotor heat are undesirable obstacles to rotating machines.

Asymmetrical load compensator can be based on passive elements, i.e. inductors and capacitors such as a Static Var Compensator (SVC), or a Voltage Source Converter (VSC) such as a Static Synchronous Compensator (STATCOM). The utilization of the negative sequence controller, an SVC or a STATCOM provides, gains a significant interest to most utilities around the globe. The compensators basically inject a different capacitive or inductive negative sequence current that has an opposite phase of the load negative sequence current. As a result, the network see symmetrical load and phase voltages and currents are balanced without exchanging active power between the network and the compensator.

The thesis investigates the benefits of the SVC negative sequence controller to a network with a detailed description about the SVC characteristics and control components. The thesis also presents unbalance assessment methods implemented in practical networks during the planning stage. Moreover, drawbacks of negative sequence components to network apparatus i.e. rotating machines and transmission lines are summarized. The analysis is carried out using PSCAD for a simple network representation and IEEE 14 bus system.

The result illustrates that the SVC allows utilities to balance asymmetrical loads to mitigate negative sequence components. The SVC response to balance asymmetrical load depends on load type, network strength and sources of unbalance. The SVC exhibits a very fast response to reduce the negative sequence components in extreme cases of unbalance such as asymmetrical short circuit. The SVC in general can mitigate negative sequence components caused by a sources connected in the same bus which means that the SVC provides local balancing only. Besides the negative sequence controller, the SVC enable a power factor correction by compensating for the reactive components of the load positive sequence current.

Index Terms: SVC, negative sequence components, voltage unbalance, imbalance, asymmetrical loads and unbalance assessments.

List of Abbreviation

Symbol	Description
PSCAD	Power System Computer Aided Design
FACTS	Flexible AC Transmission System
SVC	Static Var Compensator
STATCOM	Static Synchronous Compensator
TCR	Thyristor Controlled Reactor
TSC	Thyristor Switched Capacitor
PS	Positive sequence
NS	Negative sequence
ZS	Zero sequence
VUF	Voltage Unbalance Factor
IUF	Current Unbalance Factor

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Chapter 1

Introduction

First, the chapter gives a brief background of the thesis subject. The thesis aim and layout are discussed. The chapter ends with the main contribution of the thesis work

1.1 Background

Power electronic controllers are employed in the power systems in transmission and distribution levels. In transmission level applications, Flexible AC Transmission System (FACTS) controllers, consist of shunt and series static compensators, are applied for power flow control, stability enhancement, voltage regulation and power oscillation damping [27] [34]. In distribution level applications, custom power devices are used for voltage dip, interruption and flicker mitigations. They are normally installed close to sensitive industrial loads such as arc furnaces and paper mills.

In three phase power systems, the power quality issues of unbalanced voltages and currents, or normally called negative sequence (NS) components, are undesirable. They disturb the full utilization of the network equipments such as transmission lines and rotating machines. NS components convey useless energy and only contribute to the total loss in the system. They also impact the operation of synchronous and induction machines by causing higher heat, more loss, torque oscillation and speed reduction. These rotating machines are designed to withstand certain level of NS components without causing malfunctions. Utilities and customers have to comply certain code agreements to limit the degree of NS in the network. Suitable solutions are necessary if the NS components are excessive in the power system. A conventional way of reducing the NS components is to increase the strength of the power system by increasing the number of generation units and making the system more interconnected [26]. However, this approach is not economical and would cause other obstacles such as a high fault current which requires higher rating for protection equipments.

The concept of load compensation is based on reactive power management to reach the objectives of power factor correction, voltage regulation and load balancing (NS components mitigation) [26]. A load compensator may satisfy some or all the objectives depending on the compensator type and ability. A load compensator could be based on passive elements, inductors and capacitors, or a Voltage Source Converter (VSC). An example of a passive elements compensator is the Static Var Compensator (SVC) which is equivalent to a controllable shunt admittance. The SVC consist of Thyristor Controlled Reactor (TCR) and Thyristor Switched Capacitor (TSC). A Static Synchronous Compensator (STATCOM) is an example of VSC. Both compensators are suitable for balancing asymmetrical load.

1.2 Aim and Thesis Layout

The aim of the thesis work is to investigate the SVC capability and behaviour for asymmetrical load applications. The thesis also evaluates the impact of NS components to the network equipments. The thesis is divided into three chapters as the following:

Chapter 1. Introduction

In chapter 2, a comprehensive literature review about concepts related to unbalanced system are discussed. The chapter starts with sequence components which are used to represent unbalanced system. Several methods for defining and quantifying the degree of voltage and current unbalance are discussed. The chapter also summarizes the standards for voltage and current unbalance from a network and rotating machines perspectives. The main sources for NS components are also discussed. The fundamental concepts of unbalance assessment methods are provided. The chapter ends with a discussion about unbalance impact and conventional mitigation methods.

In chapter 3, load balancing compensators which are based on Steinmetz circuit are discussed. A method for calculating the compensator shunt susceptance for asymmetrical single phase load, three phase load and three phase load with transformer is provided. The concept of eliminating NS components using Steinmetz circuit is discussed. A comprehensive description is given about the SVC characteristics and controller components. The model of the positive sequence (PS) voltage regulator is discussed. Only a basic explanation about the NS voltage regulator is given due to the confidential information it contains to ABB. The chapter also explains the operating principles of the SVC. Harmonic generation from a single phase and three phase TCRs are discussed. Also, the switching strategies of a TSC are explained. The chapter ends with a basic comparison between the SVC and VSC in dynamic voltage regulation and load balancing applications.

In chapter 4, PSCAD simulation setup and analysis is presented. An SVC topology is built in PSCAD and tested first in an equivalent thevenin network with asymmetrical passive load. The same network is also used to study the SVC with the present of induction motor load. The response of the SVC to transient unbalance from asymmetrical short circuit is studied. Then, the voltage unbalance propagation between different voltage levels is investigated using 220 kV, 33 kV and 1 kV networks. Finally, the SVC is tested in the IEEE 14 bus test system. In each case, observations and justifications are given.

1.3 Main Contribution

The following list summarizes what, in the opinion of the author, are the main contributions presented in this thesis:

- A special attention is necessary when the degree of voltage and current unbalance, or NS component, exceed the limitation of the network code and equipment standards. NS components causes higher network loss and reduce the life time and efficiency of rotating machines.
- An SVC topology which consists of six-puls TCRs, six-puls TSCs and harmonic fixed capacitors shows a fair control of the PCC voltage unbalance. However, the six-puls TSCs are not utilized if the topology is implemented for NS voltage regulation only. This is because the TSCs cause high transient current and satisfying the free or minimum transient switching strategy is difficult when excessive variation of NS components exist. Therefore, only the TCRs and harmonic fixed capacitors control the PCC voltage unbalance by given individual controllable susceptance for each phase. The drawback of this topology, i.e. without the TSCs, is the inability of the SVC to control each phase individually if one of the TCRs in the delta connection hit zero susceptance which will cause the other TCRs to stay at constant susceptance.
- A conventional SVC, without NS voltage regulator i.e. no individual control of each phase susceptance, for PS voltage regulation implemented in a node where asymmetrical network and load exist causes worst unbalance or NS components to the network. This is because the SVC susceptance depends on the bus voltage and can not be controlled independent of the bus voltage. Therefore, the SVC injects different PS current for each phase to boost the voltage which will affect both the PS and NS components since they are decoupled by definition.
- In chapter 4 studies, the SVC, with both PS and NS sequence voltage regulators, shows a good dynamic PS voltage support and fair elimination of the NS components caused by asymmetrical load. However, a compromised solution between controlling both component is essential because they can not be controlled individually.

- The SVC response to mitigate NS components depends on the load type and network strength. Constant power loads cause the highest NS components because their impedance is varied with the input voltage to keep a fixed power. The weaker the network, the higher NS components and vice versa in stronger network. The SVC response to mitigate NS components is a trivial in strong network since both the SVC and the network "fight"each other for the NS component mitigation.
- The SVC, with a NS voltage regulator, implemented in industrial load bus, where high amount of NS components exist, stops the NS from propagating towards the industrial load motors. This will reduce the electrical torque oscillation, keep the speed constant where the mechanical and electrical torque are equal.
- In transient unbalance caused by asymmetrical short circuit, the SVC response to reduce the excessive NS components is fairly fast i.e. 0.5 to 2 cycles.
- The SVC shows only local balancing which means it can not balance asymmetrical load connected to a different bus even if it they are linked by a transmission line.

Chapter 1. Introduction

Chapter 2

Unbalanced System Background

This chapter provides a comprehensive literature review about unbalance system related concepts such as sequence components, standards and source of unbalance. Also, unbalance assessments basics during the planning stage are discussed. The chapter ends with a discussion about unbalance impact and conventional mitigation methods

2.1 Introduction

In three phase network, electrical quantities are analysed for one phase only assuming balanced system. However, this is invalid in practical analysis, where the three phase quantities are unbalanced, and sequence components representation is crucial. There are several methods that quantify the degree of voltage and current unbalance in the network. It is common to refer to voltage and current unbalance as NS components. Utilities and customers have to comply certain code agreements or standards to limit the degree of NS in the network. Unbalance assessment is usually carried out during the plaining stage to provides guidelines for system operators. High amount of NS components shows malfunction in rotating machines and higher loss in the network.

2.2 Sequence Components

In a perfect balanced system, electrical quantities i.e voltage and current on (a, b, c) phases are equal in magnitude and displaced by 120° phase shift.

ι

$$v_a(t) = \hat{V}\cos(\omega t) \tag{2.1a}$$

$$v_b(t) = \hat{V}\cos(\omega t - 120) \tag{2.1b}$$

$$v_c(t) = \hat{V}\cos(\omega t - 240) \tag{2.1c}$$

$$i_a(t) = \hat{I}\cos(\omega t - \phi) \tag{2.2a}$$

$$i_b(t) = \hat{I}\cos(\omega t - 120 - \phi) \tag{2.2b}$$

$$i_c(t) = \hat{I}\cos(\omega t - 240 - \phi)$$
 (2.2c)

Where (\hat{V}) and (\hat{I}) are the peek value of the voltage and current respectively. ($\omega = 2\pi 50$) and (ϕ) are the angular frequency and power factor angle respectively. Normally, electrical quantities in balanced system are analysed for one phase i.e. (a). However, such an approach is not valid in unbalanced condition and system analysis would be very complicated in the (abc) domain [20]. In real network, it is not possible to obtain full symmetry at all nodes for reasons which will be discussed in later sections of this chapter. Hence, the system is unbalanced where phase quantities have unequal magnitude and not displaced by 120° phase shift. Therefore, symmetrical components are essential to represent unbalanced electrical quantities

to balanced set of three variables named as *positive, negative and zero* components. An alternative way of writing 2.1 and 2.2 is in a phasor form as 2.3

$$V_a = V \qquad V_b = a^2 V \qquad V_c = a V \tag{2.3a}$$

$$I_a = I \qquad I_b = a^2 I \qquad I_c = aI \tag{2.3b}$$

where (a) and (a^2) are rotation operators and equal to ($1 < 120^{\circ}$) and ($1 < 240^{\circ}$) respectively. Thus, Fortescue transformation is expressed by 2.4 and 2.5

$$V_{abc} = \mathbf{T} V_{012} \tag{2.4a}$$

$$I_{abc} = \mathbf{T} I_{012} \tag{2.4b}$$

$$V_{012} = \mathbf{T}^{-1} V_{abc} \tag{2.5a}$$

$$I_{012} = \mathbf{T}^{-1} I_{abc} \tag{2.5b}$$

where \mathbf{T} and \mathbf{T}^{-1} are the transformation matrix and its inverse respectively which are expressed by 2.6 and 2.7

$$\mathbf{T} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}$$
(2.6)

$$\mathbf{T}^{-1} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1\\ 1 & a & a^2\\ 1 & a^2 & a \end{bmatrix}$$
(2.7)

We can notice that from 2.4 and 2.5 that any unbalanced quantities in the (abc) domain could be transformed to balanced one in (012) domain and vice versa. In addition, sequence impedance is very helpful which represents different components of the network. Therefore, 2.8 illustrates the relationship between current, voltage and impedance sequence components.

$$V_{012} = Z_{012}I_{012} \tag{2.8}$$

where

$$Z_{012} = \mathbf{T} Z_{abc} \mathbf{T}^{-1} \tag{2.9}$$

120

AV0BV0C

Moreover, fig. 2.1 shows the resolving phasor of unbalanced phase voltages into three set of balanced sequence voltages. The same procedure is also applied to phase currents.

V_{1A}

 $V_{0C} V_{0B} V_{1B} V_{1C} V_{0B} V_{1B} V_{2C}$ $V_{0C} V_{2B} V_{1B} V_{1C} V_{1B} V_{2C}$ $V_{0C} V_{2B} V_{1B} V_{2C}$ $V_{0C} V_{2B} V_{1B} V_{2C} V_{2C}$ $V_{0C} V_{2B} V_{1B} V_{2C} V_{2C}$

120

Fig. 2.1 Imbalance voltage with its symmetrical components

Theretofore, we define sequence components as follow:

- **Positive sequence components**: It consists of three phasors with equal magnitude and displaced by 120° from each other i.e. V_{1A} leads V_{1B} by 120° and V_{1B} leads V_{1C} by 120° in ABC rotation system. (phasors lags instead of leads in ACB rotation system).
- Negative sequence components: It consists of three phasors with equal magnitude and displaced by 120° from each other i.e. V_{2A} lags V_{2B} by 120° and V_{2B} lags V_{2C} by 120° in ABC rotation system. (phasors leads instead of lags in ACB rotation system).
- Zero sequence components: It consists of three phasors i.e. V_{0A} , V_{0B} and V_{0C} with equal magnitude and zero phase displacement.

2.3 Sequence Networks

The above mentioned concept bring us to the principle of sequence networks illustrated in fig. 2.2 for phase (a). They are constructed as viewed from the unbalanced point (X_1, X_2, X_0) . These unbalance points are due to short circuit, asymmetrical load and untransposed transmission lines. We notice that the positive sequence network is the only one with a voltage source which is equivalent to Thevenin network. The direction of the sequence current (I_1, I_2, I_0) are leaving the unbalanced points and the sequence voltage (V_1, V_2, V_0) are across the sequence impedance from the unbalanced point to the neutral bus (N_1, N_2, N_0) . Additionally, the value of the sequence impedance is different for each network components. For instance, rotating machines have unequal Z_1 and Z_2 while they are equal in overhead transmission lines and transformers. In three phase 3-wire power system, the zero sequence network is eliminated since I_0 flows only in the neutral wire. Hence, 2.10 illustrates the relationship between sequence voltage, current and impedance for three phase 3-wire system.

$$V_1 = V_a - I_1 Z_1 (2.10a)$$

$$V_2 = -I_2 Z_2 (2.10b)$$

From fig. 2.2, we conclude that any unbalanced segments in the network are composed into three balanced networks viewed from unbalanced point.



Fig. 2.2 Sequence components networks

2.4 Definitions and Quantifications

It is necessary to define and quantify the meaning of unbalance or asymmetry before proceeding into any unbalanced system analysis. There are several definitions and quantifications presented in literatures which depends on the application of unbalanced studies. From a network perspective, the IEEE defines and quantifies unbalance as the ratio of the maximum voltage deviation, from the average *phase* voltage, to the average *phase* voltage [2] [41] [9]. NEMA on the other hand use the *line* voltage instead of the *phase* voltage [41] [9]. Another definition from IEEE dictionary is "the difference between the highest and the lowest RMS voltage, referred to the average of the three voltages" [41]. More accurately, the IEC use symmetrical components in their definition as the ratio between NS components (V_2 , I_2) to the PS components (V_1 , I_1) [41] [9]. The definitions and quantifications for each organization is illustrates from 2.11 to 2.17 [41] [2] [9].

• **IEEE**₁: Phase Voltage Unbalance Rate (PVUR₁)

$$\% PVUR_1 = \frac{Max |V_{P_a} - V_{P_{avg}}|, |V_{P_b} - V_{P_{avg}}|, |V_{P_c} - V_{P_{avg}}|}{V_{P_{avg}}} * 100$$
(2.11)

where V_{P_a} , V_{P_b} , V_{P_c} are the phase voltages and $V_{P_{avg}}$ is the average phase voltage.

• IEEE₂: RMS Phase Voltage Unbalance Rate (PVUR₂)

$$\% PVUR_2 = \frac{Max |V_{P_{a_{RMS}}}, V_{P_{b_{RMS}}}, V_{P_{c_{RMS}}}| - Min |V_{P_{a_{RMS}}}, V_{P_{b_{RMS}}}, V_{P_{c_{RMS}}}|}{V_{P_{avg}}} * 100 \quad (2.12)$$

• NEMA: Line Voltage Unbalance Rate (LVUR)

$$\% LVUR_1 = \frac{Max |V_{L_a} - V_{L_{avg}}|, |V_{L_b} - V_{L_{avg}}|, |V_{L_c} - V_{L_{avg}}|}{V_{L_{avg}}} * 100$$
(2.13)

where V_{L_a} , V_{L_b} , V_{L_c} are the line voltages and $V_{L_{avg}}$ is the average line voltage.

• CIGRE: Unbalance Factor (UF)

$$\% UF = \sqrt{\frac{1 - \sqrt{3 - 6\beta}}{1 + \sqrt{3 - 6\beta}}}$$
(2.14)

$$\beta = \frac{|V_{ab}|^4 + |V_{bc}|^4 + |V_{ca}|^4}{[|V_{ab}|^2 + |V_{bc}|^2 + |V_{ca}|^2]^2}$$
(2.15)

where V_{ab} , V_{bc} , V_{ca} are the line voltages.

• IEC: Voltage and Current Unbalance Factors (VUF, IUF)

$$\% VUF = \frac{V_2}{V_1} * 100 \tag{2.16}$$

$$\% IUF = \frac{I_2}{I_1} * 100 \tag{2.17}$$

where V_1 , I_1 are the fundamental frequency PS voltage and current components and V_2 , I_2 are the fundamental frequency NS voltage and current components. It also common in practice and international standards to associate voltage unbalance with the NS components. In this thesis, IEC method is used to evaluates the degree of unbalance. Hence, "voltage unbalance", "current unbalance" or "NS components" refer to the absolute value of VUF and IUF in 2.16 and 2.17. It is common to call it as a "true value" in most literatures. However, voltage unbalance is also associated with the angle unbalance which is the angle difference between the fundamental frequency NS and PS components. Angle unbalance is very important to quantify specially in the present of power converters. Additionally, there is a correlation between VUF and IUF i.e voltage unbalance interacts with current unbalance.

It is obvious that all methods quantify unbalance based on voltage magnitude and neglect the phase angel except IEC, which is the most accurate one, since a change in phase angle will impact the sequence components rather than the magnitude of phase voltage. Let's evaluates the accuracy of these methods by examine three different cases i.e. under-voltage, over-voltage, clockwise phase shift and anticlockwise phase shift. Table 2.1 illustrates the result for each case.

V_a	V_b	V_c	$PVUR_1\%$	$PVUR_2\%$	LVUR%	UF%	VUF %
1 < 0	$1 < -120^{\circ}$	$1 < 120^{\circ}$	0	0	0	0	0
1 < 0	$1 < -120^{\circ}$	$0.95 < 120^{\circ}$	3.4	5.1	1.7	1.7	1.7
1 < 0	$1 < -120^\circ$	$1.05 < 120^\circ$	3.3	5	1.6	1.6	1.6
1 < 0	$1 < -120^\circ$	$1 < 115^{\circ}$	0	0	2.4	2.8	2.8
1 < 0	$1 < -120^\circ$	$1 < 125^{\circ}$	0	0	2.4	2.8	2.8

Table 2.1: Comparison result between the standards for three cases

Assume that we have a balanced base case where each phase voltage is equal to 1 pu with a 120° displacement. The result of this case is surly 0% voltage unbalance from all methods as illustrated in table 2.1. Now, two type of magnitude voltage unbalance, i.e. under-voltage and over-voltage, cases are introduced to phase (c). The result shows that both IEEE methods gives significant larger values than other methods. The result also shows that NEMA, CIGRE and IEC methods gives the exact same values. Furthermore, unbalance phase is also introduced to phase (c) i.e. clockwise and anticlockwise. The IEEE result 0% while the other shows some voltage unbalance. NEMA methods differ slightly from CIGRE and IEC. Under-voltage case shows a slightly higher voltage unbalance than over-voltage. There is no deviation in the result between clockwise and anticlockwise cases. However, phase unbalance causes higher values than magnitude unbalance. In [41] [9], a comprehensive evaluation of all methods is presented. It was found that for voltage unbalance below 5%, there is 0.8% deviation between NEMA and IEC [9].

2.5 Standards

Unbalance is usually evaluated based on a statistical concept called 95% percentile. It means that the allowed value should not be exceeded for 95% of an observation period i.e. 10 minutes aggregated values for one week in most standards. In reality, the allowed values are compared with measurement once. Another considerable issue is the background values which quantifies a certain natural unbalance in the network (0.5 - 1% depending on the network strength) [14]. Most standards and countries codes agree on (1 - 3%) of VUF which depends on the network characteristics, loads and voltage level. In Nordic region, the average measured VUF limit must be below 1% in Sweden and Denmark and 2% in 110kV Finish grid [6]. The planning level is estimated individually in each voltage level i.e. EHV, HV, MV, LV (see 2.7.2). From a current preservative i.e. IUF, voltage unbalance standards set the value of current unbalance which usually depends on the equipments. For instance, 10% VUF at the terminal of a rotating machine would causes around 100% IUF i.e (I_2) which is with (I_1) would heat the motors or the generator [11]. Table 2.2 illustrates the limitation values of VUF for several standards. (see 2.7.1 for compatibility level definition).

Table 2.2: VUF international standards values

Standards	VUF	Observation
ANSI	3%	planning level
ER P29	2%	planning level
IEC 61000-2-13	2-3%	compatibility level
Nordic	1%	compatibility level

Additionally, the IEEE and IEC standards classify the generator capability to handle unbalance into continuous unbalance (I_2) and short time unbalance (I_2^2t) i.e. faults or open conductor. It is required that NS current (I_2) , expressed in terms of per unit stator current and fault duration, are within the limit. Table 2.3 and 2.4 illustrate these standards for different generator types (Normally, synchronous machines standards are specified in terms of IUF since their terminal voltage is control to be balanced).

Type of generator	Permissible $(I_2\%)$
Salient pole	10
With connected amortisseur windings	10
With non-connected amortisseur windings	5
Cylindrical rotor	
Indirectly cooled	10
Directly cooled Up to 350 MVA	8
Directly cooled (351 to 1250) MVA	8
Directly cooled (1251 to 1600) MVA	5

Table 2.3: Continuous unbalance capability of generator [5]

Table 2.4: Short time unbalance capability of generator [5]

Type of generator	Permissible $(I_2^2 t)$	
Salient pole generator	40	
Synchronous condenser	30	
Cylindrical rotor generators		
Indirectly cooled	30	
Directly cooled (0 to 800) MVA	10	

2.6 Sources of Unbalance

In practical network, utilities struggle to maintain three phase balanced voltages and currents in all nodes. Generator terminal voltage, impedance of the transmission and distribution lines and loads are the main contributors of unbalance. Even though voltage and current unbalance interacts with each other, network apparatus i.e. rotating machines, transmission and distribution lines, and transformers mainly cause voltage unbalance while asymmetrical loads cause significant current unbalance. However, voltage unbalance responses to current unbalance in case of asymmetrical loads and perfectly balance supply. For instance, asymmetrical load draws unequal current from each phase which will cause different voltage drop in each phase of the supply system impedance. Hence, result both voltage and current unbalance. On the other hand, current unbalance response also to voltage unbalance when the load is perfectly balanced and the supply system is not. Therefore, there is a correlation between voltage and current unbalance and both have to be considered. The following text discuss the structural source of unbalance from a supply and a load perspectives. Further basic concept of transient unbalance is also discussed.

2.6.1 Unbalance supply

Large central generators do not usually contribute to voltage unbalance since their control system and strength helps to maintain balanced three phase voltages at their terminals i.e. PS voltage only. However, the current at their connection point with the transmission might consist of both PS and NS components due to the unbalance from the untransposed transmission. For economical reasons, transposition in not fully implemented in practical network. Thus, continuous voltage and current unbalance is caused by transmission lines and distribution feeders due to the unequal mutual and self capacitance and inductance. Numerous small distributed generators exist in some networks which usually are connected at the MV and LV level. For instance, small renewable sources i.e. solar cells and wind turbines introduce a significant voltage unbalance at their connection points. Most of MV and LV connection points have relatively high impedance, i.e. week network with low short circuit capacity, which enhance the degree of voltage unbalance (see 2.7.6) [4].

2.6.2 Unbalance loads

Normally, the root and the large portion of unbalance, mainly IUF, is caused by the operation of single phase, traction and arc furnaces loads. They permanently cause unbalance, because of the unequal phase current they draw, at their PCC, which propagates to other nodes in the network. Industrial load, mainly consist of numerous induction motors, is usually linked to the HV network. Induction motor loads tends to reduce the degree of the pre existing voltage unbalance at their PCC i.e. acting as a compensator (see 2.7.5). However, the attenuation to the voltage unbalance is very sensitive to the machine loading [22]. The connection of several LV loads i.e. single phase might not ensure balance distribution between the supply system phases. Even with equal single phase load distribution, most LV loads vary continuously with time which will cause unequal current drawn form the supply system. The following text discuss the characteristics of arc furnaces and traction loads.

Arc Furnaces load

The electric arc furnaces (EAF), used in steel industry, is highly non linear load which causes extreme unbalance, current harmonics, reactive power fluctuation. The phenomena of voltage fluctuation on the lighting i.e. flickers is caused by EAF due to the extreme current variation. EAF also impact the nearby rotating machines by causing a torque and power oscillation [42]. The operation of EAF uses electric power that transformed into a heat in the form of arcing between two electrodes. An example of EAF operation is the melting process of the scrap which form a liquid steel. The furnace is filled with the scrap and AC current is applied to form an arc that move up and down across the scrap. The process causes a variation in the arc length between the electrodes, which is proportional to the voltage and current, as the scrap melt. The arc is at highest length when the voltage is at maximum power. Beside the chemical energy, 70% of the EAF energy is electrical i.e. ranged between 700 KVA to 200 KVA per ton [3]. It is essential to model the EAF accurately when studying power quality phenomena. Normally, EAF are model as three phase variable resistance which varies with the arc length and radius. In [18], a suitable model, using differential equation and voltage-current characteristic, is presented for flicker, current harmonic, and reactive power variation studies.

Traction load

Locomotives are usually fed by railway feeders i.e. linked to the HV network through different transformer topologies (see 2.10). The (T) connection is a single phase transformer that is connected between two phases in the primary side. The other type is the (V) connection which consists of two single phase transformers i.e. fed by two phase voltage (ab and bc). This type of connection and other one such as (Scott, Le Blanc and Wye-Delta) lower the degree of unbalance. However, structural configuration can not reduce unbalance significantly because of the moving characteristic of the locomotives i.e. high speed, variable position which cause extreme power fluctuation. Nowadays, the power range of the traction load is very large i.e. 50-100 MW pet feeding transformer [19].

2.6.3 Transient unbalance

Unbalance from asymmetrical short circuit i.e. phase to ground, phase to phase and open conductor are classified as abnormal and disturbance condition. They usually occur in transmission system and last for very short time. They are cleared by system protection in 8-10 cycles. However, they cause the highest voltage and current unbalance. Beside the damage short circuit causes to the network equipments due to the large current, they also cause severe system instability issues. Fault type, impedance, location and point on wave inception impact the magnitude of fault current and transient NS components.

2.7 Unbalance Assessments Principles

The assessment of any unbalance system requires very sophisticated analysis due to the complex interaction between several source of unbalance in the network [23]. Most utilities around the globe comply certain guidelines to asses voltage and current unbalance in their system. Guidelines demonstrate the procedures

for setting the planning level of unbalance in the system to a certain degree. There are several methods in literatures that can be used in practical situations. One of the most comprehensive one is the IEC technical report (IEC/TR 61000-3-13) [7]. The report provides guidelines to system operators and owners to determine the requirements for the connection of three phase unbalanced installations. It also addresses the allocation of the system capacity to absorb NS unbalance type. However, the report ignores the assessment of single phase installations and ZS unbalance type since their impact is trivial and could be controlled through system configuration and maintenance [7]. Also, the guidelines are based on certain assumptions which would result no guarantee to obtain the optimum solution for all unbalance type in the network. They are based on the IEC guidelines and several other papers from the literatures which proposed further deep improvements to the it [7] [25] [24] [23] [29] [28] [31] [32] [30].

2.7.1 Compatibility level

An equipment or a system has a certain emission level, which is the maximum allowable of unbalance raised from that particular source. It also operates to a certain immunity level i.e. the maximum level of unbalance at which they still operate effectively. In other words, the IEC guidelines define the term, electromagnetic compatibility (EMC), as a satisfactory condition of an equipment or a system to operate as intended without producing electromagnetic disturbances to the surrounding environment. Therefore, the compatibility level is used as a reference value where a certain degree of balance is obtained between the immunity and the emission levels. Hence, customers must insure that the design of an equipment or the level of unbalance they deliver is up to the compatibility level while utilities have to limit the unbalance disturbance below the compatibility level. Normally, 2% VUF is suggested by the IEC guidelines as compatibility level for MV and LV networks. However, it might increase to 3% in certain cases where single phase loads are dominants. One of the drawback from the IEC guidelines is no specific values were given for HV and EHV networks.

2.7.2 Planning level

The planning level is defined as reference set of values to a particular load, equipments or network such as EHV, HV, MV and LV. It differ from case to case and specified locally by system operator or owners at particular voltage level. The IEC guidelines provide indicative values of the VUF for each voltage level as illustrated in table 2.5. Notice that the values are lower than the 2% compatibility level. This means that such indicative values allow the coordination of unbalanced installations between the voltage levels so the compatibility level is below or equal of 2% in the LV network. Thus, the planning level values are accommodated in the whole network. In [36], the result of a real cite measurements in LV, MV, HV and EHV unbalance level which meet the recommended indicative planning level.

Table 2.5: Indicative valu	es of VUF planning	level based on IE	EC/TR 61000-3-13 [7]

Voltage level	Planning level (VUF) %
EHV	0.8
HV	1.4
MV	1.8

2.7.3 Emission level

When an installation is connected to a network at a particular busbar i.e. point of evaluation (POE), it might either lead to an increase or decrease of VUF and IUF at that POE. Hence, IEC guidelines defined the term, emission level, as the magnitude of VUF and IUF, (see equations 2.16 and 2.17), which a certain installation arise at the POE. The POE could be any busbar in the network (Normally, it is the point of common coupling PCC). Fig 2.3 illustrates the impact of emission level to the post-connection VUF (actual) for an increasing and decreasing cases. The reduction in the net unbalance (post-connection) vector is caused by

the interaction between the system inherent asymmetry (i.e untransposed transmission) and impact of rotating machines at POE. It has been shown in [24] [23] that rotating machines and system inherent asymmetry interacts with the VUF of an installation and result a reduction in the net VUF at certain POE. However, IUF might be significant in such a case [7]. More analysis of load dependency and system inherited asymmetry will be discussed in further section (see 2.7.5)



Fig. 2.3 Comparison of emission vector before and after installation connection at POE [7] [24]

2.7.4 Global emission

The global emission level accounts for unbalance caused by all individual instillations and network inherent asymmetry of a system under assessment. The total system absorption capacity which is the allowed global emission of the system under assessment in fig. 2.4 is derived using 2.18.

$$V_{2,global} = {}^{\alpha}\sqrt{(L)^{\alpha} - (TL_{us})^{\alpha}}$$

$$(2.18)$$

where (α) is a summation low exponents that depends on (magnitude and phase variation degree of individual voltage unbalance, source of unbalance and other probability values). The IEC guidelines suggest a value of ($\alpha = 1.4$) for most source of unbalance. (L) and (L_{us}) are the planning level from table 2.5 of the system under assessments and upstream systems (US) respectively. (T) is the transfer coefficient between the US and DS systems (see 2.7.5). The resultant emission level, which is estimated after each individual instillation is connected at a particular busbar (x), must be below the planning level. In other words, the resultant emission level should show a satisfactory compatibility level. Hence, global emission for each busbar (x) of the system under assessment is expressed by 2.19

$$V_{2,global}^{x} = V_{2,global} \,^{\alpha} \sqrt{\frac{S^{x}}{S_{total}^{x}}} \tag{2.19}$$

Where (S^x) and (S^x_{total}) are the total (MVA) to be supplied by the busbar and the total available (MVA) of the whole system seen at the busar respectively. The value of (S^x_{total}) is calculated taking into account the voltage unbalance caused by other nearby busbar, which is quantified in terms of influence factor (see 2.7.5). Normally, the global unbalance emission in a particular busbar (x) accounts for the instillations and lines emission as shown in 2.20. (Note: $V_{2,global}$, $V_{2,line}$ and $V_{2,load}$ are in terms of VUF).

$$\{V_{2,global}^x\}^{\alpha} = \{V_{2,load}^x\}^{\alpha} + \{V_{2,line}^x\}^{\alpha}$$
(2.20)



Fig. 2.4 global emission voltage unbalance coordination

2.7.5 Assessments factors

It was shown that the global emission allocation requires the estimation of individuals unbalance at any POE in the network i.e. how much of unbalance is due to a network inherent asymmetry and how much is due to loads. It also requires the knowledge of how unbalance or NS components propagates from different voltage level in terms of transfer coefficient. Moreover, the coordination of unbalance between different buses in the network within a specific voltage level is essential to identify. To study theses issues, consider the simple radial power system in fig. 2.5 [24] [23].



Fig. 2.5 A simple radial Network

The source, line and the load contribute to the net VUF at the POE as expressed by 2.21

$$VUF_{POE} = VUF_{source} + VUF_{line} + VUF_{load}$$
(2.21)

The contribution of the load (VUF_{load}) depends on the load type. For passive loads, it is described by 2.22a in terms of sequence impedance and the voltage regulation of the line $(V_{reg-line})$. In case of unknown sequence impedance i.e. constant power and constant current loads, 2.22a can written in terms of IUF and $(V_{reg-line})$ as shown in 2.22b [24] [23].

$$VUF_{load} = \frac{Z_{21,rec}}{Z_{11,rec}} \frac{V_{reg-line}}{1 + V_{reg-line}}$$
(2.22a)

$$VUF_{load} = (VUF_{POE} - IUF) \frac{V_{reg-line}}{1 + V_{reg-line}}$$
(2.22b)

Where $(Z_{21,rec})$ and $(Z_{11,rec})$ are the NS-PS coupling impedance and PS self impedance seen at the POE respectively. They are usually equal to the load sequence impedance. $(V_{reg-line})$ is the ratio between the PS voltage drop in the line and the PS voltage at the receiving end (IUF is defined by 2.17). The line contribution (VUF_{line}) is expressed by 2.23

$$VUF_{line} = -\frac{Z_{21,line}}{Z_{11,line}} \frac{V_{reg-line}}{1 + V_{reg-line}}$$
(2.23)

Where $(Z_{21,line})$ and $(Z_{11,line})$ are the NS-PS coupling impedance and PS self impedance of the transmission line respectively. When a three phase induction motor is recognized as a load instead of passive one, it does not exhibit any voltage unbalance to the net VUF. Only, their operation is negatively influenced by the voltage unbalance at their terminal [24] [23]. In fact, induction motors introduce a reduction in the net VUF at the POE as expressed by 2.24

$$VUF_{POE} = A * VUF_{source} - \frac{Z_{2,im}}{Z_{1,im}} \frac{Z_{21,line}}{Z_{2,im} + Z_{22,line}}$$
(2.24a)

$$A = \frac{Z_{2,im}}{Z_{1,im}} \frac{Z_{1,im} + Z_{11,line}}{Z_{2,IM} + Z_{22,line}}$$
(2.24b)

Where $(Z_{1,im})$ and $(Z_{2,im})$ are the PS and NS impedance of the induction machine equivalent sequence network respectively. Notice the reduction in the net VUF by the factor (A) which usually has a magnitude that is less than unity [24] [23]. The second term in 2.24a is the contribution of the line asymmetry. Additionally, radial power system are usually feeding mix of passive and induction motor loads. Hence, the net VUF at the POE is expressed by 2.25

$$VUF_{POE} = A * VUF_{source} + B + C$$
(2.25a)

$$A = \{1 + \frac{Z_{11,line}}{Z_{11,rec}}\} * N$$
(2.25b)

$$B = \{\frac{Z_{21,pl}}{Z_{22,pl}} \frac{Z_{22,line}}{Z_{11,pl}}\} * N$$
(2.25c)

$$C = -\{\frac{Z_{21,line}}{Z_{11,rec}}\} * N$$
(2.25d)

$$N = \left\{ \frac{1}{1 + \frac{Z_{22,line}}{Z_{2,im}} + \frac{Z_{22,line}}{Z_{22,pl}}} \right\}$$
(2.25e)

Where $(Z_{11,pl})$ and $(Z_{22,pl})$ are the PS and NS self impedance of the passive load respectively. If the transmission lines are symmetric i.e fully transposed, (C) is equal to zero because $(Z_{21,line} = 0)$. Thus, (C) represents the contribution of the transmission line. The factor (B) represents the contribution of passive load while (A) for the induction motor load. Again, factor (A) is also less than unity which will result a reduction of the net VUF at the POE when (C=B=0). In [24] [23], the detailed derivation of 2.22 to 2.25 plus representing factors (A, B, and C) in terms of $(V_{reg-line})$ and IUF.

Furthermore, several important factors (or coefficients) are discussed as follow:

1. K_{UE} factor:

It is defined as the fraction of the total emission allocation that can be allocated to unbalanced load. In other words, it is a set of indicative range of values assigned to the network depending on its characteristics. The K_{UE} can be expressed by 2.26

$$K_{UE^{x}} = \{\frac{V_{2,load}^{x}}{V_{2,global}^{x}}\}^{\alpha}$$
(2.26a)

$$K_{UE} = \left\{ \frac{VUF_{load}}{VUF_{POE}} \right\}$$
(2.26b)

The (K_{UE}) is also used to estimate the emission limit to a single installation (i) at busbar (x) as expressed by 2.27.

$$E_i^x = {}^\alpha \sqrt{K_{UE^x}} V_{2,global}^x {}^\alpha \sqrt{\frac{S_i^x}{S_{total}^x}}$$
(2.27)

Where (E_i^x) and (S_i^x) are the emission limit and agreed MVA to an installation (i).

2. K'_{UE} factor:

It is the total emission allocation that account for system inherent asymmetry $(1 - K_{UE})$ and expressed by 2.28. The values of the (K_{UE}) and (K'_{UE}) factors vary between the range of (0.8-0.9)(0.1-0.2) for highly meshed network with fully transposed lines feeding high density load areas, (0.6-0.8)(0.2-0.4) for mix of meshed and radial network and (0.5-0.6) (0.4-0.5) for radial network with long transmission lines and low density load respectively.

$$K_{UE^{x}}^{'} = \{\frac{V_{2,line}^{x}}{V_{2,global}^{x}}\}^{\alpha}$$
(2.28a)

$$K_{UE}^{'} = \left\{\frac{VUF_{line}}{VUF_{POE}}\right\}$$
(2.28b)

3. K_{x-y} factor:

It is the influence factor which accounts for the voltage unbalance that propagates from one busbar (x) to another nearby busbar (y). It is defined as the voltage unbalance that arise at busbar (y) when (1pu) voltage unbalance is applied at busbar (x). The influence factor is expressed by 2.29

$$K_{x-y} = \left\{ \frac{V_{2,y(V_{2x})}}{V_{2,x}} \right\}$$
(2.29)

Where $(V_{2,y(V_x)})$ is the NS voltage vector at busbar (y) that propagated from busbar (x) as a result of NS voltage vector $(V_{2,x})$. From fig. 2.5, the propagated NS voltage vector unbalance at the receiving end from the sending is given by 2.30.

$$V_{2,rec(V_{2,send})} = V_{2,send} - Z_{22,line} I_{2,line(V_{2,send})}$$
(2.30)

Where $(I_{2,line}(V_{2,send}))$ is the NS current vector in the line which result from the unbalance at the sending end. The NS and PS self impedance of the line are equal $(Z_{22,line} = Z_{11_line})$. Furthermore, the influence factor depends on the load i.e. equal to unity in case of passive load and smaller than unity in case of induction motor load. 2.31 estimates the value of the influence factor for passive, induction motor and mix loads located in POE of fig. 2.3 respectively.

$$K_{send-rec}^{pl} \approx \{ \frac{1}{1 + \frac{Z_{11,line}}{Z_{11,rec}}} \}^{\gamma} \approx \{ 1 - V_{reg-line} \}^{\gamma}$$
 (2.31a)

$$K_{send-rec}^{im} \approx \frac{1}{1 + \frac{V_{reg-line}}{1 - V_{reg-line}} \frac{1}{\frac{1}{k_s} + \frac{1}{k_{sg}} \frac{1}{l_s(c,g)}}}$$
(2.31b)

$$K_{send-rec}^{mix} \approx \frac{1}{1 + \frac{V_{reg-line}}{1 - V_{reg-line}} \frac{k_{lv}}{\frac{1}{K_m k_s} + \frac{1}{k_{sc,lv(agg)}}}}$$
 (2.31c)

Where

- (γ) is equal to (1) for constant impedance load, (0) for constant current load and (-1 or -2) for constant power load with high or low power factor respectively.
- (k_s) is the ratio between the PS impedance and the NS impedance of the aggregated motor load supplied at the LV network $(5 < k_s > 7)$.

- $(k_{sc-lv(agg)})$ is the ratio between the short circuit capacity (MVA) and the total load in (MVA) at the aggregated LV busbar.
- (k_{lv}) is the fraction of LV load supplied by MV network.
- (*k_m*) is the ratio between the rated induction motor (MVA) and the total load in (MVA) at the LV network.

The result from the study in [31] illustrates that the influence factor depends highly on load type and the proportion of induction motor at the POE. With the most practical value of $(V_{reg-line} = 10\%, k_{sc-lv(agg)} = 20, k_s = 6.7)$, the influence factor $(K_{send-rec} = 1 \text{ and } 0.6)$ for passive and induction motor loads respectively. Alternatively, no negative sequence current $(I_{2,line(V_{2,send})})$ propagates from the sending to the receiving end when the load is passive.

4. T_{US-DS} transfer coefficient:

It quantifies the propagation of voltage unbalance between the upstream to the downstream networks which is defined by 2.32

$$T_{UD-DS} = \frac{V_{2,DS(V_{2,US})}}{V_{2,US}}$$
(2.32)

Where $V_{2,DS(V_{2,US})}$ is the voltage unbalance, in terms of VUF, at the downstream network which results from the voltage unbalance at the upstream network ($V_{2,US}$). The transfer coefficient is also load type dependent. 2.33 and 2.34 estimates the transfer coefficients of the (HV-MV) and (MV-LV) for passive, induction motor and mix loads respectively.

$$T^{pl}_{hv-mv} \approx \{1 + j \frac{1}{k_{sc,mv}} < \theta_{pf,mv}\}^{\lambda}$$
(2.33a)

$$T_{hv-mv}^{im} \approx \frac{\{1+j\frac{1}{k_{sc,mv}} < \theta_{pf,mv}\}}{\{1+\frac{1}{k_{sc,mv}}\frac{k_s}{1+\frac{k_s}{K_{sc,lv(agg)}}}\}}$$
(2.33b)

$$T_{hv-mv}^{mix} \approx \frac{\{1+j\frac{1}{k_{sc,mv}} < \theta_{pf,mv}\}}{\{1+j\frac{k_{z,mv}}{k_{sc,mv}} < \theta_{pf,(z,mv)}\} + \{1+j\frac{k_{qp,mv}}{k_{sc,mv}} < \theta_{pf,(pq,mv)}\}^{\beta} + T}$$
(2.33c)

$$T \approx \{1 + \frac{k_{lv} k_m}{k_{sc,mv}} \frac{k_s}{1 + \frac{k_m k_s}{k_{sc,lv(agg)}}}\}$$
(2.33d)

$$T^{pl}_{mv-lv} \approx \{1 + j \frac{1}{k_{sc,mv}} < \theta_{pf,lv}\}^{1-\beta}$$
(2.34a)

$$T_{mv-lv}^{im} \approx \frac{\{1 + j\frac{1}{k_{sc,lv}} < \theta_{pf,lv}\}}{\{1 + \frac{ks}{k_{sc,lv}}\}}$$
(2.34b)

$$T_{mv-lv}^{mix} \approx \frac{\{1+j\frac{1}{k_{sc,lv}} < \theta_{pf,lv}\}}{\{1+j\frac{k_{z,lv}}{k_{sc,lv}} < \theta_{pf,(z,lv)}\} + \{1+j\frac{k_{qp,lv}}{k_{sc,lv}} < \theta_{pf,(pq,lv)}\}^{\beta} + \{1+\frac{k_mk_s}{K_{sc,lv}}\}}$$
(2.34c)

Where

- (λ) is equal to (0) for constant impedance load, (1) for constant current load and between (2-3) for constant power loads respectively.
- (β) is equal to (-1 or -2) for low or high lagging power factor respectively. Also, (β) equal to (1) for constant impedance load (i.e $T_{mv-lv}^{pl_z}=1$) in 2.34 and equal to (0) for constant current load.
- $(\theta_{pf,mv} \text{ and } \theta_{pf,lv})$ are the power factor angles at the MV and LV busbar respectively (- and + for lagging and leading respectively).
- $(\theta_{pf,(pq,mv)}, \theta_{pf,(z,mv)})$ and $\theta_{pf,(pq,lv)}, \theta_{z,(pq,lv)})$ are the power factor angles for constant power and constant impedance loads supplied by the MV and LV respectively.
- $(k_{sc,mv} \text{ and } k_{sc,lv})$ are the ratio between the short circuit capacity (MVA) at the LV and MV busbars and the total load in (MVA) supplied by the MV and LV busbars respectively. In another words, they are equal to $(k_{sc,mv} = \frac{S_{sc,mv}}{S_{mv}})$ and $k_{sc,lv} = \frac{S_{sc,lv}}{S_{lv}})$

2.7.6 Power components

An alternative method for NS assessment that identify the source of unbalance is based on the flow of active (P) and reactive (Q) power [8] [39]. Tracing the sequence power components i.e. positive (P_1, Q_1) , negative (P_2, Q_2) and zero (P_0, Q_0) active and reactive enables us to identify the source of unbalance. The total active and reactive power in three phase system is expressed in terms of sequence components as 2.35

$$P_{total} = \sum_{i=a,b,c} = P_i = P_1 + P_2 + P_0$$
(2.35a)

$$Q_{total} = \sum_{i=a,b,c} = Q_i = Q_1 + Q_2 + Q_0$$
(2.35b)

$$P_{012} = 3 V_{012} I_{012} \cos \theta_{012} \tag{2.35c}$$

$$Q_{012} = 3 V_{012} I_{012} \sin \theta_{012} \tag{2.35d}$$

Where (V_{012}) and (I_{012}) are the sequence components voltage and current at the fundamental frequency respectively. (θ_{012}) is the angle difference between the sequence voltage and current components. The three phase effective apparent power, useful power a load consume, is defined by the IEEE 1459 Std as in 2.36 [8].

$$S_e = 3 V_e I_e \tag{2.36a}$$

$$V_e = \sqrt{(V_1)^2 + (V_2)^2 + (\frac{V_0}{\sqrt{2}})^2}$$
(2.36b)

$$I_e = \sqrt{(I_1)^2 + (I_2)^2 + (\frac{I_0}{\sqrt{2}})^2}$$
(2.36c)

Where (V_e) and (I_e) are the effective voltage and current respectively. The ZS components (V_0, I_0) are ignored if an assumption of three wire system. Thus, the unbalance apparent power is expressed by 2.37 which enable us to identify the unbalance factor, from the MVA values only, caused by the load at the PCC using 2.38

$$S_{unbalance} = \sqrt{(S_e)^2 - \{(P_1)^2 + (Q_1)^2\}}$$
(2.37)

$$\% SUF = \frac{S_{imbalnce}}{S_e} \tag{2.38}$$

There is a correlation between the direction of the NS active power (P_2) and the source of unbalance. When VUF exist at the PCC due to the asymmetrical load, assume a perfectly balance network i.e. equal impedance and voltage of each phase, (P_2) will propagate toward the network from the asymmetrical load $(P_2 = -)$ [39] [38]. On the other hand, $(P_2 = +)$ and propagates toward the load when network is the source of unbalance and the load is perfectly symmetrical. Hence, the NS power flow (P_2) is illustrated in fig. 2.6 where (S) is the measured apparent power at the PCC and (S_n) is the reference value when both loads and networks are perfectly symmetrical i.e (VUF, IUF) are equal to zero. The above mentioned assessment methods does not provide an accurate result compared to the method discussed previously [38]. The method also could not quantify individual unbalance when multiple source of unbalance exist.



Fig. 2.6 Negative sequence active power flow vs unbalance loading [39]

2.8 Impact of Unbalance

2.8.1 Rotating machines

Normally, the impact of unbalance to synchronous generator is analysed using sequence current components while voltage components are used in induction machines. Generators i.e. three phase synchronous machines are design to withstand a certain amount of IUF (see 2.5). However, a significant amount of NS causes both mechanical and electrical stress on the machine. It impact the operation of the machine by causing a large heat and power loss which will reduce its efficiency and life time. The ZS component on the other hand could be eliminated by choosing the configuration of the three phase machine such as delta and isolated ground connection. To understand the impact of NS components, it is essential to review the concept of current and magmatic flux. The relationship between the induced magnetic flux density (\vec{B}) , created by a current flow in a conductor, and the current at a distance (r) from the conductor is expressed by 2.39.

$$B = \frac{\mu}{2\pi r} I \tag{2.39}$$

where (μ) is the permeability of the material and (r) is the stator radius in case of rotating machines. The PS and NS currents in the stator induce flux density vectors, at the central point of the rotor, and expressed for each phase windings i.e. $(a\dot{a})$, $(b\dot{b})$ and $(c\dot{c})$ in terms of PS and NS components in 2.40 and 2.42 respectively [43].

$$\vec{B}_{1,a\dot{a}} = B_1 \sin(wt) \tag{2.40a}$$

$$\vec{B}_{1\ b\dot{b}} = B_1 \sin(wt - 120^\circ) e^{j120^\circ} \tag{2.40b}$$

$$\vec{B}_{1,zcc} = B_1 \sin(wt + 120^\circ) e^{-j120^\circ}$$
(2.40c)

$$\vec{B}_{2,a\dot{a}} = B_2 \sin(wt) \tag{2.41a}$$

$$\vec{B}_{2,bb} = B_2 \sin(wt + 120^\circ) e^{j120^\circ}$$
(2.41b)

$$\vec{B}_{2,c\dot{c}} = B_2 \sin(wt - 120^\circ) e^{-j120^\circ}$$
(2.41c)

Where $(B_1 = \frac{\mu}{2\pi r}I_1)$ and $(B_2 = \frac{\mu}{2\pi r}I_2)$. The sum of the three magnetic flux vectors for each components is then expressed as

$$\overrightarrow{B}_{1} = \overrightarrow{B}_{1,a\dot{a}} + \overrightarrow{B}_{1,b\dot{b}} + \overrightarrow{B}_{1,c\dot{c}} = -j\frac{3}{2}B_{1}e^{jw}$$
(2.42a)

$$\overrightarrow{B}_{2} = \overrightarrow{B}_{2,a\dot{a}} + \overrightarrow{B}_{2,b\dot{b}} + \overrightarrow{B}_{2,c\dot{c}} = -j\frac{3}{2}B_{1}e^{-jw}$$
(2.42b)

Chapter 2. Unbalanced System Background

Hence, we see from 2.42a that the PS current in the stator induced a flux density vector which rotates with the direction of the rotor i.e counter-clockwise at angular velocity of (w). On the other hand, NS current in the stator induce a flux density vector which rotates in the opposite direction of the rotor i.e clockwise as shown in 2.42b. Thus, the current and the flux density induced in the rotor are double frequency (2w) relative to the rotor [43]. In other words, a flux is induced at twice the rotational velocity which includes double frequency currents in the field system and the rotor body. Such an issue cause additional hysteresis loss and eddy current loss as expressed by 2.43 [15].

$$P_{loss,eddy} = K_e f^2 B_{max}^2 \tau^2 \tag{2.43a}$$

$$P_{loss,eddy} = K_e f B^n_{max} \tag{2.43b}$$

Where (τ) and (n) are the thickness of the core and an exponents constant respectively. (K_e) and (K_h) are coefficients that depend on the material. Hence, the core loss i.e. eddy current, which is proportional to (f^2) , and hysteresis are significant from the double frequency NS current.

The mechanical stress mostly causes torque pulsation and vibrations issues. In some cases, the retaining ring, slow wedge and filed winding fail to operates which will cause further rotor instabilities. The most affected parts by NS current are the retaining rings and wedges. The function of the retaining ring is to hold the winding at each end of the rotor and support them against forces. Usually, they are subjected to a high stress and shrunk into the rotor body. Thus, locking the retaining ring to the rotor body is essential to ensure no mechanical stress. However, the heat from the NS current might cause a loose retaining ring which causes a significant vibration and arcing at the shrink fits [33]. In a cylindrical generator rotor, the wedges are used to hold the copper winding into the slots. Also, the overheat from NS current in the wedges reported to cause a shear failure [33]. Additionally, [33] presents the result from an experiment which study the impact of NS current to turbine generator rotors. The result shows that the rotor damage, in small generator (15-20) MW, occur due to the retaining ring overheat which happens at lower value of $(I_2^2 t)$ than the failure of aluminium wedges (I_2 is the per unit NS current and t is time in second). For larger generator i.e. 30 MW and above, the machine fails due to the rupture of the wedges (occur before the retaining ring arc is developed). The result estimated ($I_2^2 t$) to be 30 and 60 as a maximum save and failure values respectively.

Beside the unbalance improvement that induction motors provide to the pre existing VUF at the PCC, their operation is negatively affected in the same way as synchronous machine when supplied by unbalanced voltage. Additionally, NS current produced a reversing torque to the PS one due to the air gap NS flux that rotate against the PS flux. Thus, the motor will not be able to produce its full torque i.e. a lower net and peak torque of the machine. In other words, it behaves like a superposition of two separate motors running with two different slips for PS and NS voltage expressed by 2.44 [10].

$$s_1 = \frac{N_s - N_r}{N_s} \tag{2.44a}$$

$$s_2 = \frac{-N_s - N_r}{-N_s} = 2 - s_1 \tag{2.44b}$$

Where N_s and N_r are the synchronous and rotor speeds respectively. This would cause a speed reduction and high slip operation of the motor which will increase the rotor loss and heat dissipation. Moreover, the efficiency an life time of the motor is reduced.

2.8.2 Lines and transformers

The NS current in transmission and distribution lines do not convey a useful energy. Therefore, it contributes to the total loss in the network and increase the conductor temperature. Unlike ZS components, transferors behaves to NS components in a similar way as PS components. Different configuration, such as delta connection, enable the ZS to circulate in the delta winding which might cause a temperature increase.

2.9 Negative Sequence Relays

Negative sequence relay (NSR), digital or electromechanical, is used in the power system for several applications. Frequently, NSR protects generator and motors from unbalanced condition which causes the undesirable impacts discussed in (2.8). NSR insures that the NS current which enter the generator or the motor is within the designed limitations in case of continuous and abnormal NS current. A proper coordination is essential between NSR and other protection devices such as over current relay (OCR) and short circuit breaker. Normally, abnormal conditions such as phase to phase fault which causes the highest NS current is cleared by the short circuit protection breaker within a shorter time than the NSR [12]. The inverse time characteristic of the NSR is expressed by 2.45

$$K = (\frac{I_2}{I_1})^2 t (2.45)$$

Where (I_1) is the PS rated current of the generator or motor, (t) is the relay tripping time in second and (K) is the generator or motor characteristic constant in second. The constant (K) estimates the generator or motor time capability to permit NS current and varies between 5-40. Digital NSR consist of negative sequence element (NSE) and over current element (OCE) [12]. The function of the NSE is to compute the value of $(\frac{I_2}{I_1})$ from the phase currents measurements. The OCE uses the NSE inputs to assign the output single based on the inverse time characteristic in 2.45. A detailed modelling of a digital NSR is analysed in [12].

2.10 Unbalance Conventional Mitigation Methods

Conventional mitigation techniques, such as structural modification and standards adoption, are normally implemented in the planning stage. The adoption of standards requires customers to maintain the emission level allocation specified by the system operator. On the other hand, system operator and owners must insure the control of disturbance and the limitation of network inherent asymmetry. The advantages of standards modification is the significant unbalance reduction from a systematic perspective which would show great result in all nodes. However, standards adoption is a sophisticated task and require participation from all users. Utilities usually plan the unbalance to a certain degree for specified number of years and hoping for that to be maintained.

Structural modification, for the single phase LV loads, is implemented by distributing them equally between the phases in the MV supply. However, such an approach will not guarantee the mitigation for long time since more single phase may exist in the future plus their power fluctuation. Additionally, unbalance from traction feeders could be mitigated using one of the following transformer connection topology in fig 2.7. The connection selection depends on several factors such as cost of operation and maintenance.

- **Single phase:** It is a normal transformer that is connected between two phases on the primary side. This type of connection causes the worst unbalance since one of the supply phases is not connected.
- V-V: Two single phase transformers fed by two phase i.e. AB and CB on the primary side. This type of connection reduce the unbalance on the supply system by approximetly half compare with single phase transform.
- Scott: It is one of the common topology used in traction loads which transform three phase supply system to two phase. If equal loading is reached between the two transformer, the unbalance might reduce significantly i.e. within the standards. The maximum voltage unbalance with such a connection is approximately 10.24% [1].
- Le Blanc: It is similar to scott transformer topology but with delta configuration on the primary and two winding on the secondary. The maximum voltage unbalance with such a connection is approximately 6.69% [1].



Fig. 2.7 Traction load transformer connections

2.11 Conclusion

It is impractical to maintain perfect balanced voltages and currents in three phase system. Hence, the representation of the network as a sequence components i.e. PS, NS and ZS is essential in the analysis. When defining and quantifying the degree of unbalance or NS, the IEC method is the most accurate one because it depends on sequence components rather than phase and line quantities which are not influenced by an angle variation while the former varies with the phase angle. In most standards, 1-3% VUF is consider as an acceptable limit in the network but varies between the voltage levels. The supply system contribution to voltage and current unbalance is much less than the load contribution. During the planning stage, unbalance assessment methods are essential to avoid extreme NS components in the network. However, they require very sophisticated analysis due to the complex interaction between several source of unbalance in the network. Unbalance voltage and current impact the operation of rotating machines and reduce their efficiency and life time. Hence, they should be protected against excessive NS components from the network or the load.

Chapter 3

Asymmetrical Load Compensator Principles

This chapter provides the basics of load balancing compensator which is based on Steinmetz circuit. A comprehensive discussion is given about the SVC characteristics and control components. The chapter ends with a basic comparison between the SVC and VSC.

3.1 Introduction

Overall, single phase and three phase loads fluctuate with time and causes excessive NS components in the network. A conventional method to lower the NS components is to increase the fault level at the PCC or by other means connecting the load to a stronger nodes in the network. However, that is usually not a cost effective and impossible in some situations where new loads are installed frequently. In nodes where highly asymmetrical load exists, it is essential to install load balancing compensator to keep the NS components in the network within the limitations. Load balancing compensator can be based on passive elements such as capacitors and inductors, i.e.Steinmetz circuit, or voltage source converters. Steinmetz circuit usually consists of fixed shunt susceptance connected to a asymmetrical load. However, a variable susceptance can be achived using bidirectional thyristor valves i.e. and SVC.

3.2 Load Balancing Principles

3.2.1 Steinmetz circuit for single phase Load

A circuit proposed by Charles Proteus Steinmetz illustrates that asymmetrical load, in three phase network, can be seen as symmetrical by using shunt connected passive elements i.e. inductor and capacitor. Hence, eliminating the NS components, without the need of active power, using only reactive power compensation. Steinmetz circuit is implemented in industrial application and large asymmetrical loads which cause a significant NS components at their bus. To understand the basics of Steinmetz circuit, assume that we have a single phase load connected at the PCC of three phase network i.e. three-wires network as shown in fig 3.1.



Fig. 3.1 Thevenin Network with single phase load

For simplicity, assume that the load power factor is unity i.e. only active power load. Hence, the phase currents are $(I_a = 0, I_b = I_{load} \text{ and } I_c = -I_{load})$ which causes a NS current in the network and unbalance PCC voltages $(V_a \neq V_b \neq V_c)$. To balance such a load, a current source is needed, between phase a and b, which provides a current that lags the line to line voltage (V_{ab}) . Another current source is needed, between phase c and a, which provides a current that leads the line to line voltage (V_{ca}) . This could be achieved by connecting an inductor and a capacitor as illustrated in fig 3.2.



Fig. 3.2 Thevenin Network with single phase load in the present of Steinmetz circuit.

Hence, the post currents with Steinmetz circuit are given by 3.1. Fig 3.3 shows the phasor digram of the voltage and current vectors, with and without Steinmetz circuit, for a single phase load of a unity power factor. Notice, the network currents $(I'_a, I'_b \text{ and } I'_c)$ are now balanced, i.e. PS current only, compared with the case without Steinmetz circuit (I_b and I_c). Hence, this will make a perfectly balanced phase voltages at the PCC i.e. ($V_a = V_b = V_c$). The reactances of Steinmetz circuit capacitor and inductor are chosen according 3.2, for unity and non unity load respectively, to ensure balanced network current and PCC voltage for the load in fig 3.2 [35].

$$I_a' = I_{ind} - I_{cap} \tag{3.1a}$$

$$I_{b}^{'} = I_{load} - I_{ind} \tag{3.1b}$$

$$I_c^{'} = I_{cap} - I_{load} \tag{3.1c}$$

$$X_{cap} = X_{ind} = \sqrt{3}R_{load} \tag{3.2a}$$

$$\frac{1}{Z_{load}} = \frac{e^{j\frac{\pi}{6}}}{|X_{cap}|} + \frac{e^{-j\frac{\pi}{6}}}{|X_{ind}|}$$
(3.2b)



Fig. 3.3 Voltage and current vectors for the network in fig 3.2.

In order to understand how the simple Steinmetz circuit balance the single phase load, consider having a variable inductor and capacitor in fig 3.2 instead of fixed one. Then, the inductive and capacitive currents magnitude are expressed by 3.3 assuming a sinusoidal steady state, neglected voltage drop in the network impedance and zero phase reference of the line PS voltage [35].
$$I_{ind} = \beta_1 \frac{S}{V_{ab}} I \tag{3.3a}$$

$$I_{cap} = \beta_2 \frac{S}{V_{ca}} I \tag{3.3b}$$

Where (S) and (I) are the rated power and maximum current of the variable impedance and $(0 \le \beta_{1,2} \le 1)$. In the complex domain, the inductive and capacitive currents are expressed by 3.4 [35].

$$I_{ind} = \beta_1 I e^{j(\varphi_{V_{ab}} - \frac{\pi}{2})} = \beta_1 I e^{-j\frac{\pi}{3}}$$
(3.4a)

$$I_{cap} = \beta_2 I e^{j(\varphi_{V_{ca}} + \frac{\pi}{2})} = \beta_2 I e^{j\frac{4\pi}{3}}$$
(3.4b)

Hence, the currents (I'_a, I'_b) and $I'_c)$, assuming no load is initially connected to the PCC, are expressed by 3.5 [35].

$$I'_{a} = I_{ind} - I_{cap} = -a\beta_{1}I - a^{2}\beta_{2}I$$
(3.5a)

$$I_{b} = -I_{ind} = a\beta_{1}I \tag{3.5b}$$

$$I_c' = I_{cap} = a^2 \beta_2 I \tag{3.5c}$$

Where (a) and (a^2) are rotation operators and equal to ($1 < 120^{\circ}$) and ($1 < 240^{\circ}$) respectively. The PS and NS currents in (I'_a , I'_b and I'_c) are obtained, using the transformation equation 2.5b, by 3.6 [35].

$$I_{1}^{'} = j \frac{\sqrt{3}}{3} I(\beta_{1} - \beta_{2})$$
(3.6a)

$$I_{2}^{'} = \frac{\sqrt{3}}{3} I(\beta_{1} e^{-j\frac{\pi}{6}} + \beta_{2} e^{j\frac{\pi}{6}})$$
(3.6b)

Fig 3.4 shows the PS and NS current vectors from Steinmetz circuit. Notice, the circuit compensates a purely reactive PS current as given by 3.6a. The magnitude of the compensator NS current vector is limited to the rating of the impedance and its maximum value is $(|I'_2|_{\beta_1=1} = \sqrt{3}/3I \text{ and } |I'_2|_{\beta_2=1} = \sqrt{3}/3I)$ for the inductive and capacitive range respectively. Also, the position of the NS vector is limited between the phase range of $(\frac{-\pi}{6} \text{ and } \frac{\pi}{6})$. Importantly, the PS and the NS current from Steinmetz circuit can not be controlled individually which is a major drawback of such a compensator.



Fig. 3.4 PS and NS vectors of Steinmetz circuit in fig 3.2.

The NS current vector in the network, caused by the single phase load, must be within the compensator magnitude limit with a load phase between $(\frac{-\pi}{6} \le \varphi_{load} \le \frac{\pi}{6})$ in order to reach a full NS current elimination which satisfies equation 3.7

$$I_{2}' = -I_{2}^{load}$$
 (3.7)

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After the compensation, the NS current is given by 3.8.

$$I_2 = \frac{\sqrt{3}}{3} I(\beta_1 e^{-j\frac{\pi}{6}} + \beta_2 e^{j\frac{\pi}{6}}) - j\frac{\sqrt{3}}{3} I_{load}$$
(3.8)

The solution for 3.8 enable us to find the values of $(\beta_{1,2})$, in terms of load current magnitude and angle or active and reactive power, which is given by 3.9 [35].

$$\beta_1 = \frac{1}{I} \left\{ \frac{I_{load} \cos(\varphi_{load})}{\sqrt{3}} + I_{load} \sin(\varphi_{load}) \right\}$$
(3.9a)

$$\beta_2 = \frac{1}{I} \left\{ \frac{I_{load} \cos(\varphi_{load})}{\sqrt{3}} - I_{load} \sin(\varphi_{load}) \right\}$$
(3.9b)

$$\beta_1 = \frac{1}{S} \left\{ \frac{P_{load}}{\sqrt{3}} + Q_{load} \right\}$$
(3.9c)

$$\beta_2 = \frac{1}{S} \{ \frac{P_{load}}{\sqrt{3}} - Q_{load} \}$$
(3.9d)

3.2.2 Steinmetz circuit for three phase load

Three phase load could also causes unbalance PCC voltage and network current because of their unequal line to line impedance. In this section, the values of Steinmetz circuit susceptances are determined which enable symmetrical load seen from the PCC. In Fig 3.5, a three phase asymmetrical load $(Y_{ab}^{load}, Y_{bc}^{load})$ and Y_{ca}^{load} is connected to the PCC. The goal is to balance the load using only a shunt connected Steinmetz compensator $(Y_{ab}^{comp}, Y_{bc}^{comp})$. The load admittances and compensator susceptances are defined by 3.10 and 3.11 respectively.



Fig. 3.5 Three phase load with Steinmetz compensator

$$Y_{ab}^{load} = G_{ab}^{load} + j B_{ab}^{load} \tag{3.10a}$$

$$Y_{bc}^{load} = G_{bc}^{load} + j B_{bc}^{load} \tag{3.10b}$$

$$Y_{ca}^{load} = G_{ca}^{load} + jB_{ca}^{load} \tag{3.10c}$$

$$Y_{ab}^{comp} = jB_{ab}^{comp} \tag{3.11a}$$

$$Y_{bc}^{comp} = jB_{bc}^{comp} \tag{3.11b}$$

$$Y_{ca}^{comp} = jB_{ca}^{comp} \tag{3.11c}$$

To achieve symmetrical admittances seen from the PCC, which satisfies 3.12, the susceptances of the shunt compensator are selected according to 3.13 using nodal analysis in fig 3.5 [21].

3.2. Load Balancing Principles

$$\frac{I_a}{V_a} = \frac{I_b}{V_c} = \frac{I_c}{V_c} = h + jk \tag{3.12}$$

$$B_{ab}^{comp} = \frac{1}{\sqrt{3}} (G_{ca}^{load} - G_{bc}^{load}) - B_{ab}^{load} + \frac{k}{3}$$
(3.13a)

$$B_{bc}^{comp} = \frac{1}{\sqrt{3}} (G_{ab}^{load} - G_{ca}^{load}) - B_{bc}^{load} + \frac{k}{3}$$
(3.13b)

$$B_{ca}^{comp} = \frac{1}{\sqrt{3}} (G_{bc}^{load} - G_{ab}^{load}) - B_{ca}^{load} + \frac{k}{3}$$
(3.13c)

Where (k) is an arbitrary load susceptance and (h) depends on the load conductance which is given by 3.14.

$$h = G_{ab}^{load} + G_{bc}^{load} + G_{ca}^{load}$$
(3.14)

Furthermore, 3.15 gives the required reactive power from the compensator, in terms of load active and reactive power, to achieve symmetrical load seen from the PCC. In [21], the detailed derivation of the equations in this section is presented. Also, an alternative equations are given if the shunt compensator is connected in star rather than delta.

$$Q_{ab}^{comp} = -\frac{1}{\sqrt{3}} (P_{ca}^{load} - P_{bc}^{load}) - Q_{ab}^{load}$$
(3.15a)

$$Q_{bc}^{comp} = -\frac{1}{\sqrt{3}} (P_{ab}^{load} - P_{ca}^{load}) - Q_{bc}^{load}$$
(3.15b)

$$Q_{ca}^{comp} = -\frac{1}{\sqrt{3}} (P_{bc}^{load} - P_{ab}^{load}) - Q_{ca}^{load}$$
(3.15c)

3.2.3 Steinmetz circuit for three phase load with transformer

In practice, it is usually impossible to connect Steinmetz compensator, i.e. an SVC, to the HV side due to the limitation in the thyristor valves. Thus, transformer is essential which is normally connected as grounded star in the HV side (primary) and delta in the LV side (secondary) as shown in fig 3.6. Assuming an ideal transformer, with $(n : \sqrt{3})$ turns ratio, and balanced PCC voltage, the transformation between the secondary compensator susceptance (B^{comp}) to the primary susceptance $(B^{comp'})$ is give by 3.16. Additionally, 3.17 gives the transformation in terms of the reactive power. The transformation is still valid even if the PCC voltages are unbalance given that the voltages add to zero i.e. the zero sequence voltage is equal to zero [21].



Fig. 3.6 Three phase load with Steinmetz compensator

$$B_{ab}^{comp} = \frac{n^2}{3} (2B_{ab}^{comp'} + 2B_{bc}^{comp'} - B_{ca}^{comp'})$$
(3.16a)

$$B_{bc}^{comp} = \frac{n^2}{3} \left(2B_{bc}^{comp'} + 2B_{ca}^{comp'} - B_{ab}^{comp'} \right)$$
(3.16b)

$$B_{ca}^{comp} = \frac{n^2}{3} (2B_{ca}^{comp'} + 2B_{ab}^{comp'} - B_{bc}^{comp'})$$
(3.16c)

$$Q_{ab}^{comp} = \frac{1}{3} \left(2Q_{ab}^{comp'} + 2Q_{bc}^{comp'} - Q_{ca}^{comp'} \right)$$
(3.17a)

$$Q_{bc}^{comp} = \frac{1}{3} (2Q_{bc}^{comp'} + 2Q_{ca}^{comp'} - Q_{ab}^{comp'})$$
(3.17b)

$$Q_{ca}^{comp} = \frac{1}{3} (2Q_{ca}^{comp'} + 2Q_{ab}^{comp'} - Q_{bc}^{comp'})$$
(3.17c)

3.3 Static Var Compensator Characteristic

Static var compensator (SVC) is a shunt connected static var generator or absorber which allows the controllability of specific parameters, such as bus voltage in the power system, by adjusting its capacitive and inductive current [27]. It is one of the power electronic devices from the flexible ac transmission system (FACTS) controllers family. The SVC is based on passive elements, capacitors and inductors, with the help from thyristor valves. Thyristors are mostly used in FACTS controllers for high voltage application due to their capability of high voltage and current rating at low cost, low forward voltage drop and high overloading. A thyristor starts conducting in its forward direction when a firing current is applied to its gate and the anode electrode is positive with respect to the cathode. Once the thyristor is at full conduction, their forward voltage drop is usually low which enables a low conduction loss. A conventional thyristor, used in the SVC, can not bring the current to zero i.e. turn off capability. However, there are other thyristor types with a turn off circuit such as gate turn off thyristor (GTO) which uses the concept of reverse current applied to the gate. Unfortunately, the turn off capability usually causes higher loss and cost which does not justify its benefits [27]. Thyristor can be designed to block in the forward and reverse direction with blocking voltage between 4 kV to 9 kV [27]. In practice, they are connected in series to reach the desired blocking voltage. The SVC is mainly implemented in the power system for dynamic voltage control, power transfer capacity enhancement and load balancing applications. The dynamic voltage control prevents the power system form voltage collapse and temporary overvoltages. The SVC also improves the transient and voltage stability and system damping. The SVC consists of thyristor controlled reactor (TCR) and thyristor switched capacitor (TSC) which are discussed in the following text.

3.3.1 Thyristor controlled reactor

The TCR is a shunt connected static var absorber which has a continuous control of the thyristor valve to achieve the desired effective reactance. Fig 3.7 shows the basic circuit of a single phase TCR which consists of a fixed reactor of inductance (L) and bidirectional thyristor valve.



Fig. 3.7 TCR circuit digram

The concept of continuous firing angle control of the TCR thyristor valve allows a controllability of its current from maximum current i.e. closed thyristor to zero current i.e. open thyristor. Fig 3.8 shows the TCR current, $i_L(\alpha)$, for the positive and negative half cycle of the applied voltage i.e. v(t) = V cos(wt). If the thyristor firing angle (α) is zero, i.e. fully on valve, the TCR current is $i_L(\alpha = 0)$. By using a delay angle $(0 \le \alpha \ge \frac{\pi}{2})$ with respect to the applied voltage peak, the closure of the thyristor valve is controlled which enables a continuous TCR current control expressed by 3.18 [27] [34]. Also, the higher the delay angle (α), the lower the conduction angle ($\sigma = \pi - 2\alpha$) of the thyristor. Therefore, the TCR current is controlled from full, partial and minimum conduction as shown in fig 3.9. The amplitude of the TCR current fundamental frequency components, $I_{LF}(\alpha)$, is expressed by 3.19 as a function of the delay angle (α) [34]. Hence, the TCR seems as a normal inductor with a controllable effective admittance expressed by 3.20. Fig 3.10 and 3.11 illustrates the variation of the TCR current and susceptance with the firing angle (α).

$$i_L(t) = \frac{1}{L} \int_{\alpha}^{wt} v(t) dt = \frac{V}{wL} (\sin(wt) - \sin(\alpha))$$
 (3.18)

$$I_{LF}(\alpha) = \frac{V}{wL} \left(1 - \frac{2}{\pi} \alpha - \frac{1}{\pi} \sin(2\alpha) \right)$$
(3.19)

$$B_L(\alpha) = \frac{1}{wL} \left(1 - \frac{2}{\pi} \alpha - \frac{1}{\pi} \sin(2\alpha) \right)$$
 (3.20)



Fig. 3.9 TCR voltage and current for fully, partial and minimum conduction.

Fig. 3.8 TCR firing angle control for the positive and negative half cycles.



Fig. 3.10 TCR susceptance Vs firing angle

Fig. 3.11 TCR current Vs firing angle.

3.3.2 Thyristor switched capacitor

The TSC is a shunt connected static var generator which has a stepwise control, from full to zero conduction of the thyristor valve, to achieve the desired effective reactance [27]. Fig 3.12 shows the basic circuit of a single phase TSC which consists of a fixed capacitor with capacitance (C), bidirectional thyristor valve and a small damping reactor with inductance (L). The damping inductance is needed to limit the transient surge current when switching the thyristor at a wrong time instant and during overvoltages. Switching an ac voltage source (v(t)) to a capacitor would causes an infinite current, that charges the capacitor in very short time, to the supply voltage if the capacitor initial voltage and the supply voltage are unequal i.e. $V \neq V_{c0}$ [34]. However, if both, supply voltage and capacitor initial voltage are equal at the switching time instant, the current will jump to the steady state current in infinity short time. Such issues would cause infinite (di/dt) which will increase the stress in the thyristor valves [34]. The stress might cause malfunctions in the valves since they have limited current change with time. The damping inductance might be used to filter the harmonics, generated by the TCR, and avoid resonances with the ac system impedance [27] [34].



Fig. 3.12 TSC circuit digram

The equation of the TSC circuit in fig 3.12 is expressed by 3.21a assuming an applied voltage of $(v(t) = V \sin(w_0 t + \alpha))$. The homogeneous and the particular steady state solution for such an equation are expressed by 3.21b and 3.21c respectively.

$$v(t) = LC \frac{d^2 v_c(t)}{dt^2} + v_c(t)$$
(3.21a)

$$v_{co}(t) = 2k\cos(w_n t + \theta). \tag{3.21b}$$

$$v_{cp}(t) = V \frac{n^2}{n^2 - 1} \sin(w_0 t + \alpha)$$
 (3.21c)

Hence, the capacitor voltage and current, assuming initial conditions of $(i_c(0) = 0 \text{ and } v_c(0) = V_{c0})$, are give by 3.22a and 3.22b respectively.

$$v_c(t) = v_{co}(t) + v_{cp}(t) = 2k\cos(w_n t + \theta) + V\frac{n^2}{n^2 - 1}\sin(w_0 t + \alpha)$$
(3.22a)

$$i(t) = I_{AC} \cos(w_0 t + \alpha) - nB_c (V_{co} - V \frac{n^2}{n^2 - 1} \sin \alpha) \sin w_n t - I_{AC} \cos \alpha \cos w_n t$$
(3.22b)

Where (w_0) is the fundamental nominal frequency of the sinusoidal supply voltage and (w_n) is the natural resonance frequency which is expressed by 3.23a. Also, the per unit natural frequency is given by 3.23b.

$$w_n = nw_0 = \frac{1}{\sqrt{LC}} \tag{3.23a}$$

$$w_n = \sqrt{\frac{\mid XC \mid}{\mid XL \mid}} \tag{3.23b}$$

Therefore, 3.22b tells us that the TSC current consist of a steady state current with (w_0) and an oscillating transient current with (w_n) . The peak current, with the present of a damping reactor, is given by 3.24.

$$\hat{I_{AC}} = B_c V \frac{n^2}{n^2 - 1}$$
(3.24)

The term $\left(\frac{n^2}{n^2-1}\right)$ is a magnification factor which amplifies the peak current compared to the case if a damping reactor is not presented. The TSC should be tuned for resonance frequency $(3w_0)$ and higher to keep the magnification factor close to 1 [34]. Otherwise, the magnification factor is increasing rapidly for tuning frequencies lower than $(3w_0)$. In order to eliminate the oscillating transient current in 3.22b, $(\cos \alpha)$ should be equal to zero. This means the thyristor must switch at the positive or the negative peak instant of the grid voltage. Another condition of eliminating the TSC transient current is having an initial capacitor voltage of $(V_{co} = \pm V \frac{n^2}{n^2-1})$. In practice, it is always impossible to satisfy such conditions due to several reasons such as, not having a purely sinusoidal gird voltage and charging the capacitor with a voltage that is higher than the grid voltage requires additional charging circuit.

3.3.3 SVC operating principles

The typical voltage-current digram of a conventional SVC is shown in fig 3.13. The SVC current varies between the capacitive and inductive range, depending on the required system load line, to keep a constant voltage reference (Vref). The system load line represent a thevenin equivalent of the network (V = E - jXI) which gives the magnitudes of the bus voltage for each value of the system voltage (E). Normal SVC application requires higher capacitive current, to improve the bus voltage, which requires nTSC. The capacitive current changes in discrete steps i.e. either on or off TSC. The inductive current changes continuously to absorb the capacitive current surplus from the nTSC which insures continuous voltage regulation at the bus. Unlike fixed capacitor and TCR configuration, the TCR rating is reduced by (1/n) of the maximum capacitive current in nTSC-TCR configuration [27] [34]. Hence, the non sinusoidal harmonic components generated by the TCR reduce significantly. A current droop, by allowing a 3-5% voltage error in the SVC bus, reduces the size of the SVC or enables larger regulation range (keeping the same size).



Fig. 3.13 SVC voltage and current digram

3.4 Harmonics Generation of Thyristor Controlled Reactor

The TCR current consists of the fundamental frequency current component and non sinusoidal harmonics current for firing angles between 90° and 180° . For a single phase TCR, the non sinusoidal current harmonics is expressed by 3.25.

$$I_n(\alpha) = \frac{V}{wL} \frac{2}{\pi} \left(-2\frac{\cos\alpha}{n}\sin n\alpha + \frac{\sin(n-1)\alpha}{n-1} + \frac{\sin(n+1)\alpha}{n+1}\right)$$

$$= \frac{V}{wL} \frac{4}{\pi} \left(\frac{\sin(\alpha)\cos(n\alpha) - n\cos(\alpha)\sin(n\alpha)}{n(n^2-1)}\right)$$
(3.25)

Where (n = 2k + 1, k = 1, 2, 3, ...) and V is the rms value of the voltage applied to the TCR of inductance (L). The harmonic currents (n = 3, 5, 7, 9...) are function of the firing angle (α) and reach their peak at (n - 1)/2 points which corresponds to a maximum firing angle, that gives the highest current harmonic, given by 3.26. Fig 3.14 illustrates the TCR current harmonics in pu as a function of the thyristor firing angle. We can notice that all harmonics do not reach the peak value at the same firing angle. The highest peak is in the 3rd, 5th and 7th current harmonics.

$$\alpha_{n,max} = \pi - \frac{k\pi}{n}, \ k = 1, 2, 3, ..., \frac{n-1}{2}$$
(3.26)



Fig. 3.14 Magnitude of the harmonic components in the TCR current as a function of the firing angle

For three phase TCR, they are normally connected in delta, i.e. six-pulse TCR, as shown in fig 3.15. There are three reasons that causes the network currents, (i_a, i_b, i_c) , to consists of the multiples of 3rd harmonics current. First, assigning different firing angle (α) for each TCR branch in the delta connection i.e. asymmetrical control of the TCRs. Second, non identical inductance values (L_{TCR}) in each TCR branch. Third, unbalance line to ground voltage in the ac system which causes a NS components in the network current. If non these reasons are employed, the multiples of the 3rd harmonics TCR current will circulate in the delta connection and do not propagates towards the network. The 3rd harmonic currents in the delta are displaced by 3 times 120° because of the 3 times higher frequency as expressed in 3.27 [34]. Hence, the network current will not consists of a 3rd harmonic current according to 3.28. However, other characteristic harmonics, of order ($n = 6m \pm 1$) where (m = 1, 2, 3, ...) such as 5th, 7th, 11th...etc, are injected toward the network with a 6 puls configuration.

$$i_{ab3} = \hat{i_3}\cos(3wt + \phi_3) \tag{3.27a}$$

$$i_{bc3} = i_3 \cos(3wt + \phi_3 - 3 * 120^\circ) \tag{3.27b}$$

$$i_{ca3} = i_3 \cos(3wt + \phi_3 + 3 * 120^\circ) \tag{3.27c}$$

$$i_a = i_{ab} - i_{ca} \tag{3.28a}$$

$$i_b = i_{bc} - i_{ab} \tag{3.28b}$$

$$i_c = i_{ca} - i_{bc} \tag{3.28c}$$



Fig. 3.15 Delta connection of three phase TCR

In load balancing application, each TCR in the delta connection is controlled individually i.e. asymmetrical controller. Hence, the worst situation, with respect to the 3rd harmonic current in the network, is when one of the TCR is conducting at firing angle of 120° while another TCR is either at full or zero conduction i.e. 90° and 180° . Hence, the maximum 3rd harmonic in the network current is approximately equal to 0.1379 pu (see fig 3.14). Another issues is having some tolerance in the TCR inductance (L_{TCR}) for each delta phase TCR in practice. Moreover, the ac system supply voltage is never balanced in reality. Therefore, the instillation of a third harmonic filter is essential in practice even with the six-pulse TCR configuration. Normally, the 3rd harmonic filter is designed assuming the three causes, of not blocking the 3rd harmonic current inside the delta, appear simultaneously.

3.5 Switching Strategies of Thyristor Switched Capacitor

There are two typical switching strategies that limit the TSC transient current to an adequate level when switching on the TSC in fig 3.12. They mostly depends on the residual capacitor voltage and explained as flow [27] [34]:

First Strategy: The capacitor residual voltage must be equal or less than the grid voltage i.e. (V_{co} ≤ V). With such a condition is satisfied at the time instant when the TSC is needed, the thyristor should be switched when the capacitor and the supply voltage are equal or when voltage across the thyristor is zero. Hence, the firing angle is given by 3.29a which makes an oscillating current magnitude (I_{osc}) given by 3.29b using 3.22b. Notice, the higher the discharged the capacitor i.e. (V_{co} ≈ 0), the highest the oscillating transient current. On the other hand, the lowest oscillating transient current occurs for approximately fully charged capacitor in high tuned resonance frequencies.

$$\alpha = \sin^{-1} \frac{V_{co}}{V} \tag{3.29a}$$

$$\frac{I_{osc}}{I_{AC}} = \sqrt{1 - \left(\frac{V_{co}}{V}^2\right) - \left(1 - \frac{1}{n^2}\right)}$$
(3.29b)

• Second Strategy: A higher residual voltage in the capacitor than the supply voltage i.e ($V_{co} > V$) is possible at the time instant when the TSC is needed. Therefore, the thyristor must be switched when the supply peak voltage is reached and the thyristor voltage is at its minimum value. Hence, the firing angle is given by 3.30a which makes an oscillating current magnitude (I_{osc}) given by 3.30b. Fig 3.16 shows the switching strategy for the free transient where the switching instant is marked with a bold circle.

$$\alpha = \cos^{-1}(0) \tag{3.30a}$$

$$\frac{I_{osc}}{I_{AC}} = n(\frac{n^2 - 1}{n^2} \frac{V_{co}}{v} - 1)$$
(3.30b)



Fig. 3.16 First and second strategies for free transient switching.

From the aforementioned switching strategies, there is a maximum of a full cycle delay, of the supply voltage, to switch the TSC at the right instant for minimum or free transient. Therefore, the TSC can only switch on in steps and does not have a continuous control that TCR provides. Additionally, switching out the TSC could be at the zero crossing of the current which causes the capacitor to be at peak which is given by 3.31. Therefore, the voltage blocked by the thyristor will be between zero and the rated line to line supply voltage. Hence, they have to be designed to withstand twice the supply voltage. Fig 3.17 shows the waveforms when turning the TSC off [34].

$$V_{c,i=0} = V \frac{n^2}{n^2 - 1}$$
(3.31)



Fig. 3.17 Ideal waveforms of switching off the TSC

3.6 SVC Voltage Controller Components

The overall controller components, SVC circuit and network equivalent circuit are illustrated in fig 3.18. The SVC voltage controller components are discussed as follow.

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Fig. 3.18 SVC circuit, controller components and network equivalent circuit

3.6.1 Synchronization system

An accurate detection of the system voltage angle at the SVC bus is essential to avoid a wrong firing pulse if a sudden change occurs in the voltage angle position. There are three methods used to detect the SVC bus voltage angle. The integration of the system constant fundamental frequency is one the methods to detect the voltage angel. However, the system frequency deviates and never stays at constant value in practice. Another method is by detecting the zero crossing of the voltage which can not be distinguished in the present of noise and harmonics. It is also not valid if the three phase voltages are unbalance since only one phase is measured while calculating the other two phases.

Alternatively, a phase-locked loop (PLL) is the most accurate method to detect the system voltage angle. It is designed to phase lock the voltage which enables proper voltage control at the SVC bus. The basic block digram of the PLL is shown in 3.19. The three phase voltages are measured then transformed to a voltage vector in $(\alpha\beta)$ system. The voltage vector is transformed to the (dq) system using an initial or predetermined value of the voltage angle (see appendix A for transformations between the systems). After that, the angle between the d-axis and the voltage vector is calculated which is used as an input to a PI regulator. Integrating the summation of the PI error and the nominal frequency gives the angle reference which is fed to the (dq) block to lock the d-axis with the voltage vector.



Fig. 3.19 Block digram of the PLL

3.6.2 Sequence components extraction

To control the reactive component of the PS voltage and the active and reactive components of the NS voltage, it is essential to extract the PS and NS components from the measured three phase voltage accurately. One method is to first transform the latest value of the SVC bus unbalance voltage vectors to (dq) coordinates which consists of two synchronous reference frames (SRFs) i.e.the PS SRF (dq^+) and the NS SRF (dq^-) (see the transformation method in appendix A.3). The PS and NS components are extracted by combining the latest obtained signal with the same signal delayed by one quarter of a cycle [37] [16]. This method is described in the relationship expressed by 3.32

$$v_{dq^+}(t)_1 = \frac{1}{2}(v_{dq^+}(t) + v_{dq^+}(t - \frac{T}{4}))$$
(3.32a)

$$v_{dq^{-}}(t)_{2} = \frac{1}{2}(v_{dq^{-}}(t) + v_{dq^{-}}(t - \frac{T}{4}))$$
(3.32b)

Where

- $v_{dq^+}(t)_1$ is the extracted PS voltage at the SVC bus using the PS SRF (dq^+) .
- $v_{dq^+}(t)_2$ is the extracted NS voltage at the SVC bus using the NS SRF (dq^-).
- $v_{dq^+}(t)$ is the SVC bus voltage in the PS SRF (dq^+). (see equation A.12a in appendix A.3)
- $v_{dq^-}(t)$ is the SVC bus voltage in the NS SRF (dq^-). (see equation A.12b in appendix A.3)
- T is the cycle at the fundamental frequency.

3.6.3 Positive sequence voltage regulator

The function of the PS voltage regulator is to provide a dynamic control of the PS voltage at SVC bus. In other words, the PS voltage regulator generates an output signal that compensates for the bus reactive power to reach the desired reference voltage. Fig 3.20 shows the susceptance droop model of the PS voltage regulator. It is a closed loop system which controls the PS voltage at the SVC bus i.e. $(V_{1,meas})$. The measured PS voltage is compared with the PS reference voltage $(V_{1,ref})$ and the SVC current (I_{svc}) to give an error signal used in the PI regulator. The SVC current is adjusted by the current droop which enables the advantages discussed previously (see 3.3.3). The PI regulator is normally an integrator expressed by 3.33 [34].

$$V_R(s) = \frac{1}{sR_R} \tag{3.33}$$

Where (R_R) is the response rate in (ms/pu) which is the time taken by the SVC to move from fully capacitive to fully inductive [34]. The PS voltage regulator output is the SVC PS susceptance reference $(B_{1,ref})$ which is used to determine the firing angles of the TCR and the TSC. The PI regulator output susceptance is limited by a maximum and a minimum values which are determined by the available SVC susceptance and other protection function such as the TCR valves limit. The advantages of the susceptance droop model is to overcome the difficulties of measuring the SVC current when it is operating close to zero reactive power. The SVC current, in such an operating point, consists of harmonic components and fundamental resistive components [34]. Therefore, the (I_{svc}) signal is obtained by the close loop where the suceptance is measured and multiplied by bus voltage, i.e. $(I_{svc} = B_{1,ref}V_{1,meas})$, assuming a fairly constant voltage at the SVC bus.



Fig. 3.20 Susceptance droop PS voltage regulator.

3.6.4 Negative sequence voltage regulator

Due to the confidential information the SVC NS controller contains, only a basic description is provided in this report. A simple block of the SVC NS voltage regulator is shown in fig 3.21 which is based on a PI regulator where the measured NS voltage at the SVC bus is used as an input. Then, it is compared with the desired VUF at the SVC bus which is normally between 1-3% depending on the voltage level and the asymmetrical load. The NS voltage regulator generates an output signal $(B_{2,ref})$ which is used to calculate the individual firing pulses of each TCR in the delta connection. The value of the PS suceptance $(B_{1,ref})$ is used to compromise the priority between the NS and PS voltage regulators. In other words, it is used as a limitation for the NS voltage regulator when the PS voltage is in operation and has a priority. This way the NS voltage regulator will not assume to have the whole range of the SVC susceptance and limited to the left susceptance after compensating for the PS components.



Fig. 3.21 Simple block of the PS voltage regulator.

3.6.5 Gate pulse generator

In the gate pulse generator (GPG), the PS and NS susceptance reference, from the PS and NS voltage regulators are used as inputs. These susceptances are the needed one in the primary side of the SVC transformer. The NS susceptance has to be splitted between the delat connected TCRs according to Steinmetz equations discussed in 3.2.3. From these susceptances, the firing angles of the TCRs are calculated in the GPS using the susceptance-angle relation discussed in 3.3.1. With a logic circuit, the GPG calculates the number of TSCs needed which are, in this controller, only switched on or off if a PS compensation is required. The GPG has to follow the switching strategies, discussed in 3.5, to insure minimum or free transient in the TSCs current. The output of the GPS are the firing pulses of the delta connected TCRs and TSCs.

3.7 SVC and VSC Comparison

A static synchronous compensator (STATCOM) is a shunt connected compensator, based on either voltage source converter (VSC) or current source converter, which inject or absorb capacitive and inductive current independent of the ac system voltage [27]. A simple configuration for the VSC is shown in fig 3.22 which is connected to a network with asymmetrical load. It consists of a VSC, dc-link capacitor (V_{dc}), an ac filter (X_L) and a transformer of reactance (X_T). In some applications, the VSC is equipped with energy storage to exchange active power with the ac system. The VSC is based on insulated gate bipolar transistors (IGBTs) which have fast turn on and off capability and high switching frequency [27]. The well known topologies of the VSC are the two level and the Neutral Point Clamped (NPC) three level converters [17]. Similar to the SVC, VSC can be use for dynamic voltage control and load balancing. The basic operating idea of VSC is to provide dynamic voltage control for the PCC voltages $(V_a^{pcc}, V_b^{pcc} \text{ and } V_c^{pcc})$ by injective a capacitive and reactive current. This is done by controlling the amplitude of the fundamental frequency voltage (V_{vsc}) using pulse width modulation (PWM) pattern. This imposed voltage (V_{vsc}) depends on the dc link capacitor voltage (V_{dc}) and the modulation index. Fig 3.23 shows the PCC and VSC imposed voltage vectors for three operating conditions assuming balanced ac system voltage and zero power loss in the converter. First, the VSC does not inject any current if the voltage at the PCC and VSC are equal. In case of lower voltage at the PCC than the VSC i.e $(V^{pcc} < V^{vsc})$, the VSC injects a capacitive current. If $(V^{pcc} > V^{vsc})$, the VSC injects an inductive current $(X = X_L + X_T)$.



Fig. 3.22 Shunt connected VSC to a network with asymmetrical load.

$$\mathbf{V}^{\text{vsc}} \left[\begin{array}{c|c} \mathbf{V}^{\text{pcc}} & \mathbf{V}^{\text{vsc}} \\ \mathbf{I}^{\text{vsc}} \end{array} \right] \left[\begin{array}{c|c} \mathbf{j} \mathbf{X} \mathbf{I}^{\text{vsc}} \\ \mathbf{V}^{\text{pcc}} & \mathbf{V}^{\text{pcc}} \end{array} \right] \left[\begin{array}{c|c} \mathbf{j} \mathbf{X} \mathbf{I}^{\text{vsc}} \\ \mathbf{V}^{\text{vsc}} \\ \mathbf{I}^{\text{vsc}} \end{array} \right]$$

Fig. 3.23 Voltage and current vectors of the VSC and PCC for three operating conditions

Comparing the voltage-current characteristics for the SVC and the VSC, the SVC maximum current decreases linearly with the ac system voltage as shown in fig 3.24. On the other hand, the VSC could operate at its full current at low voltage of the ac system i.e 0.2 pu. This is because the SVC consists of passive elements which become as fixed admittance at full output and they depends on the system ac voltage. The VSC shows better dynamic voltage support since its current is controlled independently of the ac system voltage. The VSC also has a higher transient rating in both capacitive and inductive range while the SVC has no higher transient rating in the capacitive range. This is because the SVC capacitive current is determined by the capacitor size while it is determined by the maximum current turn off capability of the semiconductors in the VSC [27]. Additionally, the VSC shows much faster time response than the SVC i.e. 0.5 to 2 cycles which allows the VSC to be superior to the SVC in precise continuous control [27] [17]. The size of the VSC is 30% to 40% less than the SVC becuase of the passive elements in the SVC [27].

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Fig. 3.24 SVC and STATCOM voltage-current digram.

In load balancing applications, the VSC consequence is similar to the SVC which is injecting a NS current with equal amplitude of the load NS current but with an opposite phase shift. However, the design criteria for the VSC in unbalanced PCC voltages is different than if the PCC voltages were balanced. Because the VSC has no energy storage in the dc link side, the instantaneous power between the ac and the dc should be equal. However, that is not the case if the PCC voltages are unbalanced and a NS power, with double fundamental frequency, is seen in the ac side. This will cause a second harmonic ripple current in the dc side that will generates an internal NS components in the converter plus a PS third harmonic components which might transformed into the ac side [27]. Hence, the dc link capacitor has to be designed with sufficient size to limit the second harmonic ripple current [27]. In general, the VSC has significant merits than the SVC which makes it as an alternative device for dynamic voltage support and load balancing applications

3.8 Conclusion

Balancing asymmetrical load could be achieved using shunt passive elements such as Steinmetz compensator which consists of fixed capacitors and inductors. In practice, a controllable Steinmetz susceptance is essential to achieve a continuous load balancing or NS elimination. This is accomplished using an SVC which controls its shunt susceptance using bidirectional thyristor valves. However, the SVC is mainly used for PS components control rather than a NS components control. Since the delta connected TCRs are controlled individually, a 3rd harmonic current will propagates to the network which make it essential to use a filter tuned for the 3rd harmonic. In this controller, the TSCs are switched on and off if only a PS components compensation is needed. In other controller scheme, the TSCs might switch on, if only a NS components is required, to make higher room for the NS voltage regulator. There are two switching strategies which allows free or minimum transient in the TSC current. The drawback of Steinmetz compensator is the dependency on the ac system voltage and the non individual control of the PS and NS components. In contrast, VSC injects an inductive and capacitive current independently of the ac system voltage.

Chapter 4

PSCAD Simulation and Analysis

This chapter discusses the simulation setup and analysis in PSCAD. First, an equivalent thevenin network with asymmetrical passive load is studied. The same network is also used to study the impact of induction motor load. Then, the voltage unbalance propagation between different voltage level is investigated. Finally, the SVC is tested in the IEEE 14 bus test system.

4.1 Introduction

A PSCAD simulation and analysis is essential to study the SVC controller functions such as the PS and the NS voltage regulators. The SVC topology consists of six-pulse TCRs, i.e. three singe phase TCRs, and six-pulse TSCs i.e. three single phase TSCs. The SVC is also equipped with three FCs which are tuned for the 3rd, 5th and 7th harmonics. The SVC main circuit components are built in PSCAD with the help of exporting the components parameters from Matlab to PSCAD as global variables. ABB SVC controller blocks are used, for the built topology, but adjusted to be suitable for the thesis scope. Furthermore, the SVC is linked to the network by three phase wye-delta transformer. A simple network thevenin equivalent is also built in PSCAD. Other components such as passive loads, induction machine and a network with multiple level is also built. Finally, the SVC network was also construed in PSCAD. The SVC response to correct the voltage and current unbalance depends on the load type, network strength and sources of unbalance.

4.2 SVC Components Design and Setup

The SVC circuit setup in PSCAD is shown in fig.4.1. The SVC is connected to the PCC through a three phase transformer which is a star connected in the primary and delta in the secondary. There are three single phase TCRs and TSCs which are connected in delta to form one branch. The fixed capacitors (FC) are tuned for the 3rd 5th and 7th harmonic. Normally, a delta connection of the TCRs blocks the 3rd harmonics if all TCRs firing pluses are the same, balanced PCC voltage and equal TCR inductances (L_{TCR}). However, since each TCR is controlled individually, the 3rd harmonic current is not blocked inside the delta and propagates towards the network. Thus, a 3rd harmonic filter is essential.



Fig. 4.1 SVC circuit setup in PSCAD

The VI digram of the SVC is shown in fig.4.2 in a 100 MVA and 220 kV base power and voltage. At 1 pu voltage, the capacitive and inductive values are 150 MVAR (A) and 100 MVAR (B). At 1.1 pu voltage the capacitive value is 181 MVAR (C). At 1.13 pu voltage, the inductive value is 129 MVAR (D). The voltage reference is between 0.9 and 1.1 pu with a droop slop of 0-3 %. Table 4.1 illustrates the basic data of the transformer, TCR, TSC and filters.



Fig. 4.2 SVC voltage and current digram

		Transformer		
	Nominal voltage	Nominal power	Reactance	
	220/16kV	150 MVA	15.5%	
		TCR		
	Rated inductance	Damping resistance	Reactive power	
	$L_{TCR} = 6.47mH$	$R_{TCR} = 5.08m\Omega$	185 MVAR	
TSC				
Rated capacitance	Damping inductance	Damping resistance	Tuning frequency	Reactive power
$C_{TSC} = 223.58\mu F$	$L_{TSC} = 2.23mH$	$R_{TSC} = 39.58m\Omega$	225 Hz	65 MVAR
		FC		
Tuning frequency	Rated capacitance	Tuning inductance	Damping resistance	Reactive power
3rd=157.5 Hz	$C_{FC1} = 487.3\mu F$	$L_{FC} = 2.096 mH$	$R_{FC} = 28\Omega$	50 MVAR
5th=249 Hz	$C_{FC1} = 239.2\mu F$	$L_{FC} = 1.708 mH$	-	23 MVAR
7th=348.5 Hz	$C_{FC1} = 127.4\mu F$	$L_{FC} = 1.637 mH$	-	12 MVAR

Table 4.1: SVC components values

4.3 220 kV Simple Network

4.3.1 Network characteristic

The simple network is a 220 kV supply system which consists of three phase source and a network equivalent impedance. A generic asymmetrical passive load is seen from the PCC as shown in fig. 4.3. The SVC is shunt connected to the PCC through start delta transformer.



Fig. 4.3 Network Representation

The network strength describes how much a current variation would change the voltage. For instant, a week network with low short circuit power (high network impedance) has a significant voltage change when the current varies and vice versa for strong network. The current variation depends on the load which means connecting a small load to very week network makes the network seems as a strong one since the load current is low. As a base case, the 220 kV supply system is considered as a week one with a short circuit power of 750 MVA. Normally, the 220kV network is highly inductive with high value of $(\frac{X}{R})$ ratio. Load is described as the main force of unbalance and modelled as a static one using the well known exponential model expressed for active and reactive power by 4.1.

$$P = P_0 \left(\frac{V}{V_0}\right)^{\alpha} \tag{4.1a}$$

$$Q = Q_0 (\frac{V}{V_0})^\beta \tag{4.1b}$$

Where (P) and (Q) are the active and reactive components consumed by the load when the bus voltage magnitude is (V). (P_0 , Q_0 and V_0) are the rated load active and reactive power and voltage respectively. The exponents (α) and (β) describe the load active and reactive power variation or dependency to the voltage change. They are roughly the slope, i.e. $(\frac{dP}{dV})$ and $(\frac{dQ}{dV})$ when ($V = V_0$), which is equal to 0, 1 and 2 for constant power, current and impedance load respectively. Unlike constant impedance load which has a fixed impedance regardless of the input voltage, constant power and current loads vary their impedance with the input voltage change, so the power and current are fixed respectively. In other words, loads whose active and reactive power change with the voltage, i.e. constant current and impedance, will change the power flow in the network. Table 4.2 shows the data for the base case where the source phase voltages are balanced, the network phase impedances are equal which is equivalent to fully transposed lines. In the following tests, the passive asymmetrical load is mixed of constant power, current and impedance. However, considering each load type individually is tested as well. The load was selected in such a way that the PCC voltage in not less than 0.9 pu, with 750 MVA short circuit level, but causes a higher voltage unbalance than the planning level in HV network i.e. 1.4% (see table 2.5).

Table 4.2: Base case data

Source	Transmission	Load	
$E_a: 127kV < 0^\circ$	$Z_a^{netw} = Z_b^{netw} = Z_c^{netw}$	A=60 MW+24 MVAR	
$E_b: 127kV < 240^\circ$	$S_{sc} = 750 MVA$	B=39.9 MW+12 MVAR	
$E_c: 127 kV < 120^\circ$	$\frac{X}{R} = 10$	C=19.9 MW+4.9 MVAR	

4.3.2 SVC voltage regulators comparison

Normally, the SVC operates with a PS voltage regulator or controllers. However, a NS voltage regulator function could be added to the SVC in certain applications such as railway load. When the SVC operates with a PS voltage regulator only, it just regulates the voltage at the PCC between certain values (0.9-1.1 pu). In other words, it acts as a power factor correction by mitigating the reactive components of the load PS current. When the SVC operates with a NS voltage regulator only, its mission is to mitigate the NS current in the network caused by the asymmetrical load. Hence, the voltage unbalance at the PCC is reduced to a certain deadband i.e. close to the planning level. Therefore, the supply system should continuously see a fairly symmetrical load. When the SVC has both PS and NS voltage regulators, it tries to do both i.e. regulating the voltage at the PCC and reducing the network NS current. However, the SVC can not control the PS and the NS individually because they are decoupled by definition (see 2.2 and 3.2). In this thesis, the SVC controller is designed for a PS mitigation priority rather than a NS mitigation by setting a controller limitation to the NS voltage regulator. In other words, the SVC will first regulate the PCC voltage to the reference value by assigning a PS susceptance from the PS voltage regulator. The remaining susceptance, from the SVC, is then used in the NS voltage regulator. This way the NS voltage regulator will not have the whole SVC susceptance (see 3.6).

SVC with a PS voltage regulator only:

In this case, the SVC works with a PS voltage regulator only and the NS voltage regulator is off. The base case mixed asymmetrical load is used and the network short circuit level is 750 MVA. Fig. 4.4 shows the SVC current, reactive power and TCRs susceptances. The SVC injects a different current in each phase to regulate the PCC voltage between (0.9-1.1 pu). The TCRs susceptance for each phase are equal because there is no asymmetrical controller, i.e. individual control of each single phase TCR in the delta connection,

when the SVC operates with a PS voltage regulator only. They also have a very low values because of the low voltage at the PCC and more TSCs current is needed than TCRs current to improve the PCC voltage. The reason that the SVC is injecting different current in each phase is the asymmetrical load which causes unequal phase voltages seen by the SVC. These unequal phase voltages are measured and sent to the controller which will switch the TSCs according to the strategies discussed in (3.5) for minimum or free transient. Hence, the TSCs current in the delta are unequal while the FC currents in each phase are equal. The delta connected TCRs on the other hand are fired simultaneously and must have the same susceptance because the NS voltage regulator is off i.e. no individual control of the TCRs. Hence, the TCRs see unequal phase voltages which make them to absorb unequal current ($V = \frac{I}{B}$). Therefore, the SVC current which is the subtraction of the TSCs and FC current from the TCRs current must be different in each phase. If the load was symmetrical, the SVC sees equal phase voltages and injects equal phase currents as shown in fig. 4.5.





Fig. 4.4 SVC current, reactive power and TCRs susceptances in case of asymmetrical load

Fig. 4.5 SVC current, PCC voltage and network current in case of symmetrical load

Fig. 4.6 shows the PCC voltage, network and load current where the SVC start at (t = 1s). Fig. 4.7 shows the individual phase PCC voltage in pu and network active and reactive power. The individual phase PCC voltage, active and reactive power are unbalanced and became more unbalanced after the SVC started as shown in fig. 4.7. Because the SVC is injecting unequal PS current in each phase which boosts the individual phase PCC voltage, the voltage unbalance caused by the asymmetrical load would increase after the SVC started. According to fortescue transformation (see 2.5), the magnitude of the PS and the NS voltage must increase when the phase voltages increase. Therefore, the drawback of having an SVC with a PS voltage regulator only in unbalanced network is the higher voltage and current unbalance the SVC causes to the network. This could be eliminated by having an SVC with asymmetrical controller function of the TCRs.



Fig. 4.6 PCC voltage, network and load current

Fig. 4.7 Individual phase PCC voltage, and network active and reactive power

The increase in the voltage and current unbalance that the SVC causes, in unbalance network, depends on the network strength and load type. From a load perspective, fig 4.8 shows the PCC voltage, PCC VUF,

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network IUF and load IUF for different load type. The constant power load causes the highest VUF because the load active and reactive power consumption for constant power load does not vary with the voltage i.e. $\left(\frac{dP}{dV}=0\right)$ and $\left(\frac{dQ}{dV}=0\right)$ while they vary in constant impedance load i.e. $\left(\frac{dP}{dV}=2\right)$ and $\left(\frac{dQ}{dV}=2\right)$.



Fig. 4.8 PCC voltage and VUF, network and load IUF

SVC with a NS voltage regulator only:

In this case, the SVC operates with a NS voltage regulator only while the PS voltage regulator is off. Fig. 4.9 illustrates the SVC current, reactive power and susceptance of each TCR in the delta connection i.e. $(TCR_{ab}, TCR_{bc} \text{ and } TCR_{ca})$ when the SVC operates with NS voltage regulator only. Unlike the previous case, asymmetrical controller is provided by giving a different firing pulse for each TCR, i.e. individual control, while the TSCs are switched on or off if the PS voltage regulator is on only. This will allow the SVC to inject different NS current in each phase which has an opposite angle of the load NS current.



Fig. 4.9 SVC current, reactive power and TCRs susceptances

Fig. 4.10 shows the PCC voltage, network and load current where the SVC start at (t = 1s). Fig. 4.11 shows the individual phase PCC voltage in pu and network active and reactive power. Notice, the SVC with a NS voltage regulator only does not show any voltage improvement at the PCC even though the SVC reduced the NS components in the network caused by the asymmetrical load. This is because that the reactive components of the PS current is dominating the voltage drop in the network impedance. Therefore, eliminating the NS current from the network would not reduce the voltage drop across the network impedance significantly. However, the benefit of operating the SVC with a NS voltage regulator only is illustrated in fig.4.11.

The voltage, active and reactive power for individual phase have a significant gap before the SVC started and moving toward equal values after the SVC stated at (t = 1s). Hence, eliminating the NS components allows fairly equal active and reactive power loading of each phase in the network. The reduction in the PCC VUF and network IUF depends on the network strength and load type.



Fig. 4.10 PCC voltage, network and load current

Fig. 4.11 Individual phase PCC voltage, and network active and reactive power

Fig. 4.12 shows the PCC voltage, PCC VUF, network IUF and load IUF for different load type. Again, the constant power load causes the highest VUF and lowest voltage at the PCC. On the other hand, the load IUF increased while the network IUF decreased after the SVC started. This is because the SVC injects a NS current, with an opposite angle of the load NS current, which circulates with the load NS current so the network NS current and PCC VUF is reduced.



Fig. 4.12 PCC voltage and VUF, network and load IUF

SVC with a PS and a NS voltage regulator:

In this case, the SVC operates with both PS and NS voltage regulators. Fig. 4.13 shows the SVC current, reactive power and susceptance of each TCR in the delta connection. As mentioned previously, the SVC can not control the PS and NS individually and priority is configured for the PS voltage regulator in the SVC controller. This is clearly illustrated in the TCRs susceptance which shows a PS voltage regulator priority. In other words, each TCR should give different susceptance value in order to mitigate the load NS current. However, that would consume the TSCs and FC current to improve the bus voltage. For instance, in order to maximize the NS voltage regulator from the SVC, it should operate in the middle of the TCRs range (similar to fig 4.9 for TCRs susceptance). This is because if the TCRs are close to zero current or low susceptance, there is no much room for the NS voltage regulator. Therefore, reducing the reference voltage less than unity would make higher room for the NS voltage regulator since less TSCs current is needed.



Fig. 4.13 SVC current, reactive power and TCRs susceptances

Fig. 4.14 shows the PCC voltage, network and load current where the SVC start at (t = 1s). Fig. 4.15 shows the individual phase PCC voltage in pu and network active and reactive power. Fig. 4.16 shows the PCC voltage, PCC VUF, network IUF and load IUF for different load type. In this case, the NS voltage regulator is limited to what susceptance is left after the compensation from the PS voltage regulator. Therefore, the reduction in the PCC VUF and network IUF is not significant.



Fig. 4.14 PCC voltage, network and load current

Fig. 4.15 Individual phase PCC voltage, and network active and reactive power



Fig. 4.16 PCC voltage and VUF, network and load IUF

4.3.3 Network strength impact

In the previous tests, only the impact of the load to the SVC response was tested. However, the SVC response to correct the network NS current and the PCC voltage unbalance caused by the asymmetrical load depends on the network strength as well. Using the same asymmetrical load total MVA used in the base case, the impact of the supply system strength is tested for constant power, current, impedance and mixed loads. Fig. 4.17 illustrates the variation of the PCC VUF and network IUF with the network strength for different load types with and without the SVC. For one load type (i.e constant power), the stronger the network i.e. lower impedance ($Z_a^{line} = Z_b^{line} = Z_c^{line}$), the less PCC VUF and higher the network IUF. This is because lower line impedance causes lower voltage drop across it which will result higher voltage at the PCC (see fig 4.18) and less VUF as well. On the other hand, the network IUF is high for stronger network since the network impedance is low.

Comparing different load type, constant power load causes the highest VUF (lowest voltage at the PCC as shown in fig. 4.18) while constant impedance causes the lowest VUF (highest voltage at PCC). The is because constant power load active and reactive power consumption does not vary with the voltage i.e. $\left(\frac{dP}{dV} = 0\right)$ and $\left(\frac{dQ}{dV} = 0\right)$ while they vary in constant impedance load i.e. $\left(\frac{dP}{dV} = 2\right)$ and $\left(\frac{dQ}{dV} = 2\right)$. With the SVC, there is a large gap between the values of VUF at the PCC for different load type in week network (225 MVA). However, the PCC VUF are almost equal in strong network (2250 MVA). The reason is that week network has a very large value of VUF before the SVC started and the SVC is designed with a limitation and deadband of 1% VUF. Hence, the SVC reaches it limit in week network and can not reduce the unbalance any more.



Fig. 4.17 PCC VUF and line IUF variation with the network strength for constant power, current and impedance load with and without the SVC.



Fig. 4.18 PCC voltage varation with the network strength for constant power, current and impedance load with and without the SVC.

In the case of mixed passive load, fig. 4.19 illustrates the PCC voltage and network current phasor digram for different short circuit level of the supply system before and after the energizing of the SVC. Again, the weaker the network strength, the higher the PCC VUF and the lower the network IUF. Additionally, fig. 4.20 shows the NS current phasor of the SVC, load and network after the SVC is energized. The SVC eliminates the NS current in the network caused by the asymmetrical load by injecting a NS current which has an opposite phase of the load NS current. We also can see that the higher the network strength, the easier job for the SVC to mitigate the load NS current.



Fig. 4.19 Voltage and Current phasors at the PCC



Fig. 4.20 SVC, load and PCC NS current phasor

Furthermore, with the same base short circuit level i.e. 700MVA, the value of the network resistance is varied by changing the $(\frac{X}{R})$. The result shows a similar SVC behaviour as in the base case and no significant impact to the VUF and IUF at the PCC as shown in fig 4.21. However, lower resistance causes voltage improvement in the PCC only.



Fig. 4.21 Impact of the $(\frac{X}{R})$ ratio to the VUF, IUF and PCC voltage

4.3.4 Multiple sources of unbalance

In the previous cases, the supply system is assumed to be symmetrical with no contribution to the voltage and current unbalance. In this case, the impact of having unequal network impedance is test. In most standards and grid codes, the supply system should not cause more than 1% continuous VUF at the PCC from untransposed transmission lines. Therefore, untransposed transmission lines usually contribute much less to the voltage unbalance at PCC than the load contribution. However, let's first select their impedance values in such a way that they introduce VUF at the PCC close to the one produced by the load in the base case, i.e. 5.2%, assuming symmetrical source and load. The load total MVA is the same as the base case but equally distributed between the phases.

Fig 4.22 shows the PCC VUF and network IUF for two cases i.e. unbalanced network impedance and unbalanced load and network impedance. In unbalanced network impedance case, the VUF at the PCC and IUF in the network are equal (5%) before the SVC started at (t = 1s). This indicates that the load is symmetrical because a variation of the IUF from the VUF indicates a load impedance variation [39] [38] [40]. After (t = 1s), the SVC reduced the VUF at the PCC while it increases the IUF in the network which propagates toward the source. Therefore, the SVC NS current do not circulate between the SVC and the load, since the load is symmetrical, and injected to the supply system to compensate for the voltage drop across the network impedance, caused by the NS current, in order to lower the voltage unbalance at the PCC.

In case of both unbalanced network impedance and load, the VUF at the PCC consist of both line and load contributions. The SVC was able to reduce both VUF and IUF to 4.8% and 7.8% respectively. However, the SVC could not reach its designed NS voltage deadband i.e. 1% due to the limitation in the TCR susceptance as shown in fig. 4.23. Notice, the susceptance B_{ca} hits zero, and can not go below zero value, which make other susceptance i.e. B_{ab} and B_{bc} to stay at constant values. This means that when one TCR hits zero susceptance, the other TCRs can not reduce the NS current any more.



Fig. 4.22 PCC voltage, network and load current

Fig. 4.23 Individual phase PCC voltage, and network active and reactive power

Fig. 4.24 shows the NS current phasors in the network assuming the current reference in fig 4.3. In the case of unbalanced network impedance only, the network and source NS currents are equal and injected to the symmetrical load. However, they increased after the SVC is energized since the NS current injected by the SVC does not circulate or cancel out with load NS current which is zero. Therefore, the SVC causes higher NS current in the supply system to lower the voltage unbalance at the PCC. In the case of unbalance network impedance and load, the SVC behaves in the same way as the previous base case but with higher NS current since there are two source of unbalance. In other words, the SVC Steinmetz circuit has to balance the load and the network impedance.



Fig. 4.24 SVC, load, PCC and source NS current phasor

4.3.5 Induction machine impact

Due to the negative impact of voltage unbalance to induction machine, the SVC was tested with the present of an industrial load represented by an induction machine which is connected to the PCC through a 220/13.8 kV transformer as shown in the single line digram of fig 4.25. In modelling the induction motor initially, the motor does not start from rest and first is modelled in a steady state speed, close to 1 pu, of (0.96574 pu) in order to reach the steady state speed fast. At (t = 0.1s), the motor is switched from the constant speed mode to the torque mode where the speed is measured based on the mechanical torque, developed electrical torque, inertia and damping according to the mechanical equation given by 4.2a. The mechanical load is set as an 80% of the machine power rating using the load torque characteristics in 4.2b. The machine parameters are illustrated in table 4.3. Since the power rating of the machine impact the voltage unbalance at the PCC, the machine power is varied between 5-70 MVA. The transformer is connected in grounded star in both sides with a power rating between 5-70 MVA, depending on the machine rating, and reactance of 10%.



Fig. 4.25 Single line digram of the network with an industrial load

$$T_e - T_m = J \frac{d\omega_m}{dt} + B\omega_m$$

$$T_m \propto \omega^2$$
(4.2a)
(4.2b)

Table 4.3: Induction machine parameters

	Induction machine
Rated Power	5-70 MVA
Туре	wound rotor
Turns Ratio	0.6 s
Inertia	1.3 s
Mechanical damping	0.005 pu
Stator resistance	0.05 pu
Rotor resistance	0.08 pu
Magnetizing inductance	4.5 pu
Stator leakage inductance	0.1 pu
Rotor leakage inductance	0.1 pu

With 5 MVA induction machine and transformer rating, fig 4.26 and 4.27 shows the machine electrical, mechanical torque and speed when the passive load at the PCC is symmetrical and asymmetrical respectively. The passive load total MVA is the same as in the base case but equally distributed between the phases to make a symmetrical load. The machine is turned to the torque mode at (t = 0.1s) and the speed is measured using 4.2a. Comparing the result of symmetrical and asymmetrical load, the electrical torque has no pulsation or oscillation when the load is symmetrical while it is oscillating when the load is asymmetrical. The torque pulsation is because of the NS current which produces a reverse torque to the PS current torque due to the air gap NS flux which rotates against the PS flux (see 2.8.1). The pulsation in the torque is reduced when the SVC started, at (t = 1s), since the SVC started to eliminate the NS current caused by the asymmetrical load. Also, the slight reduction of the steady state speed when the load is asymmetrical is due to the NS power, caused by the NS current, which would result a reduction in the total PS power of the machine. In other words, the motor will not be able to produce its full torque which would make the motor to behave like a superposition of two separate motors running with two different slips i.e. for PS and NS current (see equation 2.44).



Fig. 4.26 Machine torque and speed with symmetrical load at PCC



Fig. 4.27 Machine torque and speed with asymmetrical load at PCC

Moreover, the machine is now tested starting from rest, before switching to the torque mode at (t = 0.1s), where the speed is measured according to 4.2a. Fig. 4.28 illustrates the torque speed characteristic of the machine, with the present of the passive asymmetrical load, with and without the SVC. Notice the high oscillation on the electrical torque which makes it impossible to define the operating point, i.e. $(T_e = T_m)$, of the machine. However, the installation of the SVC with a NS voltage regulator eliminates the unbalance caused by the asymmetrical load. As a result, the oscillation on the electrical torque is eliminated and the machine operating point is (A) where the speed is (0.92 pu) and $(T_e = T_m = 0.69pu)$. The electrical torque oscillation, with the SVC, at low speeds is due to the start up of the machine and the SVC. The machine keeps acceleration $(T_e > T_m)$ till the steady state operating point (A) is reached where the speed is less than the synchronous speed of 1 pu.



Fig. 4.28 Electrical and mechanical torque Vs speed characteristic

Additionally, fig 4.29 compares the variation of voltage unbalance (at the PCC and induction machine terminal) and current unbalance (at the network and induction machine i.e. (I^{net}) and (I^{IM})) with the power rating of the machine in the present of the base case asymmetrical load at the PCC. It is clearly seen that the higher the rating of the machine, the lower the VUF at the PCC and machine terminal. The same observation also holds for the network and induction machine IUF. Also, the induction machine current unbalance is higher than the network one which means that induction machine draws some of the load NS current and act as a compensator. This is because induction machines consists of passive element i.e. winding inductor which would act as Steinmetz circuit to draw a NS current. Also, the machine tends to attenuate the PCC voltage unbalance as proofed mathematically (see equation 2.24).



Fig. 4.29 VUF and IUF varation with the IM rated power

4.3.6 Transient unbalance

Unlike continuous unbalance caused by either asymmetrical load or unequal network impedance, transient unbalance causes a short term extreme unbalance. Rotating machines, near the unbalanced point, are the most impacted apparatus in the network from transient unbalance. They have a certain short time unbalance capability (see table 2.4). In this case, the SVC is tested against transient unbalance caused by asymmetrical short circuit. The short term unbalance, from short circuit, depends on the fault impedance, location

and type. The fault impedance consists of arc resistance, tower grounding impedance and other objects in the fault path [13]. Assuming no grounding wires and object presence in the fault path, the effective fault impedance is mainly resistive and consists of arc and grounding resistances. Typical fault resistance for 220kV network are between the range of $3 m\Omega$ and 100Ω [13].

A typical fault is a phase to ground with a 100Ω impedance and 10 cycles duration which is applied at (t = 2s) as shown in fig. 4.30. The network current in the faulted phase is extremely high while the PCC voltage and load current are low during the 10 cycle fault duration. During the fault, the PCC VUF, network and load IUF are very high without the SVC (dotted line). In the previous cases, the SVC NS voltage regulator deadband, which is used as reference value for the SVC NS controller, was around 1%. This means that the SVC NS controller acts when only the PCC VUF is higher than 1%. Such a value is a good reference for continuous unbalance while it is very low in transient unbalance. Theretofore, the deadband value is chosen in severe faults, the SVC will introduce instability in the network and might cause worst unbalance. In this case, 10% deadband is chosen which is seen in fig 4.30 where the TCRs susceptance starts to give a different values when the VUF is 10%. Hence, the PCC VUF, network IUF and load IUF are reduced. At (t = 2.2s), the fault is cleared and the TCRs now give one equal susceptance which is the compensation of the FC i.e. the same before the fault is applied.



Fig. 4.30 PCC voltage and its VUF, network current and its IUF, load current and its IUF, SVC current and TCRs susceptance for phase to ground fault with $R_f = 100 \Omega$.

4.4 Unbalance Propagation

The propagation of voltage and current unbalance between different voltage level is studied using the high voltage (220kV), medium voltage (33kV) and low voltage (1kV) networks shown in fig 4.31. Three point of evaluation (POE1, POE2 and POE3) are the point of interest for voltage unbalance. The current (I^{220kV} , I^{33kV} and I^{1kV}) are also in our interest for current unbalance. Load 1, Load 2 and Load 3 have the same total MVA and can be asymmetrical as shown table 4.4 or symmetrical by equally distributing them between the phases. Obviously, it is not realistic to have the same load MVA in different voltage level network. However, the load was selected in such a way that it can be connected to a low, medium and high voltage network. Also, the objective of the test is to observe the variation of voltage and current unbalance between

different network with a fixed load power. The 220 kV source and transmission line are symmetrical and only load contributes to the voltage and current unbalance. Each network has its own short circuit level. The following cases are studied:



Fig. 4.31 Single line digram of 220kV, 33kV and 1kV network

Table 4.4	4: Base	case	data
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Source	Transmission	Load Load 1=Load 2= Load 3
$E_a: 127kV < 0^\circ$	$Z_a^{line} = Z_b^{line} = Z_c^{line}$	A=30 MW+15 MVAR
$E_b: 127kV < 240^\circ$	$S_{sc}^{220kV} = 750, S_{sc}^{33kV} = 550, S_{sc}^{1kV} = 50 MVA$	B=24 MW+12 MVAR
$E_c: 127kV < 120^{\circ}$	$\frac{X}{R} = 10$	C=18 MW+6 MVAR

4.4.1 Asymmetrical high voltage load

In this case, only load 1 is asymmetrical while load 2 and load 3 are symmetrical From fig 4.32, load 1 causes voltage unbalance which propagated from the point of origin i.e. POE 1 to POE 2 and POE 3. The current unbalance in (I^{220kV}) is different than the voltage unbalance at the POE 1. However, the current unbalance in $(I^{33kV} \text{ and } I^{1kV})$ is the same as the voltage unbalance in all POE. From initial assessment point of view of identifying the source of unbalance, it means that load 2 and load 3 in the medium and low voltage networks do not contribute to the unbalance because their VUF and IUF are equal. In another words, the variation of the current unbalance from voltage unbalance indicates a load impedance variation [39] [38] [40]. The SVC installed in the original source of unbalance bus reduce VUF in all points and IUF in all networks.



Fig. 4.32 VUF and IUF in case of asymmetrical load 1

4.4.2 Asymmetrical medium voltage load

In this case, only load 2 is asymmetrical while load 1 and load 3 are symmetrical. From fig 4.33, load 2 in the 33 kV network causes equal voltage unbalance in POE2 and POE3 while it causes significantly lower one in the high voltage network i.e. POE1. Comparing the values of VUF in POE2 and POE2 with the previous case, the same load MVA in the medium voltage network causes much higher VUF i.e. from 2% to 5.5%. This is because of the short circuit power is low in the downstream network compared to highstream network. Even though load 2 MVA is the same as in the previous case (when load 1 was asymmetrical), the voltage unbalance in POE1 and current unbalance in (I^{220kV}) are slightly lower when load 2 is asymmetrical than when load 1 is asymmetrical. This means that asymmetrical load in the downstream network causes lower unbalance in the upstream network than asymmetrical load in the upstream network. However, that depends short circuit power, transformer turn ratio and connection type. The transformer connection type, such as delta connection, reduces the voltage unbalance slightly from one voltage level to another voltage level. Similar to the previous case, notice that the voltage and current unbalance in the low voltage network, i.e. POE3 and I^{1kV} , are equal (i.e. 5.5%) which means that load 3 does not contribute to the unbalance. The SVC is able to reduce only the VUF and IUF in POE1 and the upstream network i.e. 220 kV. The SVC could not reduce the VUF and IUF in downstream network significantly. This is because that the SVC balance local asymmetrical loads only which are connected to the same SVC bus. In other words, the SVC can not balance asymmetrical load connected in different bus than its own bus.



Fig. 4.33 VUF and IUF in case of asymmetrical load 2

4.4.3 Asymmetrical low load

In this case, only load 3 is asymmetrical while load 1 and load 2 are symmetrical and the result is shown in fig 4.34. Similar observation to the previous case (4.4.2), the low voltage asymmetrical load causes lower voltage and current unbalance to the upstream network compare to the previous cases when high voltage and medium voltage loads were asymmetrical. Similarly, the SVC could not reduce the unbalance in other bus than its local bus as in the case of medium voltage asymmetrical load 2. Also, the SVC did not respond to the small unbalance in POE1 because it is below its deadband i.e. 0.5%.



Fig. 4.34 VUF and IUF in case of asymmetrical load 3

4.4.4 Asymmetrical high, medium and low voltage load

In this case, all loads are asymmetrical and fig. 4.35 shows the VUF and IUF. Similarly, the SVC reduces the VUF and IUF in its local bus i.e POE1 and upstream network i.e. 220kV. The VUF reduction in POE2 and POE3 is only the continuation of the unbalance from load 1. The increase in the IUF for (I^{33kV}) after the SVC is because of the NS current injected by the SVC to cancel the unbalance caused by load 1. In other words, the NS current is circulating between the SVC circuit and load 1 which might increase the NS current in the close by downstream network so the upstream network is balanced. Therefore, we conclude that SVC only mitigate local unbalance. Also, asymmetrical load in upstream networks causes higher unbalance to
its own network which propagates to downstream network.



Fig. 4.35 VUF and IUF in case of asymmetrical load 3

4.5 IEEE 14 Bus Network

The IEEE 14 bus test system shown in fig 4.36 is used to test the SVC NS controller for a larger network than the simple network. The transmission lines, transformers, generations and loads data is illustrated in appendix B.1. Without the SVC, the power flow result with symmetrical loads and transmission lines is shown in fig. 4.37 and 4.38. Since there is no source of unbalance, the VUF in each bus and IUF in each line and load are zeros. The total loss in the whole system is 13.53 MW.



Fig. 4.36 Single line digram of IEEE 14 bus test system



Fig. 4.37 Generation and load power flow result



Fig. 4.38 Transmission lines power flow result

4.5.1 Bus 9 unbalance load

In this case, only the load in bus 9 is changed from three phase to a single phase load with the same total MVA. Fig 4.39 and 4.40 shows the power flow result which is not different compare to the previous case with all loads are symmetrical.



Fig. 4.39 Generation and load power flow result



Fig. 4.40 Transmission lines power flow result

Fig. 4.41 illustrates the VUF in each bus and IUF in each line and load. Bus 9 asymmetrical load causes a VU at its bus and other nearby buses linked to it such as 7, 10, and 14. The VU also propagated to other buses such as 4, 5, 11, 12 and 13 but less significant compare to the linked buses to bus 9. Notice that all of the affected buses are load one and generation buses are not affected such as buses 1, 2, 3, 6 and 8. Transmission lines that link the affected buses have a significant IUF as well. Also, small NS current propagated towards other symmetrical loads such as L10, L11, and L14. The total loss in the system is now 14.76 MW which is slightly higher than the previous case with symmetrical loads.



Fig. 4.41 Unbalance voltage and current factors for buses, loads and lines

Fig. 4.42 shows the result for the VUF and IUF after the SVC is energized in bus 9. The VUF in the affected buses and IUF in transmission lines reduced significantly. The total loss in the system with SVC is 11.71 MW which is also slightly lower than the symmetrical loads case and asymmetrical load without the SVC. Similar to the simple network case, reducing the NS current does not show any voltage improvement in each bus in the network since the NS current is not dominant as the PS current.



Fig. 4.42 Unbalance voltage and current factors for buses, loads and lines

4.5.2 Bus 14 unbalance load

In this case, load 9 changed back to three phase load, i.e. symmetrical, and load 14 changed to single phase load. The SVC is still installed in bus 9 to investigate if it is able to reduce the VU from load 14. From fig 4.43, the SVC in bus 9 could not significantly reduces the VUF and IUF caused by load 14 even they are linked by line 9-14. Therefore, the SVC NS controller only mitigate local loads NS current, which are connected to the same SVC bus. Hence, the SVC has to be installed in the same bus where the source of unbalance is generated.



Fig. 4.43 Unbalance voltage and current factors for buses, loads and lines

4.6 Conclusion

The SVC operation or response to balance asymmetrical load depends on load type, network strength and sources of unbalance. From a load type perspective, constant power passive loads cause the worst voltage unbalance at the PCC because their impedance is varied with the input voltage to keep a fixed power. In other words, their active and reactive power slope $\left(\frac{dP}{dV}\right)$ and $\frac{dQ}{dV}$ is zero. From a network perspective, the weaker the network, the higher voltage unbalance at the PCC and vice versa in stronger network. The SVC

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response to correct the PCC voltage unbalance is a trivial in strong network since both the SVC and the network "fight" to eliminate the network NS current and balance the PCC voltage. Hence, it is essential to select a suitable ratio between the network short circuit power and the SVC MVAR rating. In case of multiple sources of unbalance i.e. untransposed network and asymmetrical load, the SVC has to balance the load and the network impedances which causes the SVC to reach it susceptance rating limit.

In most SVC applications, only a PS voltage regulation is provided and it is rarely to have a NS voltage regulation. If the unbalance in the network was extreme or some how above the limitation, the SVC with a PS voltage regulator only causes higher PCC voltage unbalance than the pre-existed value. Thus, it is essential to add a NS voltage regulator in the SVC to avoid such an issue in unbalanced networks. One of the biggest drawbacks of an SVC, with both PS and NS voltage regulators, is the dependency on network voltage. In other words, the SVC susceptance depends on the network voltage and the PS and NS can not be controlled individually. Thus, a compromised solution between the PS and NS regulation is essential.

In the present of three phase induction motor load, the voltage unbalance at the PCC is attenuated depending on the machine rating. NS components cases electrical torque oscillation and speed reduction which makes it impossible to define a constant operating speed where the speed and the torque curves meets. The SVC is able to reduce the NS components from propagating toward the motor load. Additionally, The SVC show a good response in transient unbalance caused by asymmetrical short circuit.

The propagation of voltage and current unbalance from the upstream and downstream networks was tested. The voltage and current unbalance are much higher in the downstream network since they have lower short circuit power. It was shown that the SVC, installed in the upstream network, can not balance asymmetrical load in other downstream networks. Similar result is observed in IEEE 14 bus network, the SVC can only balance asymmetrical load that are connected to the same bus. Hence, the SVC shows local balancing only.

Chapter 5

Conclusions and Future Work

This chapter Summarizes the conclusion and future work of the thesis

5.1 Conclusions

In thesis, a comprehensive evaluation is done for the SVC in load balancing applications. From chapter 2, it is essential in practice to represent unbalanced power system as set of balanced subsystems named PS, NS and ZS components to make easier analysis. Several methods are used to quantify unbalance and the IEC method is the most accurate one. Approximately, 1-3% of VUF is considered and an acceptable level. The voltage and current unbalance are caused by untransposed transmission lines and loads such as railway and arc furnaces. Utilises usually carry out a comprehensive assessment methods to set the standards during the planing phase.

From Chapter 3, a load compensator based on Steinmetz circuit which consist of variable inductors and capacitors can be employed for NS components mitigation. To reach a continuous control of Steinmetz circuit, a bidirectional thyristor valves are used which make up the SVC. In load balancing application, the six-puls TCRs in the SVC topology provides variable shunt susceptance for each phase individually to balance the voltage at the bus. However, the six-puls TSCs are not controlled individually to minimize the transient current. They only switch on if a PS voltage regulation is required. The drawback of the SVC is the dependency on the ac system voltage and inability to control PS and NS components individually. In contrast, VSC injects an inductive and capacitive current independently of the ac system voltage.

From chapter 4, the level of NS components depends on load type, network strength and sources of unbalance. Constant power load causes the highest NS components while constant impedance load causes the lowest one. If a normal SVC wih only PS voltage regulator installed in a bus where asymmetrical load and network exist, it causes worst NS components in the network than the pre existed one. Hence, it is essential to equip the SVC with NS voltage regulator. When mitigating the NS components in nodes where induction motor exist, electrical torques oscillation is reduced significantly and the motor speed stays at constant value. The SVC in general can mitigate NS components caused by a sources connected in the same bus which means that the SVC provides local balancing only.

5.2 Future Work

In the SVC topology used in this thesis i.e. six-puls TCRs and six-puls TSCs, there is no utilization of the TSCs when the SVC operates with a NS voltage regulator only. In other words, the TSCs are only switched when a PS voltage regulation is needed while the TCRs are used to control the phase voltage individually. This will make the individual phase voltage control limited to the TCRs susceptance only. In future work, the controller could be configured to switch the TSCs on if the TCRs reach their limit. Thus, this would make higher "room" for the TCRs which will allow higher NS components elimination.

Chapter 5. Conclusions and Future Work

In this thesis, a simplified model of the load, network thevenin equivalent and induction motor is used which might decrease the precision of the results. For more accurate results, the passive load could be modelled to represent its dynamic behaviour instead of using the static exponential load model implemented in this thesis. Also, modelling the transmission system with accurate untransposed lines makes the estimation of the NS components more realistic.

In future work, a comparison between the SVC and STATCOM is worth simulating for NS components mitigation. This could be done by comparing the results between an SVC and a STATCOM for a certain asymmetrical network and load.

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References

Appendix A

Three Phase System Transformation

A.1 Three Phase Quantities to Vectors Transformation

In this transformation function, a three phase quantities in the (abc) can be transformed into the a space vector representation in the $(\alpha\beta)$ frame. Assuming three phase voltages $(v_a, v_b \text{ and } v_c)$, the space vector $(v_{\alpha\beta})$ is expressed by A.1.

$$v_{\alpha\beta}(t) = v_{\alpha}(t) + jv_{\beta}(t) = A(v_{a}(t) + v_{b}(t)e^{j2\pi/3} + v_{c}(t)e^{j4\pi/3})$$
(A.1)

Where (A) depends on either a power invariant or voltage invariant transformation is needed between the two systems and equal $(\frac{\sqrt{3}}{2})$ and $(\frac{3}{2})$ respectively. The transformation matrix and its inverse are given by A.2 and A.3, assuming power invariant transformation and no zero sequence, respectively.

$$\begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{a} \\ v_{b} \\ v_{c} \end{bmatrix}$$
(A.2)

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}$$
(A.3)

A.2 Fixed to Rotating Coordinate Transformation

The transformation from fixed to rotating coordinate is called park's transformation which is usually used in control system and machines analysis. Rotating coordinate in the dq frame enables the use of DC quantities rather than AC in control integral to remove errors. Beside, it allows us to determine transients easier compared to 50 Hz components. Fig A.1 show the relation between the fixed $\alpha\beta$ frame and the rotating dqframe where the vector v(t) is the one we want to transform. The vector v(t) and the reference vector u(t)rotates, counter-clockwise, with angular frequency of w(t) in the $\alpha\beta$ frame. If the dq frame rotates with the same angular frequency i.e ($w(t) = w_g(t)$), the voltage vector v(t) will be aligned with the d axis i.e $\Delta\theta(t) = 0$. Hence, the voltage vector v(t) seems as a dc quantity in the dq frame. Assuming align reference vector u(t) with the d-axis, the transformation in vector form is expressed by A.4.

$$v_{dq}(t) = v_{\alpha\beta}(t)e^{-j\theta(t)} \tag{A.4}$$

Where $\theta(t)$ is transformation angle and given by A.6

$$\theta(t) = \theta_0 + \int_0^t w_g(\tau) d\tau$$
(A.5)

$$\Delta \theta(t) = \int_{0}^{t} (w(\tau) - w_g(\tau)) d\tau$$
(A.6)

The inverse transformation is expressed by A.11

$$v_{\alpha\beta}(t) = v_{dq}(t)e^{j\theta(t)}$$
(A.7)

Additionally, A.4 and A.11 are given in matrix form in A.8 and A.9 respectively using fig A.1.

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} \cos(-\theta(t)) & -\sin(-\theta(t)) \\ \sin(-\theta)(t) & \cos(-\theta(t)) \end{bmatrix} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix}$$
(A.8)

$$\begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} = \begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) \\ \sin(\theta)(t) & \cos(\theta(t)) \end{bmatrix} \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix}$$
(A.9)



Fig. A.1 $\alpha\beta$ and dq relationship

A.3 Voltage Vectors for Unbalance Three Phase System

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In an arbitrary three phase voltages expressed by A.10, the transformation to $(\alpha\beta)$ and (dq) coordinates is different, compared with the previous methods, if the phase voltage amplitudes are unequal i.e $(\hat{V}_a \neq \hat{V}_b \neq \hat{V}_c)$.

$$v_a(t) = \hat{V}_a \cos(\omega t - \varphi_a) \tag{A.10a}$$

$$v_b(t) = V_b \cos(\omega t - 120 - \varphi_b) \tag{A.10b}$$

$$v_c(t) = \hat{V}_c \cos(\omega t - 240 - \varphi_c) \tag{A.10c}$$

Where ($\omega = 2\pi 50$) and (φ_a , φ_b and φ_c) are the angular frequency and phase displacement taking the PS voltage as a reference. In such a case, the voltage vector in the ($\alpha\beta$) will consist of two vectors, i.e. PS and NS, which rotate in opposite to each other and expressed by.

$$v_{\alpha\beta}(t) = V_1 e^{j(wt+\varphi_1)} + V_2 e^{-j(wt+\varphi_2)}$$
 (A.11)

Where $(V_1 \text{ and } V_2)$ are the amplitudes of the PS and NS voltage vectors with the analogous angles of $(\varphi_1 \text{ snd } \varphi_2)$ respectively. Furthermore, there are two reference frames which can be used when transforming from the fixed $(\alpha\beta)$ coordinate to the rotating (dq) coordinate. They are the PS and NS synchronous reference frames $(dq^+ \text{ and } dq^-)$ which are illustrated in fig A.2. The PS reference frame is rotating in a counterclockwise direction while the NS reference frame is rotating in a clockwise direction.



Fig. A.2 PS and NS synchronous reference frames

Hence, they are represented by the transformation expressed by A.12.

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$$v_{dq^+}(t) = v_{\alpha\beta}(t)e^{-j\theta(t)}$$
(A.12a)

$$v_{dq^-}(t) = v_{\alpha\beta}(t)e^{j\theta(t)}$$
(A.12b)

Therefore, the PS component in (dq^+) reference is seen as a DC value while the NS component is seen as an oscillation with the double fundamental frequency which is given by A.13. The same reasoning also holds for the PS component in the (dq^-) reference frame.

$$v_{dq^+}(t)_2 = e^{-j\theta(t)}e^{-j\theta(t)}v_{dq^+}(t) = e^{2j\theta(t)}v_{dq^+}(t)$$
 (A.13)

Appendix A. Three Phase System Transformation

Appendix B

IEEE 14 bus Data

B.1 IEEE 14 bus network



Fig. B.1 Single line digram of IEEE 14 bus test system

B.2 Transmission Lines and Transformers Data

Table B.1: Shunt capacitor data

Sending	Receiving	Resistance (pu)	Reactance (pu)	Half susceptance (pu)	Transformer tap
1	2	0.01938	0.05917	0.0264	1
2	3	0.04699	0.19797	0.0219	1
2	4	0.05811	0.17632	0.0187	1
1	5	0.05403	0.22304	0.0246	1
2	5	0.05695	0.17388	0.017	1
3	4	0.06701	0.17103	0.0173	1
4	5	0.01335	0.04211	0.0064	1
5	6	0	0.25202	0	0.932
4	7	0	0.20912	0	0.978
7	8	0	0.17615	0	1
4	9	0	0.55618	0	0.969
7	9	0	0.11001	0	1
9	10	0.03181	0.0845	0	1
6	11	0.09498	0.1989	0	1
6	12	0.12291	0.25581	0	1
6	13	0.06615	0.13027	0	1
9	14	0.12711	0.27038	0	1
10	11	0.08205	0.19207	0	1
12	13	0.22092	0.19988	0	1
13	14	0.17093	0.34802	0	1

Table B.2: Line and transformer parameters

Table B.3: Bus voltage, generation and load power

Bus	Voltage ($pu < degree$)	Generation (MW+ MVAR)	Load (MW+MVAR)
1	1.060 < 0	232.66 - j15.86	0
2	1.45 < 0	40.42 + j45.96	21.7 + j12.7
3	1.01 < 0	0 + j25.67	94.2 + j19.1
4	1 < 0	0	47.8 - j3.9
5	1 < 0	0	7.6 + j1.6
6	1 < 0	0 + j20.72	11.2 + j7.5
7	1 < 0	0	0
8	1 < 0	0 + j24.37	0
9	1 < 0	0	29.5 + j16.6
10	1 < 0	0	9 + j5.8
11	1 < 0	0	3.5 + j1.8
12	1 < 0	0	6.1 + j1.6
13	1 < 0	0	13.5 + j5.8
14	1 < 0	0	14.9 + j5