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Design and Analysis of High Voltage to 48V DC-DC Converter Topologies for Automotive Applications

Master's Thesis in Sustainable Electric Power Engineering and Electromobility

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DEPARTMENT OF ELECTRICAL ENGINEERING

CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2024
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Master's thesis 2024

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Master's Thesis report 2024
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Typeset in LaTeX
Printed by Chalmers Reproservice
Gothenburg, Sweden 2024

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Abstract

In automotive applications, below 60V DC operation is considered a low-voltage system, meeting safety protection requirements easily. Compared to current 12V systems, 48V systems increase efficiency by reducing currents, which allows for smaller wire sizes and higher power capability. Though 48V systems provide the abovementioned advantages, it is critical to investigate the impact of various topologies and modulation techniques on DC-DC converter efficiency.
In this thesis work, based on qualitative analysis, the selected topologies are full bridge DC-DC secondary centre tap topology and full bridge DC-DC secondary side full bridge rectifier topology, which were compared with phase shift modulation and duty cycle modulation techniques. The Phase Shifted Full Bridge(PSFB) secondary side full bridge rectifier topology was then chosen to be optimized to evaluate its efficiency to the Dual Active Bridge(DAB) with its chosen modulation approaches based on various modulation comparisons.
From all analyses, the Phase Shifted Full Bridge(PSFB) observes extremely high turn-off voltage oscillations across the MOSFETs on the secondary side, making it impractical to control the oscillations with a snubber and active clamping which makes it weakens the opportunity to further optimize it. As a result, it was decided to stop optimizing the PSFB. Consequently, the focus shifted to the Dual Active Bridge (DAB), which demonstrated better performance under varying loads. Operating under Extended Phase Shift Modulation(EPS) from 3750W to 1000W, it achieved an average efficiency of 92 %. Below 1000W, the implementation of Triangular Current Modulation(TRG) further improved efficiency to an average of 94 %. This performance made the DAB a more viable and efficient solution for the intended application, justifying its selection over the PSFB. While the DAB's performance is promising and can be optimized further, concerns remain regarding high RMS and peak currents, which may result in significant copper loss in the circuit and Printed Circuit Board (PCB), and unreliable soft switching. The key limitation for high RMS and peak currents is a large input voltage range, leading to a lower turns ratio for the 48V application.

Keywords: Dual Active Bridge, Extended Phase Shift, Phase Shift Full Bridge, Triangular Current Modulation, Snubber, Active Clamp, transformer, switch, Zero Voltage Switching, efficiency.

Acknowledgements

My deepest gratitude goes out to everyone who helped and advised me while I accomplished this report.

First and foremost, I would like to sincerely thank Yujing Liu, my university examiner, for his insightful feedback, thorough assessment, and helpful recommendations. Their expertise and guidance have been crucial for enhancing and completing this work.

I owe an immense amount of gratitude to Ustun Saglam and Rajiv Augustine, my supervisors at Volvo Cars, for their unwavering assistance, wise counsel, and inspiration during the project. Their expert advice and useful insights have been extremely helpful in determining the course and conclusion of this research.

I would like to express my gratitude to all of my colleagues and friends, especially Narender Rao, Vasanth Ramesh, and Srikanth Yedehalli Lakshmeesha, for their encouragement, constructive discussions, and teamwork-oriented attitude during our work together.

My sincere gratitude is extended to my family for their constant assistance, compassion, and inspiration during our journey. Their confidence in my skills has always been a source of inspiration.

I sincerely appreciate all of your incredible support and encouragement.

Brihadeshvaran Arumugam, Gothenburg, August 2024

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

HV	High Voltage
LV	Low Voltage
PSFB	Phase Shifted Full Bridge
ZVS	Zero Voltage Switching
DAB	Dual Active Bridge
SPS	Single Phase Shift
EPS	Extended Phase Shift
DPS	Dual Phase Shift
TPS	Triple Phase Shift
TRP	Trapezoidal Current Modulation
TRG	Triangular Current Modulation
ESR	Equivalent Series Resistance
ZCS	Zero Current Switching
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation

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Introduction

1.1 Background

Usually the traditional way in the automotive industry is power conversion of High Voltage which ranges at 800V-400V supplied from battery source is step down to 12 V to auxiliary supply in the vehicle. Due to recent demand to increase power requirement ,voltage system is shifting from 12V to 48 V to increase the power capability. By increasing the auxiliary voltage system to 48V,there is a reduction in load current, which in turn reduces the weight of the wire in the system and copper losses in Printed Circuit Board(PCB). Thus it enhances by giving more room to increase the power capability and efficiency in the system. To change the voltage system to 48V, investigation and evaluation of selected toplogies are examined through PSpice and LTSpice simulations to create an efficient 48V converter .

1.2 Aim

Design and Analysis of DC-DC Converter Topologies from HV to LV 48V application

1.3 Methodology

There are many considerations to be take into account when designing DC/DC converters for 48V applications that convert high voltage (HV) to low voltage (LV). This includes topology selection, circuit design calculations and loss calculation of each component in the converter. For efficiency optimization, critical evaluations of control strategies and pulse width modulation (PWM) approaches are essential. Precise circuit models ,simulations facilitate performance evaluation, to ensure the converter meets real world requirements.In the context of 48V systems, this comprehensive approach combines simulation studies, experimental verification, and theoretical calculations to produce an effective and dependable power conversion solution.

1.4 Objectives

- Investigate and select DC/DC converter topologies that satisfies the particular needs of the 48V application.

- To make sure the converter satisfies performance requirements, undertake accurate circuit design calculations for selected topologies.
- Analyze PWM techniques and control strategies to maximize efficiency
- Develop precise circuit models and conduct simulations for performance evaluation.
- Investigate and chart MOSFET power losses to comprehend and reduce dissipation of energy.
- Balance conflicting design objectives with Pareto optimization.
- For an efficient power conversion solution, include theoretical calculations, and simulation studies.

1.5 Problem Description

The thesis begins with a comparison and investigation of different topologies for higher power capability and efficiency in 48V applications. From qualitative analysis, the selected topologies are Full Bridge Secondary Centre Tap Converter, Full Bridge-Secondary Side Full Bridge Rectifier Converter, and Dual Active Bridge Converter. First, design and evaluation is done for the full-bridge secondary centre tap DC-DC converter for duty cycle control and phase shift control. Based on the MOSFET losses of both modulation technique, we chose one type of modulation technique which has lower losses to implement in Full Bridge DC-DC Converter Secondary side Full Bridge Rectifier topology. Then both Secondary Centre tap and Full bridge rectifier topologies are compared with switch losses for different load conditions. Based on the comparison, one topology is taken into consideration for optimization to meet all requirements and make a detailed loss analysis, including core losses i.e., transformer,leakage inductance and output filter inductance. This ends the first part of the thesis. The second part begins with a Dual Active Bridge(DAB), where different modulation techniques are compared for investigating the lowest RMS and Peak currents among all modulation techniques. Based on the comparison, we choose one or two modulation techniques for different load ranges, specifically two modulation techniques for two different load ranges to improve the topology efficiency. Based on the selected modulation techniques, a detailed loss analysis is made after meeting all requirements.The first and second part topologies are compared, and conclusions are formed to provide a comprehensive picture of the comparisons with thesis conclusion.

2

Theory

Different topologies are investigated in order to achieve improved power capability and efficiency in 48V applications. To understand different topologies, we study various literature,

2.1 Full bridge with Secondary Centre Tap Converter

So, we begin evaluating with the full bridge secondary bridge centre tap topology with duty cycle control and phase shift modulation .

2.1.1 Duty Cycle Control

Firstly, looking into the duty cycle control, from [1], there are 4 switches in primary, where T1 and T2 acts as one pair and T3 and T4 acts as another pair. The two pairs are switched alternately with varying duty cycle less than 50% at switching frequencies. When the both switches are off .The inductor current freewheels in the secondary side through the two diodes D1 and D2. At this period , assuming ideal diodes, then the voltage across primary transformer is 0, where inductor voltage during this period is,

$$V_L = -V_o \quad for \quad t_{on} < t < t_{on} + \Delta \tag{2.1}$$

When integrating the average voltage across the inductor over one time period gives duty ratio as,

$$D = 2\frac{N_1.V_o}{V_{in}.N_2} \tag{2.2}$$

where $\frac{N1}{N2}$ is turns ratio ,V_{in} is input voltage,t_{on} is turn on time of the switch and V_o is output voltage.

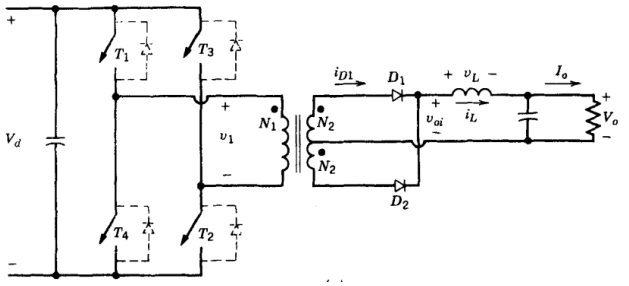

Figure 2.1: Full Bridge Secondary Tap Circuit[1]

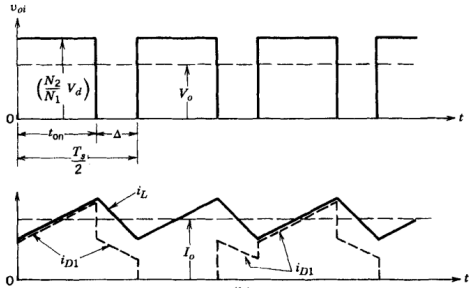

Figure 2.2: Waveforms of Voltage across Primary and Inductor[1]

2.1.2 Phase Shift Control

When compared with duty cycle control, both diagonal switches are switched with 50% duty cycle minus a small dead time.In phase shift control,the diagonal switches are controlled by phase shift, i.e., a deliberate delay is created between the two diagonal switches. As mentioned in [2], the principal components used in the phase shift technique are the output capacitance C_{oss} of the switch and the internal diode of the switch, where resonant transitions can be taken place and commutated. In this paper, the basic circuit shown in figure 3 comprises four switches Q_A,Q_B,Q_C and Q_D along with their shunted parasitic output capacitance and internal body diode.

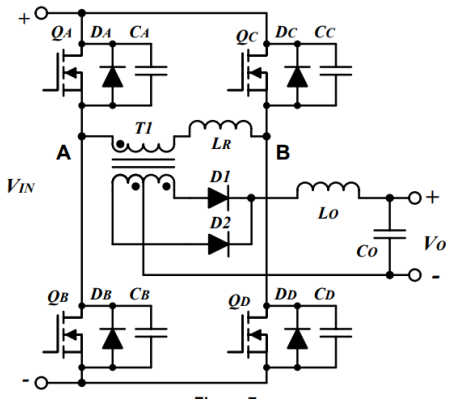

Figure 2.3: Phase Shift Full Bridge Secondary Tap Circuit[2]

We start first with the power transfer mode. During this mode, the diagonal switches are Q_A and Q_D and power is transferred to the load through the transformer.
After power transfer mode, right leg transition mode happens in figure 5, where the Q_D turns off, its shunt parasitic capacitance C_D starts charging, and the shunt parasitic capacitance of C_C starts discharging. L_R in the circuit is chosen in such a way that the inductive energy is greater than the capacitive energy during the given transition time because the inductance energy is stored when the secondary current is clamped when the primary voltage is zero. This in turn causes high circulating currents and has no effect on stored energy to perform zero voltage switching (ZVS).

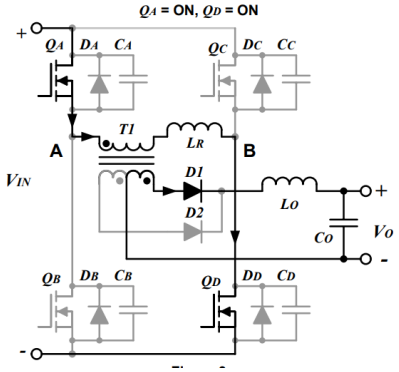

Figure 2.4: Power Transfer Mode[2]

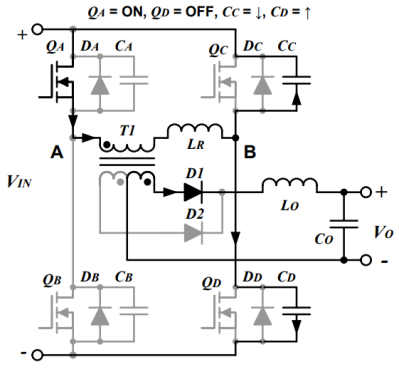

Figure 2.5: Right Leg Transition[2]

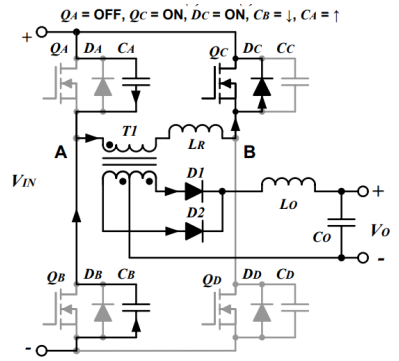

Figure 2.6: Left Leg Transition[2]

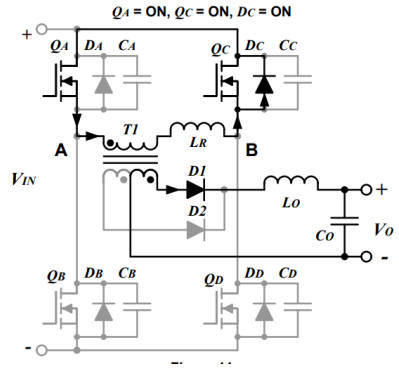

Figure 2.7: Freewheeling Mode(Zero Voltage Switching)[2]

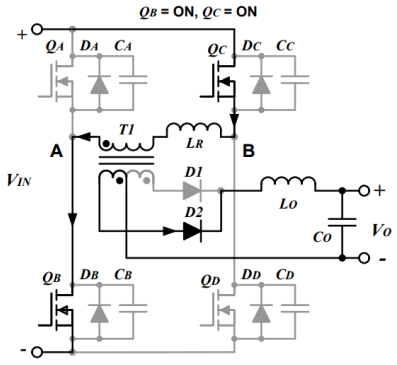

Figure 2.8: Power Transfer Mode[2]

When the right leg transition happens, the primary current is constant freewheels in the opposite direction from switch Q_A to internal diode D_C. Once switch Q_C is on, the current divides through the internal diode D_C and switch Q_C.During this freewheeling, zero-voltage switching is achieved. In this process, both D_1 and D_2 are conducted.
Furthermore, when switch Q_A is turned off, the parasitic capacitor of Q_B starts discharging, and the parasitic capacitor of switch Q_A starts charging. Once the C_A gets charged and the C_B gets discharged, current continues to flow through the internal diode D_B until the switch Q_B is on and the switch Q_C. When Q_B and Q_C are on, power transfer conversion happens, and only D_2 starts conducting, and the process continues.

2.2 Full bridge with Current Doubler

A current doubler rectifier with synchronous rectification is optimal because it divides the output current between two filter inductors, lowering conduction losses, improving thermal management, and providing ripple cancellation for improved performance[3].

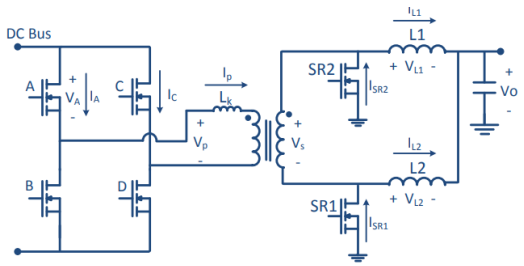

Figure 2.9: Phase Shift Current Doubler Rectifier Circuit[3]

With the mosfet control,it operates similar to Phase Shift Full Bridge Secondary Centre Tap phase shift modulation. Mode 1: Duty Cycle Loss Mode: The output receives no power. Up until the primary current switches direction, both secondary side rectifiers conduct current with zero secondary voltage.

Mode 2: Power Delivery Mode: The secondary voltage of the transformer is equal to the input voltage times the turns ratio. While the other discharges, the output inductor charges. The reflected output inductor current is equal to the primary winding current.

Mode 3: Switch C ZVS Mode: The main current charges the capacitance of switch D and discharges the capacitance of switch C. Switch C's body diode conducts when the secondary voltage drops in order to achieve zero voltage switching.

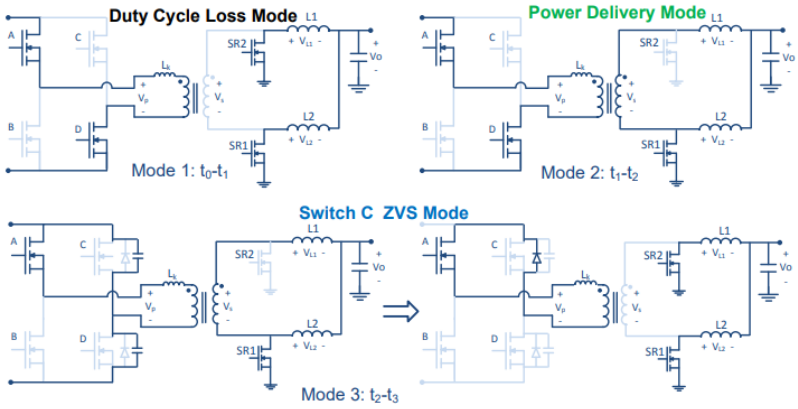

Figure 2.10: Circuit Working from Mode 4 to 7[3]

Mode 4: Freewheeling Mode: Switches A and C allow the primary current to freely flow. There is no secondary voltage on the transformer. Through the corresponding secondary side rectifiers, the output inductor discharges. Mode 5: B Switch ZVS Mode: The primary current charges the capacitance of switch A and discharges the capacitance of switch B. Switch B's body diode conducts to provide switching at zero voltage. There is no secondary voltage.
Mode 6: Duty Cycle Loss Mode: The output receives no power. Up until the primary current switches direction, both secondary side rectifiers conduct current with zero secondary voltage.
Mode 7: Power Delivery Mode: The secondary voltage of the transformer is equal to the input voltage times the turns ratio. While the other discharges, the output inductor charges. The reflected output inductor current is equal to the primary current.

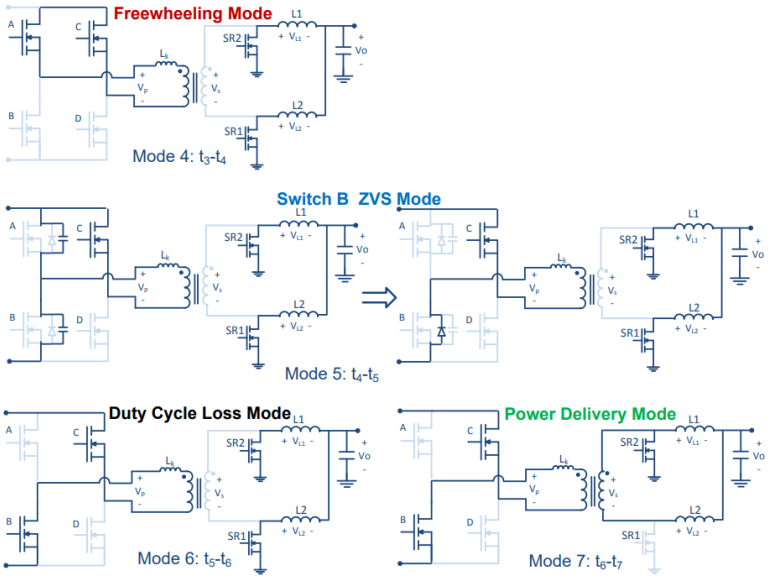

Figure 2.11: Phase Shift Current Doubler Rectifier working mode 8 to 10[3]

Mode 8: Press D ZVS Mode: The primary current charges the capacitance of switch C and discharges the capacitance of switch D. Switch D's body diode conducts when the secondary voltage drops in order to achieve zero voltage switching. Mode9: Freewheeling Mode: Switches B and D allow the primary current to freely flow. There is no secondary voltage on the transformer. Through the corresponding secondary side rectifiers, the output inductor discharges.
Mode 10: Press A ZVS Mode: The primary current charges the capacitance of switch B and discharges the capacitance of switch A. Switch A's body diode conducts to produce switching at zero voltage. There is no secondary voltage.

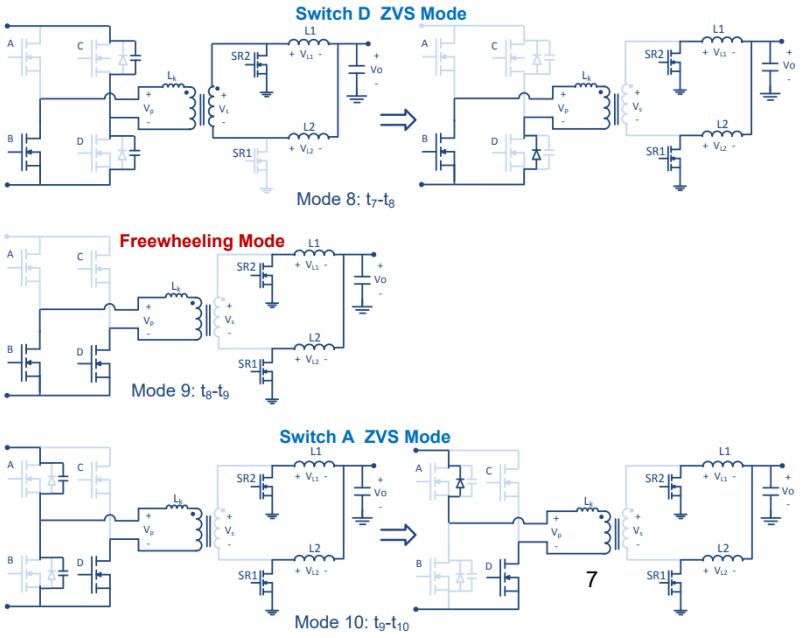

Figure 2.12: Phase Shift Technique Circuit[3]

2.3 Zero Voltage Switching (ZVS)

Between one leg ,there is a dead time between the two mosfets where both switches are off and zero voltage is clamped in the primary side by the resonant circuit [2] .Instead of turning on the switch instantly the primary current circulates shorted through the body diodes parallel to the switches until the switces are turned on .The purpose of this off-time is to close the voltage gap that exists between the moment at which the switch must turn on to achieve constant frequency operation and zero voltage. The main restriction of the varible frequency zero voltage switching is between the lowest output load and maximum output current .

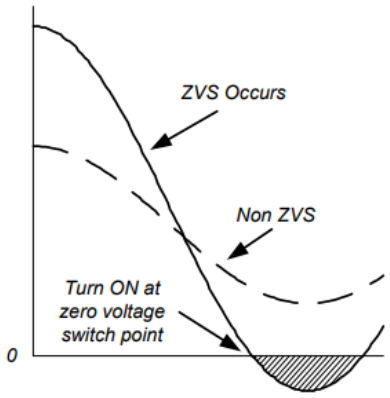

Figure 2.13: Zero Voltage Switching Range[2]

2.4 Active Clamping

Typical current-fed converters have a high-voltage spike on the MOSFETs when they switch off, which is a significant disadvantage. A passive lossy snubber across the FET is necessary for this. Further changes to the topology aid in recovering some of the energy lost in the snubber during turnoff, which increases system efficiency. An example of such a change is called the active clamp[14].

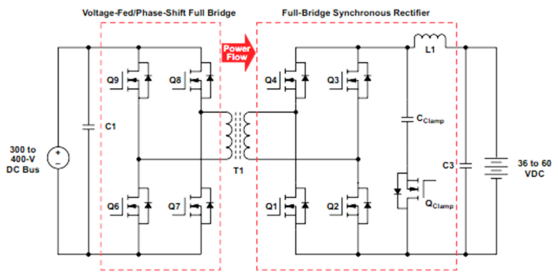

Figure 2.14: Voltage-Fed Phase Shift Full Bridge Circuit with Active Clamp[14]

A MOSFET connected in series with a clamp capacitor makes up the active clamp. By directing the current through the MOSFET and into the clamp circuit when it shuts off, it contains the voltage spike on the low-voltage MOSFET during turn off. Furthermore, just before to the low-voltage MOSFETs turning on, the active-clamp circuit applies a ZVS condition, which lowers the turn-on losses.

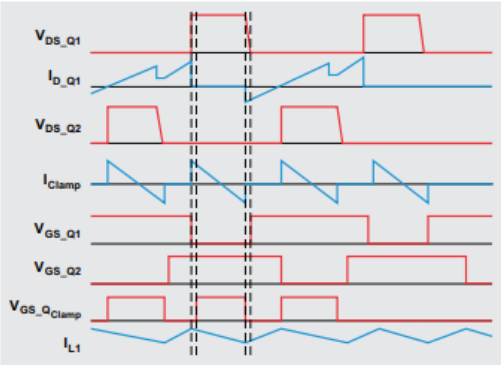

Figure 2.15: Waveforms for Voltage-Fed Phase Shift Full Bridge Circuit with Active Clamp[14]

2.5 Dual Active Bridge

The power transfer in a dual active bridge (DAB) is compared to power system power system where phase difference is required between the two sources i.e., Primary to Secondary or vice versa for active power flow.The power System equation is given below:

$$P = \frac{V_p.V_s}{X} sin(\delta) \tag{2.3}$$

where P is the Active Power ,V_p is the voltage across the primary side,V_s is the voltage across the secondary side,X is the reactance of the line and δ is phase difference between the two source. From [20],basic circuit diagram of the dual active bridge can be seen in figure 3 and waveforms of circuit in figure . All the switches are operated at 50% where the primary and secondary are operated simulationelously but with a phase shift in gate drives between primary(Q1,Q2,Q3,Q4) and secondary(Q5,Q6,Q7,Q8) switches which can be seen in the figure 3.

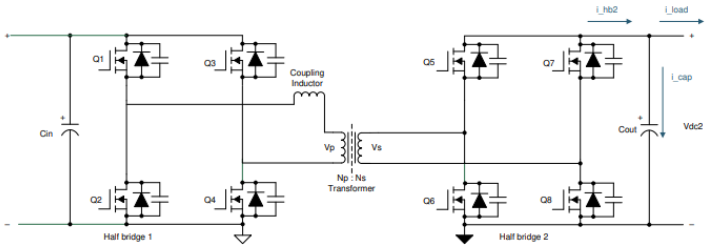

Figure 2.16: Dual Active Bridge Circuit [20]

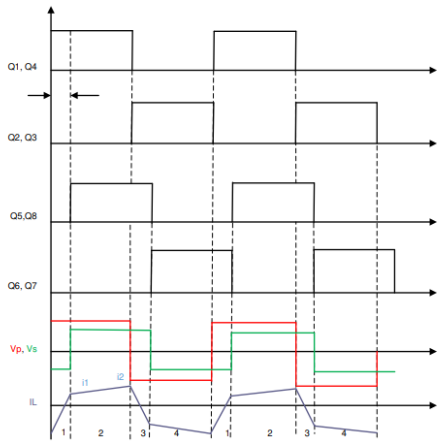

Figure 2.17: Waveform of Voltage across Primary and Inductor[20]

During Interval 1 ,the direction of inductor current is negative and positive .When the inductor current is negative, there is voltage difference across the leakage inductance ,the slope of the current is,

$$\frac{di}{dt} = \frac{Vin + Vo}{L} \tag{2.4}$$

The primary side of transformer and secondary side of voltage transformer is positive.So the rate of increase in current in interval 2 is,

$$\frac{di}{dt} = \frac{Vin - Vo}{L} \tag{2.5}$$

2.5.1 Overview of Modulation Techniques

2.5.1.1 Single Phase Shift Modulation (SPS)

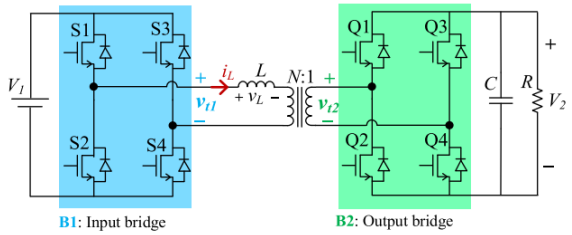

Figure 2.18: Dual Active Bridge Circuit highlighting Primary and Secondary bridge[10]

The function and overview of single phase shift(SPS) (figure 2.18) modulation technique is discussed above with waveform of gate signals, primary and secondary voltage waveform and leakage inductance current waveform in figure 2.19. The max Power that can be transmitted in SPS is given,

$$P_{max,SPS} = \frac{N.V_{in}.V_o}{8.L.f_s} \tag{2.6}$$

Therefore,the transmitted power and the peak current value is given by,

$$I_{P,SPS} = \frac{V_{in} - NV_o(1-2\phi)}{4Lf_s} \tag{2.7}$$

$$P_{SPS} = \frac{V_{in}NV_o\phi(1-\phi)}{2Lf_s} \tag{2.8}$$

The Power flows in negative direction when the Secondary side Voltage leads the Primary Side.

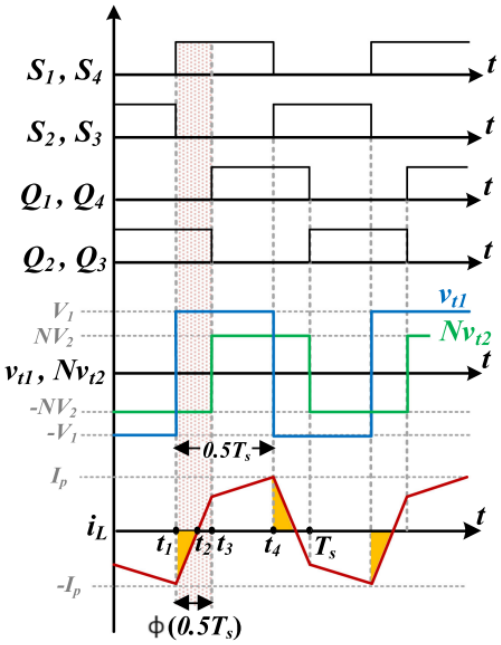

Figure 2.19: Single Phase Modulation Waveform[10]

2.5.1.2 Extended Phase Shift Modulation (EPS)

V_{prim} and V_{sec}, in contrast to the SPS control, use the EPS approach to include three voltage levels.The waveforms of V_{prim},V_{sec},I_L,and the gate signals in the EPS modulation are depicted in Figure 2, where α_p represents the relative inner phase shift[10]. The phase difference between the gate signals of two legs of a single bridge is denoted by α_p. It's important to note that the bridge with a higher equivalent voltage often uses α_p.For example, the inner shift is applied to B2's gate signals if NVo is greater than Vin.The waveforms for EPS can be seen in figure 2.20[10].

$$P_{EPS} = \frac{NV_{in}V_{out}}{4Lf_{sw}}[\alpha(1-\alpha-2\phi)+2\phi(1-\phi))] \tag{2.9}$$

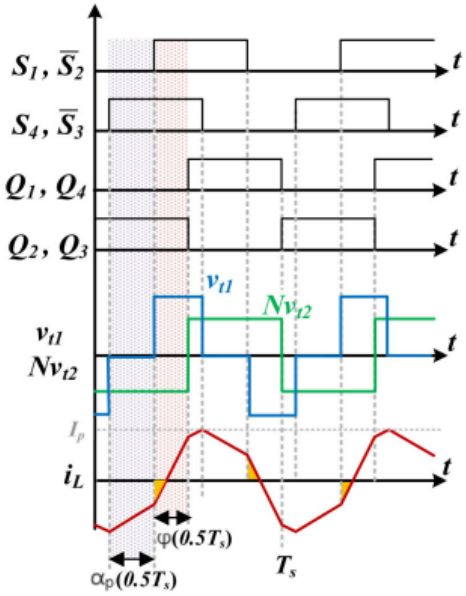

Figure 2.20: Extended Phase Shift waveforms[10]

2.5.1.3 Dual Phase Shift Modulation (DPS)

The extended phase shift technique differs from the dual phase shift (DPS) approach in that both bridges have zero voltage range. The DPS method is comparable to the EPS method[10]. There is no difference in the phase-shift ratio between primary and secondary. Consequently, the two control variables (ϕ and α_p) are the phase-shift ratios, just like in the EPS approach. Similar to the extended phase shift approach, the DPS may achieve zero voltage switching over a broad working range while decreasing the circulation current and reactive power figure 2.21 .

$$P_{EPS} = \frac{NV_{in}V_{out}}{2Lf_{sw}} \times \left\{ \left[\phi(1 - \alpha_p - \tfrac{\phi}{2}) \right], \quad \phi < \alpha_p \right. \tag{2.10}$$

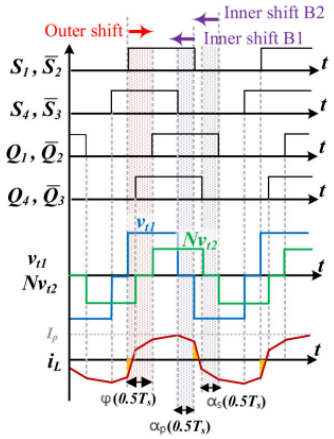

Figure 2.21: Dual Phase Shift waveforms [10]

2.5.1.4 Triple Phase Shift Modulation(TPS)

TPS is another alternate modulation technique for previous DPS , there is an interval where the voltage is zero in both inverters, similar to the DPS method. Unlike the DPS method, the phase-shift ratios in the primary and secondary can be different[10]. Therefore, in the TPS method, there are three control variables, phase shift ratios (ϕ, α_p and α_s), are used in figure 2.22. In this method, current stress, conduction and other losses are at the lowest level compared to other methods. In addition, the widest operating range of zero voltage switching is provided by this method. Since the output voltage and the transferred power are controlled by three variables, the control is more complex than other methods

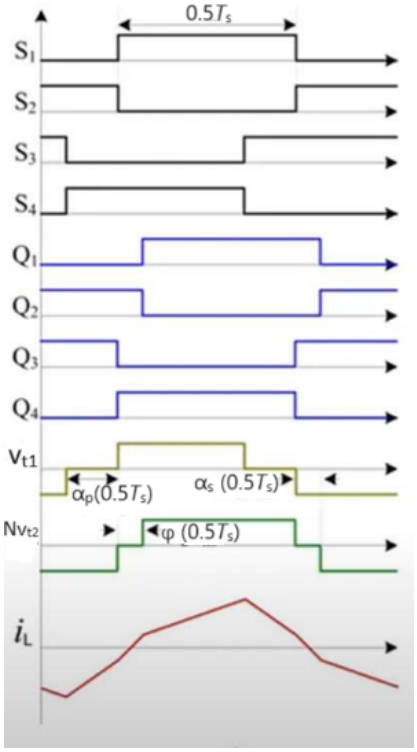

Figure 2.22: Triple Phase Shift waveform [10]

2.5.1.5 Trapezoidal Current Modulation (TRP)

Although TRG and TRP share several notable characteristics, the two approaches differ in terms of power range and number of soft-switched transitions[10]. Of the sixteen total, TRP offers eight ZCS transitions and four ZVS turn-ons. In TRP, there are theoretically four hard switching transitions—that is, two more than in TRG.The typical waveforms of vt1, vt2, and i_L in the marginal TRP are shown in Figure 2.23.

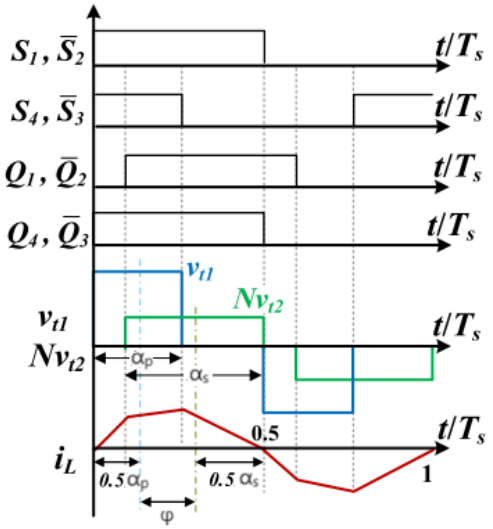

Figure 2.23: Trapezoidal Current Modulation waveform [10]

2.5.1.6 Triangular Current Modulation (TRG)

Of all the modulation techniques now in use, triangle modulation (TRG) offers the lowest switching loss. The term comes from the triangular form of the leakage inductor current (i_L in Figure 2.22) that results from using this modulation technique[10]. Zero-current switching (ZCS) is used for six turn-off instants and soft switching at all turn-on moments in the TRG approach.Nevertheless, TRG has certain shortcomings, including excessive reactive power and poor power transmission capability.

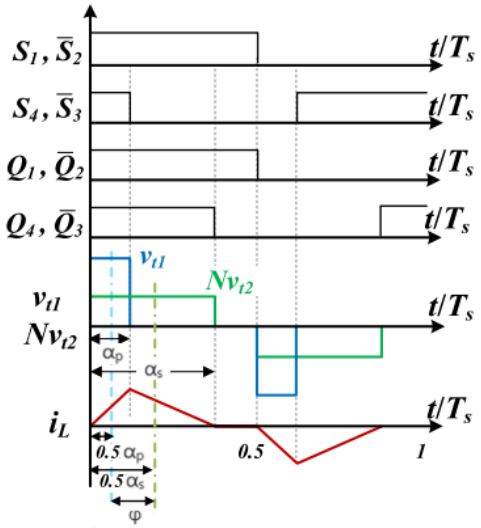

Figure 2.24: Trianagular Current Modulation waveform [10]

3

Full Bridge DC DC Converter

3.1 Design Considerations

In order to achieve efficient converter ,we need to keep in mind the selecting electrical components based on voltage rating,current rating , and Power dissipated in the device with reference to [3] and [4].

3.1.1 Full Bridge DC DC Secondary Tap Converter

3.1.1.1 Transfomer Calculation

We select turns ratio(n) of the transformer based on full load maximum duty cycle from 0.9 to a lower value based on dead time consideration and duty cycle loss in the system especillay in the Phase shift modulation .

$$n = \frac{V_{inmin}.D_{max}}{V_{out}} \tag{3.1}$$

where n is turns ratio,lower input voltage is V_{inmin},maximum full load duty cycle ratio is D_{max} and output voltage is V_{out}.
To calculate the minimum full load duty cycle for maximum voltage

$$D_{min} = \frac{V_{out} * n}{V_{inmax}} \tag{3.2}$$

where D_{min} is minimum full load duty cycle and V_{inmax} is maximum input voltage .
To calculate the maximum full load duty cycle for maximum voltage ,

$$D_{max} = \frac{V_{out} * n}{V_{inmin}} \tag{3.3}$$

RMS Currents and the transformer peak currents to be calculated with the requirement of ΔI_{LOUT} is , We estimate the current ripple percent from output voltage ripple

$$\Delta I_{LOUT} = \frac{I_{Load} - I_L}{I_L} = \frac{\frac{P_o}{V_{out}} - \frac{P_o}{V_{out}+V_{ripple}}}{\frac{P_o}{V_{out}}} \tag{3.4}$$

where ΔI_{LOUT} is filter inductor ripple current ,I_{Load} is output current,$I_L$is inductor current,V_{ripple} is output voltage ripple and P_o is output power.
To operate the converter in the voltage mode control , the L_m must be less than

the calculated value .If selected inductance more the L_m then it will operate in peak current control mode.

$$L_m \leq \frac{V_{in}(1 - D_{max})}{\frac{\Delta I_{LOUT} * 0.5}{n} * f_{sw}} \tag{3.5}$$

The peak magnetic flux density of the transformer is ,

$$B_m = \frac{L_m \Delta I_m}{2nAe} \tag{3.6}$$

Peak Secondary Current

$$I_{ps} = \frac{P_{out}}{V_{out}} + \frac{\Delta I_{LOUT}}{2} \tag{3.7}$$

RMS Secondary Current

$$I_{srms} = \frac{I_{ps}}{\sqrt{2}} \tag{3.8}$$

Peak Primary Current

$$I_{pp} = \frac{I_{ps}}{n} \tag{3.9}$$

RMS Primary Current

$$I_{prms} = \frac{I_{pp}}{n} \tag{3.10}$$

where B_m is peak magnetic flux density,Ae is area of the core,L_m is magnetizing Inductance,f_{sw} is switching ,frequency,I_{ps} is peak secondary transformer current,I_{srms} is rms secondary transformer current,I_{pp} is primary transformer peak current,I_{prms} is rms primary transformer current and ΔI_m peak magnetizing Inductor current.

3.1.1.2 Selection of Leakage Inductance L_r

Calculating the resonant inductance is based on the amount of energy required to achieve zero voltage switching. At the switch node, this inductor must be able to drain the energy from the parasitic capacitance. We calculate L_r for different loads for the worst-case scenario. The values for different L_r are shown under the results section. The main criteria is to drain the capacitance energy from inductor energy.

$$L_r.(\frac{I_{pp}}{2} - \frac{\Delta I_{LOUT}}{2})^2 \geq \frac{(4 * C_{oss}) * V_{inmin}^2}{2} \tag{3.11}$$

where C_{oss} is parasitic output capacitance of the primary mosfet .
We select L_r in lighter load such that it satisfy the ZVS in heavier load and making sure that it duty cycle is not greater than 1 for heavier load.

$$L_r. \geq \frac{(2 * C_{oss}) * V_{inmin}^2}{(\frac{I_{pp}}{2} - \frac{\Delta I_{LOUT}}{2})^2} \tag{3.12}$$

3.1.1.3 Selection Output Filter

L_{OUT},

$$L_{out} = \frac{(\frac{V_{inmin}}{n} - V_{out}) * t_{on}}{\Delta I_{Lout}} \tag{3.13}$$

C_{OUT},

$$C_{out} = \frac{(\Delta V_{out} * t_{on})}{\Delta I_{Lout}} \tag{3.14}$$

ESR of C_{OUT}

$$ESR_{cout} = \frac{\Delta V_{out}}{I_{out}} \tag{3.15}$$

Resonant frequency,

$$f_r = \frac{1}{2 * \pi * \sqrt{L_{out} * C_{out}}} \tag{3.16}$$

Equating Eq (3.15) keeping $L_{OUT} = 10\mu H$ to compute the output capacitance. where t_{on} is the turning on time,ESR_{cout} is the Equivalent series resistance of output capacitance and $f_r$is the resonant frequency.

3.1.1.4 Duty Cycle loss

$$\Delta D = Dutyloss = \frac{2 * I_{out} * Lr_{ZVS} * f_{sw}}{n.^2 * V_{inmin}} \tag{3.17}$$

3.1.1.5 Dead time

$$Deadtime = \frac{\pi.\sqrt{L_r(2.C_{oss})}}{2} \tag{3.18}$$

3.1.1.6 Total Duty Cycle

$$TotalDuty = D_{max} + \Delta D + 2.(deadtime) \leq 1 \tag{3.19}$$

3.1.1.7 Voltage Stress on Secondary Mosfets

For the Full bridge DC-DC Secondary Centre Tap Converter the Voltage Stress on the Secondary Side Mosfet Mosfets are,

$$V_{ds_QA} \geq \frac{2V_{inmax}}{n} \tag{3.20}$$

For the Full bridge DC-DC Converter the Voltage Stress on the Secondary Side Mosfet are,

$$V_{ds_QA} \geq \frac{V_{inmax}}{n} \tag{3.21}$$

3.2 Converter Specifications

Requirements	DC/DC converter (48V)
HVDC Input Voltage Range	180V-450V (Cont. Transient)
Continuous Power	3kW continuous
Transient Power	3.75kW transient @ 1.5 seconds

Table 3.1: Basic Requirements for the Converter

3.3 Full Bridge Secondary tap

3.3.1 Circuit Design

3.3.1.1 Selection of Turns Ratio and Leakage Inductance

Keeping Eq.(3.19), the full load Duty Cycle must not exceed the ratio 1. We select a turn ratio below or equal to the minimum input voltage V_{inmin} to satisfy the converter requirement on wide input voltage range. As a result, the selection of turns ratio is ranged between two and three. The maximum duty cycle is calculated for various load conditions, and the required leakage inductance is calculated to achieve ZVS for each load.

For Turns Ratio n=3		
Power Range	Min. Lr Required (uH)	Maximum Duty Cycle
3000	5.42	0.9586
2000	8.124	0.9612
1000	16.248	0.9671
750	21.66	0.9702
500	32	0.9754
400	40.6	0.98
200	81	0.9918
100	162	1.0104

Table 3.2: Required Leakage Inductance for Different Load ranges

For n=3 for Lr=16.248uH	
Power Range	Maximum Duty Cycle
3000	1.0597
2000	1.0126
1000	0.9656

Table 3.3: Leakage Inductance calculated at 1000W for turns ratio of 3

We can observe from table 3.3, that the total duty cycle crosses more than 1 for the nominal load, when Lr is calculated at 1000W. So it is not possible to have 16.248uH as leakage inductance. Table 3.2 also shows that leakage inductance calculated with a 3000W load can reduce the full load duty cycle ratio to less than one, but there is little room for transient. Therefore, achieving $Vinmin$ would be extremely challenging. Tables 3.5 and 3.2 show that with less inductance, more ZVS may be

n=3 for 8.124uH	
Power Range	Maximum Duty Cycle
3000	0.9837
2000	0.9602

Table 3.4: Leakage inductance calculated at 1000W at turns ratio of 3

covered across a wider load range than with a turn ratio of 2. One of the reasons for selecting turns ratio 2 is that there is a low duty cycle loss when selecting inductance based on higher power load.

Power Range	Lr min. req
3000	0.02uH
2000	0.0591uH
1000	0.23uH
750	0.42uH
500	0.946uH
400	1.478uH
200	5.9uH
100	23.656uH

Table 3.5: Turns Ratio=2

For Turns Ratio n=2 for chosen inductance 4uH		
Power Range	Maximum Duty Cycle	Duty Cycle Loss
3750	0.7079	0.0977
3000	0.6922	0.0781
2000	0.6622	0.0521
1000	0.6401	0.0260
750	0.6336	0.0195
500	0.6271	0.0130
400	0.6245	0.0104
200	0.6248	0.0077

Table 3.6: Selected Inductance and respective Duty Cycle Loss for each Load

So based on Eq.(3.11), We select the required Leakage Inductance of 4uH for the

turns ratio of 2. There will be certain changes in the value of Leakage Inductance due to manufacturer in-built models in PSpice.

3.3.1.2 Initial Design Table

Since achieving ZVS for light load to heavy load for turns ratio of 3 is less. The ZVS range is investigated for a turns ratio of 2 under different load conditions in order to achieve less switching loss and thus improve efficiency. Based on this selection of turns ratio, designing the parameters of the converter is done. The designed parameters of the converter for phase shifted converter is the below table 3.7,

Side	Parameter	Value
Secondary Side	Output Current (A)	62.5
	Output Ripple Current(A)	1.2
	Peak Current in Secondary(A)	62.6628
	Rms Current(A)	44.197
Primary Side	Peak Current(A)	31.33
	Rms Current(A)	22.15
	Leakage Inductance(H)	4.28μ
	Magnetizing Inductance(H)	700μ
Output Filter	Output Inductor(H)	10u
	Min. Output Capacitance(F)	391μ
	Electrostatic Resistance(Ω	4m
	Capacitance rms Current(A)	0.1897

Table 3.7: Initial Design for Phase Shifted Full Bridge Converter

Primary and Secondary Switch Parameters	
Parameter	Value
SiC MOSFET	SCT040HU65G3AG
V_{ds}	650V
I_d	30A
R_{dson}	40mOhm
V_{gsth}	4.2V
C_{iss}(Input Capacitance)	920pF
C_{oss}(Output Capacitance)	94pF
C_{rss}(Reverse transfer Capacitance)	13pF

Table 3.8: Primary and Secondary MOSFET Details

The below figure 3.1 is PSpice Ciruit Model .

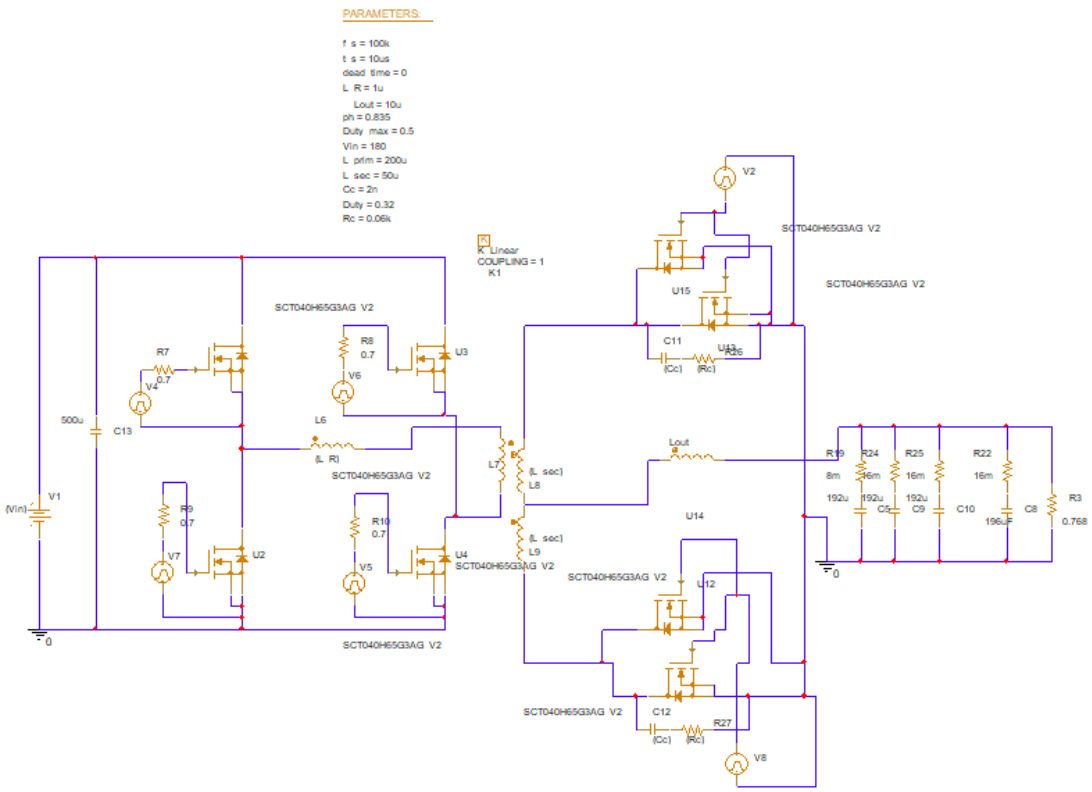

Figure 3.1: PSpice Circuit for Full bridge Secondary Centre Tap

3.3.2 Analysis

First analysis for different loads to check ZVS is done as mentioned in Table 3.9 with designed leakage inductance. Further, analysis is started for Phase-shifted modulation DC-DC Converter secondary centre tap topology to estimate MOSFET losses.
The first task is to check the designed the leakage inductance meets the Zero voltage switching for the required load range. The Duty Cycle ratios mentioned in Table 3.9 are for lower input voltage 180V, since achieving the 48V output voltage for lower range input voltage is always a challenge due effect of Duty cycle loss from the MOSFETs which contributes to the total duty cycle loss.

		0.2<Duty Cycle<0.84		
For Turns Ratio n=2				
Power Range	R_load(ohm)	ZVS	Duty Cycle	
			Simulation	Theoretical
3750	0,6144	Yes	0.93	0.7079
3000	0,768	Yes	0.84	0.6922
2000	1,152	Yes	0.75	0.6622
1000	2,304	Yes	0.64	0.6401
750	3,072	Yes	0.63	0.6336
500	4,608	Yes	0.619	0.6271
400	5,76	Yes	0.6	0.6245
200	11,52	No	0.6	0.6248
100	23,04	No	0.6	0.6128

Table 3.9: Zero Voltage Switching for different load conditions

3.3.2.1 Phase Shift Modulation

The worst-case analysis is taken into simulation by considering the lowest and highest input voltage. For 180V and 450V as Input Voltage considered as worst case, three different load ranges is simulated in PSpice to calculate the total MOSFET lossess in the topology. Based on the MOSFET losses, comparison of modulation techniques between phase shift modulation and duty cycle modulation is done and selection of the best modulation technique is used for the full bridge converter secondary side full bridge rectifier. Further, comparison of secondary side Full bridge rectifier and secondary centre tap converter with the same modulation technique is done to identify better performing topology. Based on this analysis, optimization is performed, and a detailed loss analysis of each component in the circuit is performed to produce a near-to-practical converter, which includes losses in the snubber, active clamp, transformer core and inductor cores. Then, compare it to the DAB topology to determine which topology is more efficient.
The Figures 3.2 to 3.7 below are the MOSFET loss graphs for different loads i.e., 3000W,1500W and 100W loads for two extreme voltages to keep worst case possible in mind.

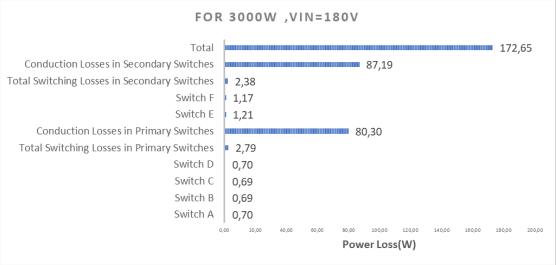

Figure 3.2: For Po=3000W,Vin=180V

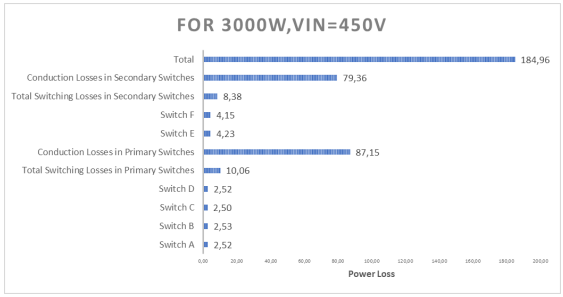

Figure 3.3: For Po=3000W,Vin=450V

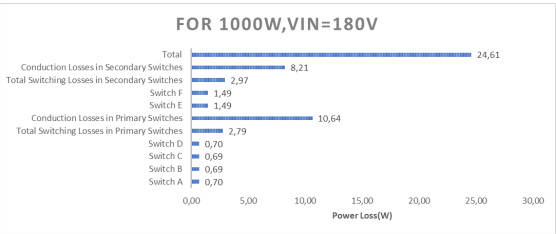

Figure 3.4: For Po=1000W,Vin=180V

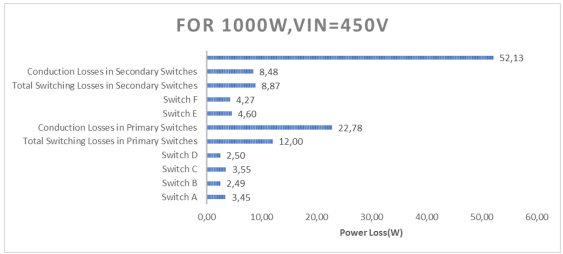

Figure 3.5: For Po=1000W,Vin=450V

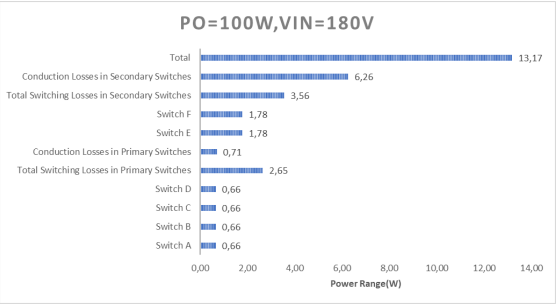

Figure 3.6: For Po=100W,Vin=180V

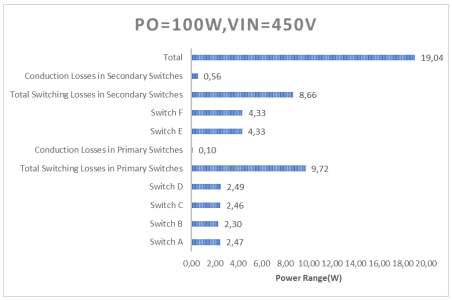

Figure 3.7: For Po=100W,Vin=450V

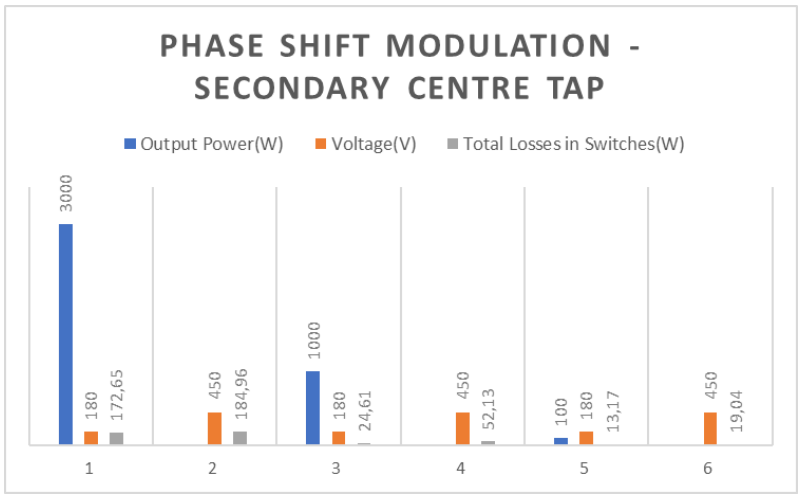

Figure 3.8: MOSFET Loss Graph for Full bridge Secondary Tap-Duty Cycle Modulation

Figure 3.8 shows that as the load decreases, the MOSFET losses continue to decrease. However, it's too soon to make a comment on this. When the Duty Cycle Modulation technique's MOSFET loss is completed, a good comparison of the top modulation techniques with respect to low MOSFET losses can be made.

3.3.2.2 Duty Cycle Modulation

Duty cycle modulation will be performed in Secondary centre tap topology is done similar to that of phase shift modulation technique in figures 3.9 to 3.13. For Po=100W and V_{inmax} i.e., 450V ,simulation in PSpice crashes before it reaches steady state .That is why above mentioned operating point observation is not taken.

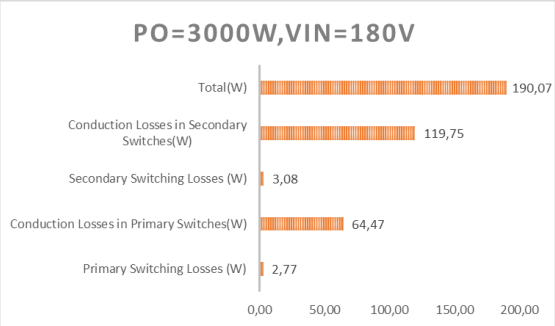

Figure 3.9: For Po=3000W,Vin=450V

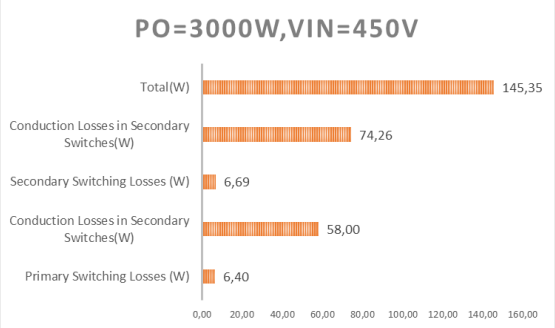

Figure 3.10: For Po=3000W,Vin=180V

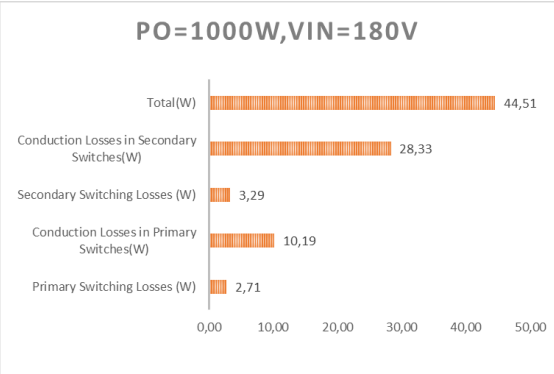

Figure 3.11: For Po=1000W,Vin=180V

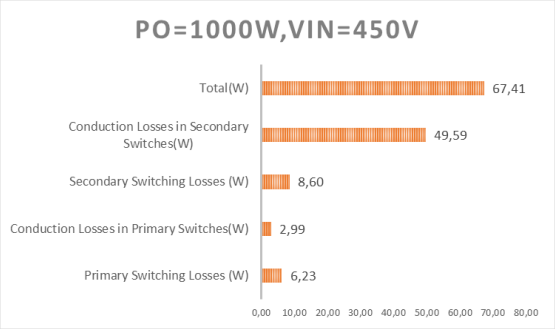

Figure 3.12: For Po=1000W,Vin=450V

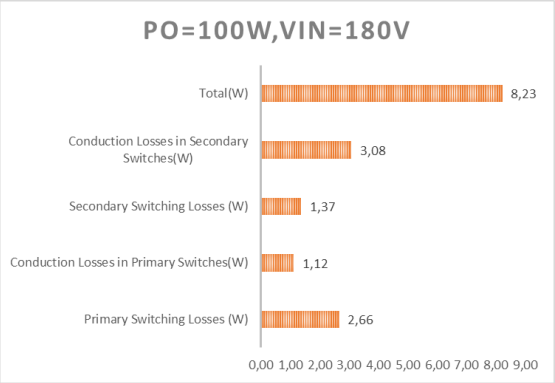

Figure 3.13: For Po=100W,Vin=180V

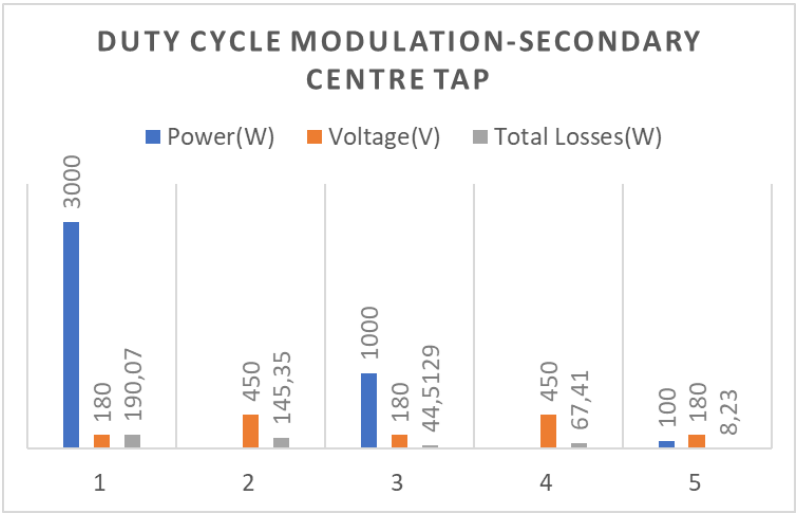

Figure 3.14: MOSFET Loss Graph for Full bridge Secondary Tap-Duty Cycle Modulation

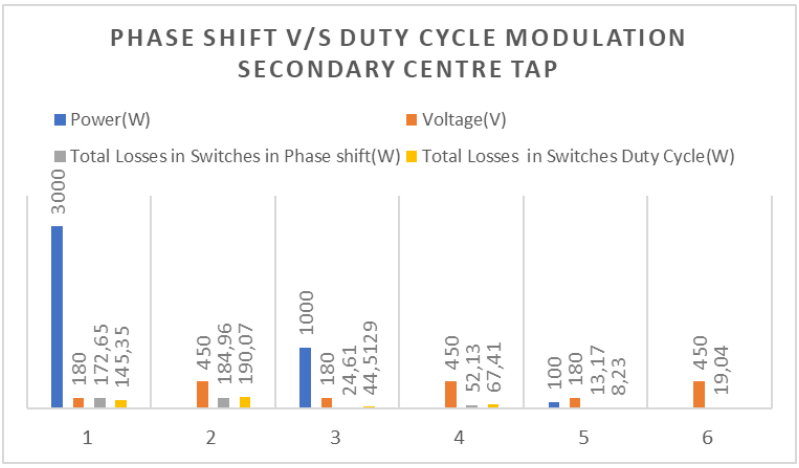

Figure 3.15: MOSFET Loss Graph for Full bridge Secondary Centre Tap-Phase Shift v/s Duty Cycle Modulation

Figure 3.15 shows that the Phase Shift Modulation technique has lower average losses across all load conditions than the Duty Cycle Modulation technique. This advances the performance of the Phase shift modulation technique over Duty Cycle modulation, allowing us to choose it for secondary side full bridge rectifier topology.

3.4 Full Bridge-Secondary side Full bridge Rectifier

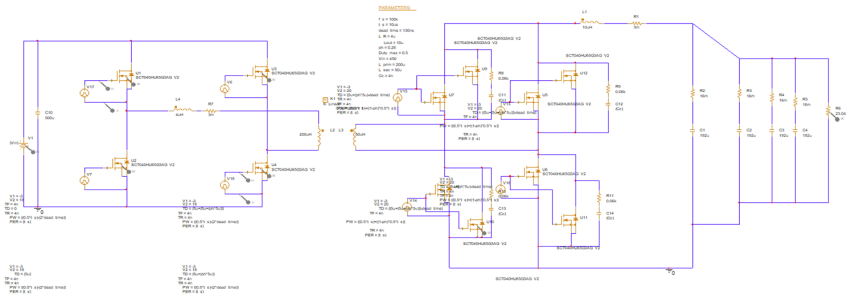

Figure 3.16: Full Bridge Secondary Side Full Bridge Rectifier Circuit PSpice Model

Phase shift modulation is implemented in secondary side full bridge rectifier. To compare the MOSFET losses of both topologies, the same observations are made as with the center tap in a full bridge rectifier which can seen in figure 3.17 - 3.22.

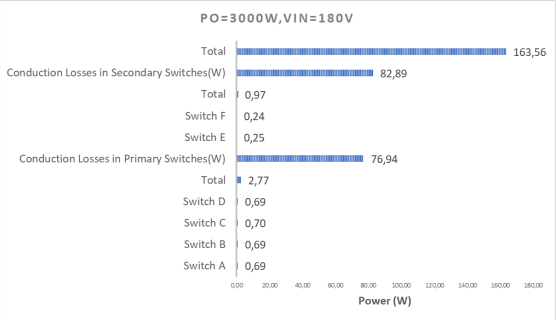

Figure 3.17: For Po=3000W,Vin=180V

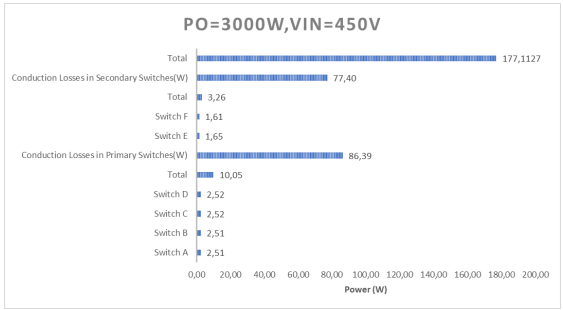

Figure 3.18: For Po=3000W,Vin=450V

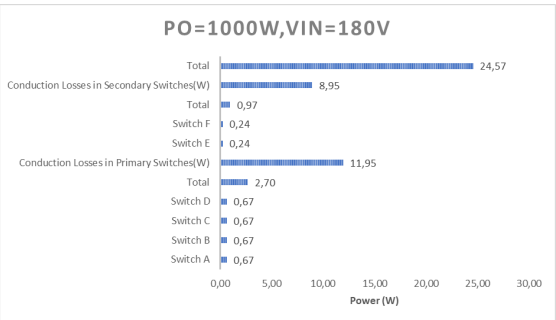

Figure 3.19: For Po=1000W,Vin=180V

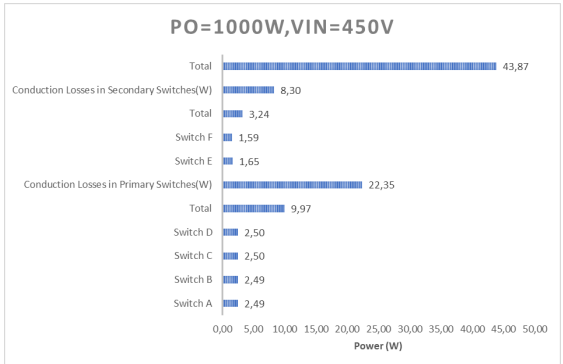

Figure 3.20: For Po=1000W,Vin=450V

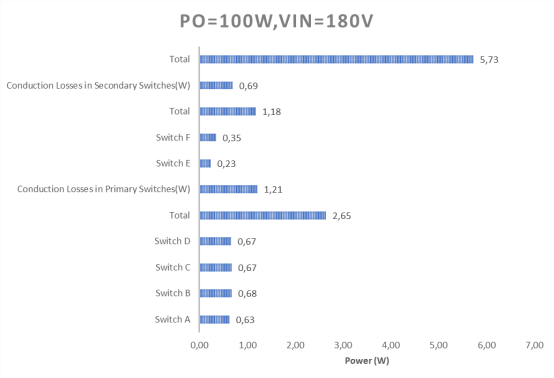

Figure 3.21: For Po=100W,Vin=180V

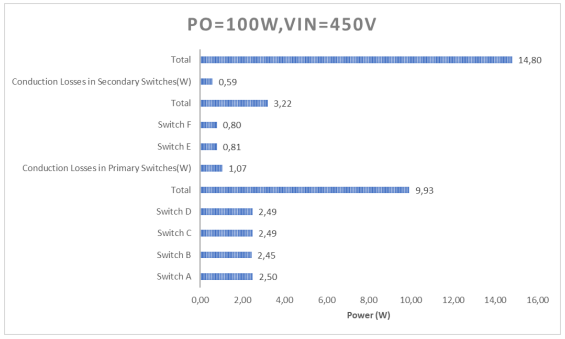

Figure 3.22: For Po=100W,Vin=450V

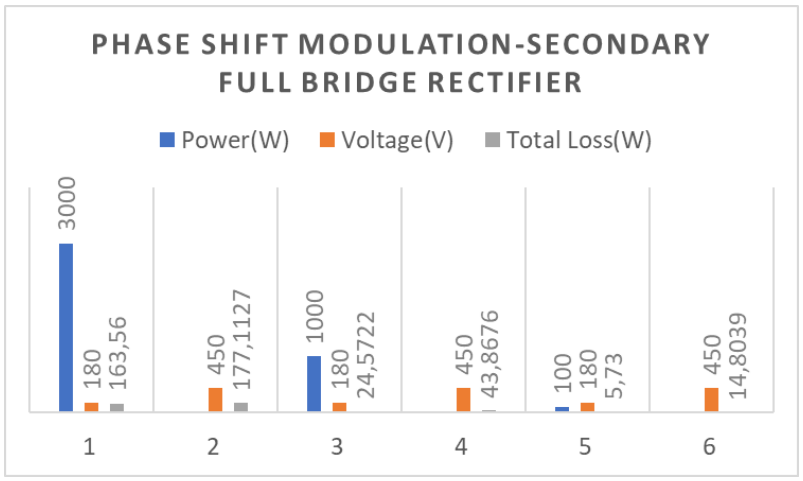

Figure 3.23: MOSFET Loss Graph for Full bridge Secondary Full Bridge Rectifier-Phase Shift Modulation

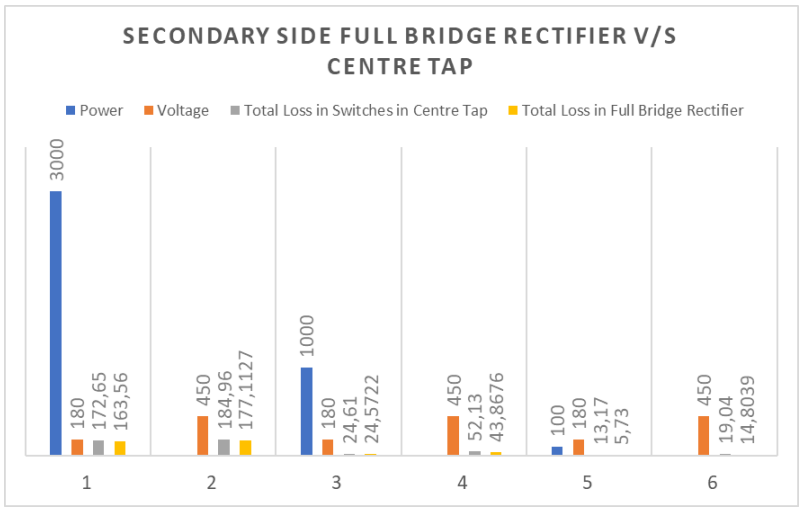

Figure 3.24: MOSFET Loss Graph for Full bridge Secondary Centre Tap v/s Full Bridge Rectifier

According to the MOSFET loss graph in Figure 3.24, the secondary side full bridge rectifier has a lower average loss across all load conditions than the secondary centre tap topology. Since we discovered the secondary side full bridge rectifier topology with lower MOSFET losses, we chose this topology for further optimization to improve the circuit in terms of reducing secondary side voltage stress by increasing the transformer's turn ratio and performing a detailed loss analysis on each circuit component.

3.5 Optimized Full Bridge Converter

Here, we start to optimise the full bridge circuit by:

- Tune the turns ratio from 2 to 3.5. The main reason for choosing the 3.5 turns ratio is to reduce the voltage stress on the secondary side.
- Choose a 150V MOSFET with a lower $R_{DS(on)}$, which means the on-state resistance of the MOSFET can reduce the conduction loss on the secondary side.
- With the increase in the turns ratio, the input voltage range reduces from 180V - 450V to 210V - 450V, as shown in Table 3.27.
- Increasing the turns ratio will reduce the currents in the primary side which in turn reduces the conduction losses in the primary side without changing the MOSFET in the primary side.

Secondary Switch Parameters	
Parameter	Value
Si MOSFET	SQM85N15-19
V_{ds}	150V
I_d	85A
R_{dson}	19mOhm
V_{gsth}	3.5V
C_{iss}(Input Capacitance)	6285pF
C_{oss}(Output Capacitance)	565pF
C_{rss}(Reverse transfer Capacitance)	270pF

Table 3.10: Secondary MOSFET Details

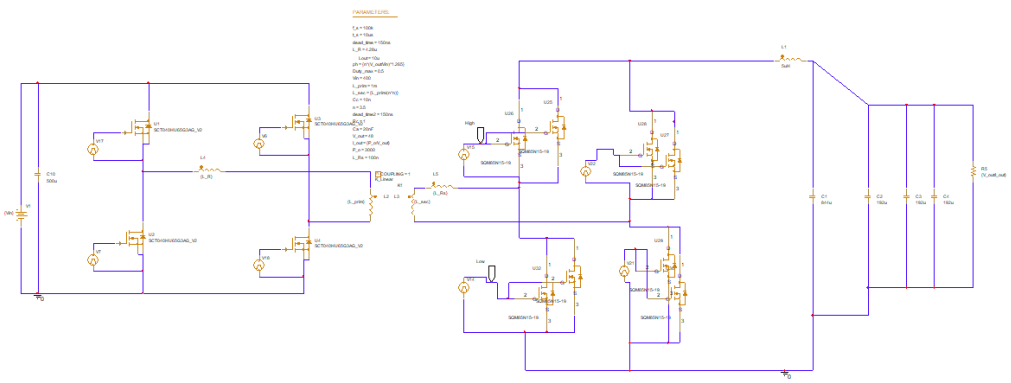

Figure 3.25: PSFB with only Snubber

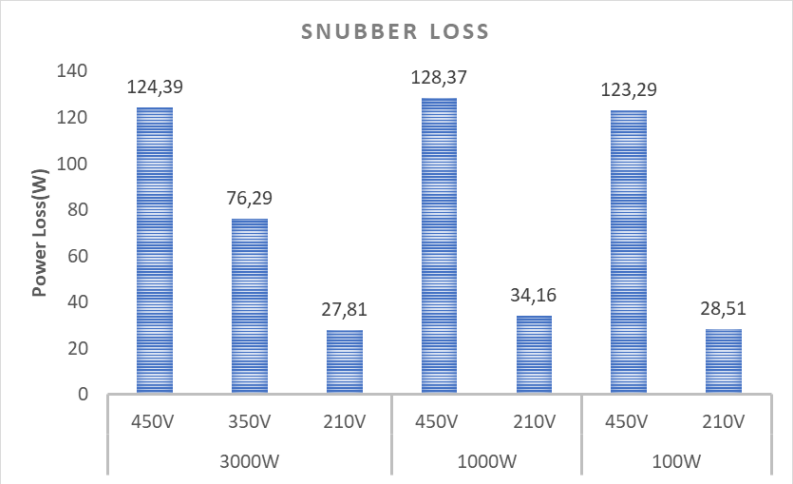

Figure 3.26: Snubber Loss Graph for Optmized PSFB

From the this optimized circuit the key takes are :
Snubber is the primary cause of the high loss, which reduces efficiency due to high oscillations in the secondary side MOSFETs during turn-off. Figure 3.26 shows how much it takes to reduce oscillations or ringing in the MOSFET using the snubber circuit. The figure shows that snubber losses are very significant (124W for four switches), equating to 31W per snubber per MOSFET, which is extremely high and impractical to implement in the real world.A snubber should typically be up to one watt or less. So it's like 54 times the loss, which is unrealistic and necessitates a larger cooling system to reduce heat from the snubber. Later, active clamping and snubber were implemented to reduce the ringing to implement more realistic circuit which can be seen the figure 3.27. The advantage of using active clamping is to reduce the resistive loss from snubber and reuse the energy from the capacitor across the active clamp.
Now, a circuit with active clamping and a snubber is implemented to reduce ringing and create a more realistic circuit, as shown in Figure 3.27. The advantage of active clamping is that it reduces resistive loss from the snubber while reusing energy from the capacitor across the active clamp.

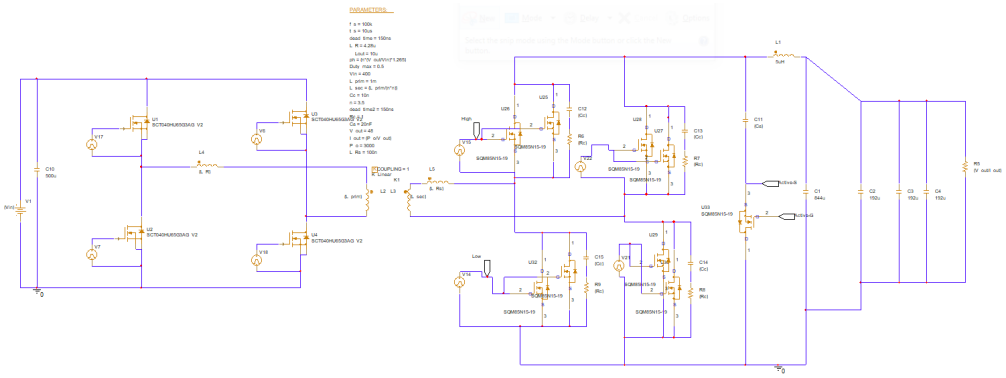

Figure 3.27: PSFB with Snubber and Active Clamping

Furthermore, in PSpice, the ringing is not as expected, as the ringing is clamped

at 150V before the introduction of Snubber and Active Clamp, which occurs due to PSpice's in-built model and does not occur in a practical scenario. The ringing did not decrease as expected after introducing a combination of active clamp and snubber circuit. We conclude our analysis of the full bridge converter topology because optimizing the circuit for a 48V application is unrealistic. We then conduct a thorough analysis of Dual Active Bridge.

4

Dual Active Bridge

4.1 Design Considerations

4.1.1 Selection of Turns of Ratio

Turns ratio n is selected to satisfy the output voltage for the required minimum input voltage range[10] ,

$$Vin = n * V_{out} \tag{4.1}$$

4.1.2 Recognizing the Phase Shift Range

We try to keep the maximum outer Phase Shift between the Primary bridge and Secondary bridge to be 0.4 and the minimum to be 0.1 which is 72° to 18° while keeping 0.1 for extra room for not considering component losses in converter. However, it is not possible to achieve with Single Phase modulation technique for wide voltage and power range. That is the reason why we explore all possible modulation techniques to satisfy the converter for the required converter[10].

4.1.3 Leakage Inductance Lr

Basic requirement for designing the Leakage Inductance from Single Phase Shift (SPS) modulation is,

$$Lr < \frac{nV_{out}V_{in}}{2.P_{max}.f_{sw}}. \tag{4.2}$$

4.2 Modulation Comparison

The selection of modulation technique for Dual Active Bridge (DAB) was to be verified. Initially, the chosen turn ratio was 3.5. So, using the modulation techniques discussed above in Theory, we consider four operating points and compare all modulation techniques in LTSpice to an ideal switch. The reason for switching from PSPice to LTspice is to improve simulation speed. This allows for a faster selection of modulation techniques. Later, the 3.5 turns ratio was changed to a turns ratio 3 because, for triangular modulation, the slope of the leakage inductance current changes when it comes to 180V input voltage. Because the secondary side referred input voltage is 51.5V, the slope reduces and causes a lesser slope for the triangular waveform. As a result, the turns ratio is decrease to three, which can help to

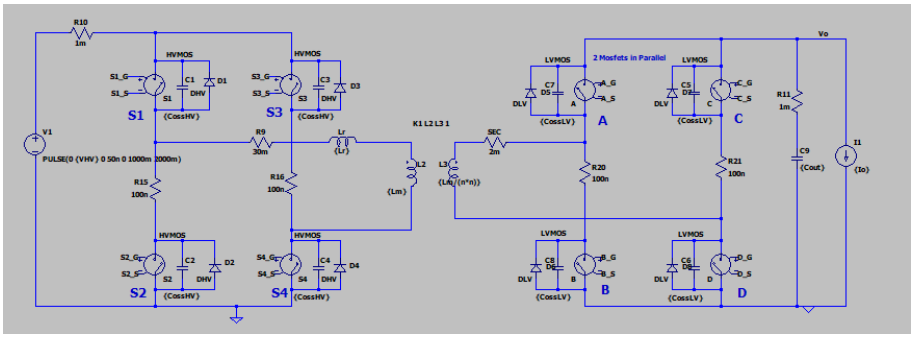

Figure 4.1: LTSpice-Ideal Circuit Model

reduce the leakage inductance value. As a result, a more accurate waveform will be obtained.

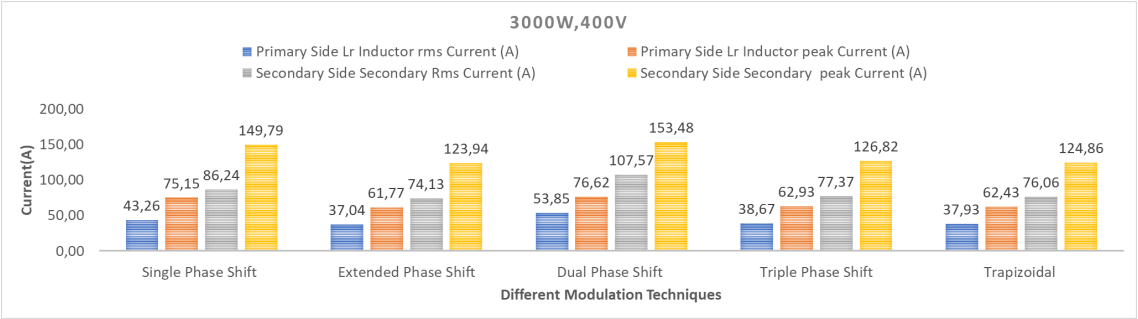

Figure 4.2: Different Modulation Techniques for Po- 3000W and Vin-400V

From the figure 4.2 above, we can see that currents in the Single Phase Shift are the highest compared to other modulation techniques. The least current through the leakage inductance in the 3000W loads is the EPS followed by Trapezoidal. The DPS is second highest after the SPS which can be seen in the figures 4.2 and 4.3. For the SPS Modulation, there was a constraint in achieving a wide voltage range. After iterating the voltage range for SPS. It was found from 290V to 450V.

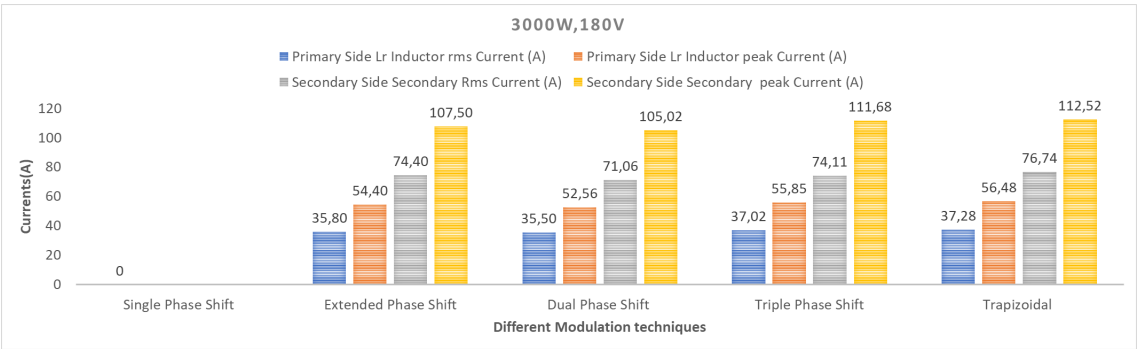

Figure 4.3: Different Modulation Techniques for Po- 3000W and Vin-180V

SPS and DPS are cancelled for lower loads because they have the highest currents for the 3000W at 400V and 180V, respectively.Triangular Current modulation is used

instead of the two previously mentioned modulation techniques. Triangular Current Modulation (TRG) is commonly used for lighter loads due to its low switching losses compared to other modulation techniques, as evidenced by numerous references. According to simulation, TRG has the lowest RMS and peak currents among modulation techniques.

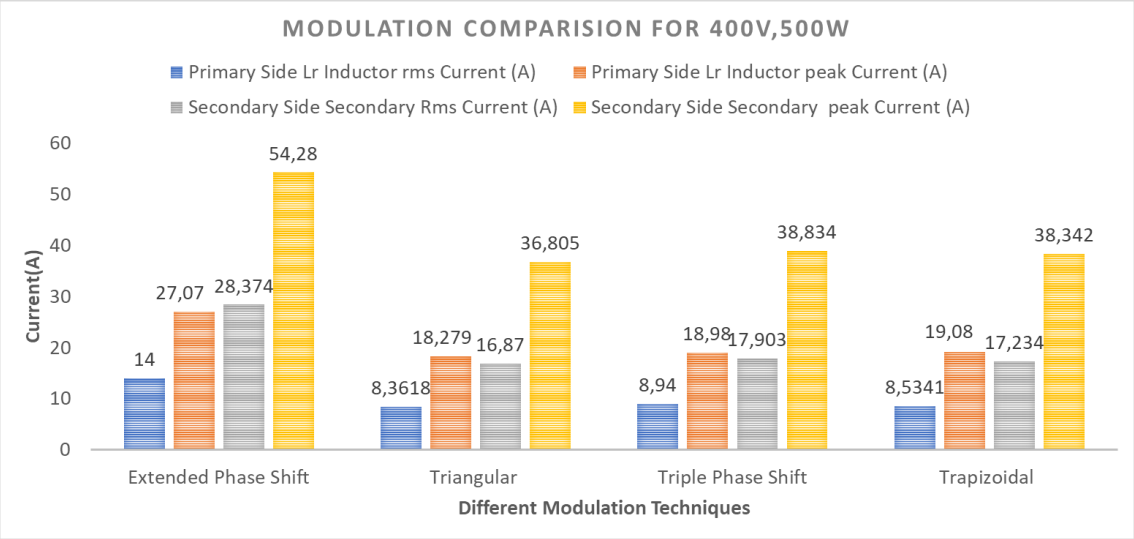

Figure 4.4: Different Modulation Techniques for Po- 500W and Vin-180V

In lighter loads, Triangular Modulation outperforms other modulation techniques where currents are low.

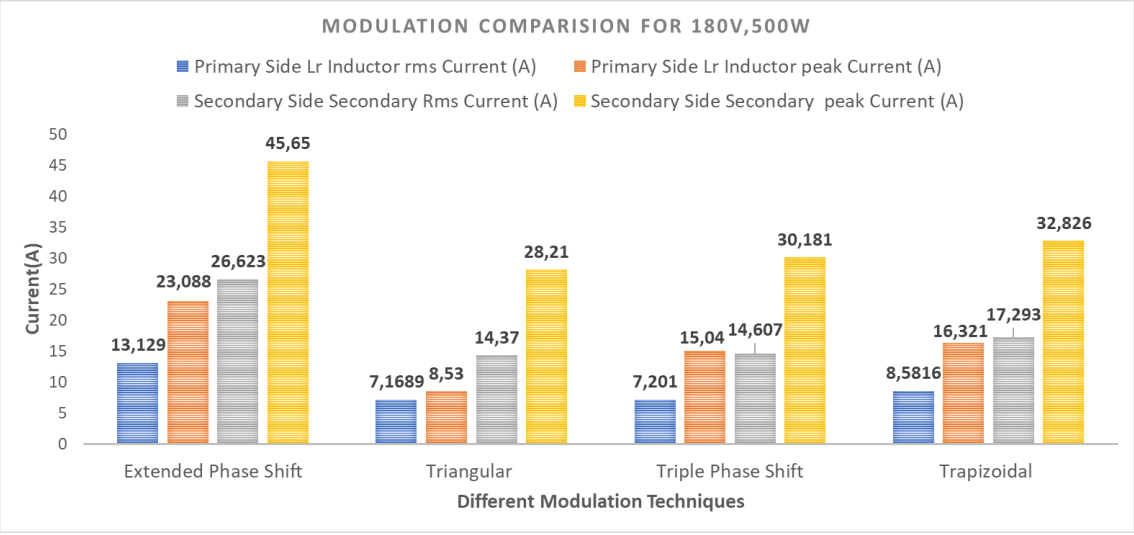

Figure 4.5: Different Modulation Techniques for Po- 500W and Vin-180V

As a result of the comparison from simulation, we chose Extended Phase Shift Modulation for Higher Loads, preferably from 1000W to 3750W, and Triangular Current Modulation from 1000W to 100W.

4.3 Analysis

4.3.1 Choosing LTSpice over PSpice for Optimization

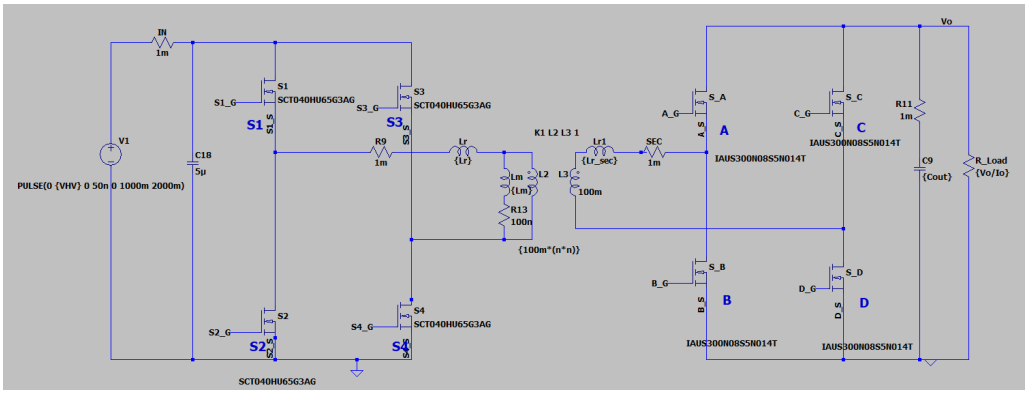

Figure 4.6: LTSpice DAB VDMOS Circuit Model

PSpice for DAB requires significantly more time to simulate than LTSpice.This is also due to the manufacturer's PSpice models, which include thermal and parasitic MOSFET characteristics such as inductor and capacitor, making the simulation take longer. When compared to a full bridge converter, DAB takes over three times longer to achieve a stable state. Moving the simulation tool from PSpice to LTSpice improves the speed with which results can be extracted. This thesis did not take into account the possibility of varying frequency based on load and voltage to improve performance in this topology.
One operating point were selected from PSpice and LTSpice to ensure a good comparison, and it was concluded that LTSpice can be used as a simulation for further analysis due to less than 1% error , as shown in Table 4.1 below.

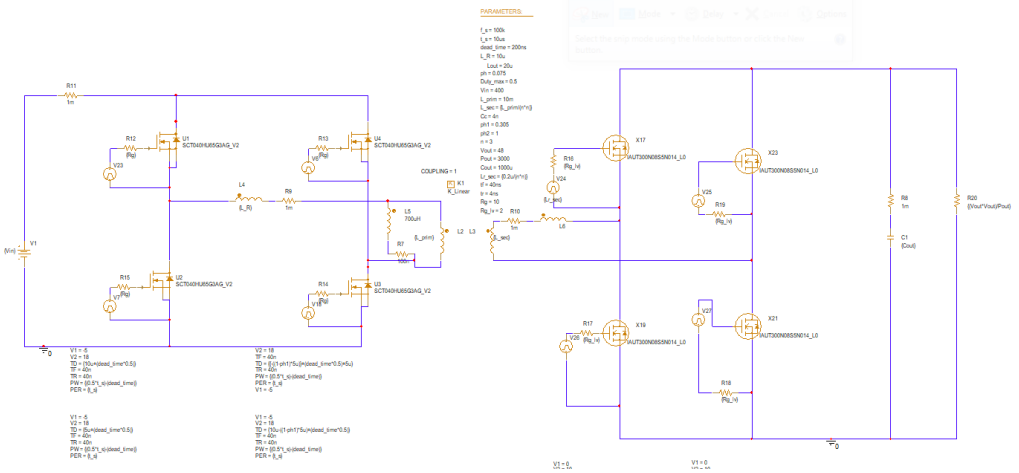

Figure 4.7: PSpice DAB Model

		For Comparison with Pspice and Ltspice	
Parameters		Pspice	Ltspice
Input Voltage(V)		400	400
Primary Peak Current (A)		46,492	45,53
Primary rms current(A)		26,992	26,66
Input Power(W)		3198,2	3231,1
Output Power (W)		3046,8	3071,4
Inner Phase Shift	Ratio	0,305	0,31
	Degree	54,9	55,8
Outer Phase Shift	Ratio	0,075	0,075
	Degree	13,5	13,5
Efficiency		95,266	95,057
Error %		0,997	

Table 4.1: Comparison Table between LTSpice and PSpice

The graphical analysis in the figure below shows that LTSpice and PSpice have values that are similar to each other. The error percentage between the two is only 0.99

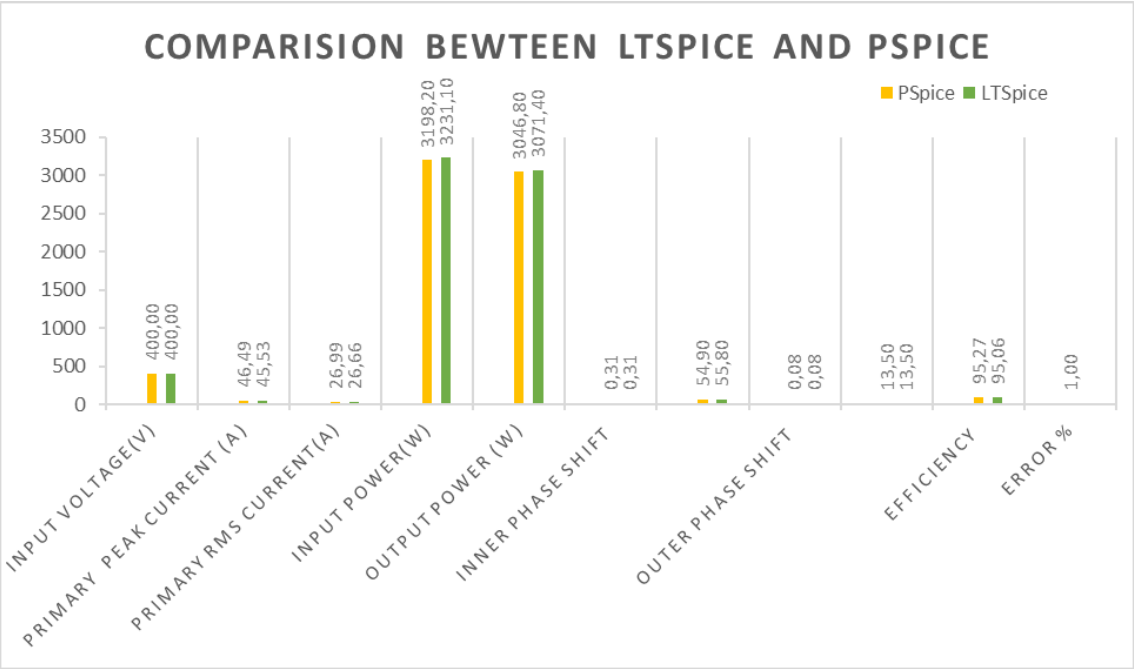

Figure 4.8: Comparison Graph Between LTSpice and PSpice

4.3.2 Basic Design Details

Table 4.2 is not considered in the above modulation comparison, whether it is for modulation or software comparison.After many iterations to satisfy the transient and continuous conditions for worst-case analysis, the design table is created and considered final for further analysis.

Basic Component Details	
Voltage Stress across Primary Mosfet	450V
Voltage Stress across Secondary Mosfet	48V
Leakage Inductance	10.8uH
Turns ratio	3
Output Capacitance	1500uF
Switching frequency	75kHz
Magnetizing Inductance	700uH

Table 4.2: Basic Component design details -Dual Active Bridge

Secondary Switch Parameters	
Parameter	Value
Si MOSFET	IAUS300N08S5N014T
V_{ds}	80V
I_d	300A
R_{dson}	1.4mOhm
V_{gsth}	3.8V
C_{iss}(Input Capacitance)	13178pF
C_{oss}(Output Capacitance)	2114pF
C_{rss}(Reverse transfer Capacitance)	106pF

Table 4.3: Secondary MOSFET Details

4.3.3 Loss Analysis

4.3.3.1 Primary Switches

As discussed above,3750W to 1000W works on EPS and from 1000W to 100W works on TRG.For the higher loads which work in DPS, it can observed from Table 4.4 that for the primary side bridge, one leg has a different I_d current waveform and the other leg has a different waveform from the Turn On and Turn Off currents. The continuation of one leg's current waveform is the other. One bridge observes ZVS which is Switch 3 and 4 which can be seen in Table 4.5 where turn-on loss is zero and turn-off is hard switched. Other bridges observe hard-switched turn-on and partial ZCS (Zero Current Switching). Though the RMS current for the primary switches is less than 30A, the peak current is 63.458A which is one of the biggest disadvantages of this topology. We can observe the losses of primary switches individually and whole in Figure 4.9 and Figure 4.10.

Modulation Technique	Power(W)	Input Voltage Range(V)	For Primary side Switch(4 switches)			
			Switch 1			
			Current at turn on(A)	Turn on Loss(W)	Current at Turn off(A)	Turn off Power(W)
Extended Phase Shift	3750	450,00	10,64	3,30	-2,43	2,77
		180,00	-7,13	1,37	42,18	4,36
	3000	450,00	17,28	4,14	-2,54	2,83
		180,00	-9,10	1,69	9,33	0,47
	1500	450,00	31,86	5,53	-1,71	2,38
		180,00	22,94	1,90	-2,56	1,14
Triangular Current Modulation	750,00	450,00	4,48	2,59	2,33	1,07
		180,00	2,24	0,97	1,90	0,46
	200,00	450,00	3,94	2,55	2,65	1,02
		180,00	1,39	0,96	1,55	0,49

Table 4.4: Primary Side Switch 1 Switching Losses

Modulation Technique	Power(W)	Input Voltage Range(V)	For Primary side Switch(4 switches)			
			Switch 4			
			Current at turn on(A)	Turn on (W)	Current at Turn off(A)	Turn Off Loss(W)
Extended Phase Shift	3750	450,00	-2,90	0,00	52,20	14,63
		180,00	-3,80	0,00	44,26	4,67
	3000	450,00	-4,54	0,00	47,40	12,87
		180,00	-3,29	0,00	37,96	3,75
	1500	450,00	-4,36	0,00	40,08	10,12
		180,00	-4,31	0,00	34,01	3,21
Triangular Current Modulation	750,00	450,00	-4,65	0,00	15,62	2,54
		180,00	-3,69	0,00	7,83	0,39
	200,00	450,00	-3,74	0,00	7,17	0,92
		180,00	-2,80	0,00	3,82	0,36

Table 4.5: Primary Side Switch 4 Switching Losses

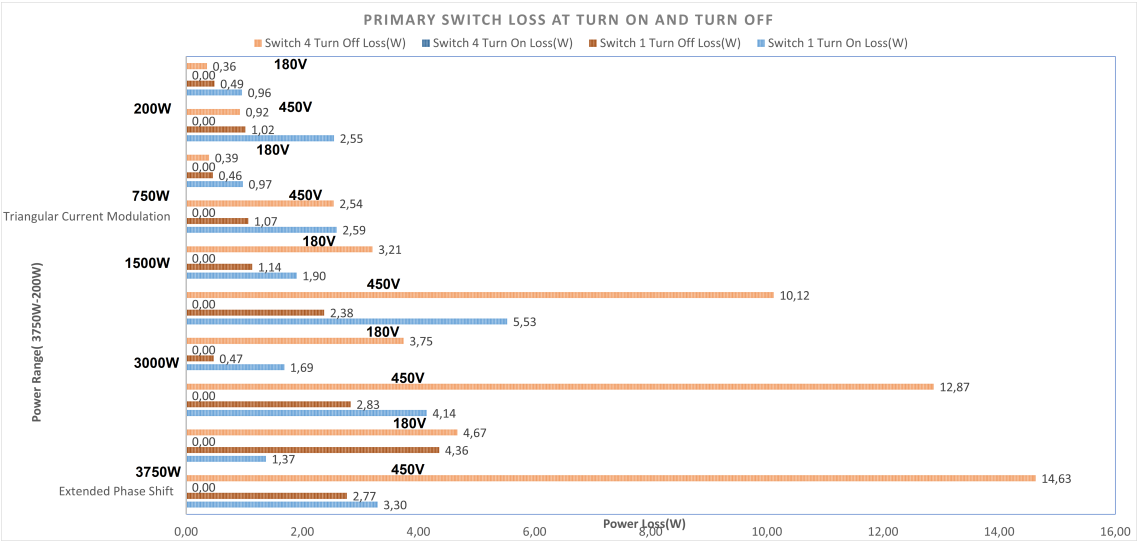

Figure 4.9: Primary Switch losses

Modulation Technique	Power(W)	Input Voltage Range(V)	For Primary side Switch(4 switches)									
			Ipk(A)	Irms(A)	Conduction Losses		Switching Losses			Total Losses for Single Switch(W)	Switching Losses from all Switch (W)	Total Loss across 4 switches(W)
					Single Switch(W)	All Switches(W)	Total Turn on(W)	Total Turn off(W)	Single Switch(W)			
Extended Phase Shift	3750	450,00	63,46	25,62	26,25	104,99	6,59	34,79	10,34	36,59	41,38	146,37
		180,00	53,92	29,18	34,05	136,19	2,75	18,05	5,20	39,25	20,80	156,99
	3000	450,00	60,64	23,88	22,80	91,22	8,28	31,41	9,92	32,73	39,70	130,91
		180,00	50,69	24,80	24,60	98,40	3,38	8,44	2,95	27,55	11,81	110,21
	1500	450,00	52,09	19,75	15,61	62,44	11,06	24,99	9,01	24,62	36,05	98,48
		180,00	46,32	19,73	15,58	62,30	3,81	8,69	3,12	18,70	12,50	74,80
Triangular Current Modulation	750,00	450,00	25,09	6,96	1,94	7,75	5,18	7,21	3,10	5,04	12,40	20,14
		180,00	13,03	4,85	0,94	3,77	1,95	1,71	0,91	1,86	3,66	7,42
	200,00	450,00	13,17	3,30	0,44	1,74	5,09	3,89	2,24	2,68	8,98	10,72
		180,00	6,90	1,97	0,16	0,62	1,92	1,69	0,90	1,06	3,61	4,23

Table 4.6: Primary Side Switches Loss Analysis

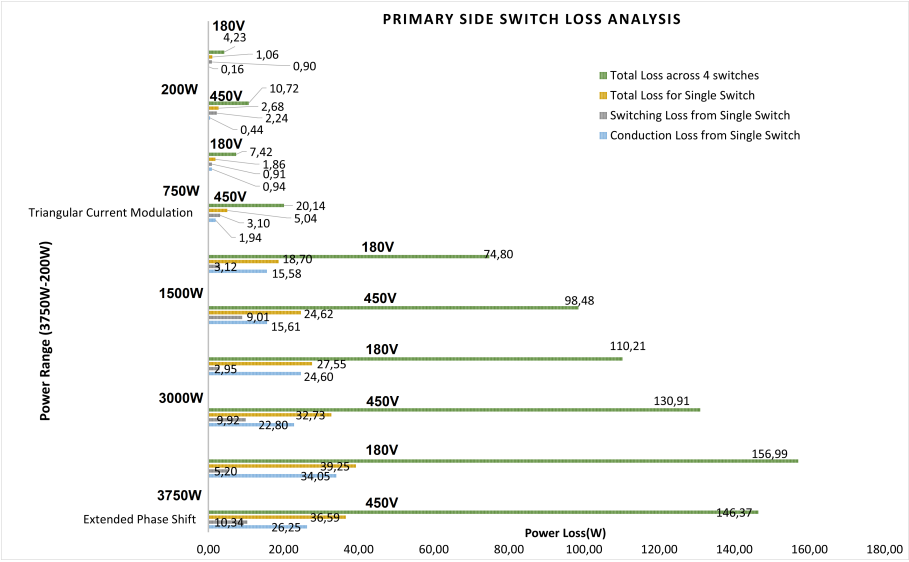

Figure 4.10: Primary Switch Loss Analysis

4.3.3.2 Secondary Switches

Given that there is no inner phase shift for heavier loads i.e., from 3750W to 1000W which works under Extended Phase Shift modulation, secondary bridge losses are similar during turned on and off in both legs of the bridge in secondary side which can be seen in Table 4.7.From Table 4.7 switching losses are reduced, as with the primary bridge for lighter loads due to implementation of TRG.

Modulation Technique	Power(W)	Input Voltage Range(V)	For Secondary side Switch(4 switches)								
			Switch A					Switch D			
			Current at turn on(A)	Voltage pk for secondary (A)	Turn on Loss(W)	Current at Turn off(A)	Turn off Loss(W)	Current at turn on(A)	Turn on Loss(W)	Current at Turn off(A)	Turn off Loss(W)
Extended Phase Shift	3750	450,00	10,32	56,88	0,29	-94,57	5,33	11,47	0,65	-101,774	5,73
		180,00	8,94	50,77	0,22	-113,017	5,68	9,32	0,47	-120,344	6,05
	3000	450,00	9,17	55,74	0,25	-106,03	5,85	8,90	0,49	-101,66	5,61
		180,00	11,10	50,36	0,28	-111,94	5,58	9,88	0,49	-115,05	5,74
	1500	450,00	7,85	55,55	0,22	-103,011	5,67	7,69	0,42	-102,011	5,61
		180,00	8,95	50,51	0,22	-105,246	5,26	6,88	0,34	-102,253	5,11
Triangular Current Modulation	750,00	450,00	5,36	54,32	0,14	-5,77	0,31	5,21	0,28	-6,48	0,35
		180,00	1,89	49,55	0,05	-2,13	0,10	3,88	0,19	-2,49	0,12
	200,00	450,00	5,20	54,37	0,14	-4,83	0,26	5,55	0,30	-5,69	0,31
		180,00	1,98	49,23	0,05	-2,47	0,12	2,20	0,11	-2,25	0,11

Table 4.7: Secondary Side Switches Turn On and Turn Off

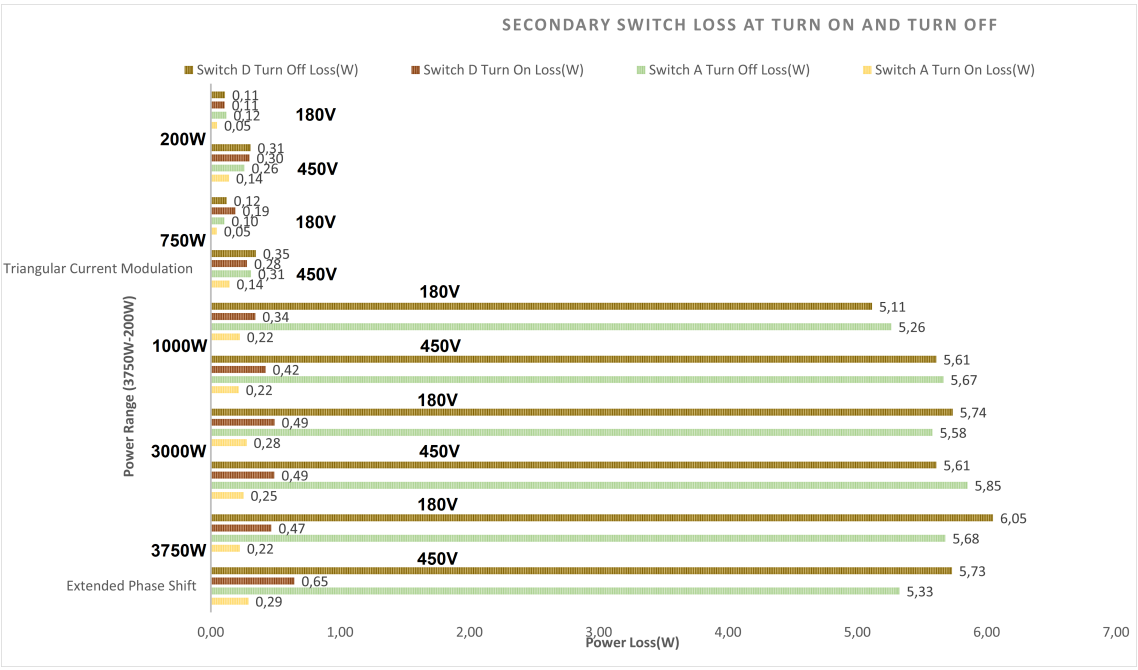

Figure 4.11: Secondary Switch Loss at Turn On and Turn Off

Modulation Technique	Power(W)	Input Voltage Range(V)	For Secondary side Switch(4 switches)									
			Ipk(A)	Irms(A)	Conduction Losses		Switching Losses			Total Losses for Single Switch	Total Switching Losses	Total Loss
					Single Switch	All Switches	Turn on Losses(W)	Turn off Losses(W)	Single Switch			
Extended Phase Shift	3750	450,00	191,80	78,03	8,52	34,10	1,87	22,11	6,00	14,52	23,99	58,08
		180,00	161,16	88,35	10,93	43,71	1,39	23,46	6,21	17,14	24,84	68,55
	3000	450,00	183,32	73,98	7,66	30,65	1,49	22,92	6,10	13,77	24,41	55,06
		180,00	152,69	76,17	8,12	32,49	1,54	22,64	6,04	14,17	24,17	56,67
	1500	450,00	156,96	61,93	5,37	21,48	1,28	22,55	5,96	11,33	23,83	45,30
		180,00	140,42	57,80	4,68	18,71	1,14	20,75	5,47	10,15	21,89	40,59
Triangular Current Modulation	750,00	450,00	76,33	21,09	0,62	2,49	0,85	1,32	0,54	1,16	2,17	4,66
		180,00	38,39	14,16	0,28	1,12	0,47	0,45	0,23	0,51	0,93	2,05
	200,00	450,00	39,22	10,13	0,14	0,57	0,88	1,13	0,50	0,65	2,01	2,58
		180,00	20,16	6,35	0,06	0,23	0,31	0,46	0,19	0,25	0,77	1,00

Table 4.8: Secondary Side Switches Loss Analysis

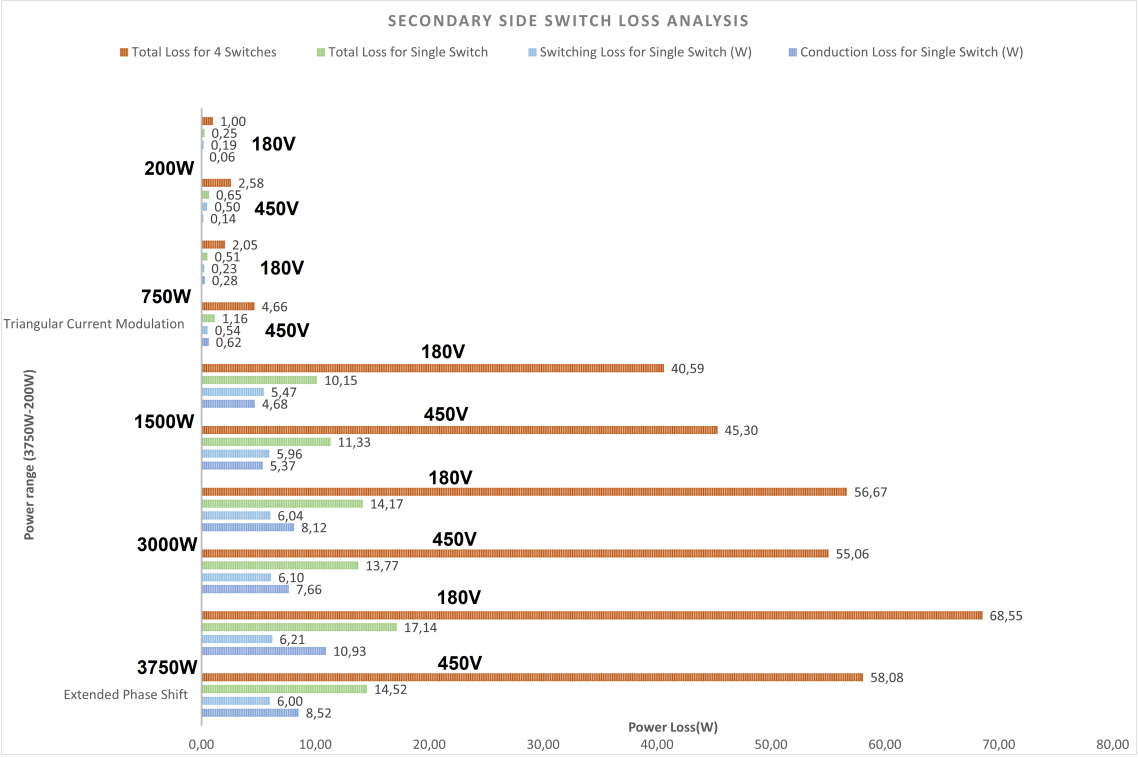

Figure 4.12: Secondary Switch Loss Analysis

4.3.3.3 Transformer

Using Equation 3.6 ,we calculate the required core loss .It is to predict the size of core required in the PCB(Printed Circuit Board) by which we can estimate the core loss.

Transformer Core details		
Lm	0,0007	700uH
Ae	0,000328	$333.7mm^2$
Number of turns in Primary side	N1	9
Number of turns in Secondary side	N2	3
Ve in cm^3	$74.2cm^3$	
Bmax	198mT	
Wire Resistance Rp	15mΩ	
Wire Resistance Rs	1mΩ	
Core type	PQ50/50	
Material	DMR95	

Table 4.9: Transformer Core Details

Power(W)	Input Voltage Range(V)	For Transformer									
		Iprms(A)	Ip peak(A)	Isrms (A)	Magnetizing Current Ripple(A)	Maximum Flux Density	PV (mW/cm3)	Core Loss(W)	Primary Copper Loss(W)	Secondary Copper Loss(W)	Total Loss(W)
3750	450,00	36,82	62,60	110,45	1,22	0,14	0,03	1,04	30,50	18,30	49,83
	180,00	41,65	53,53	124,95	1,20	0,14	0,03	1,04	39,03	23,42	63,49
3000	450,00	34,33	60,13	102,98	1,20	0,14	0,03	1,04	26,51	15,91	43,46
	180,00	36,22	50,75	108,65	1,20	0,14	0,03	1,04	29,51	17,71	48,26
1500	450,00	28,28	50,60	85,85	1,20	0,14	0,03	1,04	17,99	11,06	30,09
	180,00	27,92	46,84	83,76	1,20	0,14	0,03	1,04	17,54	10,52	29,10
750,00	450,00	9,69	24,57	29,35	0,90	0,11	0,03	1,04	2,11	1,29	4,44
	180,00	6,81	12,85	24,42	1,00	0,12	0,03	1,04	1,04	0,89	2,98
200,00	450,00	4,78	13,11	14,38	0,40	0,05	0,03	1,04	0,51	0,31	1,86
	180,00	2,84	6,58	8,52	0,60	0,07	0,03	1,04	0,18	0,11	1,33

Table 4.10: Transformer Loss Analysis

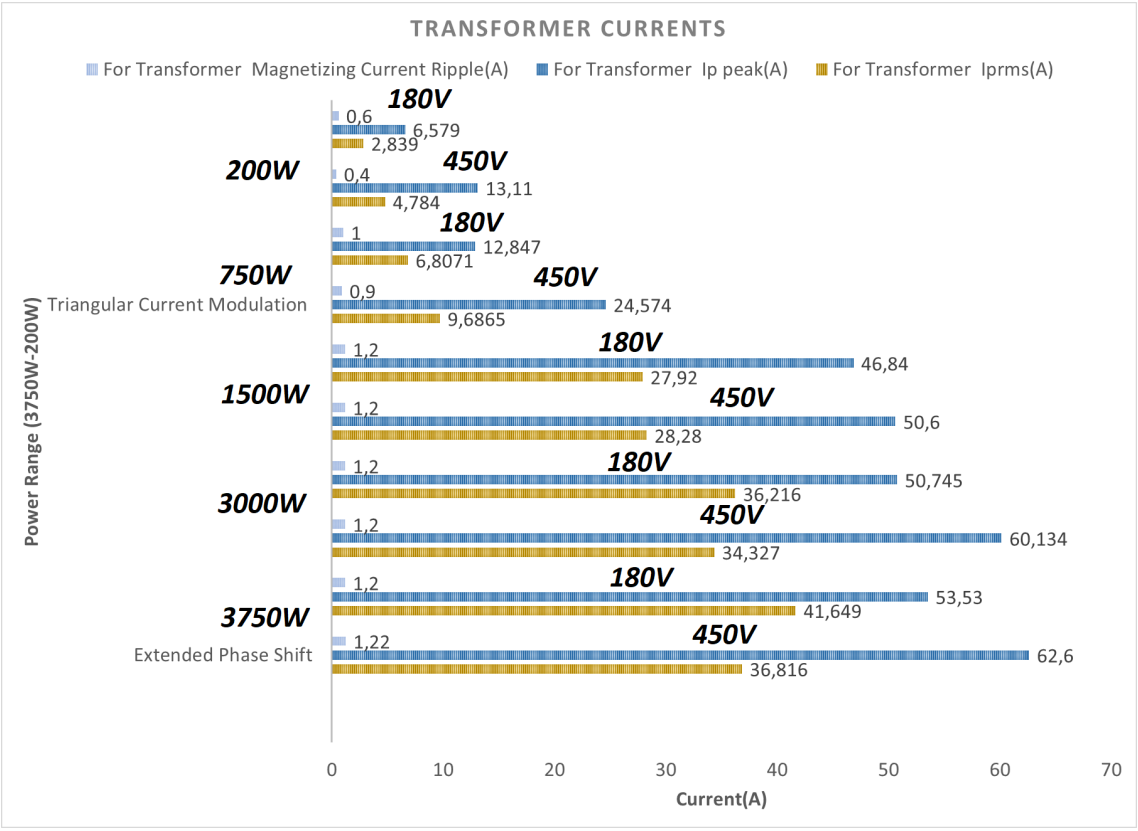

Figure 4.13: Transformer Currents

4.3.3.4 Leakage Inductance

When we see the table 4.11 ,we can observe that volume and area core is more than close to double that of transformer core .This is due to high peak current which can be seen in figure 4.11 and Table 4.10.

Inductor Core Details		
Inductance	Lr	9.8uH
Effective Area	Ae	683mm2
Peak Magnetic Flux Density	Bm	179mT
Volume of Core	V	204cm3
Resistance of the wire	5mOhm	
Airgap	2.15mm	
No of Turns	5	
Core type	EE71/33/32	
Material	DMR95	

Table 4.11: Inductance Core Details

Power(W)	Input Voltage Range(V)	For Inductor			
		PV (mW/cm3)	Core Loss(W)	Copper Loss(W)	Total Loss(W)
3750	450,00	0,05	10,20	6,78	16,98
	180,00	0,03	6,12	8,67	14,79
3000	450,00	0,05	10,20	5,89	16,09
	180,00	0,03	6,12	6,56	12,68
1500	450,00	0,03	6,12	4,00	10,12
	180,00	0,03	6,12	3,90	10,02
750,00	450,00	0,03	6,12	0,47	6,59
	180,00	0,03	6,12	0,23	6,35
200,00	450,00	0,03	6,12	0,11	6,23
	180,00	0,03	6,12	0,04	6,16

Table 4.12: Inductor Loss Analysis

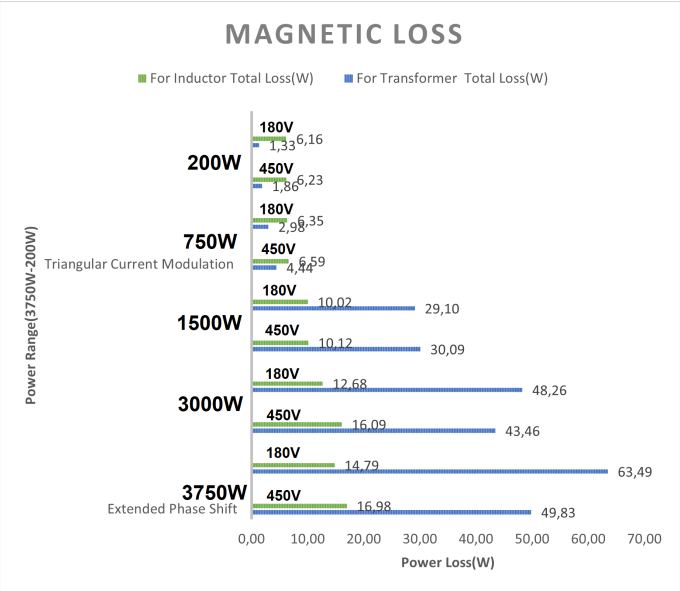

Figure 4.14: Magnetic Loss

4.3.3.5 Overall Efficiency

The overall losses can be seen in Table 4.13. The miscellaneous losses here are the copper losses of the traces in the PCB where assume it would be 50W for the maximum load and reduce by equivalent multiples according to the load. Operating under Extended Phase Shift Modulation(EPS) from 3750W to 1000W, it achieved an average efficiency of 92 %. Below 1000W, the implementation of Triangular Current Modulation(TRG) further improved efficiency to an average of 94 %. This performance made the Dual Active Bridge a more viable and efficient solution for the intended application, justifying its selection over the PSFB .

Power(W)	Input Voltage Range(V)	Overall					
		Miscellaneous Loss	Total Losses(W)	Output Power(W)	Input Power(W)	Efficiency	Input Voltage Range(V)
3750	450,00	50,00	321,26	3750,00	4071,26	92,11	450
	180,00	50,00	353,82	3750,00	4103,82	91,38	180
3000	450,00	32,00	277,52	3000,00	3277,52	91,53	400
	180,00	32,00	259,81	3000,00	3259,81	92,03	180
1500	450,00	8,00	192,00	1500,00	1692,00	88,65	400
	180,00	8,00	162,51	1500,00	1662,51	90,22	180
750,00	450,00	2,00	37,83	750,00	787,83	95,20	400
	180,00	2,00	20,80	750,00	770,80	97,30	180
200,00	450,00	0,14	21,55	200,00	221,55	90,27	400
	180,00	0,14	12,86	200,00	212,86	93,96	180

Table 4.13: Efficiencies for heavy load and light load in detail

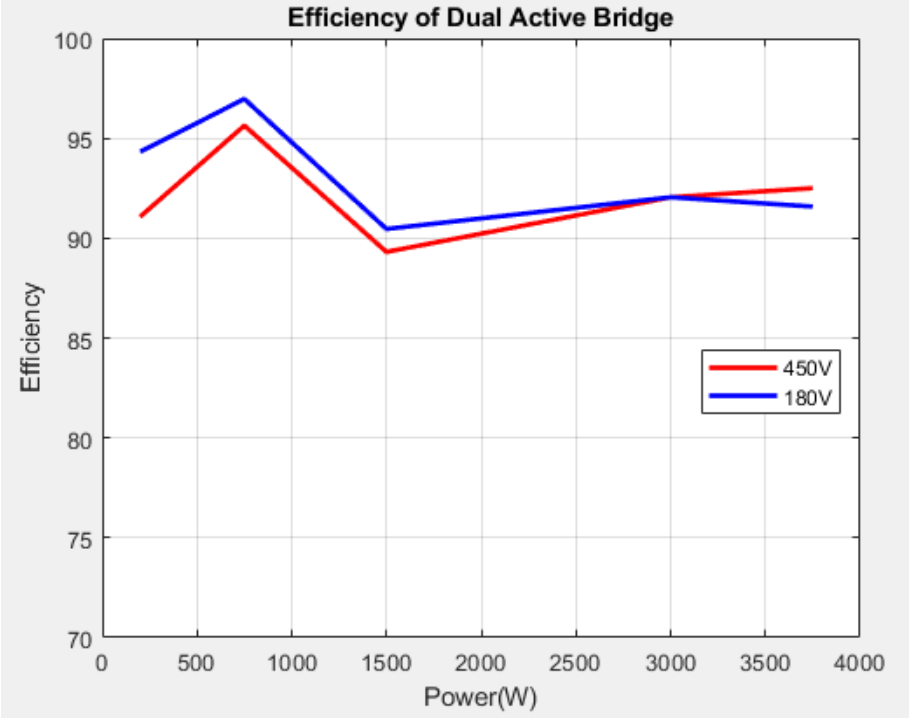

Figure 4.15: Efficiency Graph for DAB

At end we conclude, the DAB's average efficiency is good, but the implementation of the DAB with single phase is impractical. The concerns remain regarding high RMS and peak currents, which may result in significant copper loss in the circuit and Printed Circuit Board (PCB), and unreliable soft switching . The key limitation for high RMS and peak currents is wide input voltage range, leading to a lower turns ratio of the transformer for the 48V application.

5
Conclusion

On an end note from all analysis,the PSFB featured extremely high turn-off voltage oscillations across the MOSFETs on the secondary side, making it impractical to control the oscillations with a snubber and active clamping. As a result, it was decided to stop optimizing the PSFB.
Consequently, the focus shifted to the Dual Active Bridge, which demonstrated better performance under varying loads. Operating under Extended Phase Shift Modulation(EPS) from 3750W to 1000W, it achieved an average efficiency of 92 %. Below 1000W, the implementation of Triangular Current Modulation(TRG) further improved efficiency to an average of 94 %. This performance made the Dual Active Bridge a more viable and efficient solution for the intended application, justifying its selection over the PSFB .
The DAB's average efficiency is good, but the implementation of the DAB with single phase is impractical. The concerns remain regarding high RMS and peak currents, which may result in significant copper loss in the circuit and Printed Circuit Board (PCB), and unreliable soft switching . The key limitation for high RMS and peak currents is wide input voltage range, leading to a lower turns ratio of the transformer for the 48V application.
Future work could include the use of different topology architectures such as interleaved DAB, series primary input parallel secondary output, and so on, which can reduce current stress in the circuit while increasing the number of switches used.

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A

Appendix 1

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