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Design of an E-band QPSK Modulator Employing a Novel Power Combining Strategy

Master's degree thesis in Wireless, Photonics and Space Engineering

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Abstract

Quadrature phase shift keying is an important modulation format in telecommunications engineering. The most common ways in which a signal in this modulation format is generated is associated with large losses of up to and exceeding 50 % of the available signal power. At the high operating frequencies of modern state-of-the-art telecommunications circuitry, this output power comes at a significant cost.

In this work, we show how the traditional way of combining power from an in-phase and quadrature signal source in a QAM system is associated with losses. We then start from first principles and derive the conditions under which a network operates as an ideal power combiner, respecting the constraints imposed by the modulation format. Furthermore, we show how a practical passive circuit that comprises this benefit can be designed. The theory is then put into practice in an illustrative design of an E-band QPSK modulator, where we also design a purpose-built power combiner according to the elaborated theory and show that this circuit can be easily designed into a modulator circuit.

We finally perform simulations to verify the benefits of the designed power combiner. As predicted by theory, the combiner itself is almost lossless save from the small resistive losses that are expected in associated metal conductors, reasserting its benefit over traditional circuits, such as the Wilkinson power combiner.

Keywords: QPSK, Modulator, Power combiner, Circuit theory, Analog integrated circuit design.

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I would like to thank my examiner Herbert Zirath for welcoming me into the Microwave Electronics Laboratory and my supervisors Christian Fager and Mustafa Özen for their patience, insight and valuable suggestions throughout this project. Your guidance has been a tremendous source for growth.

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This thesis is dedicated to my parents and to my brother. Thank you for your endless support and motivation, and for always reminding me why I am doing what I am doing when I often forget. It has been a long way, but we finally made it!

Mark Popescu

Abbreviations

a.u.	Arbitrary units
ASIC	Application specific integrated circuit
BiCMOS	Bipolar junction transistor and MOSFETs
BJT	Bipolar junction transistor
BW	Bandwidth
CML	Current mode logic
CMOS	Complementary MOS logic
CORDIC	Coordinate rotation digital computer
f_C	Center frequency
f_{LO}	LO frequency
HBT	Heterojunction bipolar transistor
η	Efficiency
IF	Intermediate frequency
InP	Indium phosphide
LO	Local oscillator
LTE	Long term evolution
MOSFET	Metal oxide-semiconductor field effect transistor
P_{DC}	DC power
P_{OUT}	Output power
QAM	Quadrature and amplitude modulation
QPSK	Quadrature phase shift keying
RF	Radio frequency
RF-DAC	RF digital to analog converter
SiGe	Silicon germanium
SOI	Silicon on insulator
V_{OP}	Operating voltage

Contents

Chapter 1

Introduction

1.1 Communications technology

Communication is fundamental to humans. Since the earliest of times, communication has enabled our fundamentally social species to interact and evolute from the small, primordial hunter-gatherer communities of the past towards the large, highly organized societies of today. At closer inspection, our large cities are truly landmarks of human development, showcasing our ability to organize. Nevertheless, the infrastructure keeping them alive can easily be taken for granted. Communications technology is a very significant part of this infrastructure, and equally easily overseen, despite its daily usage. Today, this technology ranges from specialized applications such as satellite communications and industrial sense and control networks to the Internet itself. Implicitly, with the latter, this also encompasses the infrastructure supporting it, from the countless PC's, mobile phones and other "terminals" used to access this structure, to the enormous backbone supporting it.
The scale of the Internet and thus, roughly speaking, the scope of digital communication as a whole, is indeed difficult to imagine. Most people do realize their extent, but rarely ponder on the associated implications. As an example, attempts at estimating the power consumption of the machinery supporting the Internet alone have revealed figures of 1% or more of the global electrical energy expenditure[1]. Needless to say, any method resulting in a lower system power consumption is welcome on the grounds of both sustainability-aware policies and the cost and convenience benefits associated with such lower power consumption.
In this work, we will focus on the QPSK modulators often found in the transmitter sections of modern digital communications front ends, and discuss factors related to their power efficiency, where we will show how design tradeoffs can be made at the output stage of these important building blocks in order to achieve benefits along the lines described above.

1.2 Data frequency conversion

Whenever we want to exchange information (data) between two or more nodes over some intermediate medium, we face a situation where data of varying degrees of entropy and thus frequency content needs to be accommodated within the operating

limits of that specific medium. For instance, radio channels for over-the-air communications are limited both by physical factors, such as lower frequency limits for efficient antenna design, atmospheric molecular interaction at certain frequencies, and of course, national regulations governing the use of what is essentially a limited resource. Regardless of the data rate the user would like to achieve, adherence to strictly defined, specific frequency bands is mandatory, and often dictates the use of frequency conversion. We say that we may convert frequencies to and from the baseband, that is, the frequency spectrum needed to adequately represent the given data, and the RF band, that is, the frequency spectrum intended for its transmission. The abbreviation RF stands for Radio Frequency, showing the historical link to the earliest applications of frequency conversion to radio transmission, but communication in this fashion is not limited to air as supporting medium. In fact it applies equally well to various other modes of wave propagation along waveguides and in bulk media, such as within the field of photonics.
The process of frequency conversion is both conceptually and for the sake of practical use best illustrated with the well known trigonometric identity

$$\cos(\omega_i t)\cos(\omega_r t) = \frac{\cos((\omega_i - \omega_r)t) + \cos((\omega_i + \omega_r)t)}{2} \tag{1.1}$$

We see two terms on the right-hand side, where one is useful for so called up-conversion, that is, to convert a signal of frequency ω_i to another frequency ω such that $\omega > \omega_i$, and the dual operation of down-conversion by the usage of the second term, yielding the conversion of a signal of frequency ω_i to another frequency ω such that $\omega < \omega_i$. The unneeded term is simply filtered out. In the electrical domain, this process is achieved with components known as mixers, which are well reviewed in most electronics textbooks [2, 3]

1.3 Quadrature modulation

Quadrature modulation is an information encoding technique fundamental to modern digital communication. We saw previously how we can, through the process of frequency conversion, move data from one part of an operating frequency spectrum to another. Without formal proof or discussion of ways of doing so, we now assert that information can be encoded within a certain frequency spectrum. This statement can be verified by considering properties of signals subject to Fourier transform calculus. This theory shows how periodic signals can be represented as weighted sums of harmonic basis functions. Since a given signal space has an essentially unlimited set of basis functions in the purely mathematical sense, this also means that we in theory could have an equally unlimited space in which to encode information. In practice, though, this ideal situation is bounded by factors such as the local oscillator phase noise, among other non-idealities, effectively limiting our usable set of basis functions, and as such, also the information density we can achieve over a given frequency band.
Beyond operation frequency we can identify another degree of freedom in the phase of the harmonic basis functions with respect to some fixed phase reference. In quadrature modulation, we transmit two harmonic signals, offset by $\pi/2$ radians

with respect to each other as two signals in a floating frame of reference. This configuration has the advantage that the delay of the signal from the instant it was sent to the time of reception does not need to be fixed for successful decoding of the phase information. In fact, there is no need at all to even know when the signal was sent as the phase reference lies within the signal itself.
By applying the inner product as it is defined in the context of Fourier transforms over a period T, on two signals S_I and S_Q of unit magnitude but phase offset of $\pi/2$ radians with respect to each other, we have

$$\langle S_I, S_Q \rangle = \int_T \cos(\omega t) \cos(\omega t + \frac{\pi}{2}) = 0$$

where $T = [t, t + \frac{2\pi}{\omega}]$, showing us that two such signals are orthogonal. Since they are linearly independent, we can encode information in both of them at the same time without any repercussions at data reception save for ambiguity as to which of the components are leading or lagging the other at a certain instant. This ambiguity must be resolved in the receiver before any attempt at decoding the data is made.
The creation of two signals S_I and S_Q is simple enough when starting out with two given (baseband) data signals d_1 and d_2, a local oscillator with two outputs, where any one of them is leading or lagging behind the other by $\pi/2$ radians and two mixers to convert the data signals with these two local oscillator outputs as shown in Fig.1.1. The phase information from the local oscillator is conferred to the two baseband data signals in the frequency conversion process. This is seen by simply substituting $\omega_r t + \phi$ for $\omega_r t$ and re-evaluating (1.1). The two up-converted signals are combined before additional processing and, eventually, transmission in the form of $S_{OUT} = H(S_I + S_Q)$, where H is any additional processing before transmission, including filtering and amplification.
Beyond signal frequency and phase, the signal amplitude presents yet another degree of freedom usable for encoding data. Again, even a bounded amplitude interval, by virtue of its continuity, is infinitely subdivisible, theoretically accomodating an infinite information space for us to utilize. Unfortunately, we are again limited, but now mainly by the signal power signal to noise ratio.
For good utilization of the transmitting medium, phase and amplitude are often used freely to encode information, while the frequency content (ie. bandwidth) of the signal is often limited to a certain extent, and binned into discrete channels. This series of events is extensively reviewed in all telecommunications textbooks, for instance [4].

1.4 Possible power savings in QAM systems

We have briefly discussed some aspects of communications systems and introduced the concept of quadrature amplitude modulation as both modern mobile and wired networking standards often use some variant of this modulation format.
Referring to Fig.1.1, we can easily infer that the efficiency of the system may be improved by increasing the efficiency of any of the data converters, mixers, local oscillator, combiner Σ or output amplifier/-processing circuitry H. Of course, the topology in the figure is purely illustrative, and the components neither need to

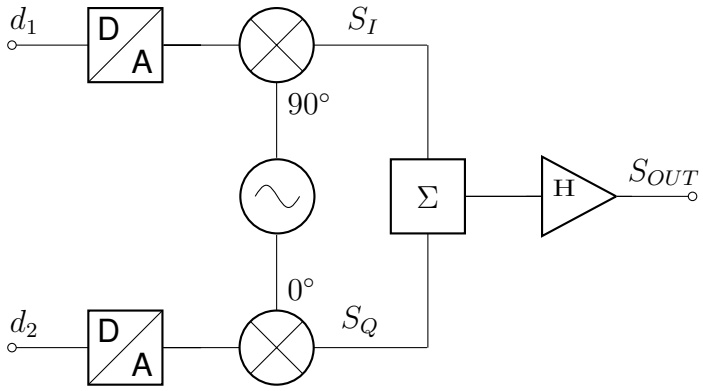


Figure 1.1: Generic analog cartesian quadrature modulator.

be ordered as shown nor the modulator implemented strictly in this way. In fact, the so called polar modulator is an alternative to this more traditional cartesian modulator, the difference being the way in which the output signal is constructed from the corresponding basis vectors. This is also shown by the identity

$$S_{OUT} = \hat{\boldsymbol{I}} S_I + \hat{\boldsymbol{Q}} S_Q = \hat{\boldsymbol{r}} S_r + \hat{\boldsymbol{\theta}} S_\theta$$

where $\hat{\boldsymbol{I}}$ and $\hat{\boldsymbol{Q}}$ are the cartesian unit vectors in the IQ signal space, while $\hat{\boldsymbol{r}}$ and $\hat{\boldsymbol{\theta}}$ are the corresponding polar unit vectors in the same space; the two representations are equivalent. The last expression on the right-hand side represents the manner in which the polar modulator covers the IQ space. The nonlinear relationship between input and output signals in the polar modulator often necessitates the use of either some CORDIC implementation or a look-up table, and associates the polar modulator with higher intermodulation distortion at the output than the cartesian modulator. Consequently, digital pre-distortion and additional considerations may also be needed in this topology, which we will not consider further in this work.
We have not addressed the digital to analog conversion process in our previous discussion. There are many ways in which this conversion can be implemented in order to respect certain design constraints. For our purpose, though, we would like to integrate this functionality in the modulator stage itself. A circuit able to synthesize the RF signal directly from baseband data is often called a RF-DAC, although the line between such a RF-DAC and a modulator can be blurred.
A literature survey reveals considerable attempts at improving the efficiency of all individual components in the signal chain except for, surprisingly, the power combiner at the end of the signal chain. This component is often implemented either by direct power combining through some current summing circuit topology, or by using some other passive power combiner structures. Often, this passive structure is implemented in the form of a Wilkinson power divider [5] connected in reverse, a so-called Wilkinson power combiner.
In the case of the Wilkinson power combiner, using the circuit as shown in Fig.1.2 with quadrature signals as inputs presents a significant problem. We can see this by defining two such input signals $S_I = V_0$ and $S_Q = jV_0$ and observing the voltage wave at the output (which is impedance matched, and implies that all output power

is delivered to the load)

$$\boldsymbol{V}_- = S\boldsymbol{V}_+ = \frac{-j}{\sqrt{2}}\begin{bmatrix}0 & 0 & 1\\ 0 & 0 & 1\\ 1 & 1 & 0\end{bmatrix}\begin{bmatrix}S_I\\ S_Q\\ 0\end{bmatrix} = \begin{bmatrix}0\\ 0\\ V_0(1-j)/\sqrt{2}\end{bmatrix}$$

and then evaluating the input and output signal power

$$P_{IN} = \frac{S_I S_I^*}{2R} + \frac{S_Q S_Q^*}{2R} = \frac{V_0^2}{R}$$

$$P_{OUT} = \frac{\frac{V_0(1-j)}{\sqrt{2}}\frac{V_0(1-j)}{\sqrt{2}}^*}{2R} = \frac{V_0^2}{2R}$$

such that $P_{OUT}/P_{IN} = 1/2$, which means that half of the power entering the Wilkinson power combiner will be dissipated in the matching resistor inside it. For designs operating at high frequencies, where both gain and output power are expensive, the prospect of preserving this additional output power by devising an appropriate power combiner is indeed attractive.

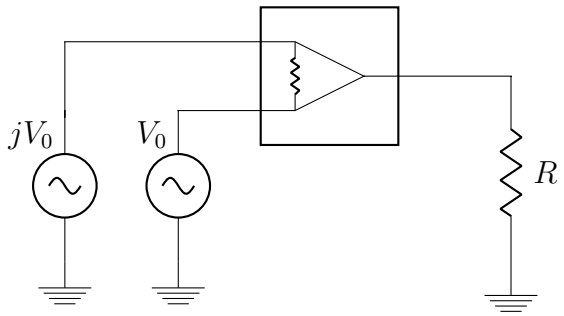


Figure 1.2: Wilkinson divider used as power combiner.

1.5 Thesis contribution and outline

In this work, we start from first principles and devise a power combiner that allows us to overcome the problems discussed in this chapter by including the phase of the signals presented to the combiner in the derivation of a combiner circuit. To the best of our knowledge, neither the concepts we will present, nor the final combiner circuit have been previously published for applications within the scope of this study, and thus represent new knowledge.

In chapter 2, we apply circuit theory in order to devise an appropriate power combiner and to design such a combiner given practical design specifications. In chapter 3, we discuss in detail the design and construction of an integrated modulator circuit using a power combiner designed according to the information in chapter 2. In chapter 4, we perform simulations on a test circuit designed according to the outline presented in chapter 3 and finally, in chapter 5, we conclude our work by comparing the designed modulator to other designs and discuss possible improvements.

Chapter 2

Initial investigation

Following the background outlined in the previous chapter, we set out to investigate how a power combiner that respects the discussed constraints can be designed, and how such a combiner would differ from the more commonly used Wilkinson or current summing junction combiners in a simulated environment.

2.1 Construction of the impedance matrix

In the case of the Wilkinson power combiner, losslessness is traded for matched impedances at all ports and the reciprocity implicit in this passive network [5]. The resistor bridging the input lines in this circuit dissipates power in certain operating points, such as the one presented in the previous chapter.
Turning to power amplifier theory, we know that power amplifiers, in general, need to be presented an impedance Z_{OPT} at their outputs in order to operate at maximum efficiency, a so called power-match [6]. In general, this impedance is not equal to the system characteristic impedance Z_0, and we can thus exploit this fact to relax the conditions on our power combiner by allowing the combiner network to present an impedance $Z_{IN} \neq Z_0$ at its inputs.
Along these lines, we would want to combine power from two phase offset sources, when fed into ports of some specified impedance $z_{IN} \neq Z_0$ in a lossless combiner with output impedance matched to the load, $Z_{OUT} = Z_L^*$. Assuming the existence of such a network, we can construct the corresponding impedance matrix as

$$\mathbf{V} = Z\mathbf{I} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \mathbf{I} = \begin{bmatrix} jX_{11} & jX_{12} & jX_{13} \\ jX_{12} & jX_{22} & jX_{23} \\ jX_{13} & jX_{23} & jX_{33} \end{bmatrix} \mathbf{I}$$

where the port voltages $\mathbf{V} = [\mathbf{v}_1, \mathbf{v}_2, \mathbf{v}_3]^T$ depend on the corresponding port currents $\mathbf{I} = [\mathbf{i}_1, \mathbf{i}_2, \mathbf{i}_3]^T$, $Z = Z^T$ assures network reciprocity and the simplification leading to the fully reactive impedance matrix represents the required losslessness.
In our case, we present the network with two input voltage signals equal in amplitude, $\mathbf{v}_1 = v_0$ and $\mathbf{v}_2 = v_0 e^{j\theta} = jv_0$, where $\theta = \pi/2$ by the definition of quadrature signals.

We now want to extract an output of the form $\mathbf{v}_3 = \boldsymbol{\alpha}(\mathbf{v}_1 + \mathbf{v}_2) = v_0 \alpha e^{j\phi}(1+j)$ from the network, such that the phase difference between the two constituent signals is preserved at the load $Z_L = R_L + jX_L$. The factor $\boldsymbol{\alpha} = \alpha e^{j\phi}$ represents any additional phase delay and signal attenuation imposed by the network.
We find the matrix elements using $e^{j\theta} = e^{j\pi/2} = j$, $Z_{IN,1} = Z_{IN,2} = Z_{OPT} = R_{OPT} + jX_{OPT}$ and $Z_{IN,3} = Z_L$ as described above. The linear system is then

$$Z_{IN} = \begin{bmatrix} Z_{IN,1} \\ Z_{IN,2} \\ Z_{IN,3} \end{bmatrix} = \begin{bmatrix} Z_{11} + Z_{12}\frac{\mathbf{V}_2}{\mathbf{V}_1} + Z_{13}\frac{\mathbf{V}_3}{\mathbf{V}_1}\frac{Z_{opt}}{Z_L} \\ Z_{12}\frac{\mathbf{V}_1}{\mathbf{V}_2} + Z_{22} + Z_{23}\frac{\mathbf{V}_3}{\mathbf{V}_2}\frac{Z_{opt}}{Z_L} \\ Z_{13}\frac{\mathbf{V}_1}{\mathbf{V}_3}\frac{Z_L}{Z_{opt}} + Z_{23}\frac{\mathbf{V}_2}{\mathbf{V}_3}\frac{Z_L}{Z_{opt}} + Z_{33} \end{bmatrix} = \begin{bmatrix} Z_{OPT} \\ Z_{OPT} \\ Z_L \end{bmatrix}$$

We expand the three equations describing this system, and split them in their real and imaginary parts to get a new system of six equations

$$M\mathbf{x} = \mathbf{b}$$

with M being the coefficient matrix of this system, $\mathbf{x} = [x_{11}, x_{12}, x_{13}, x_{22}, x_{23}, x_{33}]^T$ the vector of combiner reactances and $\mathbf{b} = [R_{OPT}, X_{OPT}, R_{OPT}, X_{OPT}, R_L, X_L]^T$ the port impedance constraints. The matrix M turns out to be singular, and the equation above can thus not be solved for the parameter vector $\mathbf{x}$ by using the matrix inverse. Instead, we can use optimization to solve for $\mathbf{x}$. Simply applying the least-squares algorithm, and rescaling the result to Z_0 yields an impedance matrix Z with the desired behaviour. To enable admittance matrix based methods of circuit synthesis, we can add the additional resistive elements $r_1 \gg \max(x_{12}, x_{13}, x_{23})$ and $r_2 = r_1 + r_\Delta$ with $r_\Delta \ll \min(x_{11}, x_{22}, x_{33})$ to the impedance matrix so that

$$Z = \begin{bmatrix} r_2 + jx_{11} & r_1 + jx_{12} & r_1 + jx_{13} \\ r_1 + jx_{12} & r_2 + jx_{22} & r_1 + jx_{23} \\ r_1 + jx_{13} & r_1 + jx_{23} & r_2 + jx_{33} \end{bmatrix}$$

At this moment it is reasonable to ask if the coefficient matrix M is not invertible after adding the resistive elements. This is, in fact, the case, but this approach is still prone to numerical errors, and no attempts at identifying the domain over which the matrix is reliably invertible were made. Solving the system of equations through optimization is always guaranteed to generate at least one solution, which for our purpose is satisfactory, and gives component values after realization which are insensitive to the choice of r_1 and r_Δ as long as these satisfy the previously given condition. For invertible matrices M, the solutions would be the same anyway, regardless of the method chosen.

2.2 Network realization for the single-ended case

A network represented by the impedance matrix we found with the previously outlined methods can now be realized in a number of ways, although there is no algorithmic method of synthesizing an optimum network based on such an impedance matrix

alone. There are infinitely many networks which reduce to any given impedance matrix, and algorithmic methods can find only a limited subset of these solutions. For our purpose, we selected a method previously used in our group to algorithmically generate a circuit for the single ended case [7]. This method is based on the representation of the entire three port network as two two-port networks joined at the load resistor. Applying the fixed load resistor to one of the ports allows us to reduce the three port network to a lossy two-port. This can be represented as either a pair of T-networks joined as the load as shown in Fig.2.1, or as a pair of π-networks by properly transforming the given T-networks.

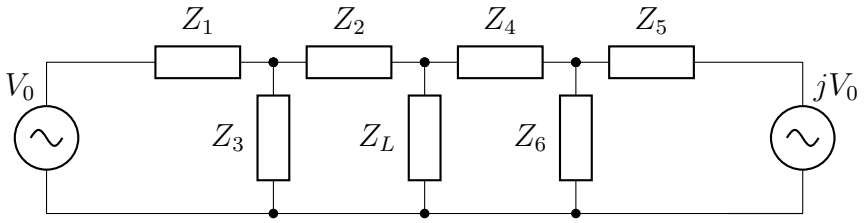


Figure 2.1: Devised power combiner circuit for the single-ended case.

When used with the Z-matrix generated according to the previous discussion, the elements Z_1 and Z_5 in Fig.2.1 will often have a negligibly small impedance and thus be possible to omit altogether, such that a finished combiner such as this one has four components in the single ended configuration or six components in the differential configuration.

2.3 Comparison between power combiners

In the following section, we will investigate the impact of two commonly used power combining strategies on combining efficiency before comparing them to a test case of our purpose designed power combiner. For these tests, we use a pair of ideal, controlled current sources with infinite output impedance and zero knee voltage as our transistor models. We define an arbitrary maximum operating voltage and a maximum operating current to enable us to define the Cripps load line [6] and corresponding required optimum impedance presented to the transistors, which in this context are biased and harmonically terminated such as to operate in class-B. With this setup, the transistors individually loaded with the required load impedance present efficiencies of $\eta = 78.5$ %, in accordance with theory. When loaded together with any of the following combiners, though, the total efficiency may drop as a result of load modulation, and is thus the subject of our following investigation.

For simplicity, these transistor amplifiers are denoted as simple transistors in the following figures, but should be interpreted as including the full supporting circuitry such as the harmonic terminations used to enable class-B operation in the simulation and so on.

2.3.1 Current summing junction power combiner

The simplest power combining topology consists of simple bridge between two separate transistor amplifier outputs as shown in Fig.2.2, or a variation thereof. This circuit exhibits the system efficiency map shown in figure 2.3. The efficiency maxima are obtained when either S_I, S_Q or both are fully enabled at once. This combiner or variations of it are often encountered in literature [8, 9, 10, 11, 12, 13, 14, 15].

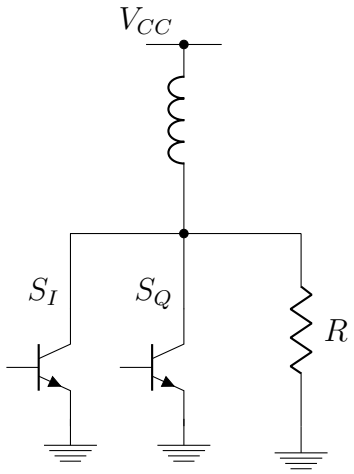


Figure 2.2: Simplified test setup for the current summing junction power combiner.

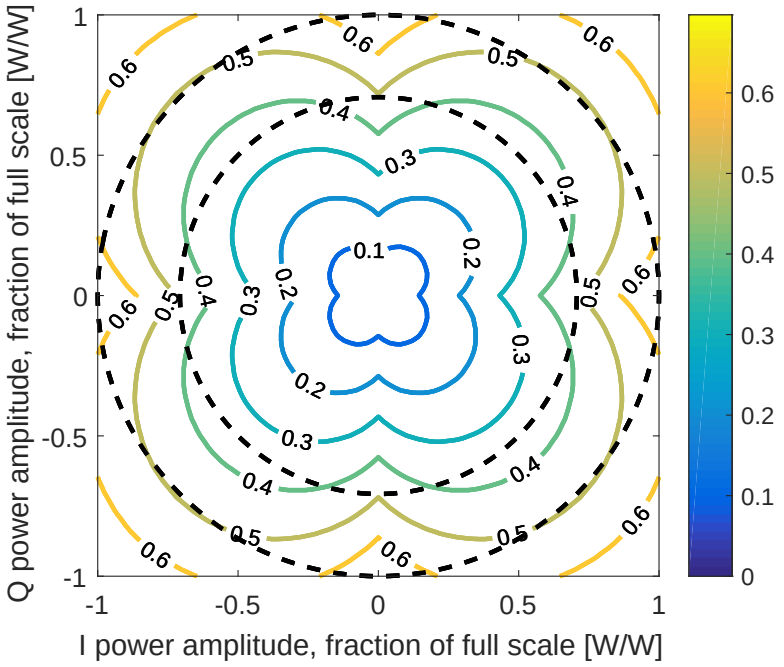


Figure 2.3: System efficiency across the IQ signal space when using a simple current summing junction as power combiner. The dashed circles represent -3 dB (outer) and -6 dB (inner) power backoff.

2.3.2 Wilkinson power combiner

The Wilkinson power combiner used as shown in Fig.2.4 is also often encountered in literature [16, 17]. It exhibits losses as described in the previous chapter, and therefore achieves a maximum system efficiency of 50 % as seen in Fig.2.5. An additional drawback to this approach is the bandwidth limitation inherent in its design.

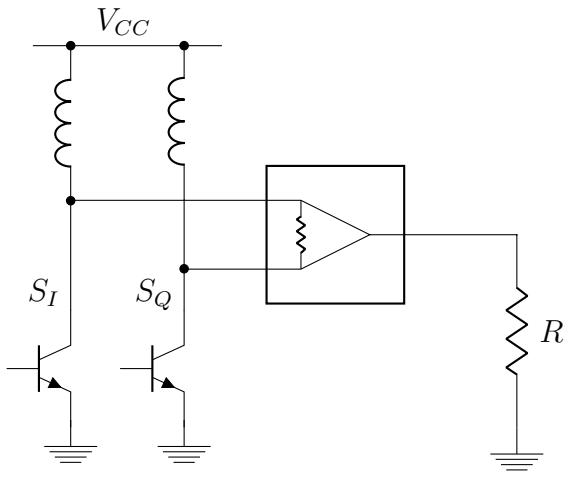


Figure 2.4: Simplified test setup for the Wilkinson power combiner.

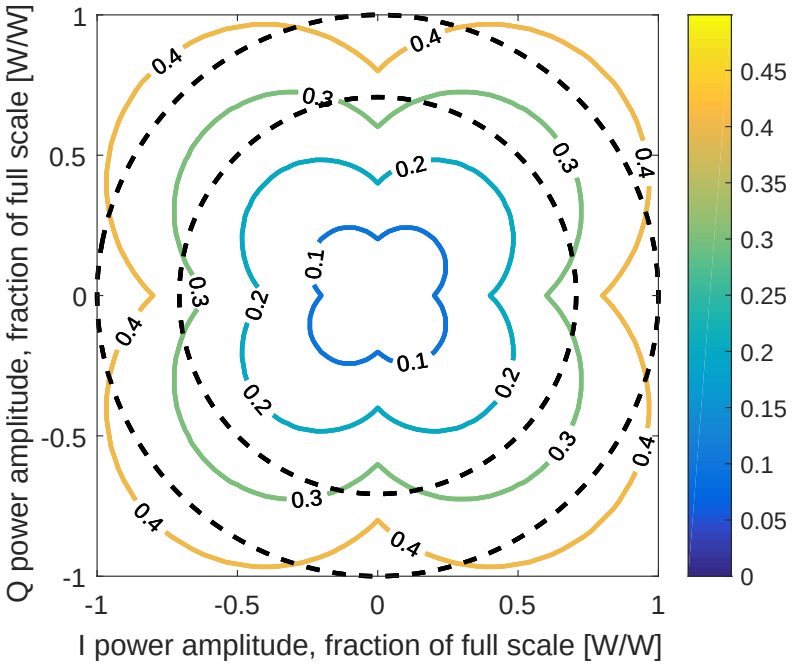


Figure 2.5: System efficiency across the IQ signal space when using a Wilkinson power combiner. The dashed circles represent -3 dB (outer) and -6 dB (inner) power backoff.

2.3.3 Purpose-built power combiner

Comparing a purpose-built power combiner (Fig.2.6) designed as explained earlier in this work with the presented power combining methods reveals its main benefits. As seen in Fig.2.7, the efficiency is close to unity at the S_I, S_Q and combined S_I and S_Q signal extremes. This makes the combiner especially well suited for QPSK modulators, in which the constellation diagram may overlap with the performance maxima seen in the circuit efficiency map. At backoff, the efficiency drops, but this drawback in applications such as LTE is mitigated by designing the combiner to

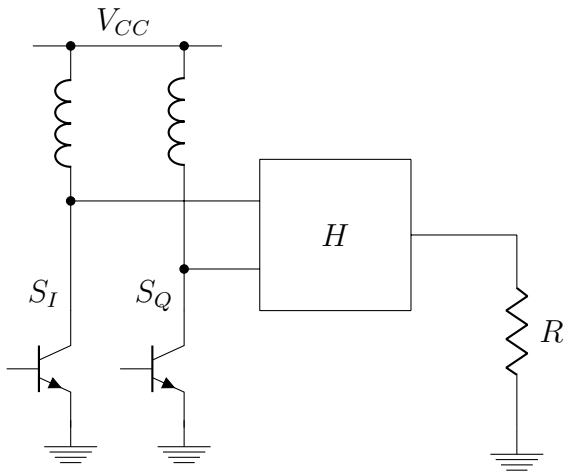


Figure 2.6: Simplified test setup for the purpose-built power combiner.

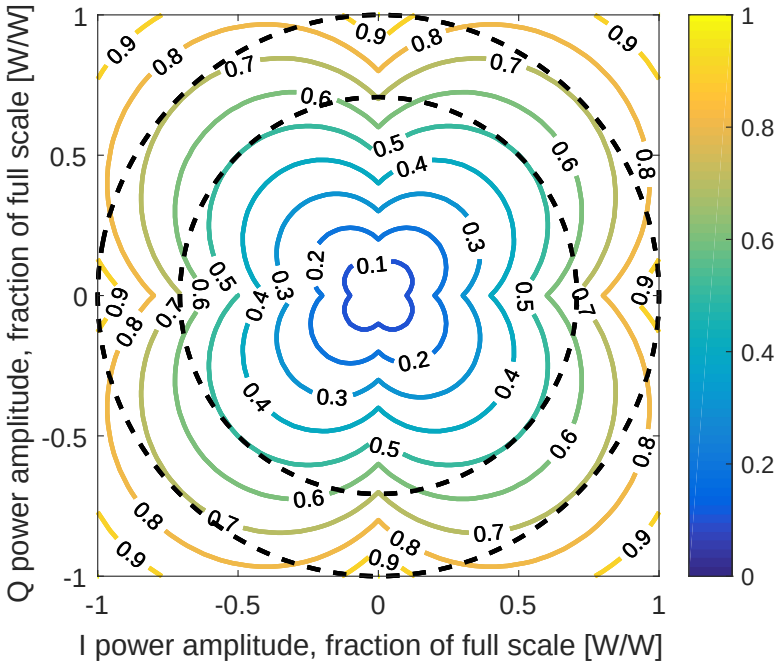


Figure 2.7: System efficiency across the IQ signal space when using a purpose-built power combiner. The dashed circles represent -3 dB (outer) and -6 dB (inner) power backoff.

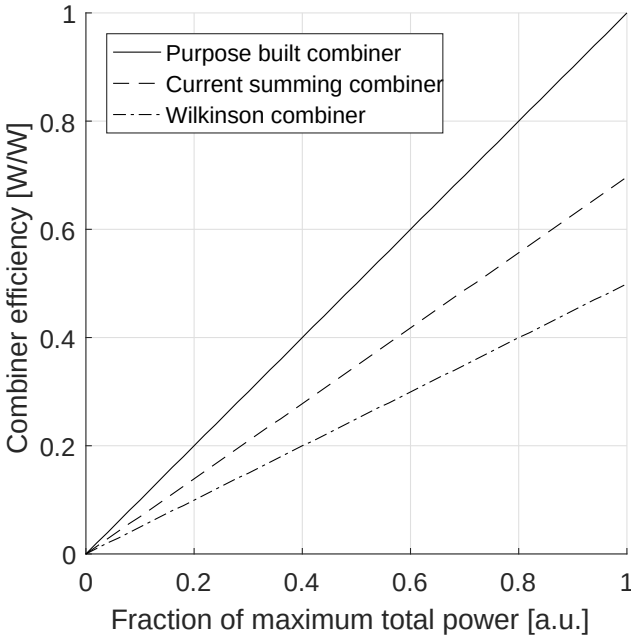


Figure 2.8: Comparison between three power combining methods.

present the impedances required at the average instead of the peak power levels. In this context it must be pointed out that the efficiency map obtained in Fig.2.7 arises if proper precautions have been taken to ensure that the S_I and S_Q always lead or lag each other, depending on choice at design of the combiner. Simply connecting the combiner to an I and Q signal source will lead to destructive interference if, say, $\angle S_I = 0°$ and $\angle S_Q$ changes from $\angle S_Q = 90°$ (leading) to $\angle S_Q = 270°$(lagging). This is understandable if we remember that the combiner circuit matrix was derived using a fixed phase relationship between S_I and S_Q, as we saw in section 2.1. We will return to this fact in section 3.5 in the next chapter.

2.3.4 Summary

To summarize the comparison between the investigated power combining methods, we can study a cross section of the efficiency maps presented above. In Fig.2.8, we see how the efficiency of the three investigated methods correlate with backoff power along the path of equal S_I and S_Q power. We see that the efficiency at maximum total power, corresponding to the corners in Fig.2.2, Fig.2.5 and Fig.2.7, is unity for the purpose designed combiner, a bit lower at 69.7 % for the current summing combiner and lowest with the Wilkinson power combiner, where the maximum total efficiency of 50 % also corresponds well to theory.

2.4 Combiner frequency dependency

As the purpose built combiner is designed for a specific center frequency, it is of interest to investigate its efficiency as function of deviation from this frequency. For this test, we use two sources operating at full power, corresponding to the corners in

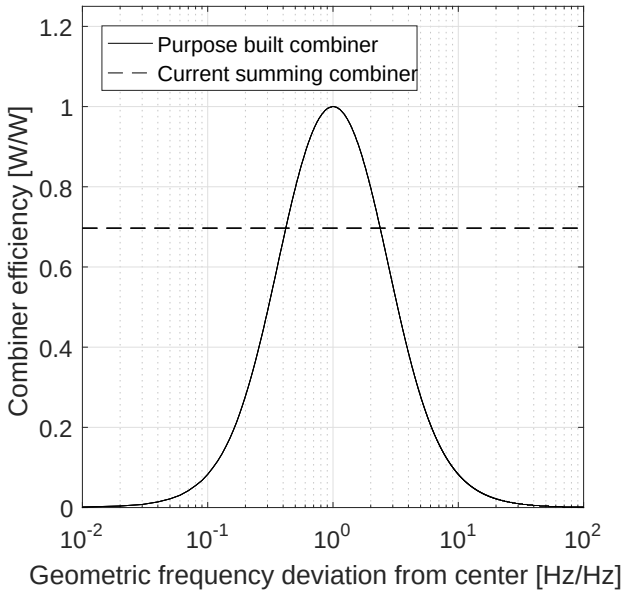


Figure 2.9: Frequency dependency of the purpose-built and current summing combiners.

Fig.2.7, and sweep the signal source frequency while observing the efficiency of the power combiner. In Fig.2.9 we see that there is an expected drop in the efficiency on either sides of the center.
The difference in efficiency between this combiner and the current summing junction combiner is less than 3dB, such that we can define its bandwidth as the region where it outperforms the latter. This is seen to be the case over the region $0.42f_C$ to $2.38f_C$ in Fig.2.9 and corresponds to a bandwidth of approximately $1.96f_C$.

2.5 Conclusion

Our pilot investigation confirms the underlying theory and shows that we can have good efficiency across all signal states in a typical QPSK modulator, although attempts at using the devised combiner in a QAM circuit will incur some performance penalty as shown above. Regardless, our findings do support further testing of the combiner in form of a practical circuit. Since the benefits of this circuit are especially desirable at higher operating frequencies, we will design a QPSK modulator targeting the E-band with the specifications given in Table 2.1, which should yield a circuit on par with or better than comparable designs (Table 5.1). The required bandwidth lies well within the capabilities of the power combiner as seen in Fig.2.9.

Performance characteristic	Value
Operation frequency range	71-76 GHz
Output power	$\geq$ 10 dBm
Bandwidth	$\geq$ 5 GHz
Supply voltage	$\leq$ 1.5 V

Table 2.1: Proof-of-concept chip design specifications.

Chapter 3

System Design

3.1 System overview

As seen in Fig.3.1, the complete QPSK modulator consists of a LO splitter network which splits the differential *LO* input signal into four phases, ϕ_0, ϕ_{90}, ϕ_{180} and ϕ_{270}, representing four copies of the LO signal phased 90° apart. These four signals are routed through buffers which drive the mixer transistors inside two mixer blocks.

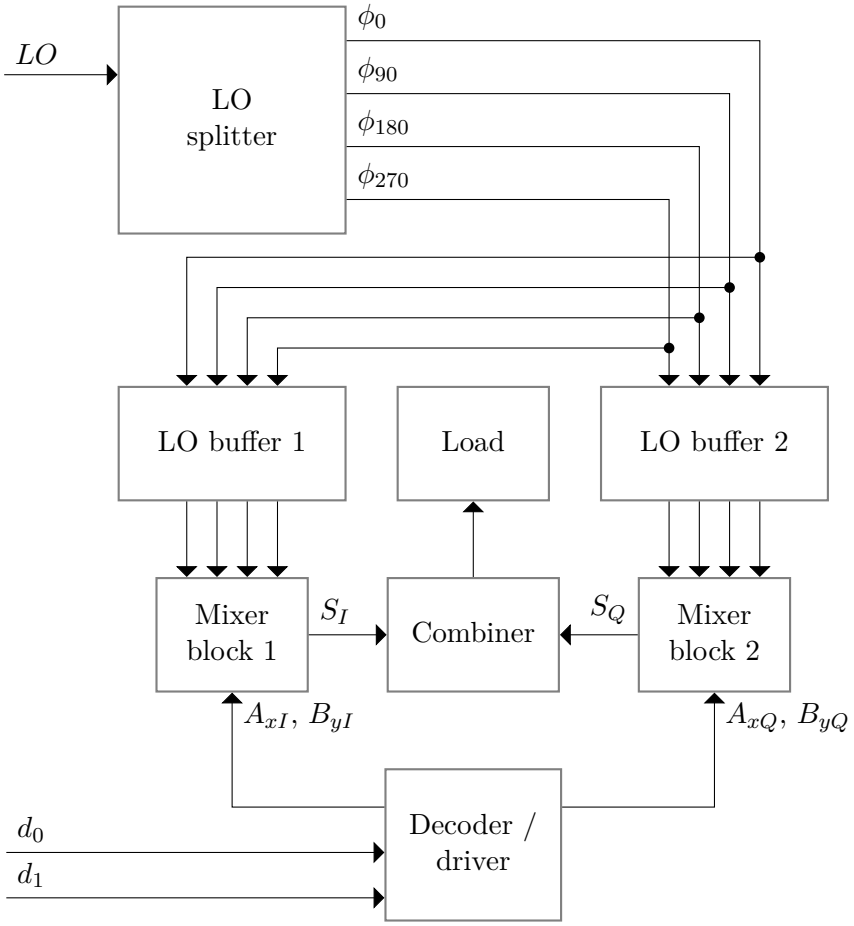


Figure 3.1: System block diagram. $x \in \{1, 2, 3, 4\}$ and $y \in \{1, 2\}$

These mixer blocks in turn generate the differential RF output signals termed S_I and S_Q, which drive the combiner network, and this combiner interfaces the load. As we saw in the previous chapter, the combiner network needs to be presented a pair of signals S_I and S_Q, which at all times have a fixed 90° phase relationship with respect to another. Driving the combiner with two mixers in the traditional manner as shown in Fig.1.1 would lead to problems with destructive interference between the signals, as explained in section 2.3.3. This issue is avoided by ensuring the proper relationship between the I and Q inputs of the combiner at all times. We do this by implementing a decoder circuit between the mixer blocks and data interface. This decoder translates the baseband data signals d_0 and d_1 into proper drive signals termed A and B, which in turn are used to drive the corresponding transistors in the mixer blocks as will be detailed in this chapter.

3.2 Integrated circuit design overview

Integrated circuit design is often associated with more degrees of freedom than design with discrete components, or the even more constrained off-the-shelf modules, circuits and even systems available and widespread within industry. This freedom, and the prospect of getting a different performance and feature profile than already available on the market comes at the cost associated with designing and taping out an ASIC.
The development of ASICs is costly both with regards to the software tools used in the design, the time needed to develop, simulate, validate and transfer any given design to production and of course, also the dreaded costs associated with the full mask set in a commercial design run. Furthermore, these expenses are even steeper in the most advanced process nodes.
This design was implemented in the B11HFC process from Infineon AG. This is a SiGe BiCMOS process optimized for use in RF and millimeter wave applications with an approximate maximum $f_T = 250$ GHz and a minimum feature size of 130 nm. The HBT transistors in this process are offered with several contact configurations, emitter lengths ranging from 700 nm to 10 μm in steps of 100 nm, and two fixed emitter widths of either 0.22 μm or 0.34 μm. The transistors are optimized for either speed, high voltage operation, or a third feature set between these two endpoints. In addition to the HBT transistors, the process also allows for fabrication of CMOS transistors suitable for both analog and digital circuitry.

3.3 The mixer block

Each of the two mixer blocks shown on either side of the combiner in Fig.3.1 consist of two Gilbert multiplier mixers and a differential pair allowing for switching between the two, as seen in Fig.3.4. The topology in its entirety corresponds to a traditional QPSK modulator, although we are not using it as such, but rather as a mixer where we can control the phase relationship between the LO signal and baseband signal it is being mixed with. One of the constituent Gilbert multiplier mixers is driven by the LO signal phases ϕ_0 and ϕ_{180} and the second one by the LO signal phases ϕ_{90}

and ϕ_{270}. By properly switching between these two mixers, the output of the mixer block can cover the entire QPSK signal space, as will be discussed in the following. Moreover, the blocks may do so while we ensure that the output from one of the mixer blocks always leads or lags the output of the other mixer block by 90° as discussed previously.

3.3.1 The Gilbert multiplier and its structure

Mixers can be realized in a variety of ways. In semiconductor technology at high frequencies, this is commonly done by employing the classic Gilbert multiplier shown in Fig.3.2. This circuit is extensively treated in all fundamental electronics textbooks (for instance [2, 3]), but we can also summarize its operation by considering its small-signal BJT equivalent as follows. The multiplier consists of two upper, cross-coupled differential amplifier circuits. The differential output voltage of the circuit is a superposition of the contribution from each of the two top differential pairs

$$v_{out,d} = v_{o+} - v_{o-} = g_{m1,2}R_c(v_{1+} - v_{1-}) + g_{m3,4}R_c(v_{1-} - v_{1+}) \tag{3.1}$$

Since the transconductances g_m are dependent on the collector currents I_c and approximated by $g_m \simeq I_c/v_T$ (by simplifying the classic Ebers-Moll model and considering only forward gain), with v_T being the thermal voltage, we can introduce the contribution from the lower differential pair, where $g_{m1,2} \simeq I_{c,5}/v_T = g_{m5}v_{2+}/v_T$ and $g_{m3,4} \simeq I_{c,6}/v_T = g_{m6}v_{2-}/v_T$, and thus

$$v_{out,d} = g_{m5}v_{2+}R_c(v_{1+} - v_{1-})/v_T + g_{m6}v_{2-}R_c(v_{1-} - v_{1+})/v_T$$

$$= g_{m5}v_{2+}R_cv_{1,d}/v_T - g_{m6}v_{2-}R_cv_{1,d}/v_T = g_mv_{2,d}R_cv_{1,d}/v_T = kv_{1,d}v_{2,d} \tag{3.2}$$

where we applied the substitution $v_{x+} - v_{x-} = v_{x,d}$, representing differential mode input voltage. The net result of these simple expressions shows a remarkable result, $v_{out,d} = kv_{1,d}v_{2,d}$, which represents a true arithmetic product of the differential input signals. The factor k can be calibrated out by selecting a collector load and adjusting the transconductance in the lower pair by biasing with a properly temperature compensated tail current. This ensures accurate multiplication over the same range of operating temperatures. Although (3.2) is true only for small-signal operation, it demonstrates how the Gilbert multiplier implements the arithmetic product of two signals. This operation extends to large-signal operation, save for added signal distortion which is not accounted for in our small-signal analysis.
The Gilbert multiplier is a doubly balanced mixer circuit, which exhibits rejection of both the baseband and LO input signals at the output. Moreover, the physical adjacency of the mixer components in an integrated circuit design ensures relatively good matching between them, both with respect to device performance and temperature effects, which is especially beneficial for the circuit performance in this respect. The possibility of using this circuit without transformers, such as needed in for example diode ring mixers also proves favorable in integrated circuit design, where large circuit size and good magnetic coupling are correlated, and thus both come at a premium.

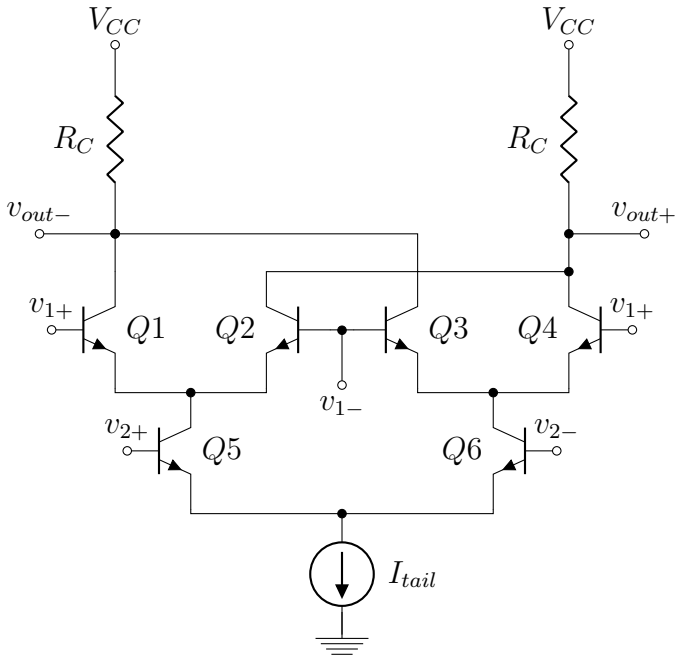


Figure 3.2: Gilbert multiplier.

3.3.2 Extending the Gilbert multiplier to a mixer block

In the previous chapter, we saw how the mixer blocks need to generate a specific RF signal pattern depending on the data input, to ensure that one input of the combiner always sees a signal that leads or lags the other combiner input by 90°. We achieve this by simply connecting two Gilbert multiplier mixers in parallel, as shown in Fig.3.4. The first mixer, consisting of transistors $Q1$-$Q6$ is fed with the LO signals ϕ_0 and ϕ_{180}, and the second mixer consists of transistors $Q7$-$Q12$, and is fed with the LO signals ϕ_{90} and ϕ_{270}. The upper A inputs allow for switching between either of the given signals ϕ_0 and ϕ_{90} and their inverses ϕ_{180} and ϕ_{270} at the outputs, and the lower B inputs allow for selecting between the mixers to be activated at the output. All inputs are thus differential, and the LO signals are amplified by transistors $Q1$-$Q4$ and $Q7$-$Q10$ which together with the tail current source operate in the linear region. The remaining transistors all operate as switches alternating between the cut-off and linear/saturation boundary regions of operation. This operating scheme achieves the lowest possible voltage drop across the switch transistors for a given collector current, as seen in Fig.3.3.
Switching between the two conduction states discussed above results in the LO signal being multiplied by either 1 or -1 when the baseband signal is applied to the A inputs, explaining the generation of the phase inverse, and a all-or-nothing selection between either of the two mixers when the signal is instead applied to the B inputs.

3.3.3 Transistor biasing

The HBT transistors exhibit different operation characteristics depending on their biasing. We are interested in high frequency operation, which is obtained by biasing the transistor with an emitter current corresponding to a current density of $J_{opt} =$

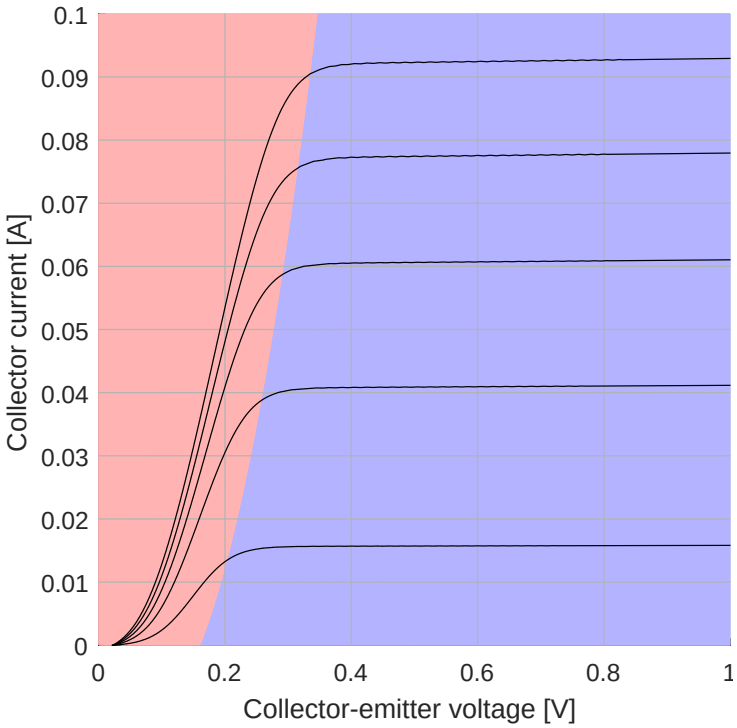


Figure 3.3: A typical family of transistor collector characteristic curves. The linear region is shaded red, and the saturation region blue.

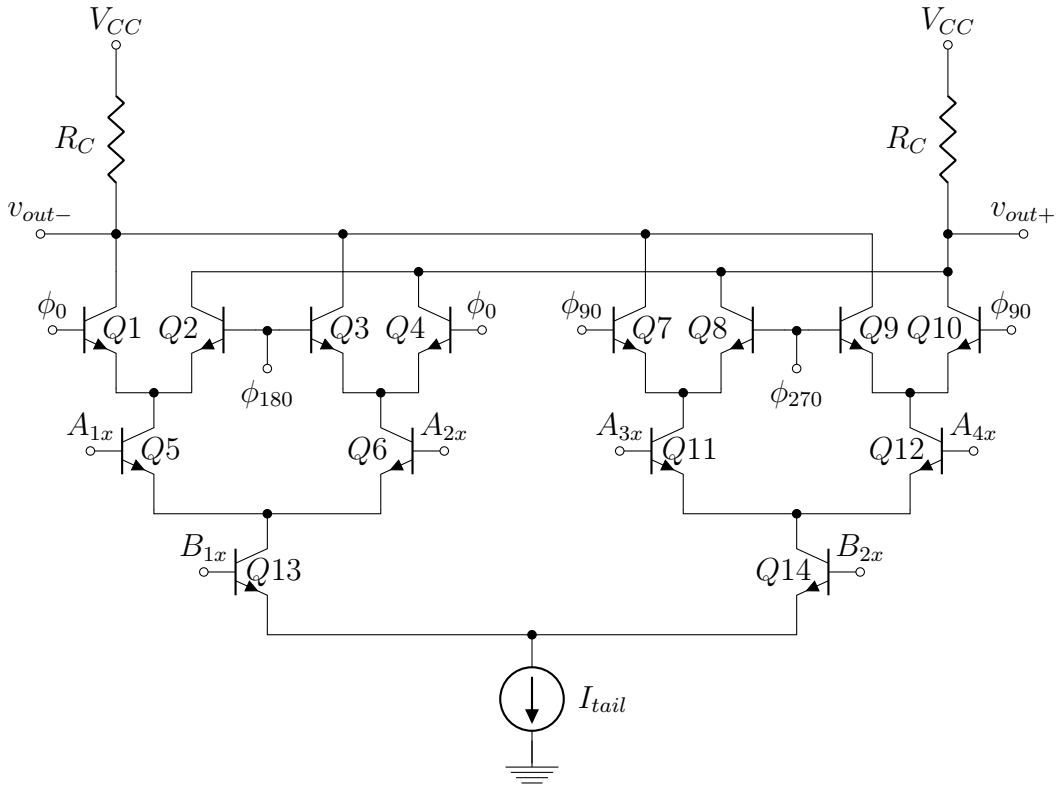


Figure 3.4: Simplified view of the mixer block. $x = \{I, Q\}$

11.5 mA/μm^2 of effective emitter area, as given in the process operation manual. The process user manual also identifies another current density of $J = 13$ mA/μm^2 associated with the maximum operating frequency of CML logic ring oscillators. This should be viewed as an upper bound for current density through any HBT transistor. For very high bias levels, there is a risk of avalanche breakdown in the strongly forward biased BE junction as well as impaired operation related to various phenomena such the Kirk effect. We therefore respect the target the current density J_{opt} throughout this design.

3.3.4 Tuned load dimensioning

The physical structure of the transistor is associated with an inherent capacitance which we can model, in its simplest form, as BE-, CE- and CB- capacitances. The familiar CB- or Miller capacitance limits high frequency voltage amplification. At high frequencies, sizeable currents may also flow through the BE- capacitance, lowering the power available to the transistor BE junction, and the CE- capacitances, lowering the otherwise large collector impedance at low frequencies. In our case, the total output capacitance of the gain transistors in the Gilbert multipliers can be estimated to approximately The small signal equivalent of the differential-mode half circuit of this arrangement is shown in Fig.3.6, and illustrates how the output capacitance C_{out} and the collector inductance L_C create a parallel resonant tank, thus also exhibiting an impedance maximum at resonance. In practice, this means that the reactances associated with these cancel each other out in our region of interest, and the collector load appears resistive, corresponding to the combination $R_L||r_o$ shown in Fig.3.6.
Another consequence of the inductive collector feed can easily be overseen. Current flowing through this inductor cannot instantly return to zero in the off-state transistor due to energy conservation. In this case, the current continues to flow through the load, and since the inductors in this situation remain connected to the load in series with the power supply, this circuit arrangement increases the effective supply voltage to

$$V_{CC,eff} = V_{CC} + L\frac{\mathrm{d}I_L}{\mathrm{d}t} \tag{3.3}$$

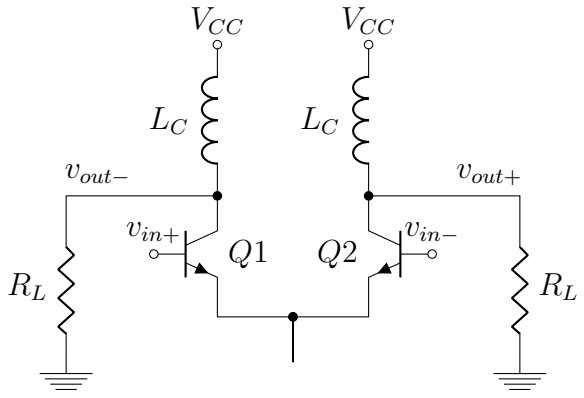


Figure 3.5: Inductive loading of a differential pair.

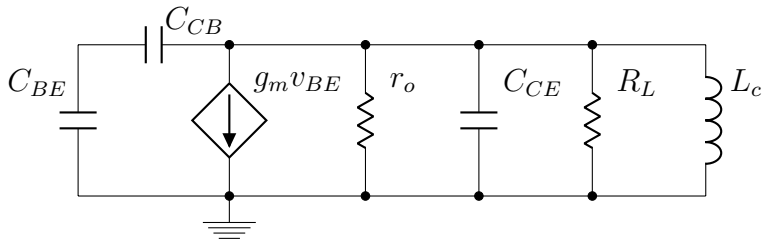


Figure 3.6: Small signal equivalent showing L_c effectively in parallel with C_{out}, the load resistance R_L and the transistor output resistance in the saturation region, r_o.

We can approximate this value by assuming the entire tail current I_{tail} is superimposed onto each inductor for exactly half of the baseband period, in effect creating a 50 % duty cycle boost converter as familiar from power electronics. In this case, for an ideal square wave switching profile and operation in the continuous conduction mode, we would have had an output voltage of

$$v_{out} = v_{in}M = v_{CC}\frac{1}{1-0.50} = 2v_{CC} \tag{3.4}$$

which is a convenient oversimplification in our case, but still proves useful to understand why and how the inductive loading works as it does, and perhaps even more so since it is so widely used for the very common task of decoupling RF circuits from their supplying DC power rails.
We select an initial value for these inductances by extracting the modelled output impedance of a transistor using the setup shown in Fig.3.7, where the leftmost component represents a network analyzer port. The transistor output capacitance is extracted from S-parameter simulations through the intermediate Z-parameters using the simple formula

$$C = \frac{-x_{11}}{2\pi f(x_{11}^2 + r_{11}^2)} \tag{3.5}$$

where $Z_{11} = r_{11} + jx_{11}$ and it is assumed that all output capacitance and resistance lie in parallel with each other without any additional series impedances. The initial inductor values are then found using $X_L = X_C/4$ (due to the four parallel transistor collectors present at each output) giving

$$L = \frac{1}{16(\pi f)^2 C} \tag{3.6}$$

and tuned according to simulation results.

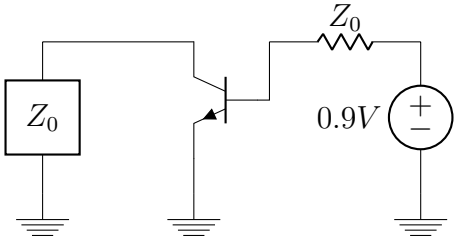


Figure 3.7: Transistor output impedance extraction setup.

3.3.5 Even-mode inductors

We have seen how the transistor output capacitance can affect its operation at high frequencies, and indeed, limit the device performance. There will always be some leakage of power to the emitters in the Gilbert cells, even in a presumably entirely symmetrical circuit. This may be due to both device mismatch and any level of common mode signal content at the inputs. This leakage to the tails of the Gilbert cells causes deterioration of their common mode rejection, and thus also in the appearance of stronger second order mixing products at the outputs. One way to address this problem is by adding an even-mode inductance L_{even} to the tail circuit as shown in Fig.3.8. The purpose of this is to set up a resonant circuit similar to the one we discussed in section 3.3.4, between the capacitance originating from the transistor emitters and present at the tails of the Gilbert cells and this added inductance. We can start here by simply assuming an equivalent capacitance equal to half of that found at the output of one transistor, and increase this value slowly in accordance with simulations, as this value turns out to have lower impact on circuit operation than does that of the output capacitance. This value is also more dependent on the operating points and the amount of common mode signal present at the tail node. The values of the even-mode inductance and the tuned collector loads are shown in the final circuit schematics, as seen in Fig.C.5.

3.3.6 Multiplexer structure

The mixer block is completed by adding two separate Gilbert multiplier mixers in parallel as discussed above and shown in Fig.3.4, and using a third differential pair $Q13$ and $Q14$ to switch between these mixers. The same result could have been achieved by using a separate multiplexer to switch between either of the LO phases ϕ_0 and ϕ_{180} or ϕ_{90} and ϕ_{270} to be presented to a single Gilbert cell multiplier mixer. This would have made the input to this multiplexer the equivalent of the B inputs in

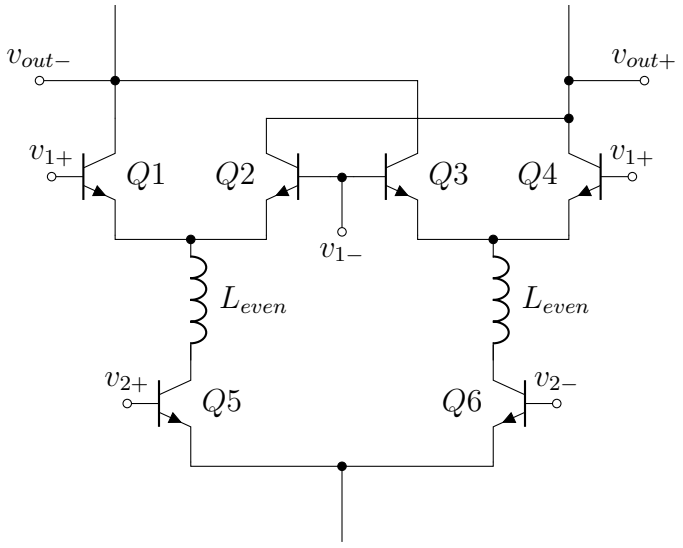


Figure 3.8: Addition of even mode inductors L_{even} to the Gilbert multiplier cell shown in Fig.3.2.

Fig.3.4, as well as eliminated the voltage drop across $Q13$ and $Q14$ from the design. Unless implemented as a CML gate as shown in Fig. 3.9 or similar, the problem with this approach would have been the need to simultaneously switch off the phases ϕ_0 and ϕ_{180} and to switch on the phases ϕ_{90} and ϕ_{270}, and vice-versa to avoid distorsion. Additionally, leakage through the off-state multiplexers and insertion loss in the on-state multiplexers would have compounded the problem. The MOSFET transistors included in the process we use in this work are severely limited for operation at the required LO frequencies and power levels. On the other hand, a CML multiplexer using HBT transistors may have have been a good alternative, albeit at the cost of the additional static current dissipation through such a multiplexer gate.
By using the transistors $Q13$ and $Q14$ with two separate Gilbert multiplier mixers (Fig.3.4), we avoid these problems while also simplifying the driver circuitry needed at the cost of the additional V_{CE} voltage drop across these two transistors. This voltage drop, on the order of 100 mV, constitutes a significant fraction of the voltage headroom available at the output in a low voltage design, and complicates a definitive a priori assessment as to which of the two discussed approaches would be optimal from the point of view of power output. Our choice of switching between the LO pairs by steering tail current in two separate Gilbert multiplier mixers is arguably simpler to design with, such that we chose to continue with this approach.

3.3.7 Mixer block biasing

We discussed the impact of correct circuit biasing previously. The probably easiest way to correctly bias the entire mixer block is to first select a target tail current in accordance with the output power requirements and available output voltage headroom, and simply set this current using a tail current source. The main requirements

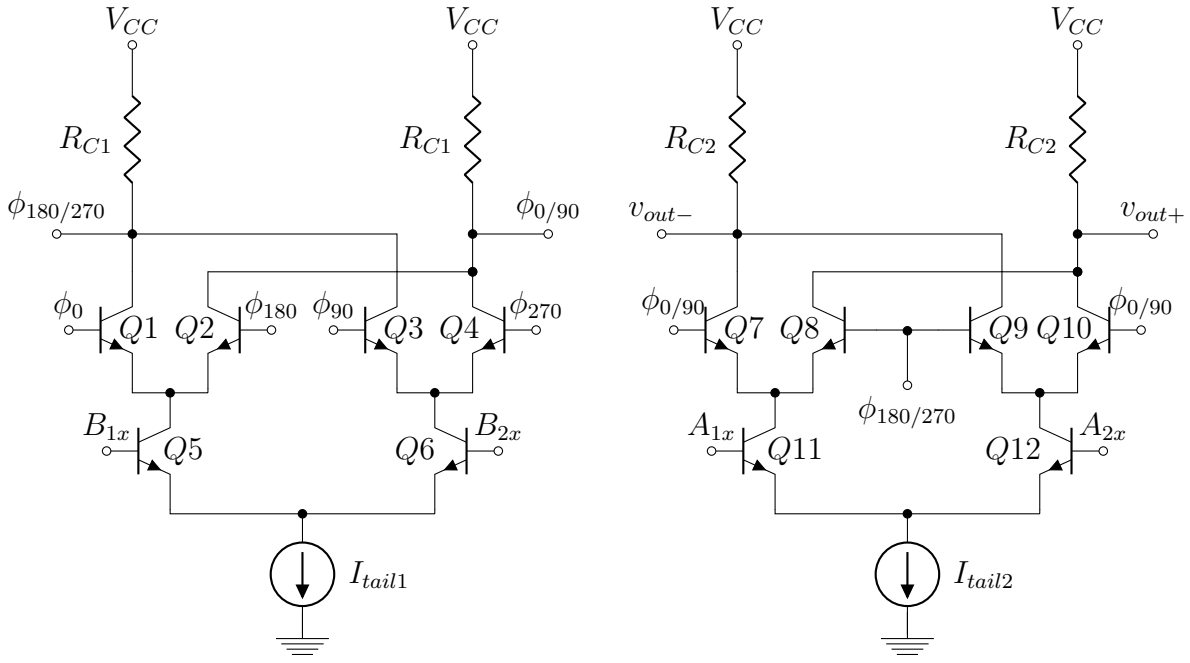


Figure 3.9: Alternative mixer block design with separate CML driver. $x = \{I, Q\}$

on this current source is as small an associated voltage drop across it as possible and that it stays in the saturation region (blue region in Fig.3.3) at all times in order to maintain as high an output impedance as possible. The voltage drop across the transistor in this current source is inversely related to its emitter area. Increasing the transistor size comes at the cost of increased parasitic output capacitance, which deteriorates performance at high frequency. Luckily, we do not need this source to perform very well in the dynamic operation mode, as needed if it were operating as an active load, but merely provide the mixer block above a correct static bias. We can thus use a relatively large transistor, and we select it some 2-3 times larger than the other transistors above. We need to accept some voltage drop across it anyway, to maintain the condition of operation in the saturation region across some hundred mV V_{CE} variation.
By now, all collector currents in the mixer transistors are determined by the tail current source. We need to set correct base bias to complete the biasing. The simplest way to achieve this is by using resistive biasing networks designed using the transistor base to collector transfer characteristic curve of each transistor. In this work, we chose to bring out these bias nets off chip through decoupling inductors to allow for fine tuning with external sources.

3.3.8 Practical mixer block design procedure

The target output power was specified as 10 dBm or more, so we can settle for a design where each of the two Gilbert multipliers in the mixer block are sized for an output power of approximately 7-10 dBm. By selecting a proper mixer tail current of 32.5 mA, we can reach an output power close to the upper bound of this requirement over a range of load resistances. Over this range, a tradeoff between absolute output power and power gain needs to be made, and the source impedance, upon which both are also dependent, taken into consideration. We can define a figure of merit as the product between the power gain and output power. This figure is then optimized by iteratively performing sweeps of the source power, source and load impedance. We get optimum values for a source impedance of $10{+}1.77j\ \Omega$ (single ended), and load resistance of 105 Ω (differential) with load inductors of 27 pH. These values give a power gain of 10.9 dB for an input power of -1.4 dBm and a corresponding output power of 9.5 dBm, which lets us reach our design goals in the finished mixer block while also providing good power gain, mitigating the requirements on the local oscillator block.
Transistors with a CBEBEBC contact configuration and 0.22 μm emitter width are selected in the mixer output stage and the optimum size is

$$32.5\ \text{mA} = 2 \cdot (L - \Delta) \cdot (0.22\mu - \Delta) \cdot 11.5\ \text{mA}/\mu m^2$$

which gives an optimum length of $L = 9.5$ μm when adjusting for effective emitter size with the $\Delta = 0.07$ μm linear terms. The switching stages consist of 10 μm long CEBEC transistors at the A stage (cf. Fig.3.4) and 2x10 μm long CEBEC composite transistors at the B stage. This choice yields a B stage base capacitance approximately double that of the A stages above, in which pairs of two bases are attached together and driven by the same driver output in the finished modulator.

This ensures the RC time constants associated with the nodes at the A and B stages are approximately equal. Finally, the tail source consists of a 3x10 μm CBEBEBC composite transistor.
The iterative optimization steps above also allow us to include even-mode inductors with values of 20 pH at the output stage transistor tails for some speed improvement, as well as define correct base bias voltages for the transistors in the circuit, which are saved for subsequent use in the design of the base driver circuitry.

3.4 The output power combiner

3.4.1 Circuit parameter synthesis

The design and theory behind the combiner has been discussed previously. In the final design, we use a Wolfram Mathematica® script (see Appendix B.1) to calculate the values required for the combiner at a given frequency and set of input and output impedances. We generate the differential form of the combiner by simply mirroring the circuit resulting from the single ended design across the ground plane and simplifying the circuit as required.
We thus generate a combiner circuit matrix for a circuit with 52.5 Ω (single ended) source and 25 Ω (single ended) load resistance, and feed this to a MATLAB script calculating the required component values. These are merely entered in the circuit simulator schematic capture tool in order to complete the design, which should provide 105 Ω (differential) loads to each of the two mixers and present a 50 Ω (differential) output to an equally sized load.
Finally, we use this combiner to couple power from the two I and Q mixer blocks to the output load. The form of the final combiner is shown in Fig.4.5.

3.5 The decoder/driver block

We saw in the second chapter how the combiner performs as intended when the input signals do not violate the assumptions under which it was derived. One input must always lead the other input by 90°. In practice, we achieve this by properly enabling and disabling phases in each of the two mixer blocks. This is achieved using a decoder block as shown at the bottom of Fig.3.1, translating the data inputs to proper A and B signals driving the switch transistors in each mixer block. We now want to devise the logic function which maps the four distinct data bit states to these correct output phase combinations, and we can use the logic truth table shown in Table 3.1 to achieve this. We have arranged the signal outputs from the two mixer blocks, S_I and S_Q, respectively, in a manner that ensures that S_Q always leads S_I by 90°. Which of the signals actually leads or lags is a notational choice and irrelevant for circuit operation as long as we design the combiner accordingly and respect our choice when decoding the data at the receiver. We have extended the A and B signal line indices in each of the the two mixer blocks with the additional indexing I or Q subscripts to denote the corresponding signals of the respective side.

ϕ	S_Q	S_I	d_0	$\overline{d_0}$	d_1	$\overline{d_1}$	A_{1Q}	A_{2Q}	A_{3Q}	A_{4Q}	A_{1I}	A_{2I}	A_{3I}	A_{4I}	B_{1Q}	B_{2Q}	B_{1I}	B_{2I}
1	0°	270°	0	1	0	1	1	0	x	x	x	x	0	1	1	0	0	1
2	90°	0°	0	1	1	0	x	x	1	0	1	0	x	x	0	1	1	0
3	180°	90°	1	0	0	1	0	1	x	x	x	x	1	0	1	0	0	1
4	270°	180°	1	0	1	0	x	x	0	1	0	1	x	x	0	1	1	0

Table 3.1: Mixer block truth table

We can also see the relationship between the data inputs $d_0/\overline{d_0}$ and $d_1/\overline{d_1}$ and the required output signals in Table 3.1. Applying the don't care conditions indicated by crosses in the table allows us to tie the signals A_{1I} and A_{3I} together. We do the same with A_{2I} and A_{4I} and correspondingly on the Q side by tying together A_{1Q} with A_{4Q} and A_{2Q} with A_{3Q}. This yields the reduced truth table shown in Table 3.2.

ϕ	d_0	$\overline{d_0}$	d_1	$\overline{d_1}$	$A_{1Q}\|\|A_{3Q}$	$A_{2Q}\|\|A_{4Q}$	$A_{1I}\|\|A_{4I}$	$A_{2I}\|\|A_{3I}$	$B_{1Q}\|\|B_{2I}$	$B_{2Q}\|\|B_{1I}$
1	0	1	0	1	1	0	1	0	1	0
2	0	1	1	0	1	0	1	0	0	1
3	1	0	0	1	0	1	0	1	1	0
4	1	0	1	0	0	1	0	1	0	1

Table 3.2: Reduced mixer block truth table

At this point we observe how the required decoder block can be realized in its entirety using buffers, inverters and proper signal routing. If we use differential logic, both a buffer and an inverter can be realized within one single gate, as will be shown in section 3.5.1, and thus this decoder block is easily implemented.

3.5.1 The Inverter/buffer gate

The simplest way of realizing a logic inverter gate in B11HFC would be the standard static CMOS approach, using the MOS transistors provided with this process. The main drawback with such an approach is the speed limitation inherent in voltage mode designs such as is the case with static CMOS. A common way of increasing this speed is by implementing so-called current mode circuits, where the signals of interest are conveyed by currents instead of voltages. In ideal current mode circuits, the node impedances and voltage swings both tend to zero, as opposed to voltage mode circuits, where the node impedances tend to infinity and node currents to zero. Albeit a cursory explanation, the speed increase associated with a current mode design can be intuitively understood as a result of the lower associated node impedance reducing the effective node time constant RC.
The simplest differential current-mode logic gate is the resistively loaded inverter/buffer gate shown in fig 3.10. The current source at the tail of the differential pair biases the circuit and sets the quiescent common mode voltage at the outputs

$$V_{out,cm} = R_C \left(\frac{V_{CC}}{R_C} - \frac{I_{tail}}{2} \right) = V_{CC} - \frac{1}{2} I_{tail} R_C$$

where it is assumed that there is no resistive DC path to ground through Z_L for notational convenience.

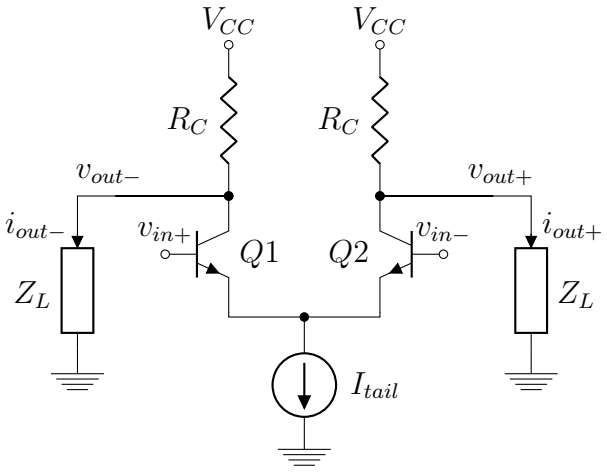


Figure 3.10: The most simple current mode gate.

Since this circuit exhibits the usual inverting effect at the collector of the same transistor as any given input, as well as a non-inverting characteristic at the collectors of any transistor with respect to the input on the opposite side, the gate can be used as both buffer and inverter depending on the our choice of output polarity. Since we will be driving another set of differential pairs in the mixer block with these gates, we need to determine the voltage excursion needed for commutation of a differential pair circuit. Referring to Fig.3.10, and approximating the large signal collector current through the transistors using the simplified version of the well known Shockley diode equation,

$$I_C = I_S e^{V_{BE}/\eta V_T}$$

we can solve the nodal equations of this circuit, and end up with

$$V_{C1/C2} = V_{CC} - \frac{I_T R_C}{\frac{I_{S2/S1}}{I_{S1/S2}} e^{\frac{V_{in-/in+} - V_{in+/in-}}{\eta V_T}} + 1}$$

where Z_L in the figure is neglected. Plotting the differential output voltage, $\pm(V_{C1} - V_{C2})$ as function of the differential input voltage $\pm(V_{in+} - V_{in-})$ at two operating temperature extremes, as seen in Fig.3.11, reveals that we need only approximately ± 200 mV to fully commutate across the entire range of operating temperatures between these extremes.

3.5.2 Delay tuning

Circuits with differing gate sizes along their various signal paths may need delay tuning to compensate for different group delays associated with unequal RC time constants in each of the paths. The very simple logic needed in this circuit is not associated with significant skew, such that delay tuning is not needed either.

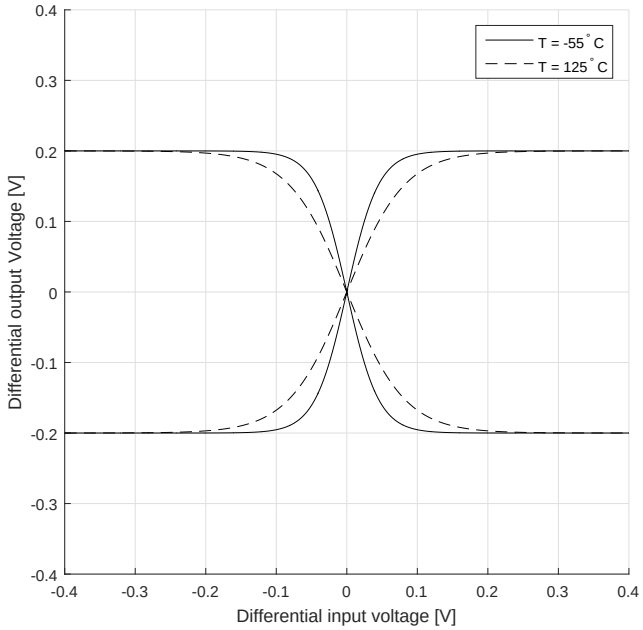


Figure 3.11: A CML gate with $I_T = 5$ mA, $R_C = 40\ \Omega$ and $\eta = 1.2$ commutates fully with an input voltage of ± 200 mV across a wide range of operating temperatures.

3.6 Auxiliary components

3.6.1 Overview of the LO splitter network

The modulator block is designed to be fed with a differential LO signal terminated into 50 Ω(single ended). The signal is routed through a phase shifter and splitter block shown as the LO splitter block in the upper left corner in Fig.3.1. This block is based on quadrature power splitters (as shown in Fig.3.14) arranged in a differential setup, thereby creating two signals phase offset 90 degrees with respect to each other. The power splitters are implemented with lumped components and followed by the emitter followers that buffer the LO signals further before feeding the mixers.

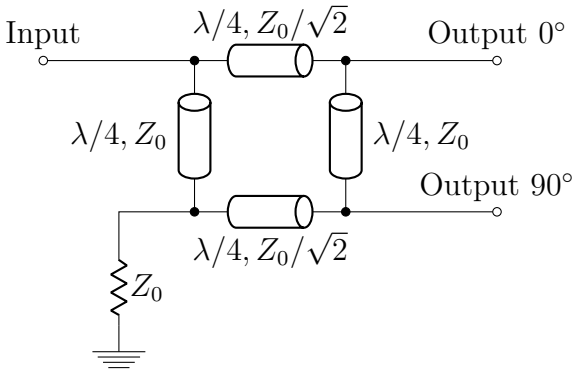


Figure 3.12: Generic quadrature power splitter based on a 90° hybrid.

3.6.2 The quadrature power splitter

We can design the quadrature power splitter with lumped components by introducing a first order approximation of a short transmission line segment using three impedances arranged in a π-network as shown in Fig.3.13b. This network and its associated impedance or admittance matrices can be transformed into a transfer parameter matrix and equated to the transfer parameter matrix of a short transmission line segment, as shown in (3.7).

$$T_{TL} = \begin{bmatrix} \cos(\beta l) & jZ_0 \sin(\beta l) \\ j\sin(\beta l)/Z_0 & \cos(\beta l) \end{bmatrix} = \begin{bmatrix} 1 + \frac{Y_B}{Y_C} & \frac{1}{Y_C} \\ Y_A + Y_B + \frac{Y_A Y_B}{Y_C} & 1 + \frac{Y_A}{Y_C} \end{bmatrix} \tag{3.7}$$

The values of the components subscripted A,B and C in Fig.3.13b can thus be approximated by the following expressions

$$L_C = \frac{Z_0 \sin(\beta l)}{2\pi f} = \frac{Z_0}{2\pi f} \tag{3.8}$$

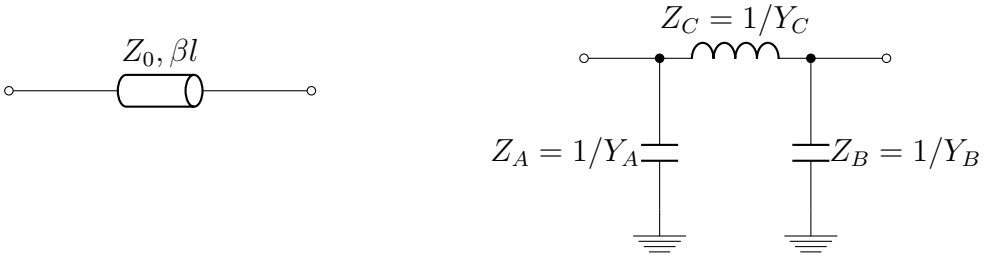
$$C_x = \frac{1 - \cos(\beta_x l)}{2\pi f Z_{0,x}} = \frac{1}{2\pi f Z_{0,x}} \qquad x \in \{A, B\} \tag{3.9}$$

where we used the fact that $\beta l = \pi/2$ in all segments of the quadrature hybrid. We can use this to find the following design equations of a general lumped element first order approximation of a quadrature network as shown in Fig.3.14.

$$L_1 = \frac{Z_0}{2\pi f} \tag{3.10}$$

$$L_2 = \frac{Z_0}{2\sqrt{2}\pi f} \tag{3.11}$$

$$C = \frac{1 + \sqrt{2}}{2\pi f Z_0} \tag{3.12}$$



(a) A transmission line segment with characteristic impedance Z_0 and electrical length βl.

(b) Lumped element approximation of the transmission line segment shown in Fig.3.13a.

Figure 3.13

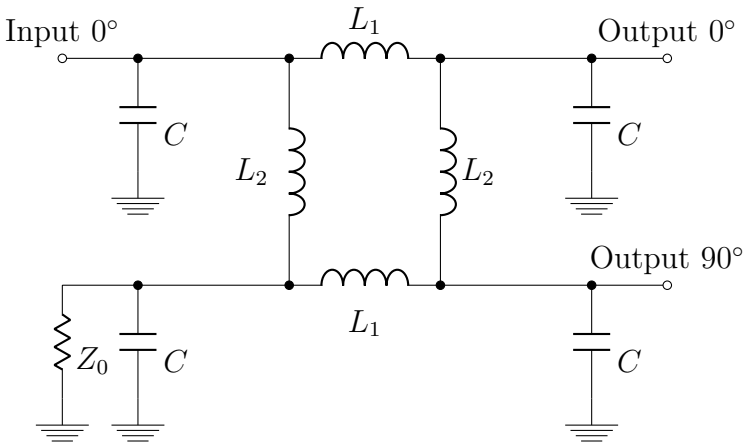


Figure 3.14: Lumped element quadrature power splitter.

3.6.3 LO driver impedance matching

The outputs from the LO distribution network are impedance matched to the Gilbert multiplier pairs using emitter followers in the LO buffer blocks shown in Fig.3.1. The required source impedance to be presented to the mixers is estimated by load-pull sweeps of the nearly finished mixer block, optimizing the circuit for output power and efficiency. The resistive part of this impedance is generated by the effective combination of the resistor R_E and the emitter resistance $r_E \simeq 1/g_m$, and the reactive part generated through a suitable inductor X_L connecting the emitter of the impedance converter stage with the base of the driven transistor.

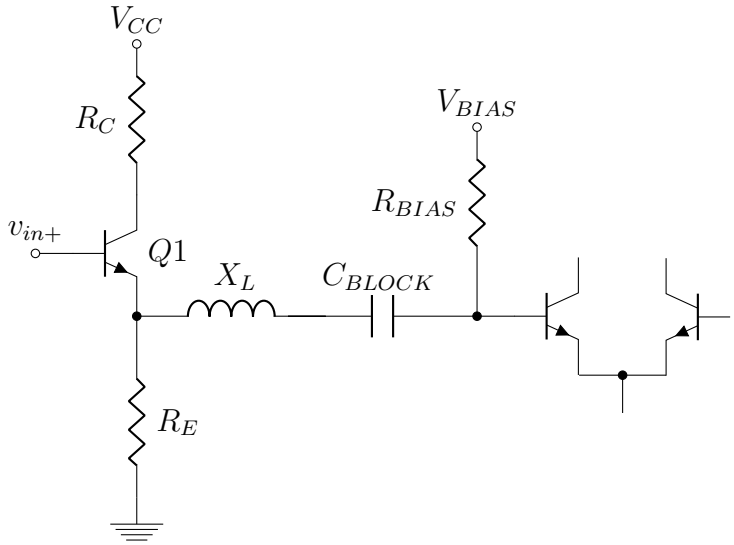


Figure 3.15: Active impedance converter.

Chapter 4

Results

4.1 Mixer block performance

The two mixer blocks needed for a complete modulator were designed according to the discussion in the previous chapter. As a full circuit layout was not in the scope of this work, the design optimization was done without considering parasitics. The impact of these is discussed in the next chapter along with other factors of importance at tape-out.

4.1.1 Output stage power gain

The output stage was optimized with respect to the figure of merit we defined in the previous chapter as the output power-power gain product. We see in Fig.4.1 how this figure depends on the LO input power as well as the operating frequency. By individually plotting the output power and power gain as functions of input power and LO frequency in Fig.4.2a and Fig.4.2b, respectively, we can clearly see a tradeoff between these parameters. At this stage, we can choose an input power of -2 dBm

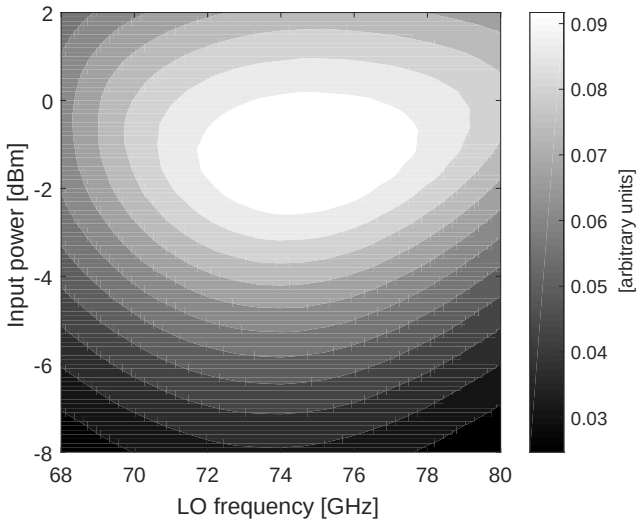
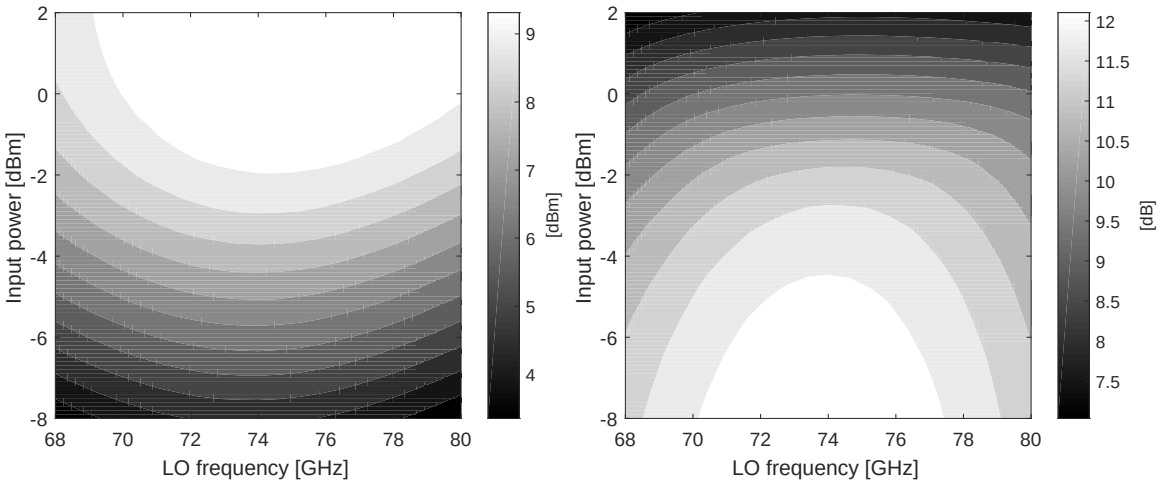


Figure 4.1: The output power-power gain product as function of input power and LO frequency.



(a) Output power (dBm). **(b)** Power gain (dB).

Figure 4.2: The output power and power gain of the output stage as function of LO frequency and LO input power.

using the figures above, which over the range of operating frequencies gives a good tradeoff between circuit output power and power gain, as shown in Fig.4.3. For this input power, we see that the circuit power gain is better than 10 dB and the output power is better than 7 dBm across the range of operating frequencies. The latter fact ensures that the modulator output power will be better than 10 dBm when we combine power from two individual mixers in the final modulator using the nearly lossless combiner we've discussed in this work. The 1 dB compression point of the modulator is P1dB = -2.5 dBm referred to the input; the output power as function of input power for $f_{OP} = 75$ GHz can be seen in Fig.4.4.

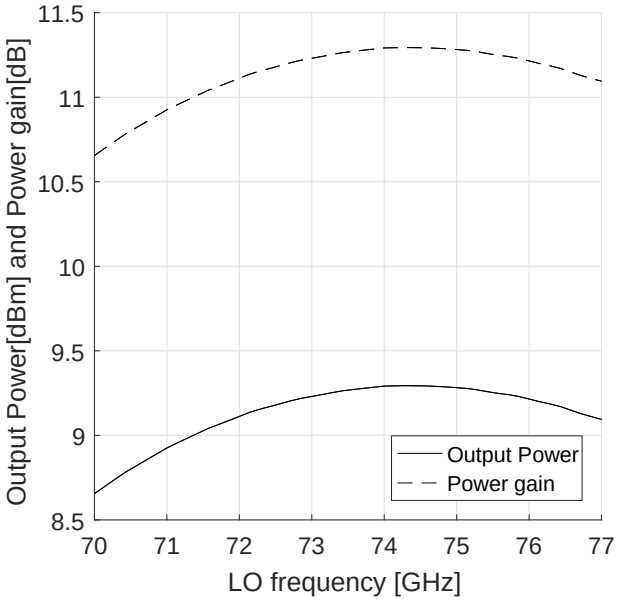


Figure 4.3: Output power and power gain of the mixer output stage as function of LO frequency with a fixed LO input power of -2 dBm.

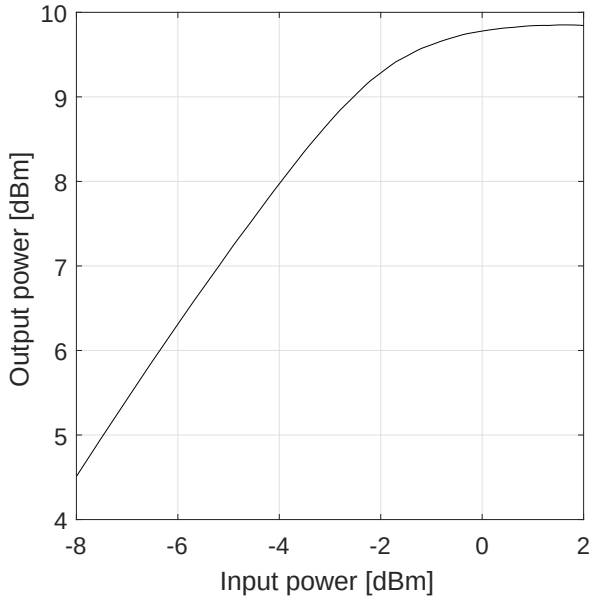


Figure 4.4: The output power as function of input power for $f_{OP} = 75$ GHz.

4.1.2 LO input matching network

The matching between the LO clock splitter and the mixers is performed using emitter followers such as described in last chapter. A quiescent current of approximately 2 mA was chosen on the basis of computer simulations.

4.1.3 Power consumption

The mixer circuit power consumption is determined by the supply rail voltage and its quiescent current, as this current flows through the mixer at all times. The static consumption of one mixer is thus simply

$$P_{mixer} = (V_{CC} - V_{EE}) \cdot I_{tail} = 44.5 \text{ mW}$$

The efficiency of the mixer circuit is not too meaningful to calculate at this point though, as the base driver circuitry consumes a significant fraction of the static power, and thus must be included in these considerations, as we will see shortly.

4.1.4 Mixer block summary

The mixer circuit in this work is designed mainly under the constraints of output stage power. In other designs, the linearity of the Gilbert multiplier structure may take precedence over this constraint. We chose to largely ignore this part of the mixer in this design with the assumption that the corresponding transistors operate strictly between the linear region and cutoff, such that all tail current flows through one transistor in the A and one in the B stages at all times. As such, and as far as the load is concerned, the mixer block appears as one single, active differential pair stage with three other "silent" differential pair stages (or rather, the equivalent of their output impedances) in parallel. The mixer block performance satisfies the requirements set on power gain and output power in the design criteria.

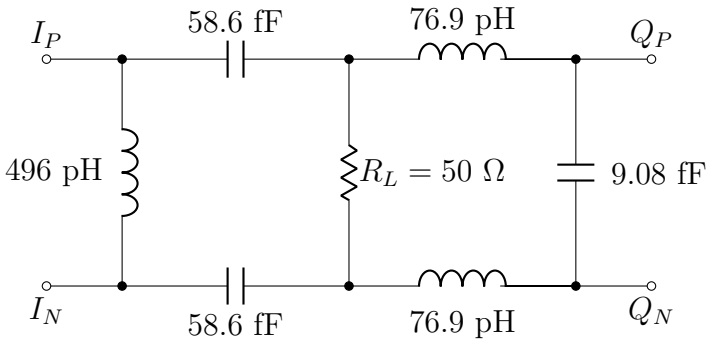


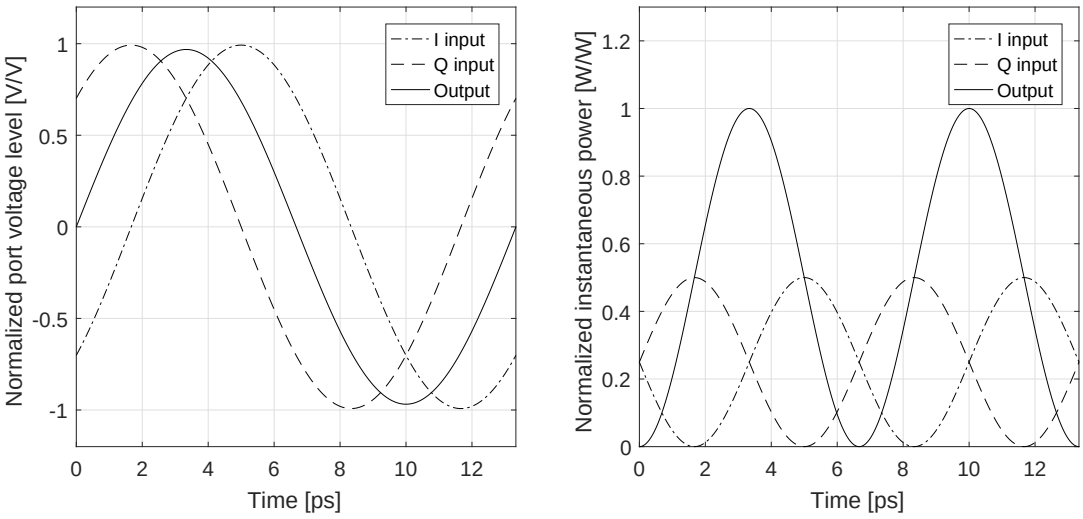
Figure 4.5: Circuit topology and component values for a power combiner with the specifications discussed in the text.

4.2 Combiner performance

Our design mandates the use of a load resistance of 105 Ω (differential) at each mixer block, and moreover, we want to drive a 50 Ω (differential) load with the combiner (Fig.4.5). Following the previously discussed design procedure, the following circuit suits these needs over our range of operating frequencies.

The function of this circuit is easily tested with a time domain transient simulation which confirms valid operation (Fig.4.6). The small losses in the circuit are associated with effective series resistance intrinsic to the circuitry).

In Fig.4.5 we also see that the output DC potential is referred to that present at the quadrature signal ports. If galvanic isolation is needed, blocking capacitors, transformers or other forms of isolation may be implemented as required, although this can also be done off-chip. We did not proceed further with specifying details concerning this aspect of the circuit.



(a) Instantaneous port voltage. **(b)** Instantaneous port power.

Figure 4.6: Normalized instantaneous port voltage and power levels as function of time.

4.3 Logic block performance

4.3.1 Speed

We saw in the previous chapter how, due to the RC time constants associated with switched nodes, there is a direct tradeoff between the maximum operating frequency of a CML gate and the minimum possible bias current, which also sets the power consumption of the gate. We used a bias current of 5 mA as a compromise between power consumption and commutation speed. With collector resistors of 40 Ω, this provides the voltage swing required to drive the differential pairs in the mixer. The rise and fall settling times of the circuits under these constraints are 29 ps and 25 ps, respectively, and operation under load shown in Fig.4.7. The trace shows the voltage at one of the driver outputs (single-ended output). The differential output voltage is thus better than the required ±200 mV at a switching frequency of 5 GHz. The settling time, i.e. the sum of the rise and fall times, also limits the upper modulation frequency to approximately 18 GBaud, although the modulator would be very inefficient operating at these speeds, as most of the cycle time would be spent with the mixer transistors operating in the linear regions, effectively limiting gain and thus output power. Accepting an effective 30% of the cycle time in the settling region gives an operating baseband data rate limit of 5.5 GBaud. We used a baseband data rate of 5 GBaud (10 Gbps) in the simulation tests shown in this chapter.

4.3.2 Power consumption

Since we settled for a simple current-mode logic gate design, the power consumption is static and fixed at

$$P_{gate} = (V_{CC} - V_{EE}) \cdot I_{tail,CML} \simeq 6.3 \text{ mW}$$

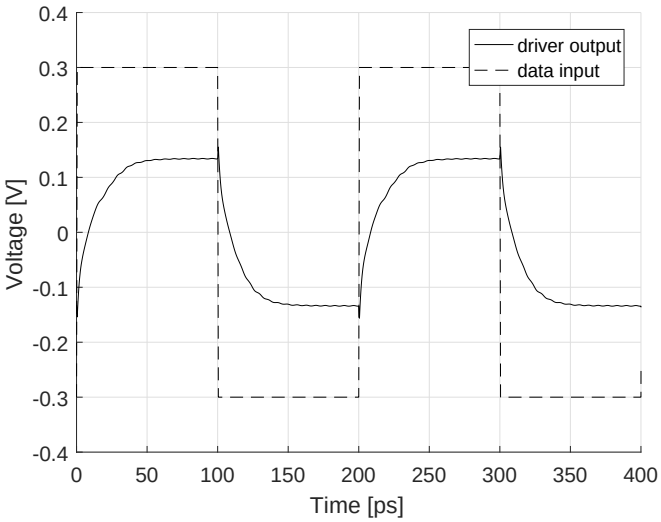


Figure 4.7: The driver output voltage (single-ended) waveform (solid trace) as function of driver input data (dashed trace).

where $I_{tail,CML}$ is the gate tail current driven by a current source. Note that the power consumption in the mirror reference branch is not included in this figure, although it can be minimized by sharing this branch among several current sources and dimensioning the circuit such as to make use of the current multiplication available in its translinear loops. The mixer circuit base bias is determined by the supply voltage of the base driver bases, which again is tuned according to the V_{CE} voltage drops across the other transistors at the emitter of any of the driven transistors, and the required V_{BE} voltage at the driven transistors. We selected supply voltages of 1.1 V for the lower level driver and 1.25 V for the upper level driver.

4.4 Modulator performance

Two mixers and the corresponding base drivers are merged with a combiner circuit to form a final modulator core. This modulator core is interfaced directly to the differential digital lines of a corresponding baseband data source and to an external 50 Ω load. The LO can be interfaced through an additional balun and matching network, and finally, the circuit completed by providing current sources externally or on-chip. The latter alternative is typically preferred in commercial designs, and in practice merely an exercise in dimensioning transistors, generating a proper reference current, preferrably by using a bandgap-based source, and verifying the design across design corners. Supplying the reference externally, on the other hand, is sufficient for characterisation purposes, and allows for the flexibility and accuracy associated with sources off chip. Thus, we decided to follow this last route in this work.

4.4.1 Output signal

The modulator is simulated using transient analysis with all components in place, a carrier frequency of 75 GHz and driven using two random signal bitstreams with total data rate of 5 GBaud. A snapshot of the instantaneous signal waveform in the time domain is shown in Fig.4.8.
The gaps in the waveform at multiples of 200 ns are due to the settling time associated with switching current paths in both the mixer block lower and upper levels, whereby a large charge needs to be transferred to the respective transistor base before the corresponding BE-junction gets forward biased. The current associated with this charge transfer is limited by the 40 Ω collector resistor in the base drivers, such that a lower resistance value there may decrease this interval at the expense of increased quiescent power consumption. The corresponding transistors in the modulators may also be made smaller to decrease the associated capacitances, but this comes at the expense of the transistor on-state resistances and thus mixer efficiency. Fig.4.9 shows the spectrum of the modulator output signal shown in Fig.4.8 estimated using Welch's method. The sidebands are well behaved with monotonous roll-off away from the carrier. This modulated carrier data is collected over an adequate period of time, synchronously demodulated using a digitally synthesized carrier and filtered using an IIR low-pass filter with a Butterworth characteristic, yielding the constellation diagram shown in Fig.4.10. This figure shows good symbol separation at the data rate required in our design specifications.

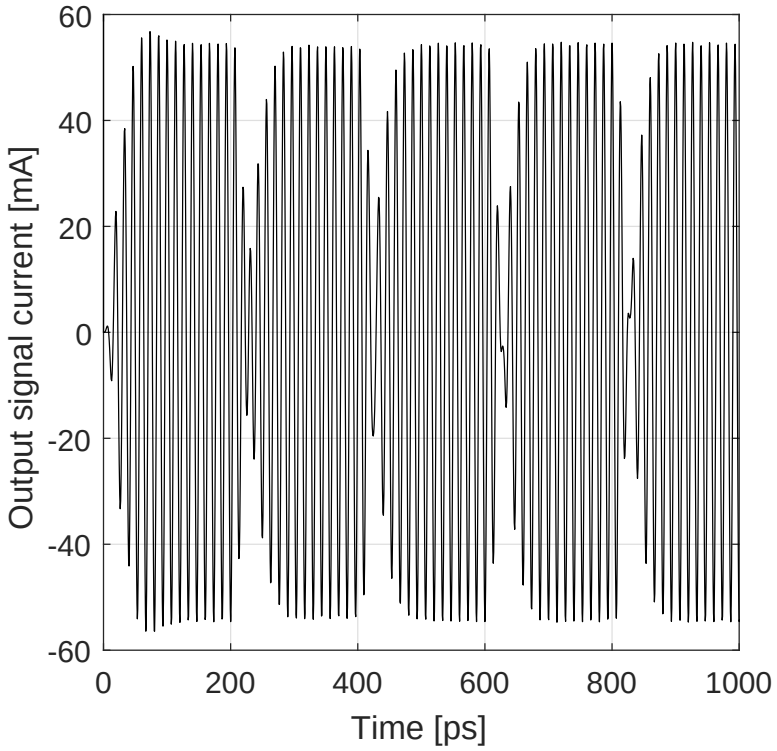


Figure 4.8: Modulator output signal current in the time domain. 75 GHz carrier modulated with random data at a symbol rate of 5 GBaud.

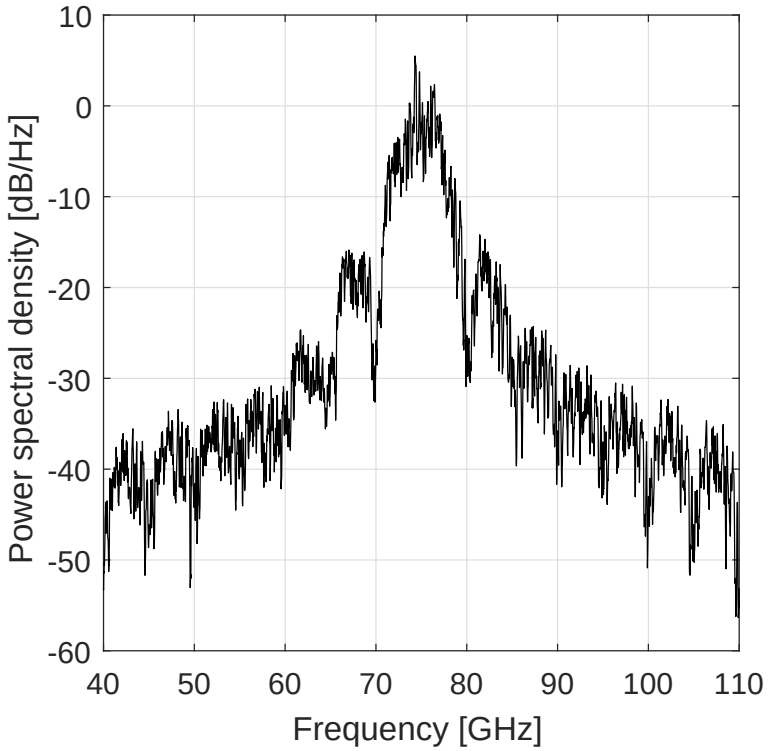


Figure 4.9: Circuit output power spectral density estimated by analysis of time domain simulation of the signal shown in Fig.4.8 using Welch's method.

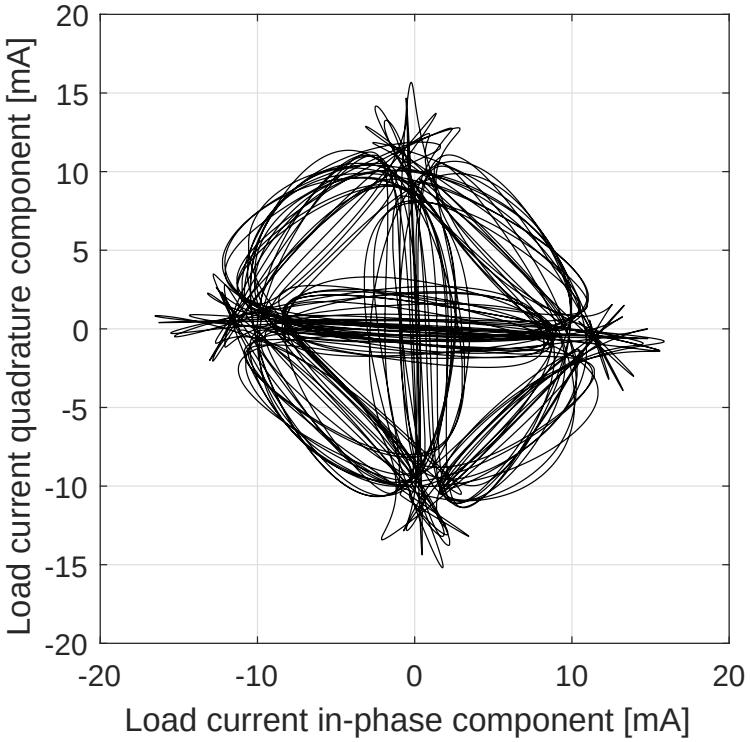


Figure 4.10: Modulator output signal constellation after down-conversion and low-pass filtering of the signal shown in Fig.4.8.

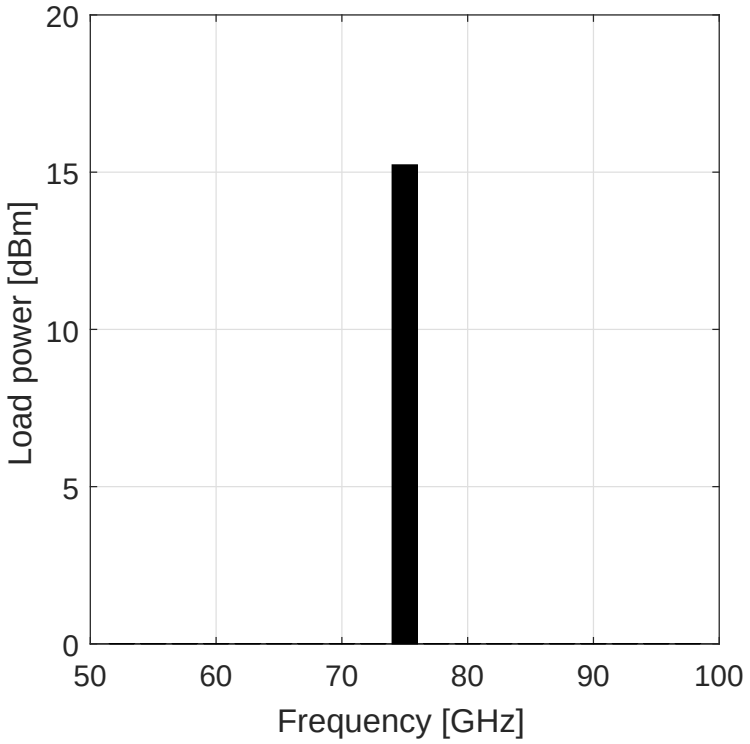


Figure 4.11: Harmonic balance analysis of circuit output power with unmodulated carrier. $P_{OUT} = 15.2$ dBm.

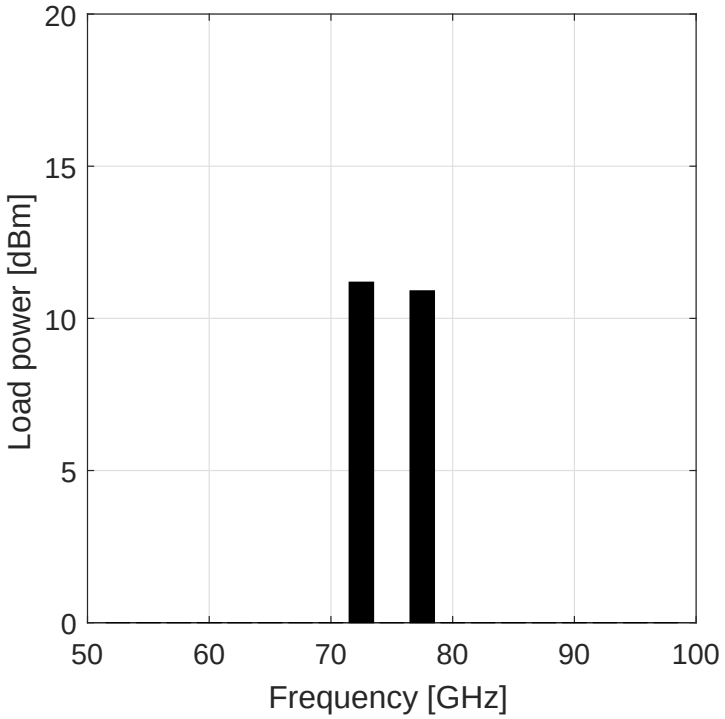


Figure 4.12: Harmonic balance analysis of circuit output power with carrier modulated using 2.5 GBaud repetitive sequence at baseband data port. $P_{OUT} = 14.1$ dBm. Carrier suppression 62.7 dB with respect to the upper sideband.

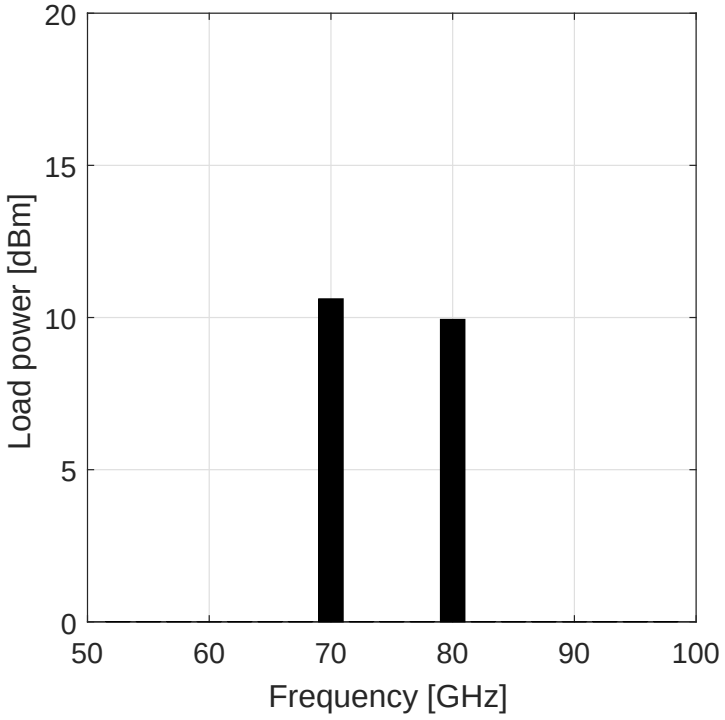


Figure 4.13: Harmonic balance analysis of circuit output power with carrier modulated using 5 GBaud repetitive sequence at baseband data port. $P_{OUT} = 13.3$ dBm. Carrier suppression 65.3 dB with respect to the upper sideband.

Harmonic balance analysis on the circuit shows that the modulator operates within its 3 dB bandwidth and yields good output power over the required baseband data rate as seen in Fig.4.11 through Fig.4.13. Carrier suppression was estimated to 65.3 dB using harmonic balance analysis, as seen in Fig.4.13. This value was derived under idealized conditions though, and probably does not accurately represent the values to be expected in a real circuit.

4.4.2 Power consumption

As expected, the mixers draw most of the power in the circuit at 44.4 mW each, followed by the base drivers. The total power consumption of the circuit is 114 mW. This figure does not include losses in current source- and additional circuitry such as voltage references which may be added to realize a complete system.

	Power consumption
Mixers	88.9 mW
Base drivers, upper	12.6 mW
Base drivers, lower	12.6 mW
LO buffers	12.1 mW
Total	126 mW

Table 4.1: Estimated power consumption in the various parts of the modulator.

4.4.3 Summary

The previous figures show that the modulator works as expected. Its output signal spectrum is shown in Fig.4.9 and the baseband IQ trajectory in Fig.4.10, representing valid operation of the power combiner studied in this work.
In over the air applications, the data rate this modulator is capable of may create a signal with sidelobes extending far outside of and potentially violating the allocated frequency range of the E band at 71-76 GHz, if not somehow band limited. A complete performance summary is listed in Table 4.2.

	Value
Supply voltage	1.5 V
Supply power	126 mW
Output power at 5 GBaud data rate	13.3 dBm
Carrier suppression at 5 GBaud data rate	65.3 dB
System efficiency at 5 GBaud data rate	17 %
Output power at 2.5 GBaud data rate	14.1 dBm
Carrier suppression at 2.5 GBaud data rate	62.7 dB
System efficiency at 2.5 GBaud data rate	20 %
Supported data rate	$\geq$ 5 GBaud

Table 4.2: Estimated performance summary.

Chapter 5

Discussion

5.1 Parasitic circuit elements

Although outside the scope of this thesis, the designed circuit would at this stage be completed by performing layout and parasitic extraction, where resistive, inductive and capacitive effects associated with the physical features of the circuit are extracted. These effects cannot be fully modelled or included at an earlier stage of the design due to their dependence on the actual circuit layout including length and shape of interconnects, proximity of a given device to one another and so on.
Parasitics affect the designed circuit in a variety of ways. For instance, the LO splitter network at the input would exhibit a shift in center frequency and also an uneven splitting of the signal. The mixer blocks would have reduced gain due to resistive as well as reactive effects affecting the characteristic frequencies of the resonant circuit elements, such as the even mode inductors and input matching networks. The mixer base drivers would see additional capacitance from the interconnects, resulting in slower rise and fall times and thus lower maximum baseband data frequency. Carrier suppression would probably also be affected, and turn out worse than what we estimated. Moreover, the combiner center frequency and port impedances would shift, resulting in lower efficiency and maximum power output and so on, due to the altered effective impedance presented to the mixer transistors, although Fig.2.9 suggests that this effect is probably not too significant.
The effects introduced by the parasitics can be mitigated by careful layout, tuning of the component values, re-simulating and repeating these steps until satisfactory results are obtained.

5.2 Comparison

We can see a list of performance specifications in recently published QPSK modulator designs in Table 5.1. The most comparable design is part of a larger system project [10], and can be seen to consume more power and needs a higher system supply voltage for lower output power. The comparison between a parasitic-free, simulated circuit and a finished circuit is still somewhat unfair, and we could expect the real differences to be slightly smaller than this comparison suggests.

	Technology	f_{LO}	Datarate	V_{OP}	Combiner topology	P_{OUT}	P_{DC}
This	**130 nm SiGe BiCMOS**	**71-76 GHz**	**$\geq$ 10 Gbps**	**1.5 V**	**Custom Combiner**	**13.3 dBm**	**126 mW**
[10]	130 nm SiGe BiCMOS	70-80 GHz	18 Gbps	3.3 V	Current Combiner	6 dBm	238 mW
[8]	45 nm SOI CMOS	155 GHz	20 Gbps	2 V	Current Combiner	1 dBm sat	290 mW
[9]	65 nm CMOS	60 GHz	4 Gbps	1 V	Current Combiner	-7.2 dBm	43 mW
[11]	180 nm SiGe BiCMOS	60 GHz	3.5 Gbps	1.8 V	Current Combiner	-9 dBm	27.5 mW
[12]	65 nm CMOS	55-61.5 GHz	5 Gbps	1 V	Current Combiner	N/A	5 mW
[13]	65 nm CMOS	240 GHz	20 Gbps	1 V	Current Combiner	-5 dBm	7.5 mW
[15]	250 nm SiGe BiCMOS	60 GHz	11 GHz (IF BW)	3 V	Current Combiner	-11 dBm	48 mW
[16]	250 nm InP HBT	300 GHz	50 Gbps	4 V	Wilkinson	-20 dBm	40 mW

Table 5.1: Comparison between this design and other recent publications.

5.3 Summary

As we have seen in the previous chapters, there are indeed opportunities for power savings in the QPSK modulator, which is otherwise a proven, mature building block with an established position in practice. The main limitation of the power combiner circuit we have discussed in this work is set by the design constraints we imposed themselves. The modulator circuitry must guarantee that the required phase relationship between the two combiner ports is preserved at all times, but as seen, this is easily corrected for in the modulator circuitry.
Amplitude modulation is a bit more problematic with this approach since the combiner efficiency at backoff is severely limited. The applicability of this circuit to QAM-based modulation formats is thus restricted. At backoff, the effective impedance at the drive ports change incurring severe efficiency penalties.
Extending the passive combiner network can yield additional degrees of freedom, allowing for the definition of fixed impedances at several operating points. The main problem in this regard is the network synthesis aspect, which for higher orders becomes increasingly challenging.

5.4 Possible improvements

The list of possible improvements in this work is long. The most important of these relate to the power combiner itself. As discussed previously, a higher order combiner that presents correct impedances to the driving transistors also for other power levels at backoff would be very interesting in QAM-style transmitter applications.
Except for the power combiner, there could be further improvement of the actual modulator circuitry, which was designed mainly for evaluation of the power combiner in a simulated setting. Nevertheless, at this stage the circuit is indeed still very competitive when comparing to similar designs (Table 5.1).
For production, we would need to add proper pads, generate a layout and extract parasitics, followed by a new simulation and reiterating until proper results achieved if needed. Finally, one would verify the design before proceeding to tapeout.
Regardless, the impact of these last steps on the results presented should be expected to be minimal when proper corrective measures being taken along the way. Temperature effects were not considered in the design (i.e. simulations were done at a fixed ambient temperature without temperature sweeps), but could be included in a proper verification across design corners. In this respect, inclusion of a temperature

compensated voltage reference on or off chip would come naturally at some point with the need to generate a largely temperature and supply voltage independent reference point with which to set our biasing.

5.5 Conclusion

Although limited with respect to higher orders of modulation in its basic form presented in this work, the power combiner we have introduced is suited for improving the power output of standard QPSK modulators. It will give a 3 dB gain in output power compared to a Wilkinson combiner, and also a good improvement over pure current combining, which is otherwise often encountered in publications on this topic. The ideas introduced in this work are especially valuable in state of the art applications at high frequencies, where we hope they may provide the designers of such circuits with an additional degree of freedom, ultimately enabling them to create the next world class designs at the frontiers of performance.

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Appendix A

A.1 Derivation of formula (3.5)

Assuming output resistance R and capacitance C in parallel

$$Z_{11} = R||C = \frac{R}{1 + j\omega RC} = r_{11} + jx_{11}$$

$$R = r_{11} + jx_{11} + j\omega RCr_{11} - \omega RCx_{11}$$

giving

$$R = r_{11} - \omega RCx_{11}$$

$$0 = x_{11} + \omega RCr_{11}$$

which we substitute into each other before applying $\omega = 2\pi f$ to get

$$-x_{11} - \omega Cx_{11}^2 = \omega Cr_{11}^2$$

$$-x_{11} = \omega Cx_{11}^2 + \omega Cr_{11}^2 = \omega C(x_{11}^2 + r_{11}^2)$$

$$C = \frac{-x_{11}}{2\pi f(x_{11}^2 + r_{11}^2)}$$

Appendix B

B.1 Combiner Z-matrix generator

This script was written for and run in Wolfram Mathematica ® version 10.3.1.0

```
(* I/Q Combiner network calculator v2.2 *)
(* Mark Popescu 2016.02.15 *)
(* Clear variables, set input and output port impedances by specifying *)
(* resistances z_r and reactances z_i at the ports *)
Clear["Global`*"]
zor = 52.5/2;
zoi = 0;
zlr = 25;
zli = 0;
z0 = 50; (* characteristic impedance *)
(* Define some arbitrary values for the corresponding resistive parts of the *)
(* resulting Z matrix that would yield a small series resistance and parallel *)
(* conductance yielding a invertible impedance matrix at the end. *)
r11 = 5000.0001;
r12 = 5000;
r13 = 5000;
r22 = 5000.0001;
r23 = 5000;
r33 = 5000.0001;
(* Define the calculation variables *)
ZL = zlr + I * zli ;
ZOPT = zor + I*zoi;
alpha = x + I*y;
I1 = V1/ZOPT;
I2 = V2/ZOPT;
I3 = V3 / ZL;
V1 = v0;
V2 = I*v0;
V3 = (V1+V2)*alpha;
Z1 = ZOPT;
Z2 = ZOPT;
Z3 = ZL;
(* Set up the matrix equation and substitute for the port voltages, insert resistive elements
   *)
EQ1 = z11 + z12*(I2/I1) + z13*(I3/I1) /.{ z11>r11+I*x11, z12>r12+I*x12, z13> r13+I*x13};
EQ2 = z21*(I1/I2) + z22 + z23*(I3/I2) /.{ z21>r12+I*x12, z22>r22+I*x22, z23> r23+I*x23};
EQ3 = z31*(I1/I3) + z32*(I2/I3) + z33 /.{ z31>r13+I*x13, z32>r23+I*x23, z33> r33+I*x33};
```

```
(* Split into real/imag *)
EQM = {ComplexExpand[Im[EQ1]], ComplexExpand[Re[EQ1]],ComplexExpand[Im[EQ2]],
    ComplexExpand[Re[EQ2]],ComplexExpand[Im[EQ3]], ComplexExpand[Re[EQ3]]};
(* Separate out the dependent variables as a matrix equation Mx = b *)
M = (Normal[CoefficientArrays[EQM,{x11, x12, x13, x22, x23, x33}]][[2]]);
(* Substitute for the input/output power conservation factor *)
Q = M /. {y -> Sqrt[(zlr/zor) x^2]};
(* Choose the remaining free variable arbitrarily (phase of output, which is irrelevant and
    thus unrestricted) *)
Q = Q/. {x -> 0};
(* Solve the equation for the dependent variable vector x by optimizing Mx = b (M is
    noninvertible) *)
M2 = LeastSquares[Q, {0,zor, 0, zor, 0, zlr }]/z0 // N;
(* Scale the resulting variable vector to the known output resistance zor *)
M2 = zor*M2/Part[M2,1];
x11 = Part[M2,1];
x12 = Part[M2,2];
x13 = Part[M2,3];
x22 = Part[M2,4];
x23 = Part[M2,5];
x33 = Part[M2,6];
(* Collect the results in a convenient Z matrix and export to matlab *)
Export["C:\\Users\\marpop\\Desktop\\combinerCalc_v2_2.mat","Z_matrix"->{{I*x11,I*x12,I*x13},{I
    *x12,I*x22,I*x23},{I*x13,I*x23,I*x33}},"LabeledData"];
```

Appendix C

C.1 System schematics

The system schematics present an overview over the most central aspects of the design. Bias voltages were intended to be generated off-chip in this design, and therefore details regarding this as well as other trivial details were omitted for the sake of clarity.

C.1.1 LO 90° hybrid

The LO 90° hybrid splits the incoming LO reference signal into an in-phase and a quadrature component which in turn feed the mixer blocks.

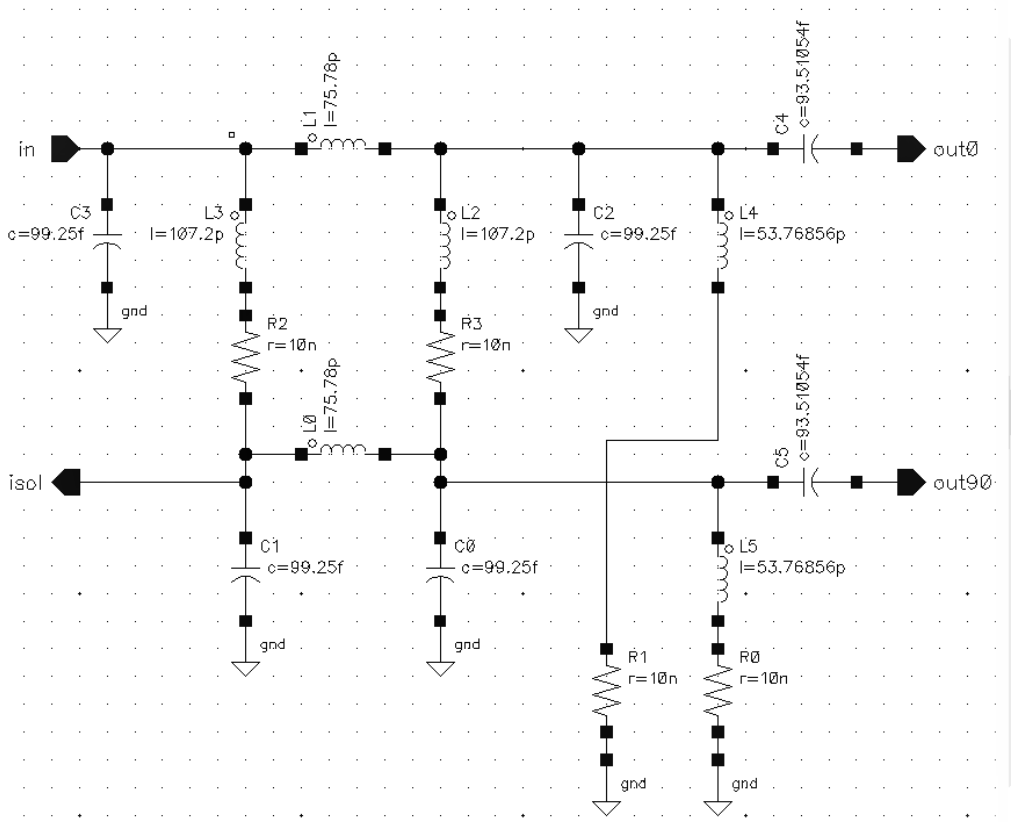

Figure C.1: LO 90° hybrid.

C.1.2 LO input matching buffers

The LO input matching buffer is designed to present a low impedance at the emitter terminal, which drives the bases of the mixer transistors in the mixer blocks. The LO shifter/splitter block in Fig.C.2 consists of two parallel 90° hybrids which generate $\phi = 0°$ and $\phi = 90°$ from the LO_P input (0°), and $\phi = 180°$ and $\phi = 270°$ from the LO_N input (180°). The buffer base bias resistors are $r\_bias\_driver = 700$ Ω. Emitter resistors were chosen to yield a 10 Ω source resistance in combination with the emitter resistance and the voltage swing needed for an input power of approximately -2 dBm at the mixers. Collector resistors of $r\_c\_buf \simeq 400$ Ω limit the voltage drop across the transistors. The inductors $l\_source = 3.8$ pH set the required reactance at the mixer inputs.

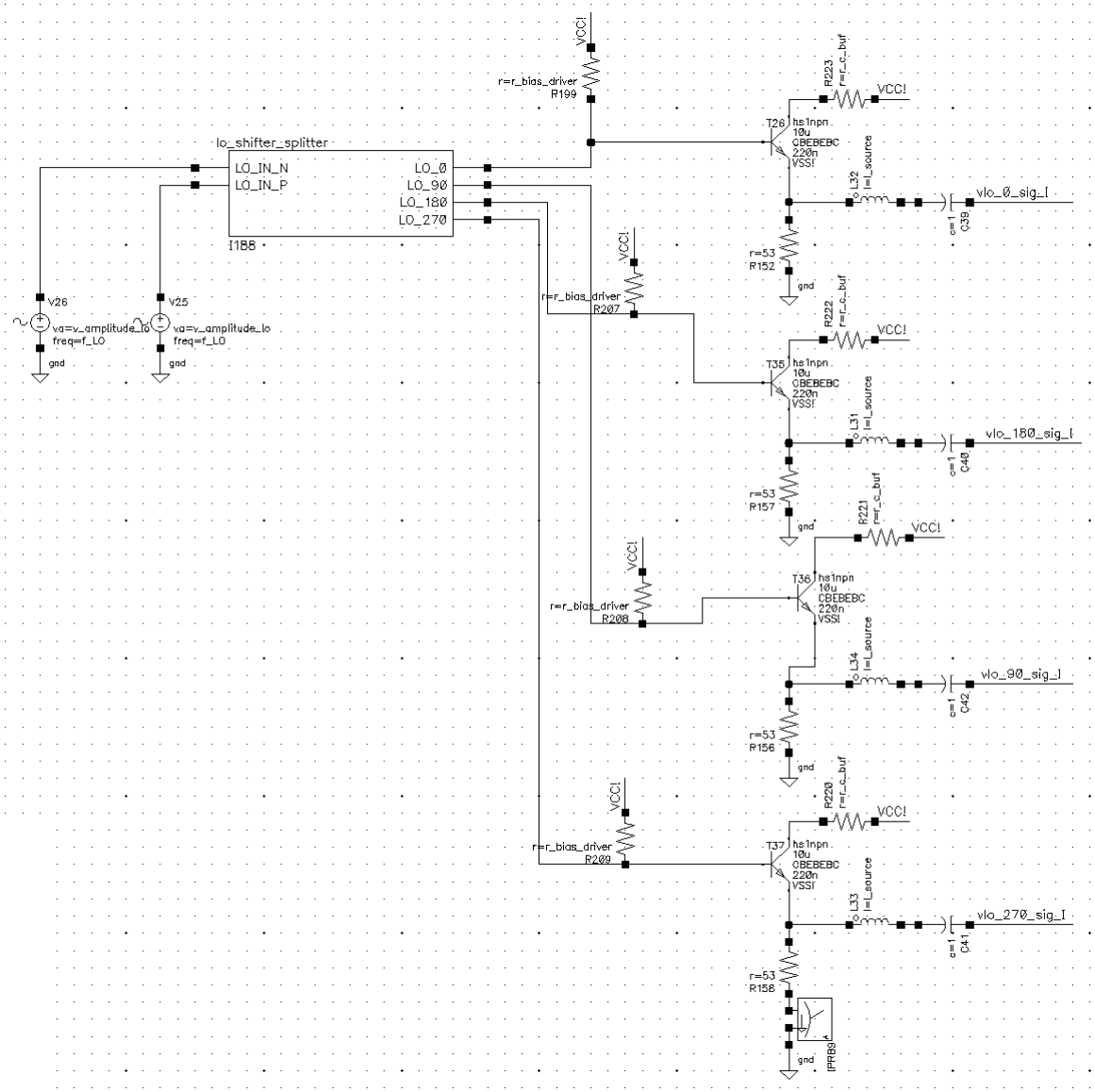

Figure C.2: LO input matching buffers.

C.1.3 Base driver

The base drivers are configured as CML inverter/buffer gates and drive the mixer current steering transistors. The collector resistors are both $r\_src = 40\ \Omega$, and the length of the drive transistors $dr_len = 2\ \mu$m.

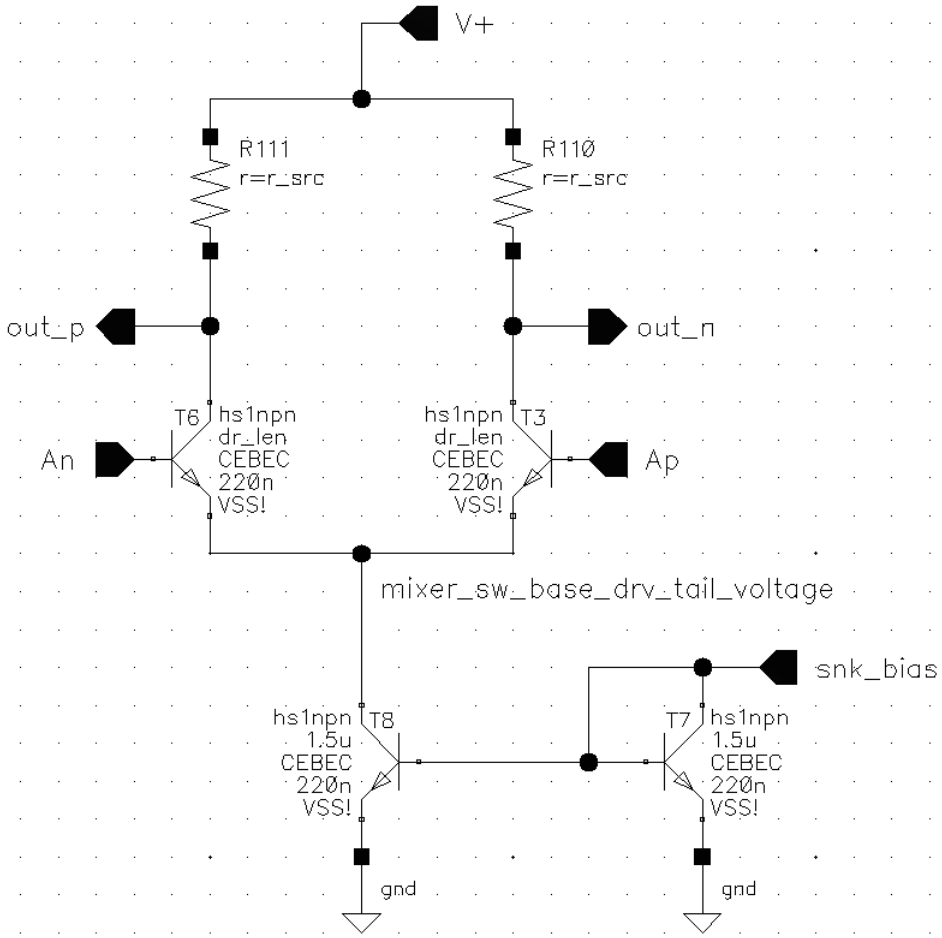

Figure C.3: Base driver.

C.1.4 Mixer block

The mixer block generates the mixing products between LO and baseband data. $L\_mixer\_harmonic = 27$ pH and $L\_interstage\_top = 20$ pH.

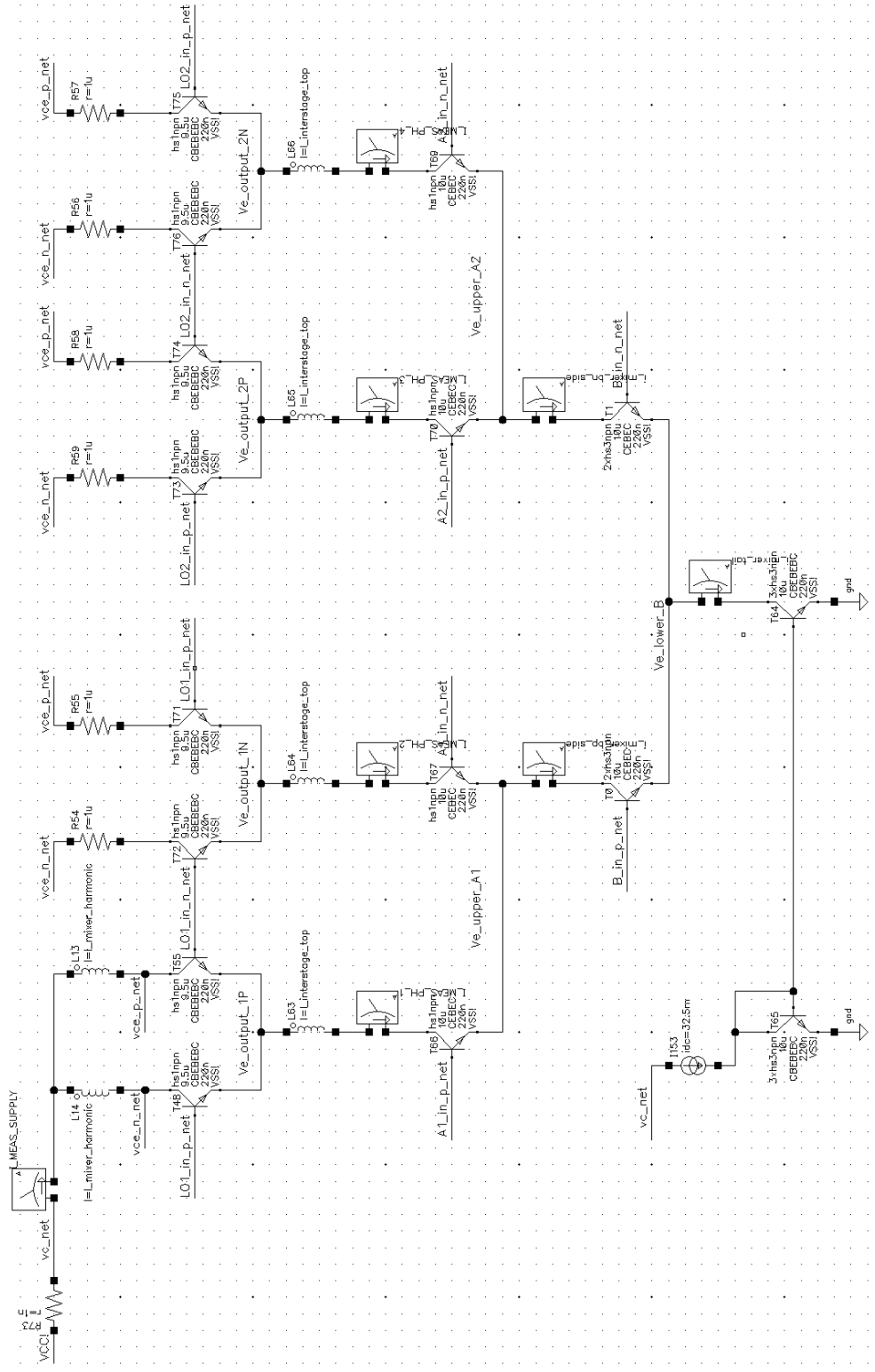

Figure C.4: Mixer block.

C.1.5 Output power combiner

The output signals from both the I and Q sources are combined in the previously designed power combiner shown in Fig.C.5. DC decoupling capacitors and resistors for aiding numerical convergence at simulation time are included, and constitute the difference with respect to the combiner circuit shown in Fig.4.5.

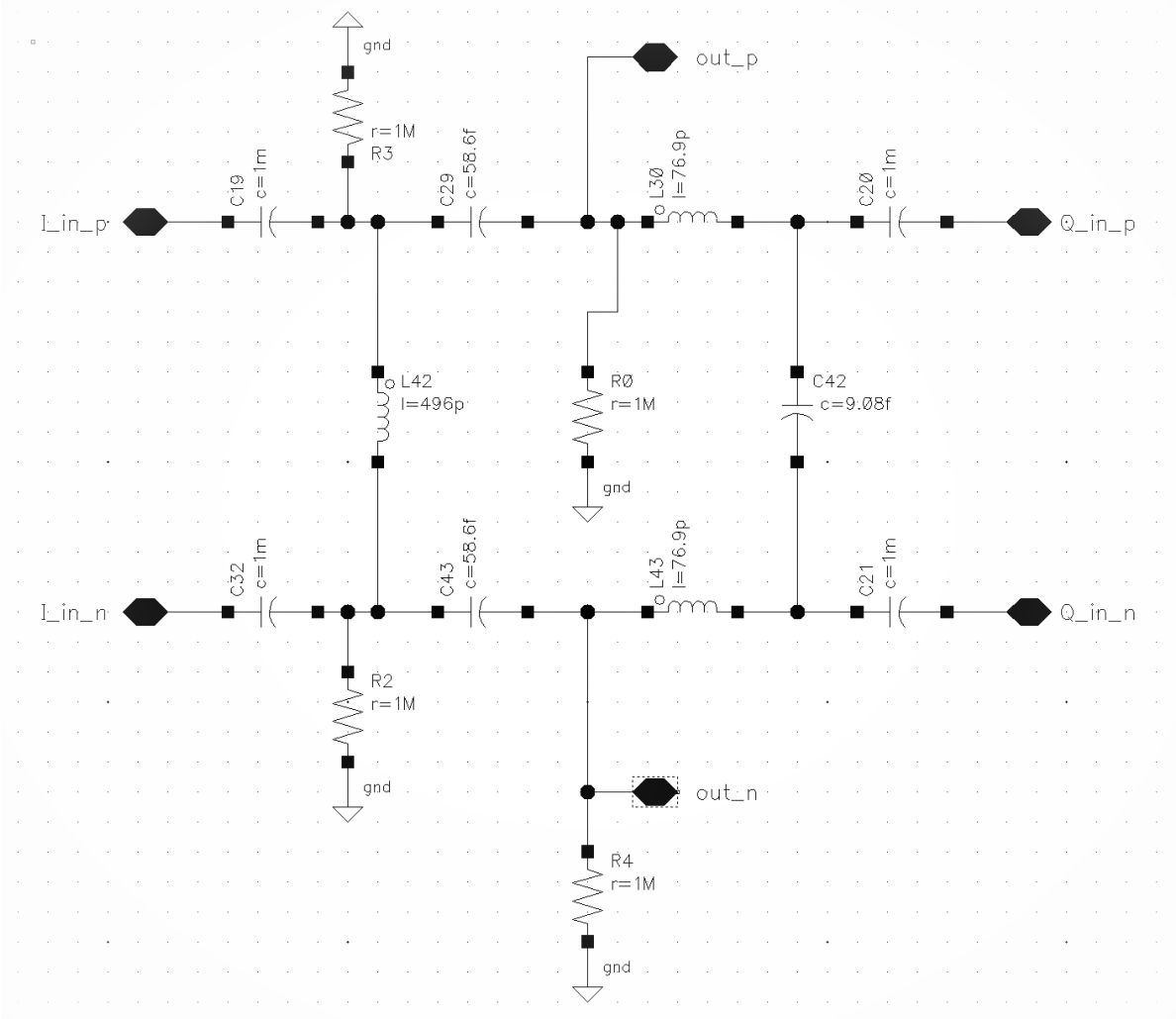

Figure C.5: Output power combiner.