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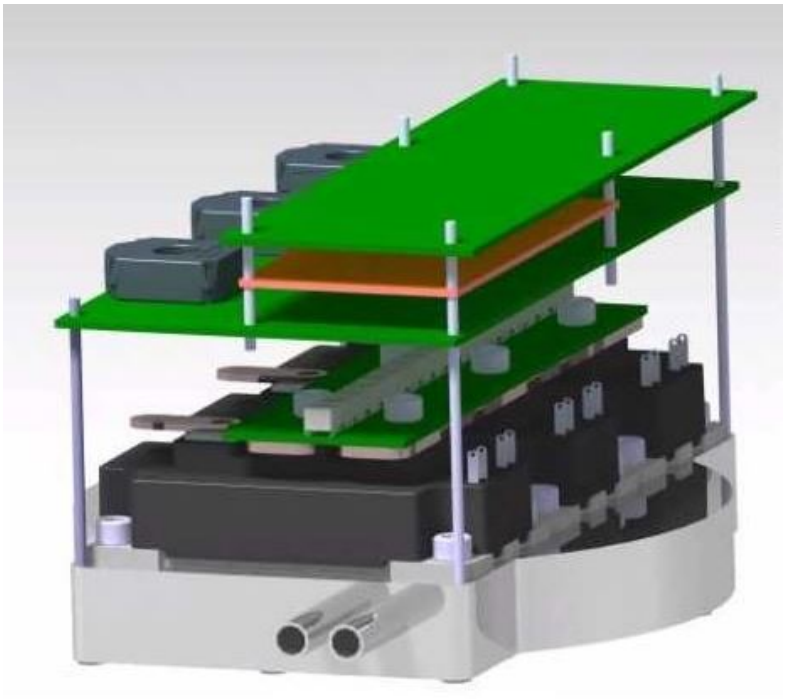

Design and Testing of a 3-Phase Voltage source Inverter for Mild Hybrid Vehicle Application.

Master's thesis in Electric Power Engineering.

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Department of Electric Power Engineering at Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

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Cover: Computer Aided Drawing of the Finalized Inverter Circuit.
Gothenburg, Sweden 2018

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Abstract

In this thesis a 3 phase Voltage source inverter has been designed, built and tested with Voltage level of 48V to illustrate the maximum output power levels that can be achieved in a given size and volume without the need to parallel the MOSFETS. The inverter is built using Si MOSFET Modules. Computer Aided Drawing is used to finalize the inverter's mechanical concept. The Printed Circuit Boards for the gate driver of the Inverter are designed. Cooling performance of the inverter is evaluated using CFD simulations and finally the inverter is built and tested with the static load.
To conclude, the inverter has been tested to deliver an output power of up to 15kVA, the designed gate driver circuit works properly for the inverter. Since the load demands in the Mild Hybrid vehicle are limited by the output of Power electronics this thesis illustrates that high power density per volume is achievable with further optimization in the design thus making the Mild Hybrid Vehicle more feasible.

Keywords: Mild Hybrid, Electric Vehicle, 3-phase inverter, High Power Density.

Acknowledgements

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Yashovardhan Rastogi, Gothenburg, January 2018

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1
Introduction

Regulating the carbon dioxide emissions is on the mind of every automotive manufacturers [1]. According to the new regulations passed by the European Commission the average carbon emission from the fleet of all new cars from a manufacturer should not exceed above 95g/CO_2. corresponding to a 23 % decrease from 2014's fleet average (123.4g/CO_2). One smart and quick way to meet that desired target of CO_2 emission is by converting the existing power train to some kind of electrified power train. According to the level of electrification a vehicle is categorized as Electric Vehicle, Hybrid Vehicle and Mild-Hybrid vehicle [2]. A typical electric power train consists a power supply which is mostly provided by a battery, an electric motor which is used the propel the car and a DC to AC inverter that transforms the DC voltage from the supply to the equivalent AC used to drive the electrical motor. A mild hybrid vehicle works on a 48 volt level and is usually present in combination with an internal combustion engine. It consists of an Integrated Starter Generator working like a normal alternator to produce energy for charging the battery and also supply to the electric loads, when the engine is running and recover energy during the vehicle's deceleration called regenerative braking. It's use a motor includes to start/cold crank the combustion engine and to aid the internal combustion engine for short duration of time, also called as torque assisting or boosting. It is easy to integrate with the existing power train of the vehicle and is less complex to implement as it does not require complex protective circuitry as defined by LV 148 standard [3] . Integration of the inverter with the ISG is a smart way to utilize the limited space in the existing car model [4]. The carbon emission reduction and performance boost are two of the main drivers for adoption of 48v dual-voltage systems until 2025.

1.1 Electrical Architecture in a vehicle

The Electrical architecture existing today is divided into 3 categories depending on the voltage type. The figure 1.1 shows the classification.

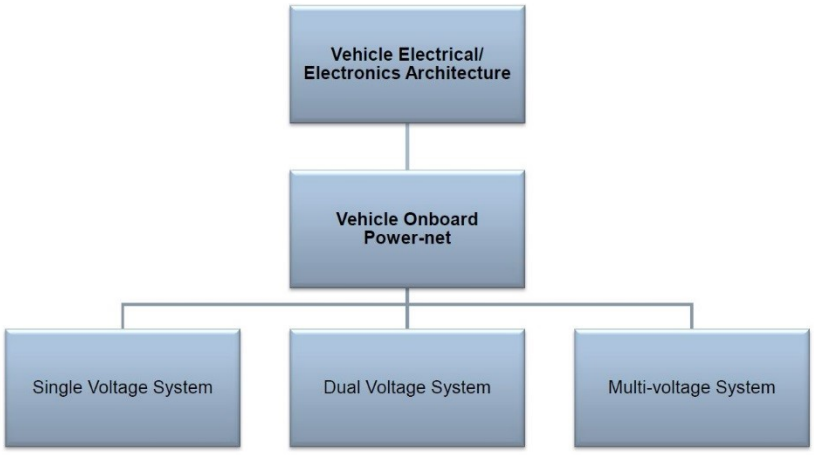

Figure 1.1: Classification of Vehicle's Electrical Architecture.

Single Voltage Architecture: A single voltage system will cater to only one voltage level, as found in current vehicles, such as a complete 12v system or a dedicated 48v system.
Dual Voltage Architecture: A dual voltage system will essentially cater to two voltage systems such as a 12v/48v system. A higher voltage system aims at reducing the weight and volume of the wiring harness and at the same time provides emission reduction.
Multi-voltage Architecture: A multi-voltage system is a voltage architecture capable of generating three or more voltages. Voltage changes depending on the application. For instance, lighting might be a 12v application, roll stabilization might be a 48v application, and eBoosting might require 60v or more.

1.2 Benefits of 48V technology over traditional architecture.

The table 1.1 shows the comparison between the traditional 12V architecture and the newer 48V dual architecture.

Table 1.1: Comparison between 12V and 48V architecture

	12 V traditional Architecture	**48V Dual Architecture**
Start Stop System	Starting time: 2-3 sec	Starting time: 0.4 to 1 sec, Engine Boost: 10kW power—sufficient for 30 seconds of driving.
Fuel Saving	Start-Stop + eBoosting + Downsizing could cumulatively result in 8–10% of fuel consumption savings compared to baseline vehicle without these technologies.	Start-Stop + eBoosting + Downsizing + Coasting + Porting power-hungry applications to 48v cumulatively results in 15–20% of fuel consumption savings, inching closer towards Euro6 compliance.,Coasting technique helps restore power to accumulator/battery during downhill operation and also boosts engine power during uphill operation.

The figure 1.2 shows the suitability of the mild hybrid application compared to the traditional 12V architecture and the recently existing and more sophisticated "High Voltage" system. Increasing the voltage levels to 48v not only provides the aforementioned benefits, but also bridges the gap between current day 12v hybrid solutions and more state-of-the-art high-voltage hybrid solutions.

Packaging and Weight: Due to higher voltage, the size of the prime-mover (e.g., motor, valve, and actuator) and related wiring can go down by 50–66.7%, thereby providing better packaging advantages. Most of the mechanical components will be electronic based, so accessories can now be located outside the engine bay, which facilitates better packaging, lower weight, and higher efficiency, and, ultimately, reduces CO2 emissions.

Higher Performance: Electrifying the present day hydraulic system offers better performance by reducing the reaction time drastically. Large amounts of fuel savings and performance benefits can been achieved by merely electrifying the earlier pure hydraulic-assist systems.

CO2 Reduction: In an ideal scenario, 15% of the existing level of emissions can

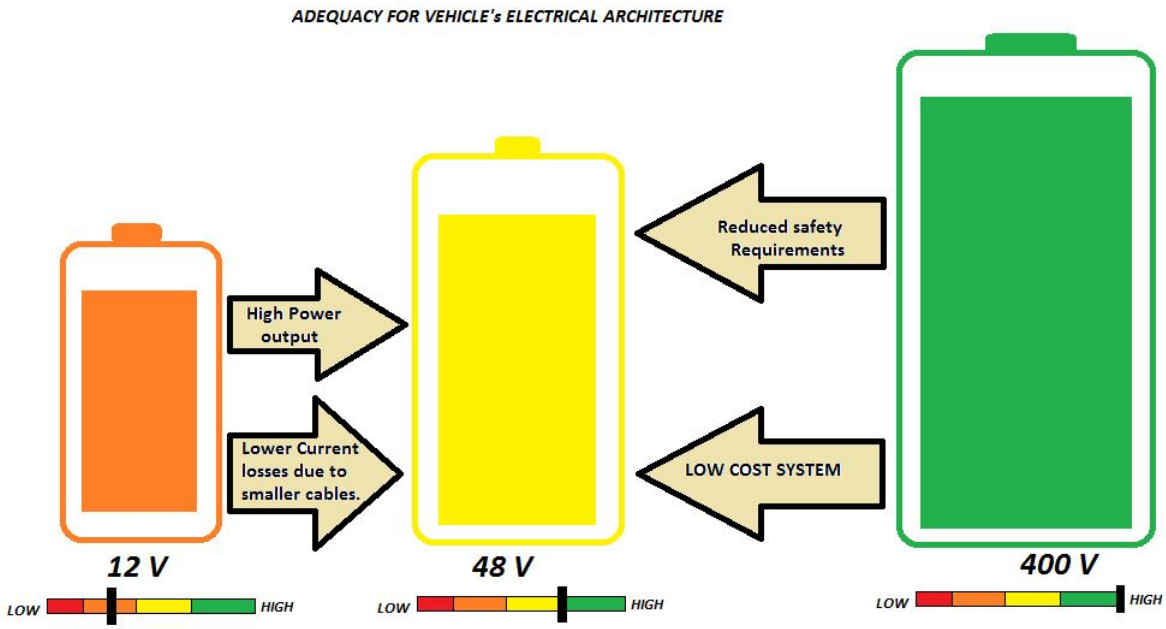

Figure 1.2: Suitability of 48V dual voltage architecture.

be brought down, despite using an additional 48V battery.
The current 12V architecture has reached its limit and can no longer meet the increasing demands of in-vehicle electrical loads. A marginal increase in voltage to a range of between 20V and 24V will not provide the level of improvement needed for sufficient performance. However, between 24V and 36V performance improvement can be achieved, but some functional limitations will persist. On the other hand, going beyond 52V also results in functional limitations, and going beyond 60v requires special measures to protect a vehicle's occupants from exposure to the electrical system. The ideal voltage range exists between 36V and 52V. Early initiatives focused on a dedicated 42V level, but the proposed 48V provides a secondary voltage level as an add-on power supply in the vehicle.

2
PROBLEM DESCRIPTION

Mild hybrid vehicle is usually realized by combining relatively a downsized internal combustion engine with a high power electrical machine in the power ranges of 10kW to 20kW to implement several fuel saving functions: start-and-stop, torque assistance, regenerative braking, fully electric steering, and electrically controlled air-conditioning compressors, to name just a few. A belt driven motor generator also called Integrated Starter Generator replaces the already existing alternator thus avoiding major mechanical changes in the layout of the drivetrain of the car. Since the electrical machine is required to achieve the power levels around 20kW, the conventional inverters are pushed to their limit since the supply current for cranking the engine would be 500A. One solution is to have the parallel connected electronic switches to meet the high power (which in turn translates into high current demand) or to have the parallel connected inverter to share the lead. This strategy results in additional components thereby increasing the cost to implement this technology. Also with limited space available in the existing powertrain of the car increasing number of components is not a feasible solution. Thus the aim of this thesis work is to design a compact DC-AC three phase 2 level voltage source inverter with high power density per unit volume with the aim to reduce the use of discreet components thus saving space and cost.

3

48V Mild Hybrid Drive train (System Description)

The figure 3.1 represents the 48V system overview as implemented in Delphi's second generation mild hybrid system architecture [5] The main components are described in the following sections:

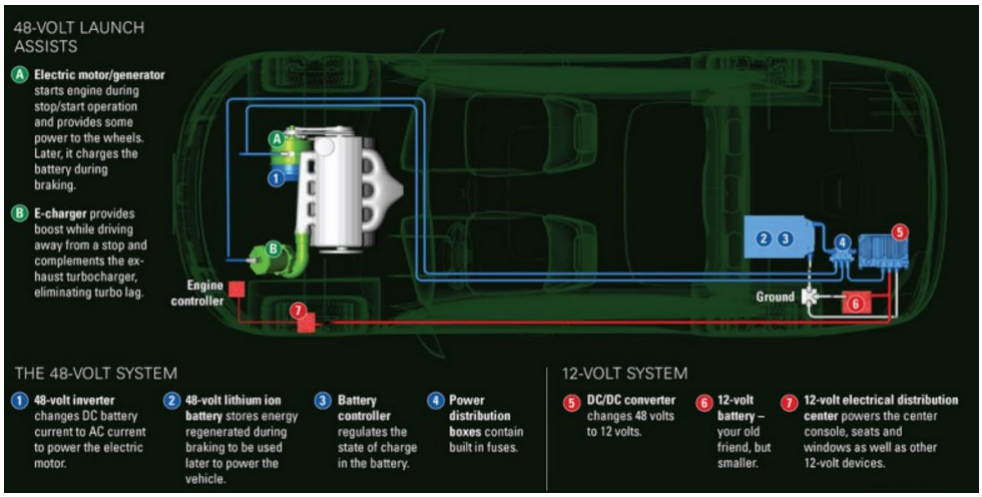

Figure 3.1: 48V system drive train adopted from Delphi's second generation system architecture.

3.1 Motor generator unit

The motor generator unit in a 48V mild hybrid system is connected to the engine's crankshaft via an accessory belt. Due to the heavy load demands the 48-volt unit is often liquid cooled. The most normal operating conditions are 5kW continuous operation of the motor generation, a 30 second 10kW operation and a finally a 20kW peak operation lasting for few seconds. In the first two cases, the approximately 5kW and 10 kW unit acts as a motor, receiving current from the 48-volt lithium-ion battery in the trunk through an inverter, which changes DC power to AC to drive the motor. That motor then turns the gasoline or diesel engine over via the drive belt. This then either quickly fires up the combustion engine after a start/stop event (a 12-volt starter remains for cold starts), provides a "boost" to the engine to improve acceleration performance (particularly after a start/stop event), or reduces

engine loads at other strategic times to maximize fuel economy. The unit does not only act like a motor and send torque to the crankshaft—as its name implies it's also a generator, receiving torque in order to fulfill its most basic duty of generating electricity for the 48-volt battery pack in the back of the car. This happens not only when the engine is on and spinning the belt (like with a conventional alternator), but also when the engine is off and the vehicle is coasting or braking. This means the internal combustion engine is able shut off the fuel supply, and the wheels actually rotate the internal combustion engine through a locked torque converter. The belt from the motoring engine's crankshaft then spins the unit, which creates energy for the 48-volt battery. Thus, the unit acts not just to seamlessly start the car after a start/stop event, perform the alternator's charging duty, and help reduce the load on the engine by exerting torque on the crankshaft, but it also allows for regenerative braking. The 48V electrical system does not replace the car's standard 12V electrical system; instead, it's connected to the 12V system via a DC/DC converter. The starter generator is a closed-loop controlled electrical machine using electronic devices to limit power consumption. According to the current state of technology, the starter generator can feed up to 15 kW into the 48-volt system when the IC engine is running. Two machine technologies exist – synchronous and asynchronous machines 3.2. Synchronous machines are subdivided into machines with exciter winding, either of the salient-pole or claw-pole rotor type, permanent magnet synchronous machines and reluctance machines. Asynchronous or inductance machines are also known as squirrel-cage machines due to their rotor technology. The cage can be made of aluminum or copper. The speed, efficiency and power density of the machines may vary subject to the power and maximum current of their respective rectifiers. Electric machines currently employ drives based on permanent magnet synchronous motors (PMSMs) or induction motors. Induction motors and PMSMs can be driven with a proper power electronic converter. These kinds of drives can only reach very high torque at low speeds through the injection of very high current in the machine stator winding. Electromagnetic flux control methodology must be used to drive the motor at very high speeds. PMSM motors are widely adopted in electric and hybrid vehicles. However, the cost is very expensive because of the permanent magnet, and the efficiency is reduced at high speeds owing to the weakened flux. For induction motors, flux control can be adopted at high speeds; how- ever, guaranteeing high torque at low speed is difficult. Recently, the wound rotor synchronous motor (WRSM) has received a great deal of attention for automotive applications requiring robustness and high-speed operation. It is a cost-effective motor that does not use permanent magnets. Since the motor does not contain any rare earth permanent magnets, the WRSM offers a considerable reduction of manufacturing costs. Other advantage is that since a short burst of high current can be fed into the rotor, a higher peak torque density can be achieved. The peak torque however, is limited by the power electronics that feed the stator and rotor coils of the motor. The rotor current regulation provides a very high power factor, enabling excellent inverter utilization. In other words, the separately excited motor delivers the highest output power for a given inverter current and battery voltage Appropriate rotor excitation regulation produces an outstanding power curve. In fact, the current-excited motor delivers an almost constant power

output above the corner speed. The separately excited motor is highly efficient at low torque [6]. Correct selection of the rotor current also means efficiency can be optimized for low power operating points, which are used most during conventional drive cycles. In spite of its advantages, the system architecture of a current excited motor is more complex compared with other popular motors. In fact, it requires a power transfer system to feed the rotor coil with the appropriate current. To achieve this, carbon brushes combined with slip rings are usually employed. However, these elements are prone to wear and produce large amounts of dust inside the motor. Therefore to solve this problem a rotating transformer to transfer power to the rotor coil is used. Compared with the other motors, WRSM has the advantage of various control methods, because it has three control variables: (if, id, and iq) [7]. However, this means that finding an appropriate current combination is difficult. In addition, it is difficult to predict the characteristics of WRSM because of magnetic saturation. For accurate current control, a current map (if, id, and iq) according to the load conditions is required. The figure 3.2 classifies the various existing technologies used for the motor generator unit in 48V mild hybrid.

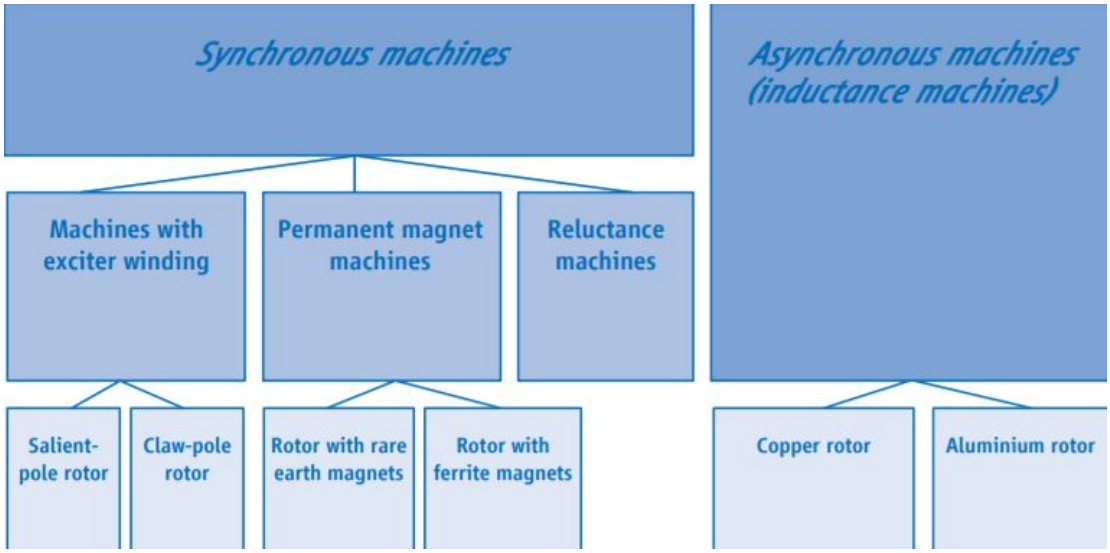

Figure 3.2: Electrical Machines comparison.

3.2 Inverter:

A bidirectional inverter is required for operating a starter generator [8]. This inverter transforms the battery's direct current into a 3-phase alternating current, supplying the individual winding of the electrical machine with electric energy. The energy flow is reversed for recuperation. In this case, the inverter transforms the alternating current generated into direct current to charge the battery [9]. In terms of its functional configuration, the inverter of 48-volt systems is similar to that of the high-voltage inverters used in full hybrids or all-electric cars, as it connects the battery accumulator to the three-phase WRSM motor. (figure 32). One of the main differences lies in the power semiconductors used. Unlike the high-voltage systems using primarily IGBTs (Insulated Gate Bipolar Transistors), MOSFETs are predestined for use as switching elements in inverters for starter generators due to their lower voltages. To control a 3-i-phase machine, MOSFETs are configured as three half-bridges. A voltage converter (DC/DC converter) is used to transfer energy between the two subsystems of a dual voltage system. Since it mostly transfers energy from the 48-volt system to the 12-volt level, it is primarily operated as a step-down converter. In this energy transfer direction, the DC/DC converter replaces the generator for the traditional 12-volt system. The figure 3.3 shows the block diagram of the inverter electronics.

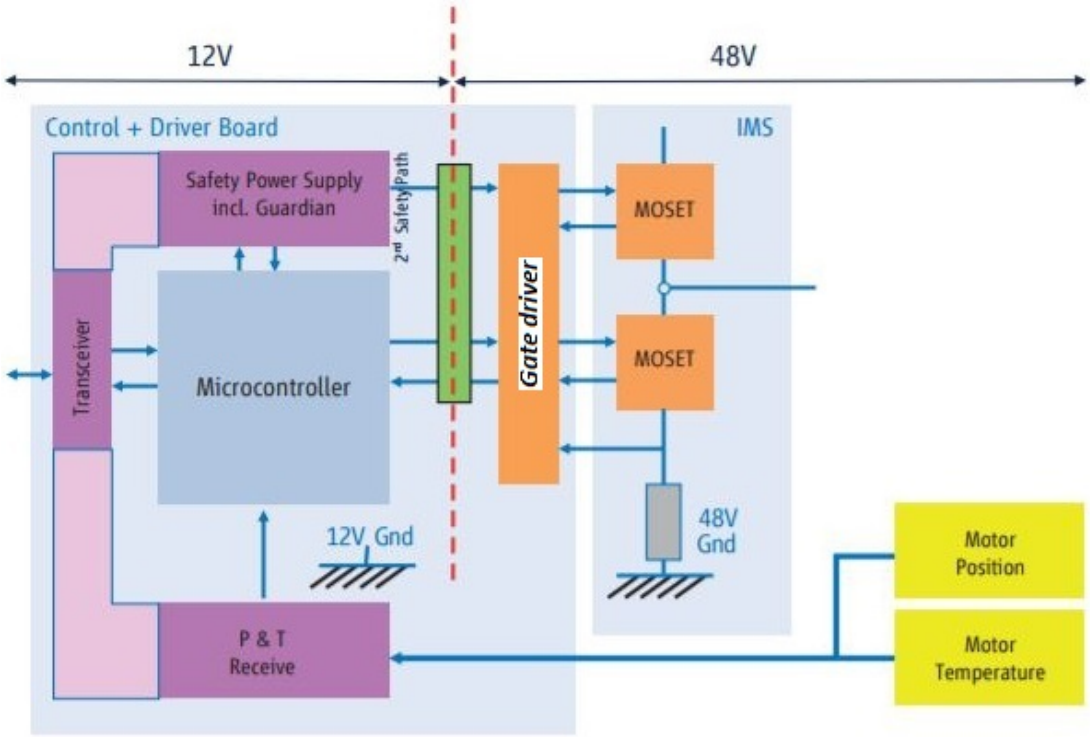

Figure 3.3: Inverter Electronics.

3.3 Energy and battery management

The dual-voltage system considered in this thesis comprises of a 12-volt lead acid starter battery and a 48-volt lithium-ion battery. The 48-volt lithium-ion battery supplies high-power loads such as the A/C system, water pump, active chassis control and electric drive support, and stores electric recuperation energy generated during braking. The 12-volt lead acid battery supplies all other system components such as lighting, entertainment electronics and other standby power loads such as clocks and safety systems. It serves as a fallback solution in the event of the supply from the 48-volt system being interrupted.The main requirements for 48-volt batteries typically relate to the supply of pulsed power in the charging and discharging directions, and to the need for a sufficiently high charge level and temperature range to ensure the availability of adequate power. The cell pack consists of a number of cells determined by the cell chemistry selected and connected together in series or parallel or a combination of both depending on the required battery capacity and the individual capacity of the selected cells Although prismatic cells or pouch cells are preferably used, round cells are also available.

3.4 Hybrid Control Software

To control the entire functionality of start stop function, pure electric drive, Battery power management and other functionality the main Engine Control Unit (ECU) acts as the brain of the entire mild hybrid drivetrain.

4

Design of a 48V inverter

Electric motors are the main propulsion system in electric vehicles. Hybrid electric vehicles have two propulsion systems: an ICE combined with electric motor in different configurations of either series, parallel or mixed. In contrast to ICE, electric motors offers various important advantages: High torque at low speeds, the instantaneous power values exceed 2-3 times the rated ICE, torque values are easily reproducible, adjustment speed limits are higher. Due to these characteristics a good dynamic performance in the form of large accelerations and small time both at start up and braking is ensured. The voltage source inverter (VSI) connects the battery accumulator to the three-phase EESM motor. The VSI modulates the three-phase current waveforms driving the motor in the car. The figure below shows the general configuration of the VSI. In this structure, the DC voltage of the battery accumulator can be converted to three-phase AC voltages, by modulating sinusoidal waveforms with high frequency switching of power semiconductors.

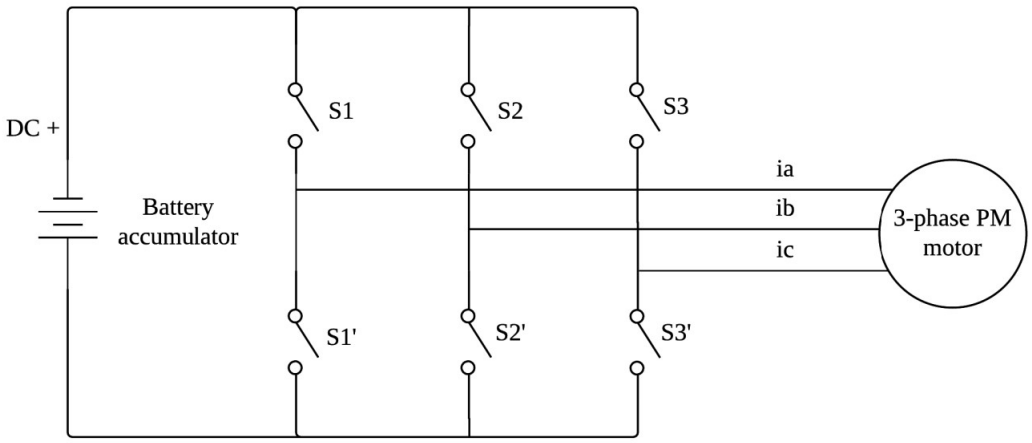

Figure 4.1: Functional diagram of 3-phase inverter

The main parameters identified for the inverter design in this project are described in the table 4.1. The peak operation point was set at 20kW and the continuous operating point of the inverter was at 5kW.

Table 4.1: Important Inverter design parameters

Maximal DC voltage	48V dc
Continuous output current	100A
Peak output current	500A (rms)
Clock frequency	20-25 kHz
Size	Cylindrical shape 180*50mm

4.1 Inverter Components

The voltage source inverter is made up number of components which are described in detail in following subsections:

4.1.1 Semiconductor Switches

The most commonly used electronic switches for low voltage and medium voltage power electronic converters are MOSFET [10] MOSFET is abbreviated for Metal Oxide Semiconductor Field Effect Transistor and it is a switching power transistor that behaves as a switch turning On and off with a very fast switching frequency. It consist of three terminals (figure 4.2) drain (D), source (S), and a gate (G). When the switch is closed the flow of the current is from the drain to the source terminal with a resistance called On state Resistance between the drain and source.

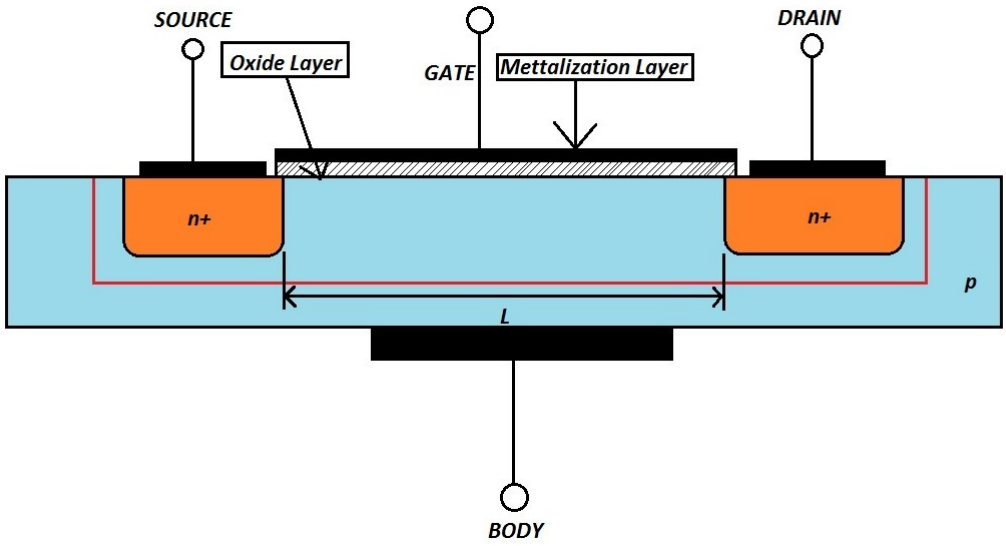

Figure 4.2: Mosfet

Due to an intrinsic anti-parallel diode also called body diode the MOSFET can not block the egative-polarity voltage. So, the MOSFET blocks only the positive Voltage called as V_{DS}. Power MOSFETs have a vertical structure by virtue of which the voltage rating of the transistor is directly related to the doping and thickness of the layer called N epitaxial layer while the current rating is the direct function of channel width. This structural configuration makes the transistor capable to have high blocking voltage capability and also higher current conducting capability [11].Some general characteristics of the switched semiconductors are described in the figure 4.3

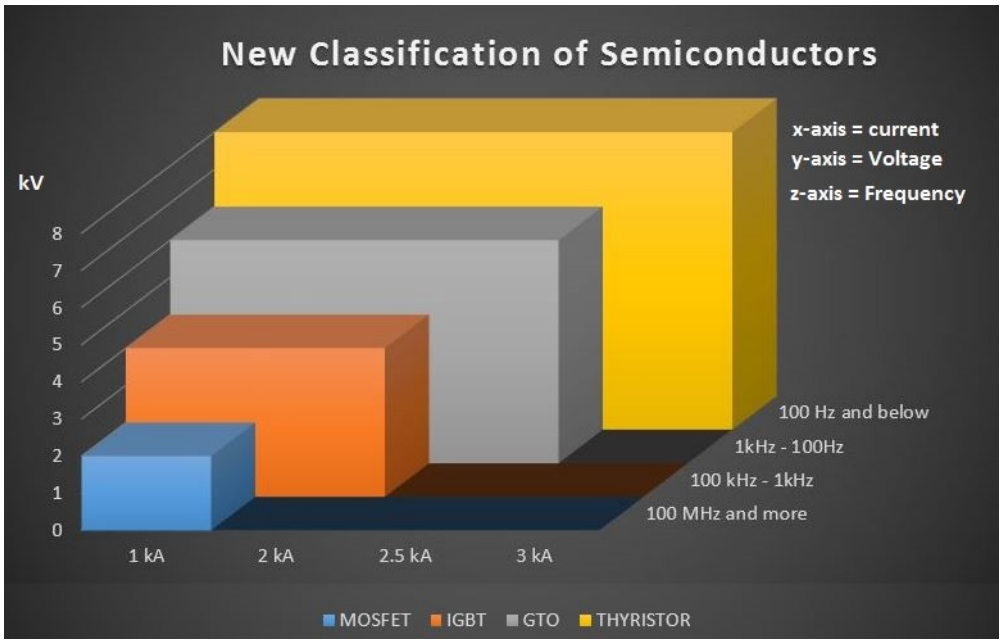

Figure 4.3: Mosfet Classification

The power MOSFET in the on-state behaves like a clsoed switch with a resistance between the drain and source terminals. This resistance (called R_{DSon} for "drain to source resistance in on-state") is the sum of many elementary contributions as seen in the figure 4.4:

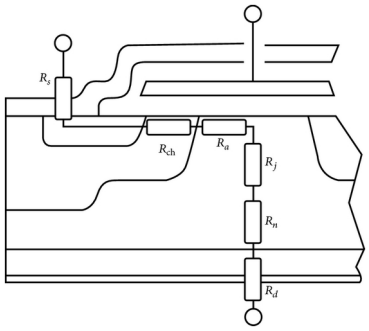

Figure 4.4: Mosfets ON state resistance description.

- R_S is the source resistance representing all resistances between the source and the channel of the MOSFET i.e. resistance of the wire bonds, of the source metallisation, and of the N+ wells;
- R_{ch}. This is the channel resistance. It is inversely proportional to the channel width and the channel density. The channel resistance is one of the main contributors to the RDS_{on} of low-voltage MOSFETs.
- R_a is the access resistance representing the resistance of the epitaxial zone directly under the gate electrode, where the direction of the current changes from horizontal (in the channel) to vertical (to the drain contact);
- R_J is the detrimental effect of the cell size reduction mentioned above: the P implantations form the gates of a parasitic JFET transistor that tend to reduce the width of the current flow;
- Rn is the resistance of the epitaxial layer. Rn is directly related to the voltage rating of the device. A high voltage MOSFET requires a thick, low-doped layer (i.e. highly resistive), whereas a low-voltage transistor only requires a thin layer with a higher doping level. As a result, Rn is the main factor responsible for the resistance of high-voltage MOSFETs;
- R_d is the equivalent of R_S for the drain. It represents the resistance of the transistor substrate [11].

The two main parameters governing both the breakdown voltage and the R_{DSon} of the transistor are the doping level and the thickness of the N epitaxial layer. The thicker the layer and the lower its doping level, the higher the breakdown voltage. On the contrary, the thinner the layer and the higher the doping level, the lower the R_{DSon} (and therefore the lower the conduction losses of the MOSFET). Therefore, there is always a trade-off in the design of a MOSFET, between its voltage rating and its ON state resistance.

Packaging inductance: To operate, the MOSFET must be connected to the external circuit, most of the time using wire bonding. These connections exhibit a parasitic inductance, which is in no way specific to the MOSFET technology, but has important effects because of the high commutation speeds. Parasitic inductance tend to maintain their current constant and generate over-voltage during the transistor turn off, resulting in increasing commutation losses.

A parasitic inductance can be associated with each terminal of the MOSFET as seen in figure 4.5. They have different effects as described below:

- The gate inductance has little influence (assuming it is lower than some hundreds of nanohenries), because the current gradients on the gate are relatively slow. In some cases, however, the gate inductance and the input capacitance of the transistor can constitute an oscillator. This must be avoided as it results in very high commutation losses (up to the destruction of the device). On a typical design, parasitic inductances are kept low enough to prevent this phenomenon
- The drain inductance tends to reduce the drain voltage when the MOSFET turns on, so it reduces turn on losses. However, as it creates an overvoltage during turn-off, it increases turn-off losses.
- The source parasitic inductance has the same behaviour as the drain inductance, plus a feedback effect that makes commutation last longer, thus increasing commutation losses.
- At the beginning of a fast turn-on, due to the source inductance, the voltage at the source (on the die) will be able to jump up as well as the gate voltage; the internal VGS voltage will remain low for a longer time, therefore delaying turn-on.
- At the beginning of a fast turn-off, as current through the source inductance decreases sharply, the resulting voltage across it goes negative (with respect to the lead outside the package) raising the internal VGS voltage, keeping the MOSFET on, and therefore delaying turn-off

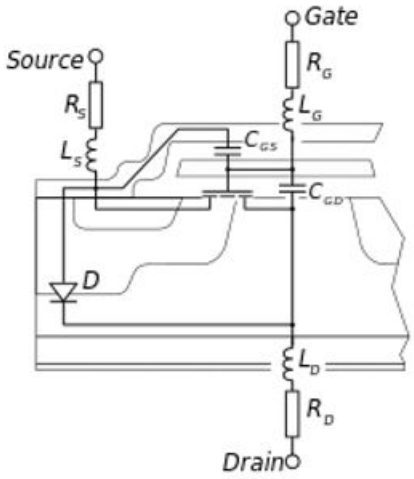

Figure 4.5: Mosfets packaging inductance description.

The MOSFET selected in this project is a phase leg MOSFET module which means 1 module represents one phase leg. The figure 4.6 represents the equivalent circuit of the phase leg module.

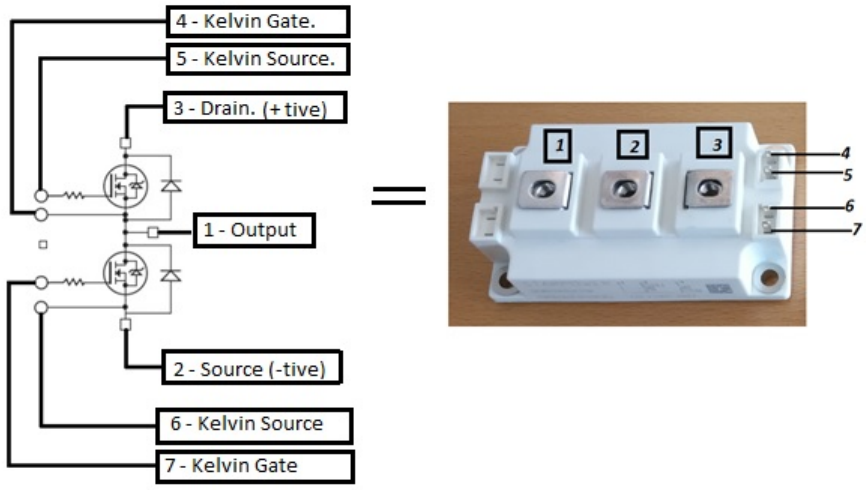

Figure 4.6: Equivalent Circuit of Phase leg MOSFET Module.

This meant that 3 of those modules would be needed to make the 3-phase inverter. The specifications of the MOSFET module chosen are listed in figure 4.7.

Absolute Maximum Ratings T_C=25℃ unless otherwise noted

Symbol	Description	MD1026HFM150C2S	Units
V_{DSS}	Drain-Source Voltage	150	V
V_{GSS}	Gate-Source Voltage	±30	V
I_D	Drain Current @ T_C=25℃ @ T_C=80℃	1026 726	A
I_F	Diode Forward Current	1026	A
P_D	Maximum Power Dissipation @ T_j=175℃	2083	W
T_{jmax}	Maximum Junction Temperature	175	℃
T_{jop}	Operating Junction Temperature	-40 to +150	℃
T_{STG}	Storage Temperature Range	-40 to +125	℃
V_{ISO}	Isolation Voltage RMS,f=50Hz,t=1min	2500	V
Mounting Torque	Power Terminal Screw:M6 Mounting Screw:M6	2.5 to 5.0 3.0 to 5.0	N.m

Figure 4.7: Important mosfet parameters

4.1.2 Gate driver Circuit

MOSFETs require a gate drive circuit to translate the on/off signals from a digital controller into the power signals necessary to control the MOSFET [12] A MOSFET is a voltage controlled device. It has three terminals: a gate, a drain, and the source. The source and drain are the terminals through which the current flows. The gate and bulk voltages control the current. There needs to be a certain gate-to-source voltage, called threshold voltage, in order for the MOSFET to turn on. However the isolated gate-electrode of the MOSFET forms a capacitor, called gate capacitor, which must be charged or discharged each time the MOSFET is switched on or off respectively . As a transistor requires a particular gate voltage in order to switch on, the gate capacitor must be charged to at least the required gate voltage for the transistor to be switched on. Similarly, to switch the transistor off, this charge must be dissipated meaning that the gate capacitor must be discharged. This is why a gate driver is usually needed, especially for high frequencies. A gate driver is basically a power amplifier that takes a low-power input from a controller and produces a high current drive input for the gate of a MOSFET. Making sure there is sufficient current for the charging and discharging of internal capacitor of the MOSFET. For the MOSFET module used to build a 3-phase voltage source inverter it requires sophisticated PWM control signals to turn the power-devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency, and phase of the inverter. These low level control signals are provided by the microcontroller (MCU), and are at low-voltage levels such as 3.3 or 5.0 V. The gate controls required by the MOSFETs, on the other hand, are in the range of 12 to 20 V, and need higher currents to be able to drive the large capacitive loads offered by those power transistors. Also, the

gate drive needs to be applied with reference to the source of the MOSFET and by inverter construction, the source node of top Mosfet swings between 0 to the DC bus voltage, which is 48 Volts. Since the MOSFET floats with respect to ground at the power stage, both the power supply and the gate circuitry should be isolated from the inverter ground. This gives the need for the use of potential isolation between low level and high level signals. The gate driver IC used in this project is a galvanically isolated single channel MOSFET driver IC that can provide an output current of at least 6A and up to 10A at separate output pins with an input voltage range from 3V -15V and consisting of an integrated isolation thus simplifying the design by eliminating the need for a separate optocoupler or an isolation transformer. The figure 4.8shows the gate driver circuit schematic for one phase leg of the inverter circuit. .

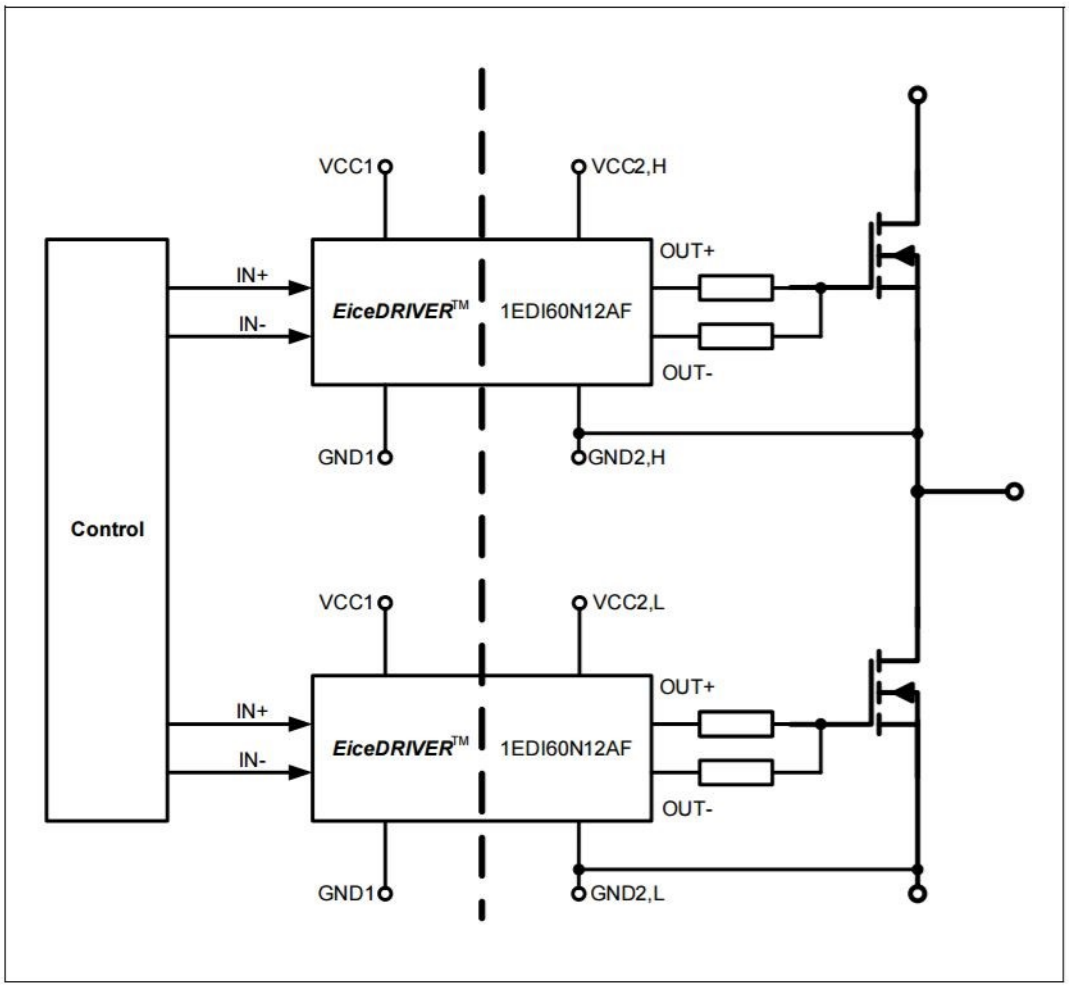

Figure 4.8: Typical application of gate driver IC for phase leg in an inverter.

Gate driver PCB Board Description: The Gate driver PCB consists of:

- Mosfet power module's driver IC. A total of six independent driver ICs are used for driving six switches in the inverter stage. The driver IC is isolated gate driver capable of sourcing a 6A and 10-A sink current to drive the MOSFETs. The PCB footprint supports surface mounting of different electronic

components from different manufacturers.

- A dc-dc converter powered from 48-V main supply with isolated 72-V/-10-V rails is used to power gate drivers.
- Isolated current transducers are used for measuring the phase current. To make the size and cost of the PCB as efficient as possible, only two Hall-effect current transducers are used to measure the two phases of output current which is enough to eliminate any redundancy during the stage when the inverter would be tested along with a motor. The third LEM hall sensor is used to measure the phase current of the full bridge converter that is used for the magnetization of rotor of the electric machine.
- 2000 Launchpad Evaluation board for controlling the inverter and generating the sinusoidal voltage applied to the load is created by using the Space Vector modulation Pulse width Modulation technique implemented in the MCU. The C2000 Launchpad is based around the C2000 Piccolo TMS320F28027 MCU, which features a 60- MIPS processing core, 64-KB integrated flash, and 8 PWM channels with high resolution capability, 12-bit 4.6- MSPS ADC, capture interface, serial connectivity, and more.

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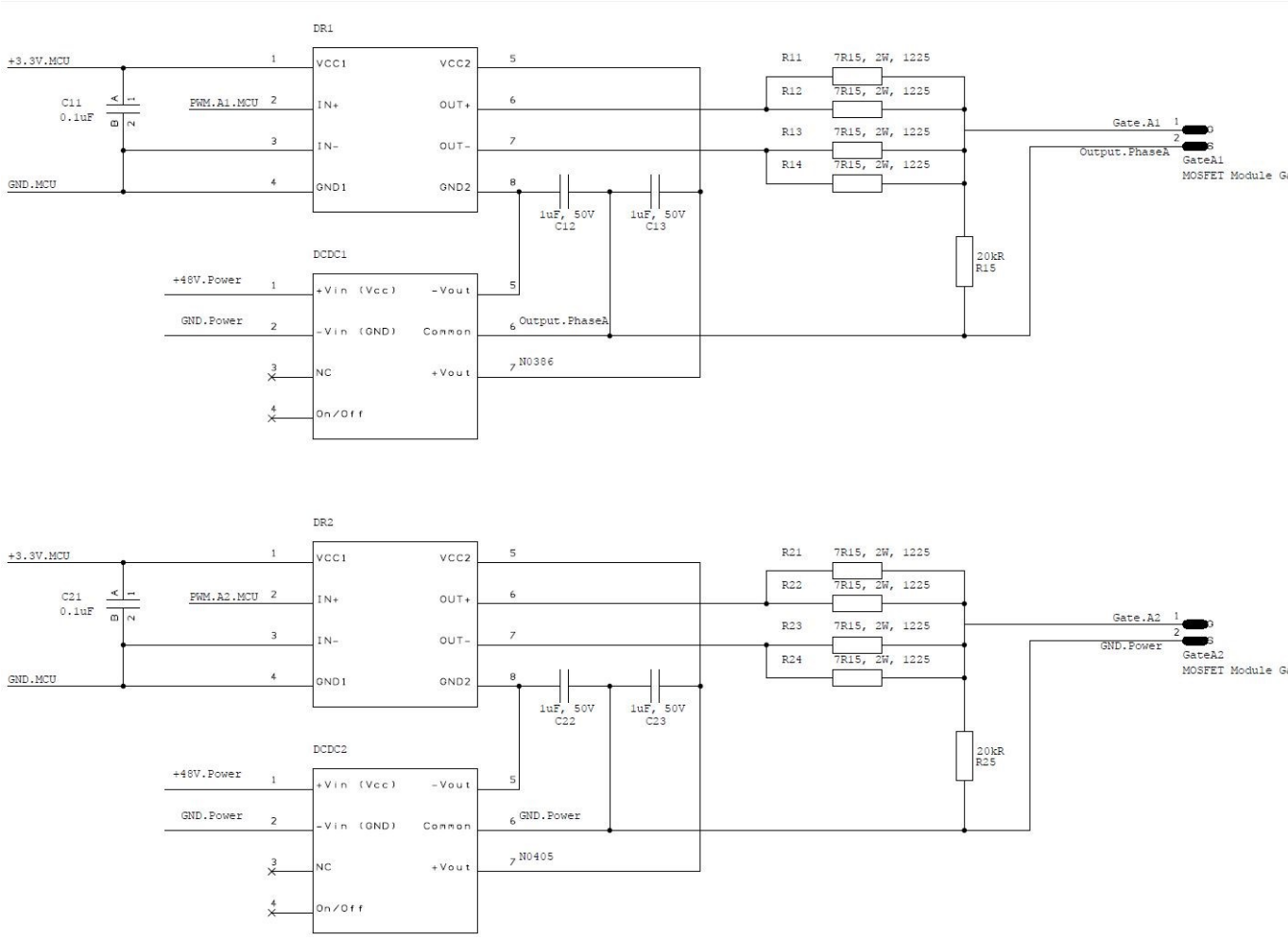

Figure 4.9: Gate driver circuit design.

The gate driver selected for this design is the Infineon's 1EDI EiceDRIVER (refer Appendix C) . The gate driver performs the function of level shifting (3.3 to 12 V) and buffering the PWM output of the microcontroller to the MOSFET gate. Six individual half bridge gate driver IC are used to control the three-phase inverter. The gate circuit for the both the high side and the low-side switch for phase A is described in this section. The sub circuit is shown in figure 4.9. The gate driver PCB is placed as close as possible to the MOSFET module.

The gate driver is powered from the same power supply of 48Vdc and is stepped down to 12V using the dc-dc converter. C1 is the bulk capacitor placed close to the gate driver and helps prevent droop on the 12 VDC rail during load transients. C11 and C21 is the high-frequency decoupling capacitors that that prevents high-frequency current edges from flowing through the long tracks from the power supply input helping reduce noise on the 12-VDC rail. It also helps prevent overshoot and undershoot on the input signals due to the parasitic track or cable inductance from the controller to the gate inputs. The gate drive inputs IN+ is driven from the PWM output pins of MCU, which is connected to the computer using a USB cable. The turn-on and turn-off times of the MOSFETs are independently controlled by placing the gate resistors before the MOSFET gate. A slow turn on is used to minimize overshoot and ringing on the phase output due to unavoidable circuit layout parasitic. The turn on gate current path is through resistor R11 and R12 placed close to the MOSFETs. Similarly the resistors R13 and R14 are used for the turn-off of the MOSFET module. The controlled switching rise time and fall time helps to reduce high-frequency ringing between the FETs due to circuit layout parasitic. The MOSFET can be completely turned on by a V_{GS} of 10 V, and therefore, a VDD of 12 V is enough for such an application.

Rise Time and Fall Time Limits calculation

- **Rise Time Limit:** Overcurrent may happen during capacitive switching action, when the current changes from one diode to the opposite MOSFET on the same leg, i.e. from D- to T+, or from D+ to T-. During the commutation, the reverse recovery charge of the diode needs to be absorbed by the MOSFET.

$$I_{(g.on.max)} < \frac{Q_{plateau}}{t_{rise}} = \frac{660[nC]}{110[ns]} = 5.5[Amp] \tag{4.1}$$

  Where $I_{(g.on.max)}$ is the maximum current required to charge the gate capacitors in order to turn on the mosfet in 110 ns

.

- **Fall time limit:** Overvoltage may happen during the turn-off of the MOSFET and therefore it is required to control the fall time of the MOSFET. The overvoltage happens due the parasitic in the circuit, it is given by:

$$V_{DS} = L\frac{di}{dt} + V_{dc} = L\frac{\Delta I}{\Delta T} + V_{dc} \tag{4.2}$$

  Where, V_{DS} is the maximum drain to source voltage that can be applied without MOSFET module being damaged.
  L = stray inductance in the circuit.
  Δ I = Change in the current from 0 to max value (700 A peak assumed in this case.)
  Δ T = fall time and V_{dc} = applied dc voltage.

Therefore,

$$\Delta T = L_\sigma \frac{\Delta I}{V_{DS} - V_{dc}} = 20 * \frac{700}{150 - 48}[ns] = 137[ns] \tag{4.3}$$

Pulse gate current required to achieve the fall time of 137 ns is given by:

$$I_{(g.off)} < \frac{Q_{plateau}}{t_{fall}} = \frac{660[nC]}{137[ns]} = 4.4[Amp] \tag{4.4}$$

Therefore, the gate driver should maximally give 5.5 A for turn-on, and 4.4 A for turn-off.
The gate driver IC can source and sink up to 10A of current therefore to limit this current external gate resistors are added before the gate of the MOSFET module. $R_{(g.M)}$=0.62 [Ω] (Internal gate resistance of the MOSFET) The value of external gate resistance required to limit the turn ON current to 5.5 A is given by:

$$R_{(gon)} = \frac{V_{GS}}{I_{(g.on.max)}} - R_{(g.M)} = \frac{(12 - 6.5)}{(5.5) - (0.62)}[\Omega] = 3.8[\Omega] \tag{4.5}$$

The value of external gate resistance required to limit the turn OFF current to 4.4 A is given by:

$$R_{(goff)} = \frac{V_{GS}}{I_{(goffmax)} - R_{(gM)}} = \frac{(6.5 - (-12))}{(4.4 - 0.62)}[\Omega] = 3.6[\Omega] \tag{4.6}$$

Average gate current required by the gate drive circuit to charge the gate capacitor is given by:

$$I_{gavg} = Q_g * f_{sw} = 1[\mu C] * 25[kHz] = 25[mA] \tag{4.7}$$

Peak Current required by the gate drive circuit to charge the gate capacitor is given by:

$$I_{(gon-peak)}) = \frac{24}{(3.8 + 0.62)}[A] = 5.4[A] < 10[A] \tag{4.8}$$

(Sourcing current capacity of the driver IC)

$$I_{(goff-peak)} = \frac{24}{(3.6 + 0.62)}[A] = 5.7[A] < 9.4[A] \tag{4.9}$$

(Sinking current capacity of the driver IC)
Average Power dissipated by the turn ON and turn OFF resistor:

$$P_G = Q_G * V_{DD} * f_{sw} = 1[\mu C] * 24 * 25[kHz] = 600[mW] \tag{4.10}$$

$$P_{(on-avg)} = P_G * \frac{R_{(gseries-on)}}{R_(gtotal)} = 600 * \frac{3.8}{(3.8 + 0.62)}[mW] = 516[mW] \tag{4.11}$$

$$P_{(off-avg)} = P_G * \frac{R_{(gseries-off)}}{R_(g - total)} = 600 * \frac{3.6}{(3.6 + 0.62)}[mW] = 512[mW] \tag{4.12}$$

With all the important parameters being identified the gate driver PCB was designed using the PCB design Software called “Design Spark” which is a free tool available online to design the PCBs as shown in figure 4.10 The PCB was manufactured and the components soldered on it took the form as can be seen in the figure 4.11

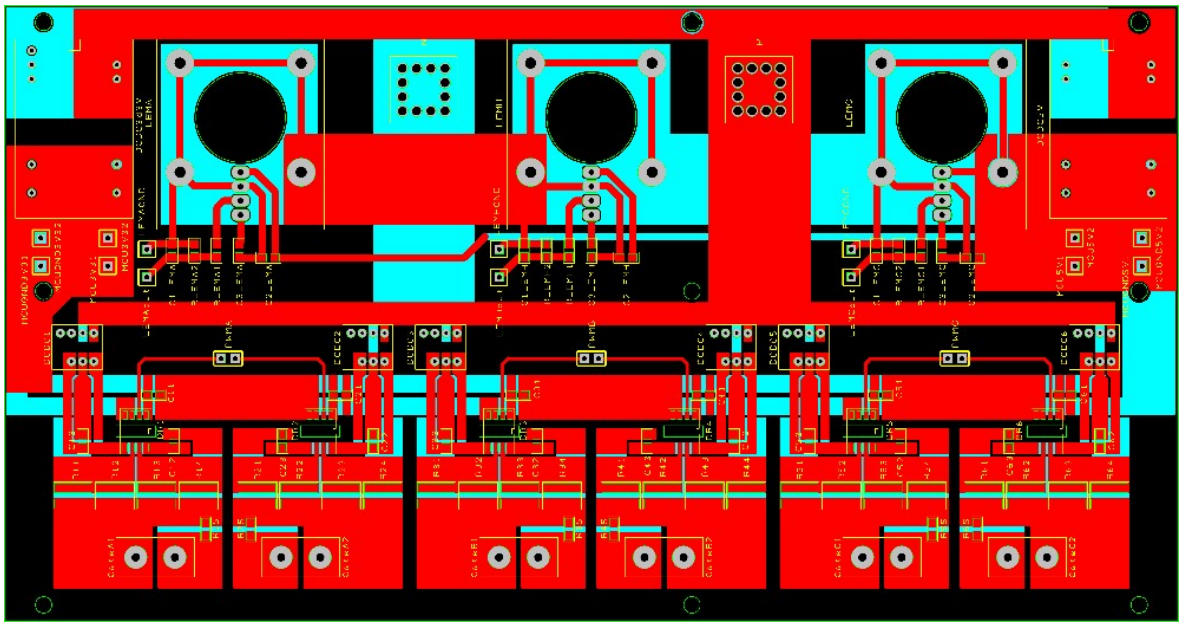

Figure 4.10: Gate driver PCB layout.

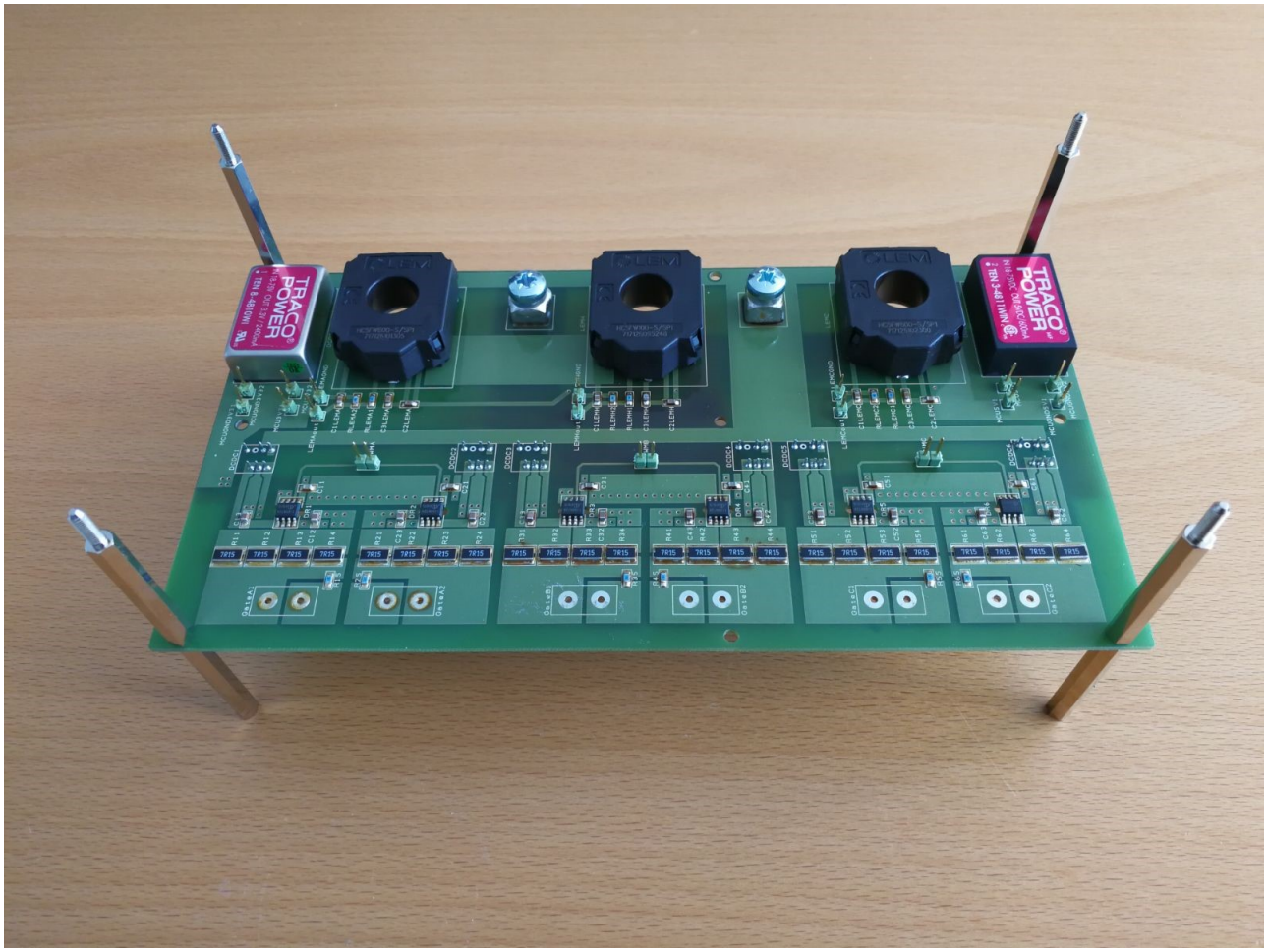

Figure 4.11: Gate driver circuit PCB.

4.1.3 DC Link Capacitance Bank:

In inverters for electric vehicle applications, the DC link capacitor is used as a load-balancing energy storage device. The DC link capacitor is usually placed between the supply side of Dc bus and the AC load side of the voltage inverter. The capacitor is placed parallel to the DC supply, to maintain a stiff DC voltage across the inverter. The capacitor bank also helps protect the inverter network from momentary voltage spikes, surges and EMI. The noise is generated by the pulsed inverter current (which is regulated at high frequencies) and DC Link Capacitor's stray inductance on the DC bus The selection of the proper DC link capacitor and capacitance bank

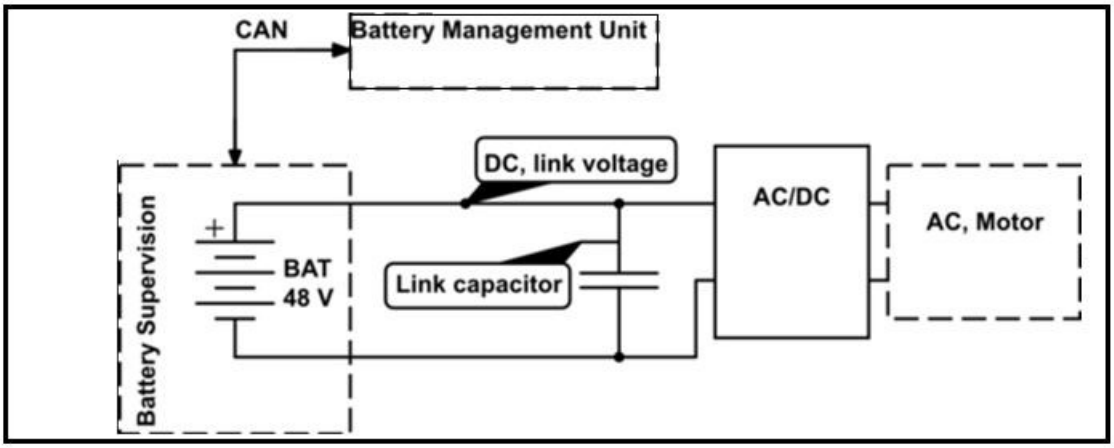

Figure 4.12: Typical Electrical Vehicle's Electrical architecture showing the presence of DC-link capacitor bank.

is important to achieve the proper performance of the system. An under designed DC link capacitor can cause a premature failure of the inverter circuitry as the momentary surges will not be dampened , or, it will cause EMI interference resulting in problems with other electronic circuitry. An over-designed DC link capacitor is not as cost- or size-efficient. Usually, the two most-common capacitor technologies that are used for an inverter are Electrolytic capacitor or the Film capacitor. The electrolytic capacitors provide the advantage of having a large capacitive value in small size and less cost per capacitance. The downside of using them is high Equivalent series resistance (ESR), low temperature operating range and reduced life time [13] The film capacitor offers lower capacitance value but it has other advantages such as high ripple current handling capability, low ESR, higher life-time and better operating temperature range. What can be the best solution depends on lot of factors such as overall system requirements, EMI and EMC specifications, cost or budget for the product to name a few. In this thesis, both the Electrolytic capacitor and Film capacitor (Multi-layer ceramic film capacitor) were studied and their suitability was weighted on the basis two main parameters: Cost and size. The design of the DC link capacitor is mainly dependent on two main criteria of input voltage ripple and output current ripple. For the specifications given by the Volvo Car Corporation on the requirements of voltage ripple i.e. maximum 10% of the maximum DC-bus

voltage and current ripple i.e. Maximum 10% of the output current, the calculated value of the capacitance using the formula:

$$\Delta V(50\%)dutycycle = \frac{V_{bus}}{(32 * L * C * f2)} \tag{4.13}$$

and

$$\Delta I(50\%)dutycycle = 0.25 * \frac{Vbus}{(f * L)} \tag{4.14}$$

The above formula is referred from a scientific article [14]. This gives the capacitance value of around 180μ F. Since this was only the analytic method of estimating the dc-link capacitance requirement at 50% duty cycle, it was decided to have the capacitance safety margin of 100 %. The total capacitance was 407μF. The multilayer film capacitor that was chosen in this project was rated for 100V dc with 22μF capacitance at 0V and 11μF at 50V. Therefore to achieve 407μF of capacitance, 37 film capacitors were arranged in parallel (25 on the top face of the PCB shown in figure 4.13 and the remaining 12 on the bottom face of the PCB in figure on a separate PCB which was then connected using the bolts directly to the positive and negative terminals of the three mosfet module. The arrangement of the capacitors

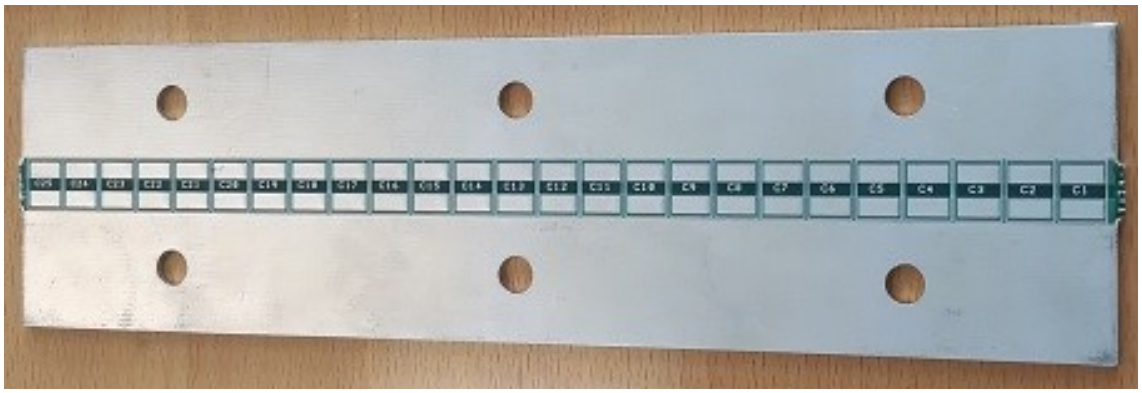

Figure 4.13: DC link capacitor bank designed by using ceramic film capacitor connected in parallel on a seperate PCB

is marked from C1-C25. The six holes on the PCB are to connect to the positive and negative terminals respectively of the three mosfet modules. To make the PCB handle large ripple current and also provide better thermal relief most of the PCB was covered with solder mask. To reduce the stray inductance, the commutation current loop was made as small as possible by keeping the capacitors as close as possible to the mosfet switches.

4.1.4 Cooling System

In order to increase the system's performance and durability under continuously high loading of the integrated starter generator (ISG) motor and inverter the heat dissipation requirements should be met [15]. Most applications have power dissipation losses that ranges from hundreds of watts to few kW. However, waste heat for electric drive train converters can be as high as several kilowatts. Also, electronic

cooling designs are required to dissipate heat and be reliable in ambient temperatures ranging from -40°C to 150°C depending on the product mounting location within the vehicle. As a result, drive train applications require the use of high-performance cooling systems. The most commonly used are forced cooling solutions either air cooled system or liquid cooled system. This thesis was the follow up of a study from the "Design Project" course at the Department of Electric Power Engineering at Chalmers University in Gothenburg, Sweden where it was studied and decided that the water cooling solution will result in the most compact and robust design of the inverter, therefore, it was decided to go ahead with the water cooling solution. The cooling system assembly consisted of two plates a liquid cooling plate with the semiconductor components placed on top surface of the plate with water running across the serpentine shaped channels which were to be milled and a cover plate to seal off the entire assembly. These plates were mounted together using the screws. The sealing of this assembly was ensured by a rubber ring the blue shaped ring shown in the figure 4.14. To validate the design several attempts were made

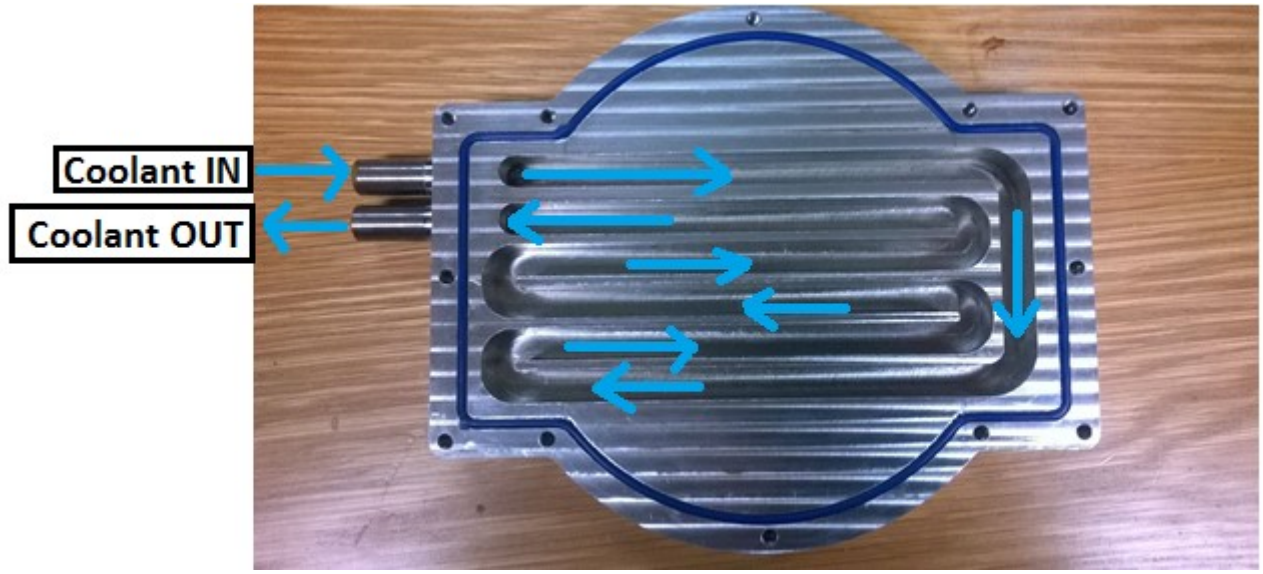

Figure 4.14: Heat Sink showing direction of water flow.

to calculate the heat dissipation rate by the help of advanced CFD simulations but due to the lack of time the model was never fully developed. The best available simulations at that time however gave some understanding on the process of heat flow.

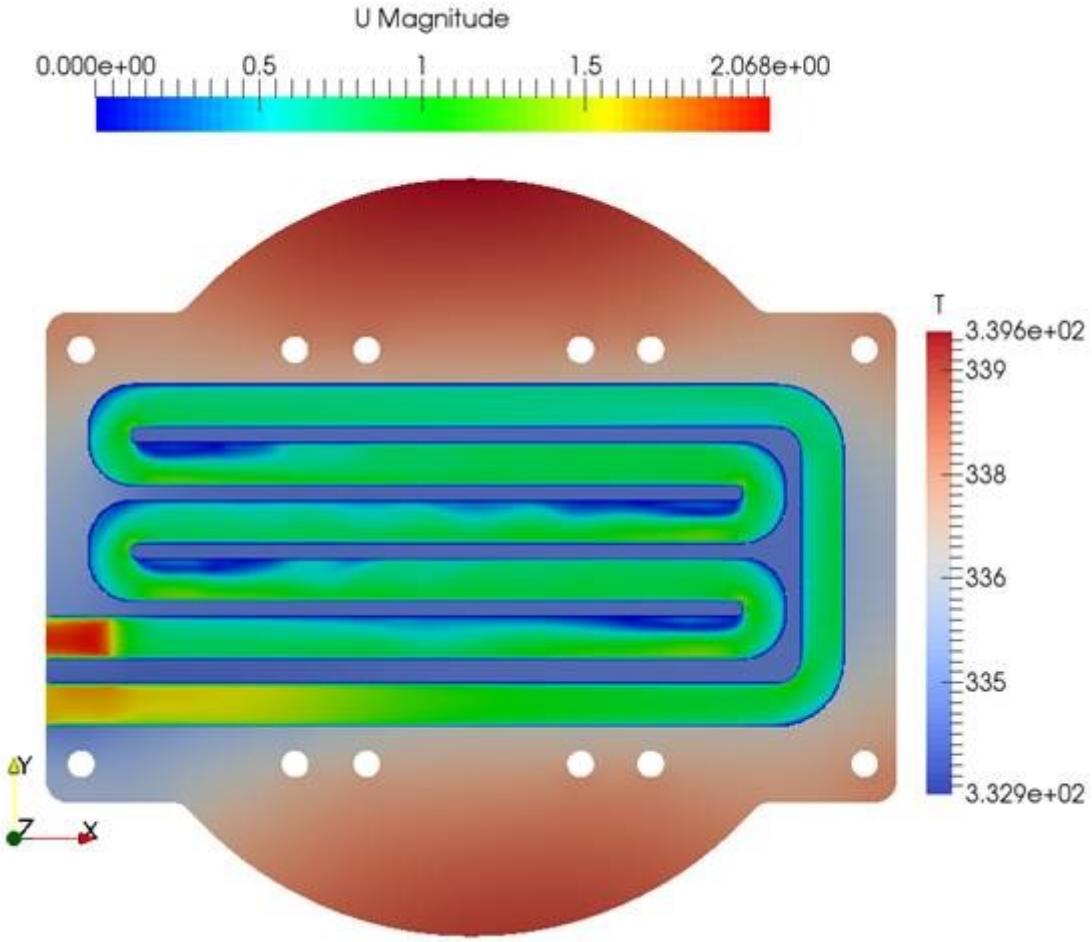

Figure 4.15: Flow Velocity Profile in the cooling channel.

The cross section of top face of the heat sink is shown in the figure 4.15 along with the fluid flow profile that illustrates the flow of water in the channel at a rate of 13L/minute. The flow profile is mostly smooth with some high velocity profile and therefore greater losses towards the outlet end of the heat sink. The holes seen in this figure are the ones that were used for the mounting of the Mosfet module. The flow velocity and the profile could have been more optimized by using the flow straighteners built inside the channels but since the overall flow profile was smooth enough it was decided not to introduce any flow straighteners due to the lack of simulation results with that feature added. The simulation was done with a water flow rate of 13L/minute, where only the heat transfer between mosfet module and heatsink was considered. The figure 4.16 shows the temperature distribution on the top surface of the heat sink. In this figure 4.16, the top surface is modelled as constant power source generating 300 W of total losses which are assumed to be dissipated as heat into the Aluminium block and the heat dissipation to the surrounding by radiation or other phenomenon have been neglected. The 300W losses is a conservative estimation of the normal operational condition based on the power dissipation estimations done before in the design project. At a total losses of 300W, and the inlet water temperature at 40 degrees with a flow rate of 13L/minute,

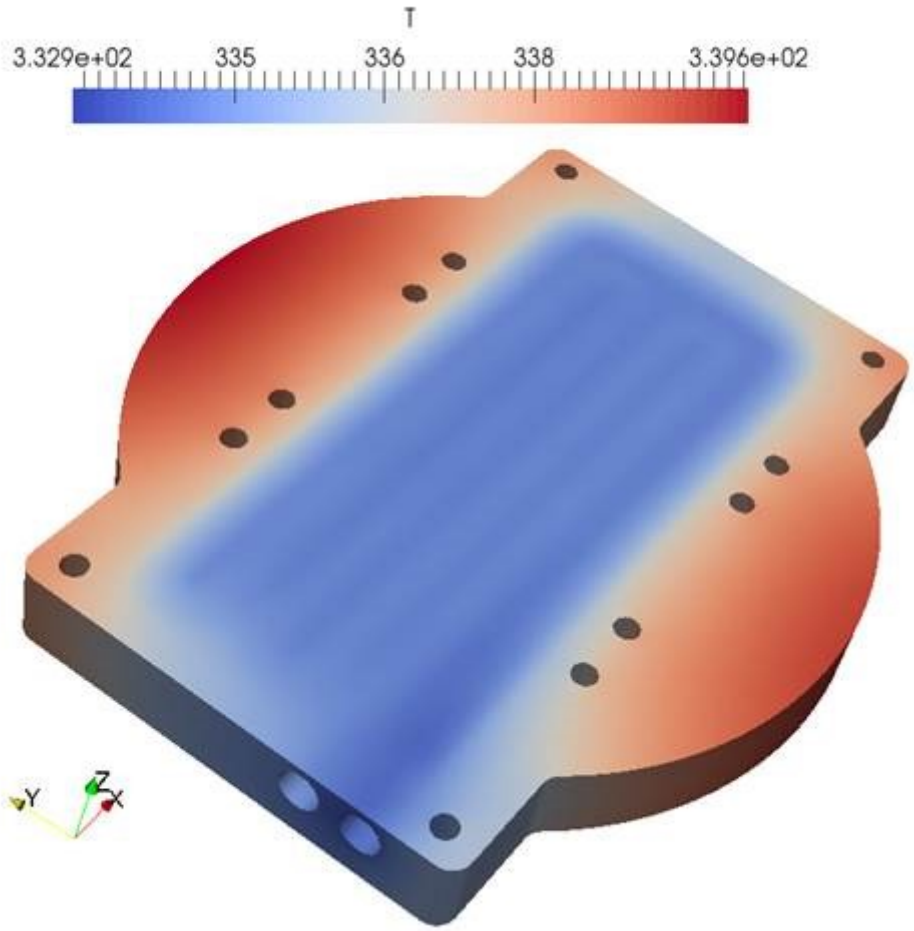

Figure 4.16: Heatsink simulation of temperature distribution.

the water can take out at least 300W of total losses from the top surface of the cooling plate which is good enough to keep the mosfet modules at a temperature much below their thermal breakdown rating of 150 degrees as given in the manufacturer's datasheet. This simulation is based on a lot of assumptions but it gives a rough estimate and some information on the expected thermal behaviour of the heat sink and therefore helping in making a decision to proceed with manufacturing of this design.

5
Results

The main idea behind design validation was to test the designed gate driver circuit board for its functionality, the micro-controller board and the entire inverter assembly against the predefined system requirements set on the performance of the inverter earlier during the design phase of the project. The series of test were carried out to validate the effective working of above mentioned designed PCB's and the inverter circuit.

5.0.1 Gate driver circuit Test and Initial Test on Power Module.

The first testing was done on the gate driver circuit board with only the gate driver interface. This circuit board was tested to see whether the driver IC's were producing the desired switching for both the upper leg and the lower leg. The PWM signals required to switch the gate driver were generated from a microcontroller board with the dead-time of around 90μ seconds. Since the controller at that time was not programmed to generate the three phase PWM, therefore the driver circuit was tested with one phase leg at a time. The figure 5.1 below shows the switching waveforms of the driver circuit board.

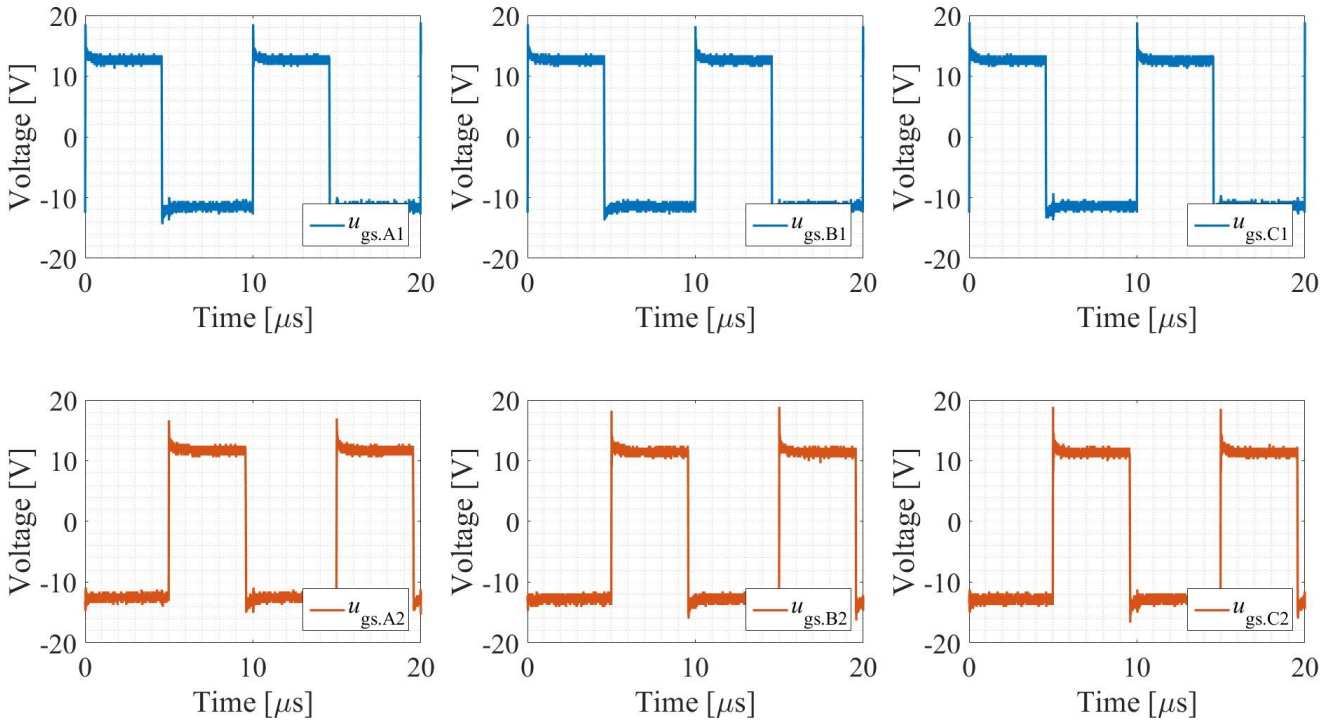

Figure 5.1: Waveform of Driver IC

As described above each leg was tested individually to observe the switching waveform and as can be seen in the figure, the driver IC's are switching properly with small Voltage spikes that have been generated due to high switching frequency of 25 kHz and also because of the stray inductance introduced on the gate driver IC by the measurement set-up.
Next step carried out in the testing was to determine whether the gate driver board was able to turn-on and turn-off the MOSFET module. The measurement setup is shown in figure 5.2

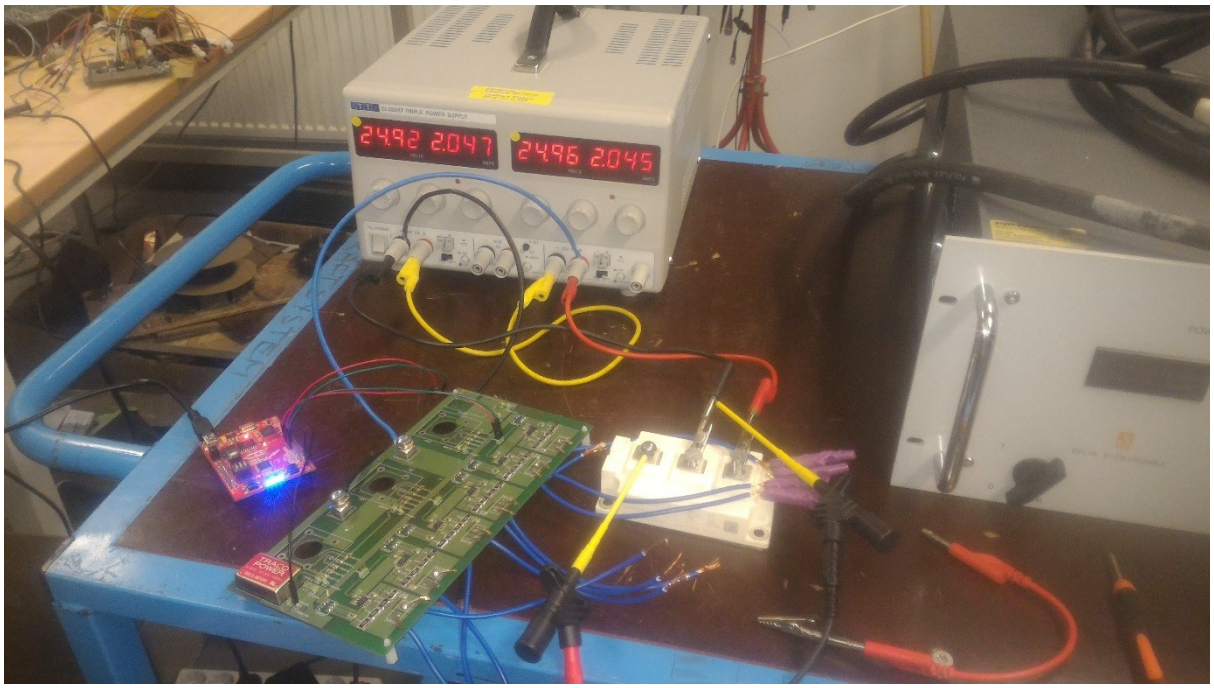

Figure 5.2: Measurement setup for testing Gate driver board on Mosfet Module.

With the applied Voltage of 24V between the drain and source of the Mosfet module, the driver board was able to switch on and switch-off the Mosfet module as can be seen in the figure 5.3 and figure 5.4
The waveform recorded by the oscilloscope, measuring the voltage between the gate and source of the Mosfet's both upper and lower leg respectively. At this stage the gate-source voltage looked fine with some spikes introduced by the switching frequency. The applied voltage between the Drain and source of the mosfet module was then increased from 25V up to 50V which was the operating voltage levels in this project.
Even before one could realize, this resulted in the immediate breakdown of the Mosfet module under test. The reason for the immediate breakdown was because of the overvoltage spike across the drain and source of the lower leg of the Mosfet module.

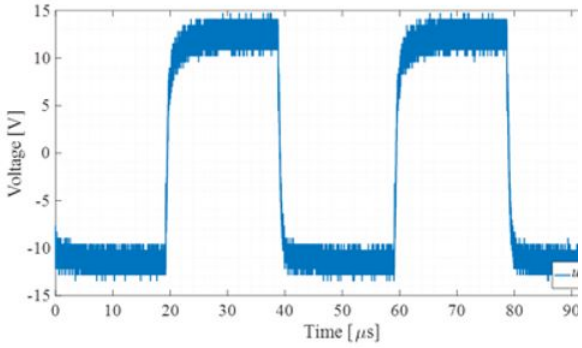

Figure 5.3: Mosfet G-S (V) upper leg.

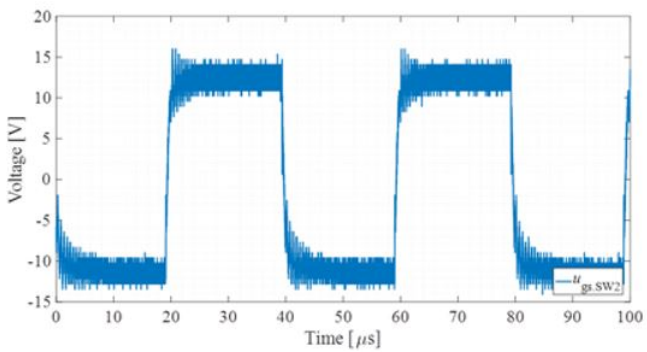

Figure 5.4: Mosfet G-S (V) lower leg.

This kind of Mosfet Modules are very sensitive to voltage spikes and the electrostatic discharge caused from the presence of stray inductances and high switching frequencies of these modules lead to their immediate breakdown. The new Mosfet module was then tested again this time with a small 300nF film capacitor placed across the drain and source tabs of the Mosfet module. The figure 5.5 shows the waveform recorded by the oscilloscope before and after the addition of a small film capacitor. The blue waveform shows the voltage across drain and source of the mosfet module without the capacitor and the orange waveform shows the voltage across drain and source after addition of a 300nF film capacitor. As observed, the addition

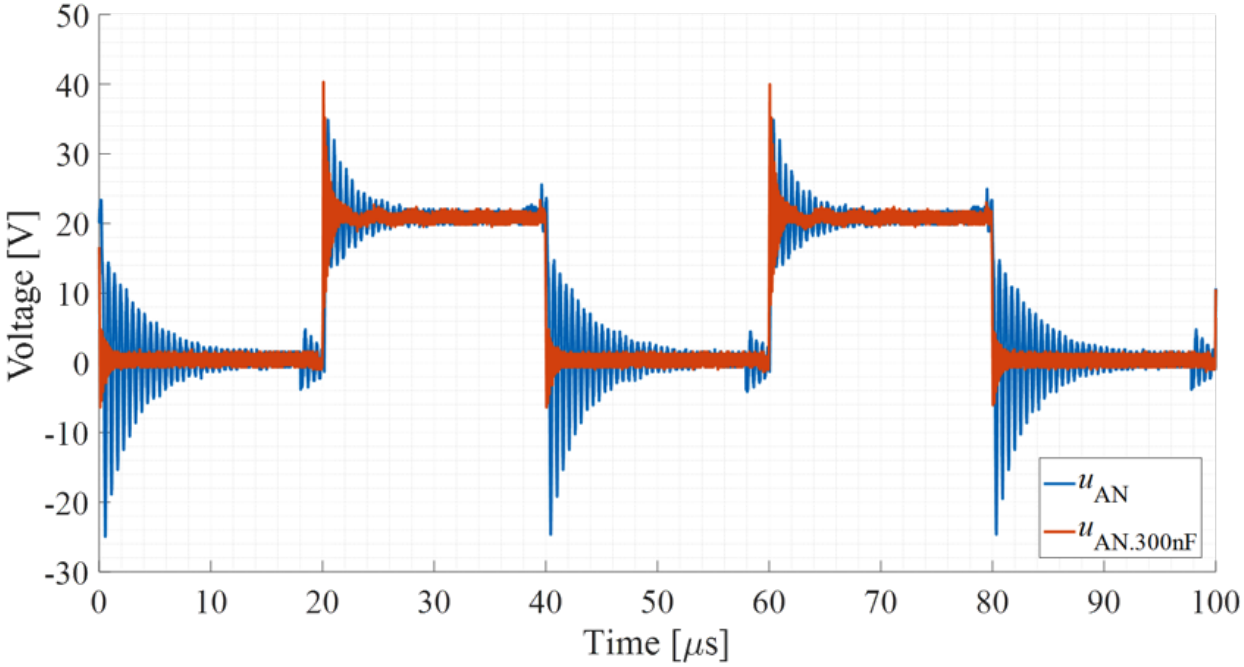

Figure 5.5: Gate waveform with and without capacitor.

of capacitor reduces the turn-on ringing quite significantly but does not reduce the turn-off overshoot. An approximately 100% overshoot has been measured at the turn-off with the applied voltage of 20 V-dc. It was then decided that all the further testing would be done with a proper inverter assembly including the designed dc-link capacitance bank, the three phase SVPWM programmed microcontroller along with proper measurement set-up.

5.0.2 Inverter Assembly Test and Measurement Setup

The inverter circuit was assembled in order to have a proper measurement set-up and continue forward with the functional design verification of the inverter. The three Mosfet module that comprised of six inverter switches, were mounted on the heat sink which was previously manufactured and assembled. The driver PCB, Dc link capacitor PCB, Full bridge converter PCB for the rotor excitation of the EESM and the microcontroller board along with DC-positive and negative bus-bars connecting

the drain and source of all the three Mosfet module's tabs were assembled together. The total vertical height of the converter ended up at 120mm. The figure 5.6 shows the final assembled VSI

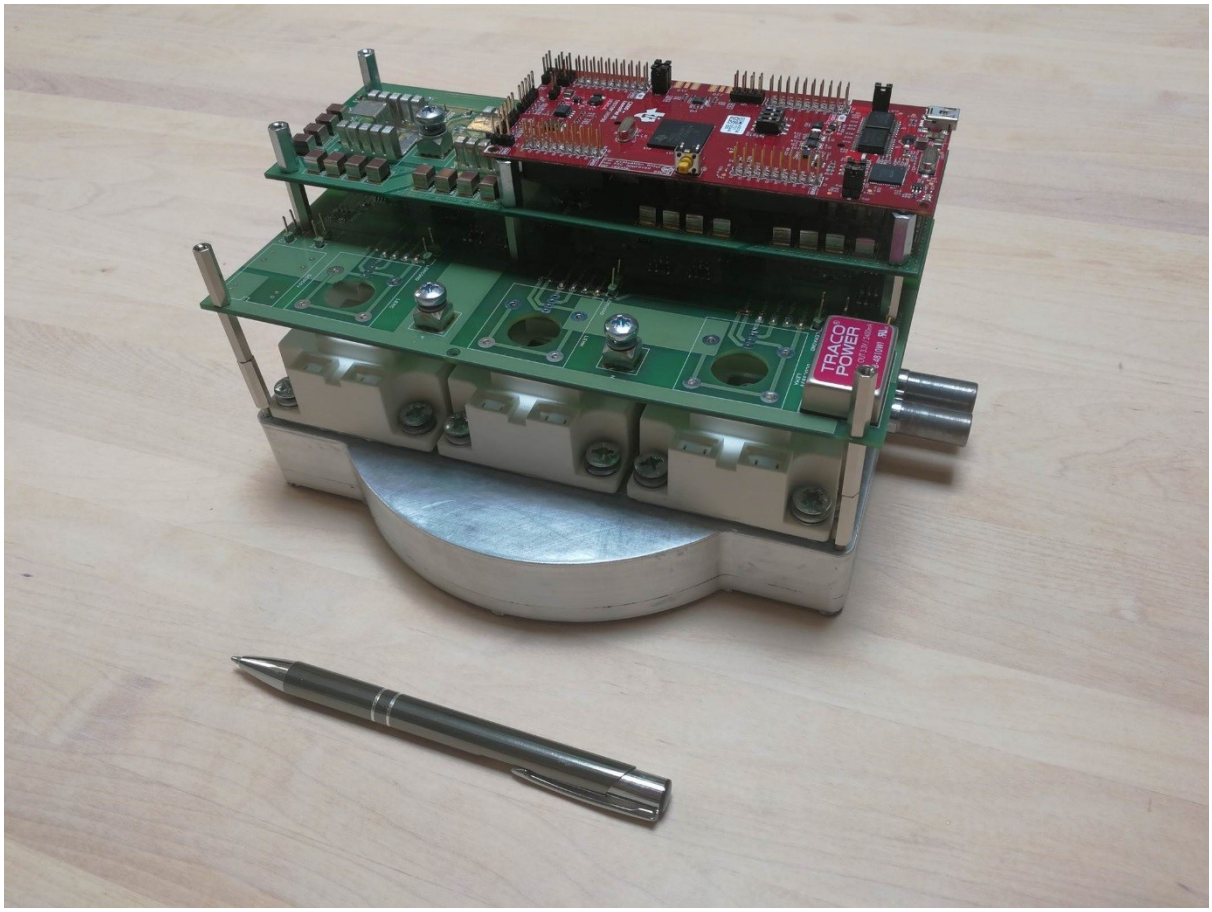

Figure 5.6: Inverter full assembly.

5.0.2.1 Three phase no load test

The functional validation of the complete assembly was carried out by performing the series of tests starting with the no load of the inverter. The SVPWM technique was used to generate the three phase switching signals. The thermal behaviour of the driver circuit was an important aspect to note here since the driver circuit was put into full function of turning on and of the three phase VSI. Initially, the heat-sink wasn't connected to any external cooling because the tests were performed at no load. The strategy for testing the complete inverter assembly was to start with very low DC voltage levels i.e. at 25V and slowly increase the voltage levels in the step of 5 volts until the supplied Dc voltage was 60V. This was done in order to be sure about the voltage spikes that might be possible during the switching cycle of the inverter. The waveforms were recorded at each step.

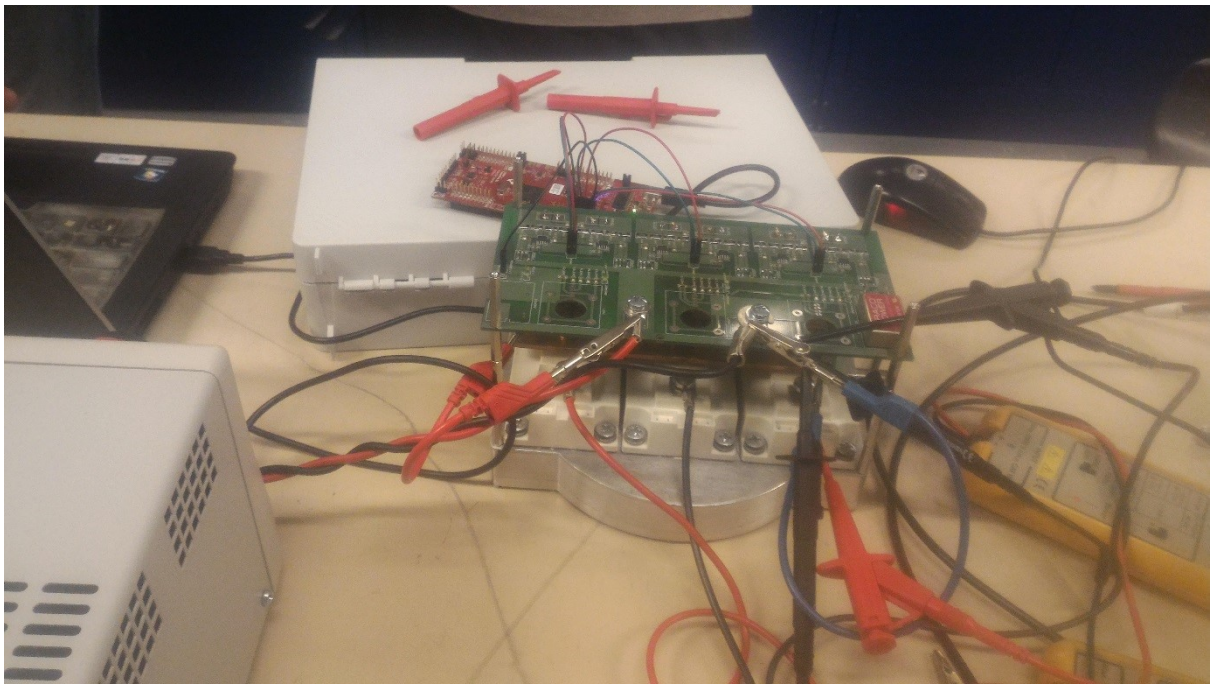

Figure 5.7: No load test Measurement setup.

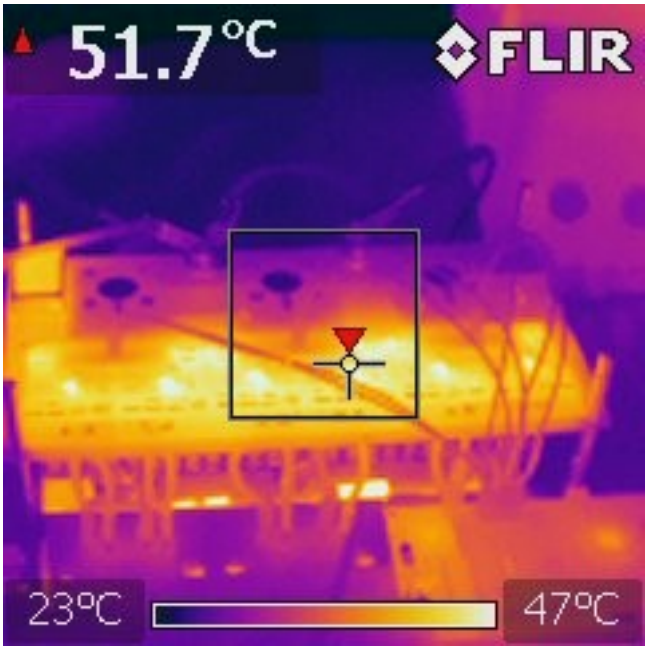

Figure 5.8: Thermal profile of gate driver PCB recorded using a thermal camera.

The temperature of the driver circuit was monitored throughout the test procedure using the IR camera. The figure 5.8 shows the image of the temperature distribution across the driver board at the supply voltage of 60V dc. The highest temperature was recorded on the middle part of the driver board and the maximum heat dissipation was across the external gate resistors. The temperature on the gate driver board became stable at 52deg C after about 5 minutes of continuous operation. The driver IC, the external gate resistors and all the other components on the driver board

have a temperature rating of over 100 deg C. For the driver PCB to be functionally validated it was necessary to observe the voltage waveform and to make sure whether it was switching the mosfet modules as desired. The figure xx shows the voltage waveform across drain to source for both upper and lower legs of the three phase VSI. At the applied dc voltage of 60V dc the maximum voltage peak to peak was 75V. The voltage spikes were much higher at lower voltage levels but as the supply voltage was stepped up the spikes were almost negligible and as seen in the figure 5.9 the voltage across drain and source of both the upper and the lower legs of the three Mosfet modules converges towards the supply voltage of 60V dc. Since the mosfet

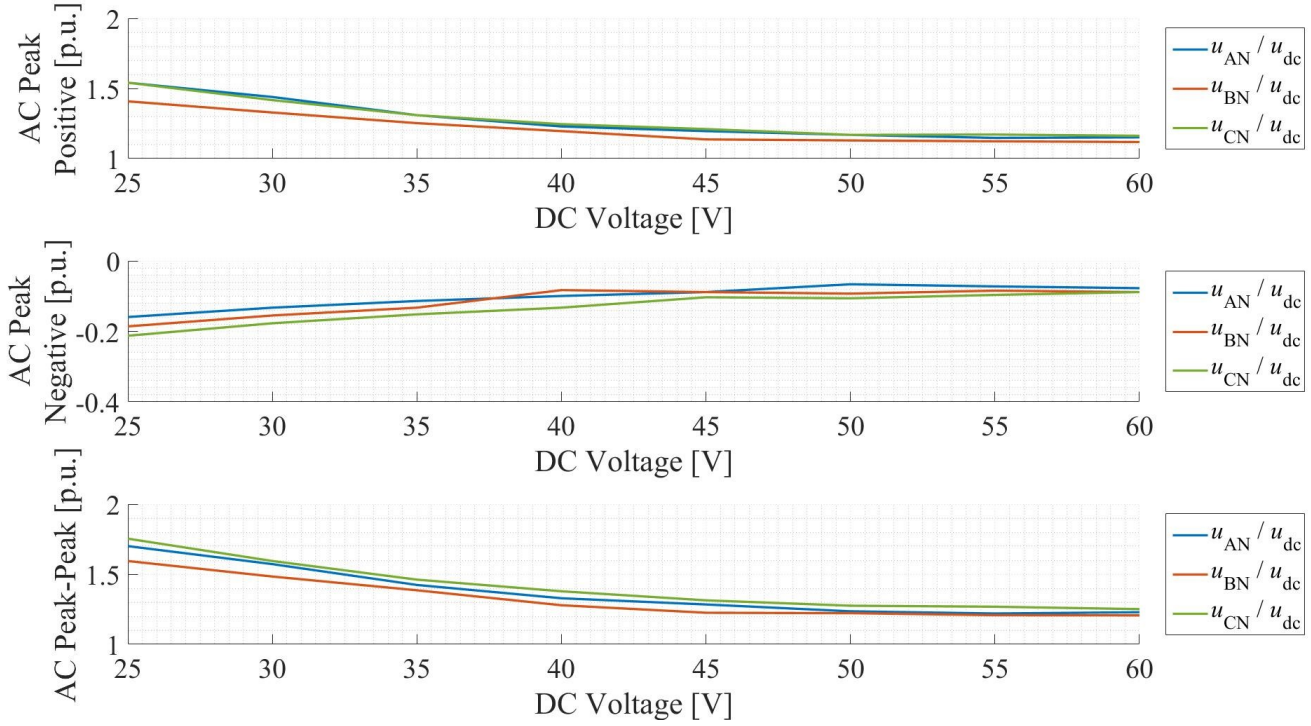

Figure 5.9: Voltage across drain and source of both the upper and the lower legs of the three Mosfet modules.

modules are rated for the breakdown voltage Vds of 150V, the mosfet modules are safe for operation at no-load. Hence, the driver board was tested functional and ok.

5.0.2.2 Three Phase resistive load test

The next phase of the functional validation was done by connecting a small resistive bank. Each resistor in the resistor bank is of 10Ω and is rated at 100W. The controller was set to generate the SVPWM signals at a duty cycle of 0.9. With the AC fundamental frequency set at 250 Hz, the inverter was switched at 25 KHz switching frequency. The measurement set-up for this test is shown in the figure xx. The supply voltage was set at 48V dc and each resistor of 10Ω was connected across the each phase output in order to give the symmetrically balanced active load. The gate driver and the inverter circuit are supplied by the same DC source of 48Vdc. To cool off the heat dissipated by the resistor bank, a small fan is used to blow the

air that is fed 12V by the separate dc-supply. The test waveforms of both voltage and current are measured using the probes and recorded on the oscilloscope. The recorded data was then processed with a matlab code to generate the waveforms.

Figure 5.10: Measurement set-up for resistive load test.

The obtained waveforms for the phase voltage and current can be seen in the figure 5.11 As can be seen in the figure 5.11, the peak to peak output voltage is not more

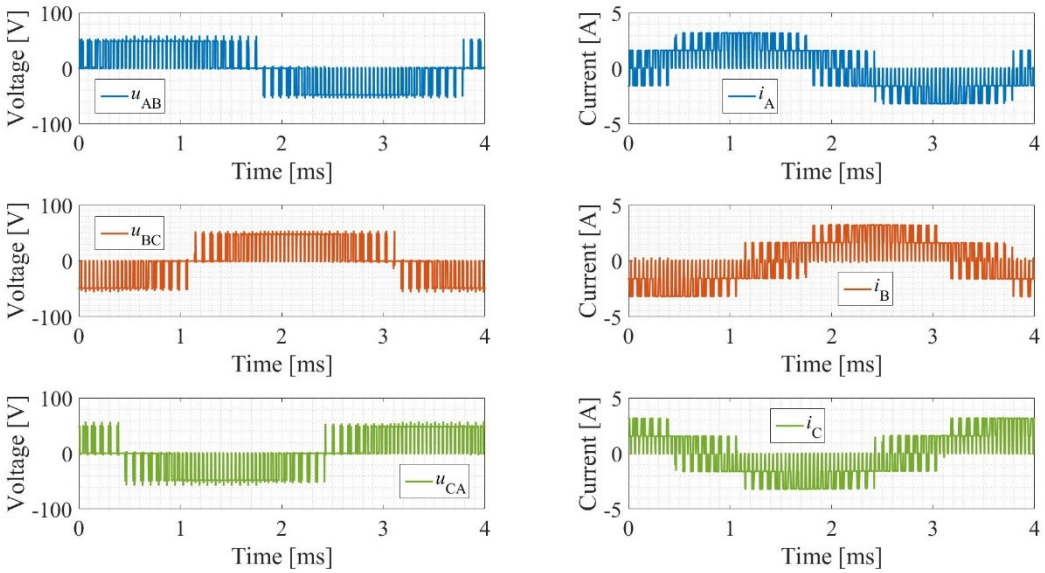

Figure 5.11: Measurement set-up for resistive load test.

than 60 V which well under the limit of the breakdown voltage of the switches. The output current waveform looks as expected and the figure 5.12 shows the output power (both Active and reactive) from the inverter. The average reactive power in

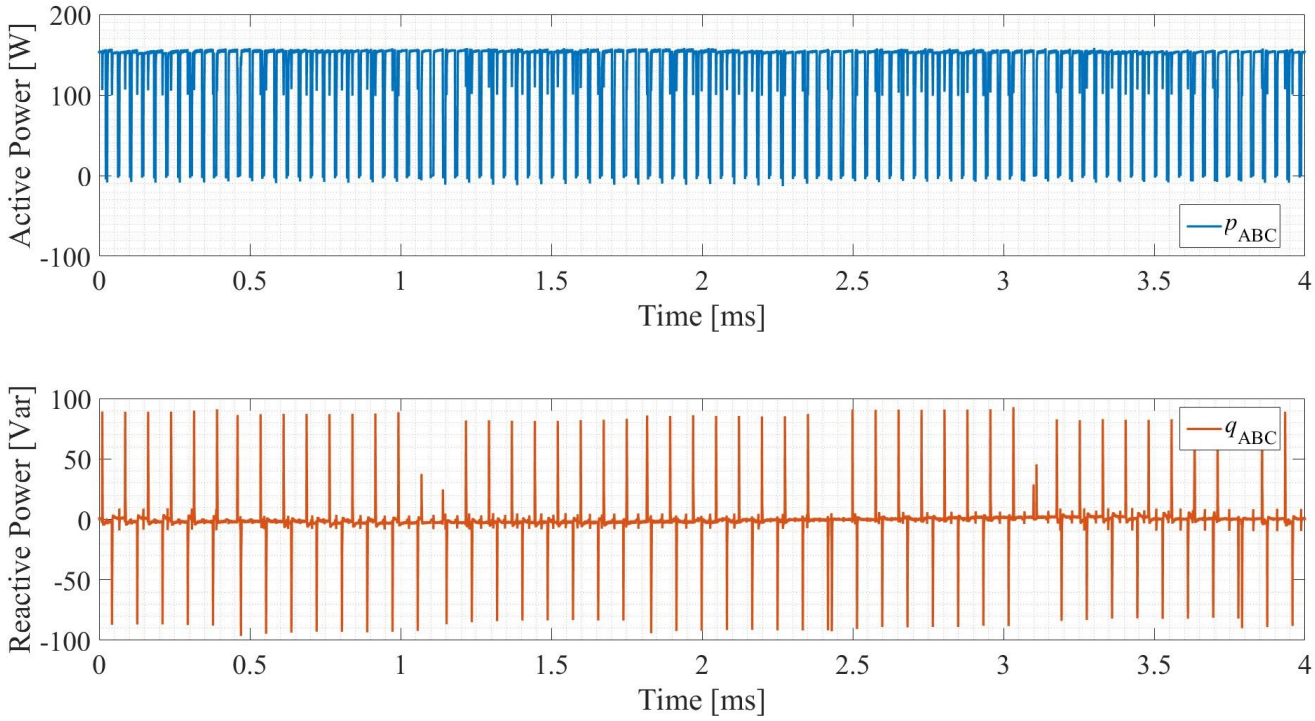

Figure 5.12: Measurement set-up for resistive load test.

this test was measured to be 127 Watts. The resistor connected at the output as the load were already too hot within 5 minutes of operation since the power dissipation was above the rated power dissipation of the resistor, the test with the resistive load was then not continued. The gate driver PCB board's temperature was monitored using the IR thermal camera and the temperature stabilized at around 59degC.

5.0.2.3 Three Phase Inductive Load Test

To test the power output performance of the inverter the tests were performed using the purely inductive load i.e. a transformer as the load. The load was composed of balanced 1mH three phase star-connected transformer. The reason for choosing this type of load was due to the unavailability of the electrical machine during the time of testing and to also eliminate the amount of heat that would be dissipated by the resistive load. The schematic of the laboratory set-up to perform the inductive load test is shown in the figure 5.13 To monitor the temperature rise of the heat sink

Figure 5.13: Measurement set-up for inductive load test.

an IR thermal camera was always used. Various components including the mosfet switches and dc-link capacitors were monitored for the temperature rise. The main goal of running this test was to determine the output power capability and to push the inverterto deliver more output power. During the test the gate to source voltage waveform of the Mosfet module consisted of lot of oscillations. One possible reason for this could be the presence of stray inductance that might have been introduced across the gate and source of the module due to the distance between the gate driver PCB and the Mosfet module. To overcome this problem film capacitors of value 300nF were soldered on the kelvin gate and source pins of the mosfet modules externally. The gate-source voltage waveform became smoother after the addition of capacitor. The figure 5.14 shows the gate-source voltage waveform before and

after the addition of capacitor. The figures on the left side are the ones after adding the capacitor across the kelvin pins of the module while the ones on the right are the before the addition of capacitor. As it is observed in the figure, the gate-source voltage waveform is relatively smoother on the left side than on the right side. As

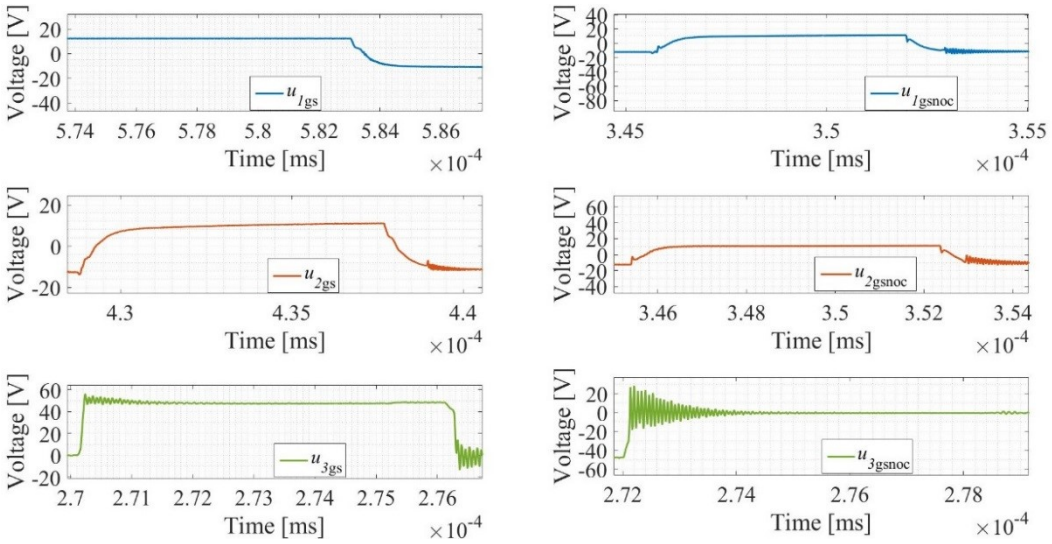

Figure 5.14: Gate-source waveform after adding film capacitor (right) and before adding film capacitor (left).

can be seen the waveforms on the left hand side are comparatively "smoother" than the ones on the right hand side. The amount of ringing and unwanted oscillations were also damped by the addition of the film capacitor on the gate pins of the mosfet module.
As can be seen in figure 5.15, the voltage and current waveforms appear as expected, with load current waveform being almost sinusoidal with small ripples. The output voltage as can be seen in the waveform has small overshoots but these overshoots are still much below the breakdown voltage of the switches. The dc voltage at this stage of the test was stable as can be seen by the black curve in the top of figure 5.15. The table 5.1 shows the output results obtained with the load connected in star at the supply voltage of 48V dc and ac fundamental frequency of 250Hz with SVPWM switching frequency at 25 KHz with a duty cycle of 0.9

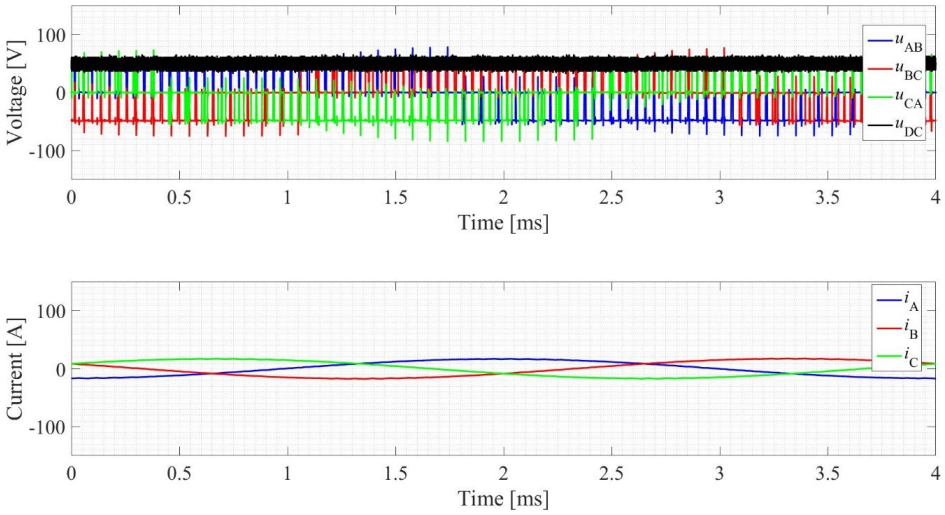

Figure 5.15: Voltage and current waveform in star connected inductive load test.

Table 5.1: Star Connected Inductive Load at 48Vdc

	VOLTAGE				**CURRENT**				**POWER**		
	Ph. A	*Ph. B*	*Ph. C*	*Av.*	*Ph. A*	*Ph. B*	*Ph. C*	*Av.*	*P*	*Q*	*S*
	V [rms]	V [rms]	V [rms]	V [rms]	A [rms]	A [rms]	A [rms]	A [rms]	[W]	[Var]	[VA]
RMS	36.50	36.49	36.63	36.54	11.81	12.22	11.98	12.00	-	-	760.04
Inst.	-	-	-	-	-	-	-	-	83	633	638.10

Since the inverter was operating normally during this test, it was then decided to change the connection configuration of the load by connecting the load in delta instead of star. As stated earlier, the aim of this test was to investigate the output power capability of the inverter. By changing the values of supply dc voltage, ac fundamental frequency and connection configuration of the load different level of output power could be achieved. The figure 5.16 illustrates the waveform of phase current and voltage. As can be seen clearly, the current waveform is quite sinusoidal with small ripples which is due the fact that there is no output filter to filter out the various other frequency component in the output current waveform. The table 5.2 presents the results of the delta connected load at the supply voltage of 48V dc and ac fundamental frequency of 250Hz with SVPWM switching frequency at 25 KHz with a duty cycle of 0.9 The output power from the inverter was around 2kVA. At this point the temperature of the heat sink was still around room temperature and both the gate driver PCB and the dc link capacitors were still much lower than the highest temperature rating of them therefore the need for external forced cooling was not realized.

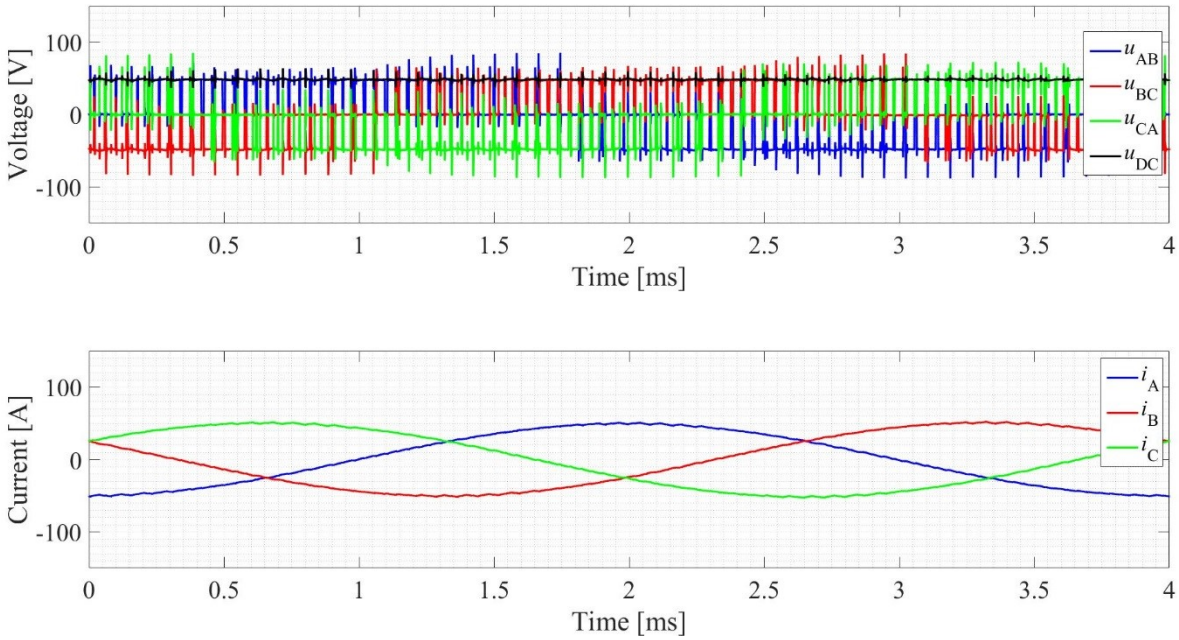

Figure 5.16: Voltage and current waveforms in Delta connected inductive load test.

Table 5.2: Delta connected inductive load test results

	VOLTAGE				CURRENT				POWER		
	Ph. A	*Ph. B*	*Ph. C*	*Av.*	*Ph. A*	*Ph. B*	*Ph. C*	*Av.*	*P*	*Q*	*S*
	V [rms]	V [rms]	V [rms]	V [rms]	A [rms]	A [rms]	A [rms]	A [rms]	[W]	[Var]	[VA]
RMS	36.51	36.47	36.57	36.52	35.30	35.87	36.13	35.77	-	-	1.89k
Inst.	-	-	-	-	-	-	-	-	235.5	1.88k	1.97k

5.0.2.4 Five kW Test

During the early design phase of the project, the specifications of the inverter were described and one of the key specification around which most of the design was based was to deliver an output power of 5kW for a continuous duration of time. To test this requirement, the load was changed from a delta connected 1mH transformer to a three phase step up transformer along with resistive load in series. The schematic of the measurement setup is shown in the figure 5.17.

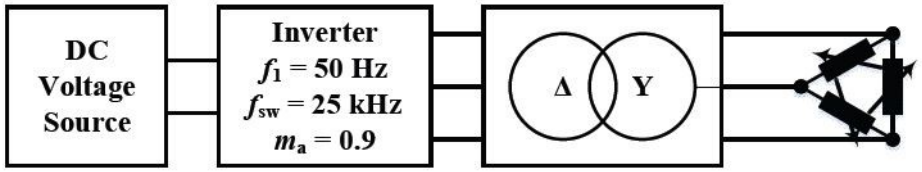

Figure 5.17: The schematic of the measurement setup for 5kW output power test.

The DC power from the voltage source is converted to AC power through the inverter, and then the AC power is delivered to a three-phase load through a Δ - Y connected transformer to step up the voltage by a ratio of approximately 10. Figure 5.18 shows the measurement set-up in the laboratory.

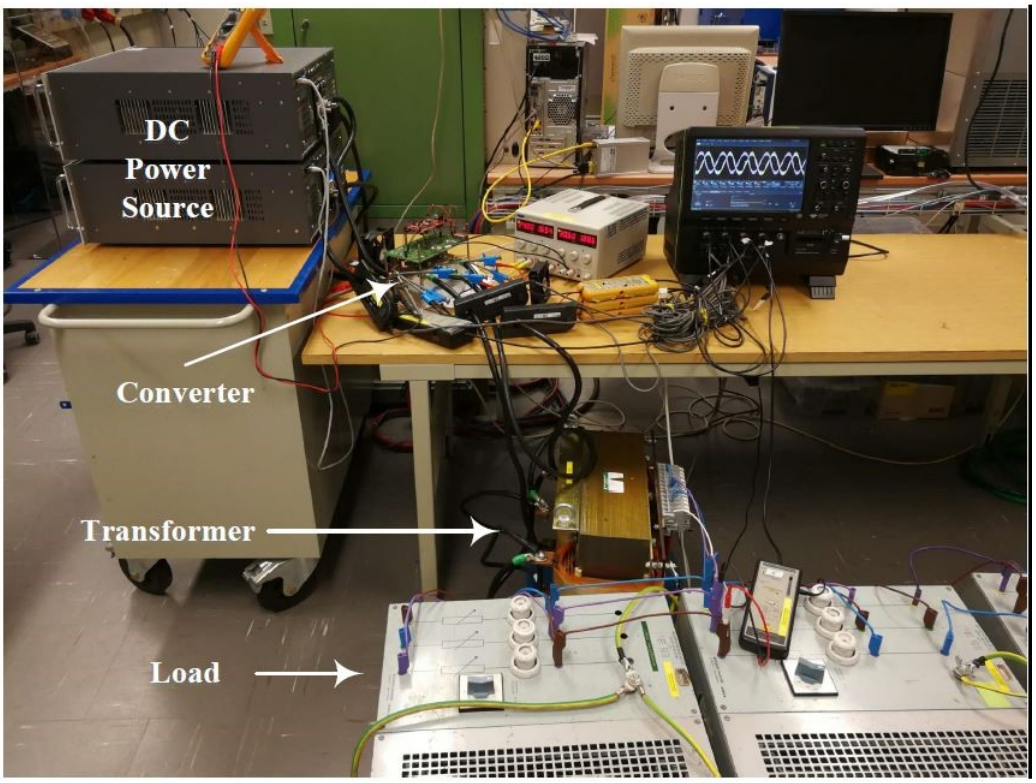

Figure 5.18: Actual image of the measurement setup for 5kW output power test.

The voltage waveform of the phase A, B and C is shown in the figure 5.19. With the supply for voltage of 48V, peak to peak spikes are well below under the voltage breakdown rating of the mosfet switch. As it can be observed in the figure there are

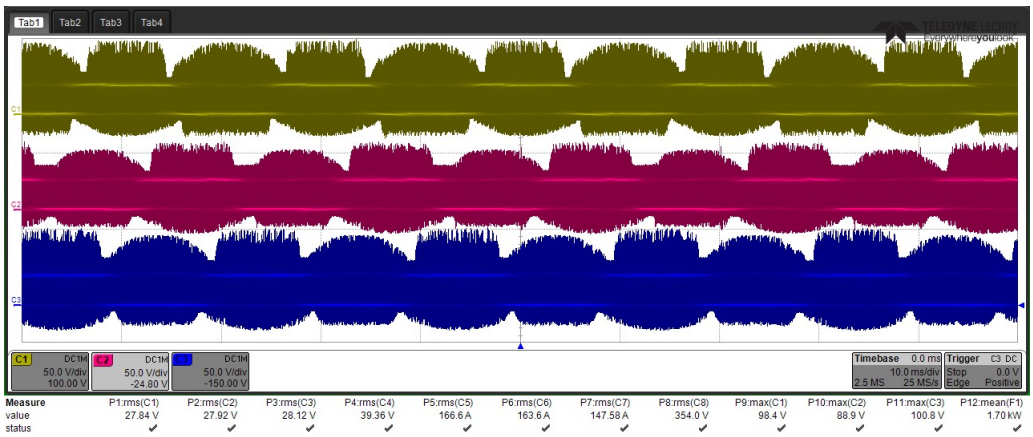

Figure 5.19: Obtained phase voltage waveforms for 5kW output power.

a lot of ripples in the phase voltage. This is further investigated and a Fast Fourier

Transform of the voltage ripple is performed which shows the presence of higher frequency components than the fundamental frequency which explains the presence of ripples in the voltage waveform. One solution to make the output phase voltage smoother is to design a low pass filter that will allow the fundamental frequency component to pass through it and block the other harmonic components. The figure 5.20 illustrates the phase current waveform recorded from the 5kW continuous operation test. Only two phases (A and C) have been measured in this test. The phase current of the third phase can be calculated or determined from the 2 phases. As it is observed in the figure 5.20 the current waveform is quite sinusoidal with very

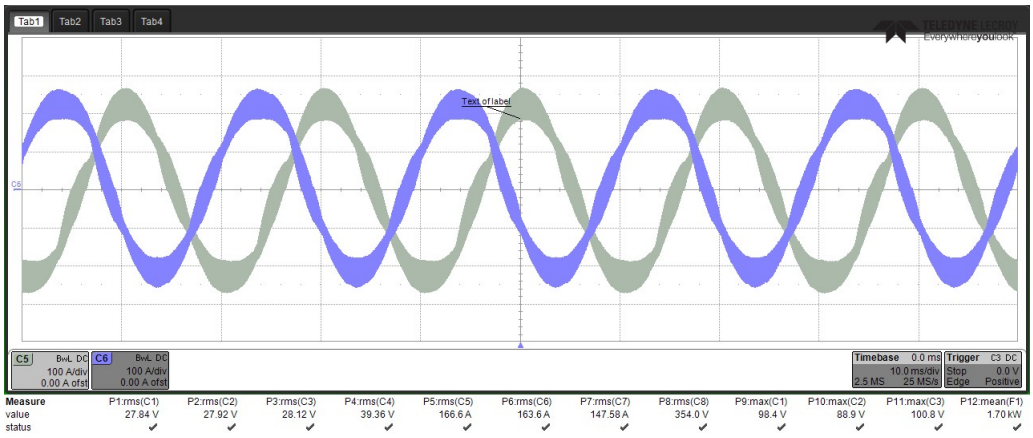

Figure 5.20: Obtained phase current waveforms for 5kW output power.

small and negligible ripples and the inverter was operating at a switching frequency of 25 KHz, with the supply voltage of around 40Vdc. The reason for performing the test at a reduced voltage of 40Vdc was to depict its actual operating scenario in the car where the battery's voltage for the continuous operating point would be somewhere around 40Vdc.
A Fast Fourier transform of the current waveform is shown in the figure 5.21 which gives us the details of all the frequency components influencing the current waveform. As can be seen in the figure, the higher frequency components are almost negligible, thus accounting for a smooth sinusoidal current waveform. The table 5.3 shows the measurement data and the output results. For the supply of 40Vdc, the active power is 5.6kW at a continuous operation of 10 minutes without any external forced cooling.

Table 5.3: Measurement data and the output results for 5kW output power test.

Udc [V]	**Idc [A]**	**Pdc [kW]**	**Uline.rms.avg [V]**	**Irms.avg [A]**	**Pac [kW]**	**Qac [kVar]**	**Sac [kVA]**	**Effic. [%]**
39.3	147.5	5.8	27.0	162.0	5.6	5.1	7.6	96.7

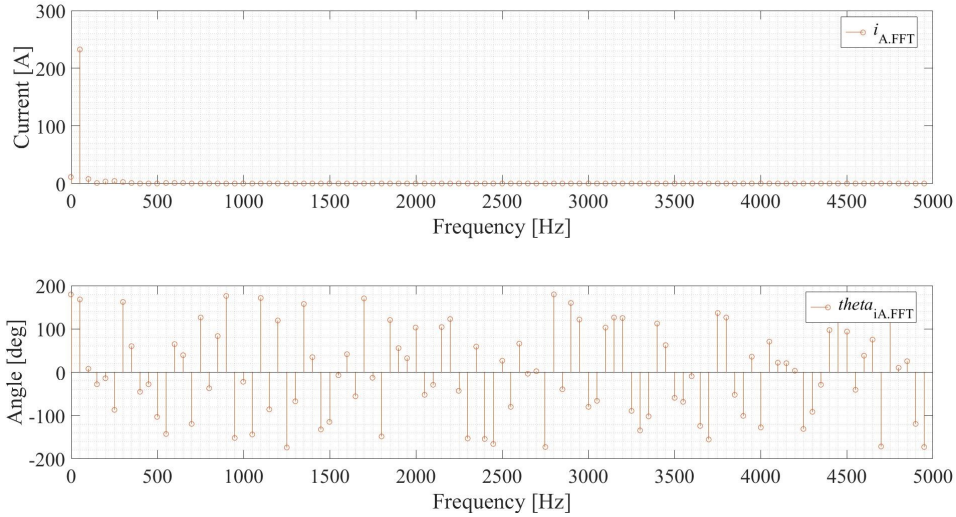

Figure 5.21: FFT of the current waveform showing influence of various frequency components for 5kW output power test.

Temperature of inverter components including the gate driver PCB, the dc link capacitor bank, the mosfet switches and the heat sink was continuously monitored during this test using an IR thermal camera. The figure 5.22 shows the temperature distribution across various components. The highest temperature of 59 deg. C in the test was of the dc-link capacitors that were across the middle capacitors of the capacitor bank assembly which stabilized at 59deg. C. Thus the inverter was concluded to be operating well for the given requirements of 5kW continuous operation.

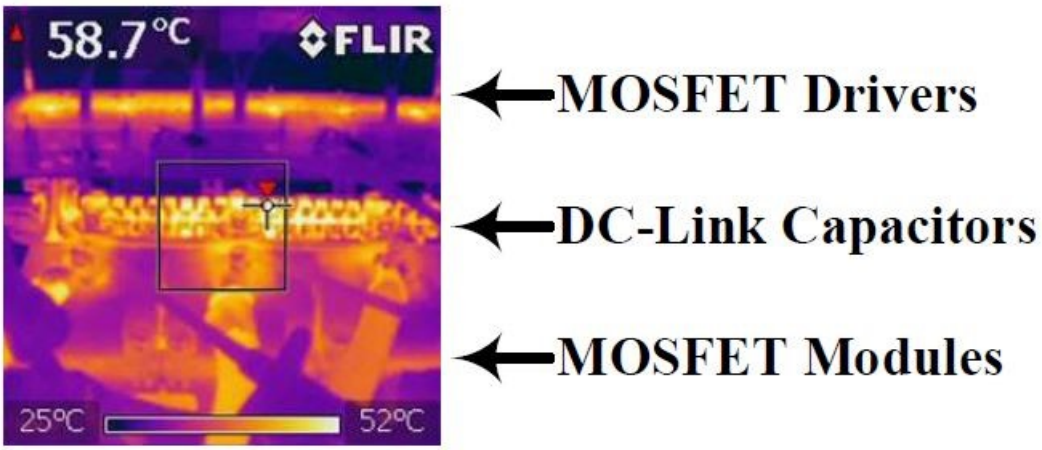

Figure 5.22: Temperature distribution of inverter components under 5kW load test

5.0.2.5 Further Testing and Evaluation

Further testing and evaluation on the inverter was done by varying the equivalent resistance of the variable resistor bank to get out higher level of output active and

Table 5.4: Results obtained from high power tests.

Test No.	Udc [V]	Idc [A]	Pdc [kW]	Uline.rms.avg [V]	Irms.avg [A]	Pac [kW]	Qac [kVar]	Sac [kVA]	Effic. [%]
1	55	200	11.0	37.7	209.9	10.3	9.0	13.7	93.9
2	30	390	11.7	19.5	419	9.5	10.4	14.1	91.6

reactive power. The schematic of the measurement set-up for Test 1 is shown in the figure 5.23. The dc supply is set at 48V and is represented by the 48V block, the inverter is switched with a switching frequency of 25 KHz with the duty cycle of 0.9 at an AC fundamental of 50 Hz. The transformer is a 3 phase load which is Y-connected at the inverter output and Δ -connected on the secondary side feeding a variable resistor bank. The transformer steps up the voltage by a factor of 10 from the primary to the secondary. The equivalent value of the resistor bank is varied by adjusting the switches on the resistor bank to a certain number marked on the resistor bank. These tests were performed to investigate the maximum output power

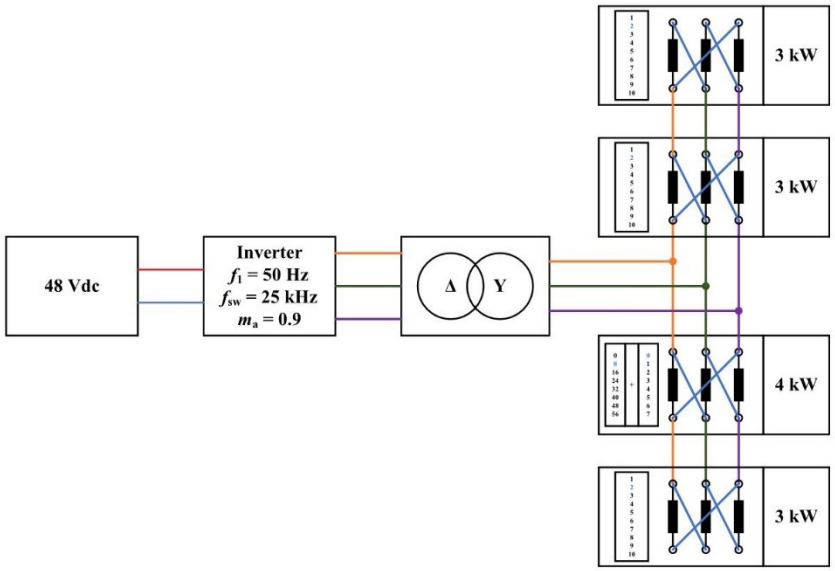

Figure 5.23: High power test - 1.

delivered by the inverter. The target was to achieve 10kW for an approximate period of 10 seconds. It was done by regulating the voltage and current. In the first test higher dc voltage (55Vdc) and lower current was applied and in the second lower dc voltage and higher current was applied. The table 5.4 shows the measured data obtained from during the tests.
The figure 5.24 and 5.25 shows the phase voltage and phase current of the test 1 and test 2 respectively.

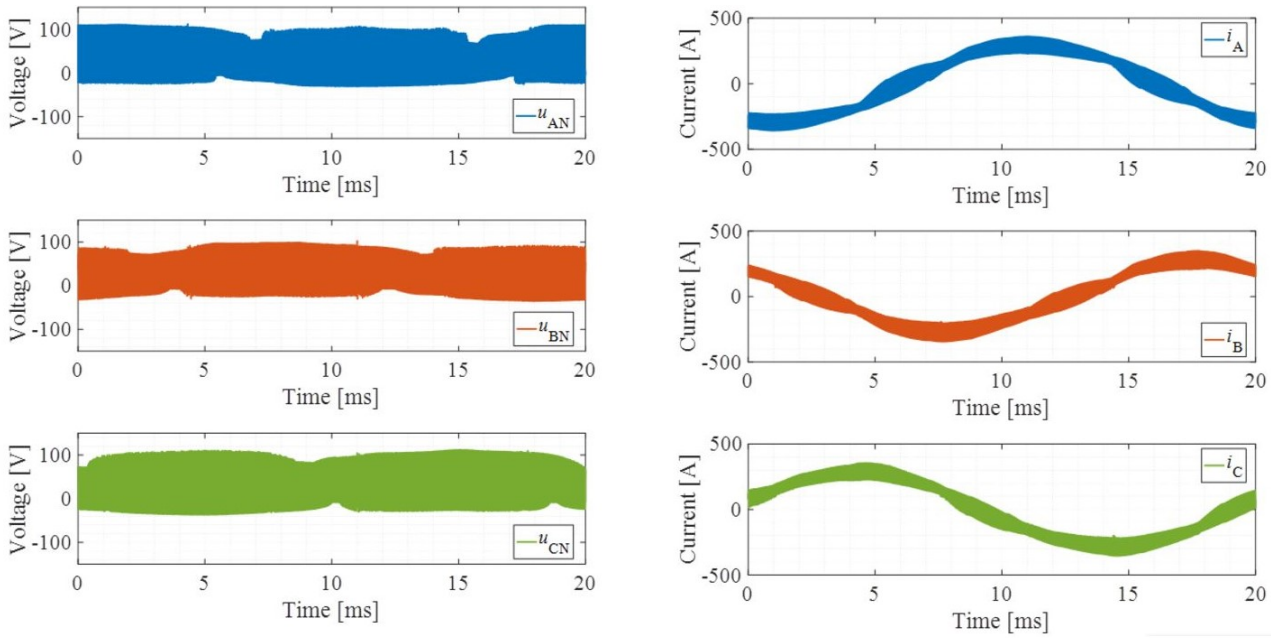

Figure 5.24: High power test - 2.

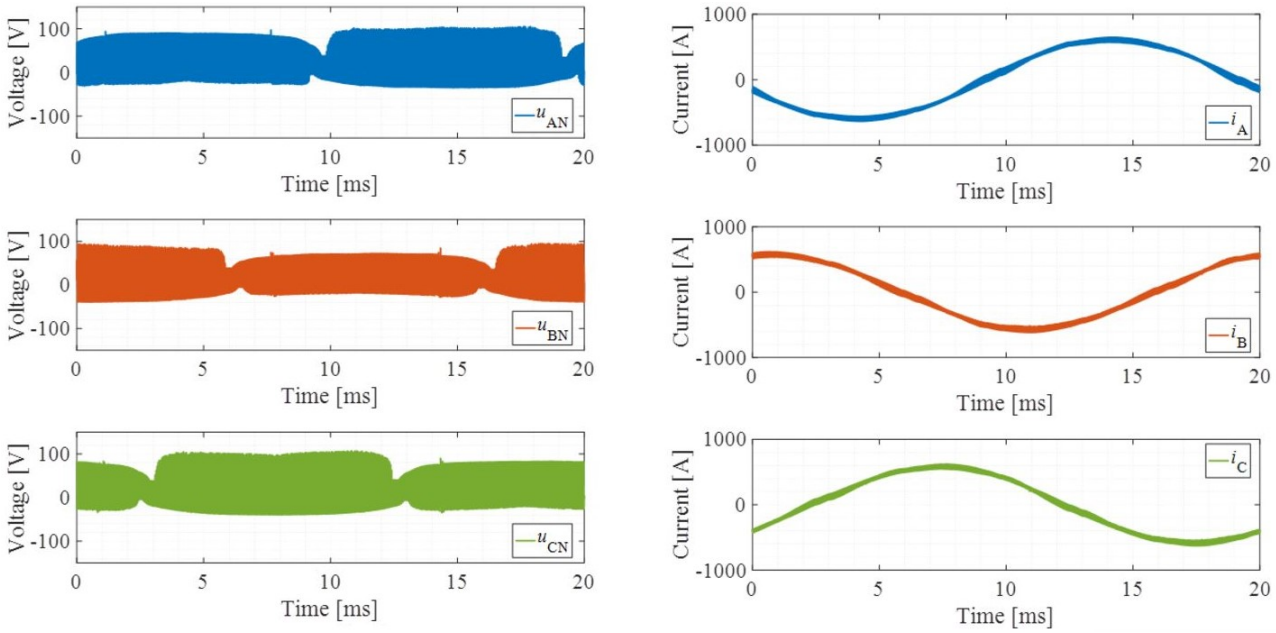

Figure 5.25: High power test

The phase voltage spikes were observed to be larger in the Test 2 (5.25). Although the capacitance along the DC-link $C_{dc.A}$, $C_{dc.B}$ and $C_{dc.C}$ can produce a stiff dc voltage, but the voltage ripple in the output phase voltage are the effect of the large common source inductance inside the module itself and the inductance caused by the tabs that are used for external connection for the dc positive, dc negative and the output (drain, source and output tab respectively) of the mosfet module. On tearing down of one the mosfet module it was observed that the module comprised of 6 mosfets in parallel on both upper and lower leg respectively connected by direct

bonded copper (DBC) technique and the inductance caused by Mosfet tabs i.e. the connection tabs of the module, the common source inductance and the output tab which is represented by $L_{A.\sigma.1}$ - $L_{A.\sigma.4}$, $L_{B.\sigma.1}$ - $L_{B.\sigma.4}$ and $L_{C.\sigma.1}$ - $L_{C.\sigma.4}$ respectively in the figure 5.26 inside the power module was responsible for these voltage spikes. Therefore, a lower output current would help in reducing di/dt which would in turn reduce the voltage swing on the output phase voltage. One suggestion to get a control on this issue was to either select MOSFETs with high breakdown voltage, or, to increase the gate resistance to decrease di/dt.

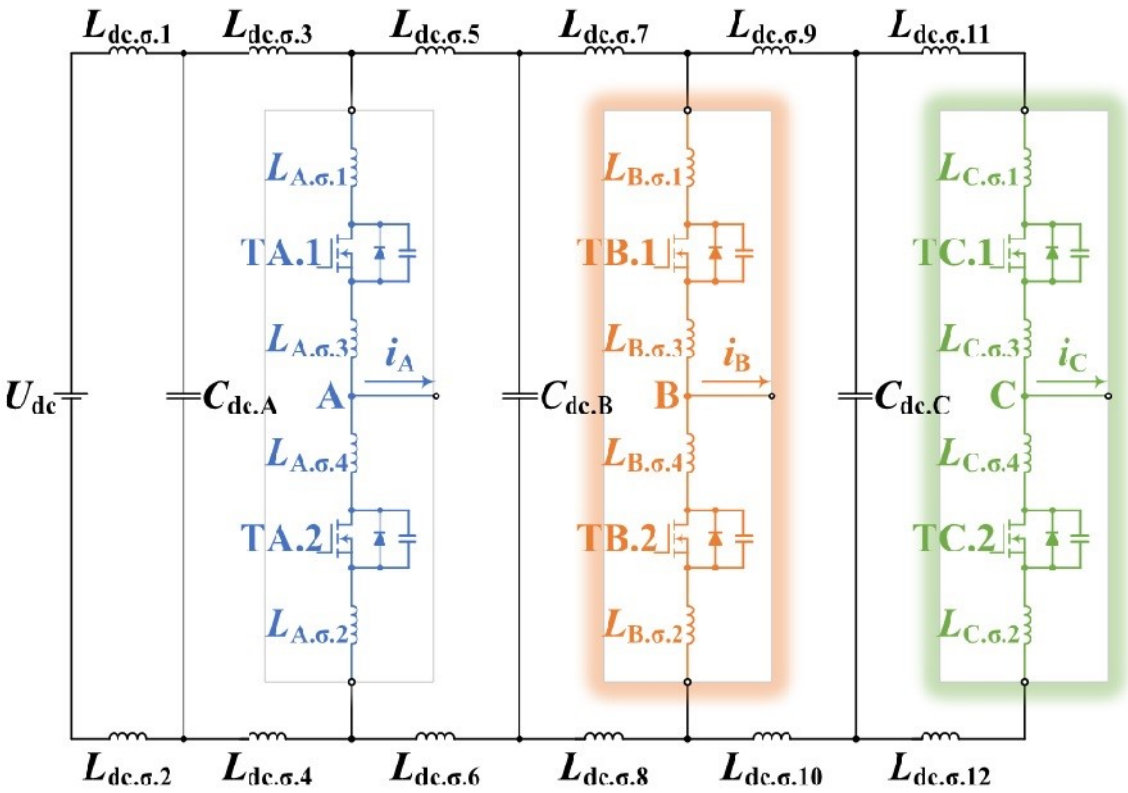

Figure 5.26: Distribution of inductance inside the Mosfet module package.

It was observed that the temperature distribution over the dc-link capacitance bank during these two tests was not uniform. The figure 5.27 shows the temperature variation along the DC-link capacitors in Test 1, where capacitors close to Phase B give the highest temperature. The explanation can be illustrated by Figure 5.28. The

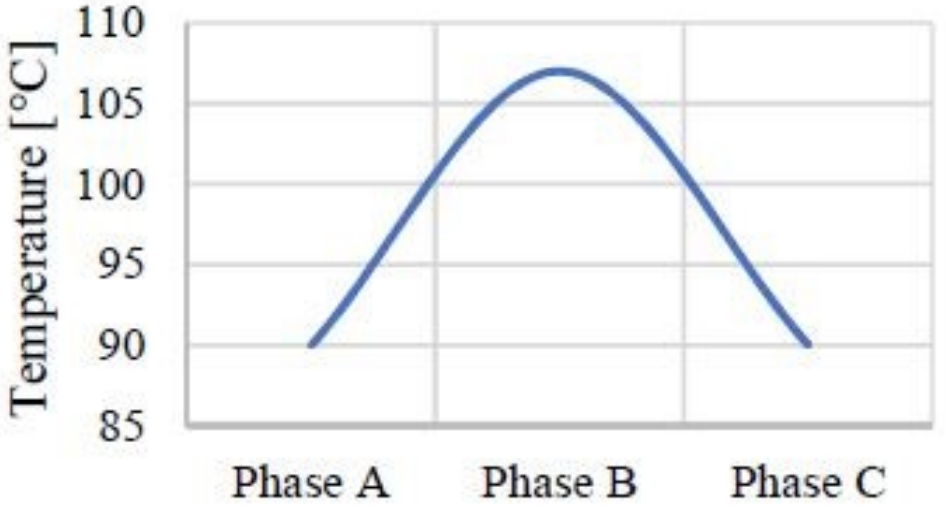

Figure 5.27: Distribution of temperature on dc-link capacitors.

commutation currents between all the three phases passes through the capacitors leg in the middle, and therefore its concentration is the highest along the capacitors that are in the middle of the capacitor bank. Almost all of the ripple current therefore passes through the capacitor in the middle and due to the ESR of the capacitor, the I2R losses across it are responsible for the generation of heat. Also, due to the layout of the PCB the heat generated by the ESR and the ripple current does not gets dissipated in a good way by the natural convection process resulting in the temperature rise of the capacitors along the middle part of the capacitor PCB.

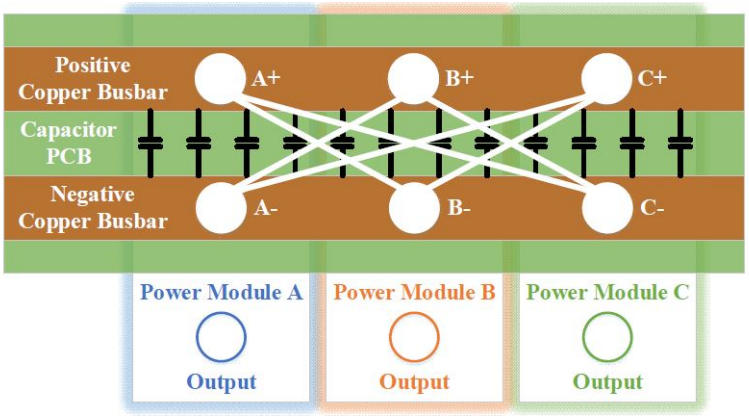

Figure 5.28: Illustration of concentration of commution current on capacitors in the middle.

This unbalanced heat dissipation along the dc link capacitors resulted in burning of some of the capacitors placed on the bottom face of the PCB and in the middle of the dc-link capacitor bank PCB as seen in figure 5.29

Figure 5.29: Burnt capacitors on PCB.

Due to the lack of adequate load that could further load the inverter to draw more output power and therefore test the maximum output power that the inverter could deliver further evaluation was not done. It was then decided to conclude that inverter could deliver up to 14kVA apparent power with adequate cooling and the further evaluation of the inverter using the static load was discontinued. Further testing of the inverter would be done with the dynamic load i.e. the WRSM for which the inverter had been designed originally for which was out of the scope for this thesis work.

6
Conclusion

This aim of this thesis was to design, manufacture and test a three phase Voltage source inverter and its gate driver circuit, intended to be used for the stator excitation of the WRSM which could deliver the output power of 20kW. Previous work done at Chalmers used the concept of parallel Mosfets which brought up the problem of stray inductance due to the inverter circuit layout. Therefore, special focus was given to minimize the effect of parasitic inductance by using Mosfet module pack thereby eliminating the need to parallel them manually. The three phase sinusoidal current waveform as shown in figure The sinusoidal output current waveform as shown in 5kW power test and various other tests illustrates that the designed gate driver circuit and the micro-controller's PWM generation works properly. The temperature of inverter components shows that the designed cooling solution as well as the load sharing of the various inverter components is good, therefore, the cooling solution works as expected . There are, however, number of improvements that can be done with the current design of the inverter's dc-link capacitor bank. The dc-link capacitors being burned brings out the design errors while estimating the ripple current. The method to theoretically estimate the ripple current underestimates the actual ripple current commuting through the dc-link capacitors which results in the overheating of the capacitors and thereby resulting in their breakdown. The size targets set in the project initially have been deviated towards the end to make the design possible. The inverter can output power levels of up to approximately 15 kVA. The inverter has also been tested successfully to achieve a continuous operation of 5kW without the need for any external forced cooling. Further evaluation of the designed inverter with WRSM will give a clearer picture on the functionality and suitability of the inverter for this application.

6.0.1 Ethics and Sustainable Development

To comply with the strict regulations on carbon emission by the legislation all over the world there has been an accelerated shift from normal combustion engine cars to the electrified cars. Mild hybrid is one such response from car manufactures to meet those targets. The effectiveness of electrifying the vehicles is still a subject to think and discuss. Whether electrification of vehicles will actually contribute towards the lower emission if they are sold as the mainframe vehicles is still an uncertainty. One way to think about this argument is if these vehicles run on electricity that itself is generated is a non-sustainable way for example by burning coal or petroleum and the number of electrified vehicles increase then these cars will put a lot of pressure on the national grid to meet the increased energy demands and we might end up in a

situation where more demand of energy might result in more carbon dioxide emission if the energy is produced using non renewable resources such as coal and petroleum. So contrary to contributing to lower emission, it will end up causing more hazardous emission. Also important to see is to the clean up the manufacturing approach of the electric vehicle. The use of such rare earth metals for examples in the permanent magnets for electric motor and Lithium in the battery manufacturing, puts a lot of pressure towards the environment due to the unsustainable extraction process of these metals from earth. On the other hand it is safe to assume that Electric cars score higher than combustion cars when it comes to noise pollution and also other hazardous pollutants such as Nitrous oxide, sulphur dioxide and lead that are otherwise emitted from the tail of combustion cars would be eliminated. Therefore electrified vehicles are really a future. But, it has to be done in a more sustainable way. Alternatives have to be thought about the battery technologies such as fuel cells, solar power and so on. Energy produced to meet the demands of electrified vehicles have to be produced using renewable resources such as wind, hydro, solar etc. Usage of permanent magnets obtained from are earth elements has to be checked or alternatives would have to be implemented. The future of electrified vehicles is still dependent on cost, since today these vehicles are a lot more expensive than normal combustion vehicles of same class. Therefore, both science and legislation has to go hand in hand to make this a success. Nevertheless, the introduction of electrified vehicles is a promising step towards a more sustainable society.

6.0.2 Future work

Although the inverter has been built, designed and tested for the basic operational functionality, there are lot of ways to keep on working with the current design to further validate and test it and also to improve the current design both mechanically and electrically. The obvious mechanical improvements can be done with the PCB layout and mounting points for the PCB which was discovered during the testing that they were not aligned with other PCB's and therefore made the PCB's difficult to be mounted. The cooling plate's size can be reduced and/or optimized with more accurate thermal model and detailed CFD simulations. Electrical design of the inverter has lot of areas for improvement. The dc-link capacitor bank needs to be redesigned due to that the dc-link capacitors get really hot even during the normal continuous operation of the inverter. The thermal behaviour of the inverter has not been tested or verified and that opens up more scope for continuation of the work. The testing has been done on the static load with the transformer as the output load. Therefore, only apparent power of the inverter has been tested. The real power output of the inverter must be tested with a dynamic load. Therefore more testing should be done with an electrical machine as the load.

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[8] *A 500Arms 48V power stage of BSG inverter with TO-Leadless MOSFET for Mild HEV*
http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=8011373

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http://ieeexplore.ieee.org/document/6243442/

[10] *48V systems: Design considerations for a typical auxiliary power inverter.*
https://e2e.ti.com/blogs_/b/behind_the_wheel/archive/2015/07/08/48v-systems-design-considerations-for-a-typical-auxiliary-power-inverter

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https://www.sbelectronics.com/wp-content/uploads/2009/11/Reliability_Considerations_Inverter_DC_Link_IMAPS_paper.pdf

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http://ieeexplore.ieee.org/document/5075431/

[15] *Comparison of converter topologies for battery-powered high-speed drives considering different cooling conditions and semiconductor materials for ultra lightweight hybrid systems.*
http://ieeexplore.ieee.org/document/6631792/

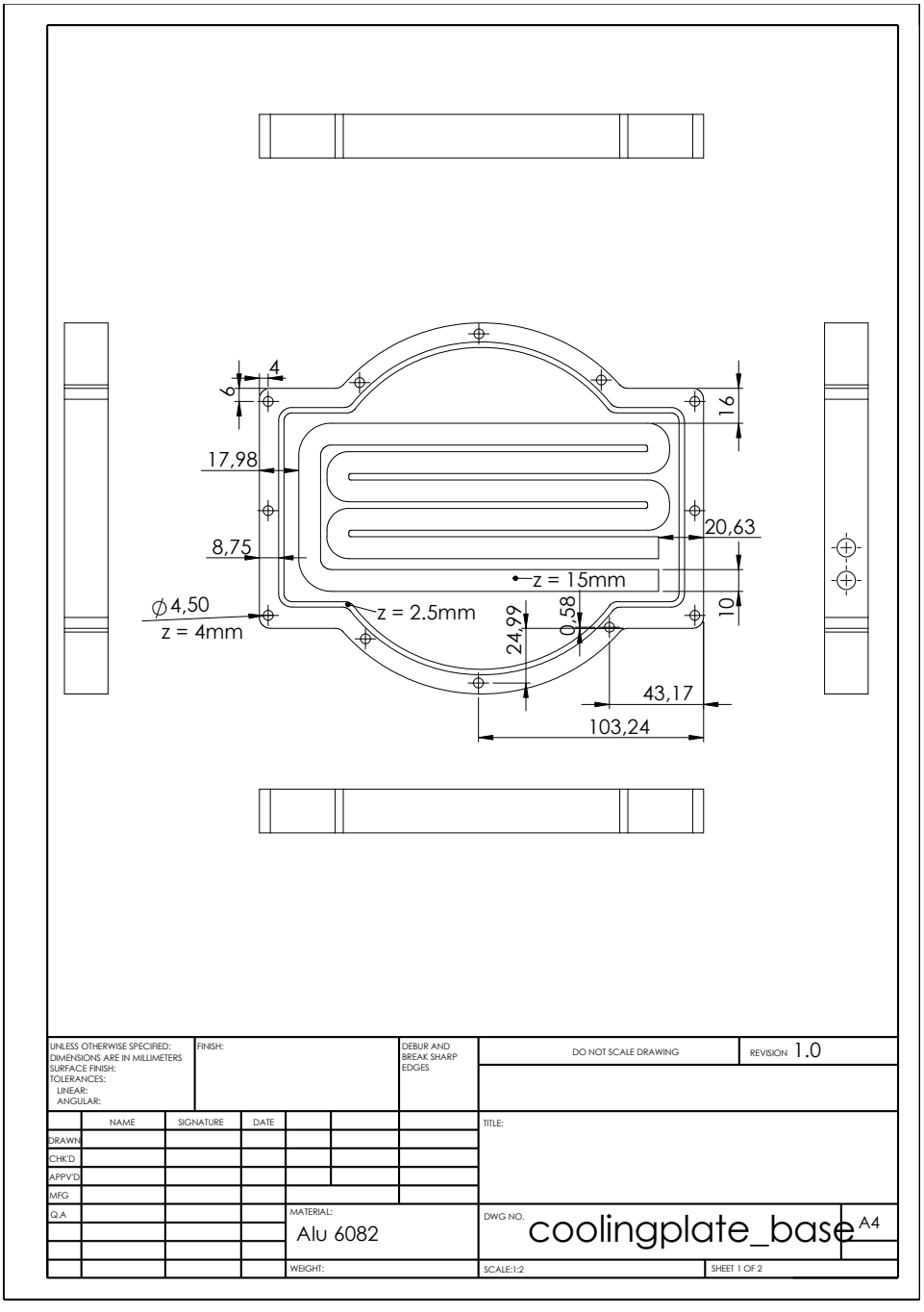
[16] *Gate Driver IC - 1EDI EiceDRIVER™ Compact*
https://www.infineon.com/dgdl/Infineon-1EDI60N12AF-DS-v02_00-EN.pdf?fileId=db3a3043427ac3e201428e5da08f372a

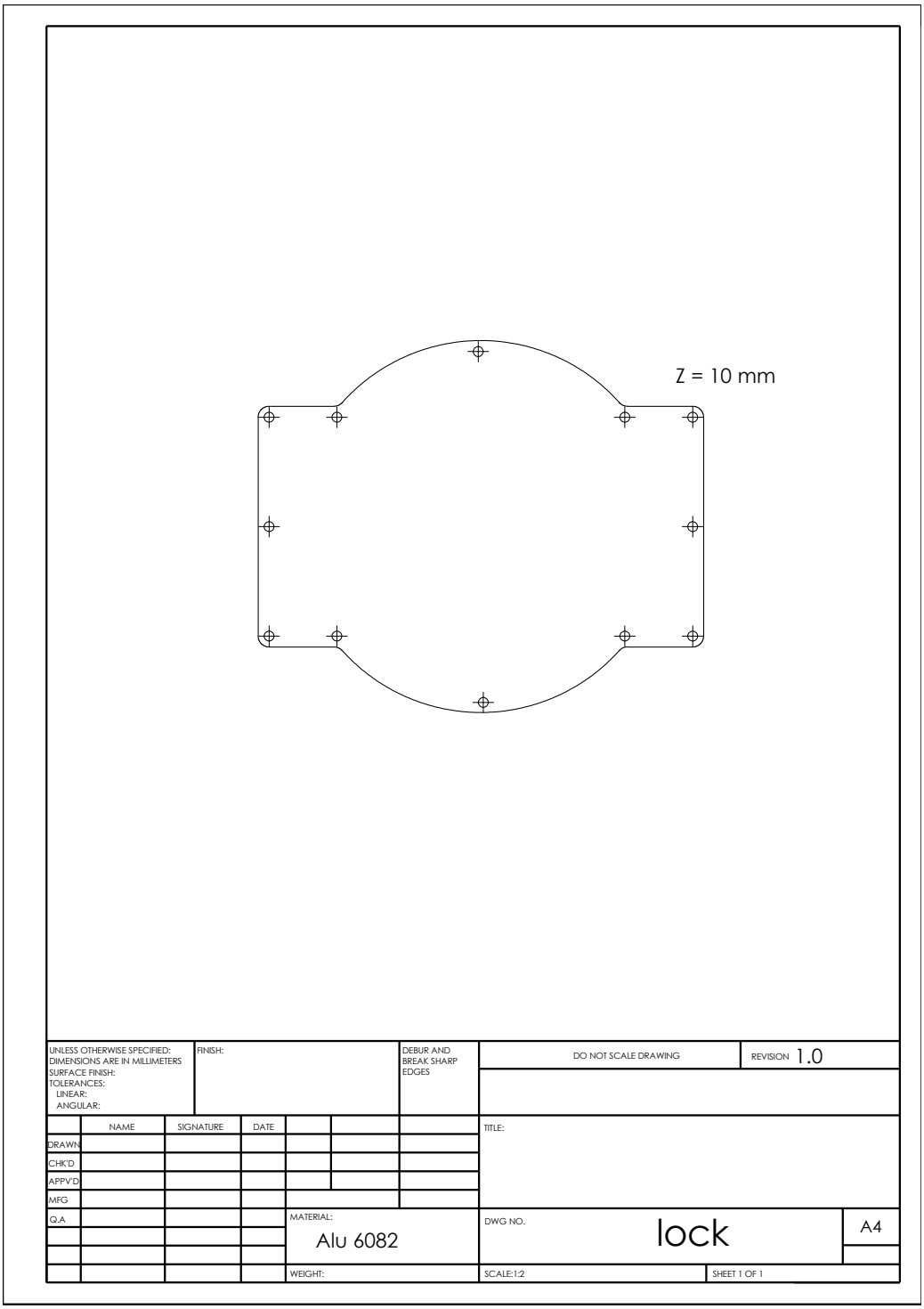
[17] *STARPOWER SEMICONDUCTOR MOSFET MD1026HFM150C2S Molding Type Module 150V/1026A 2 in one-package*
http://www.starpowereurope.com/media/296973/-MD1026HFM150C2Spdf.pdf

[18] *TDK corporation. Oct. 2014.*
https://product.tdk.com/en/search/capacitor/ceramic/mlcc/info?part_no=CKG57NX7S2A226M500JH

A

Appendix 1 - Cooling Plate Drawing




Z = 10 mm
UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
SURFACE FINISH:
TOLERANCES:
LINEAR:
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BREAK SHARP
EDGES
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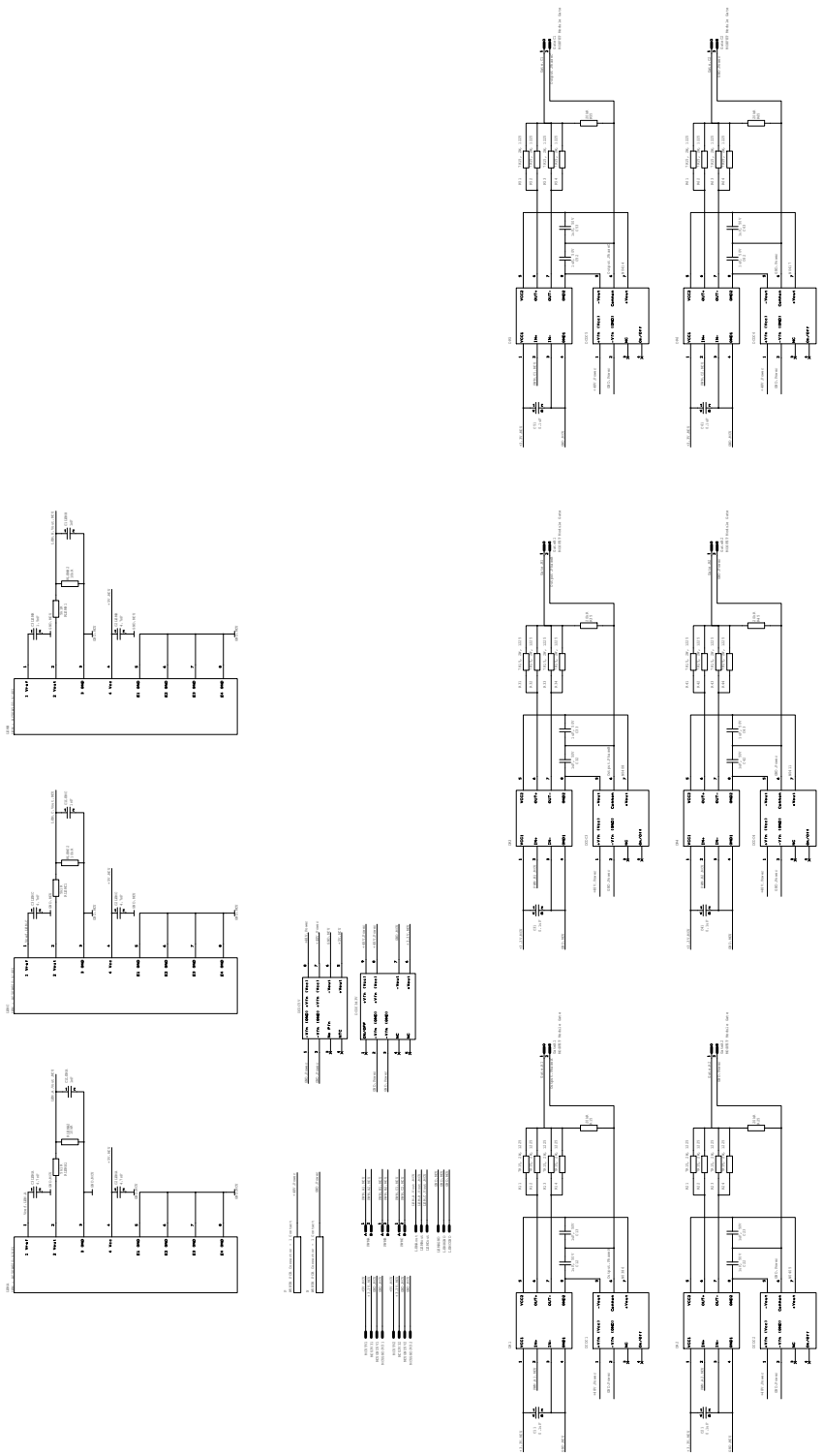
CHK'D
APPV'D
MFG
Q.A
TITLE:
MATERIAL:
Alu 6082
DWG NO.
lock
A4
WEIGHT:
SCALE:1:2
SHEET 1 OF 1

B

Appendix 2 - Gate PCB Schematic



C

Appendix 3 - Datasheets

Capacitor Datasheet

Characterization Sheet (Multilayer Ceramic Chip Capacitors)

CKG57NX7S2A226M500JH

TDK Item Description : CKG57NX7S2A226MT****

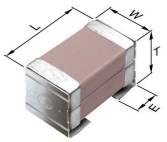
Lead Free | Halogen Free | REACH | RoHS COMPLIANT

Application & Main Feature

Commercial Grade (MEGACAP Type)

Series

CKG57N(5750) [EIA CC2220]



Dimensions

L	6.00mm +/-0.5mm
W	5.00mm +/-0.5mm
T	5.00mm +/-0.5mm
E	1.60mm +/-0.3mm

Temperature Characteristic
X7S (-55 to 125 degC +/-22%)

Rated Voltage
2A (100Vdc)

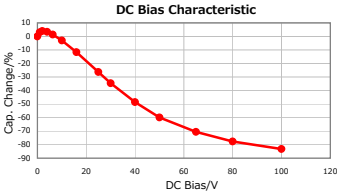
Capacitance
22uF

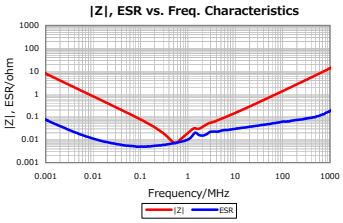
Capacitance Tolerance
M (+/-20%)

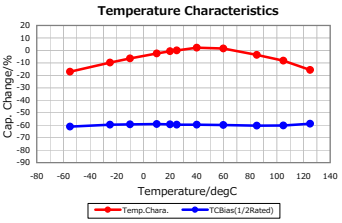
Dissipation Factor
5% Max.

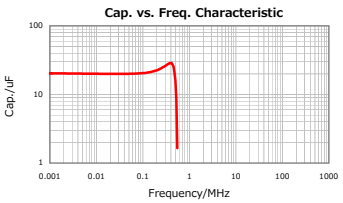
Insulation Resistance
22Mohm Min.

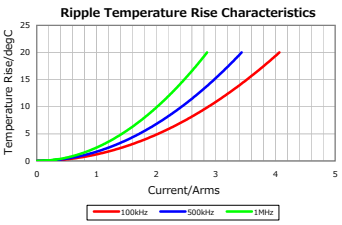
AEC-Q200
Not Applicable











TDK

All specifications are subject to change without notice.

January 4, 2016

Mosfet Module Datasheet

STARPOWER

SEMICONDUCTOR **MOSFET**

MD1026HFM150C2S

Molding Type Module

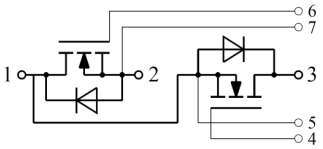
150V/1026A 2 in one-package

General Description

STARPOWER MOSFET Power Module provides very low $R_{DS(on)}$ as well as optimized intrinsic diode. It's designed for the applications such SMPS and DC drives.

Features

- Low $R_{DS(on)}$
- Optimized intrinsic reverse diode
- Low inductance case avoid oscillations
- Kelvin source terminals for easy drive
- Isolated copper baseplate using DBC technology



Equivalent Circuit Schematic

Typical Applications

- Main and auxiliary AC drives of electric vehicles
- DC servo and robot drives
- Battery vehicles
- UPS equipment
- Plasma cutting

Absolute Maximum Ratings T_C=25℃ unless otherwise noted

Symbol	Description	MD1026HFM150C2S	Units
V_{DSS}	Drain-Source Voltage	150	V
V_{GSS}	Gate-Source Voltage	±30	V
I_D	Drain Current @ T_C=25℃ @ T_C=80℃	1026 726	A
I_F	Diode Forward Current	1026	A
P_D	Maximum Power Dissipation @ T_j=175℃	2083	W
T_{jmax}	Maximum Junction Temperature	175	℃
T_{jop}	Operating Junction Temperature	-40 to +150	℃
T_{STG}	Storage Temperature Range	-40 to +125	℃
V_{ISO}	Isolation Voltage RMS,f=50Hz,t=1min	2500	V
Mounting Torque	Power Terminal Screw:M6 Mounting Screw:M6	2.5 to 5.0 3.0 to 5.0	N.m

Electrical Characteristics of MOSFET T_C=25℃ unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	T_j=25℃	150			V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=V_{DSS},V_{GS}=0V, T_j=25℃			120	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=V_{GSS},V_{DS}=0V, T_j=25℃			600	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate-Source Threshold Voltage	I_D=1.5mA,V_{DS}=V_{GS}, T_j=25℃	3.0		5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	I_D=618A,V_{GS}=10V, T_j=25℃			0.98	mΩ
g_{fs}	Forward Transconductance	V_{DS}=50V,I_D=618A	972			S

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
R_{Gint}	Internal Gate Resistance			0.62		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=98V,I_D=618A, R_G=0.17Ω,V_{GS}=±10V, T_j=25℃		28		ns
t_r	Rise Time			120		ns
$t_{d(off)}$	Turn-Off Delay Time			50		ns
t_f	Fall Time			85		ns
Q_g	Total Gate Charge	I_D=618A,V_{DS}=75V, V_{GS}=10V		906		nC
Q_{gs}	Gate-Source Charge			312		nC
Q_{gd}	Gate-Drain ("Miller") Charge			330		nC
C_{iss}	Input Capacitance	V_{GS}=0V,V_{DS}=50V, f=1.0MHz		62.8		nF
C_{oss}	Output Capacitance			5.86		nF
C_{rss}	Reverse Transfer Capacitance			1.22		nF
L_{CE}	Stray Inductance				20	nH
$R_{CC'+EE'}$	Module Lead Resistance,Terminal to Chip	T_C=25℃		0.35		mΩ

Electrical Characteristics of Inverse Diode T_C=25℃ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Diode Forward Voltage	I_F=618A,V_{GS}=0V,T_j=25℃			1.30	V
t_{rr}	Diode Reverse Recovery Time	V_R=100V,I_F=618A, di/dt=600A/μs, T_j=25℃		110		ns
Qrr	Diode Reverse Recovery Charge			3.09		μC

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case (per MOSFET)		0.072	K/W
$R_{θCS}$	Case-to-Sink (Conductive grease applied)	0.035		K/W
Weight	Weight of Module	300		g

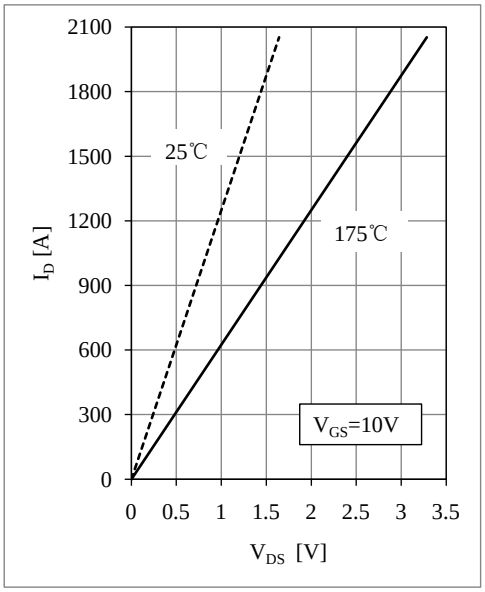


Fig 1. Mosfet Output Characteristic

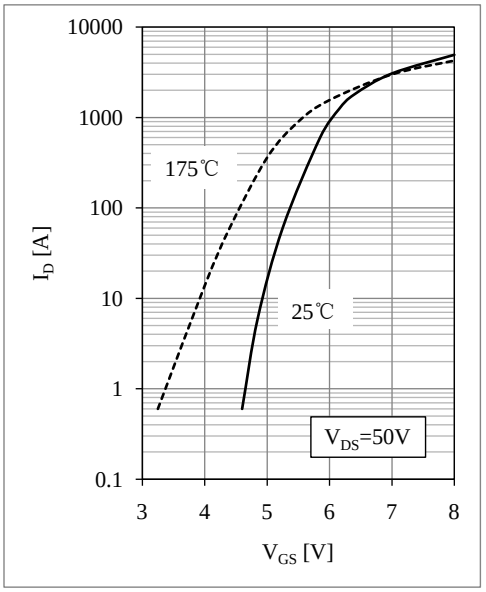


Fig 2. Mosfet Transfer Characteristic

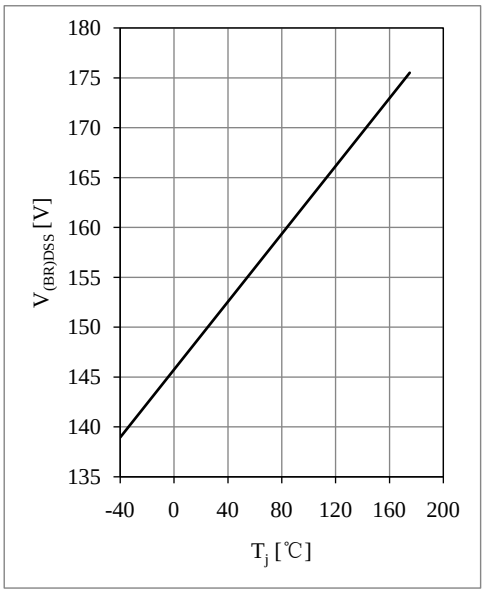


Fig 3. Brakedown Voltage vs. Temperature

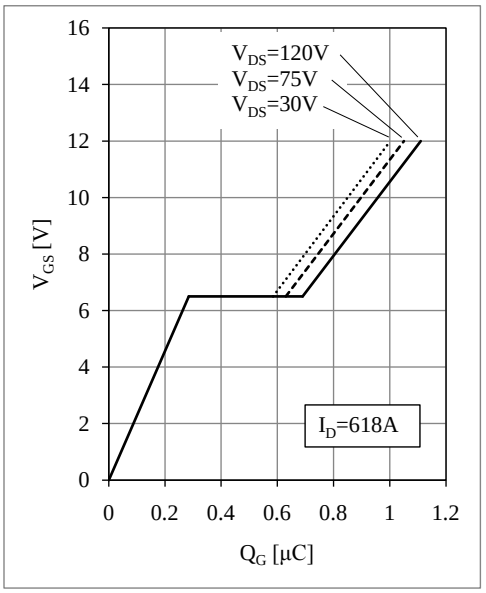


Fig 4. Gate Charge Characteristic

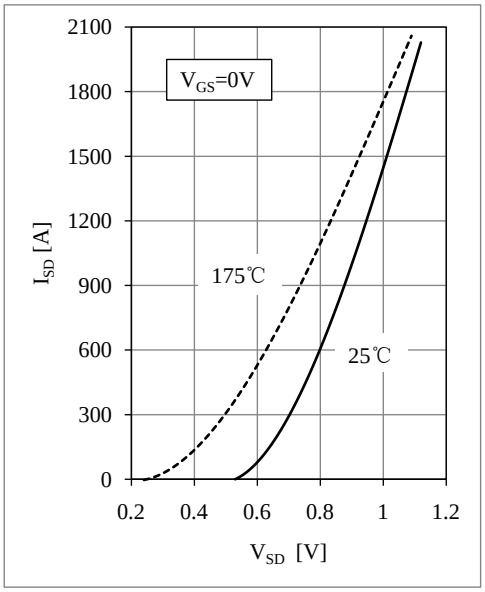


Fig 5. Inverse Diode Output Characteristic

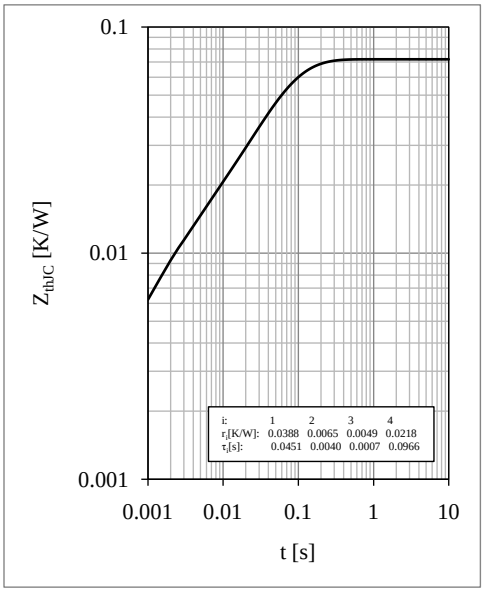
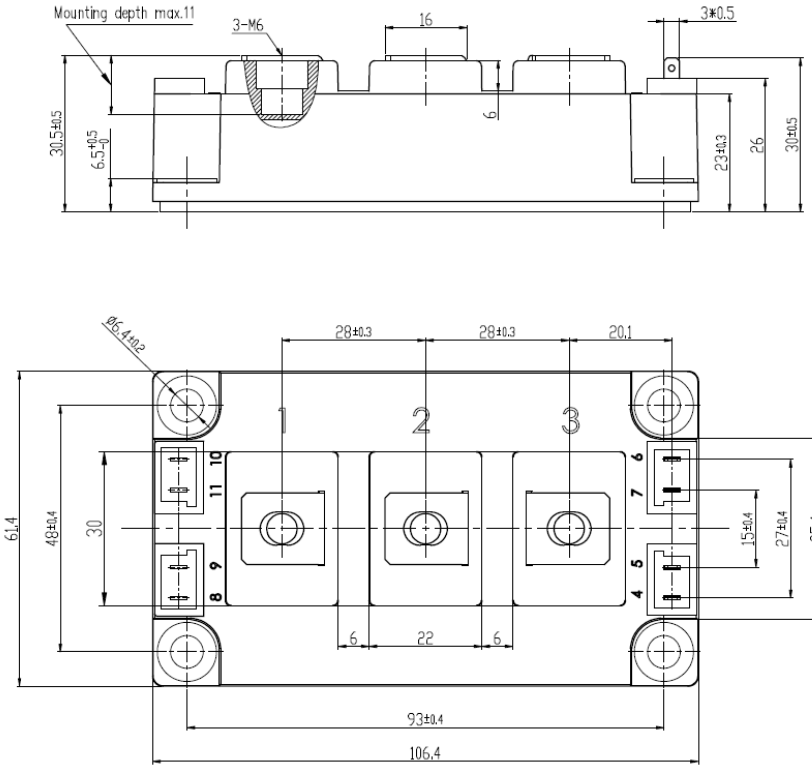


Fig 6. Transient Thermal Impedance

Package Dimensions

Dimensions in Millimeters



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The data contained in this product datasheet is exclusively intended for technically trained staff. you and your technical departments will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to such application.

This product data sheet is describing the characteristics of this product for which a warranty is granted. Any such warranty is granted exclusively pursuant the terms and conditions of the supply agreement. There will be no guarantee of any kind for the product and its characteristics.

Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of our product, please contact the sales office, which is responsible for you (see www.powersemi.cc), For those that are specifically interested we may provide application notes.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact the sales office, which is responsible for you.

Should you intend to use the Product in aviation applications, in health or live endangering or life support applications, please notify.

If and to the extent necessary, please forward equivalent notices to your customers.
Changes of this product data sheet are reserved.

Gate driver IC datasheet

1EDI EiceDRIVER™ Compact
Single Channel MOSFET Gate Driver IC

Separate output variant for MOSFET

1 Overview

Main Features

- Single channel isolated MOSFET Driver
- Input to output isolation voltage up to 1200 V
- For high voltage power MOSFETs
- Up to 10 A typical peak current at rail-to-rail outputs
- Separate source and sink outputs

Product Highlights

- Galvanically isolated Coreless Transformer Driver
- Wide input voltage operating range
- Low input to output capacitive coupling
- Suitable for operation at high ambient temperature

Typical Application

- AC and Brushless DC Motor Drives
- High Voltage PFC, DC/DC-Converter and DC/AC-Inverter
- Induction Heating Resonant Application
- UPS-Systems
- Welding
- Solar MPPT boost converter

Description

The 1EDI60N12AF is a galvanically isolated single channel MOSFET driver in a PG-DSO-8-51 package that provides output currents of at least 6 A at separated output pins.

The input logic pins operate on a wide input voltage range from 3 V to 15 V using CMOS threshold levels to support even 3.3 V microcontroller.

Data transfer across the isolation barrier is realized by the Coreless Transformer Technology.

Every driver family member comes with logic input and driver output under voltage lockout (UVLO) and active shutdown.

Product Name	Gate Drive Current (min)	Package
1EDI60N12AF	±6.0 A MOSFET level optimized	PG-DSO-8-51

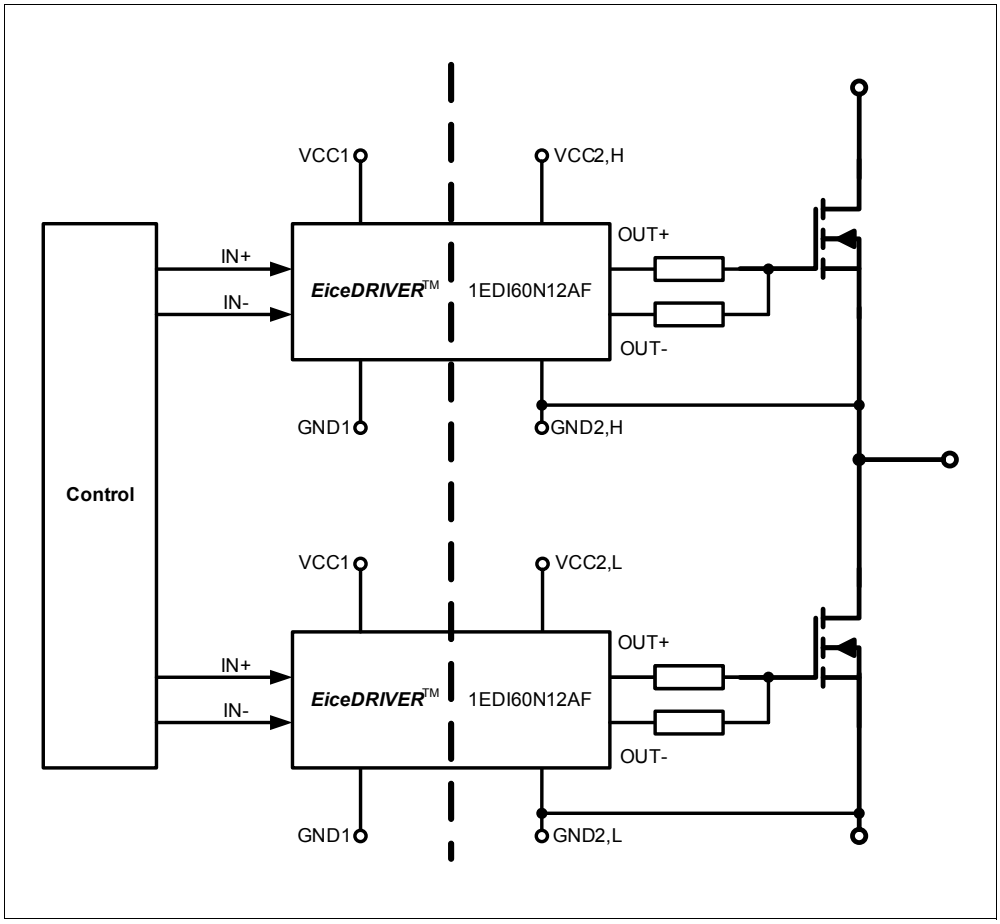


Figure 1 Typical Application

2 Block Diagram

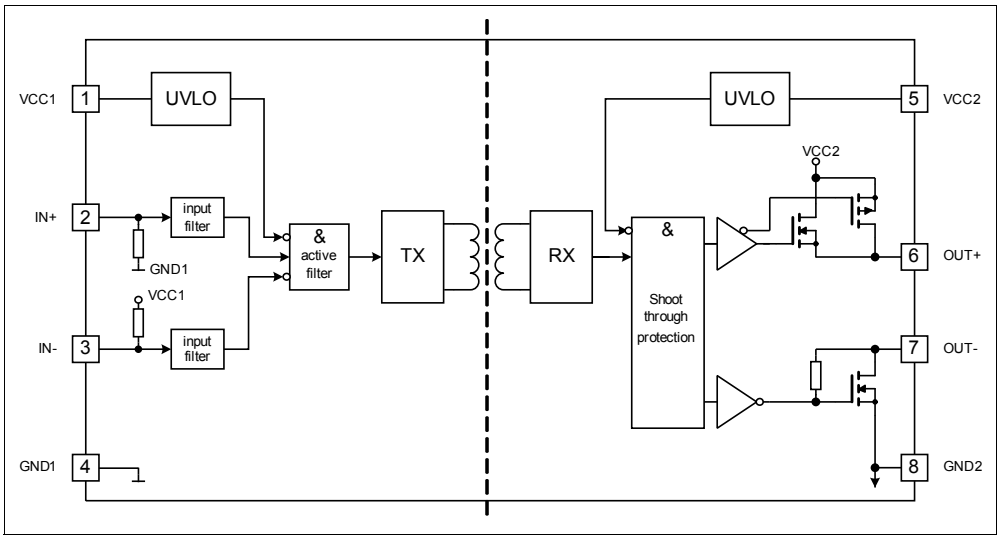


Figure 2 Block Diagram 1EDI60N12AF

3 Pin Configuration and Functionality

3.1 Pin Configuration

Table 1 Pin Configuration

Pin No.	Name	Function
1	VCC1	Positive Logic Supply
2	IN+	Non-Inverted Driver Input (active high)
3	IN-	Inverted Driver Input (active low)
4	GND1	Logic Ground
5	VCC2	Positive Power Supply Output Side
6	OUT+	Driver Source Output
7	OUT-	Driver Sink Output
8	GND2	Power Ground

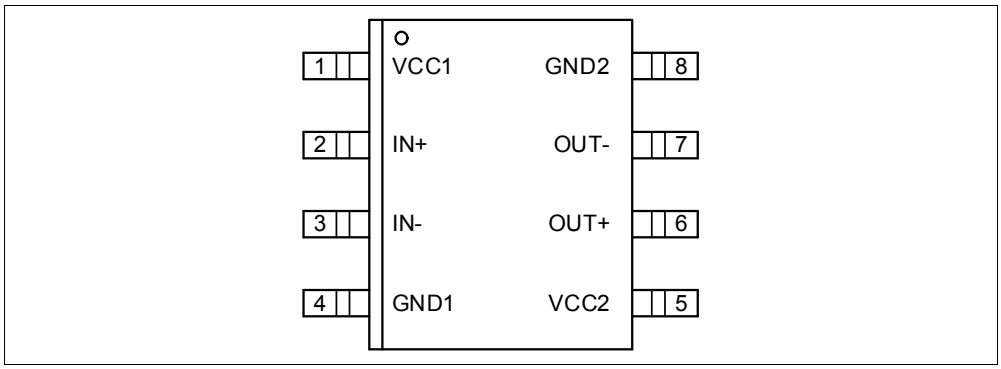


Figure 3 PG-DSO-8-51 (top view)

3.2 Pin Functionality

VCC1

Logic input supply voltage of 3.3 V up to 15 V wide operating range.

IN+ Non Inverting Driver Input

IN+ non-inverted control signal for driver output if IN- is set to low. (Output sourcing active at IN+ = high and IN- = low)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at IN+. An internal weak pull-down-resistor favors off-state.

IN- Inverting Driver Input

IN- inverted control signal for driver output if IN+ is set to high. (Output sourcing active at IN- = low and IN+ = high)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at IN-. An internal weak pull-up-resistor favors off-state.

GND1

Ground connection of input circuit.

VCC2

Positive power supply pin of output driving circuit. A proper blocking capacitor has to be placed close to this supply pin.

OUT+ Driver Source Output

Driver source output pin to turn on external MOSFET. During on-state the driving output is switched to VCC2. Switching of this output is controlled by IN+ and IN-. This output will also be turned off at an UVLO event.

During turn off the OUT+ terminal is able to sink approx. 100 mA.

OUT- Driver Sink Output)

Driver sink output pin to turn off external MOSFET. During off-state the driving output is switched to GND2. Switching of this output is controlled by IN+ and IN-. In case of UVLO an active shut down keeps the output voltage at a low level.

GND2 Reference Ground

Reference ground of the output driving circuit.

In case of a bipolar supply (positive and negative voltage in reference to the MOSFET source) this pin is connected to the negative supply voltage.

4 Functional Description

4.1 Introduction

The 1EDI EiceDRIVER™ Compact is a general purpose MOSFET gate driver. Basic control and protection features support fast and easy design of highly reliable systems.

The integrated galvanic isolation between control input logic and driving output stage grants additional safety. Its wide input voltage supply range support the direct connection of various signal sources like DSPs and microcontrollers.

The separated rail-to-rail driver outputs simplify gate resistor selection, save an external high current bypass diode and enhance dV/dt control.

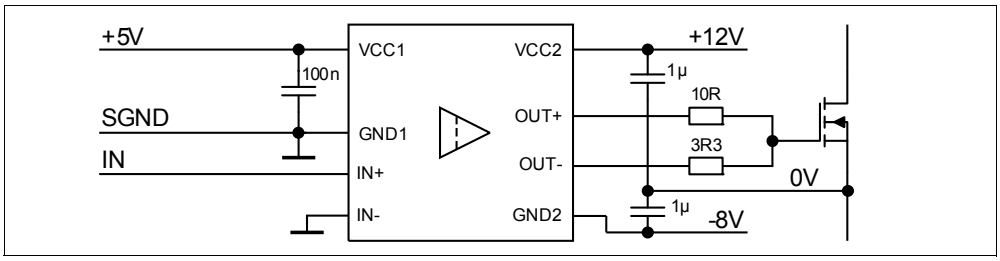


Figure 4 Application Example Bipolar Supply

4.2 Supply

The driver can operate over a wide supply voltage range, either unipolar or bipolar.

With bipolar supply the driver is typically operated with a positive voltage of 12 V at VCC2 and a negative voltage of -8V at GND2 relative to the source of the MOSFET as seen in **Figure 4**. Negative supply can help to prevent a dynamic turn on of the MOSFET.

For unipolar supply configuration the driver is typically supplied with a positive voltage of 12 V at VCC2. In this case, careful evaluation for turn off gate resistor selection is recommended to avoid dynamic turn on (see **Figure 5**).

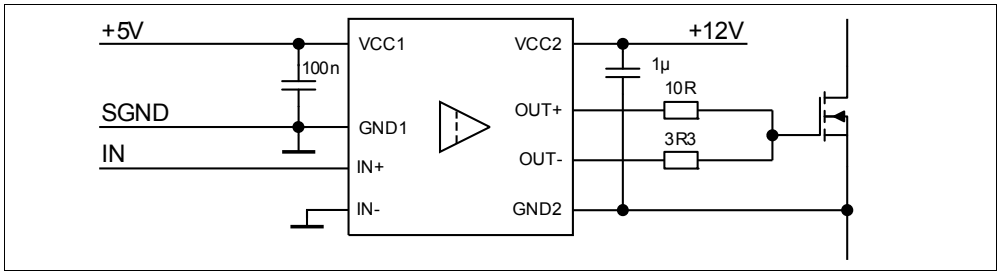


Figure 5 Application Example Unipolar Supply

4.3 Protection Features

4.3.1 Undervoltage Lockout (UVLO)

To ensure correct switching of MOSFETs the device is equipped with an undervoltage lockout for input and output independently. Operation starts only after both VCC levels have increased beyond the respective V_{UVLOH} levels (see also **Figure 8**).

If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The MOSFET is switched off and the signals at IN+ and IN- are ignored until V_{VCC1} reaches the power-up voltage V_{UVLOH1} again.

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the MOSFET is switched off and signals from the input chip are ignored until V_{VCC2} reaches the power-up voltage V_{UVLOH2} again.

Note: V_{VCC2} is always referred to GND2 and does not differentiate between unipolar or bipolar supply.

4.3.2 Active Shut-Down

The Active Shut-Down feature ensures a safe MOSFET off-state if the output chip is not connected to the power supply, MOSFET gate is clamped at OUT- to GND2.

4.3.3 Short Circuit Clamping

During short circuit the MOSFET's gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUT+ limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through this path for 10 µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

4.4 Non-Inverting and Inverting Inputs

There are two possible input modes to control the MOSFET. At non-inverting mode IN+ controls the driver output while IN- is set to low. At inverting mode IN- controls the driver output while IN+ is set to high, please see **Figure 7**. A minimum input pulse width is defined to filter occasional glitches.

4.5 Driver Outputs

The output driver section uses MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the driver's supply is stable. Due to the low internal voltage drop, switching behaviour of the MOSFET is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

5 Electrical Parameters

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	-0.3	40	V	1)
Gate driver output	V_{OUT}	V_{GND2}-0.3	V_{VCC2}+0.3	V	–
Positive power supply input side	V_{VCC1}	-0.3	18.0	V	–
Logic input voltages (IN+,IN-)	$V_{LogicIN}$	-0.3	18.0	V	–
Input to output isolation voltage (GND2)	V_{ISO}	-1200	1200	V	
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_S	-55	150	°C	–
Power dissipation (Input side)	$P_{D, IN}$	–	25	mW	2) @T_A = 25°C
Power dissipation (Output side)	$P_{D, OUT}$	–	400	mW	2) @T_A = 25°C
Thermal resistance (Input side)	$R_{THJA,IN}$	–	145	K/W	2) @T_A = 85°C
Thermal resistance (Output side)	$R_{THJA,OUT}$	–	165	K/W	2) @T_A = 85°C
ESD capability	$V_{ESD,HBM}$	–	2	kV	Human Body Model[3]

1) With respect to GND2.

2) See **Figure 10** for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

3) According to EIA/JESD22-A114-C (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

5.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.

Table 3 Operating Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	10	35	V	1)
Power supply input side	V_{VCC1}	3.1	17	V	–
Logic input voltages (IN+,IN-)	$V_{LogicIN}$	-0.3	17	V	–
Switching frequency	f_{sw}	–	4.0	MHz	2) 3)
Ambient temperature	T_A	-40	125	°C	–
Thermal coefficient, junction-top	$\Psi_{th,jt}$	–	4.8	K/W	3) @T_A = 85°C
Common mode transient immunity (CMTI)	$\lvert dV_{ISO}/dt \rvert$	–	100	kV/µs	3) @ 1000 V

1) With respect to GND2.
2) do not exceed max. power dissipation
3) Parameter is not subject to production test - verified by design/characterization

5.3 Electrical Characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 3, GND2 for pins 5 to 7).

5.3.1 Voltage Supply

Table 4 Voltage Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO threshold input chip	V_{UVLOH1}	–	2.85	3.1	V	–
	V_{UVLOL1}	2.55	2.75	–	V	–
UVLO hysteresis input chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	90	100	–	mV	–
UVLO threshold output chip (MOSFET Supply)	V_{UVLOH2}	–	9.1	10.0	V	–
	V_{UVLOL2}	8.0	8.5	–	V	–
UVLO hysteresis output chip (V_{UVLOH2} - V_{UVLOL2})	V_{HYS2}	550	600	–	mV	–

Table 4 Voltage Supply (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Quiescent current input chip	I_{Q1}	–	0.65	1.0	mA	V_{VCC1} = 5 V IN+ = High, IN- = Low =>OUT = High
Quiescent current output chip	I_{Q2}	–	1.2	2.0	mA	V_{VCC2} = 15 V IN+ = High, IN- = Low =>OUT = High

5.3.2 Logic Input

Note: Unless stated otherwise VCC1 = 5.0V

Table 5 Logic Input

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
IN+,IN- low input voltage	V_{IN+L},V_{IN-L}	–	–	30	%	of VCC1
IN+,IN- high input voltage	V_{IN+H},V_{IN-H}	70	–	–	%	of VCC1
IN+,IN- low input voltage	V_{IN+L},V_{IN-L}	–	–	1.5	V	–
IN+,IN- high input voltage	V_{IN+H},V_{IN-H}	3.5	–	–	V	–
IN- input current	I_{IN-}	–	70	200	µA	V_{IN-} = GND1
IN+ input current	I_{IN+},	–	70	200	µA	V_{IN+} = VCC1

5.3.3 Gate Driver

Table 6 Gate Driver

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High level output peak current 1EDI60N12AF	$I_{OUT+,PEAK}$	 6.0	– 10.0	–	A	1) IN+ = High, IN- = Low, V_{VCC2} = 15 V
Low level output peak current 1EDI60N12AF	$I_{OUT-,PEAK}$	 6.0	– 9.4	–	A	1) IN+ = Low, IN- = Low, V_{VCC2} = 15 V

1) voltage across the device $V_{(VCC2 - OUT+)}$ or $V_{(OUT- - GND2)} < V_{VCC2}$.

5.3.4 Short Circuit Clamping

Table 7 Short Circuit Clamping

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage (OUT+) (V_{OUT} - V_{VCC2})	V_{CLPout}	–	0.9	1.3	V	IN+ = High, IN- = Low, OUT = High I_{OUT} = 500 mA pulse test, t_{CLPmax} = 10 µs)

5.3.5 Dynamic Characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V and V_{VCC2} = 15 V.

Table 8 Dynamic Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input IN to output propagation delay ON	T_{PDON}	95	120	142	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50% @ 25°C
Input IN to output propagation delay OFF	T_{PDOFF}	105	125	150	ns	
Input IN to output propagation delay distortion (T_{PDOFF} - T_{PDON})	T_{PDISTO}	-15	5	25	ns	
Input pulse suppression IN+, IN-	T_{MININ+}, T_{MININ-}	30	40	–	ns	–
IN input to output propagation delay ON variation due to temp	T_{PDONt}	–	–	10	ns	1) C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
IN input to output propagation delay OFF variation due to temp	T_{PDOFFt}	–	–	10	ns	1) C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
IN input to output propagation delay distortion variation due to temp (T_{PDOFF}-T_{PDON})	$T_{PDISTOt}$	–	–	4	ns	1) C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
Rise time	T_{RISE}	5	10	20	ns	C_{LOAD} = 1 nF V_L 20%, V_H 80%
Fall time	T_{FALL}	4	9	19	ns	C_{LOAD} = 1 nF V_L 20%, V_H 80%

1) The parameter is not subject to production test - verified by design/characterization

5.3.6 Active Shut Down

Table 9 Active Shut Down

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD} [1)]	–	2.2	2.5	V	$I_{OUT-}/I_{OUT-,PEAK}$=0.1, V_{CC2} open

1) Referred to GND2

6 Timing Diagramms

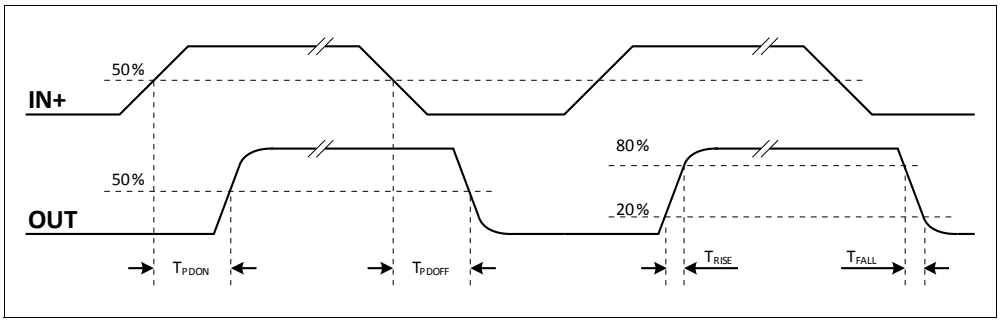


Figure 6 Propagation Delay, Rise and Fall Time

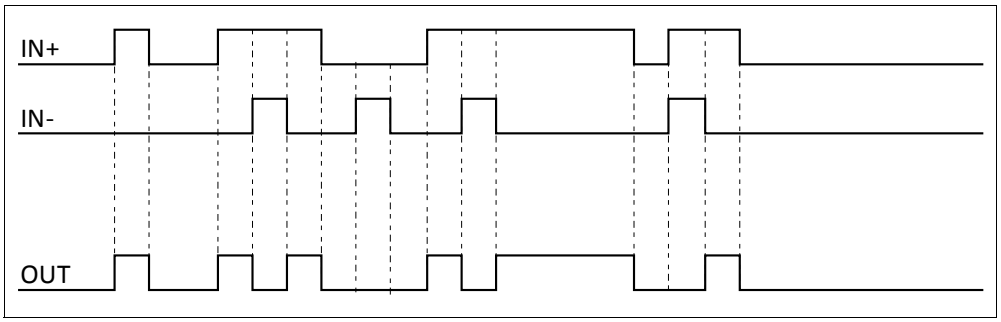


Figure 7 Typical Switching Behavior

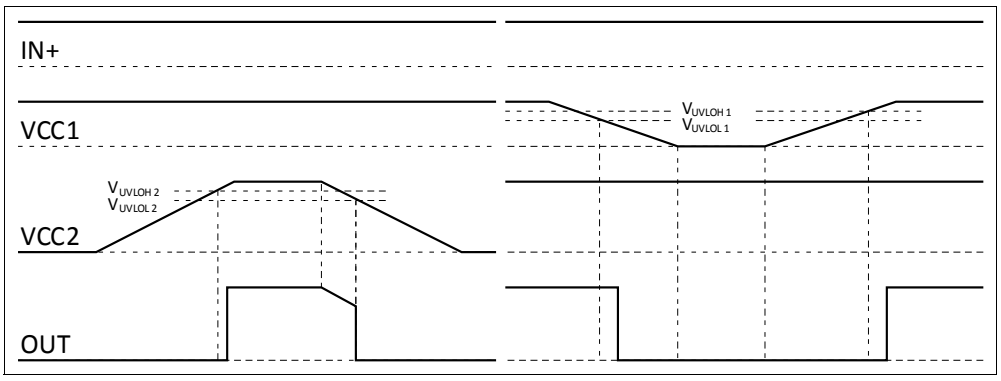
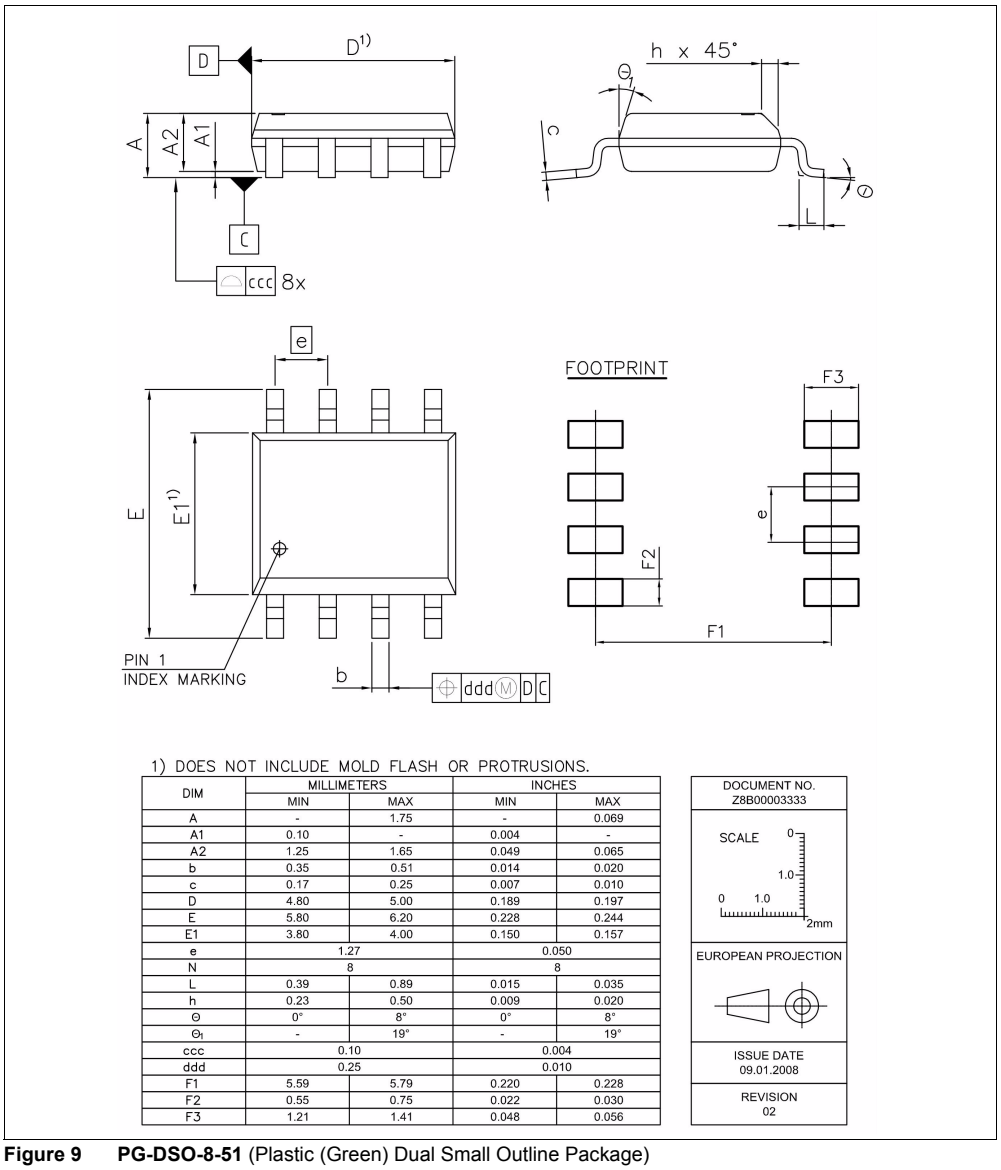


Figure 8 UVLO Behavior

7 Package Outlines



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ_1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

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SCALE 0 1.0 0 1.0 2mm

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Figure 9 **PG-DSO-8-51** (Plastic (Green) Dual Small Outline Package)