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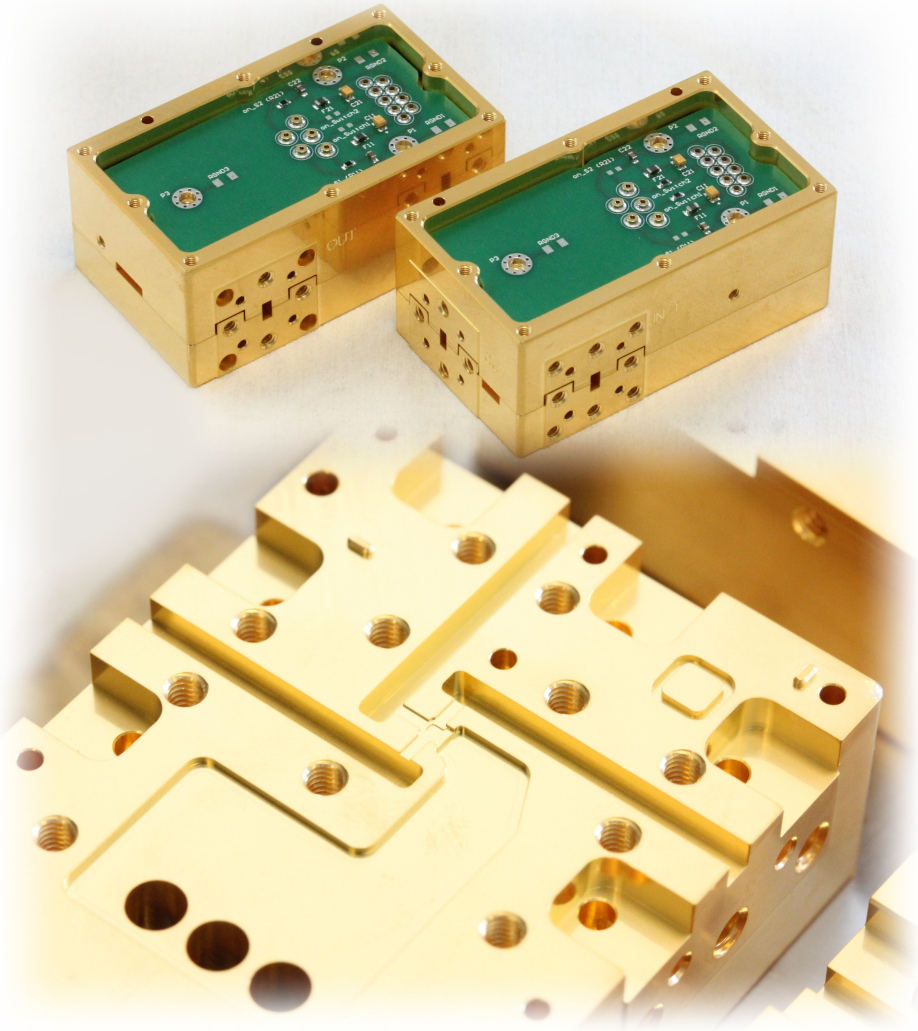

Packaging of a State-of-the-art V-band Active Cold Load and RF Switch

RF Design and Packaging Integration for Millimeter-Wave SiGe MMICs

Master's thesis in Wireless, Photonics and Space Engineering

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Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2026
www.chalmers.se

Master's thesis 2026

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Cover: Photograph of the assembled ACL and RF switch split-blocks (top) and a switch split-block half showing the inner cavity (bottom).

Typeset in LaTeX
Printed by Chalmers Reproservice
Gothenburg, Sweden 2026

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Abstract

Microwave radiometers must be regularly calibrated to maintain high measurement accuracy. Conventional calibration systems often use cold sky and onboard reference views. These different views are typically selected using a rotating mirror. An Active Cold Load (ACL) can provide an electronically controlled cold reference directly in the receiver chain, while a Radio Frequency (RF) switch routes the receiver between the measurement and calibration reference paths.

This thesis presents the packaging and integration of two V-band Silicon-Germanium (SiGe) Monolithic Microwave Integrated Circuits (MMICs), an ACL and an RF switch. The thesis includes the design of a WR-15 waveguide-to-planar transition, bondwire interconnects between MMIC and transition, split-block design and biasing boards. Specifically an E-plane probe on alumina was developed and designed for the SiGe MMIC interface using a Coplanar Waveguide with Ground (CPWG) section and a multi-stage impedance transformer optimized in ANSYS High Frequency Structure Simulator (HFSS).

The transition achieved a simulated return loss of $S_{11} < -26.9$ dB and $S_{21} > -0.3$ dB across the targeted frequency band $50 - 60$ GHz. In addition, a back-to-back structure showed $S_{11} < -17.8$ dB and $S_{21} > -0.6$ dB. Furthermore, a sensitivity analysis was performed, demonstrating that the design remained below $S_{11} < -20$ dB for all investigated variations. The design was evaluated through full-wave electromagnetic (EM) simulations, while the planned scattering parameter and noise temperature measurement procedures are described for future characterization. The simulation results suggest that the proposed packaging design is suitable to realize compact V-band ACL and RF switch modules for radiometer calibration.

Keywords: Active cold load, RF switch, waveguide-to-planar transition, SiGe MMIC, packaging, E-plane probe, split-block.

Acknowledgements

This work would not have been the same without the people behind it. I am especially grateful to my supervisors, Alhassan Aljarosha at Omnisys Instruments and Vessen Vassilev at Chalmers, for their guidance and insight throughout the project. I would also like to thank the MiRACL team at Omnisys: Kalle Kempe for his many fruitful discussions, suggestions and advice, Madeleine Yttergren for generously sharing her knowledge and experience and David Håkansson for sharing his expertise. I would also like to extend my thanks to the rest of the team at Omnisys for their support, contributions and for the opportunity to carry out this work.
Finally, my sincere thanks go to my friends and family for their constant support and encouragement.

Gustav Yngström, Gothenburg, June 2026

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

ACL	Active Cold Load
B2B	Back-to-Back
CNC	Computer Numerical Control
CPW	Coplanar Waveguide
CPWG	Coplanar Waveguide with Ground
DC	Direct Current
DUT	Device Under Test
EM	Electromagnetic
GSG	Ground-Signal-Ground
HFSS	High Frequency Structure Simulator
MMIC	Monolithic Microwave Integrated Circuit
mmWave	Millimeter-Wave
PCB	Printed Circuit Board
PEC	Perfect Electric Conductor
RF	Radio Frequency
SiGe	Silicon-Germanium
SLC	Single Layer Capacitor
SPDT	Single-Pole Double-Throw
S-parameters	Scattering parameters
TE	Transverse Electric
TEM	Transverse Electromagnetic
TM	Transverse Magnetic
TRL	Thru-Reflect-Line
VNA	Vector Network Analyzer

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1
Introduction

The demand for accurate numerical weather prediction continues to grow in order to improve weather forecasting and enable earlier warning of extreme weather events such as floods and droughts. These events can have major societal and economic consequences, making improved forecasting increasingly important. Satellite data collected by microwave instruments play a crucial role for high precision and coverage data. The successful demonstration of the ESA Arctic Weather Satellite (AWS) has further highlighted the growing demand for frequent satellite-based atmospheric observations [1]. Following the demonstration, ESA and EUMETSAT are proceeding with the EPS-Sterna program, which will deploy a constellation of small satellites to provide coverage of atmospheric temperature and humidity measurements [2]. This suggests a clear trend towards compact microwave instruments, especially in small satellites and constellations.

The microwave instruments used for these observations are microwave sounders. Microwave sounders observe the Earth's atmosphere by measuring emitted thermal radiation at microwave frequencies. They typically operate in the frequency range of $(23 - 325)$ GHz. In particular, the $50 - 60$ GHz band is the oxygen absorption band used for temperature and 183 GHz for humidity. Microwave sounders are microwave radiometers that operate with multiple frequency channels, where each channel is sensitive to a different part of the atmosphere. Because the atmospheric absorption varies with frequency, the measured radiation corresponds to different atmospheric layers. By combining the information from all channels, a vertical profile of the atmosphere can be determined [3].

In order to convert the instrument output into brightness temperatures, microwave sounders must be calibrated. This is necessary since the receiver gain and system noise temperature drift with time, aging and temperature. As a result, frequent calibration is required in order to maintain accuracy. For satellite-borne instruments, onboard calibration is often performed by two radiometric reference views using a mechanical motor with a reflector in order to point towards two calibration views: a cold view which typically points towards cold space and an onboard warm calibration target. For example, satellites operated by NOAA and equipped with the Advanced Microwave Sounding Unit-A employ two point calibration using cold space and an internal reference to perform total power calibration [4],[5].

Similarly, the AWS uses a rotating mirror with constant angular rotation in order to direct the receiver view toward the Earth, cold sky and an onboard calibration target using an additional secondary mirror, enabling continuous in orbit calibration [6]. Other combinations, such as, cold space with hot noise source or hot noise source with room temperature can also be implemented at the cost of reduced dynamic range.

This calibration approach requires significant volume to accommodate the physical onboard target, the rotating mechanism and the optical paths. This is particularly relevant in the $50 - 60$ GHz region. At these frequencies, the physical calibration target must be large enough for the beam width and sufficiently deep to provide high emissivity. The lower frequencies can result in calibration targets with dimensions of several centimeters. Calibration using only room temperature and hot references increases the uncertainty when observing colder brightness temperatures.

1.1 Motivation

The mentioned limitations of conventional radiometric calibration are the motivation for developing a compact and integrated solution. A driving factor is the need to reduce the volume, mass and complexity due to the quasi-optical calibration and mechanical moving parts without sacrificing sensitivity or accuracy. Such a solution is especially attractive for compact ground-based weather monitoring systems and for CubeSat and SmallSat constellations, where volume, mass, power consumption and complexity are critical considerations.

This work proposes an alternative to conventional radiometric calibration, utilizing an Active Cold Load (ACL) and a Radio Frequency (RF) switch based on a novel Silicon-Germanium (SiGe) Monolithic Microwave Integrated Circuit (MMIC) design. The ACL provides a well-characterized and electronically controlled cold noise reference directly in the receiver chain and the RF switch is used to electrically route the receiver between different signal paths, such as the measurement path, the ACL reference path and possible external calibration targets without relying on mechanical switching. For example, in an instrument such as the AWS, the onboard calibration target and its associated secondary mirror could potentially be replaced by the ACL and RF switch, reducing the total mass and volume.

It is important to note that an ACL and RF switch do not necessarily remove the need for a rotating mirror. In instruments where the same mirror is also used to scan the Earth scene and obtain a wide swath, the ACL and switch can complement the calibration setup rather than completely replace the scanning mechanism. In such systems, the ACL and switch modules can be used as an additional electronically controlled calibration reference. In this case, both the duration and timing of the reference observation can be selected during operation, allowing the ACL to be activated for a chosen period and at different points in the scan sequence. As a result, the calibration sequence could be adjusted after launch.

The ACL can also be used for laboratory measurements, since a well characterized cold reference often requires liquid nitrogen or a vacuum chamber. In comparison, an ACL could provide a simpler and more convenient alternative for measurements where a compact and repeatable cold reference is needed. Together with the RF switch, different signal paths and calibration states can also be evaluated in a laboratory setup.

Previously, SiGe ACLs have been realized at lower frequencies, demonstrated at L-band in [7] and studied for radiometer calibration at X-band in [8]. The solution proposed in this project would be the first to extend the concept to millimeter-wave (mmWave) frequencies such as $50 - 60$ GHz. The monolithic SiGe BiCMOS technology offers higher integration and lower cost compared to III-V technologies such as GaAs or InP [9]. As a consequence of using SiGe, the MMIC is lacking a metalized backside ground plane, which introduces a grounding constraint that must be addressed in the packaging design.

For clarification, the thesis is motivated by the need to realize a compact calibration solution in practice. More specifically, the work focuses on packaging and integration of an ACL MMIC and an RF switch MMIC, including waveguide-to-planar transitions, biasing structures and mechanical housings for implementation in a radiometric receiver system, while the MMICs are designed externally at Chalmers University of Technology.

1.2 Aim of thesis

The aim of the thesis is to design, manufacture and characterize the packaging and integration of two separate mmWave circuits: An ACL and an RF switch. The main focus is to investigate how packaging affects the performance of the two circuits by comparing the modules to on-chip measurements and evaluate the possibility of using the ACL as a cold reference and the RF switch as an electrically controlled routing component for calibration.

The ACL packaging consist of a waveguide-to-planar transition such that the MMIC interfaces with a standard WR-15 waveguide. The RF switch is based on a Single-Pole Double-Throw (SPDT) circuit, where each port is interfaced to WR-15 waveguide with the same waveguide-to-planar transition as for the ACL module. Figure 1.1 illustrates the concept for the two different modules.

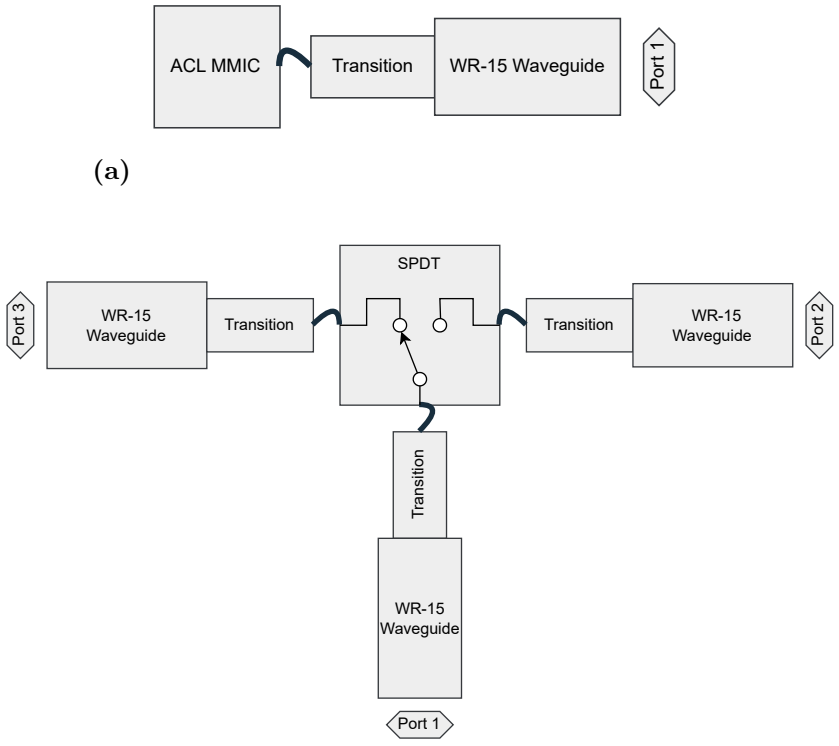


Figure 1.1: (a) ACL module, (b) SPDT switch module.

The ACL and switch are realized as separate modules, thus the performance of each package can be investigated individually. This makes it possible to analyze how the packaging affects the performance by comparing to on-chip measurements. Initially, a third module, where the RF switch and ACL were integrated on the same die was planned to be packaged. However, due to issues with the integrated circuit, this module could not be realized within the scope of this thesis.

2
Theory

The purpose of this chapter is to introduce the theoretical framework for which the design of the packaged modules are based upon. The chapter presents the fundamental microwave theory used to analyze the design, which includes transmission line, network parameters, rectangular waveguide, planar transmission lines and waveguide-to-planar transitions. The fundamental theory is based primarily on [10] and complemented with [11].

2.1 Microwave fundamentals

At microwave frequencies, in comparison to circuit theory, the physical dimensions of the circuit are no longer negligible in comparison to the wavelength. Therefore, the voltage and currents can not be treated as a uniform quantity, instead varying along the wave guiding structure. Transmission line theory provides the tools for analyzing wave propagation, characteristic impedance, reflections and impedance matching in microwave circuits.

2.1.1 Transmission line characteristics

A transmission line can be modeled as cascaded infinitesimal sections of length Δz. Each section is represented with a model of lumped-elements. These elements are series resistance $R\Delta z$, series inductance $L\Delta z$, shunt conductance $G\Delta z$ and shunt capacitance $C\Delta z$, shown in Figure 2.1.

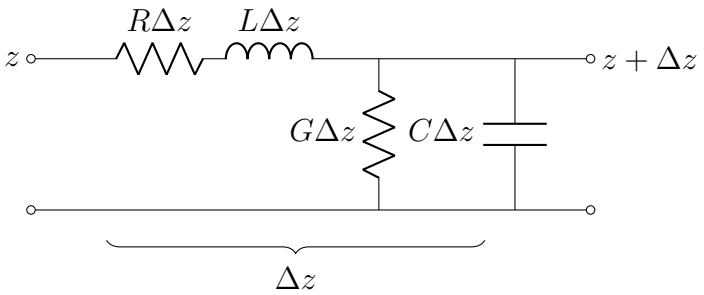


Figure 2.1: Infinitesimal transmission-line section.

The telegrapher equations is derived by taking the limit of the segments as $\Delta z \to 0$ and apply Kirchhoff's voltage and current laws which gives:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.1}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z). \tag{2.2}$$

These equations describes how the voltage and current vary along the transmission line in a steady-state condition. Combining these two equations gives the wave equation for voltage and current on the line and the behavior is described with the complex propagation constant

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta \tag{2.3}$$

where α is the attenuation constant and β phase constant. The general solution for voltage and current can then be written as

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.4}$$

$$I(z) = I_0^+ e^{-\gamma z} - I_0^- e^{\gamma z} \tag{2.5}$$

where V_0^+ and I_0^+ denotes the incident voltage and current, while V_0^- and I_0^- denotes the reflected voltage and current respectively. The characteristic impedance Z_0 is defined as

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.6}$$

hence the current can also be expressed in terms of voltage and characteristic impedance by applying 2.1 with 2.4 gives

$$I(z) = \frac{\gamma}{R + j\omega L}\left(V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}\right) = \frac{1}{Z_0}\left(V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}\right). \tag{2.7}$$

Considering a transmission line terminated with a load Z_L, any discrepancy between Z_L and the characteristic impedance of the line causes a portion of the incident wave to be reflected back. The ratio of the incident wave and reflected wave defines the reflection coefficient for the load at the interface with equation 2.4 and 2.7 gives

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{2.8}$$

The equations above are defined as if the load was seen directly at the interface from the transmission line. Alternatively, the effect of the load can be expressed as the input impedance when seen through a transmission line with length l and terminated by Z_L. Then the input impedance is defined as

$$Z_{in} = Z_0 \frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tanh(\gamma l)}. \tag{2.9}$$

which for a lossless transmission line, where $\gamma = j\beta$ simplifies to

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)}. \tag{2.10}$$

An important matching principle for microwave design is the quarter-wave transformer. For a transmission line section with length $l = \lambda/4$, the input impedance is

$$Z_{in} = \frac{Z_0^2}{Z_L} \tag{2.11}$$

where Z_0 is the characteristic impedance of the quarter-wave section, Z_{in} is the impedance looking into the quarter-wave section and Z_L is the load impedance. The quarter-wave section transforms the load impedance to a different input impedance. Consequently, to obtain a match, the characteristic impedance Z_0 of the quarter-wave section can be chosen such that the transformed input impedance matches the impedance seen at the input side:

$$Z_0 = \sqrt{Z_{in} Z_L} \tag{2.12}$$

which shows how a transmission line with a certain impedance can be used as a impedance transformer.

2.1.2 Scattering parameters

As mentioned in previous section 2.1.1, microwave circuits are often described in terms of incident and reflected waves. This type of wave based description can be extended from a single transmission line to a network by defining wave quantities at each port. Instead of solving the full electromagnetic field distribution of the whole system, the network can be described in a few quantities at the ports. This is practical for many problems, since the interesting quantities is not always the detailed electromagnetic field in each point in space but the interaction between connected components. These port quantities are often effects such as reflections, transmission, loss, impedance mismatch and is intuitive in comparison to a field analysis.

Therefore, microwave circuits are often characterized by scattering parameters (S-parameters), which describes the incoming and outgoing waves at the port. For an N-port network, the relation between the incoming and outgoing waves at all ports is represented by the S-parameter matrix as

$$\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_N \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1N} \\ S_{21} & S_{22} & \cdots & S_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ S_{N1} & S_{N2} & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ a_N \end{bmatrix} \tag{2.13}$$

where a_n represents the incoming wave at port n and b_n the outgoing wave at port n. A specific element of the scattering matrix can be written as

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k=0,\, k\neq j}. \tag{2.14}$$

which is the ratio of the outgoing wave amplitude at port i to the incoming wave amplitude at port j, when all other ports are terminated with matched loads such that there are no reflection from those ports.

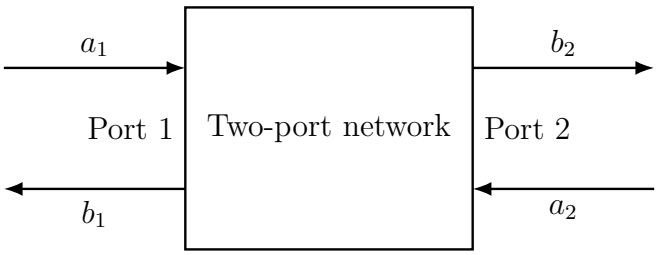


Figure 2.2: Incoming and outgoing waves in two-port network. Incoming wave a_1 and a_2, outgoing waves b_1 and b_2.

For a two-port network, see Figure 2.2, the matrix becomes

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.15}$$

which can also be written as

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.16}$$

$$b_2 = S_{21}a_1 + S_{22}a_2. \tag{2.17}$$

Equation (2.16) and (2.17) describes how each outgoing wave is given by a linear combination of the incident waves at both ports in a two-port network. Consequently, if port 2 is terminated in a matched load the equations gives $S_{11} = \frac{b_1}{a_1}$ which corresponds to the reflection coefficient Γ and $S_{21} = \frac{b_2}{a_1}$ which corresponds to the transmission coefficient looking into port 1 when port 2 is terminated. These reflection and transmission coefficients are often expressed in dB denoted as return loss (RL) and insertion loss (IL) given by

$$RL = -20\log_{10}|S_{11}| \text{ dB}, \tag{2.18}$$

$$IL = -20\log_{10}|S_{21}| \text{ dB}. \tag{2.19}$$

2.1.3 Cascaded networks

The previously discussed S-parameters are used to characterize an arbitrary number of ports, however for a cascade of connections of two or more two-port networks it is convenient to use ABCD matrices. The overall response of a cascade can then be directly obtained by matrix multiplication. For a two-port network, the ABCD matrix relates the total voltage and current at port 1 to the total voltage and current to port 2 as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}. \tag{2.20}$$

The notation is slightly changed in comparison to the S-parameters. Here V_1 and I_1 denotes the total voltage and current at port 1, while V_2 and I_1 denotes the total at port 2. In the convention used here, shown in Figure 2.3, the current I_2 is defined as positive flowing out of port 2.

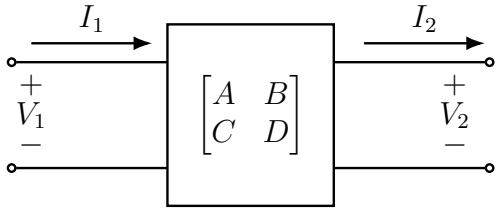


Figure 2.3: Two-port network described by ABCD parameters.

As mentioned, the main advantage of ABCD representation is that a cascaded two-port network can be combined by matrix multiplication and the over response can be obtained. For example for a two cascaded network, as shown in Figure 2.4.

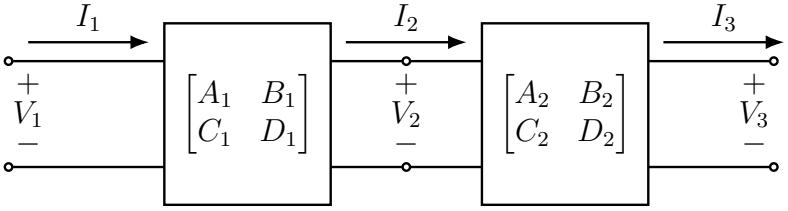


Figure 2.4: Two cascaded two-port networks described by ABCD matrices.

The matrices becomes

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{2.21}$$

and

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_3 \\ I_3. \end{bmatrix}. \tag{2.22}$$

By substituting 2.22 into 2.21 gives the overall relation for the cascaded network

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_3 \\ I_3 \end{bmatrix}. \tag{2.23}$$

Which shows that a cascade of two-port networks can be represented by a single ABCD matrix which is formed by multiplying the individual matrices.

2.2 Rectangular waveguide

A rectangular waveguide is a metallic structure that guides electromagnetic (EM) waves along a defined direction. Energy is confined through reflections at the conducting boundaries, resulting in lower losses compared to other types transmission lines. In addition, the metallic enclosure provides shielding, preventing external fields from coupling into the waveguide. Fundamentally, a rectangular waveguide can propagate Transverse Electric (TE) and Transverse Magnetic (TM) modes however Transverse Electromagnetic (TEM) modes cannot propagate due to TEM mode requires two separate conductors [10].

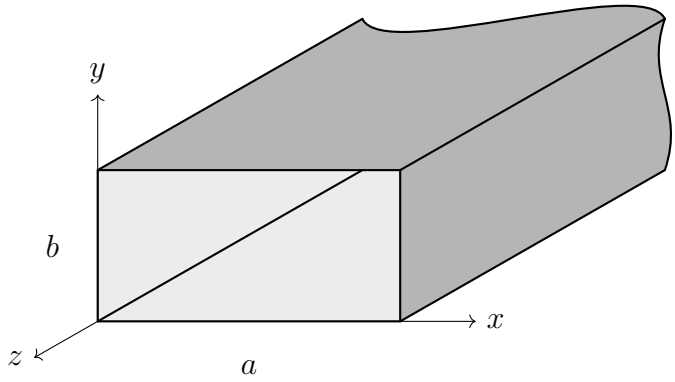


Figure 2.5: Cross section of a rectangular waveguide with $a = 2 \cdot b$.

2.2.1 Waveguide modes, cutoff Frequency and impedance

Rectangular waveguides supports an infinite number of discrete modes, denoted as $TE_{m,n}$ and $TM_{m,n}$ where m and n are integers corresponding to the field variations in the transverse directions [10],[11]. The longitudinal field variation in a rectangular waveguide can be written as

$$\mathbf{E}(x, y, z) = \mathbf{E}_t(x, y)\, e^{-\gamma z} \tag{2.24}$$

where γ is the complex propagation constant defined as

$$\gamma = \alpha + j\beta \tag{2.25}$$

with α representing the attenuation constant and β the phase (propagation) constant. The propagation characteristics follow from the waveguide dispersion relation

$$k^2 = \beta^2 + k_c^2 \tag{2.26}$$

where $k = \omega\sqrt{\mu\varepsilon}$ is the wavenumber in the medium and k_c is the cutoff wavenumber determined by the waveguide geometry

$$k_c^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2. \tag{2.27}$$

Propagation requires β to be real which means $k > k_c$. The cutoff condition corresponds to $\beta = 0$, giving the cutoff frequency

$$f_{c,mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}. \tag{2.28}$$

When $f > f_c$, the propagation constant becomes

$$\beta = \sqrt{k^2 - k_c^2} = k\sqrt{1 - \left(\frac{f_c}{f}\right)^2}, \tag{2.29}$$

and the mode propagates along the waveguide.
The wave impedance for a transverse electric (TE) mode is

$$Z_{TE} = \frac{\omega\mu}{\beta}. \tag{2.30}$$

Since β depends on frequency, the wave impedance is frequency dependent. As the operating frequency approaches the cutoff frequency, $\beta \to 0$ and the wave impedance increases rapidly. Assuming the waveguide is air filled and $f \gg f_c$, $Z_{TE} \to \eta_0 \simeq 377\,\Omega$, meaning that the guided structure approaches the behavior of free space.
When $f < f_c$, β becomes imaginary and the propagation constant is purely real

$$\alpha = \sqrt{k_c^2 - k^2} = k_c\sqrt{1 - \left(\frac{f}{f_c}\right)^2}, \tag{2.31}$$

meaning that the field components decay exponentially as

$$\mathbf{E}(z) = \mathbf{E}_0 e^{-\alpha z}. \tag{2.32}$$

Such modes are called cutoff modes or evanescent modes. The attenuation in decibels over a distance z is

$$A_{dB}(z) = 8.686\,\alpha z. \tag{2.33}$$

Practical waveguide systems, are typically designed to operate exclusively in TE_{10} which is called the fundamental or dominant mode. Ensuring single mode operation is essential as simultaneous propagation of multiple modes leads to dispersion and distortion which may degrade the signal integrity.

The cut off frequency of the dominant TE_{10} mode, obtained from eq. 2.28 is given by:

$$f_{c,10} = \frac{1}{2a\sqrt{\mu\varepsilon}} \tag{2.34}$$

To maximize the frequency separation of dominant mode and higher order modes, practical waveguides are designed such as $a = 2b$. This ensures that the next propagating mode, which is either TE_{20} or TE_{01} and by using eq. 2.28 have cutoff frequencies:

$$f_{c,20} = \frac{1}{a\sqrt{\mu\varepsilon}} \qquad f_{c,01} = \frac{1}{2b\sqrt{\mu\varepsilon}} \tag{2.35}$$

which becomes equal. Therefore, for a typically dimensioned waveguide the higher order modes start to propagate at exactly twice the cutoff frequency of the dominant mode:

$$2f_{c,10} = f_{c,20} = f_{c,01}. \tag{2.36}$$

Table 2.1 presents the most common standardized rectangular waveguide dimensions for mmWave applications and their corresponding frequency band [12].

Waveguide	**Frequency Range (GHz)**	**Band**
WR-62	12.4-18	Ku
WR-42	18 – 26.5	K
WR-28	26.5 – 40	Ka
WR-22	33 – 50	Q
WR-19	40 – 60	U
WR-15	50 – 75	V
WR-12	60 – 90	E
WR-10	75 – 110	W
WR-8	90 – 140	F
WR-6	110 – 170	D
WR-5	140 – 220	G
WR-4	180 – 260	H
WR-3	220 – 325	J

Table 2.1: mmWave rectangular waveguide standards

The guided wavelength, λ_g, describes the wavelength of the wave propagating inside the waveguide. It is defined from the propagation constant β from eq 2.29 as:

$$\lambda_g = \frac{2\pi}{\beta} = \frac{2\pi}{k\sqrt{1-\left(\frac{f_c}{f}\right)^2}} = \frac{\lambda_0}{\sqrt{1-\left(\frac{f_c}{f}\right)^2}}, \tag{2.37}$$

where $k = \frac{2\pi}{\lambda_0}$ is the wavenumber in free space, f is the operating frequency, and f_c is the cutoff frequency.

2.2.2 Rectangular waveguide electric and magnetic field distribution

As discussed in Section 2.2.1, the mode indices m and n defines the discrete waveguide propagation modes and determine the cutoff frequencies. In addition, they describe how the fields vary across the waveguide cross-section. The metallic walls impose the boundary conditions such that the tangential electric field must be zero at the conducting walls [10]. Therefore, the field distribution inside the waveguide form a standing wave pattern. For the dominant TE_{10} mode, the field have a half wave variation across the broadside a, while no variation occurs along the narrow wall b, see Figure 2.6. For the TE_{20} mode, the field have two half waves across the broad wall, resulting in another standing wave pattern. In the TE_{01} mode, the variation occurs instead across the narrow wall b. The TE_{11} mode exhibits variation in both directions and can therefore be regarded as a combination of the field variations along both a and b. Each mode is associated with a unique field distribution, propagation constant β, and cutoff frequency f_c.

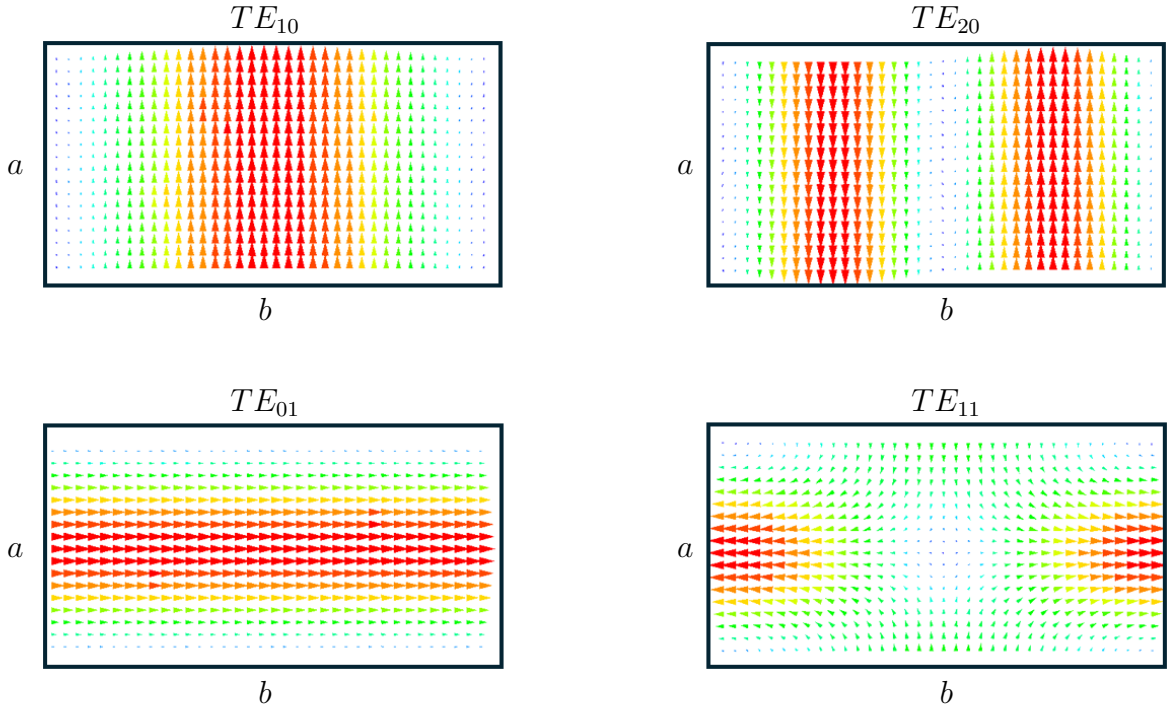


Figure 2.6: Electric field distributions of different modes in rectangular waveguides. Illustrating standing wave variation across the waveguide walls. From blue (weak electric field) to red (strong electric field).

2.2.3 E-plane and H-plane split-block waveguides

For a rectangular waveguide operating in TE_{10} the most widely used manufacturing configurations are to either split the waveguide in E-plane or H-plane, shown in Figure 2.7. This is due to conventional Computer Numerical Control (CNC) machining techniques, where the geometry is realized by machining two separate blocks that are laterally aligned and assembled into one piece. For a H-plane split, the waveguide is divided along the plane in parallel to the broad wall a and for the E-plane split, the waveguide is divided along the plane parallel to the narrow wall b.

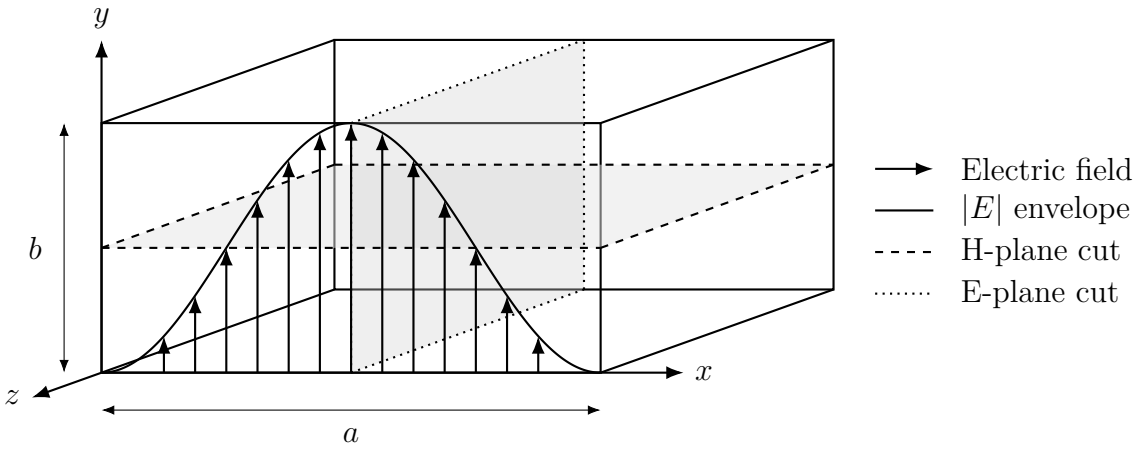


Figure 2.7: Rectangular waveguide with dimensions a and b, showing the TE_{10} E-field distribution, with wave propagation in z-direction. The shaded regions indicate the H-plane and E-plane cuts.

For a rectangular waveguide operating in TE_{10} mode, an E-plane split is generally preferred over an H-plane split in conventional split-block waveguides. The main reason is since for an H-plane split, the split is perpendicular to the surface current on the waveguide wall, such that the current path is cut by the split. In contrast, the E-plane split better preserves wall-current continuity. Additionally, the low loss properties of E-plane split waveguides are further supported by reported low-loss performance for E-plane split-block waveguides, where an average loss of $\simeq 0.04\ dB/cm$ has been reported for WR10 waveguide. Therefore, the E-plane split is generally regarded as a more robust choice with respect to maintaining the surface current path and reduce losses [13],[14],[15].

Furthermore, it should be noted that this preference for E-plane splits are not universal. For other applications and fabrication technologies such as some silicon micro-machined waveguides, H-plane and double H-plane split have been studied to be beneficial due to being less sensitive to misalignment during assembly and can reduce the effect of etched sidewall roughness, consequently reducing the insertion loss at higher frequencies [16].

2.3 Planar transmission lines

Planar transmission lines are guided structures, meaning the electromagnetic fields are confined and directed along a path by the geometry of the conductors and surrounding dielectric medium, rather than allowing the waves to radiate into free space. The most common planar transmission structures are: microstrip line, coplanar waveguide (CPW), coplanar waveguide with ground (CPWG) and stripline. Although MMIC processes can provide multiple metal layers for routing and passive components, the RF signal paths are typically implemented using microstrip or CPW/CPWG in MMIC design [17]. For microstrip and CPW/CPWG a true transverse electromagnetic (TEM) mode cannot exist because the fields propagate partly in a dielectric substrate and partly in air, meaning the fields are not confined between two conductors in a homogeneous medium. As a consequence, these structures support a quasi-TEM mode, where non TEM fringing components are small, thus the propagation characteristics closely resemble those of a pure TEM.

2.3.1 Microstrip lines

Microstrip lines are widely used in MMIC technology and other RF applications, the microstrip line is constructed in a inhomogeneous medium with a dielectric substrate between the strip conductor and the ground plane, shown in Figure 2.8. Due to its ease of fabrication and convenient integration with other RF structures, the microstrip lines are one of the most commonly used planar transmission lines.

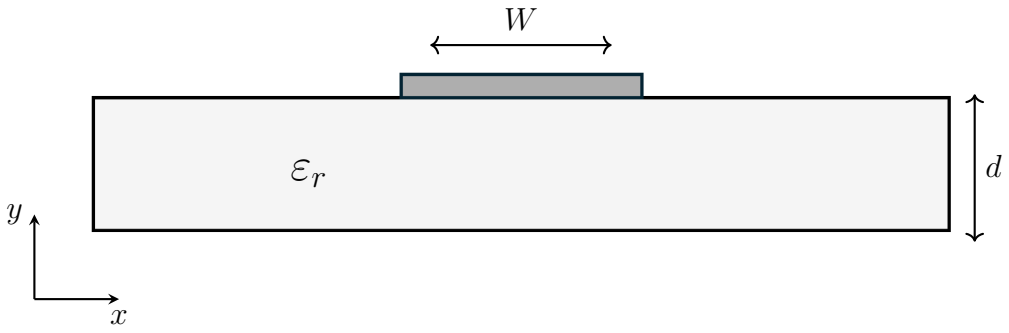


Figure 2.8: Cross section of a microstrip line showing conductor width W, substrate thickness d, and substrate relative permittivity ε_r.

A microstrip line consist of a conductor with width W, placed on top of a substrate with thickness d and relative permittivity ε_r. Due to the inhomogeneous structure a microstrip line is not true TEM and therefore, commonly characterized using an effective relative permittivity ε_e. For a microstrip line in air, the effective permittivity satisfies:

$$1 < \varepsilon_e < \varepsilon_r \tag{2.38}$$

The effective relative permittivity can be calculated as:

$$\varepsilon_e = \begin{cases} \dfrac{\varepsilon_r + 1}{2} + \dfrac{\varepsilon_r - 1}{2} \left[\dfrac{1}{\sqrt{1 + 12\frac{d}{W}}} + 0.04 \left(1 - \dfrac{W}{d}\right)^2 \right], & \text{for } \frac{W}{d} \leq 1 \\ \dfrac{\varepsilon_r + 1}{2} + \dfrac{\varepsilon_r - 1}{2} \dfrac{1}{\sqrt{1 + 12\frac{d}{W}}}, & \text{for } \frac{W}{d} \geq 1 \end{cases} \tag{2.39}$$

and the characteristic impedance Z_0 is given by the ratio of W/d with the effective permittivity:

$$Z_0 = \begin{cases} \dfrac{60}{\sqrt{\varepsilon_e}} \ln\left(\dfrac{8d}{W} + \dfrac{W}{4d}\right), & \text{for } \frac{W}{d} \leq 1 \\ \dfrac{120\pi}{\sqrt{\varepsilon_e}} \left[\dfrac{1}{\frac{W}{d} + 1.393 + 0.667 \ln\left(\frac{W}{d} + 1.444\right)} \right], & \text{for } \frac{W}{d} \geq 1 \end{cases} \tag{2.40}$$

As can be seen in equation (2.40) the characteristic impedance is determined by the ratio of the conductor width and substrate thickness and effective permittivity. Consequently, for a fixed substrate height, a wider strip gives lower impedance.

Because the air and dielectric substrate have different permittivity the mode propagation is not a pure TEM hence the name quasi-TEM which means it resembles TEM propagation. Figure 2.9 below shows how the electric and magnetic fields look for a microstrip line.

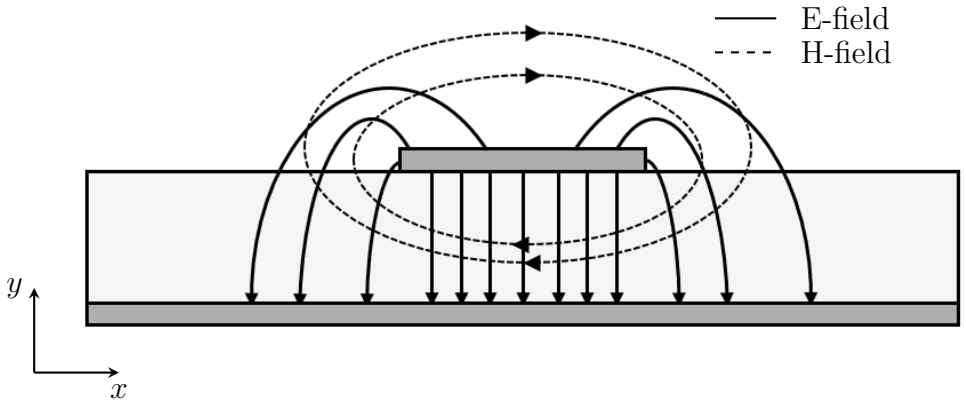


Figure 2.9: Electric and magnetic field distribution for a quasi-TEM mode in microstrip line.

The previously introduced expressions in (2.39) and (2.40) are commonly used to estimate the effective permittivity and characteristic impedance of a microstrip line. However, these expressions are approximate and assume open region around the microstrip. In practical implementations, including this work, the microstrip substrate is often implemented with nearby metallic walls, which affects the field distribution and consequently the permittivity and characteristic impedance. Therefore, these expressions are mainly used for initial estimate, while a full EM simulation is used to obtain more accurate result.

2.3.2 Coplanar waveguide and coplanar waveguide with ground

Coplanar waveguide and (CPW) is a planar transmission line where the signal conductor is placed in the middle of two surrounding ground conductors in the same plane. In coplanar waveguide with ground (CPWG), a backside ground plane is added on the bottom of the substrate. This configuration resembles a combination of microstrip and CPW. In addition, adding the backside ground plane modifies the field distribution in comparison to conventional CPW and generally leads to stronger confinement of the fields inside the substrate [17], see Figure 2.10.

Similarly for as for the microstrip case, the CPW/CPWG characteristic impedance and effective permittivity ε_e are determined by the conductor width, substrate thickness, relative permittivity ε_r and the gap between the ground signal ground configuration. In practical structures, the finite top ground width also affects the characteristic impedance and effective permittivity compared to the ideal case. In contrast to microstrip, a CPW or CPWG can support both odd and even modes. This is because it consist of multiple conductors where the grounds can have different potential. As a result the structure can excite both odd and even modes. Closed form expressions to calculate the characteristic impedance for CPW and CPWG exist, as for microstrip eq (2.40 and 2.39).

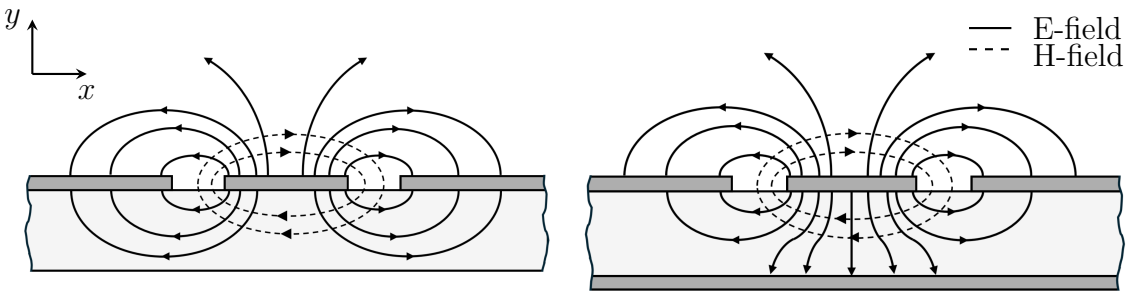


Figure 2.10: Electric and magnetic field distributions in (a) CPW and (b) CPWG.

CPWG is also the necessary interface for the MMICs used in this work. Unlike GaAs MMICs, which provide RF grounding through a metalized backside, the SiGe MMICs used in this work have no backside ground plane and the ground reference must therefore be provided by coplanar on the topside.

2.4 Waveguide-to-planar transition

Waveguides are commonly used in mmWave radiometric front ends due to their low insertion loss and integration with other passive front-end components such as antennas. However active components in the receiver chain are on planar substrates such as mixers and amplifiers. Therefore, a transition is needed to transfer the EM wave from the rectangular waveguide to a planar transmission line. The principle of a EM transition is based on coupling between the TE_{10} mode in the waveguide to a quasi-TEM mode on planar transmission line. The transition can be analyzed in terms of S-parameters, by its insertion loss and return loss. In general, a transition mainly performs two objectives:

- *Modal conversion*, that the electromagnetic fields are gradually changed from one mode to another
- *Impedance matching*, that the high waveguide impedance is matched to the low impedance of the planar line in order to minimize reflections

2.4.1 In-line transitions

In order to achieve a transition, several types of topologies have been proposed, such as the in-line ridged waveguide-to-CPWG transition in [18], where a ridge is placed in one broad wall and a slot in the opposite wall. The CPWG is placed at the end of the waveguide, while the ridge gradually splits and rotates the TE_{10} field into the quasi-TEM mode at the CPWG. Other in-line transitions, meaning transitions placed along the propagation direction of the waveguide, include in-line tapered fin transitions [19] and antipodal fin transitions [20]. These topologies are similar to the ridge case in the sense that they achieve modal conversion by gradually changing the electric field along the propagation direction, typically by using stepped or tapered structures.

Figure 2.11 shows the modal conversion for a ridged transition to CPWG and antipodal in-line transition to microstrip with the transition in same direction as the propagating wave, each sub figure represent the cross-section along the propagation direction, redrawn from [18], [20].

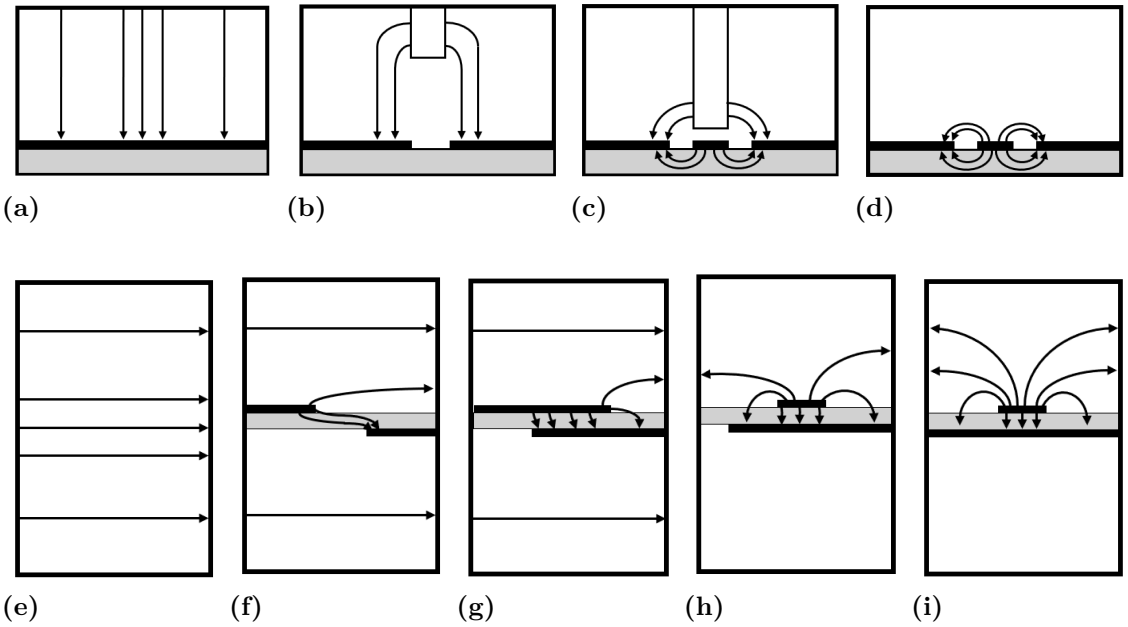


Figure 2.11: (a)-(d) modal conversion for ridged waveguide-to-CPWG transition, (e)-(i) modal conversion for antipodal fin-line transition from waveguide-to-microstrip.

As mentioned, these types of transitions achieves modal conversion by gradually changing the electric field. However, in contrast, other type of transitions such as the E-plane probe operates differently, discussed further in the following section.

2.4.2 E-plane probe transition

An E-plane probe is a widely used transition between a waveguide and a planar transmission line. Various probe geometries have been proposed, including dipole [21], radial [22], and bow-tie shaped probes [23]. This work focuses on a single-ended rectangular E-plane probe, which consists of a microstrip or coplanar waveguide (CPW) that extends into the waveguide through an aperture, perpendicular to the propagation direction [24],[25]. Depending on the implementation, the probe can be inserted in a broadside configuration, where the substrate faces the backshort or in a longitudinal configuration, where the substrate is oriented parallel to the waveguide propagation direction, as shown in Figure 2.12.

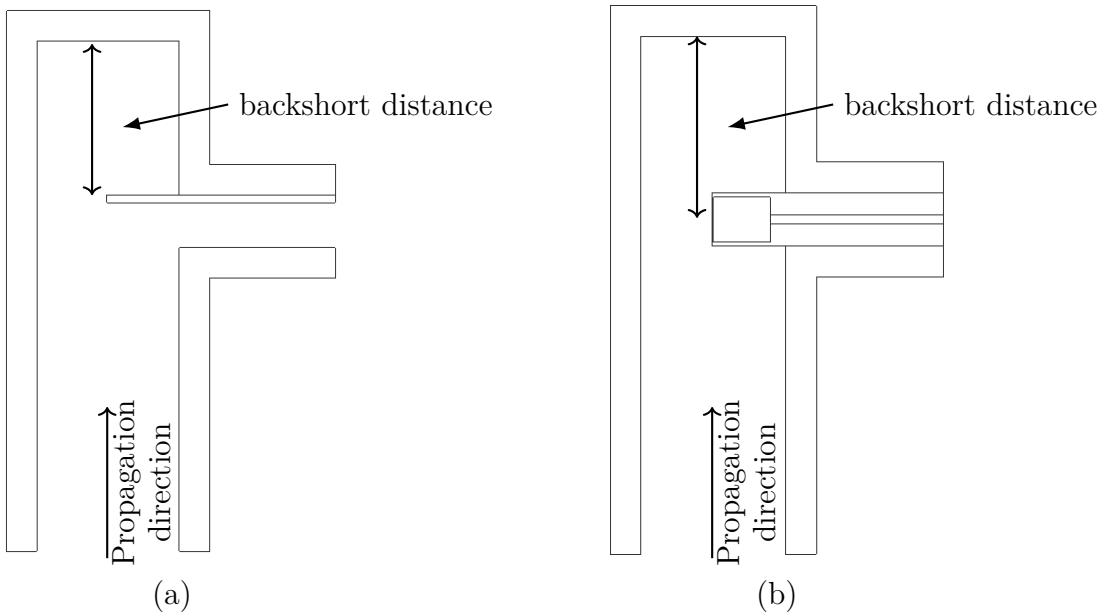


Figure 2.12: (a) Broadside and (b) longitudinal probe alignment.

The microstrip line or CPW is fabricated on a dielectric substrate, the probe is formed by extending the signal conductor beyond the ground plane edge. Inside the cavity the probe interacts with the propagating TE_{10} mode. The probe is placed such that the maximum field couples to the probe, which induces currents on the probe and launches a quasi-TEM mode on the planar transmission line. The current is then guided onto the planar transmission line, thereby converting it to the corresponding quasi-TEM mode.

The field distribution can be controlled in the cavity by placing the metallic wall at a specific distance from the probe, see Figure 2.12. The operating principle of the backshort wall is illustrated in Figure 2.13. At the backshort wall, the boundary condition requires the tangential electric field components to be zero. This creates a pattern in the waveguide cavity such that the electric field reaches a maximum at approximately one quarter wave ($\lambda_g/4$) from the backshort. Therefore, by positioning the probe near this location, it enforces a strong coupling of the field onto the probe.

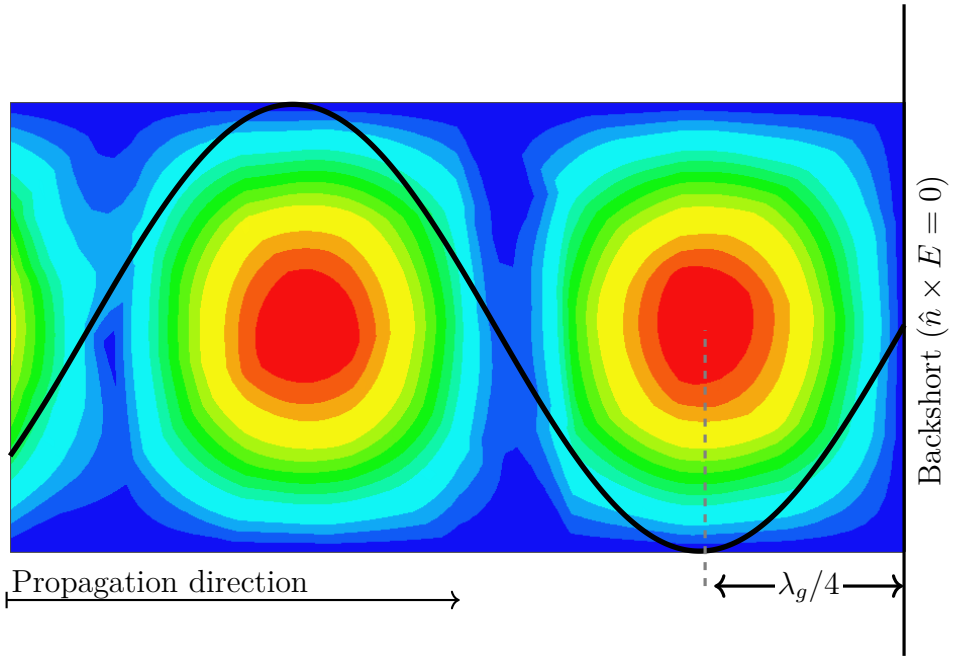


Figure 2.13: Electric field distribution in waveguide cavity illustrating the backshort boundary condition. The electric field reaches maximum at $\lambda_g/4$.

The probe itself introduces a discontinuity and the impedance of the waveguide is often much higher than the planar transmission line, which must be compensated with impedance matching. The impedance matching of an E-plane probe is often implemented with a multi section matching network. This impedance matching section often consists of one or more matching network elements depending on the application. Additionally, the rectangular E-plane probe can be considered as a monopole antenna radiating into the waveguide. A monopole positioned over an infinite ground plane achieves resonance when the reactive components are zero. This happens when the length of the monopole is approximately a quarter-wavelength ($\lambda/4$) and the monopole is then purely a resistive load [26].

2.5 Noise in microwave systems

Any resistive material at a temperature above absolute zero exhibit random motions of electrons [10]. This random motion has kinetic energy which is proportional to the temperature. As a result, a resistor exhibits small random voltage and current fluctuations, which causes noise.

2.5.1 Noise representation

In microwave systems, the noise is often described in terms of noise power [10]. The available thermal noise power P_n over a bandwidth B is given by

$$P_n = kTB \tag{2.41}$$

where k is the Boltzmann's constant and T is the temperature. The expression shows that the thermal noise power is proportional to both the bandwidth and temperature.

For a two-port networks such as an noisy amplifier, instead of describing all noise mechanisms separately, it is convenient to describe the total noise generated by the network. The total noise can be represented by an equivalent input noise temperature T_e. In this way, a noisy amplifier is modeled as a ideal noiseless device with additional noise at the input. The output noise power can then be written as

$$P_{n,out} = Gk(T_{in} + T_e)B \tag{2.42}$$

where T_{in} is the source input noise temperature, for example 290 K for a 50 ohm matched load in room temperature (RT) and T_e is the equivalent input noise temperature added by the amplifier itself and G is the gain of the amplifier.

2.5.2 Y-factor

The Y-factor method is commonly used for determining the noise performance of a receiver or amplifier [27, 28]. The method is based on measuring the output power of two known input sources, with the source temperatures denoted as T_{s1} and T_{s2} respectively. The corresponding measured output noise powers are denoted as

$$N_1 = Gk(T_{s1} + T_e)B \tag{2.43}$$

$$N_2 = Gk(T_{s2} + T_e)B \tag{2.44}$$

and the Y-factor is defined as the ratio between these two noise powers

$$Y = \frac{N_1}{N_2} = \frac{T_{s1} + T_e}{T_{s2} + T_e}, \qquad T_e = \frac{T_{s1} - YT_{s2}}{Y - 1} \tag{2.45}$$

where the two input reference temperatures must be different and $T_{s1} > T_{s2}$. Thus, the equivalent noise temperature of the noisy receiver or amplifier can be determined from two measured output noise powers and two known reference temperatures.

3
Design

This chapter presents the design of the packaging for the ACL and RF switch MMICs. The work focuses on the RF design for the waveguide-to-planar transition, using an E-plane probe and its integration into the split-block housing, including mechanical design and DC biasing board for the MMICs.

In this work, ANSYS High Frequency Structure Simulator (HFSS) was used for the EM design and analysis of the transition and package integration. HFSS is a 3D full-wave solver based on the finite element method (FEM), used to simulate the EM performance of parametrized 3D models. The design process consisted of defining the waveguide, transition geometry, material properties and boundary conditions after which simulations, parameter sweeps and optimization tools were used to refine the dimensions. The transition performance was evaluated using S-parameters, such as return loss S_{11} and insertion loss S_{21}, as well as impedance behavior and field distribution. In the simulation setup, the waveguide, transition and DC boards were fully enclosed by a metallic structure with Perfect Electric Conductor (PEC) walls. Additionally, a user-defined alumina substrate was used in accordance with material parameters provided by the manufacturer SERMA Microelectronics.

Material	ε_r	μ_r	Dielectric loss tangent	Density (g/cm^3)
Alumina (Al_2O_3)	9.6	1	0.0003	3.86

Table 3.1: Material parameters used for the alumina substrate in the HFSS simulation based on manufacturer specifications.

The RF design process begins with the WR-15 waveguide and an initial E-plane probe. The first dimensions, such as the probe length, probe width and back-short distance are estimated from theory and previous works. The geometry is then adapted to the present work by considering package constraints, i.e. MMIC placement, Ground-Signal-Ground (GSG) pad interface, bondwire connection and split-block layout. Finally, the complete transition is optimized for return loss, S_{11}, and evaluated through sensitivity analysis to dimensional and assembly variations.

The mechanical and PCB design focuses on realizing manufacturable split-block modules for both the ACL and switch MMICs based on the RF layout. The split-block must integrate the waveguide transition, MMIC, biasing board and bondwire connections while maintaining correct alignment and practical assembly. The biasing boards were designed with a modular approach, allowing different bias and filtering configurations to be tested without changing the RF package.

3.1 RF Design

The RF design consists of the waveguide-to-planar transition and its integration into the split-block layout. Although the transition can be designed and optimized on its own from an EM perspective, it must be designed such that it can be realized in the physical layout of the split-block. Additional constraints such as MMIC placement, bondwire length and height, DC routing and mechanical tolerances influence the final geometry. Therefore, the transition design must be verified against the mechanical layout to ensure that both EM performance and practical integration requirements are satisfied.

3.1.1 Design specifications

The objective of the RF design is to realize waveguide-to-planar transitions suitable for packaging two separate MMIC modules, the ACL and RF switch. Each module is implemented in its own split-block housing operating in V-band ($50 - 60$ GHz). The transitions must provide efficient coupling between a standard RWG interface to the pads on the MMIC. Although the ACL and switch are packaged in separate modules, the design requirements for the transitions are similar and must satisfy the following specifications:

- Operation across $50 - 60$ GHz range.
- Integration with SiGe MMIC technology
- Input/Output return loss $<$ -15 dB
- Compact geometry to facilitate short bondwire interconnects
- Compatibility for practical bondwire assembly
- Sufficient space for DC routing for both bias PCB and switch integration
- Bias decoupling and RF isolation for DC paths (decoupling capacitors and filtering).
- Robustness for machining tolerances and assembly

The transition is therefore not only optimized for EM performance but also constrained by the practical implementation due to transition fabrication capabilities, split-block machining tolerances and assembly considerations.

3.1.2 Initial design

The initial design concept was inspired by [24], as discussed in Section 2.4.2. The implementation and parameter selection in this work were developed independently and do not follow their design methodology or starting dimensions. The structure consists of a rectangular waveguide with a microstrip substrate inserted into the waveguide wall, see Figure 2.12. The E-plane probe is selected to be oriented in the longitudinal direction, as discussed in Section 2.4.2, primarily selected because it is better suited to the split-block implementation, where all internal cavities could be arranged along the same plane.

3.1.2.1 Standard rectangular waveguide WR-15

The targeted frequency range is $50-60$ GHz, therefore a standard WR-15 waveguide was selected, with inner dimensions $(a \times b) = (3.759 \times 1.88)\ mm$. The waveguide supports single-mode operation of TE_{10} from $40 - 75$ GHz. Figure 3.1 shows the rectangular waveguide model created in HFSS. A wave port is assigned at the waveguide end, as seen in 3.1b and excited with dominant TE_{10} mode. The electric field varies in x-direction and the wave propagates in z-direction. The thin line in the center of the waveguide indicates the intended machining split plane of the module. Consequently, at the end on the opposite side from the port, the CNC process does not allow for sharp 90° corners, thus the corners must be rounded and is selected to a radius of 0.5 mm.

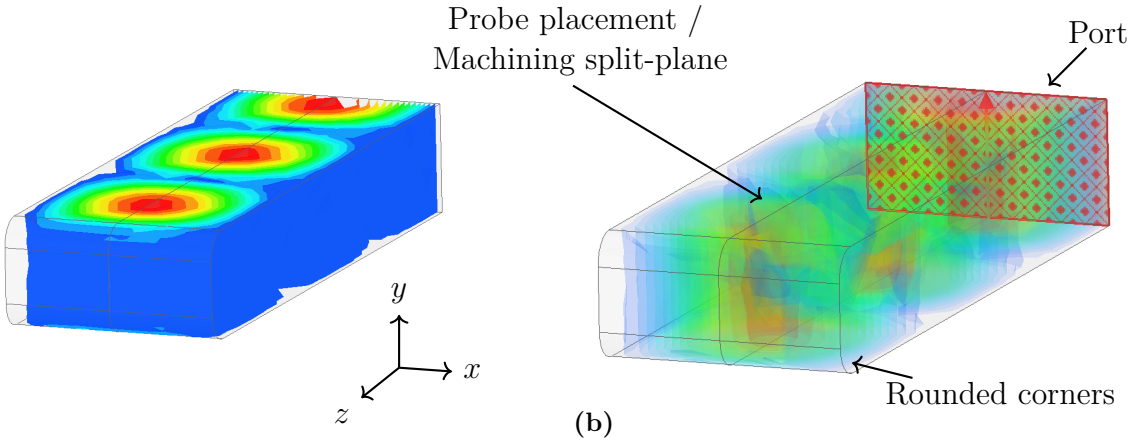


Figure 3.1: (a) Electric field distribution of the dominant TE_{10} mode in the WR-15 waveguide. (b) Illustrates wave port definition and excitation in HFSS also machining split-plane and rounded corners.

3.1.2.2 Probe channel sizing

After defining the standard waveguide dimensions, the next dimensions to be established are those of the waveguide channel where the probe substrate is placed. The selected dimensions are: width $W_c = 750\ \mu m$ and height $H_c = 500\ \mu m$, shown in Figure 3.2. This cavity acts as a partially loaded waveguide and its dimensions must satisfy two conditions.

- The cavity must suppress waveguide propagation within the channel by being small enough such that the cutoff frequency f_c is significantly larger than the operating frequency.
- The cavity must be large enough for practical implementation, i.e. features such as the CPWG structure, via-hole fabrication and mechanical manufacturing tolerances.

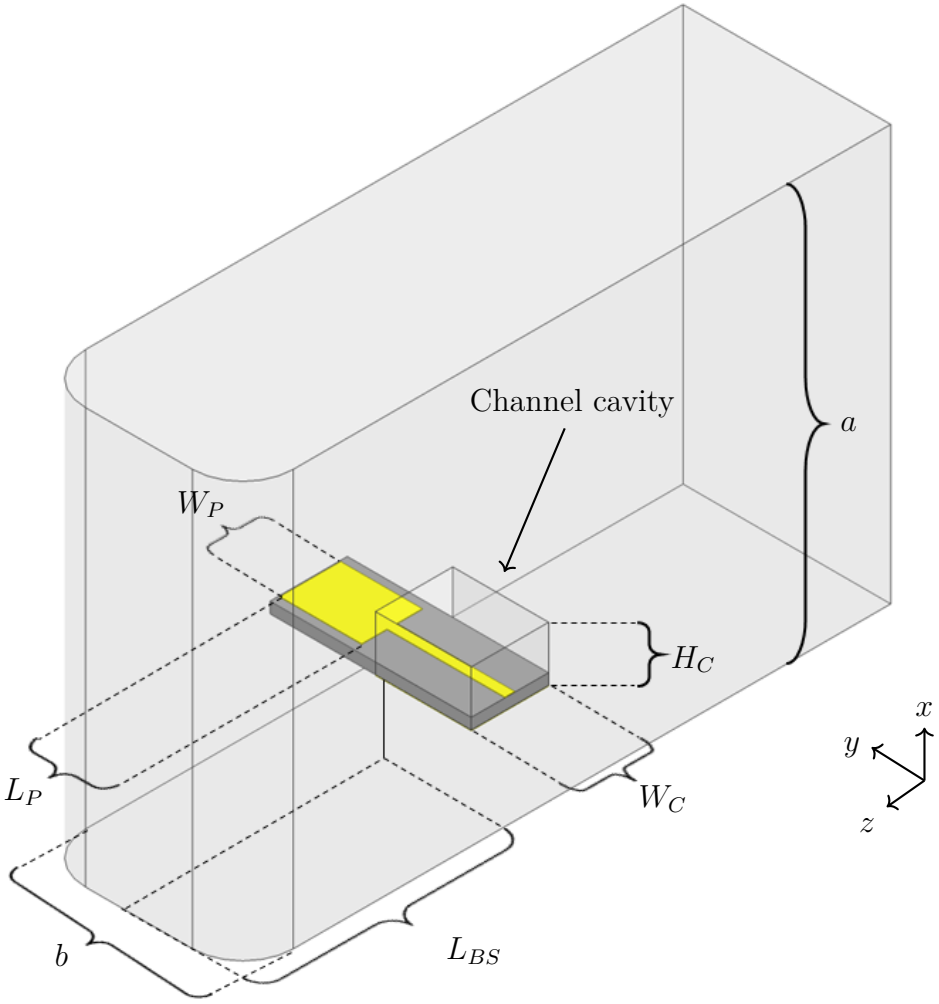


Figure 3.2: WR-15 waveguide dimensions a and b, and the transition channel dimensions W_c and H_c. Wave propagation in z-direction for WR-15 waveguide cavity with TE_{10} mode.

For suppressing waveguide propagation inside the channel cavity, the channel can be treated as a rectangular waveguide with cross section $a_c = W_c = 750\ \mu m$ and $b_c = H_c = 500\ \mu m$. By using eq. 2.28 the cutoff frequency for the dominant TE_{10} mode is

$$f_{c,10} = \frac{c}{2W_c} \simeq 200\ GHz \tag{3.1}$$

However, this is by assuming that the channel is filled with air which is not the case. Instead, the channel is partially filled with a dielectric and thus the cutoff frequency will be lower. Considering the worst case for a fully filled channel with alumina dielectric with permittivity $\varepsilon_r = 9.6$ the cutoff frequency for the dominant TE_{10} mode is approximately

$$f_{c,10}^{filled} = \frac{c}{2W_c \cdot \sqrt{\varepsilon_r}} \simeq 64.5\ GHz \tag{3.2}$$

In addition, there is an air gap between the substrate and the channel, metallization for the microstrip and CPWG structure and vias. Therefore, there is to the author's knowledge no simple expression to numerically solve for the exact cutoff frequency for the structure. However, by assuming the worst case, the cutoff frequency for the fully loaded waveguide, where $f_{c,10}^{filled} \simeq 64.5$ GHz is above the target range of $50-60$ GHz.

The length of the protruding channel cavity must be selected with respect to the complete package. Initially a shorter probe was considered. However, when the complete switch package was designed, the spacing between adjacent waveguide cavities was very thin $\simeq 100\mu m$. Such thin wall is difficult to manufacture since machining tolerances may lead to misalignment or cavity imperfections. Therefore, a longer probe was designed in order to increase the separation. In this work, the total probe length L_{sub} was selected to be 3 mm such that the protruding channel length is approximately 2 mm, shown in Figure 3.3. The discussed wall with adjacent waveguide cavities is shown in Figure 3.4 for the 3 mm probe case. Initially, with shorter probes the wall was approximately $\simeq 100\ \mu m$. However, with the longer probes the adjacent cavity walls are more than 0.86 mm thus reliable for manufacturing.

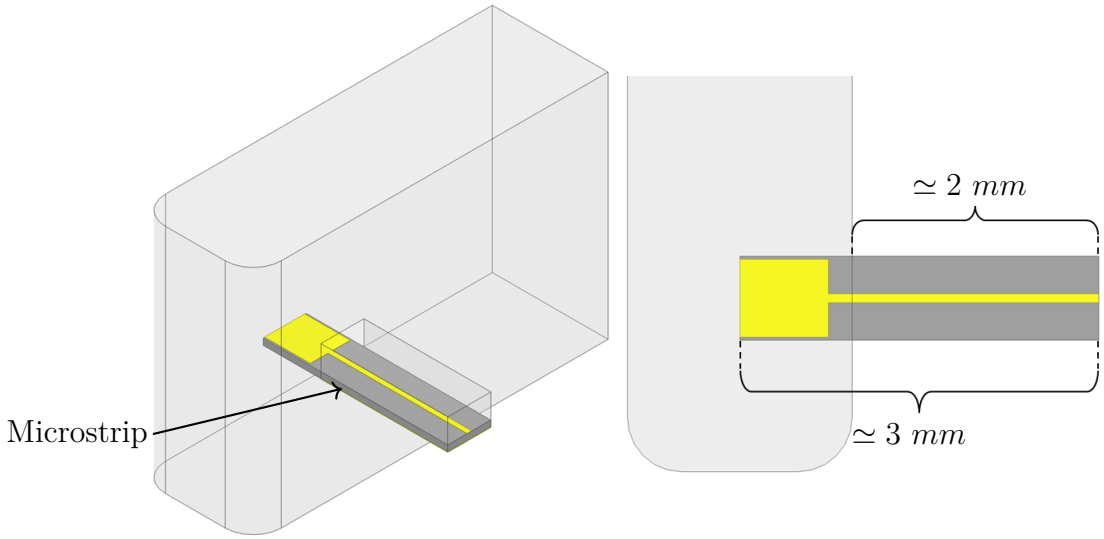


Figure 3.3: Figure illustrating total length of the initial microstrip probe and protruding probe length.

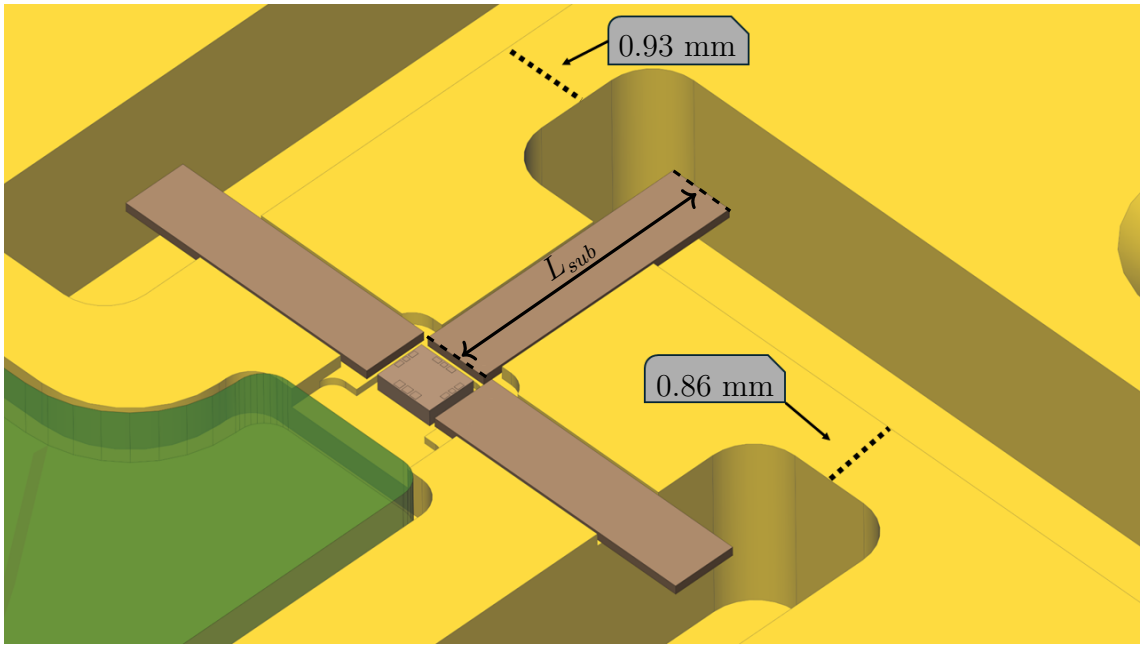


Figure 3.4: Illustrating the backshort wall to adjacent wall distance, designed accommodated for manufacturability, where $L_{sub} \simeq 3\ mm$, depicted as the brown substrate.

3.1.2.3 Probe design and backshort distance

For the transition substrate, a thickness of $H_{sub} = 100\ \mu m$ was selected, which was the thinnest available substrate from the probe manufacturer. Although the initial design is based on a microstrip structure, the substrate thickness was chosen with the later CPWG implementation (Section 3.1.3) in mind. The CPWG requires grounding vias to connect the top and bottom ground metallization and a thinner substrate allows for smaller via diameters, which alleviates the spatial constraints that the CPWG impose. The required via space is determined by both the via diameter and the minimum annular ring needed for manufacturing. A thicker substrate would require larger vias, further limiting the space available for the track width and gap of the coplanar structure.

Prior to any secondary matching networks such as dedicated impedance transformers are implemented, the probe length L_p, the probe width W_p and the backshort distance L_{BS} are determined. Both L_p and L_{BS} can be used as tuning elements to obtain small variations in both the real and imaginary parts of the impedance [24, 25]. As mentioned in Section 2.4.2, an initial estimate for the probe length is selected as approximately a quarter effective wavelength, $\lambda_{eff}/4$, in accordance with the analogy of a monopole radiating into a waveguide. The backshort distance is estimated as a quarter guided wavelength $\lambda_g/4$, since the short circuit boundary conditions places the maximum electric field at this distance, described in Section 2.4.2.

For a substrate height of $H_{sub} = 100\ \mu m$, a track width of $W_{track} = 98\ \mu m$ was selected to give a characteristic impedance of $Z_0 \simeq 50\ \Omega$ according to eq. (2.40). Using the corresponding effective permittivity $\varepsilon_{eff} \simeq 6.485$ from eq. (2.39), the initial probe length is obtained from the quarter wave relation, while the backshort distance follows from the guided wavelength of eq. (2.37):

$$L_p = \frac{\lambda_{eff}}{4} = \frac{c}{4f\sqrt{\varepsilon_{eff}}} \qquad L_{BS} = \frac{\lambda_g}{4} = \frac{\lambda_0}{4\sqrt{1 - \left(\frac{f_c}{f}\right)^2}}. \tag{3.3}$$

The resulting quarter-wavelength values are summarized in Table 3.2. These values are only first estimates, since the actual resonance depends on the complete geometry including the backshort distance, probe width, substrate, waveguide geometry and channel size. Therefore, parametric sweeps in HFSS were used to refine the estimated dimensions. The initial estimates were used as a starting point for a coarse sweep with relatively large step sizes to identify promising regions. The ranges were then narrowed and swept with finer step sizes, presented in Figure 3.5-3.7. The figures show the input reflection coefficient S_{11} over the $50 - 60$ GHz band, where each curve corresponds to one value of swept parameters.

Table 3.2: Initial quarter-wavelength values for probe and backshort lengths.

Frequency	$L_p = \lambda_{eff}/4$ (mm)	$L_{BS} = \lambda_g/4$ (mm)
50 GHz	0.59	2.48
60 GHz	0.42	1.68

Figure 3.5, shows the parametric sweep of the backshort distance L_{BS} from 1.45 mm to 1.95 mm with a step size of 0.1 mm. Each curve traces the impedance across the band, such as a shorter curve or arc means less variation over frequency. For the backshort case, when the length L_{BS} increases, the capacitive behavior increases and the impedance over frequency shifts. This is observed in the smith chart as a downwards shift. It can also be seen that the impedance variation over frequency is minimized at $L_{BS} = 1.55$ mm (light green curve).

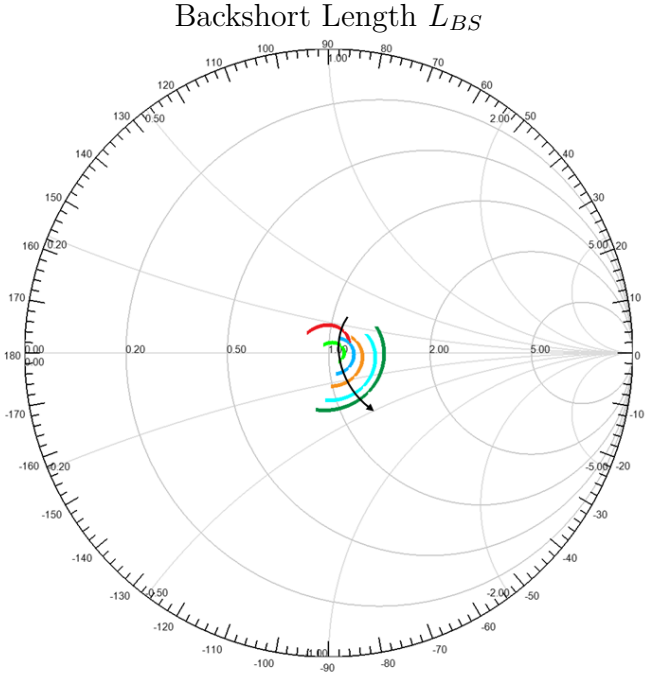


Figure 3.5: Parametric sweep of the backshort distance (L_{BS}). Arrow indicates increasing length.

Figure 3.6, shows the parametric sweep of the probe length L_p from 500 μm to 800 μm with a step size of 20 μm. As the length increases, in contrast to the backshort length, increasing the probe length increases the capacitance and there is also a change in impedance variation over frequency. The lowest impedance variation is for $L_P = 740$ μm (inner gray curve). Figure 3.7, shows the parametric sweep of the probe width W_P from 400 μm to 650 μm with a step size of 50 μm. Increasing the width moves it mostly to lower impedance with a small shift towards more capacitive. In contrast to the backshort length and the probe length, almost no change to the variation of impedance over frequency can be seen. Therefore no value is preferred in terms of impedance variation over frequency. Selected values from these simulations are summarized in Table 3.3.

Table 3.3: Selected values for backshort length, probe length and probe width.

Parameter	Backshort (mm)	Probe Length (μm)	Probe Width (μm)
Value	1.55	740	650

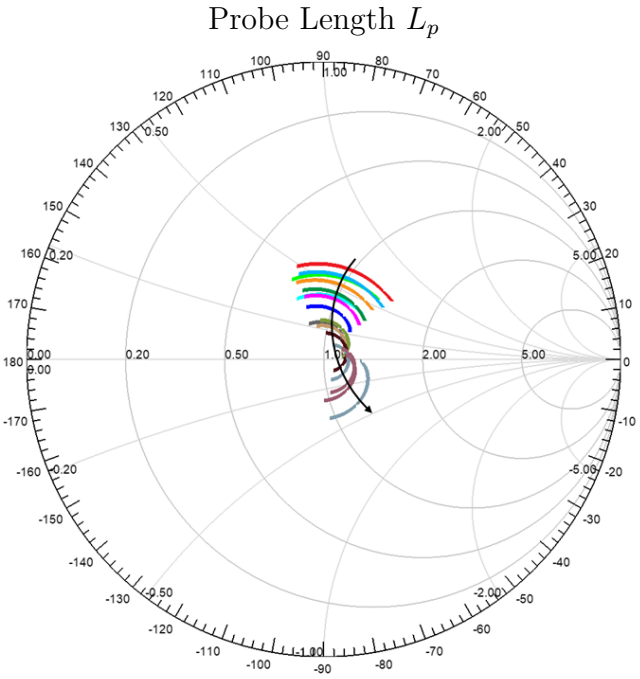


Figure 3.6: Parametric sweep of the probe length (L_p). Arrow indicates increasing length.

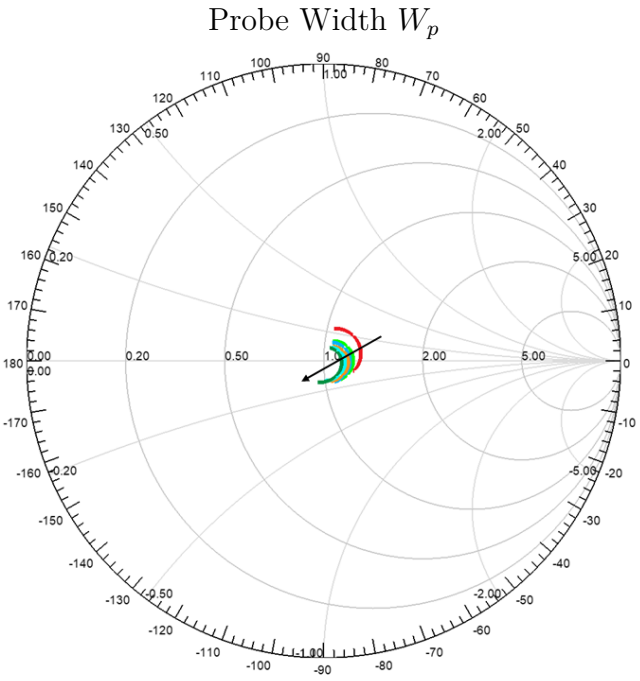


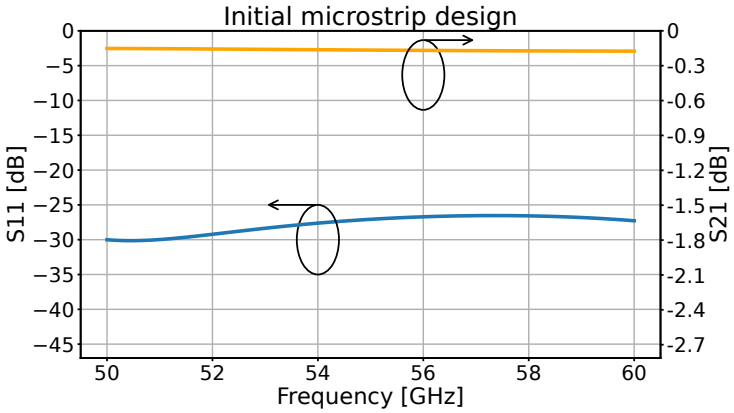
Figure 3.7: Parametric sweep of the probe width (W_p). Arrow indicates increasing width.

3.1.2.4 Initial microstrip probe design results

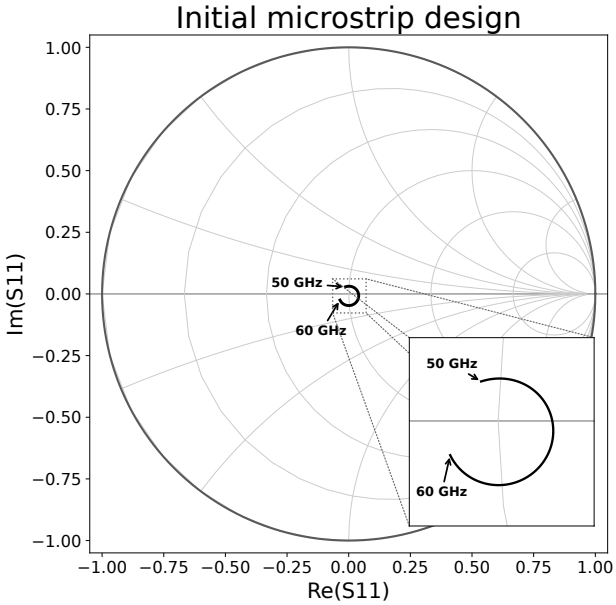
The initial probe design was used to select L_p, W_p and L_{BS} with small impedance variation over frequency. The results are used as a starting point for the next section, where the integration with SiGe MMIC is considered by implementing a CPWG interface and bondwire connections to the MMIC. The obtained dimensions are summarized in Table 3.4. The geometry is shown in Figure 3.3, the simulated S-parameters and impedance variation for the microstrip design are shown in Figure 3.8a and Figure 3.8b.

Table 3.4: Selected starting parameters for the initial probe design.

W_{track}	W_c	H_c	L_{sub}	L_{BS}	L_p	W_p	H_{sub}
98 μm	750 μm	500 μm	$\simeq$ 3 mm	1.55 mm	740 μm	650 μm	100 μm



(a) Return loss S_{11} and insertion loss S_{21}.



(b) Input reflection coefficient $S_{11} = \Gamma_{in}$.

Figure 3.8: Simulated performance of the initial microstrip probe design over $50 - 60$ GHz.

3.1.3 Interface to SiGe MMIC

The previously presented microstrip-based design is used as a initial starting point for the probe width W_p and length L_p, as well as for selecting the channel dimensions and backshort length. However, this design is not suitable for the final implementation due to the grounding constraints of the MMIC. The MMIC is fabricated in SiGe technology and does not include a backside metalized ground plane. In contrast to GaAs, InP, or GaN MMICs, where RF grounding is provided through the backside metal with the split-block housing, the SiGe routes the grounding in different metal layers and there is no backside ground which could be connected to the split-block alumina housing. As a result, the RF interface between the probe and the MMIC must provide the ground on the topside metallization to the Ground-Signal-Ground (GSG) pads on the MMIC die. Therefore, the ground reference must be transferred from the probe substrate to the MMIC pads using bondwires.

3.1.3.1 CPWG interface design

One approach, as in [29], is to realize the transition as a CPWG structure over most of its length, while only the probe tip extends beyond the ground planes into the waveguide cavity. In this work, a full length CPWG implementation was not implemented but instead only a short CPWG section was introduced close to the MMIC interface. The benefit of this approach is that it provides the required coplanar grounding at the MMIC side and the short CPWG section introduces two extra tuning parameters, the CPWG length L_{CPWG} and the fillet radius R_{fillet}, which can be used to improve the matching.

As mentioned, the interface between the transition and MMIC needs to be coplanar and therefore Chemandy Electronics coplanar waveguide with ground calculator was used in order to estimate initial values for the structure [30]. By using the calculator, the track width $W_{track} = 74\ \mu m$, gap width $G_{track} = 56\ \mu m$ and with the predetermined substrate thickness $H_{sub} = 100\ \mu m$ was selected, see Figure 3.9. For the initial coplanar design the width of the coplanar ground is then the remaining substrate width

$$W_{CPWG} = \frac{W_{sub}}{2} - \frac{W_{track}}{2} - G_{track} = \frac{700\ \mu m}{2} - \frac{74\ \mu m}{2} - 56\ \mu m = 257\ \mu m. \quad (3.4)$$

The calculator result suggests a characteristic impedance of 50.54 Ω with an effective dielectric constant $\varepsilon_{eff} = 5.762$.

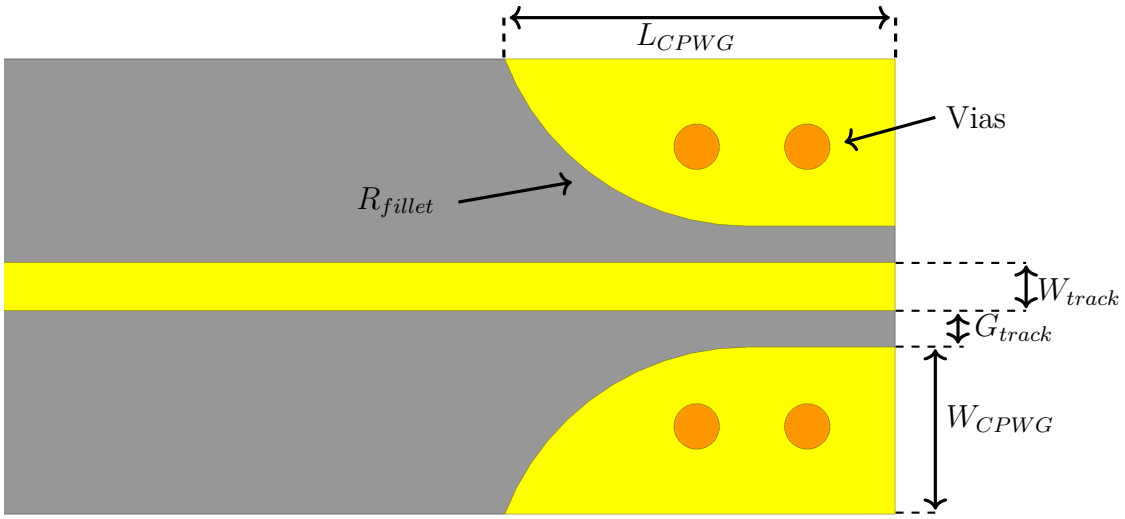


Figure 3.9: Parameters of the CPWG interface: L_{CPWG}, W_{CPWG}, G_{track}, W_{track} and R_{fillet}.

Figure 3.10, shows the simulation result of the calculated parameters using the online calculator. The simulation result closely resembles the estimate provided by the calculator. The impedance shown in Figure 3.10 is the port impedance at the CPWG interface from HFSS simulation.

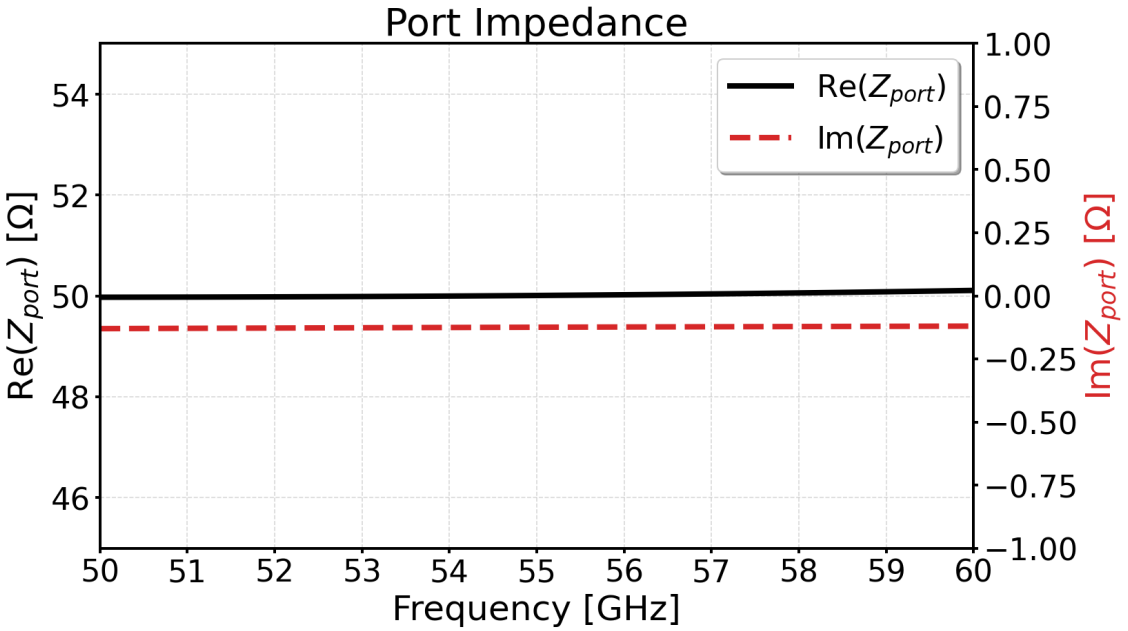


Figure 3.10: Simulated characteristic impedance at CPWG port interface for the probe structure with CPWG interface.

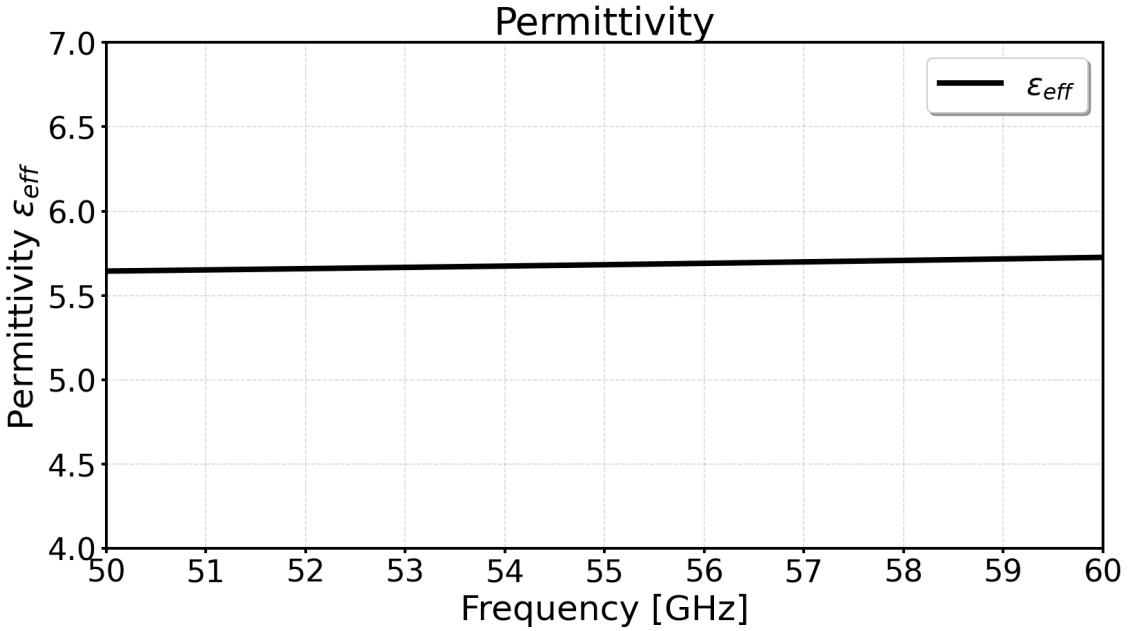


Figure 3.11: Simulated effective permittivity at CPWG port interface for the probe structure with CPWG interface.

A comparison between the calculator estimate and the HFSS result is shown in Table 3.5.

Table 3.5: Comparison between initial CPWG calculator estimates and HFSS port result at the implemented CPWG interface.

Parameter	Calculator [30]	Simulation at 50 GHz	Simulation at 60 GHz
Z_0 (Ω)	50.54	$50.2596 - j0.1284$	$50.3955 - j0.1187$
ε_{eff}	5.762	5.6848	5.7650

The HFSS result agrees well with the Chemandy Electronics CPWG calculator estimate, indicating that the selected CPWG dimensions provide an appropriate starting point for the interface design.

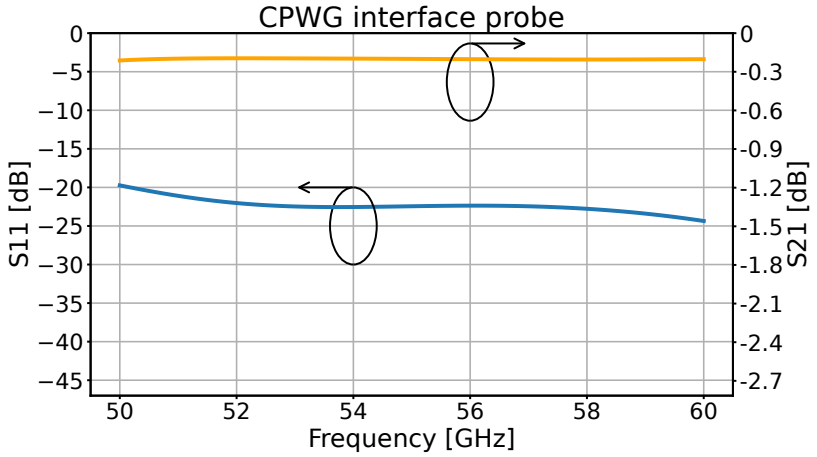
3.1.3.2 CPWG interface probe design results

At this stage, the design has changed from a microstrip based to a more complex with CPWG interface. Simulations of the structure using previously obtained and new parameters shown in Table 3.6, gives the following S-parameters and impedance matching, see Figure 3.12a and Figure 3.12b.

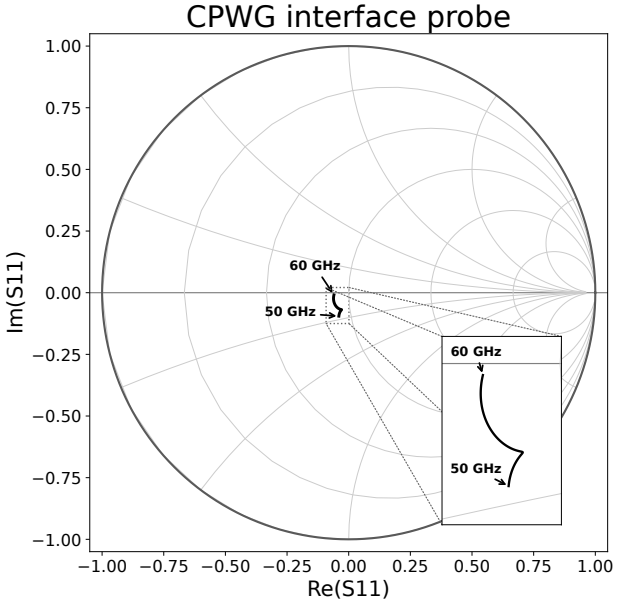
Table 3.6: Parameters for the CPWG interface design.

W_{track}	W_c	H_c	L_{sub}	L_{BS}	L_p	W_p	H_{sub}
98 μm	750 μm	500 μm	$\simeq 3$ mm	1.55 mm	740 μm	650 μm	100 μm

W_{track}	G_{track}	W_{CPWG}	L_{CPWG}	R_{fillet}
74 μm	56 μm	257 μm	600 μm	400 μm



(a) Return loss S_{11} and insertion loss S_{21}.



(b) Input reflection coefficient $S_{11} = \Gamma_{in}$.

Figure 3.12: Simulated performance of the CPWG interface probe design over $50 - 60$ GHz.

3.1.3.3 Channel cutoff and attenuation

At this stage, two estimates of the effective permittivity have been obtained, $\varepsilon_{eff,1} \simeq 5.762$ from the CPWG port simulation and $\varepsilon_{eff,2} \simeq 6.485$ from eq.(2.39). It should be noted that neither of these values represents the complete channel permittivity. The value obtained from the simulations describes the local permittivity for the CPWG interface at the port, while the other value represents the section further into the channel towards the probe, which resembles a microstrip structure, see Figure 3.9. Therefore, the actual effective permittivity in the channel is expected to lie between these two estimates. In Section 3.1.2.2, the channel cavity was dimensioned such that it operates below cutoff under worst case assumptions. Using the obtained effective permittivities, a improved estimate of both the cutoff frequency and channel attenuation can be made. The cutoff frequency of the dominant TE_{10} mode in the channel is given by

$$f_{c,10} = \frac{c}{2W_c \cdot \sqrt{\varepsilon_{eff}}} = \begin{cases} 83.3 \text{ GHz}, & \varepsilon_{eff,1} = 5.762, \\ 78.5 \text{ GHz}, & \varepsilon_{eff,2} = 6.485. \end{cases} \tag{3.5}$$

which is well above the intended frequency band. Below the cutoff frequency, the attenuation of the field for a given frequency can be calculated by using eq. (2.31, 2.32, 2.33). Thus, for a channel length $z \simeq 2\ mm$ and using

$$\alpha = \sqrt{k_c^2 - k^2}, \qquad k_c = \frac{\pi}{a}, \qquad k = \frac{2\pi f}{c} \cdot \sqrt{\varepsilon_{eff}} \tag{3.6}$$

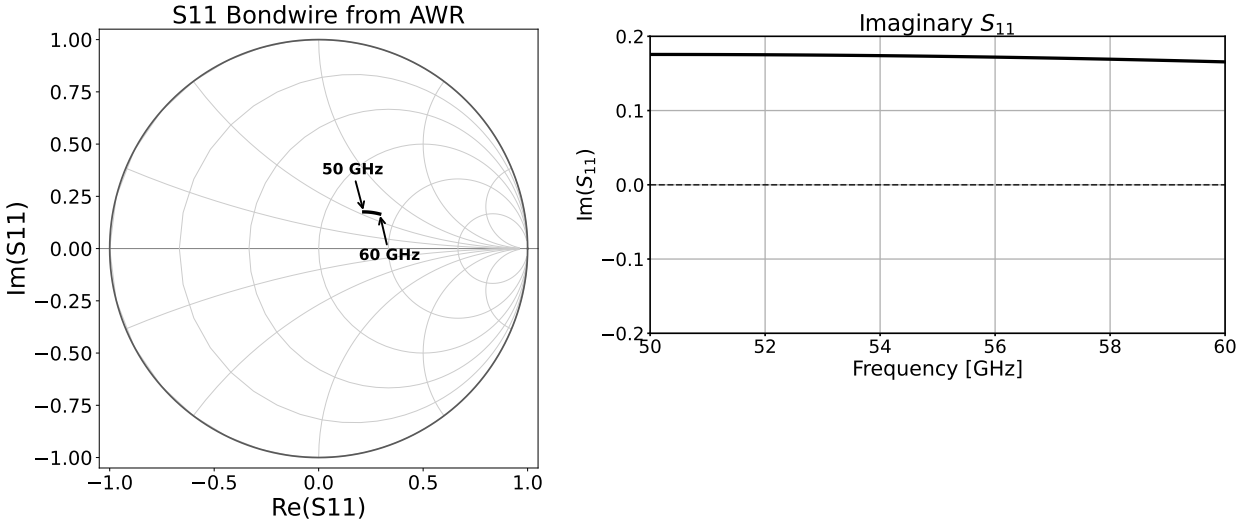
where $a = 750\ \mu m$, the attenuation in dB is then

$$A_{dB}(z) = 8.686\alpha z = \begin{cases} 58.2 \text{ dB}, & f = 50 \text{ GHz}, \ \varepsilon_{eff,1} = 5.762, \\ 50.5 \text{ dB}, & f = 60 \text{ GHz}, \ \varepsilon_{eff,1} = 5.762, \\ 56.1 \text{ dB}, & f = 50 \text{ GHz}, \ \varepsilon_{eff,2} = 6.485, \\ 46.9 \text{ dB}, & f = 60 \text{ GHz}, \ \varepsilon_{eff,2} = 6.485. \end{cases} \tag{3.7}$$

The calculated attenuation demonstrates that the channel operates below the cutoff frequency and the field attenuation exceeds 45 dB for the intended frequency band. This indicates that parasitic waveguide modes excited inside the channel decay rapidly.

3.1.3.4 Bondwire transition to MMIC

The bondwire connection between the MMIC pad and the transition line was modeled using a lumped π equivalent network, such as in [31]. The model consists of a series resistance and series inductance. In addition, shunt capacitances are added for each pad. The series inductance is primarily determined by the length and loop height of the bondwire while the shunt capacitances are included in order to model the parasitics of the pads. The lumped model was implemented in Cadence AWR using a 150 μm bondwire length. From an EM perspective the length should be as short as possible to minimize the series inductance, but 150 μm was selected as a realistically achievable length for the bonding process. The model shows that the bondwire introduces inductance, which can be seen in Figure 3.13.



(a) (b)

Figure 3.13: Simulation results of the lumped π equivalent bondwire network implemented in Cadence AWR for a bondwire spacing of 150 μm. (a) Smith chart showing the inductive shift introduced by the bondwire. (b) Imaginary part of S_{11} illustrating the added inductive contribution

In order to simulate the parasitic effect introduced by the bondwires, a landing CPWG structure was added in the simulation model. Figure 3.14 shows the geometry for the setup. The 50 Ω structure was used to represent the MMIC die. A more realistic implementation would require metallization stackup information, however since the MMIC stackup was not available, a simple CPWG structure was implemented instead. The bondwires are created in HFSS by making a structure resembling the reality as close as possible. In an EM design perspective it is preferably for the bondwires to be as short and straight as possible, interfacing between the transition and the MMIC. However, in reality the bondwires cannot be a straight line from point A to point B arbitrary. The bonding machine has limitations and therefore a model was created in HFSS to resemble the actual bondwires to simulate more representative of reality.

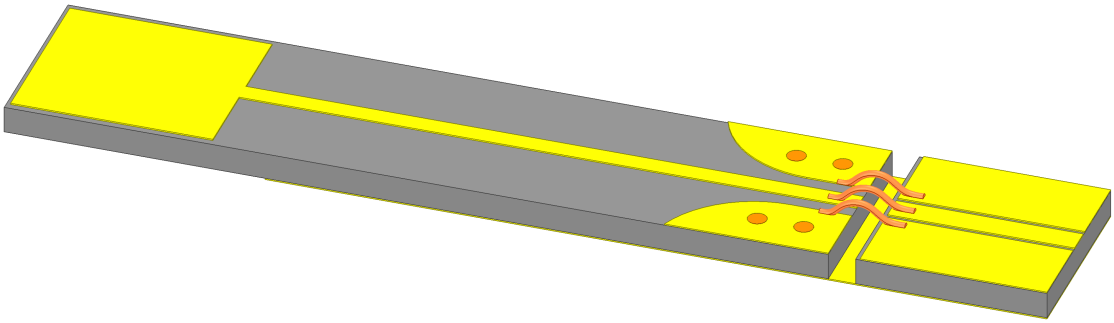


Figure 3.14: Simulation setup for bondwires using a 50 Ω CPWG landing structure to emulate the MMIC.

Figure 3.15 shows simulated S_{11} for standalone probe with CPWG interface and with bondwires plus the emulated MMIC CPWG structure from 50 to 60 GHz. The inclusion of the bondwires shifts the impedance shown in the Smith chart.

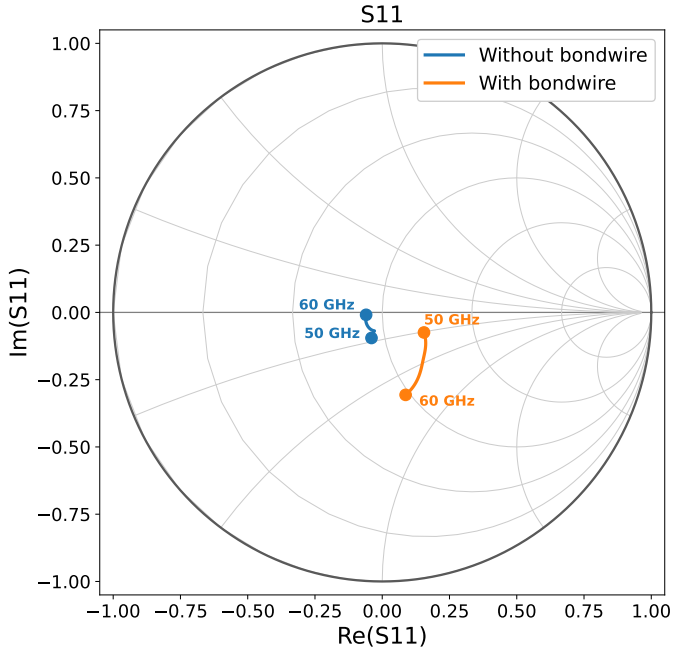


Figure 3.15: Simulation result of input reflection coefficient $S_{11} = \Gamma_{in}$ for with and without bondwires from 50 GHz to 60 GHz.

To further analyze the behavior, the input impedance was calculated as

$$Im(Z_{in}) = Im(50 \cdot \frac{1 + S_{11}}{1 - S_{11}}) \tag{3.8}$$

and is shown in Figure 3.16. The result indicates that the addition of the bondwires and emulated the MMIC substrate changes the reactive component significantly.

In contrast to the π model in AWR, the impedance does not move inductively for the full frequency range but instead the response suggests additional capacitance from 50 to 60 GHz. A possible explanation for the difference between the AWR and HFSS results is that the HFSS model includes additional parasitic capacitance that are not captured in the AWR model. In HFSS both the CPWG landing structure on the emulated MMIC side and the probe substrate CPWG interface contribute to the capacitance. In addition, there is also capacitive coupling between the probe substrate and the emulated MMIC substrate across the gap. Therefore, even though the bondwires introduce inductance, the total response in HFSS can still appear to add more capacitive over the band. Although the Smith chart in Figure 3.15 could be interpreted as a clockwise rotation caused by the series inductance, this is not believed to be the case, since the imaginary part of the input impedance in Figure 3.16 is more negative with the bondwires than without, indicating a more capacitive rather than inductive net reactance.

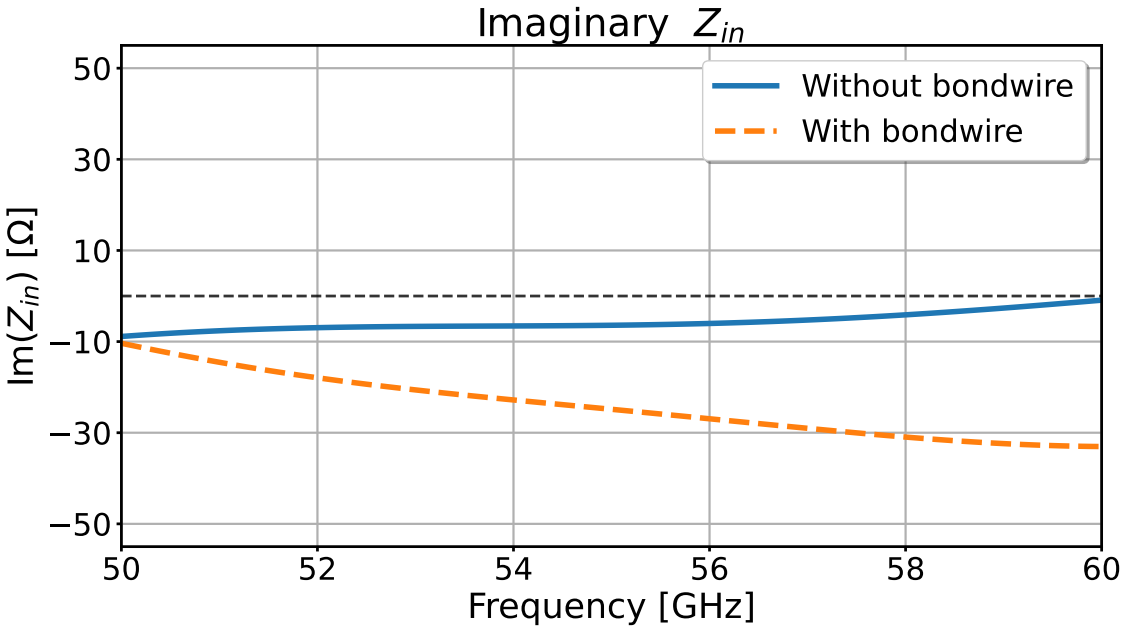


Figure 3.16: Simulation result for with and without bondwires from $50 - 60$ GHz.

Numerous simulations were conducted in order to compensate the impedance shift by varying previously mentioned parameters such as the probe width and the CPWG interface. Although several sweeps of the already defined parameters were evaluated, no sufficiently broadband match was obtained. To address this, additional parametrization is introduced in the next chapter, by adding additional impedance transforming sections.

3.1.4 Multi-stage Impedance Transformer

As previously mentioned, the design concept was inspired by [24] as a general concept, but was adapted to this work packaging constraints. The main difference is the added CPWG section at the MMIC interface in order to provide the interface to the GSG pads on the MMIC through bondwires.

The transition can be divided into four sections, each section is defined by a set of geometric parameters that are used for matching, shown in Figure 3.17.

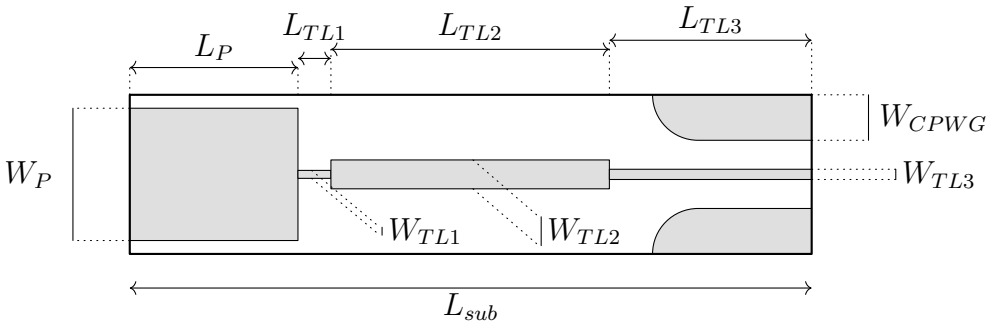


Figure 3.17: Multi-stage impedance transform parametrization.

1. **Section 1: Probe.** The substrate is inserted into the waveguide cavity, in this section the bottom ground plane is removed to enable coupling from the dominant TE_{10} mode to quasi-TEM. The probe is parameterized by the width W_P and length L_P.

2. **Section 2: High-impedance line.** Immediately after the probe, a short narrow high impedance microstrip section is used in order to transform the impedance by tuning the reactance. This transmission TL_1 line is parameterized by width W_{TL1} and length L_{TL1}.

3. **Section 3: Low-Impedance line.** A wider microstrip section is then introduced in order to further change the impedance. The lower impedance line TL_2 is parameterized by width width W_{TL2} and length L_{TL2}.

4. **Section 4: Microstrip to CPWG.** The microstrip line is transitioned into a CPWG in order to provide grounding to the topside for the MMIC GSG interface. The CPWG section is parametrized with the line width and length W_{TL3} and L_{TL3} respectively. Additionally, due to manufacturing limitations for the vias, there is a minimum width for the CPWG section W_{CPWG} and the gap is varied purely by the width of the transmission line and CPWG section.

Additionally, from the manufacturer design rules of the ceramic Alumina substrate, the minimum via diameter for the selected substrate thickness ($H_{sub} = 100\ \mu m$) is 70 μm, minimum via ring width is 50 μm and the minimum distance between the via ring and substrate edge is equal to the substrate thickness, thus 100 μm. In practice, this results in a minimum $W_{CPWG,min}$:

$$W_{CPWG,min} \geq 70\ \mu m + 50\ \mu m + 100\ \mu m = 220\ \mu m. \tag{3.9}$$

By assuming that the bondwires are straight between the CPWG interface and the MMIC introduces another geometric constraint on W_{CPWG}. The spacing from the center of the middle RF pad to the outer edges of the grounding pads is 87 μm and the bondwires diameter are 25 μm, the minimum allowed distance from the center of the middle RF conductor to the closest edge of the CPWG:

$$d_{max} = 87\ \mu m - 25\ \mu m = 62 \mu m. \tag{3.10}$$

Since the total substrate width is fixed at 700 μm, the minimum allowed $W_{CPWG,min}$ is obtained by

$$W_{CPWG,min} \geq \frac{W_{sub}}{2} - d_{max} = 350\ \mu m - 62\ \mu m = 288\ \mu m. \tag{3.11}$$

In practice, the bondwires do not have to be perfectly straight and can be placed with a angle. This relaxes the second constraint imposed by the MMIC pad spacing. Therefore, narrower values of W_{CPWG} were also allowed during the optimization.

Prior to running optimization for the multi-stage impedance transformer probe, a fixed 15 μm metal to edge pullback was included at the probe, shown in Figure 3.18 below. These edges are critical for the RF performance and a metal extending to the end of the substrate is difficult to manufacture. Therefore, the pullback relaxes the manufacturing constraints. The edge offset was kept constant throughout remaining simulations for consistency.

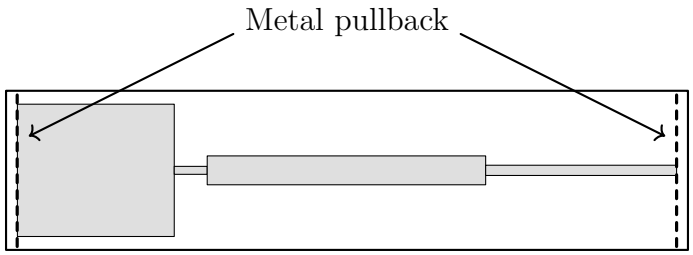


Figure 3.18: Metal-to-edge pullback of 15 μm at both edges.

3.1.4.1 Optimizing the Multi-stage Impedance Transformer

To find a solution for the impedance transformation, the built-in optimization tool in HFSS was used. First, a global search was performed by using Genetic Algorithm (random search) to broadly search for promising candidates. When a candidate is identified from the search it was refined using a Quasi-Newton (gradient) optimizer. Additionally, several starting points were also evaluated to reduce the risk of converging to a suboptimal minimum.

The optimization objective was to obtain a broadband impedance match over the target frequency range $50-60$ GHz. Meaning, that the optimizer searches for candidates that have the lowest return loss (S_{11}) within specified band. The optimization of the multistage impedance transformer resulted in several designs with improved performance in comparison to the previous design. Among these, two candidates were selected based on their performance. Since the optimizer returns continuous-valued parameters, the obtained dimensions are sub-micrometer precision and not suitable for manufacturing. Therefore, the dimensions were rounded to nearest micrometer integer and re-simulated to verify their performance. Additionally, a local parametric sweep was performed using neighboring values for each parameter to ensure the best combination was selected using micrometer integers. Table 3.7 summarizes the geometrical parameters for the two selected designs. Figure 3.19 compares their return losses and Figure 3.20 shows the impedance matching behavior. The frequency sweep was extended to $40-75\ GHz$ to visualize behaviors outside the targeted design band and to define the $-10\ dB$ bandwidth denoted as BW_{-10dB}.

Table 3.7: Geometrical parameters for the two design candidates.

Candidate	L_p [μm]	W_p [μm]	W_{TL1} [μm]	L_{TL1} [μm]	W_{TL2} [μm]	L_{TL2} [μm]	W_{TL3} [μm]	W_{CPWG} [μm]
1	740	553	29	126	136	1170	31	282
2	740	581	35	145	128	1225	44	288

Candidate	max(S_{11}) (50–60 GHz) [dB]	$\text{BW}_{-10_{\text{dB}}}$ [GHz] (center)
1	-26.46	24.30 (57.55)
2	-26.90	25.00 (56.70)

Table 3.8: Comparison of performance for the two optimized candidates. max(S_{11}) denotes the highest return loss value within the target frequency band ($50-60$ GHz. The bandwidth is defined at -10 dB, with the corresponding center frequency given in parentheses.

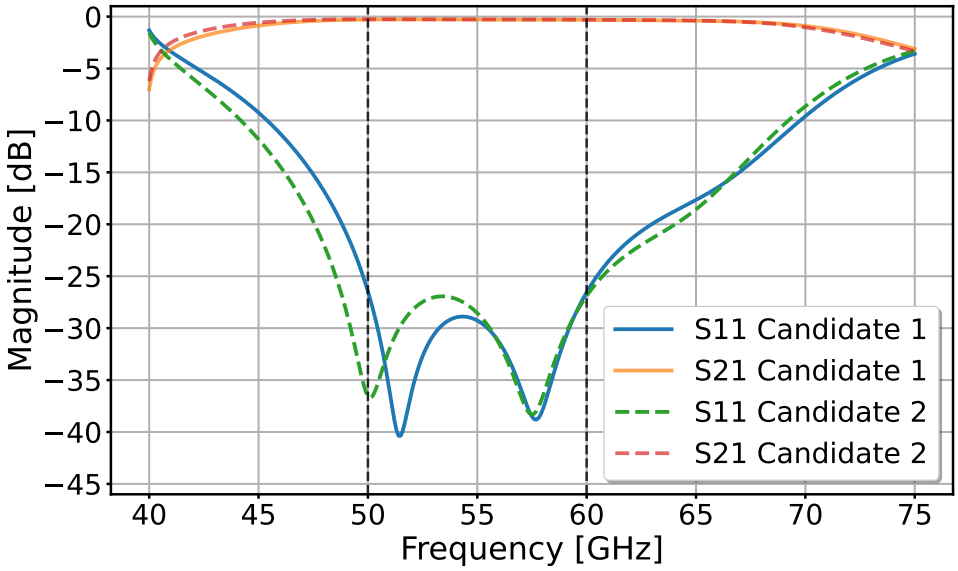


Figure 3.19: Comparison of the two candidates, return loss S_{11} and insertion loss S_{21}. Candidate 1 is shown with solid lines and candidate 2 with dashed lines. Extended frequency band for visualization with targeted frequency within dashed lines.

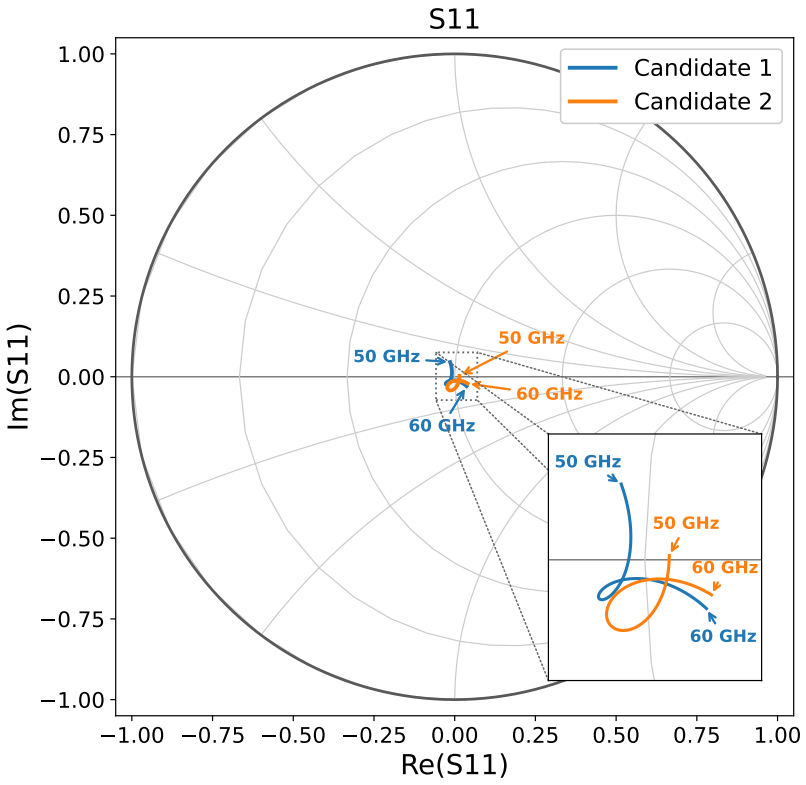


Figure 3.20: Smith chart comparison of the input reflection coefficient, $S_{11} = \Gamma_{in}$ for the two candidates. Candidate 1 is represented by blue line and candidate 2 with orange line.

3.1.4.2 Sensitivity analysis to dimensional and bondwire placement variations.

To evaluate the robustness of the designs, analysis of small variations from manufacturing and assembly was performed. All transmission line widths, including the probe were varied by $\pm 3\ \mu m$ according to manufacturing tolerance. The return loss was evaluated within the targeted band $50 - 60$ GHz, while the simulations were plotted over an extended frequency range $40 - 75$ GHz. The extended range was included to visualize and identify variations close to the targeted band and to determine the -10 dB bandwidth.

In addition to dimensional tolerances of the transmission line, variations to the positioning of the ground bondwires were evaluated. The bondwires were initially simulated as aligned with the propagation direction and could be placed exactly at the edge of the CPWG conductor. In practice, small misalignment during the bonding process are expected. To account for this, rotations of the ground bondwires from 0° to 10° were introduced to evaluate the robustness against bondwire placement errors. The resulting S_{11} variations are shown in Figure 3.21 and summarized in Table 3.9.

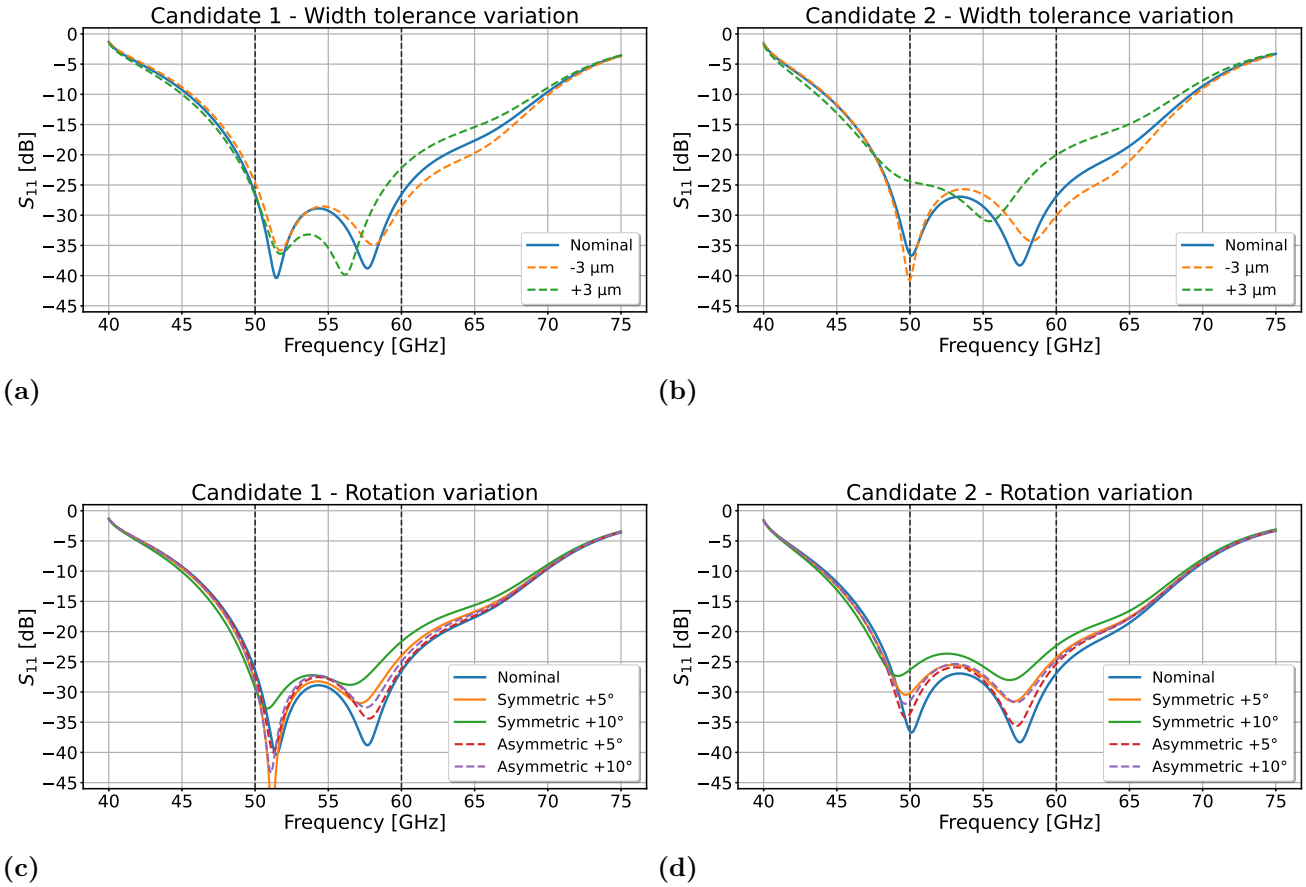


Figure 3.21: S_{11} robustness analysis over 40-75 GHz. (a,b) $\pm 3\ \mu m$ transmission line width variation for Candidates 1 and 2. (c,d) Symmetric and asymmetric bondwire rotation for Candidates 1 and 2.

Table 3.9: Robustness analysis of transmission line width variation and ground bondwire rotation.

(a) $\pm 3\,\mu$m Transmission Line Width Variation

Candidate	Variation	max(S_{11}) [dB] (50–60 GHz)	BW$_{-10\text{dB}}$ [GHz] (f_c)
1	Nominal	−26.46 @ 50.00	24.30 (57.55)
	$-3\,\mu$m	−24.62 @ 50.00	24.30 (57.85)
	$+3\,\mu$m	−22.19 @ 60.00	24.10 (57.15)
2	Nominal	−26.90 @ 60.00	25.00 (56.70)
	$-3\,\mu$m	−25.69 @ 53.60	25.20 (56.90)
	$+3\,\mu$m	−20.04 @ 60.00	24.70 (56.05)

(b) Ground Bondwire Rotation

Candidate	Rotation	max(S_{11}) [dB] (50–60 GHz)	BW$_{-10\text{dB}}$ [GHz] (f_c)
1	Nominal	−26.46 @ 50.00	24.30 (57.55)
	Symmetric +5°	−23.98 @ 60.00	24.20 (57.40)
	Symmetric +10°	−21.65 @ 60.00	24.30 (57.15)
	Asymmetric +5°	−26.10 @ 60.00	24.30 (57.55)
	Asymmetric +10°	−24.98 @ 60.00	24.20 (57.50)
2	Nominal	−26.90 @ 60.00	25.00 (56.70)
	Symmetric +5°	−24.28 @ 60.00	25.00 (56.50)
	Symmetric +10°	−22.34 @ 60.00	24.90 (56.25)
	Asymmetric +5°	−25.35 @ 60.00	25.00 (56.60)
	Asymmetric +10°	−24.74 @ 60.00	24.90 (56.55)

Candidate 1 performs slightly better for the +3 μm width variation and the asymmetric bondwire rotations. Candidate 2 performs better for the nominal case, the −3 μm width variation, the symmetric bondwire rotations and also provides a slightly larger −10 dB bandwidth. Overall, the difference between the two candidates is very small since $S_{11} < -20$ dB for both candidates within the targeted band for all variations.

3.1.4.3 Final design selection

Regarding the multi-stage impedance transformer, the length of TL_2 was not fixed to a quarter wavelength as in [24]. Instead, it was treated as an optimization parameter, allowing the optimizer to select the length that provided the best broadband match over the target band. Therefore, TL_2 was not implemented as a conventional quarter wave transformer. A likely explanation is that the optimizer favors a length deviating from a conventional quarter wave transformer due to the reactive part of the impedances being matched, where a non-quarter wave appears to provide a better broadband match.

Based on the robustness analysis in Table 3.9, both candidates show similar RF performance. Candidate 2 was therefore selected primarily due to practical implementation considerations. In particular, the width of W_{TL3} is 44 μm for Candidate 2 compared to 31 μm for Candidate 1. The wider transmission line gives a larger bondwire landing area, which is important during assembly and reduces the sensitivity to bondwire placement inaccuracies.

The simulated S-parameter performance of the selected design is shown in Figure 3.22. The result indicates a return loss of $S_{11} < -26.9$ dB over the targeted band $50 - 60$ GHz. The corresponding impedance behavior over the same band is shown in Figure 3.20, denoted as Candidate 2.

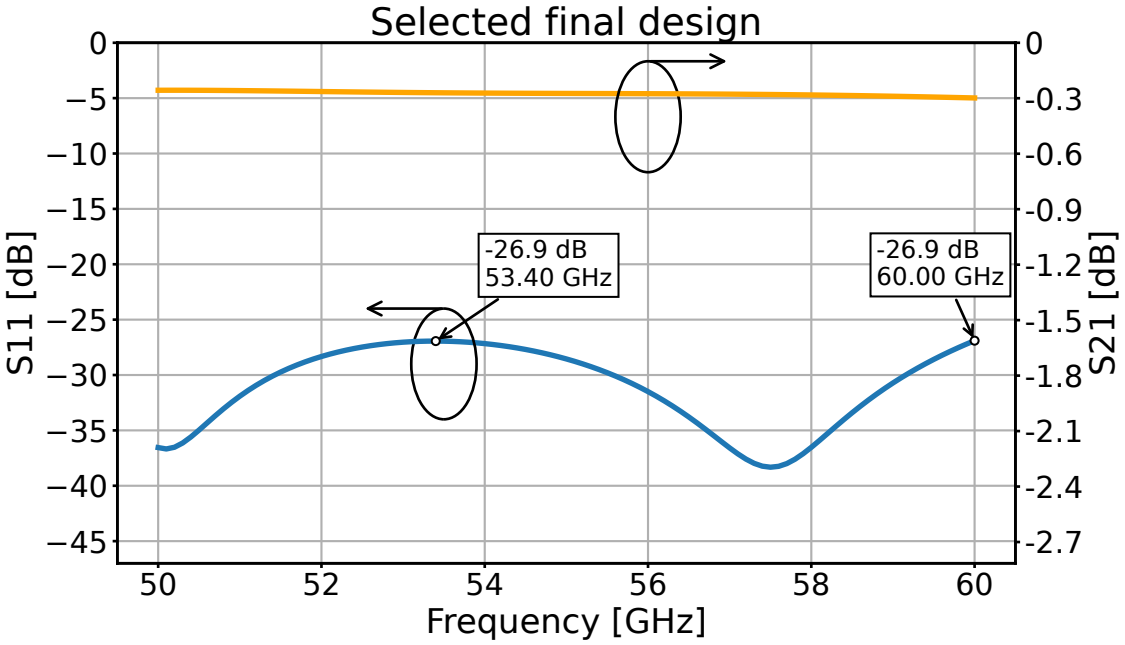


Figure 3.22: Simulated S-parameters of the selected final design over the $50 - 60$ GHz band.

3.1.4.4 DC coupling analysis

Since the biasing board is inside the enclosure and the cutout for the biasing board introduces an additional cavity. Incoming waves at the transition could couple and such coupling could excite parasitic modes inside the inner PCB cavity, which in turn could create standing waves and degrade the RF performance of the packaging. This is particularly relevant since the PCB traces and bondwires may act as unintended coupling elements inside the cavity and disturbances could couple to the DC biasing.

The implementation of these structures is described in Section 3.2. The purpose of these simulations was not to evaluate the DC functionality itself, but rather to investigate how much the RF signal couples to the bias board inside the PCB cavity.

In order to evaluate this effect a larger model was created including all cavities close to the transition core. Also including pads connected by bondwires from the MMIC to PCB substrate. A port was placed at the PCB pad to represent the DC connection, such that the coupled RF power from the waveguide transition into the bias board could be simulated. In addition to measuring the coupled signal, the electric field distribution inside the structure was also visually monitored in order to identify any standing wave fields inside the cavity. Figure 3.23 and Figure 3.24 represents the simulated model structure for the ACL and Switch packaging.

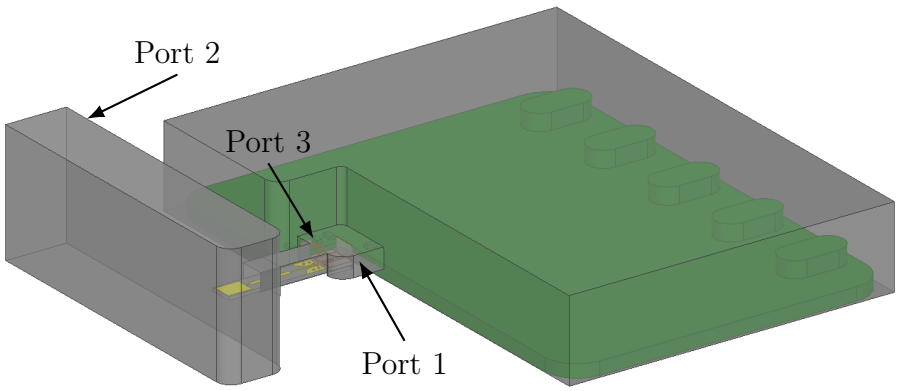


Figure 3.23: Simulation model for RF coupling to DC bias PCB from the ACL MMIC circuit, including PCB cavity, bondwires and ports at the DC pads.

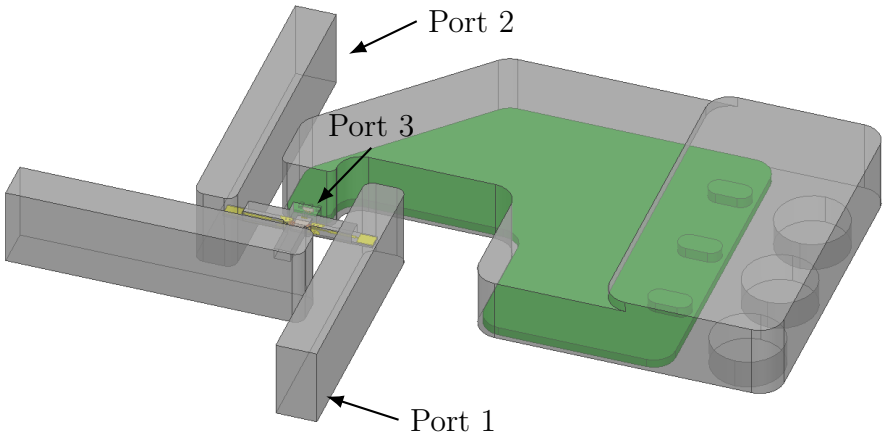
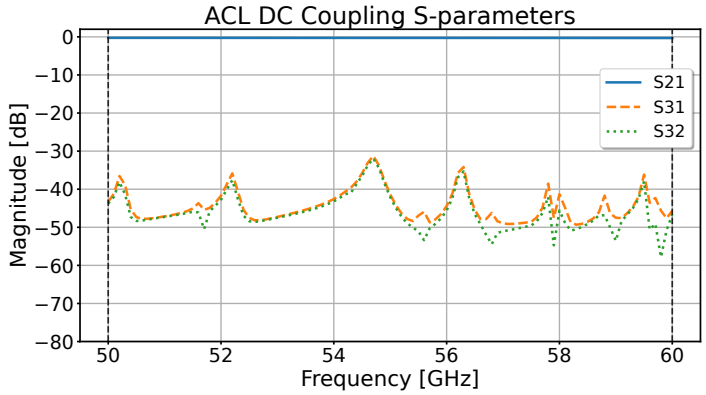
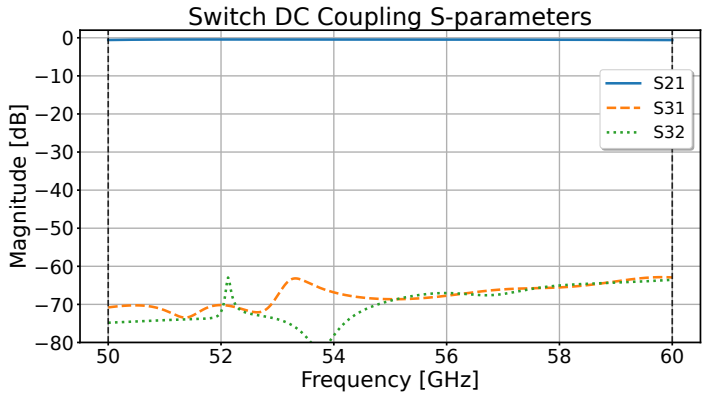


Figure 3.24: Simulation model for RF coupling to DC bias PCB from the Switch MMIC circuit, including PCB cavity, bondwires and ports at the DC pads.

The coupled RF power into the PCB cavity was quantified using S-parameters. Figure 3.25 show the simulated coupling from the ACL and Switch MMIC to the DC pads respectively.



(a) ACL DC coupling



(b) Switch DC coupling

Figure 3.25: Simulated RF coupling from the waveguide signal path to the DC PCB pads for the ACL and switch packages.

The simulations shown in Figure 3.25a and 3.25b suggest that the coupling is higher for the ACL package, approximately $S_{31} \simeq S_{32} \simeq -45$ dB. While in comparison, the switch package exhibits approximately $S_{31} \simeq S_{32} \simeq -70$ dB of coupling. Although the ACL package shows higher coupling, the level is still low and not expected to significantly degrade the RF performance.

The difference is likely related to the geometry of the cavities. For both cases, port 3 is perpendicular to the propagating wave. However, for the ACL package, the opening towards the DC PCB cavity extends further and wraps around to the direction of the propagating wave, see Figure 3.26. This creates a larger opening and may cause parasitic modes to resonate inside the DC cavity and degrade the RF performance.

The reasoning for the selected geometry was due to the initial uncertainty regarding which chip to be packaged. Initially, during simulation and design of the split-blocks there was still a uncertainty to use another ACL MMIC which would require five bias lines instead of two. Since the available space was limited, especially for placing single layer capacitors (SLCs), the additional opening was included to allow routing of the extra bias lines in that direction if needed. Lastly, if resonances are observed during measurements, RF absorbing materials, e.g. Eccosorb can be mounted inside the cavity to damp these parasitic modes.

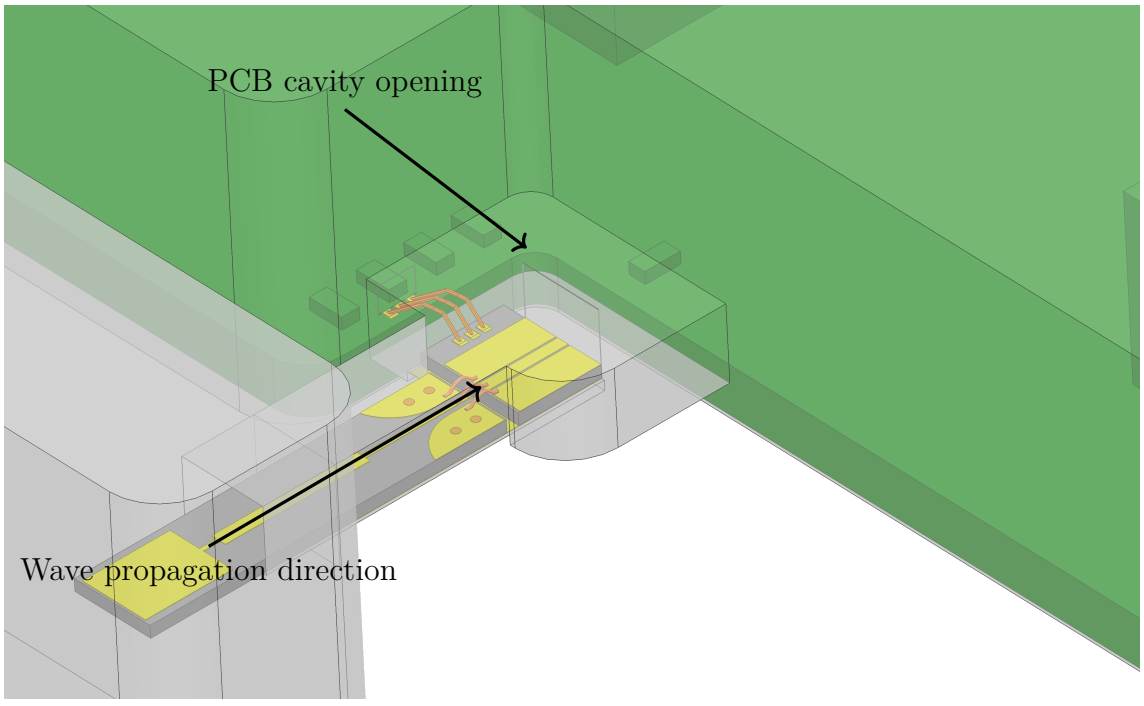
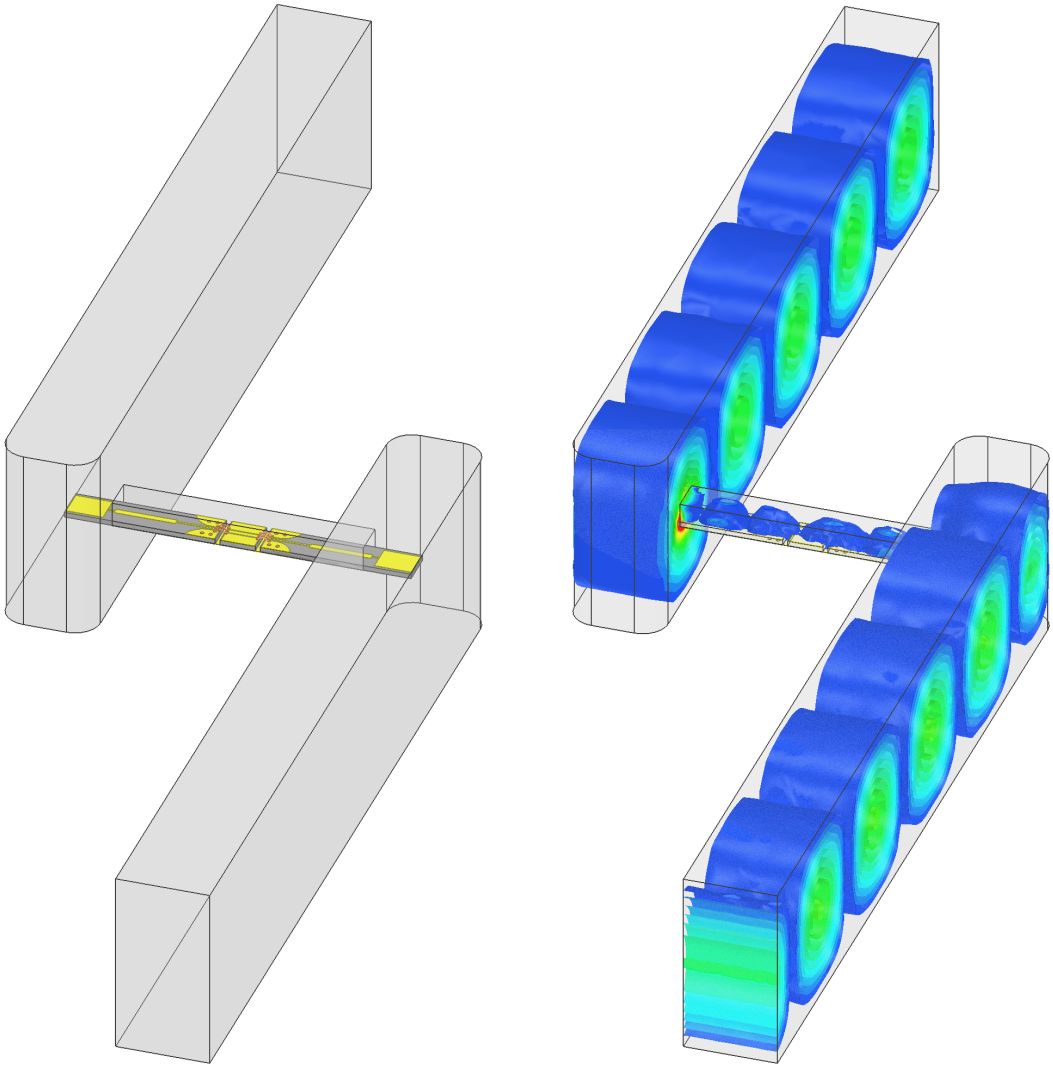


Figure 3.26: Figure showing the opening of PCB cavity for the ACL package and wave propagation direction.

3.1.4.5 Back to back performance analysis

The back-to-back (B2B) simulation was conducted in order to evaluate the performance of the transition itself. Since there will be no fabrication of a back-to-back structure, the validation of the simulated result will be conducted by de-embedding the on-chip measurement of the switch and measure a through path with the switch module, discussed in detail in Section 5.1.2. The simulated model of the B2B structure is shown in Figure 3.27a and the E-field distribution between the TE_{10} waveguide mode and planar mode is shown in Figure 3.27b.



(a) **(b)**

Figure 3.27: Back-to-back simulation structure. (a) HFSS model of the back-to-back transition. (b) Electric field distribution at 60 GHz, illustrating the coupling between the TE_{10} waveguide mode to planar and back.

The simulated performance of the B2B structure is presented in Figure 3.28, showcasing performance of $S_{11} < -17.8$ dB and $S_{21} > -0.6$ dB over the targeted $50 - 60$ GHz band, indicating good impedance matching and low transmission loss respectively.

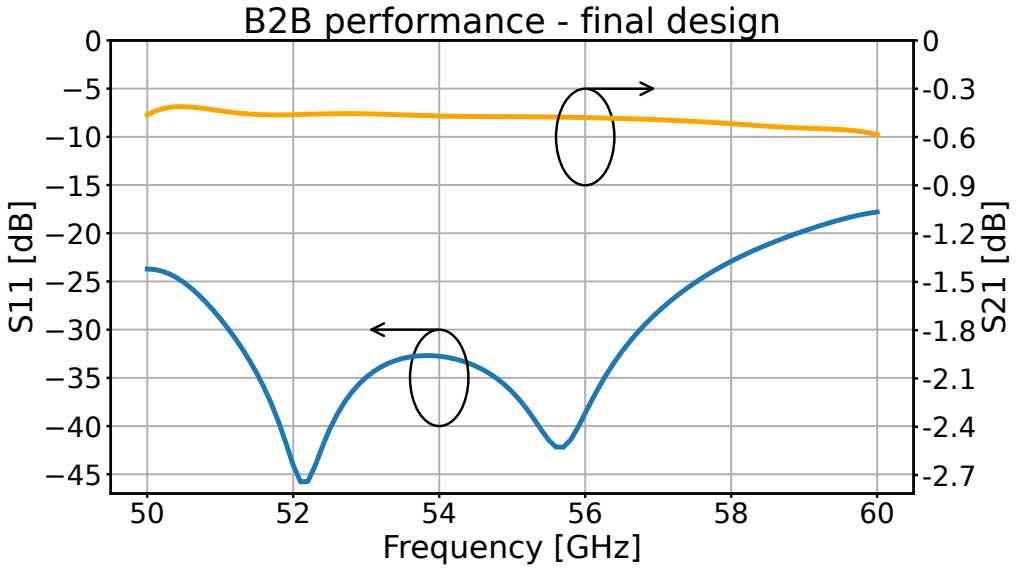


Figure 3.28: Simulated S-parameters of the back-to-back (B2B) structure over the frequency range.

3.2 Mechanical and biasing board Designs

The mechanical design of the split-blocks was carried out in collaboration with mechanical engineer, David Håkansson. The internal RF layout was designed by the author to ensure RF performance in accordance to the simulation results. This includes the placement of the waveguide transition, the MMIC cavity, the cavity for the bias PCB as well as the positioning of the bondwires and single layer capacitors used in the biasing network. The layout was developed in accordance to the RF performance and also accommodating practical assembly constraints such as bondwire lengths, component clearance for the PCBs and fabrication of the split-blocks.

The mechanical engineer was primarily responsible for the external mechanical structure. This includes the overall geometry, mechanical interface between the split-block halves, alignment features such as guiding pins, fastenings and machining tolerances required to ensure proper electrical performance and reliable assembly. In addition, the aluminum split-block will be gold plated after machining, which requires appropriate geometric compensation prior to fabrication to ensure correct final dimensions.
The overall module was therefore developed through a co-design process, where the mechanical and RF requirements were continuously evaluated together. The final design is therefore the result when taken into account both the EM and mechanical manufacturing considerations.

To give an overview of the mechanical assembly, an exploded view of the switch split-block is shown in Figure 3.29. The figure shows the parts of the module, including the waveguide ports, screws, guiding pins and flanging guide pins (dowels) used for alignment and fastening. Since the ACL and the switch module follow the same overall assembly technique, only the switch module is shown. A detailed description of the design choices is presented in the following section.

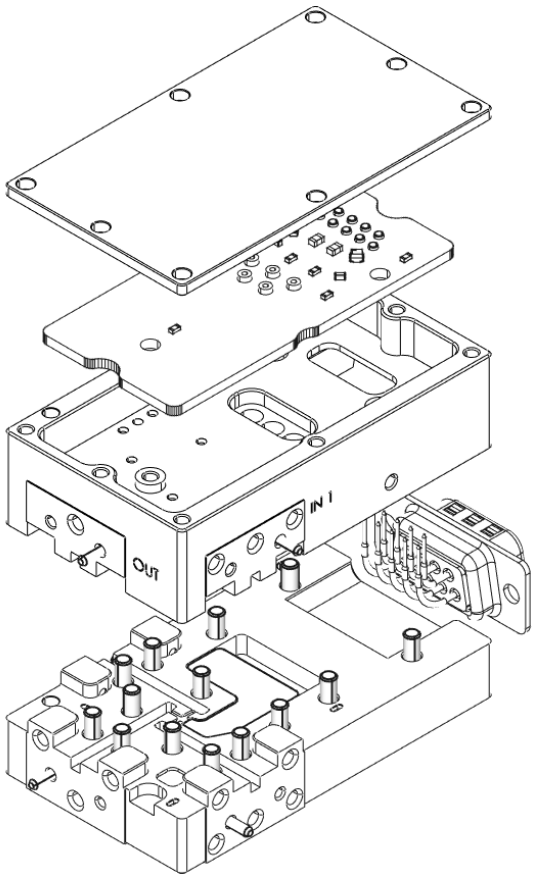
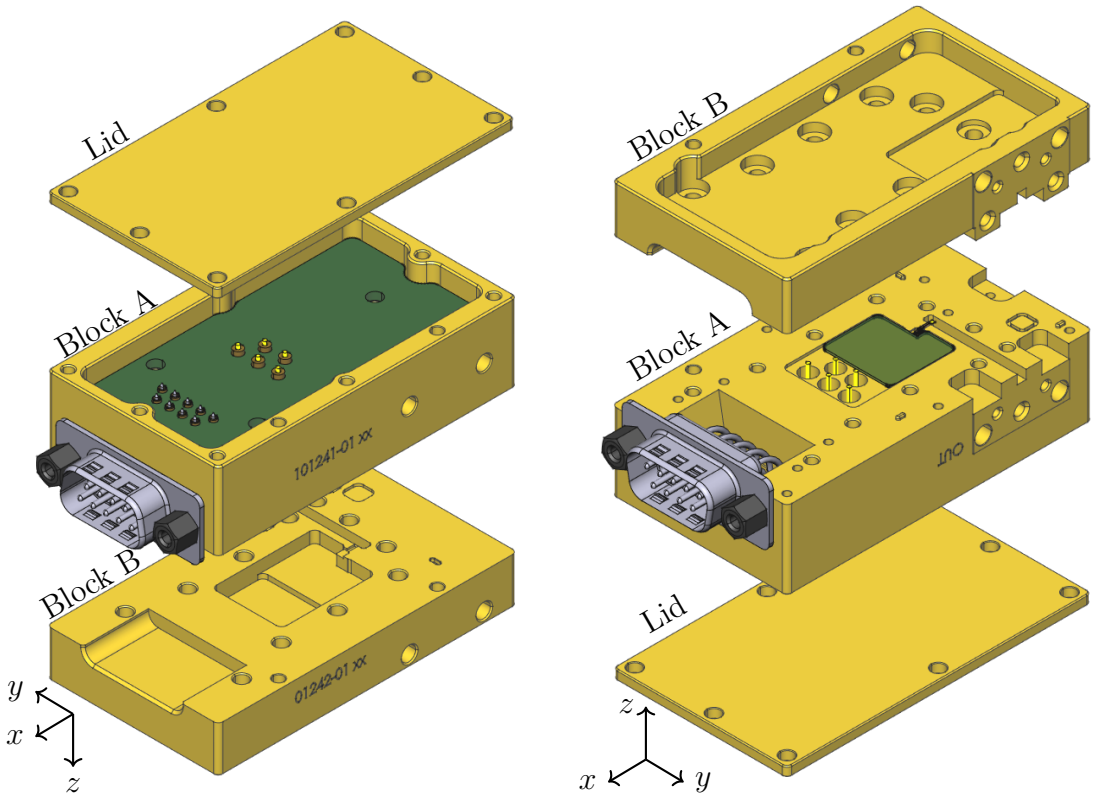


Figure 3.29: Exploded view of the switch split-block. Some screws are omitted for clarity.

3.2.1 Active Cold Load and Switch Split-block

The mechanical structure of the ACL split-block is shown as exploded view in Figure 3.30a and 3.30b. The module consists of two main blocks (Block A and Block B) with a removable lid.



(a) Assembled ACL housing

(b) Exploded view of ACL housing

Figure 3.30: Mechanical housing of the ACL module showing the assembled split-block in exploded view (a) and 180° rotated about the x-axis (b).

Starting from the underside of Block A and hiding block B exposes the RF layout consisting of the probe, the MMIC cavity and inner PCB used for bias routing. This surface is intentionally kept flat and open, since height differences may obstruct the bonding machine. The open area allows for bondwires to be placed both between the transition probes to the MMIC, as well as between the MMIC and PCB.

Additional consideration was given to the vertical alignment of the RF conductors. The probe substrate and the MMIC pads are positioned such as the conductor surfaces are flush, where the only vertical displacement is due to variation in the adhesive glue. The reason for the alignment is in order to avoid adding additional parasitics and avoid degrading the RF performance. Therefore, since the probe substrate is thinner than the MMIC, the plateau for the probe substrate is slightly raised. The same is true for the PCB which is thicker and therefore the plateau is lowered, shown in Figure 3.31.

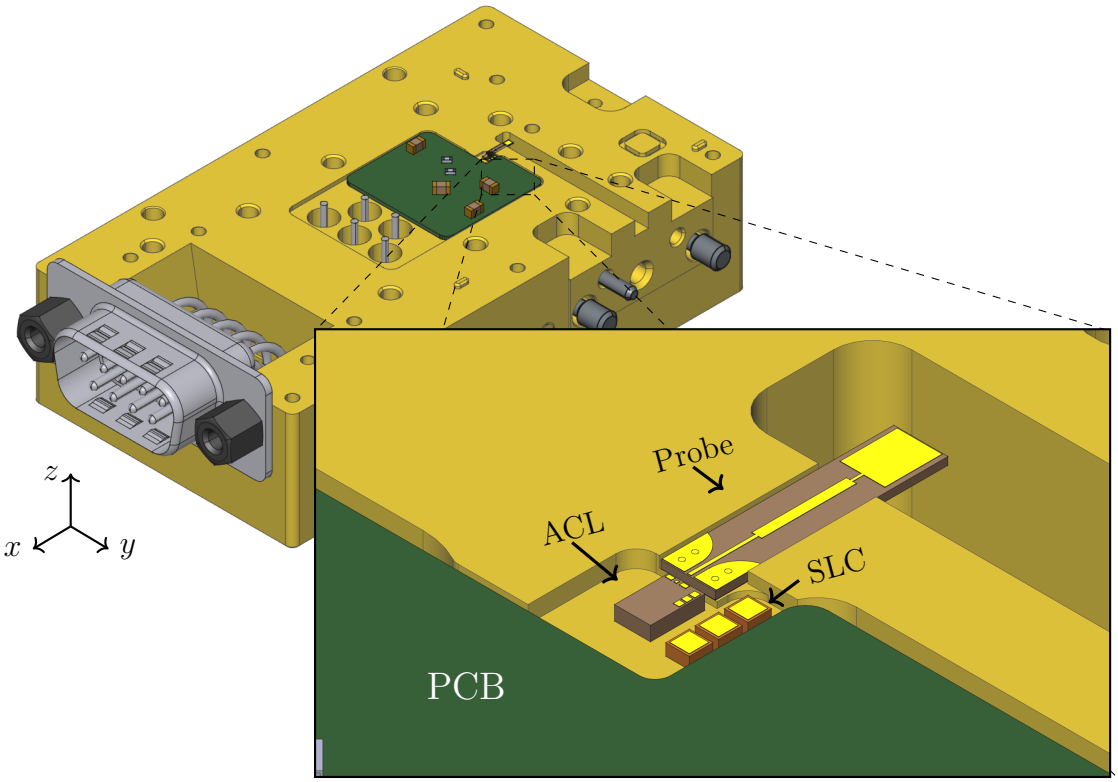
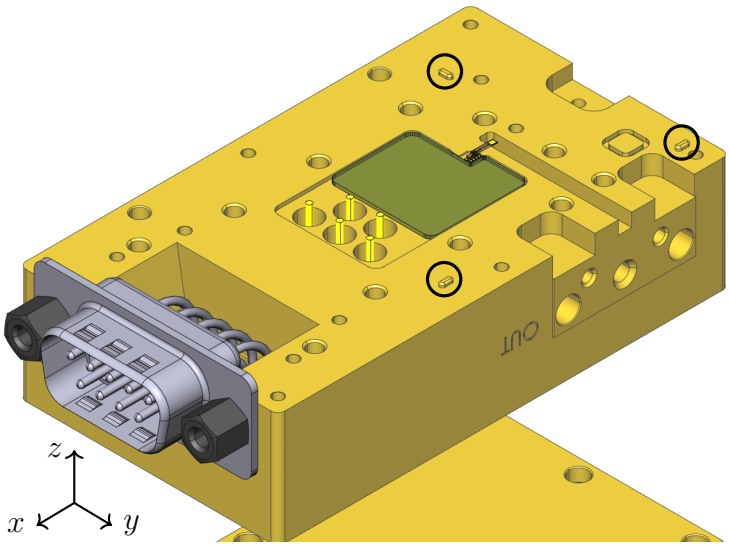
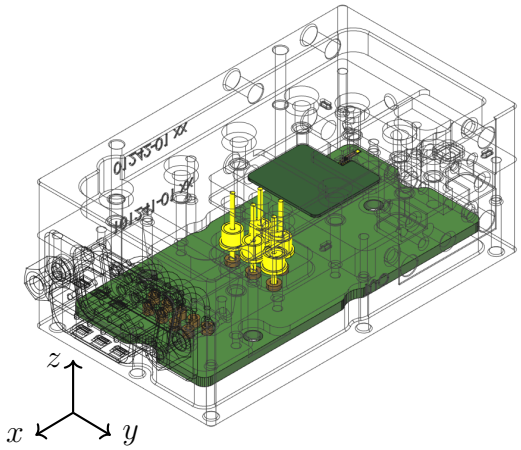


Figure 3.31: Alignment of components in the ACL split-block with a zoomed-in view of the highlighted region showing the probe, MMIC ACL, PCB, and Single layer capacitors (SLC).

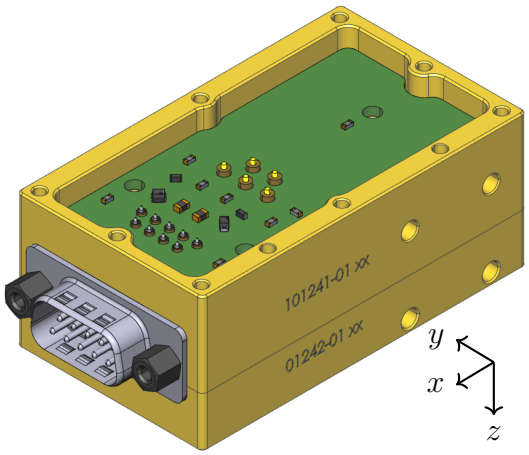
Between block A and B, shown in Figure 3.32a, small alignment shoulders are added in order to constrain the lateral movement during assembly. These pins prevent small shift that could otherwise damage the probes, bondwires or the MMIC. On the top-side of Block A, shown in Figure 3.32c, a larger external PCB is connected through feedthrough capacitors. This external board serves two main purposes. First, it provides additional space for more complex bias circuitry if necessary without requiring a larger cavity inside the split-block. Second, the inner PCB is permanently attached inside with silver epoxy, making modifications more difficult, however changes to the external PCB can be made without disassembling the module. In addition, only an internal PCB means that any modifications require opening the split-block, in turn necessitates realignment of the waveguide, which introduces uncertainty between measurements.



(a) Alignment shoulders



(b) Feedthrough connection



(c) External PCB

Figure 3.32: (a) Alignment shoulders between Block A and Block B used to prevent lateral movement during assembly. (b) Wireframe view of the PCB connections exposing the feedthrough capacitors. (c) Top view of the outer (external) PCB with example mounted components.

The same principles described in this section were applied to design the switch split-block. The main difference is the internal layout, i.e. the switch has one input and two output ports, such that the module must accommodate three waveguide transition structures instead of one. Figure 3.33 shows the internal layout of the switch package. In addition, the switch has a different pad layout, meaning that reusing the same inner PCB not practical. The switch inner PCB was designed smaller, allowing more space for the waveguide transition structures. Lastly, the switch requires only three feedthrough filters. As a result, two pins on the outer PCB are left unconnected.

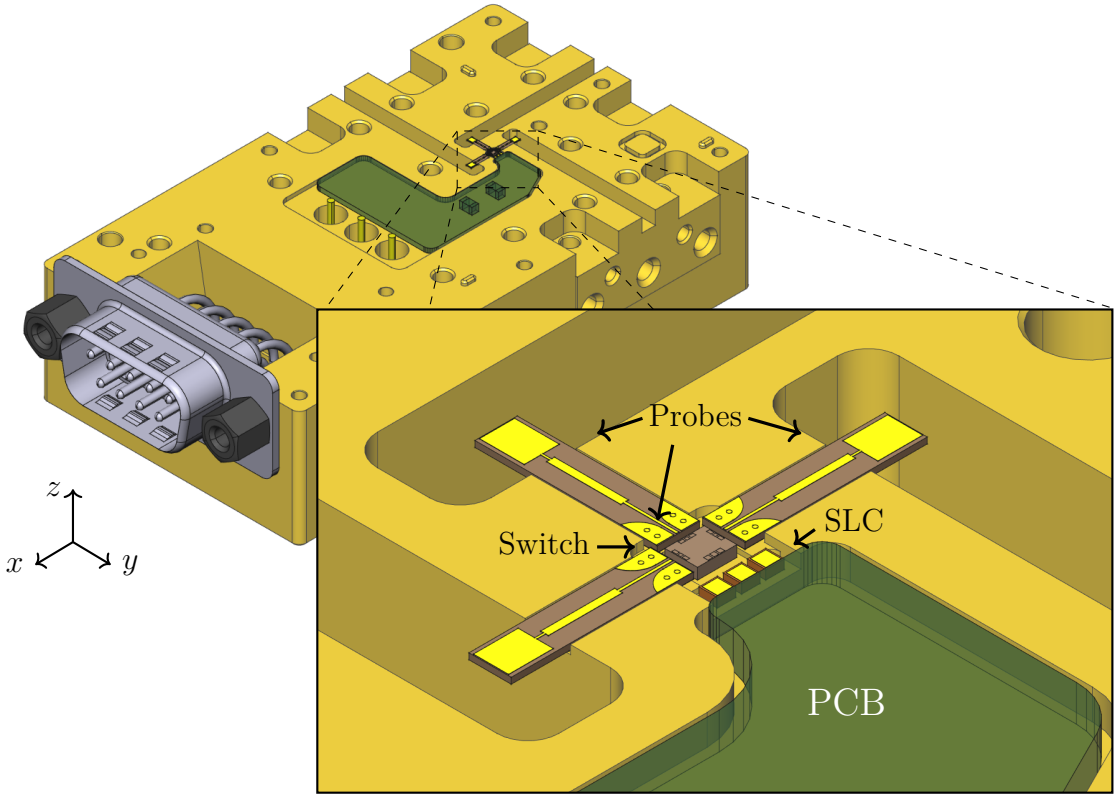


Figure 3.33: Alignment of components in the switch split-block with a zoomed-in view of the highlighted region showing the probe, MMIC switch, PCB, and single-layer capacitors (SLC).

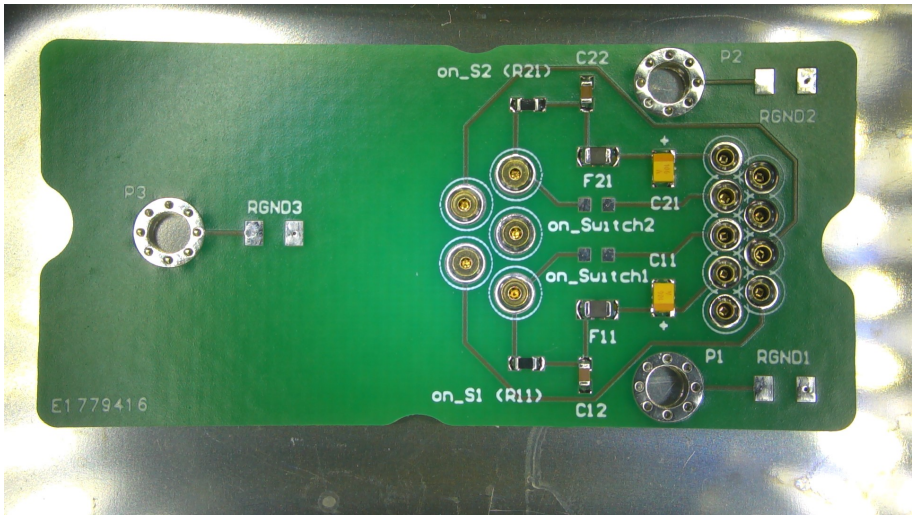
3.2.2 Biasing board

The biasing network was implemented using two different inner PCBs, one for the ACL MMIC and one for the RF switch MMIC. In order to reduce the manufacturing cost and simplify the assembly, both inner PCBs were interfaced to a common outer PCB designed for both cases. The DC signals were routed to the outer PCB through a standard 9-pin D-sub connector. In total, seven of the pins were used, i.e. one for ground, two for ACL bias, two for switch bias, and two for resistance temperature detector (RTD) measurements. Consequently, two pins of the D-sub remained unconnected.

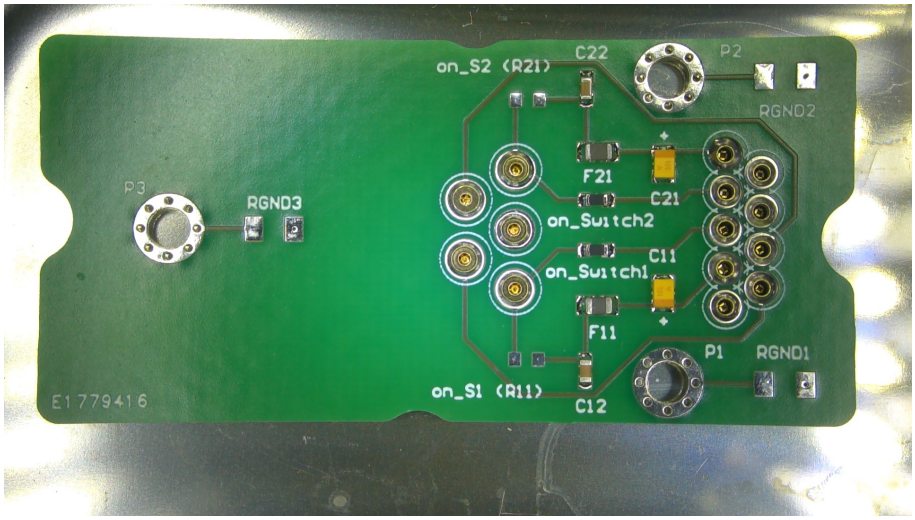
The most critical decoupling was placed as close to the MMICs as possible. Between the MMICs and the inner PCBs, single layer capacitors of 100 pF were used. On both inner PCBs, additional 0603 (imperial) sized decoupling capacitors, primarily 1000 pF, were included on the bias lines. For the ACL inner PCB, a PT1000 RTD was also included for monitoring the local package temperature. The connection between the inner and outer PCBs was realized using 22 nF feedthrough capacitors, see Figure 3.32. The feedthrough capacitors provide a DC path through the housing between the inner and external PCB, while simultaneously filtering the bias lines. In order to make the outer board removable, plated holes and pin receptacles were used, such that the outer PCB could easily be disconnected and modified without opening the split-block and disturbing the split-block alignment while also not needing to re-solder into place. The main objective of the outer PCB was to serve as an evaluation platform for additional biasing components. Therefore, extra footprints were included for additional components, e.g. bypass capacitors, ferrite beads and jumper resistors in order to determine experimentally which configuration was necessary for optimal performance. Figure 3.34 and 3.35 shows the assembled bias boards. The two inner PCBs were fabricated on Rogers 4350 substrate with a thickness of approximately 0.5 mm, while the outer PCB was fabricated on FR4 with a thickness of approximately 1.55 mm. All components used for the biasing boards were selected as commercially available off-the-shelf components.

(a) **(b)**

Figure 3.34: Inside biasing PCBs for the two modules: (a) ACL, (b) switch.



(a)



(b)

Figure 3.35: Outside biasing PCBs for the two modules: (a) ACL, (b) switch.

4

Fabrication and Assembly

The present chapter describes the fabrication and assembly process for the ACL and switch modules. The modules consist of several parts, i.e. split-blocks, probe substrates, MMICs, SLCs and biasing boards, which all need to be assembled with high accuracy. Poor surface quality, dimensions or misalignment may degrade the RF performance. The chapter first describes the fabrication process of the probe substrates and the split-blocks. The probe substrates are manufactured externally while the split-blocks are manufactured in-house at Omnisys Instruments using CNC milling. The second part of the chapter details the assembly procedure of the complete packaged modules. This includes PCB assembly, surface preparation, epoxy attachment of components and bondwires.

4.1 Probe fabrication

The probe substrates were manufactured by SERMA Microelectronics using their thin-film fabrication process. According to information provided by the manufacturer, the non-confidential fabrication steps include substrate laser drilling and cutting, Physical vapor deposition (PVD) sputtering by plasma, photolithography pattern etching with electrolytic chemical bath and finally diamond blade dicing. In addition, the via connection is performed by palladium deposited during the PVD step and also during the electrolytic bath. Since the detailed process sequence is proprietary, a representative fabrication flow for alumina substrates is shown in Figure 4.1. The figure is included to provide process context, i.e. it should not be interpreted as the exact manufacturing routine used by the supplier.

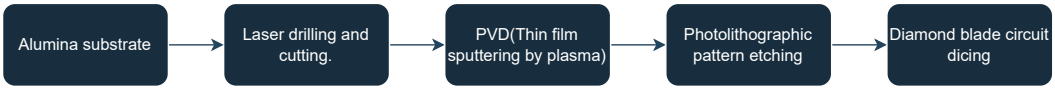


Figure 4.1: Representative thin-film fabrication flow for the probe substrates, shown for process context only.

4.2 Split-block fabrication

The split-blocks were manufactured in-house at Omnisys Instruments. The mechanical design was realized as a split-block structure, meaning the geometry is divided along the split plane and machined as three different parts: Block A, Block B and the lid, as described in section 3.2.1. The parts were milled from solid aluminum blocks using a Primacon P40 CC CNC machine. Figure 4.2 shows the CNC machine and the split-block during milling process.

(a) Primacon P40 CC CNC machine **(b)** Split-block during milling

Figure 4.2: In-house fabrication of the split-blocks at Omnisys Instruments.

After machining, the split-blocks were sent for electrochemical gold plating by PROVEXA. Since the split-blocks are made of aluminum, the gold plating provides a more conductive surface than bare aluminum [32]. This is important in the waveguide structure, since most of the current flows close to the conductor surface, so the surface finish affects the conductor loss. The plating also improves corrosion resistance by providing an oxidation-resistant surface. Since the plating adds material to the machined parts, the critical dimensions, such as waveguide dimensions and cavity depths, were measured both before and after plating to quantify the dimensional changes and verify that they were still consistent with the CAD model, hence the simulated geometry.

4.3 Assembly procedure

The assembly of the complete two modules was not completed within the thesis timeline. However, the biasing boards are fully assembled with components, see Figure 3.34 and 3.35 and the split-blocks are machined and gold plated, so they are ready for assembly. The manufacturing of the probes was severely delayed. Therefore, since the probes interface with the MMIC and other components are preferably mounted after or at the same time as the probes, the modules were not fully assembled. This section describes the intended assembly procedure, such that it can be followed once the probes are available. The following procedure is essentially identical for both the ACL and switch modules.

The biasing boards were assembled outside the split-block, where the PCBs were placed on a heating pad in order to solder the components on to the boards. The remaining steps, described below, will be performed once the probes are available. Before assembly to the split-blocks, the surfaces on the split-blocks will be cleaned in order to remove any particles or contamination that could affect the adhesion, electrical connection or alignment. After surface cleaning, the PCBs, probes, MMIC and SLCs will be attached to the split-block using silver filled electrically conductive epoxy (H20E) from EPOTEK. Careful placement and alignment of the probes and MMICs is critical, since a small misalignment can significantly degrade the RF performance. After placement, the components should be inspected under microscope before and after curing in order to verify correct alignment and placement.

When the epoxy has cured and all components are in place, the bondwire process will be performed. The most critical bondwires are the ones between the MMIC and the probes. Since the MMIC pad dimensions ($30 \times 37\ \mu m$) for the RF path are very small, this step is particularly challenging. For this assembly, 25 μm diameter, edge-to-edge bondwires will be used. The landing area is therefore larger than the pad itself, which complicates achieving a good electrical connection. After bondwiring, the connections will be inspected under microscope to detect any possible defects, e.g. misplaced bonds or deformed loops. Thinner 17 μm bondwires could make this step easier, but are not available with the current bonding setup. As an alternative, future iterations of the MMIC design should consider larger pad dimensions to allow easier and more reliable bondwiring

Once all bondwire connections are made, e.g. the probe to MMIC, MMIC to SLC and SLC to PCB, the split-block halves will be fastened together with screws. When closing the split-block, careful mechanical alignment of the waveguide cavities is critical, since even a small misalignment can introduce discontinuities in the waveguide, leading to degradation of the RF performance.

5
Measurement and characterization

The measurement and characterization of the ACL and switch modules was originally planned as part of the thesis. However, due to delays in the probe manufacturing process, the characterization could not be completed within the thesis timeline.

This chapter presents the planned measurement methodology to characterize the ACL and RF switch. The planned measurements are described such that they can be used as a guideline for future measurements once the modules have been fully assembled. In addition, measurement uncertainties are discussed in order to identify and mitigate errors that could affect the final result and also to obtain reliable measurements to compare with simulated results in section 3.1.

5.1 VNA Measurement Setup

The S-parameter measurements of the ACL and Switch modules are performed using a Vector Network Analyzer (VNA), specifically a Keysight PNA-X with a native frequency range of 10 MHz to 67 GHz. Since the targeted frequency band $50 - 60$ GHz is within the native frequency range of the VNA, no additional frequency extenders are needed. However, since the VNA interfaces with coaxial cables, WR-15 waveguide extenders are required to interface with the modules.

Prior to any measurement, the VNA must be calibrated to move the reference plane. The calibration de-embeds systematic errors introduced by the measurement setup such as cables, connectors and waveguide extenders. If not calibrated, these errors would distort the measurement results [33]. For this work, the calibration plane is referenced to the interface between the WR-15 waveguide extenders and the Device Under Test (DUT), e.g. the ACL and Switch module interface, shown in Figure 5.1 and 5.2. By calibrating before measurement the measured S-parameters represent the response of the DUT itself not including the measurement setup.

The calibration is performed using a Thru-Reflect-Line (TRL) method with a Keysight V11644A WR-15 calibration kit [34], which is the WR-15 kit available in the Chalmers waveguide laboratory. The calibration is verified prior to DUT measurements by connecting a thru and monitoring the insertion loss S_{21}.

5.1.1 S-parameters for ACL Module

The ACL module is a one port device and is characterized by the input reflection coefficient S_{11}, which represents how well the transition is matched to the ACL MMIC. The measurement is repeated under different biasing conditions as well as for the unbiased state to evaluate how the active circuit affects the input impedance seen at the waveguide port. The measurement setup for the ACL is shown in Figure 5.1.

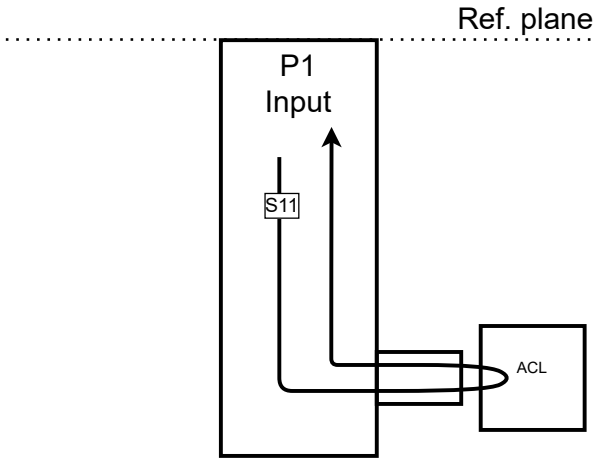


Figure 5.1: Measurement setup for characterizing ACL module, including calibration plane and S-parameter path.

5.1.2 S-parameters for Switch Module

The switch module is a three-port device, consisting of one input (P1) and two outputs (P2, P3). While the input is always active, the output path is selected through biasing. Since only two WR-15 waveguide extenders are available, only one signal path can be measured at a time. The unused port is therefore terminated with a matched WR-15 load in order to prevent reflections from the unmatched port, which would otherwise distort the measurement results.

In this configuration, two different insertion loss paths can be characterized. When the switch is biased such that P1-P2 path is active, the transmission coefficient S_{21} which represents the insertion loss of that path can be measured. Similarly, when P1-P3 is biased, S_{31} can be measured. In addition the isolation can be measured by measuring the transmission when opposing path is biased, e.g. S_{21} while P1-P3 is biased and vice versa. The input return loss S_{11} at P1 is measured with both output ports terminated with matched WR-15 loads.

The transitions themselves are assumed to be identical but a small variation due to manufacturing and assembly alignment may appear. The measured S-parameters are the result for the whole switch module. Thus, in order to evaluate the transition performance, a de-embedding procedure is applied in post-processing in order to isolate the transition performance. This is performed by de-embedding the on-chip measured S-parameters of the switch MMIC and compare the simulated transition to the measured. The measurement setup for the switch is shown in Figure 5.2.

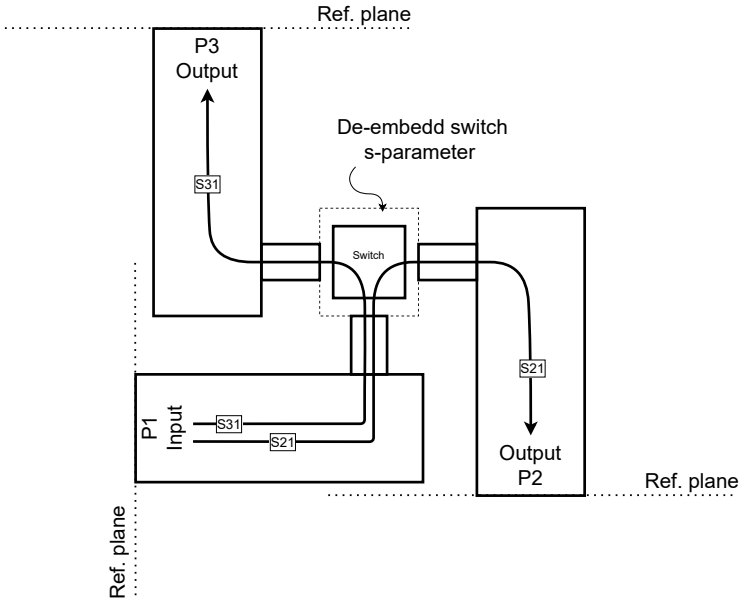


Figure 5.2: Measurement setup for characterizing switch module, including calibration plane, de-embedding location and S-parameter path.

5.2 Noise Temperature Measurement

In addition to S-parameter characterization, the noise temperature of the ACL module is measured in order to evaluate its performance as a cold reference. The measurement is conducted using a 54 GHz receiver developed at Omnisys Instruments. The same receiver was previously used for the on-chip measurements, using coaxial cables and probes to interface the GSG pads. This makes the two measurements easily comparable with the only difference being the interfacing.

The noise temperature of the ACL is characterized using the Y-factor method, described in Section 2.5.2. The measurements are performed in two stages. First, the receiver noise temperature T_e is measured using two known reference loads, a hot absorber and a cold load using liquid nitrogen, connected to the receiver input. From the ratio of the measured noise powers, T_e is extracted as described in Section 2.5.2. Once T_e is known, the ACL is connected to the receiver and its on-state cold temperature T_C is determined. The ACL is switched between its two bias states: in the on state the ACL produces the unknown cold reference $T_C = T_{on}$, while in the off state it acts as a hot reference at approximately room temperature $T_H = T_{off} \simeq 300$ K. The noise power is measured for each state and the Y-factor is obtained as the ratio of the two measured noise powers. Thus, the Y-factor becomes

$$Y = \frac{T_H + T_e}{T_C + T_e} \tag{5.1}$$

and since Y is measured, T_H is $\simeq 300$ K, and T_e is determined in the first step, T_C can be extracted as

$$T_C = \frac{T_H + T_e}{Y} - T_e. \tag{5.2}$$

The presented equations represent an ideal case where losses introduced by connectors, cables and other interfacing components are neglected. However, these losses should be estimated and corrected for and not considered purely as an uncertainty.

5.3 Measurement uncertainties

The previously mentioned measurements are all subjected to several uncertainties that may affect the accuracy of the result. This section discusses the sources of these uncertainties for both the VNA and noise temperature measurements.

VNA calibration accuracy

The calibration performed on the VNA moves the reference plane and de-embeds systematic errors introduced by the measurement setup. However, in practice, no calibration is perfect and therefore, some residual errors exist. As mentioned in Section 5.1, the accuracy of the calibration can be verified, however, some level of error always remains.

Connector and waveguide interface

In order to conduct either measurement, the waveguide connection between the VNA extenders and the DUT or between the receiver and the DUT is a source of uncertainty. When connecting the two waveguide flanges, some small variation is introduced in terms of misalignment and torque. Thus, to minimize these variations between measurements, the waveguide connections should be tightened to a consistent torque and measurements should be repeated several times to reduce the uncertainty.

Physical temperature of the ACL in off state

If the off state of the ACL is used as the room temperature reference, its noise temperature is assumed to be close to 300 K. However, if the ACL has been biased for some time, heating of the package may increase the physical temperature, thus shifting the reference temperature T_H. This could directly affect the extracted cold temperature T_C. To reduce this effect and improve repeatability, the ACL should reach steady state during measurements.

6
Discussion

The following discussion is primarily based on the simulation result presented in Section 3.1. The discussion includes summary and interpretation of the simulated result and evaluation on the impact of packaging and mechanical constraints on the RF performance. Following the discussion, suggestions of future work is presented.

6.1 Summary and interpretation of simulation results

The RF design demonstrate results that meets the design specifications presented in Section 3.1.1. Specifically, a waveguide-to-planar transition, realized in a split-blocks for both the ACL and RF Switch, where each module operates at $50 - 60$ GHz. They are integrated with SiGe MMIC technology by using the CPWG section such at the bondwires are interfacing the GSG pads on the MMICs. For both modules, there is sufficient space for the DC routing, meaning the biasing boards with sufficient decoupling and filtering. The design is also robust for machining tolerances which is validated through an sensitivity analysis. According to the simulated result, the performance of the RF design reaches beyond the specified $S_{11} < -15$ dB.

The selected final design, Candidate 2, show a simulated return loss $S11 < -26.9$ dB over the full band $50 - 60$ GHz, see Figure 3.22, which is well above the specified requirement. In addition, the insertion loss of the transition is simulated to be below 0.3 dB indicating an efficient coupling between the waveguide to MMIC.

A B2B structure was simulated, which represents two transition connected by the switch MMIC. The B2B, shows a return loss $S_{11} < -17.8$ dB over the full band and an insertion loss below 0.6 dB. The slightly worse return loss in comparison to a single transition is likely due to additional parasitics being added when another transition is introduced, further shifting the impedance match from 50 ohm. It should be noted that the B2B performance is simulated using the simplified CPWG substrate to emulate the MMIC, not including the actual stackup of the SiGe MMIC.

Lastly, the sensitivity analysis demonstrated a robustness to manufacturing tolerances by varying the width and lengths of the transmission lines and assemble variation for the bondwiring. The result indicates that the return loss S_{11} remained below -20 dB for all investigated variations, see Table 3.9 and Figure 3.21.

6.2 Packaging impact

The work shows that the probe model can not be designed independently from the package it is integrated in. The work started with an initial simple microstrip design, which from a purely EM perspective showed good performance. However, when introducing each packaging constraint such as the CPWG interface, increased probe length and bondwires shifted the impedance away from the initial match. This occurred subsequently for each packaging constraint that was introduced. The initial microstrip probe, with no multi-stage impedance transformer was well matched to 50 Ω. By optimizing just a few parameters and adding the CPWG section, see Table 3.4 and Table 3.6, the impedance shifted slightly and a small degradation of performance was seen. The CPWG section itself was required because the SiGe MMIC lacks a backside ground plane, and the ground reference therefore had to be transferred to the topside GSG pads through bondwires. Adding the bondwires introduced an additional impedance shift, and with the current parameters no solution could be found. The solution was to add the multi-stage impedance transformer, which gave more degrees of freedom to find an impedance match. The final result showed an even better in-band performance in comparison to the initial design, likely due to more time and simulations was spent on optimizing the final design.

The most significant mechanical layout that affected the RF performance was the probe length. In a purely EM perspective a shorter probe would be preferable, but in the switch package, a shorter probe resulted in a very thin wall of only 100 μm. Extending the probe to approximately a total length of 3 mm increased the wall thickness to 0.86 mm, which can be reliably machined with the CNC process.

The DC coupling analysis showed that the RF signal coupling from the waveguide signal path to the MMIC and PCB cavities is approximately −45 dB for the ACL and −70 dB for the switch module. The difference is mainly attributed to the difference in geometry. However, the level is low enough that it is not expected to show significant degradation in RF performance. In addition, if degradation is suspected during measurement, the cavity for the MMIC and PCB is large enough to add an Eccosorb RF absorber if needed.

When biased, according to on-chip measurements and the biasing conditions of the MMIC circuit, the device dissipates only a small amount of DC power. The DC dissipation is assumed to be on the order of 1 mW. The MMIC is attached to the split-block with epoxy (H20E), which provides a thermal path from the die to the housing. Since the aluminum split-block is comparatively large, it effectively acts as a heat sink for the circuit. The temperature rise due to self heating is therefore expected to be small. The package temperature still might matter because the ACL off-state is used as the room temperature reference, so a temperature shift might change the measured cold temperature T_C. To monitor the package temperature and its stability, a PT1000 RTD is mounted on the ACL inner PCB to measure the inner package temperature.

6.3 Limitations

There are a few limitations worth discussing regarding the presented results. Although the simulated results meet the design specifications, there are limitations that should be considered when evaluating the results. Much effort was put into making the model as close to reality as possible, however this will never fully be the case.

An important limitation of the simulated result is the simplified CPWG substrate used to emulate the MMICs. Since no metallization stackup was provided, a CPWG model was created in HFSS to represent the MMIC interface. The model was designed to minimize the additional capacitance such structure introduces, since the MMIC pads are assumed to be 50 Ω. The emulated MMIC model still exhibited a slight capacitance, which may affect the accuracy of the simulated result compared to the actual MMIC.

The bondwires are modeled to resemble how they may look in reality, but it is very hard to predict how they will actually turn out once bonded. Especially since the small pad size will make the mounting of the bondwires very difficult, which could shift the impedance response significantly. The same applies for the placement of the probes and MMICs. In all simulations, they are assumed to be perfectly place at a specific distance. However, in reality exact placement is difficult, since the components can shift slightly in the epoxy during curing.

Finally, the measurement and characterization of the physical modules could not be completed within the thesis timeline, thus the evaluation of the design is entirely based on simulated S-parameters. Unfortunately, the noise temperature performance, which is the primary application of the work is very hard to predict from simulated S-parameters alone. In addition, no thermal simulations were performed, which is a limitation since the package temperature can affect the noise performance of the ACL. The measurement methodology presented in Chapter 5.2 provides the planned measurements once the modules are fully assembled.

6.4 Future work

The continuation of this work is to complete the planned measurements and evaluate the performance of the assembled modules. This includes, S-parameter characterization of both modules using VNA measurements and noise temperature measurements of the ACL module. In addition, combining the two modules to resemble the integrated version with both the ACL and switch on the same die.

Several aspects of the work could be improved in future iterations. The accuracy of the simulations could be increased by using the real metallization stackup of the SiGe MMIC. In addition, alternative design for the probe could investigated in order to realize the impedance matching differently. The current design required relatively narrow transmission lines, which are sensitive to small variation in manufacturing. An alternative approach would be to perform more of the matching at the probe tip itself, for example using radial probes instead of a rectangular one. Furthermore, the current design also uses an alumina substrate to facilitate the fabrication of the grounding vias. Substrates such as quartz could be considered, where the topside ground could be realized with wrapping the conductor around the edge instead of through vias which is hard to realize on quartz.

7
Conclusion

This thesis presented the packaging and integration of two separate V-band SiGe MMICs, an Active Cold Load and an SPDT RF switch, intended to investigate a compact, electronically controlled alternative to conventional radiometer calibration. For both modules, a complete package was designed, comprising of a WR-15 waveguide to planar transition using an E-plane probe, bondwire interconnects from probe to MMIC, an aluminum split-block housing and a modular DC biasing board. Due to manufacturing delays, measurements of the assembled modules could not be completed within the thesis timeline.

A longitudinal E-plane probe on a 100 μm alumina substrate was designed and optimized in HFSS for the $50-60$ GHz targeted frequency band. Since the SiGe MMICs lack a backside ground plane, the ground was connected from the MMIC GSG pads to the probe by introducing a short CPWG section at the probe interface. During the design process, it was shown that the packaging constraints such as the CPWG interface, bondwires, probe length and split-block geometry affected the impedance response of the probe. In order to compensate for the impedance shift, a multi-stage impedance transformer was introduced and optimized using HFSS. To the author's knowledge, this is the first packaging of an ACL in the V-band frequencies.

The final transition achieved a simulated return loss $S_{11} < -26.9$ dB and an insertion loss $S_{21} > -0.3$ dB across the full $50-60$ GHz, which is beyond the specification $S_{11} < -15$ dB. In addition, to evaluate the performance of the switch packaging, a back-to-back structure was simulated and showed $S_{11} < -17.8$ dB and $S_{21} > -0.6$ dB. To account for manufacturing tolerances, a sensitivity analysis was performed by investigating dimensional and bondwire placement variation. The sensitivity analysis confirmed that for all investigated cases, the return loss S_{11} remained below -20 dB. This indicates that the design is robust to the considered manufacturing and assembly tolerances. In addition, simulations of RF to DC coupling to the inner biasing board were conducted, the result indicates low coupling, approximately -45 dB for the ACL and -70 dB for the switch package and is not expected to significantly degrade the performance.

Further considerations for the mechanical manufacturability and assembly were implemented. The probe was lengthened to approximately 3 mm such that the wall between the adjacent waveguide cavities for the RF switch was increased from initial 100 μm to 860 μm. The probe, MMIC and inner PCB cavities were designed such that the vertical alignment of the conductor surfaces remained flush, minimizing parasitics. In addition, two separate biasing boards for each module were designed such that the biasing network could be modified using the outer biasing board without opening the split-block and disturbing the alignment. The most challenging aspect of the assembly was the bondwiring to the small (30×37 μm) MMIC pads, since the bondwire landing is larger than the pad itself.

The most significant limitation of the work is the characterization and evaluation is entirely based on the EM simulations. Since the modules were not measured, the noise temperature performance, which is the primary application of the ACL was not evaluated within the timeline of the thesis. Furthermore, since the metallization stackup of the MMIC was not available, it was represented by a CPWG substrate emulating the MMIC. The accuracy of the simulated matching is therefore limited by how closely this model represents the real MMIC. In particular, the emulated model retained a small residual capacitance, and the parasitics of the actual MMIC may differ from the model. Another limitation is for all simulations, the components are perfectly aligned, whereas in practice they can shift during the curing of the epoxy.

Despite the mentioned limitations, the simulated results indicate that the proposed packaging approach is suitable for V-band ACL and RF switch modules. Future work includes measuring the S-parameter performance for both modules, noise temperature measurement for the ACL and comparing the result to on-chip measurements. The next step is to package the integrated version, with an ACL and RF switch on a single die. In addition, alternative probe geometries, such as a radial probe, could be explored to perform more of the impedance matching at the probe tip and reduce the sensitivity associated with the narrow transmission lines of the current design.

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