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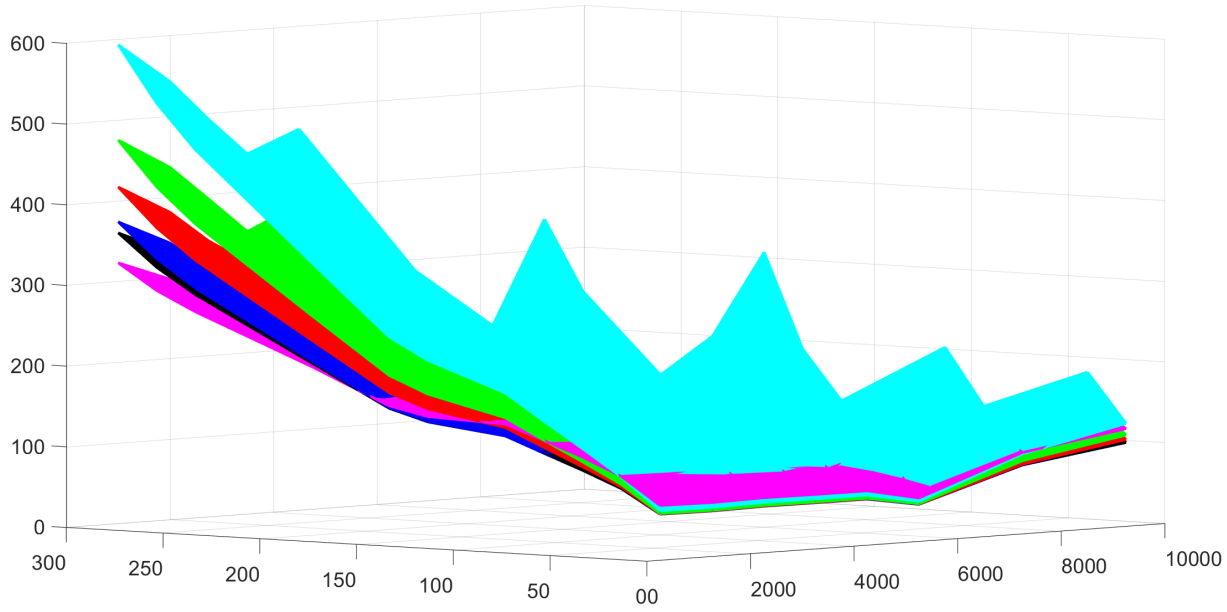

Improving the Efficiency of SiC-based Inverter in BEV by Selecting the Switching Slew Rate for Optimisation of Switching Losses and Voltage Overshoot

Master's Thesis in Sustainable Electric Power Engineering and Electromobility

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Gothenburg, Sweden 2024
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Abstract

Silicon Carbide (SiC) inverters are increasingly utilized in Battery Electric Vehicles (BEVs) due to their superior efficiency and thermal performance compared to traditional silicon-based inverters. However, managing turn-off switching losses and voltage overshoot is a significant challenge that affects overall inverter performance and reliability. This thesis addresses these issues by investigating different value of turn-off gate resistors, applying a multi-step pulse strategy at the gate drive signal V_{GG}, and incorporating a snubber circuit.

The methodologies were evaluated using a Double Pulse Test (DPT) setup in LTspice and a drive system model in PLECS. According to the DPT results, it was found that applying a multi-step pulse at V_{GG} with appropriate magnitude and duration at lower I_{ds} reduces current oscillation and voltage overshoot without significantly affecting current slew rate and turn-off switching losses. However, this method effectively decreases voltage overshoot and current slew rate at higher currents but slightly increases turn-off losses.

Additionally, based on the results from the simulations in LTspice and PLECS, larger gate resistors reduce voltage overshoots and slew rates but simultaneously increase turn-off energy and losses. The snubber circuit proved most effective in reducing the voltage overshoot. For minimizing switching energy and losses, the multi-step V_{GG} method, with a 2V step voltage magnitude and 30ns duration, maintained switching losses similar to the original circuit with advantages at relatively lower current and torque levels, while the snubber circuit can be considered at higher currents and torque, as it effectively reduces voltage overshoot while the increase in switching losses is slight.

Lastly, the effect of varying the DC link was investigated. The goal is to have the lowest losses for a DC link voltage. Increasing the DC voltage helps reduce conduction losses due to the decrease in current. Additionally, depending on if different methods are used, the voltage rating of the transistor can be reduced giving lower conduction losses. For the switching energy, the multi-step V_{GG} method, with a 2V step voltage magnitude and 30ns duration, is effective at relatively lower current levels, maintaining the total switching energy comparable to the original circuit while reducing the voltage overshoot. At higher currents, the snubber circuit is more effective, offering a balanced approach to decrease voltage overshoot and improving the efficiency of the BEV inverter.

Keywords: SiC, Voltage Overshoot, Turn-off Losses, Gate Resistor, Snubber Circuit

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Thanks to Sepideh and Zeekr Technology Europe for providing me with the opportunity to work on this thesis. This experience has been an excellent learning opportunity, allowing me to apply what I have learned in the classroom to real-world industrial challenges.

Yumeng Shao Gothenburg, November 2024

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

BEV	Battery Electric Vehicle
EMI	Electro Magnetic Interference
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PMSM	Permanent Magnet Synchronous Machine
SiC	Silicon Carbide
SPWM	Sinusodial Pulse Width Modulation
WBG	Wide Band Gap
DPT	Double Pulse Test
DUT	Device Under Test
AGD	Active Gate Driver
FEM	Finite Element Method
LUT	Look-up Table

Nomenclature

Below is the nomenclature of parameters and variables that have been used throughout this thesis.

Parameters

V_{GG}	SiC MOSFET Gate Drive Voltage
V_{ds}	SiC MOSFET Drain-Source Voltage
V_{dc}	DC link Voltage
V_{d}	DC link Voltage
I_{ds}	SiC MOSFET Drain-Source Current
E_{off}	SiC MOSFET Turn-off Switching Energy
E_{on}	SiC MOSFET Turn-on Switching Energy
L_{σ}	Stray Inductance
R_{g}	Gate Resistor
R_{goff}	Turn-off Gate Resistor
R_{gon}	Turn-on Gate Resistor
I_{o}	Load Current
I_{load}	Load Current
C_{s}	Turn-off Snubber Capacitor
R_{s}	Turn-off Snubber Resistor
C_{ov}	Overvoltage Snubber Capacitor
R_{ov}	Overvoltage Snubber Resistor
P_{loss}	SiC MOSFET Turn-off Switching Losses
V_{peak}	SiC MOSFET Turn-off Overvoltage Peak Value
R_{DS}	Drain Source resistor

Variables

i_{Cs}	Current Flowing through The Turn-off Snubber Capacitor
t_{fi}	Current Falling Time
v_{Cs}	Turn-off Snubber Voltage
t_{on}	Transistor On Time over One Switching Period
$\Delta v_{\mathrm{ds,max}}$	Maximum Difference Between Overvoltage and DC Link Voltage
k	Overvoltage Severity Factor

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1

Introduction

Battery Electric Vehicles (BEVs) have become a focal point of development in recent years. Unlike traditional internal combustion engine vehicles that rely on fossil fuels, BEVs are powered by electricity, which significantly reduces dependence on fossil fuels and thereby mitigates environmental pollution. Moreover, the widespread adoption and promotion of BEVs contribute to the advancement of sustainable development.[1][2].

However, the efficiency of the drive system can constrain the development and widespread adoption of electric vehicles. As one of the core components of the drive system, the inverter plays a crucial role in determining overall efficiency. Enhancing the efficiency of the inverter can significantly improve the overall efficiency of the drive system, thereby advancing the development of electric vehicles.[3][4][5].

1.1 Problem Background

Silicon Carbide (SiC) semiconductors have emerged as a superior alternative to traditional silicon-based devices in BEV inverters, offering faster switching speeds, and better thermal performance[6]. However, the optimization of SiC-based inverters is a complex challenge, where achieving a balance between switching losses and voltage overshoot is critical. Higher switching speeds introduce certain challenges, such as increased voltages across transistors during turn-off, which can cause EMI, false triggering [7], and necessitate the use of transistors with higher voltage ratings. However, by adjusting the slew rate to slow down the switching speed, voltage overshoots can be mitigated, but this also leads to increased switching losses. Therefore, a balanced solution must be sought to optimize these competing factors.

As a result, considerable and ongoing research has been undertaken in this field. Various approaches have been explored and implemented to optimize switching losses by reducing slew rates and minimizing overshoot voltage. For instance, methods such as adjusting the gate resistor[8][9], incorporating snubber circuits[10][11], and implementing a procedure of multi-step gate drive pulses for slew rate control[12][13] have been introduced. However, existing studies have yet to fully compare these methods in the aspects of slew rate, voltage overshoot and inverter-side losses.

1.2 Purpose

This thesis aims to compare various methods for optimizing turn-off switching losses and voltage overshoots in SiC-based inverters. The study will examine three approaches: adjusting turn-off gate resistor values, implementing snubber circuits, and using multi-step gate drive pulses to control current slew rate. Their impact on turn-off slew rate, voltage overshoot, total switching losses and total losses including switching losses and conduction losses will be analyzed and compared. Additionally, the thesis will explore the effects of varying DC link voltage levels on the turn-off switching process. By comparing different scenarios and assessing inverter-side losses throughout the entire drive system, this research seeks to identify the most energy-efficient solution.

1.3 Sustainability

The development of SiC-based inverters for BEVs is crucial for advancing sustainable transportation. Optimizing inverter-side voltage overshoot and switching losses can reduce the overall energy consumption of BEVs. This contributes to sustainability by increasing power transfer efficiency for a given volume, thereby reducing the footprint, extending the range of electric vehicles, decreasing dependence on fossil fuels, and lowering greenhouse gas emissions associated with transportation[14].

1.4 Ethics

This thesis adheres to ethical standards and conducts simulations and data processing within the requirements set by Chalmers University of Technology and Zeekr Technology Europe.

2

Theoretical background

This section introduces the fundamental theoretical knowledge related to the SiC MOSFET turn-off process and the factors influencing it, providing a theoretical foundation for the subsequent chapters.

2.1 Turn-off Switching Losses and Influencing Factors

Figure.2.1 illustrates the process of switching off a transistor.

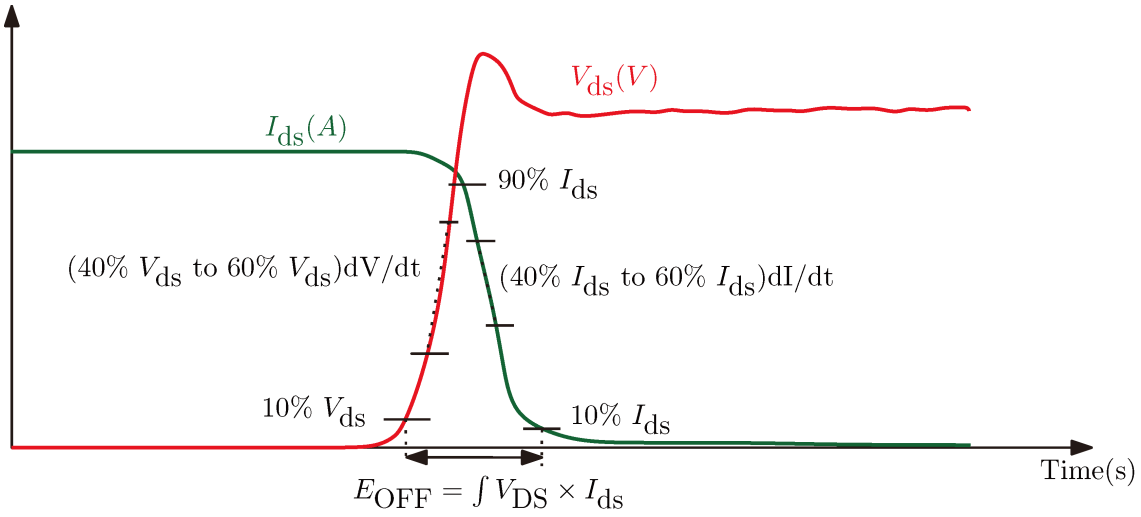

Figure 2.1: Turn-off Switching Process

As observed from Figure.2.1, when the gate drive pulse V_{GG} transitions from high to low, V_{ds} gradually increases and approaches V_{dc}, at which point I_{ds} begins to decrease. As I_{ds} gradually decreases to zero, V_{ds} stabilizes at the value of V_{dc}. Therefore, during the turn-off process, due to the variations in V_{ds} and I_{ds}, turn-off energy E_{off} is generated. According to the Wolfspeed datasheet[15], the integration time for E_{off} is defined from the moment V_{ds} reaches 10% to the moment I_{ds} reaches 10%.

2.1.1 Voltage Overshoot

Based on the turn-off process depicted in Figure.2.1, it can be observed that when V_{ds} rises to V_{dc}, it continues to increase before eventually decreasing and stabilizing at V_{dc}. This voltage overshoot is caused by the presence of stray inductance in the circuit[16], as shown in Figure2.2.

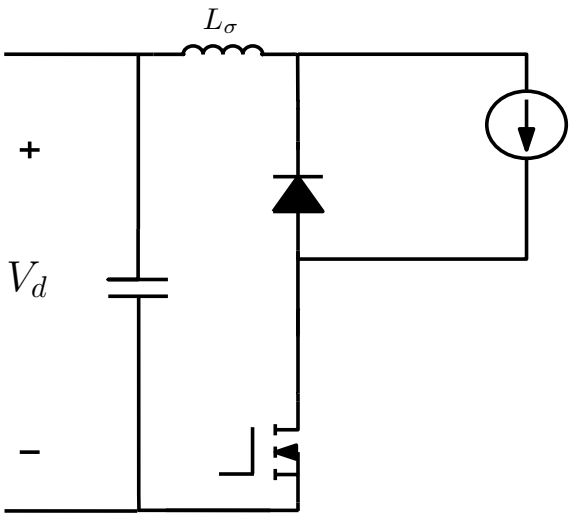

Figure 2.2: Converter Circuit with Stray Inductance

During the turn-off of the switch, the current decreases, leading to a negative current slew rate. Consequently, the presence of stray inductance induces additional overvoltage on the switch, where L_σ is stray inductance. Higher overvoltage results in increased turn-off energy, which in turn leads to greater turn-off losses.

$$V_{\mathrm{ds}} = V_{\mathrm{d}} - L_\sigma \frac{di_{\mathrm{ds}}}{dt} \tag{2.1}$$

2.1.2 Slew Rate

According to the Wolfspeed datasheet[15], the voltage slew rate is defined as the slope corresponding to the rise from 40% V_{ds} to 60% V_{ds}. Similarly, the current slew rate is defined as the slope corresponding to the decline from 60% I_{ds} to 40% I_{ds}.

According to (2.1), it can be observed that the current slew rate is one of the factors influencing overvoltage. Theoretically, reducing the current slew rate can mitigate overvoltage. However, as shown in the turn-off process in Figure.2.1, lowering the current slew rate increases the integration area, which leads to higher turn-off losses. Nevertheless, since the overvoltage is reduced, a comprehensive assessment is required to determine the overall impact on turn-off losses.

In the turn-off process shown in Figure.2.1, the voltage slew rate is also a factor influencing turn-off losses. A lower voltage slew rate increases the integration area, leading to higher turn-off losses.

2.2 Conduction Losses

Conduction losses can be calculated using the relation

$$P_{\text{cond}} = R_{\text{DS}} I_{\text{ds}}^2 \tag{2.2}$$

2.3 Switching Losses and Voltage Overshoot Optimization Methods

2.3.1 Gate Resistance

In a SiC MOSFET, the gate resistance R_g connected in series at the gate terminal affects the charging and discharging speed of the parasitic capacitances during the switching process. When R_g increases, the time constant for gate charging and discharging also increases, causing the gate voltage to change more slowly, thereby reducing the switching speed of the SiC MOSFET[17]. The increased R_g delays the change in gate voltage, which in turn slows down the rate of change of V_{ds} or I_{ds}, resulting in a lower slew rate.

2.3.2 Snubber Circuit

2.3.2.1 Turn-off Snubber

Figure.2.3 displays the topology of the turn-off snubber[16].

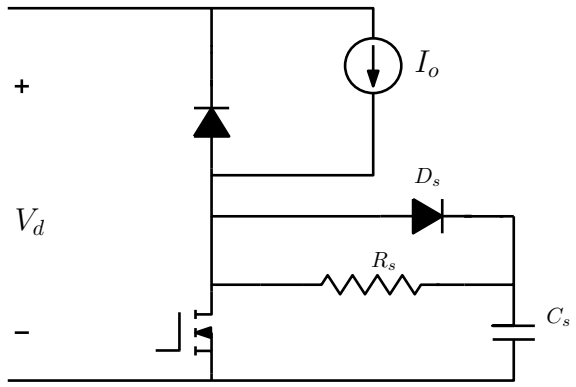

Figure 2.3: Turn-off Snubber

The purpose of a turn-off snubber is to reduce turn-off losses by altering the switching trajectory. During turn-off, the transistor current I_{ds} gradually decreases, and the current flowing through the turn-off snubber capacitor is given by

$$i_{\text{Cs}} = \frac{I_{\text{o}} t}{t_{\text{fi}}} \quad 0 < t < t_{\text{fi}} \tag{2.3}$$

Therefore, the voltage across the turn-off snubber capacitor is

$$v_{\mathrm{Cs}} = \frac{1}{C_{\mathrm{s}}} \int_0^t i_{\mathrm{Cs}} dt = \frac{I_{\mathrm{o}} t^2}{2 C_{\mathrm{s}} t_{\mathrm{fi}}} \tag{2.4}$$

When $t = t_{\mathrm{fi}}$ and $v_{\mathrm{Cs}} = V_{\mathrm{d}}$, the voltage of the turn-off snubber capacitor can be calculated using the relation

$$C_{\mathrm{s}} = \frac{I_{\mathrm{o}} t_{\mathrm{fi}}}{2 V_{\mathrm{d}}} \tag{2.5}$$

For selecting the turn-off snubber resistor, it is generally considered to limit the diode's reverse-recovery current during turn-on to $0.2 I_{\mathrm{o}}$. Therefore, the turn-off snubber resistor can be calculated using the equation

$$R_{\mathrm{s}} = \frac{V_{\mathrm{d}}}{0.2 I_{\mathrm{o}}} \tag{2.6}$$

When the switch is on, the turn-off snubber capacitor typically needs to discharge V_{Cs} to $0.1 V_{\mathrm{d}}$ before the next turn-off comes. The selected values of the capacitor and resistor should satisfy the inequality

$$t_{\mathrm{on}} > 2.3 R_{\mathrm{s}} C_{\mathrm{s}} \tag{2.7}$$

2.3.2.2 Overvoltage Snubber

Figure.2.4 displays the topology of the overvoltage snubber[16].

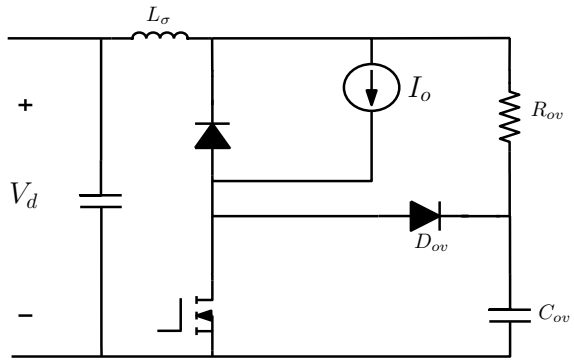

Figure 2.4: Overvoltage Snubber

The purpose of an overvoltage snubber is to absorb the overvoltage during turn-off. The basic principle involves transferring the energy stored in the stray inductance into the overvoltage snubber capacitor. According to the following energy transfer equation, a larger C_{ov} will reduce the overvoltage,

$$\frac{C_{\mathrm{ov}} \Delta v_{\mathrm{ds,max}}^2}{2} = \frac{L_\sigma I_{\mathrm{o}}^2}{2} \tag{2.8}$$

The overvoltage caused by stray inductance can be expressed as

$$k V_{\mathrm{d}} = \frac{L_\sigma I_{\mathrm{o}}}{t_{\mathrm{fi}}} \tag{2.9}$$

If $\Delta v_{\mathrm{ds,max}}$ is set to $0.1V_{\mathrm{d}}$, the capacitance of the overvoltage snubber can be determined using (2.8) and (2.9),

$$C_{\mathrm{ov}} = \frac{100kI_{\mathrm{o}}t_{\mathrm{fi}}}{V_{\mathrm{d}}} \quad (\Delta v_{\mathrm{ds,max}} = 0.1V_{\mathrm{d}}) \tag{2.10}$$

Similar to the turn-off snubber, the selected values of the capacitor and resistor for the overvoltage snubber should satisfy the following inequality in order for the overvoltage capacitor to be sufficiently discharge before next turn-off,

$$t_{\mathrm{on}} > 2.3R_{\mathrm{ov}}C_{\mathrm{ov}} \tag{2.11}$$

2.3.3 Multi-step Gate Drive Pulse

Typically, gate drive pulses are of the single-step type, where the transistor turns off when the gate drive pulse transitions from a high level to a low level. To control the slew rate and consequently reduce voltage overshoot, a multi-step gate drive pulse is employed. The basic principle involves introducing intermediate steps during the transition of the gate drive pulse from high to low, thereby slowing down the slew rate [13][18][19][20].

Figure 2.5 shows the original gate drive pulse and the gate drive signal with an intermediate pulse applied at the end of turn-off. The purpose of this approach is to control the current slew rate.

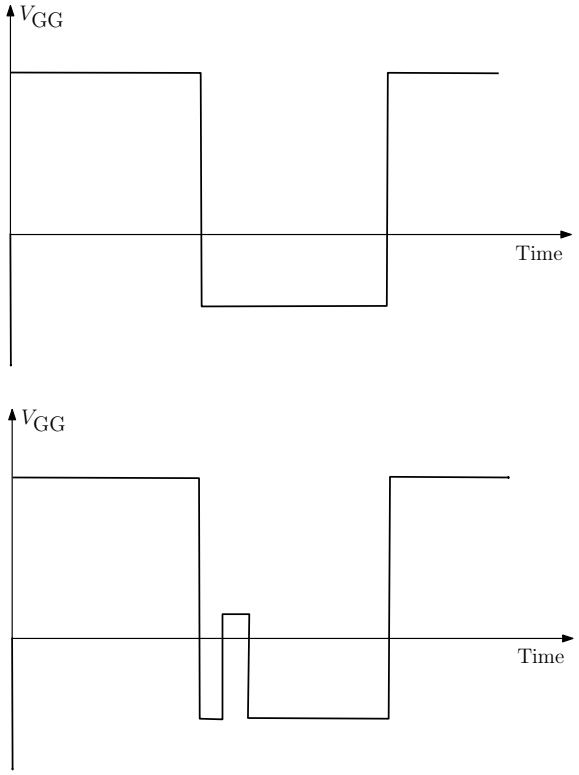

Figure 2.5: Different Gate Drive Pulse

3

Case Set-up

This section presents two simulation models used to test the turn-off switching process and to analyze the distribution of drive system losses, respectively.

3.1 Double Pulse Test (DPT) Setup

Figure.3.2 shows the Double Pulse Test (DPT) setup used for evaluating the switching characteristics of the SiC MOSFET module.

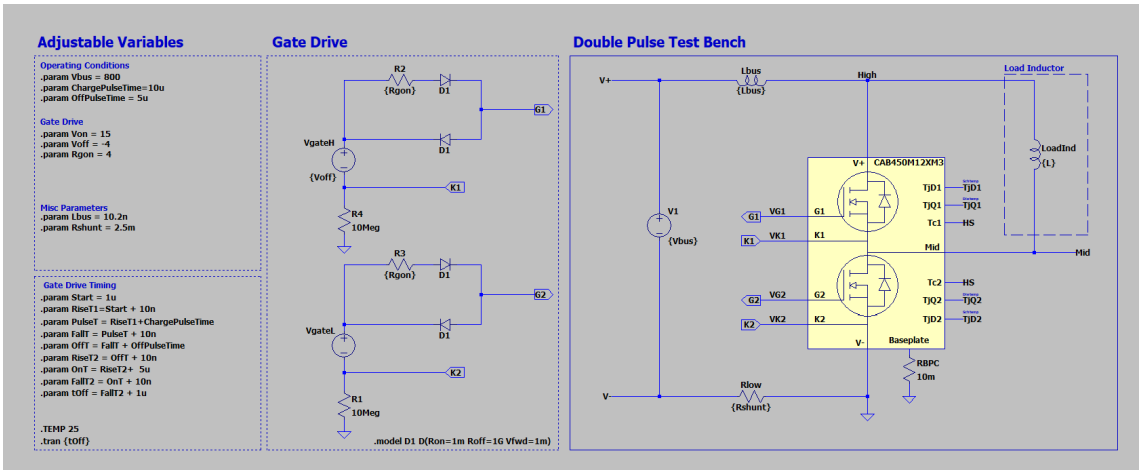

Figure 3.1: DPT

The setup includes adjustable parameters such as the bus voltage, gate drive voltage, and gate resistance. The circuit consists of a gate drive section, which controls the turn-on and turn-off of the MOSFETs, and the main test bench, where the device under test (DUT) is subjected to double pulse switching events.

In the LTspice simulation, the SiC module's upper switch is kept in the off state at all times, while the lower switch is subjected to a DPT. During the simulation, the load inductance is adjusted to achieve different load currents. However, in practical experiments, it is usually necessary to adjust the pulse width while keeping the load inductance constant to achieve different load currents.

Figure.3.2 shows the DPT working principle.

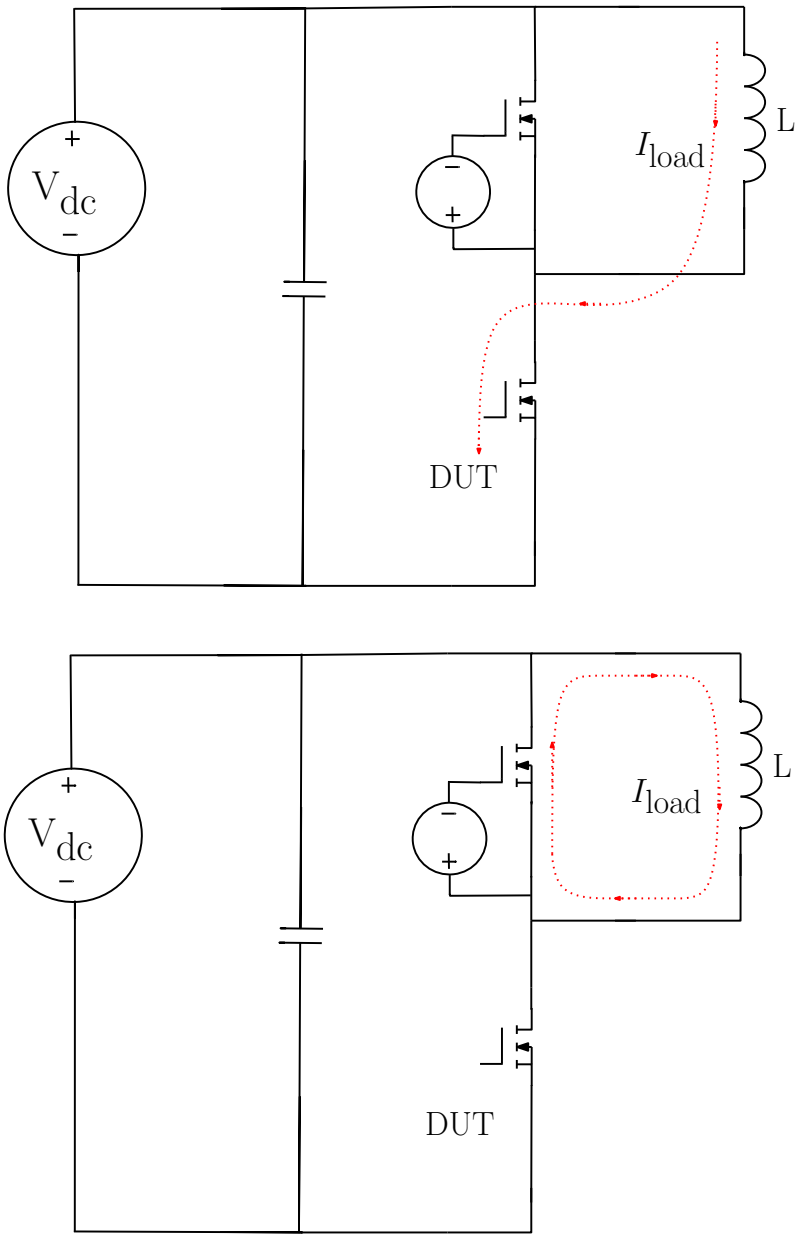

Figure 3.2: DPT Working Principle, Upper Figure:current accelerating; Lower Figure:current after turn-off, and before turn-on

Figure.3.2 shows that initially, the drive circuit generates the first pulse, which turns on the device under test (DUT). At this point, current begins to accumulate in the inductance, establishing a current path. After the first pulse ends, the DUT is turned off, allowing the off-state characteristics of the device to be measured. During the off period of the first pulse, the current in the inductance remains constant (assuming that the energy stored in the inductance does not significantly dissipate). Subsequently, the driver emits a second pulse, causing the DUT to turn on again. At this stage, the current in the inductance continues to flow, and the turn-on characteristics of the DUT can be measured during the onset of the second pulse.

Figure.3.3 shows the gate voltage pulse waveform of the DPT as well as the waveform

when the load current I_{load} is 450A.

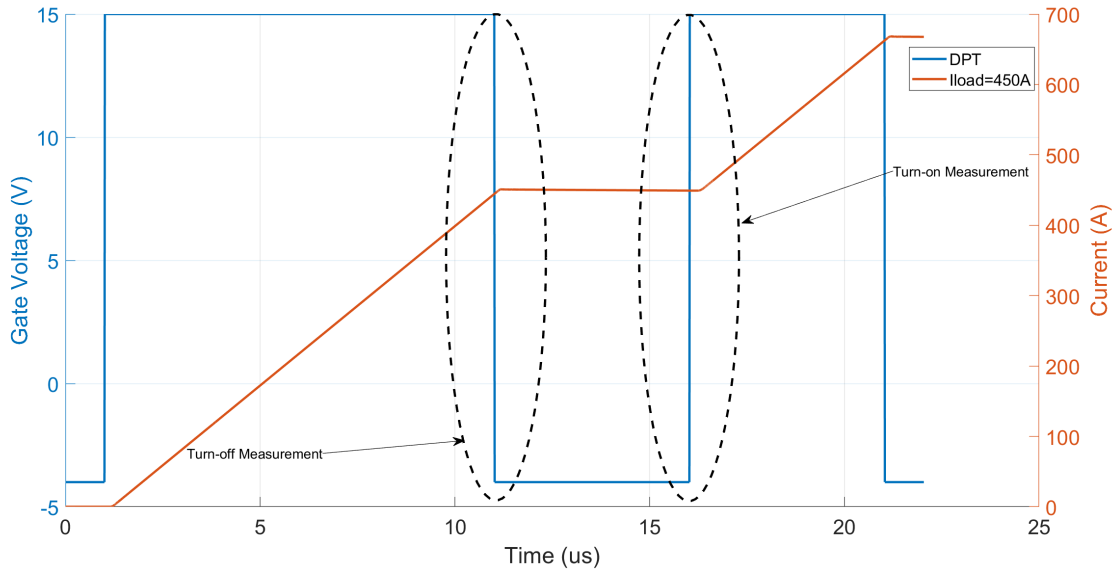

Figure 3.3: DPT Pulse and Load Current $I_{\text{load}} = 450\text{A}$

As shown in Figure.3.3, the SiC MOSFET turn-off process can be measured at the moment indicated by the first dashed ellipse, while the SiC MOSFET turn-on process occurs at the moment indicated by the second dashed ellipse. During the first high-level pulse, known as the charge pulse time, the load current begins to rise. Once it reaches the desired value, the pulse transitions from high to low. During the off pulse time, the load current is maintained at the desired value, which in this example is 450A.

Table 3.1 displays the parameters used in DPT simulation.

Table 3.1: DPT Parameters used in LTspice

Parameters	**Value**
Stray Inductance	10.2nH
Shunt Resistor	2.5mΩ
Gate Drive Voltage	-4V/+15V
Turn-on Gate Resistor	4Ω
DPT Charge Pulse Time	10μs
DPT Off Pulse Time	5μs
DPT Pulse Raise Time	10ns
DPT Pulse Fall Time	10ns
Transistor type	SiC MOSFET from Wolfspeed(CAB450M12XM3)

Table 3.2 shows the load inductance used in DPT simulation.

Table 3.2: Load Inductance used in DPT Simulation

Load Current	Inductance
25A	320μH
50A	160μH
75A	106.6μH
100A	79.6μH
150A	53.1μH
200A	39.8μH
250A	31.8μH
300A	26.5μH
350A	22.7μH
400A	19.8μH
450A	17.6μH

The inductance values used for measuring the original setup are shown in Table 3.2. It can be observed that changes in load inductance lead to variations in load current. An alternative would have been to use various times for the current accelerating and using the same load inductance. In the DPT simulation, when measuring the effects of different gate resistor values, multi-step gate drive pulses, and snubber circuits on the turn-off process based on the original setup, there are very slight differences in the load inductance around the values in Table 3.2 to achieve the corresponding load current. This also suggests that in practical experiments, adjusting the pulse width rather than the load inductance is a more practical and reasonable approach.

3.2 Drive System

Figure.3.4 shows the simulation of the drive system built in PLECS.

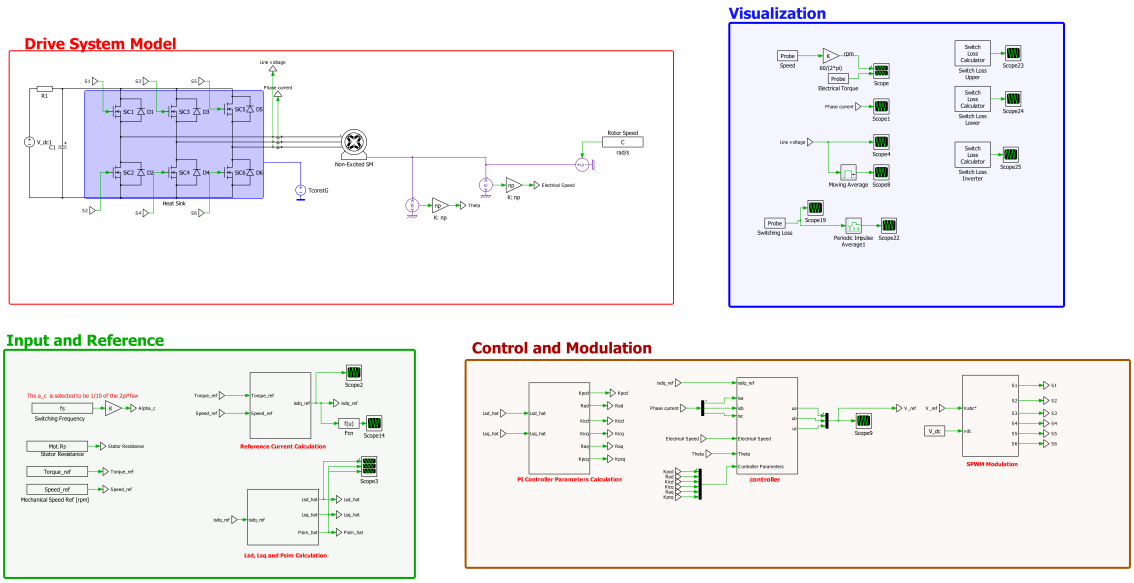

Figure 3.4: Drive System

The drive system consists of a battery, a three-phase SiC-based inverter, and a motor. The battery is simulated using a DC voltage source, and the SiC model from Wolfspeed is imported into the PLECS library's MOSFET model for the inverter side. The motor is modeled by importing FEM data (i.e. look-up table for I_d,I_q,ψ_d,ψ_q, the inductance is calculated from the flux linkage data) into the non-excited synchronous machine model in PLECS.

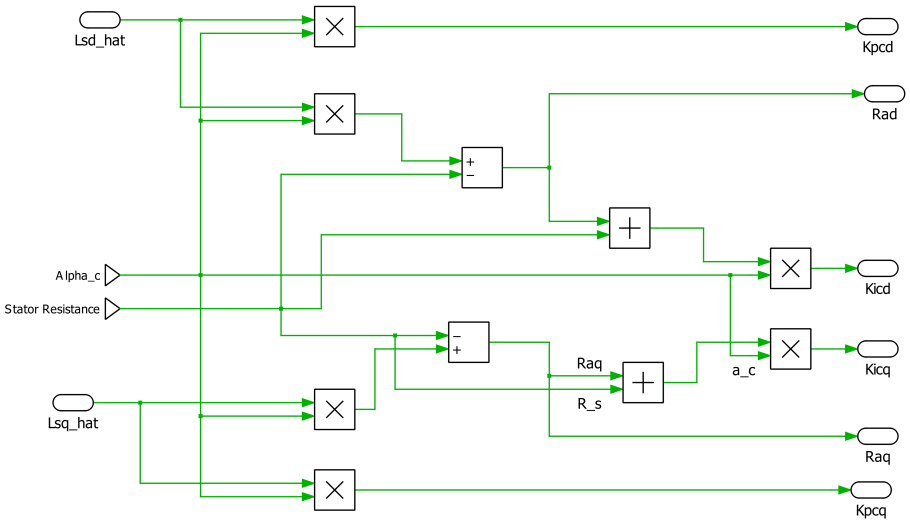

Figure 3.5: PI Controller Parameters Calculation

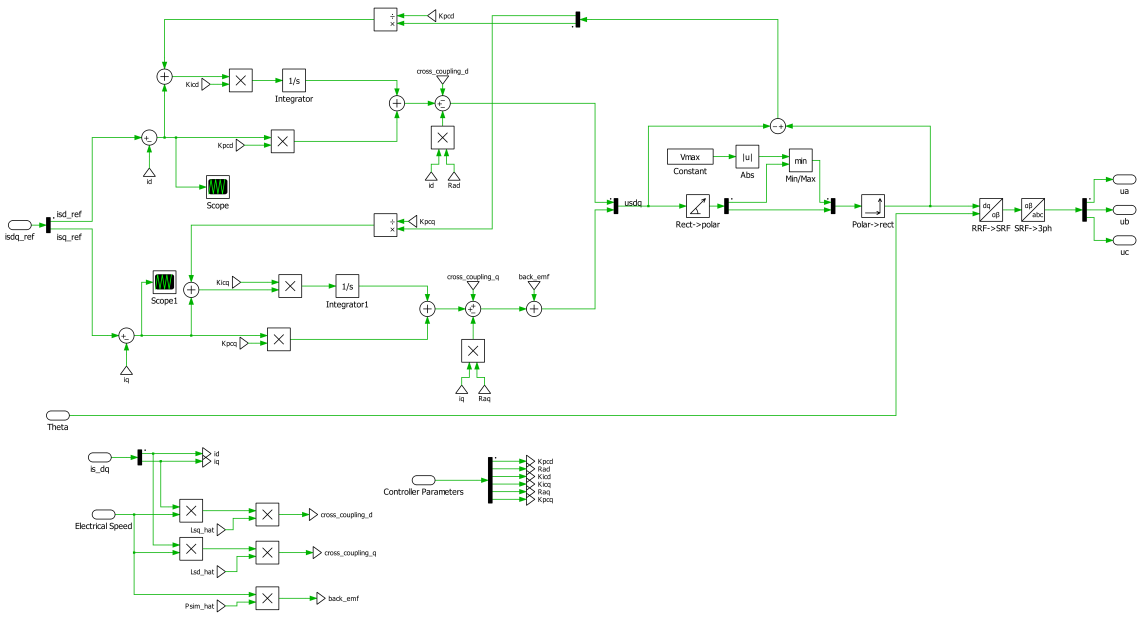

Figure 3.6: Current Controller

The control part employs a current controller. With reference speed and torque as inputs, the reference current is calculated based on the imported LUT[2]. Based

on the obtained reference current, and using the imported LUT, the necessary values of L_d, L_q, and ψ_m required for the controller design can be determined. The calculation of the controller parameters and the simulation block diagram of the current controller are shown in Figure.3.5 and Figure.3.6, respectively. The reference voltage signal output from the controller is fed into the modulation module, which then generates the switching signals for controlling the three-phase inverter[2].

In the simulation, a speed controller is not used; instead, the motor is maintained at the reference speed. The modulation technique employed is SPWM.

Table 3.3 displays the parameters used in drive system simulation.

Table 3.3: Drive system parameters used in PLECS

Parameters	**Value**
Stator resistance	0.046 Ω
Stator leakage inductance	9.4 μH
Number of pole pairs	4
Transistor type	SiC MOSFET from wolfspeed(CAB450M12XM3)
Switching frequency	10 kHz
DC voltage source	800 V
Machine	Non-excited synchronous machine with lookup tables
DC Capacitor	800uF
Temperature	25 °C

Figure 3.7, Figure 3.8, and Figure 3.9 show the distribution of the power factor, modulation ratio, and the peak value of the inverter output current.

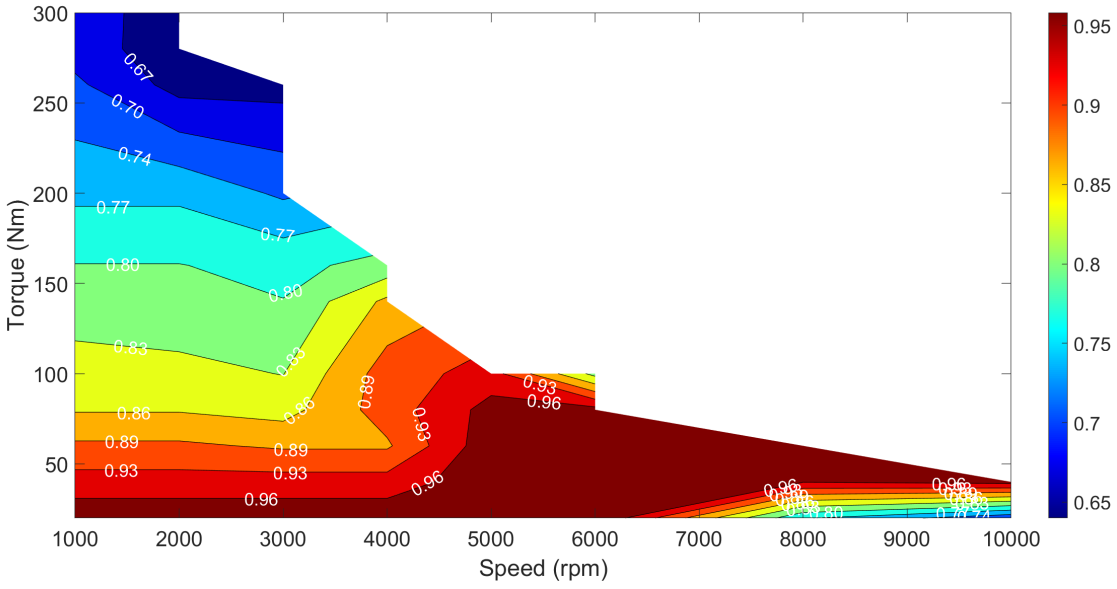

Figure 3.7: The distribution of the power factor in the drive region

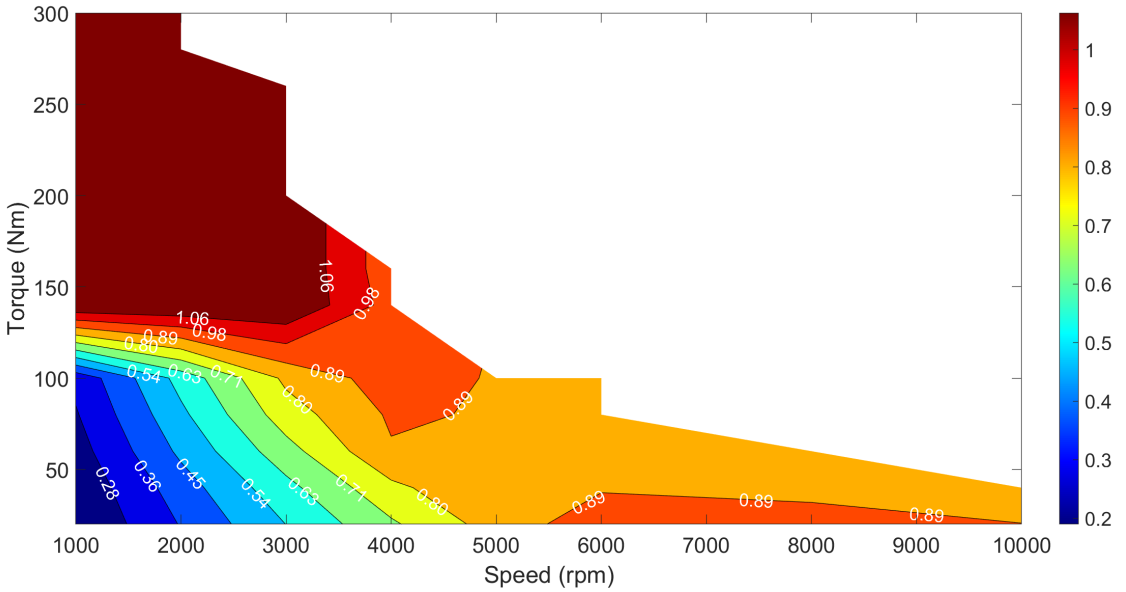

Figure 3.8: The distribution of the modulation ratio in the drive region

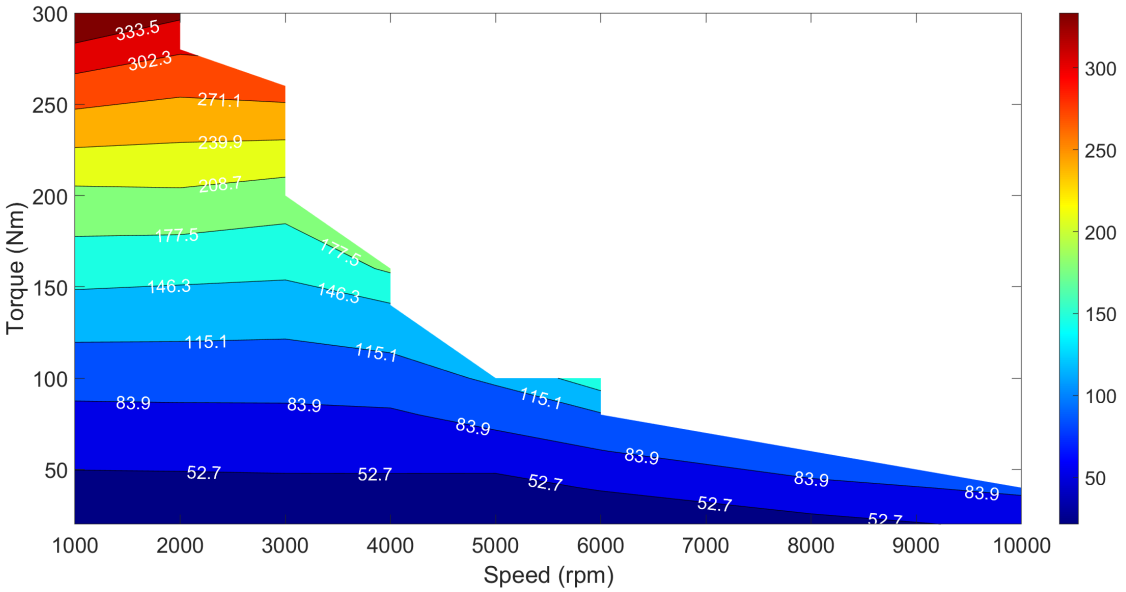

Figure 3.9: The distribution of the peak inverter output current in the drive region

4

Methodology

This section introduces three different methods that influence the turn-off process. The DPT simulation in LTspice is conducted using these three methods to generate different LUTs.

4.1 Gate Resistance Set-up

The gate drive circuit is shown as Figure.4.1.

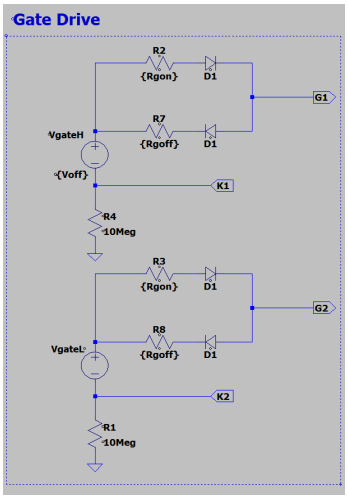

Figure 4.1: Gate Drive Circuit

To study the impact of R_g on the turn-off process, an LTspice simulation was conducted with R_{gon} consistently set to 4 Ω, and R_{goff} set to 0, 2, 4, and 8 Ω, respectively, for the DPT.

4.2 Multi-step Gate Drive Pulse with Varying Magnitude and Duration

In LTspice, the PWL function can be used to set different pulses. In experiments, the generation of multi-step gate drive pulses is often achieved using Active Gate Drivers (AGD). The switching process can also be affected by the different types of switches used in AGD.

This thesis only considers the impact of multi-step gate drive pulses on SiC MOSFETs and does not take into account the additional losses generated by AGD.

During the turn-off process, the DPT simulation sets the gate drive voltage (V_{GG}) to have a voltage amplitude step at specific moments (e.g., when V_{ds} rises to 90% V_{dc}). The multi-step pulse is maintained for a specific duration. This method simulates the impact of current slew rate on the turn-off switching process.

Fig.4.2 and Fig.4.3 display the V_{GG} with different voltage steps at various durations when I_{ds} = 100A and I_{ds} = 400A, respectively.

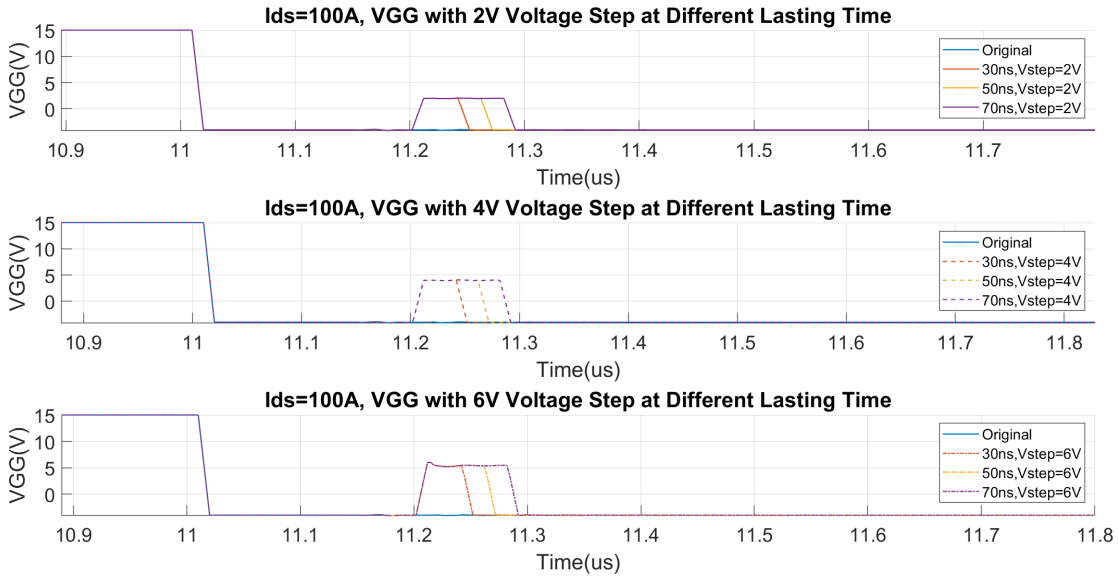

Figure 4.2: I_{ds}=100A, V_{GG} with Different Voltage Step at Different Lasting Time

Figure 4.3: I_{ds}=400A, V_{GG} with Different Voltage Step at Different Lasting Time

To investigate the impact of varying magnitudes and duration of the multi-step pulse on V_{ds}, I_{ds}, and turn-off energy, the DPT simulation is performed at two different current levels, 100A and 400A, with V_{dc} set to 800V. The applied gate drive pulse V_{GG} shown in Figure.4.2 and Figure.4.3 show that V_{ds} reaches 90% of V_{dc} a little bit quickly at a current of 400A compared to 100A. At 100A, the intermediate step pulse rises at approximately 11.2µs, whereas at 400A, the intermediate step pulse rises earlier than 11.2 µs

Fig.4.4 and Fig.4.5 display the V_{ds} with different voltage steps at various durations when I_{ds} = 100A and I_{ds} = 400A, respectively.

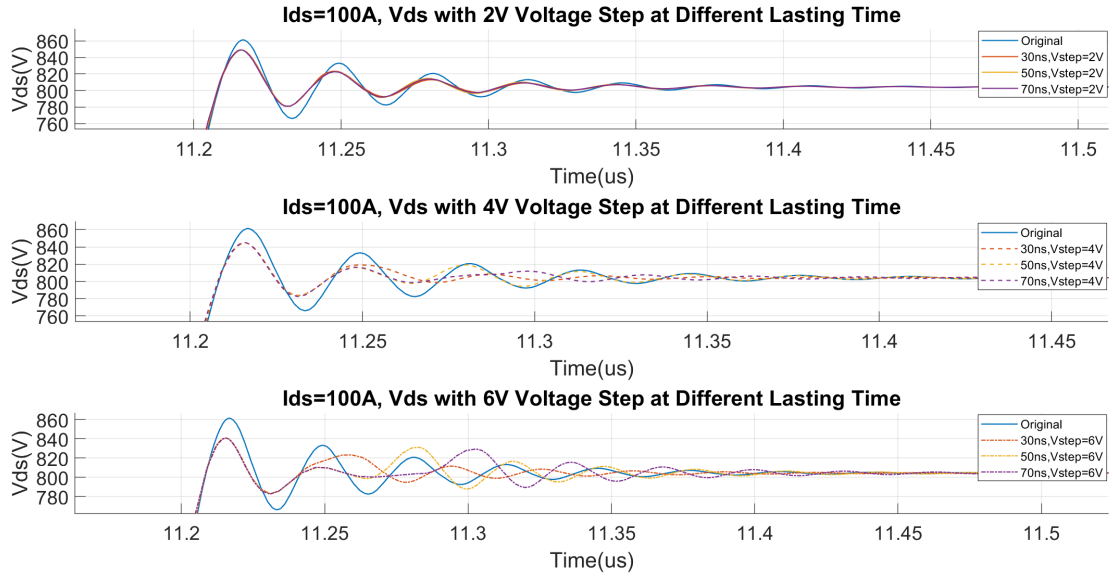

Figure 4.4: I_{ds}=100A, V_{ds} with Different Voltage Step at Different Lasting Time

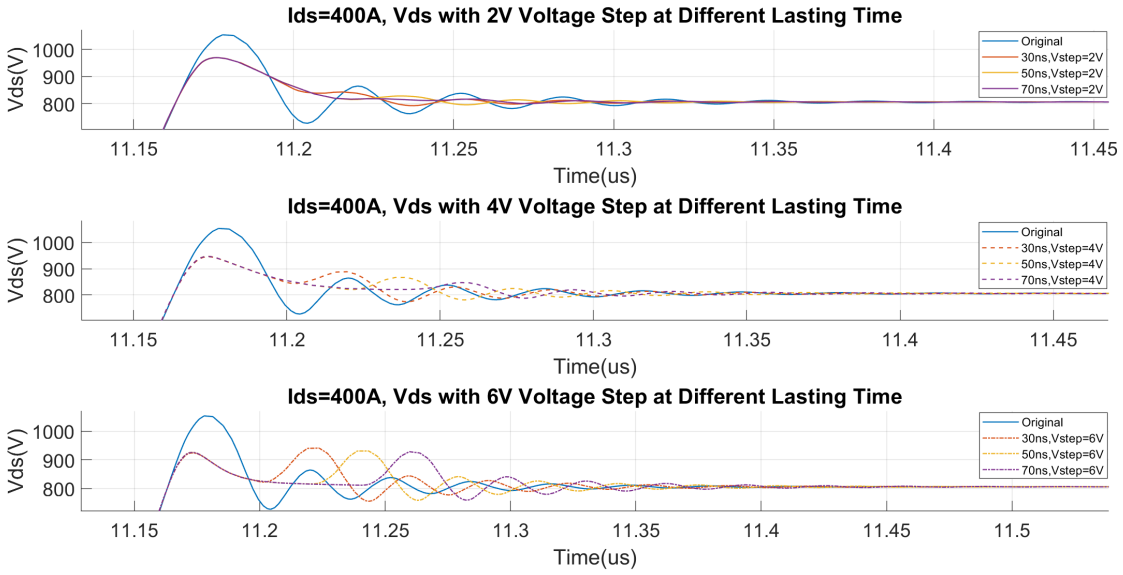

Figure 4.5: I_{ds}=400A, V_{ds} with Different Voltage Step at Different Lasting Time

From Figure.4.4, it can be noted that under relatively low current conditions (100A), the application of a multi–step gate drive pulse, compared to the original circuit, results in decreased voltage overshoot. The higher the magnitude of the step pulse, the lower the resulting voltage.The V_{ds} oscillation magnitude under the 2V and 4V step voltages decreases compared to the original setup.

However, when the step pulse magnitude increases to 6V, the oscillation magnitude of V_{ds} before reaching a steady state shows no significant difference compared to the original setup. Regarding the effect of step duration, it does not have a noticeable impact at 2V and 4V, but at 6V, as the step duration increases, the onset of oscillation is delayed. This indicates that with a longer step duration, V_{ds} requires more time to reach a steady state.

As shown in Figure 4.5, I_{ds} at a higher current (400A) exhibits some differences compared to its behavior at 100A. Specifically, the extent of the voltage overshoot reduction, as indicated by Vpeak/Vdc, is greater than at 100A. Additionally, the oscillation at 4V and 6V step voltages increases, and the effect of step duration at 4V is more pronounced than at 100A.

Fig.4.6 and Fig.4.7 display the I_{ds} with different voltage steps at various durations when I_{ds} = 100A and I_{ds} = 400A, respectively.

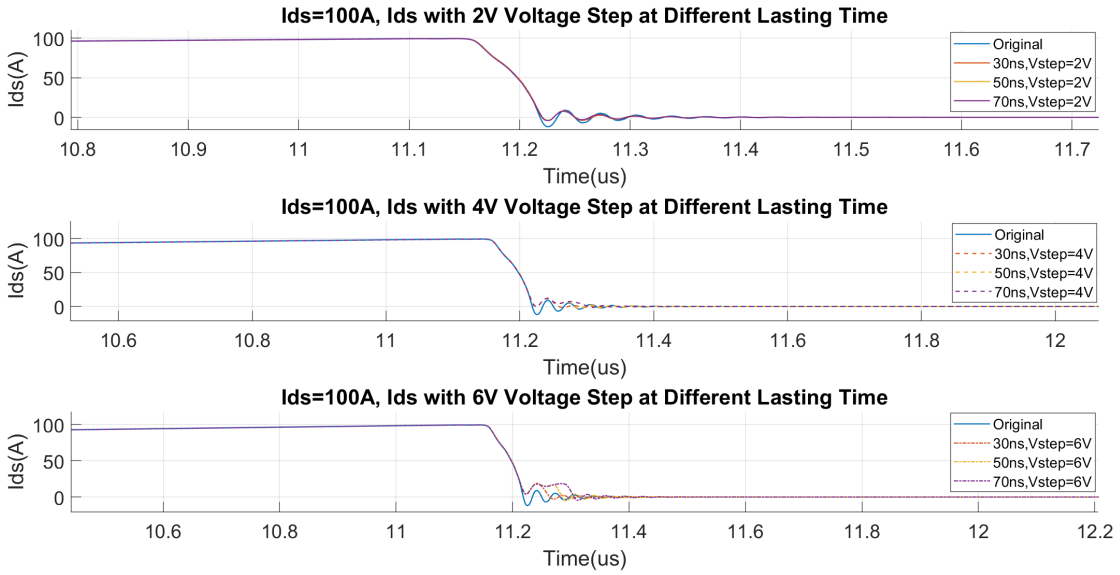

Figure 4.6: I_{ds}=100A, I_{ds} with Different Voltage Step at Different Lasting Time

At 100A, as shown in Figure.4.6,the current slew rate of Ids under different step voltage magnitudes shows no noticeable difference compared to the original circuit. This is because when V_{ds} rises to 90% of V_{dc} , the drive pulse V_{GG} starts to increase, and by that time, Ids has already decreased to a relatively low value.

Therefore, with small step voltages of 2V and 4V, the V_{GG} pulse primarily serves to reduce oscillations. In the case of a relatively higher 6V step voltage, the V_{GG}

pulse causes Ids to maintain a nearly constant current value when the oscillation just begins, for a duration that closely matches the step pulse. This also explains why, for the 6V step voltage, the onset of the V_{ds} oscillation is delayed further as the duration of the step pulse increases.

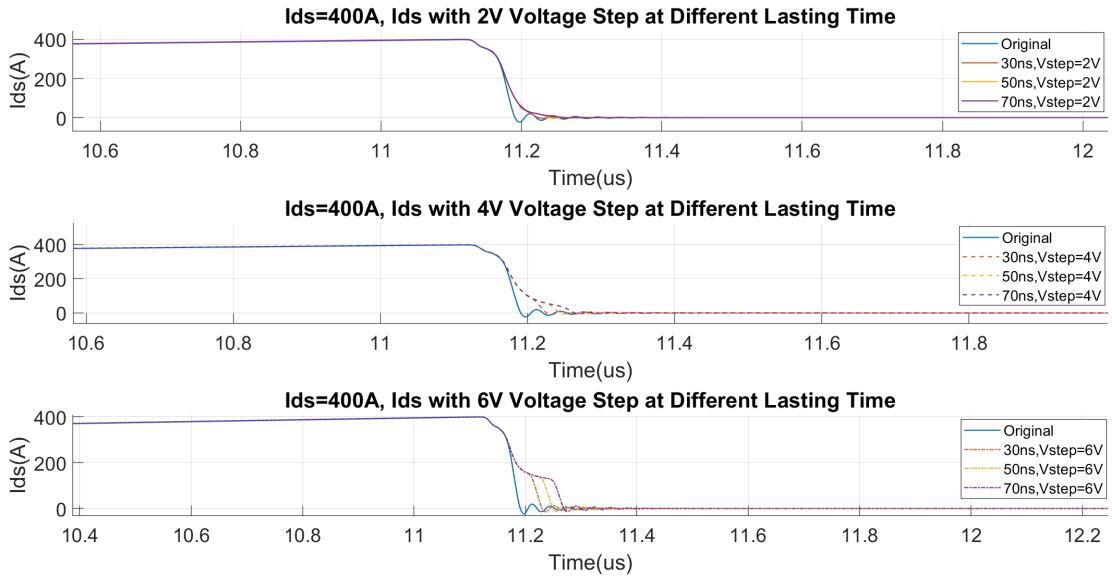

Figure 4.7: I_{ds}=400A, I_{ds} with Different Voltage Step at Different Lasting Time

Figure.4.7 displays that the current slew rate becomes flatter as the step voltage magnitude increases at 400A. The reason is that when V_{ds} rises to 90% of V_{dc}, I_{ds} has only dropped to around 280A. Thus, the step voltage plays a role in adjusting the current slew rate. This also explains why the reduction in voltage overshoot is more significant at 400A. The duration of the pulse does not have a noticeable effect on the current slew rate; it only delays the onset of V_{ds} oscillation. The reason why the V_{ds} oscillation increases at 4V and 6V is that the larger step pulses cause a step-like decrease in current, leading to higher V_{ds} oscillations.

Fig.4.8 and Fig.4.9 show the turn-off P_{loss} with different voltage steps at various durations when I_{ds} = 100A and I_{ds} = 400A, respectively. As shown in Figure.4.8, regarding turn-off losses, at a current of 100A, the difference in losses between the 2V step voltage and the original circuit is not significant, with only minor differences during the oscillation phase. However, as the step voltage magnitude and pulse duration increase, the losses during the oscillation phase also increase compared to the original circuit.

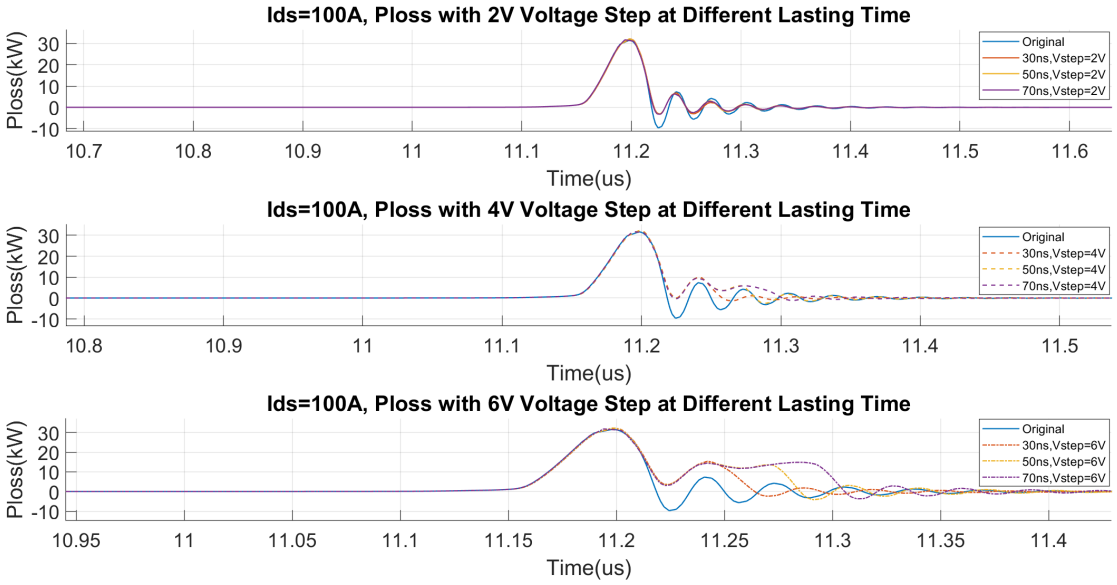

Figure 4.8: I_{ds}=100A, P_{loss} with Different Voltage Step at Different Lasting Time

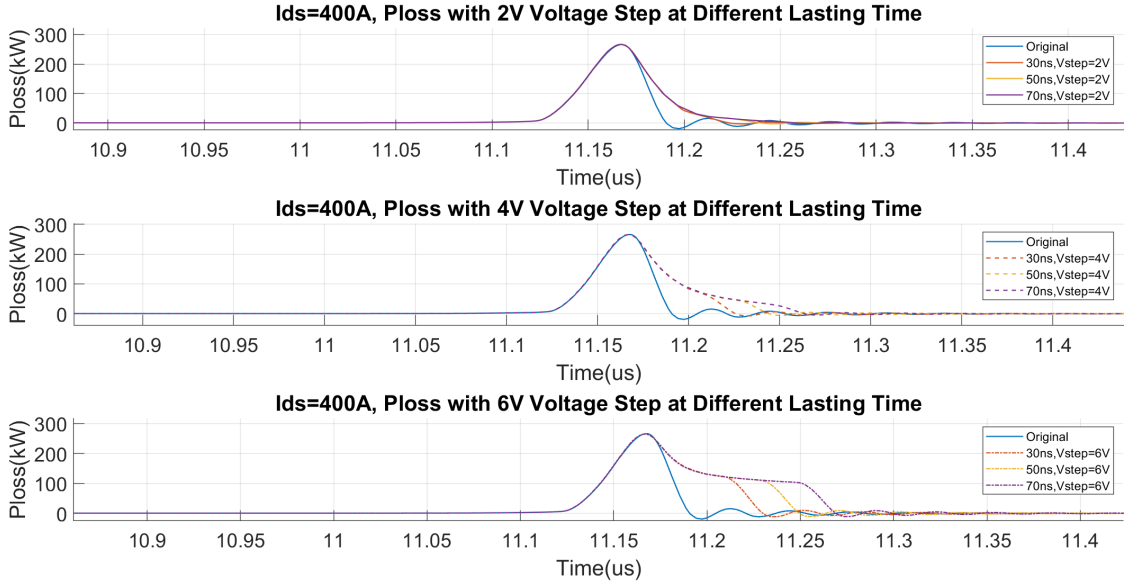

Figure 4.9: I_{ds}=400A, P_{loss} with Different Voltage Step at Different Lasting Time

When the current is 400A, as illustrated in Figure.4.9, the step voltage reduces the current slew rate, leading to increased losses. Additionally, as the step voltage duration increases, the losses further increase. In summary, the analysis section selects the 2V step voltage magnitude with a 30ns duration, which results in the lowest losses, to compare with other approaches.

4.3 Snubber Circuit

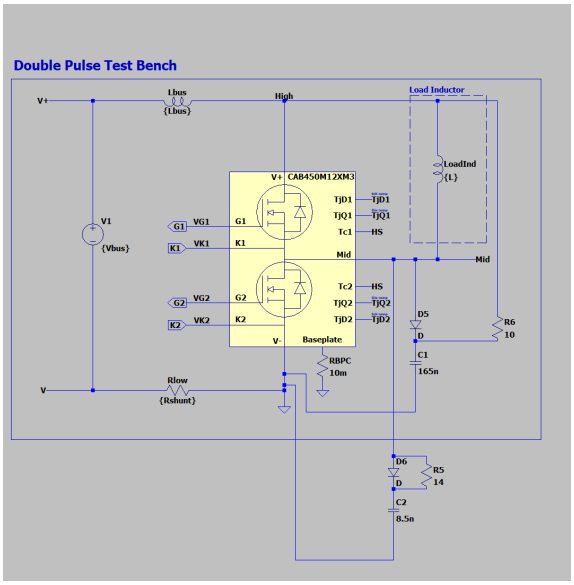

Figure 4.10: Snubber Circuit

The turn-off snubber and overvoltage snubber are used to reduce turn-off losses and voltage overshoot, as shown in Figure 4.10. The selection of the capacitor and resistor values is based on the maximum V_{ds} and I_{ds} that the Cree SiC module can withstand. The current fall time during turn-off is set to an average value of 44 ns.

The turn-off snubber capacitor and resistor can be calculated as

$$C_{\mathrm{s}} = \frac{I_{\mathrm{ds}} \cdot t_{\mathrm{fi}}}{2 \cdot V_{\mathrm{ds}}} = \frac{450\mathrm{A} \cdot 44\mathrm{ns}}{2 \cdot 1200\mathrm{V}} = 8.25\mathrm{nF} \tag{4.1}$$

$$R_{\mathrm{s}} = \frac{V_{\mathrm{ds}}}{0.2 \cdot I_{\mathrm{ds}}} = \frac{1200\mathrm{V}}{0.2 \cdot 450\mathrm{A}} = 13.33\Omega \tag{4.2}$$

Based on the calculation results, the turn-off snubber capacitor C_{s} is selected as 8.5 nF, and the resistor R_{s} is chosen as 14 Ω, giving

$$t_{\mathrm{on}} > 2.3 \cdot R_{\mathrm{s}} \cdot C_{\mathrm{s}} = 2.3 \cdot 14\mathrm{nF} \cdot 8.5\Omega = 273.7\,\mathrm{ns} \tag{4.3}$$

The drive system's switching frequency is 10 kHz, providing ample time for the turn-off snubber to release its energy.

The overvoltage snubber capacitor is determined as

$$C_{\text{ov}} = \frac{100 \cdot k \cdot I_{\text{ds}} \cdot t_{\text{fi}}}{V_{\text{ds}}} = \frac{100 \cdot 0.1 \cdot 450\text{A} \cdot 44\text{ns}}{1200\text{V}} = 165\text{nF} \tag{4.4}$$

If the overvoltage snubber resistor is considered to be 10Ω, the following calculations determine the t_{on},

$$t_{\text{on}} > 2.3 \cdot R_{\text{ov}} \cdot C_{\text{ov}} = 2.3 \cdot 165\text{nF} \cdot 10\Omega = 3795\,\text{ns} \tag{4.5}$$

Therefore, this selection still provides sufficient time to release the energy stored in the overvoltage snubber before the next turn-off.

5

Analysis part

This section first compares the changes in slew rate, voltage overshoot, and switching losses under 800V DC link voltage using different methods based on the LUTs obtained from DPT simulations in LTspice. Secondly, the LUTs of switching energy for various methods are imported into PLECS, where the entire drive system is modeled to obtain the distribution of switching losses within the drive region. Finally, a comparative analysis is performed based on the LUTs derived from DPT simulations under different DC link conditions.

5.1 Analysis of Slew Rate During Turn-off at 800V DC Link

Fig. 5.1 illustrates the impact of different methods on the voltage slew rate during the turn-off process at $V_{\mathrm{ds}} = 800\,\mathrm{V}$.

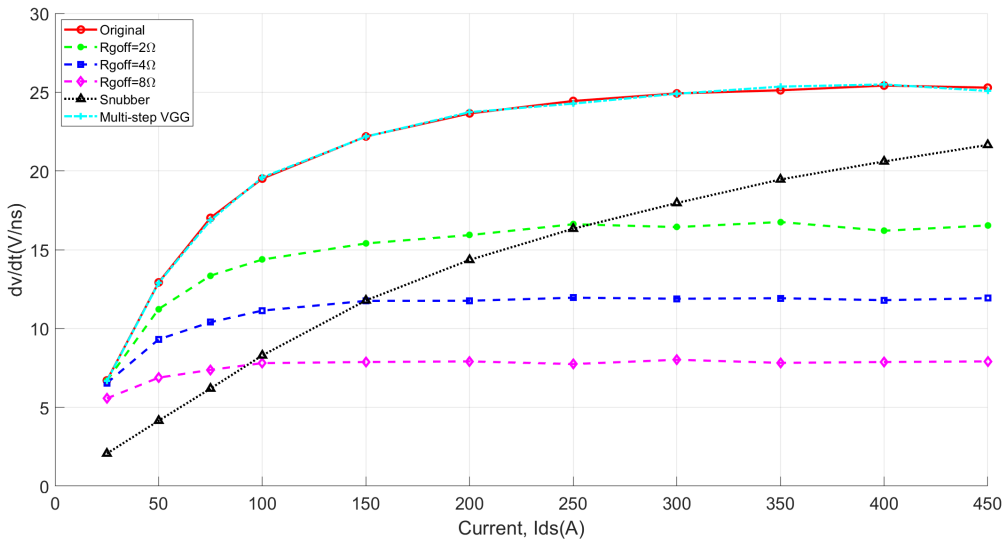

Figure 5.1: Comparison of the effects of different methods on the voltage slew rate during the turn-off at $V_{ds} = 800V$

Under the original conditions, the voltage slew rate increases rapidly when the current I_{ds} is below approximately 100 A, and then it increases more slowly, becoming relatively constant at 25 V/ns after $I_{\mathrm{ds}} = 250\,\mathrm{A}$.

For the R_{goff} effect, it is evident that as the R_{goff} increases, the voltage slew rate decreases compared to the original condition. When I_{ds} is below approximately 100 A, the voltage slew rate increases quickly, but the rate of increase reduces as the gate resistance value increases. Beyond $I_{\text{ds}} = 100\,\text{A}$, the slew rates at $R_{\text{goff}} = 2\,\Omega$, $4\,\Omega$, and $8\,\Omega$ stabilize at approximately 16 V/ns, 12 V/ns, and 8 V/ns, respectively.

Regarding the snubber circuit, it generally reduces the slew rate compared to the original condition, but the voltage slew rate still increases as the current increases. For the Multi-step V_{GG}, the voltage slew rate remains essentially the same as the original condition, as expected.

Fig. 5.2 displays the impact of different methods on the current slew rate during the turn-off process at $V_{\text{ds}} = 800\,\text{V}$.

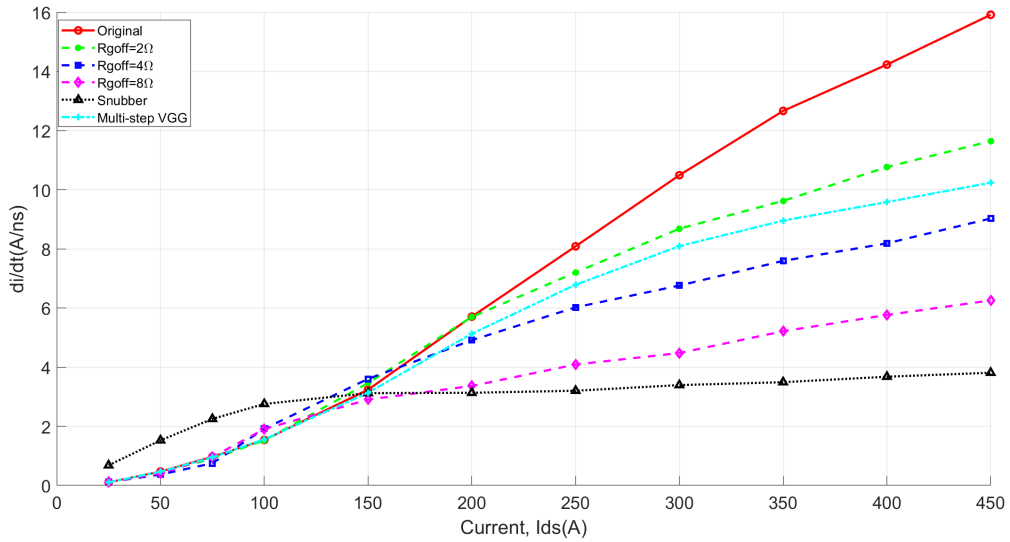

Figure 5.2: Comparison of the effects of different methods on the current slew rate during the turn-off at $V_{ds} = 800V$

As shown in Fig. 5.2, the current slew rate increases under all conditions as the current increases. R_{g} and a Multi-step V_{GG} have essentially the same effect on the current slew rate as the original circuit when the current I_{ds} is below 150 A. However, the snubber circuit results in a slightly higher current slew rate within this current range. When the current exceeds 150 A, the application of gate resistance leads to a reduction in the current slew rate compared to the original condition, with higher gate resistance values resulting in lower current slew rates. Beyond 150 A, the Multi-step V_{GG} causes a little bit lower current slew rate compared to $R_{\text{g}} = 2\,\Omega$. Among these conditions, the snubber circuit achieves the lowest current slew rate when the current is above 150 A.

5.2 Analysis of Voltage Overshoot During Turn-off at 800V DC Link

Fig. 5.3 illustrates the effects of different methods on reducing voltage overshoot.

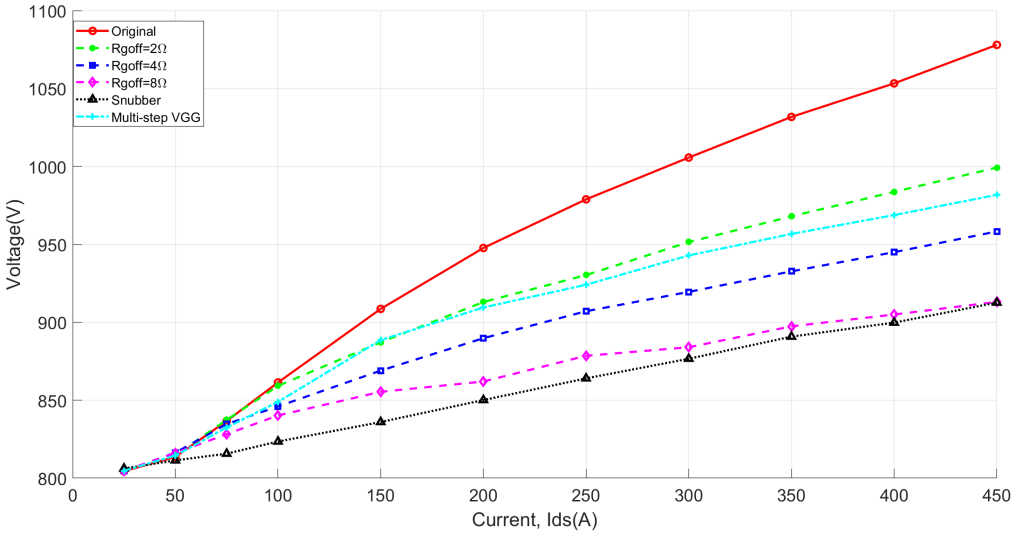

Figure 5.3: Comparison of the effects of different methods on the voltage overshoot during the turn-off at $V_{ds} = 800V$

The most effective method is the snubber circuit. For gate resistance, the reduction in voltage overshoot corresponds to the gate resistance value; the higher the R_{goff}, the lower the voltage overshoot. The Multi-step V_{GG} reduces voltage overshoot slightly more than $R_{goff} = 2\Omega$.

From Fig. 5.1 and Fig. 5.2, it can be observed that the Multi-step V_{GG} method results in the same voltage slew rate as the original circuit. However, as the current increases, it achieves a lower current slew rate. As shown in Fig. 5.3, the voltage overshoot when using the Multi-step V_{GG} method is lower than under the original conditions, illustrating that the current slew rate has a significant impact on the voltage overshoot as the current increases.

5.3 Analysis of Switching Losses at 800V DC Link

5.3.1 Switching Energy at Different Current

Fig. 5.4 shows the effects of different methods on turn-off switching energy. The turn-on switching energy are shown in Fig. 5.5.

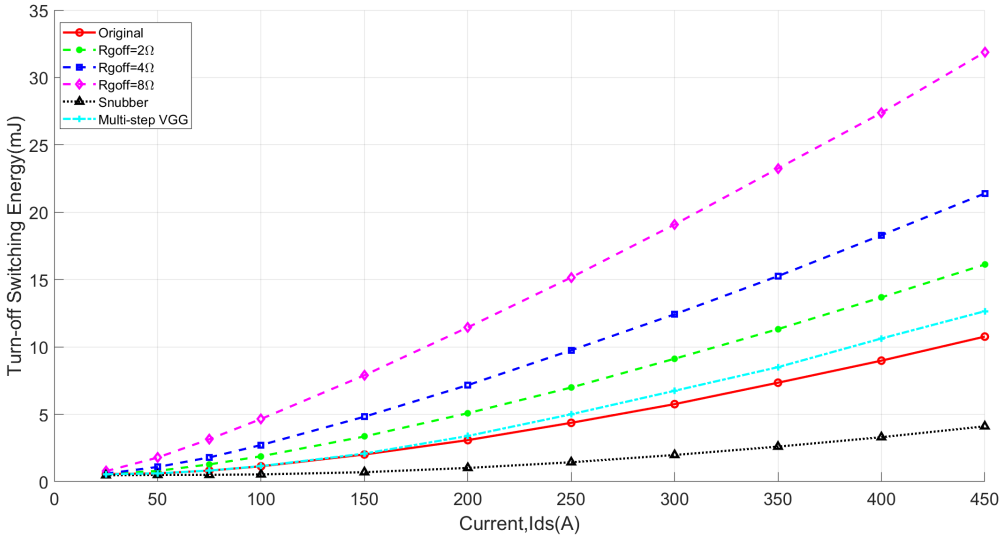

Figure 5.4: Comparison of the Effects of Different Methods on Turn-off Switching Energy at $V_{ds} = 800V$

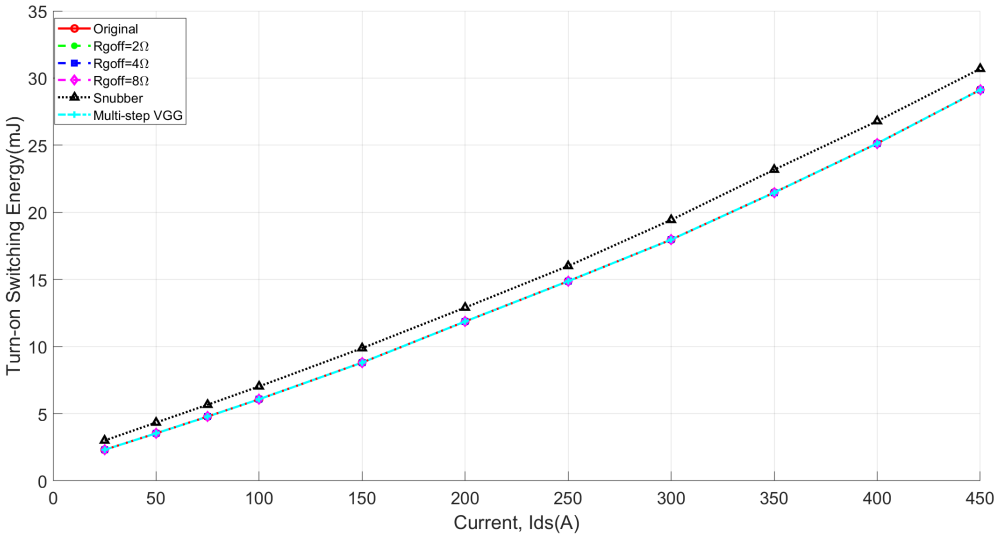

Figure 5.5: Comparison of the Effects of Different Methods on Turn-on Switching Energy at $V_{ds} = 800V$

It is noted that the snubber circuit can decrease turn-off switching energy compared to the original setup. The gate resistance leads to varying degrees of increase in turn-off switching energy; higher gate resistance results in higher turn-off switching energy. The Multi-step V_{GG} maintains similar turn-off switching energy to the original condition when the current is below around 150 A, and increases turn-off switching energy as the current rises. However, this increase is less than that caused by $R_g = 2, \Omega$. The snubber circuit results in higher turn-on switching energy compared to other methods. Since the turn-on gate resistance remains constant, varying the turn-off gate resistance does not affect the turn-on switching process. The Multi-

step V_{GG} is applied only during the turn-off period, so the turn-on switching energy remain unchanged.

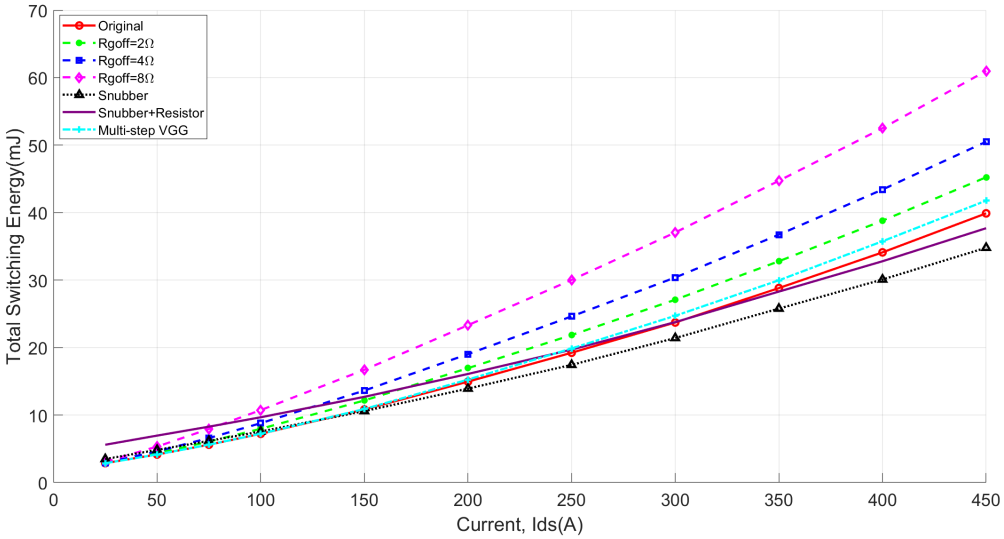

Figure 5.6: Comparison of the Effects of Different Methods on Total Switching Energy at $V_{ds} = 800V$

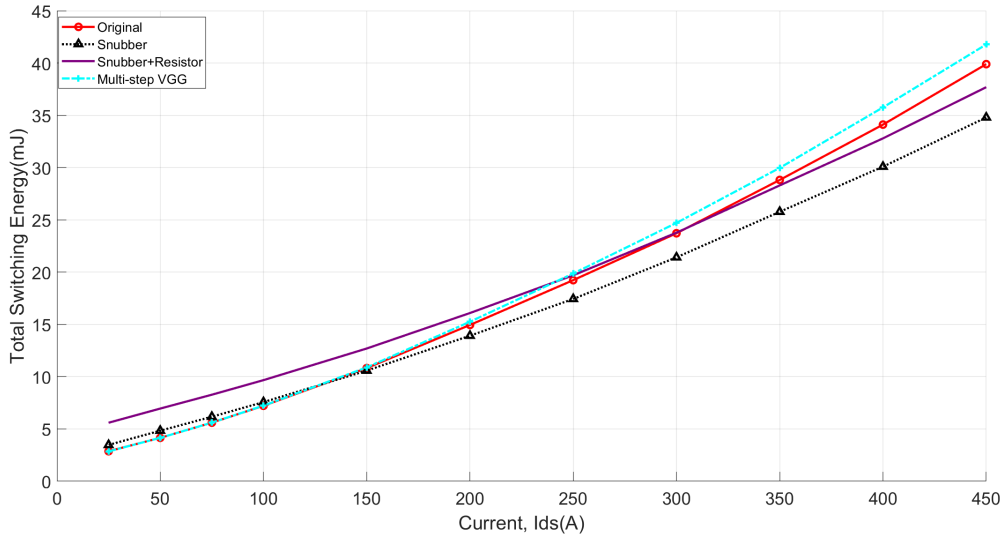

Figure 5.7: Comparison of the Effects of Snubber Circuit and Multi-step V_{GG} with Original Setup on Total Switching Energy at $V_{ds} = 800V$

From Fig. 5.6, it can be concluded that the turn-off gate resistor contributes to an increase in switching energy. A larger turn-off gate resistor results in greater switching energy. As shown in Fig. 5.7, the Multi-step V_{GG} method maintains nearly the same switching energy as the original setup when the current is below 150A, but it increases switching energy as the current rises. Nonetheless, the Multi-step V_{GG} method leads to a smaller increase in switching energy compared to using turn-off gate resistance alone, as observed in Fig. 5.6. Additionally, Fig. 5.7 shows that the

snubber circuit increases switching energy when the current is below approximately 100A. But, as the current increases, the snubber circuit becomes the most advantageous, as demonstrated in Fig. 5.6. Despite this advantage, when accounting for the losses of the snubber resistor, the overall losses—including the total switching losses of the transistor and the losses caused by the snubber resistor—tend to increase when the current is below approximately 300A. Nevertheless, as the current continues to rise, these losses eventually become lower than those in the original circuit.

5.3.2 Distribution of Losses in Drive Region

5.3.2.1 Turn-off Losses Distribution

Fig.5.8 displays the distribution of turn-off switching losses using different methods in the drive region. The switching frequency is 10kHz.

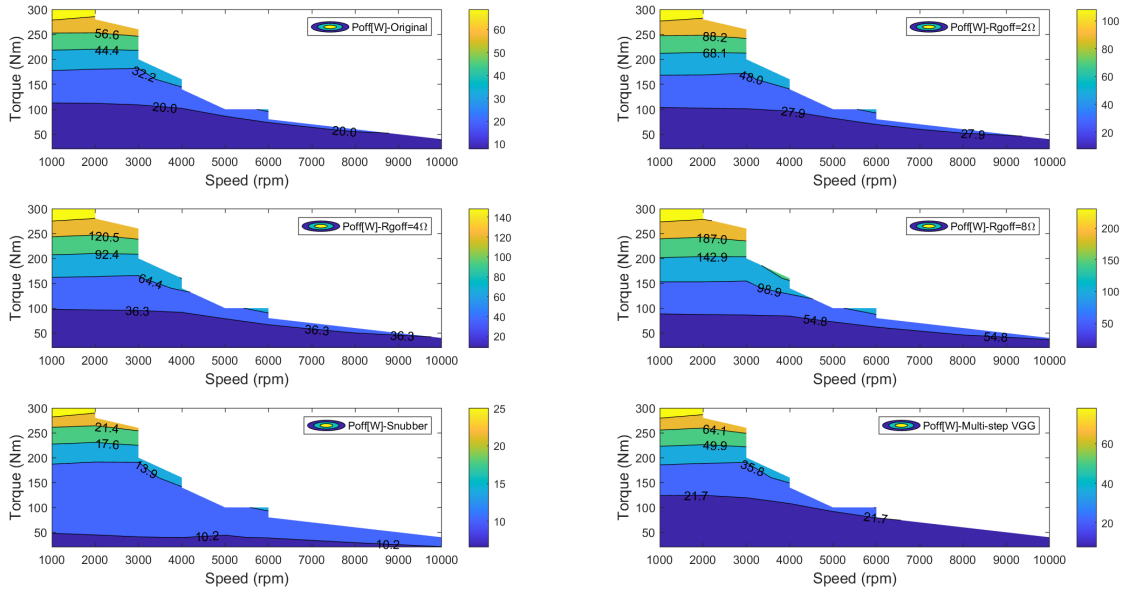

Figure 5.8: Distribution of Turn-off Losses in Drive Region Using Different Methods

From the color bar of each sub-figure in Fig 5.8, it can be observed that as R_{goff} increases, the turn-off losses also increase throughout the entire drive region. The multi-step V_{GG} method results in turn-off losses that are essentially the same as those of the original circuit in the drive region. The snubber circuit significantly reduces the turn-off losses in the drive region.

5.3.2.2 Switching Losses Distribution (Excluding Snubber Circuit Resistors)

Fig. 5.9 displays the distribution of total switching losses, excluding the losses caused by the snubber circuit resistors, using different methods in the drive region. The switching frequency is 10kHz.

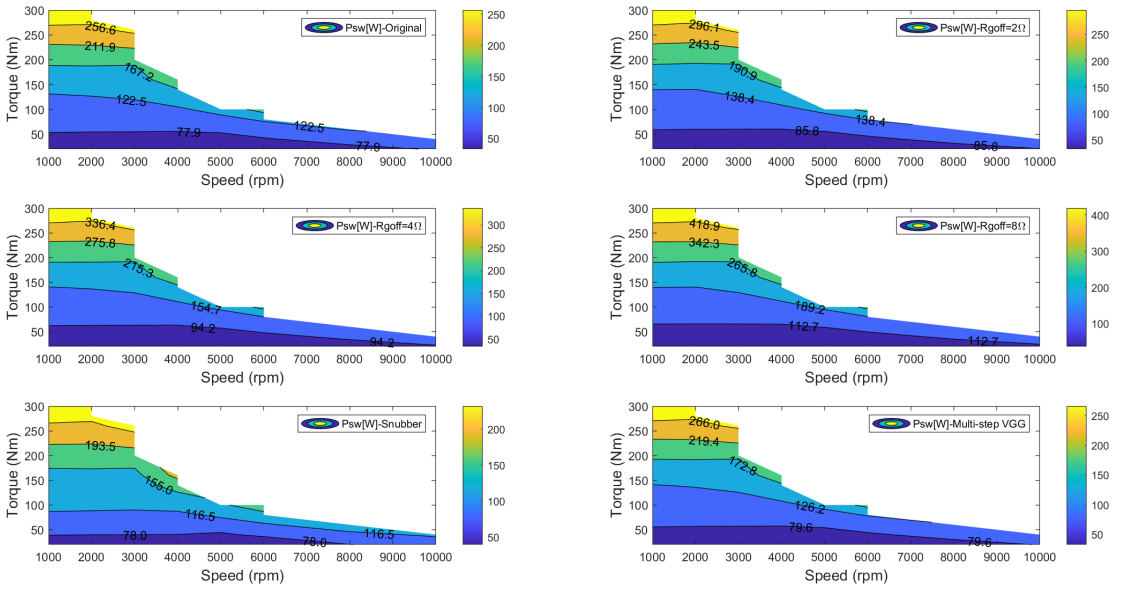

Figure 5.9: Distribution of Total Switching Losses in the Drive Region Using Different Methods (Excluding Snubber Circuit Resistor Losses)

From the color bar of each sub-figure in Fig 5.9, it can be observed that as R_{goff} increases, the total switching losses also increase throughout the entire drive region. The multi-step V_{GG} method results in total switching losses that are essentially the same as those of the original circuit in the drive region, though slightly higher. The snubber circuit reduces the switching losses as the torque increases.

The comparisons of total switching losses,excluding the losses caused by the snubber circuit resistors, using different methods in the drive region are shown in Fig. 5.10 and Fig. 5.11.

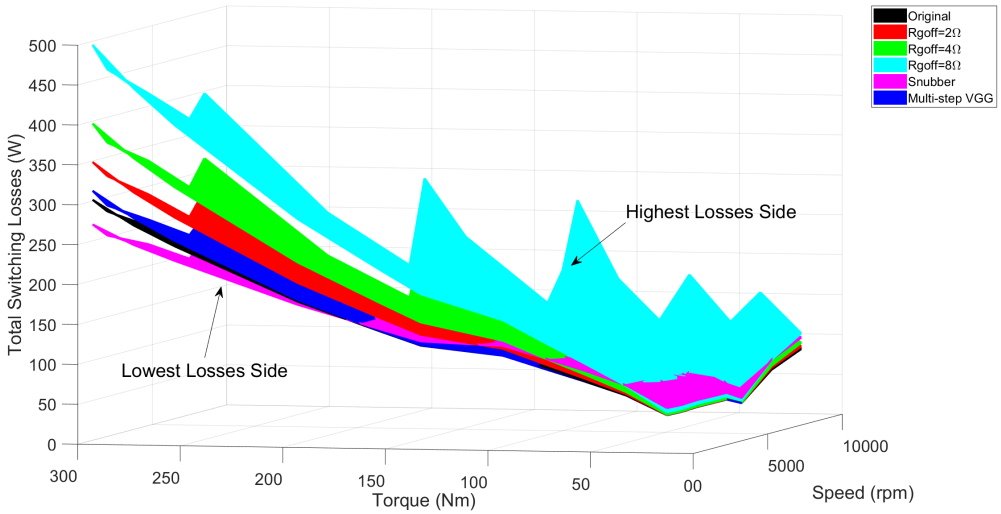

Figure 5.10: Comparisons of Total Switching Losses Under Different Methods in Drive Region–Highest Losses Side (Excluding Snubber Circuit Resistor Losses)

In Fig.5.10, it can be observed that when the output torque is below approximately 50 Nm, and the speed is around 5000 rpm, the snubber circuit results in relatively a little bit higher total switching losses.

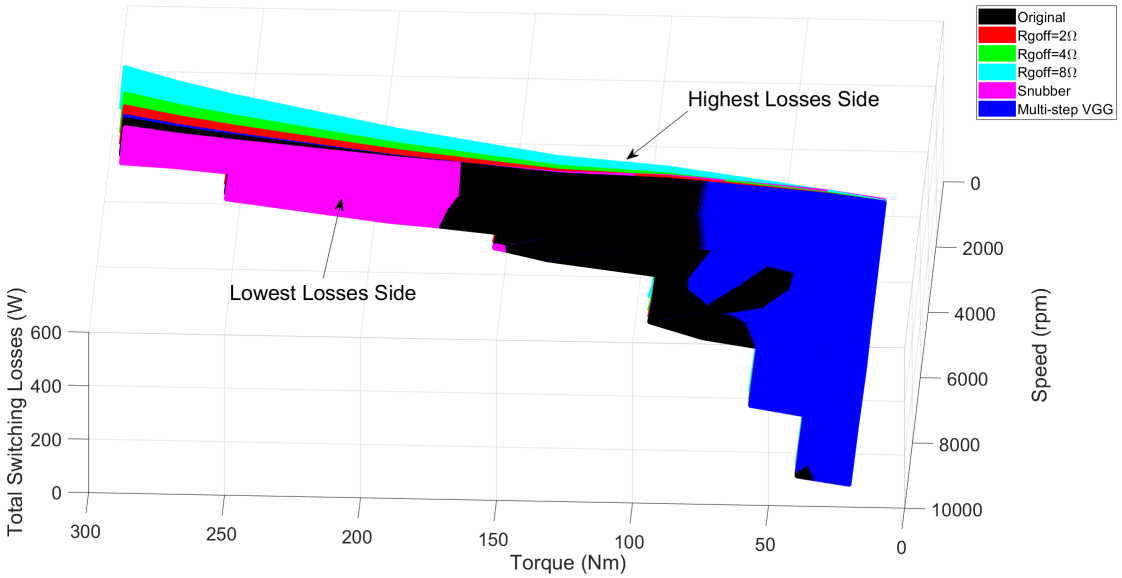

Figure 5.11: Comparisons of Total Switching Losses Under Different Methods in Drive Region–Lowest Losses Side (Excluding Snubber Circuit Resistor Losses)

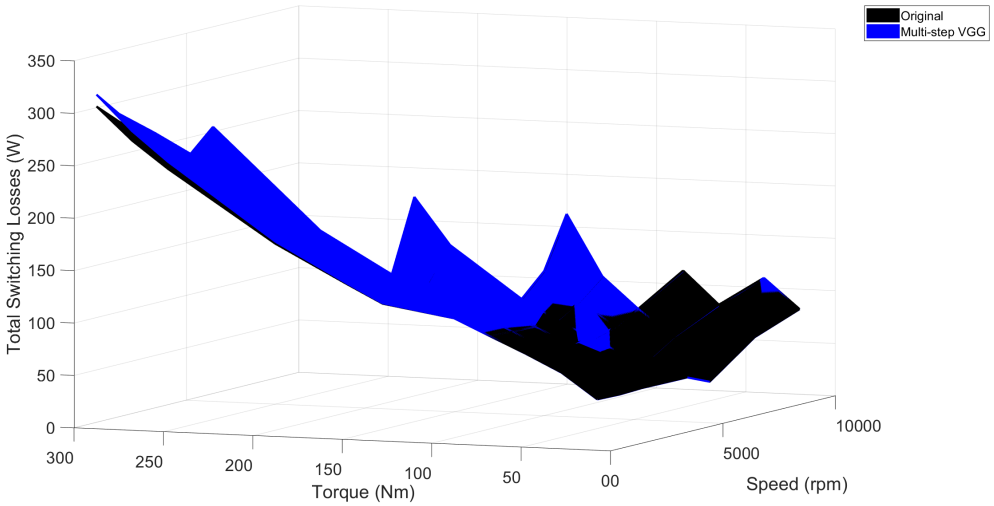

Figure 5.12: Comparison of the Effects of Multi-step V_{GG} with Original Setup on Total Switching Losses in Drive Region

As shown in Fig.5.11, the Multi-step V_{GG} method is advantageous, resulting in lower switching losses when the output torque is below approximately 80 Nm, except for several operating points at medium speed region. The original circuit generally maintains the lowest switching losses when the torque is between around 80-170 Nm. However, according to Fig.5.12 and the DPT results shown in Fig.5.7, there is no noticeable difference in total switching losses until the high torque region. The

snubber circuit performs better in reducing switching losses in the high torque region (torque higher than 170 Nm).

5.3.2.3 Switching Losses Distribution (Including Snubber Circuit Resistors)

Fig.5.13 displays the distribution of total switching losses, including the losses caused by the snubber circuit resistors, using different methods in the drive region. The switching frequency is 10kHz.

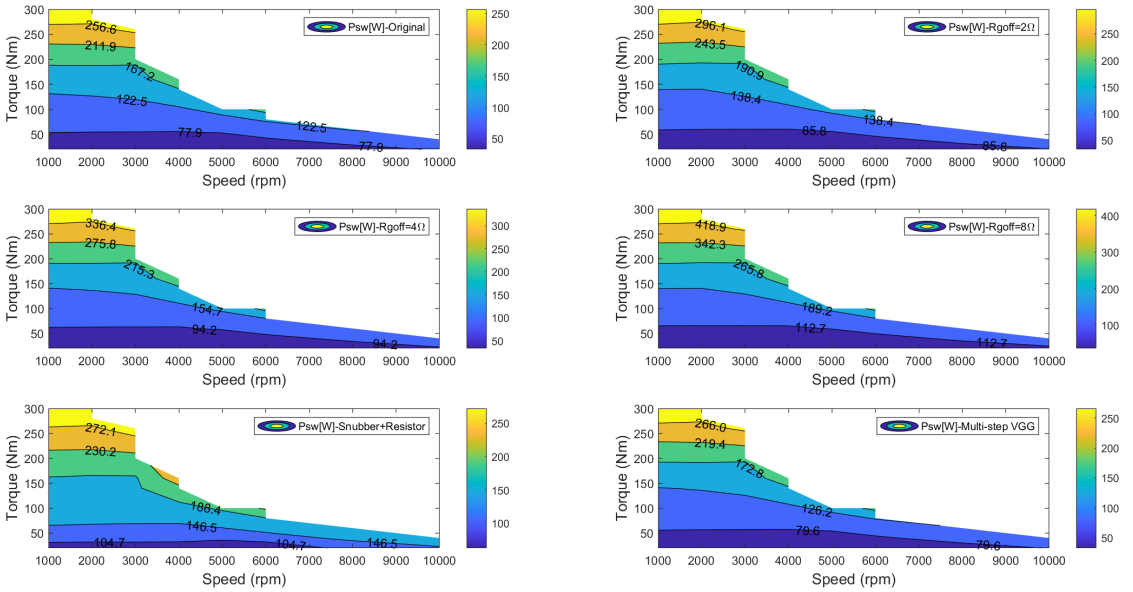

Figure 5.13: Distribution of Total Switching Losses in the Drive Region Using Different Methods (Including Snubber Circuit Resistor Losses)

From the color bar of each sub-figure in Fig. 5.13, it can be noted that when the snubber circuit resistor losses are included, the snubber circuit causes the highest total switching losses in the relatively low torque region. In the relatively higher torque region, the snubber circuit causes lower losses than the R_{goff} method, but a little bit higher losses than the Multi-step V_{GG} method.

The comparison of total switching losses,including the losses caused by the snubber circuit resistors, using different methods in the drive region is shown in Fig. 5.14.

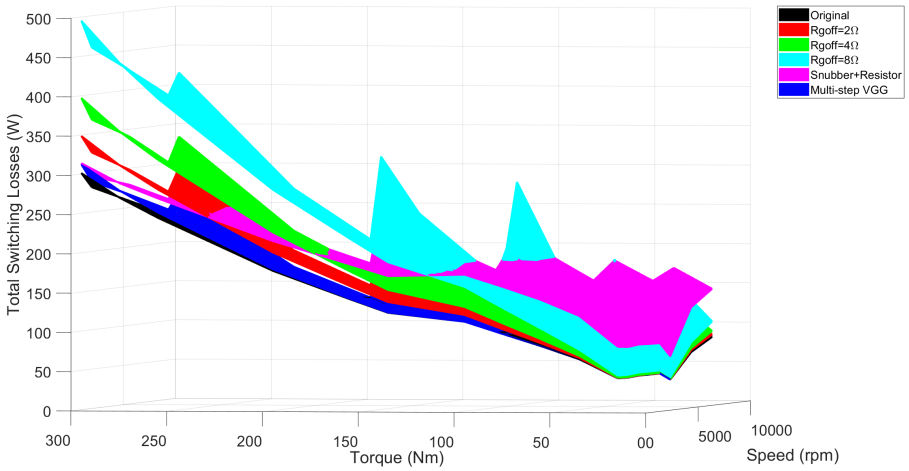

Figure 5.14: Comparison of Total Switching Losses Under Different Methods in Drive Region–Highest Losses Side (including Snubber Circuit Resistor Losses)

Fig. 5.14 shows that when considering the losses introduced by the snubber circuit resistors, the snubber circuit causes the highest total switching losses when the torque is below approximately 100 Nm compared to the other methods. As the torque increases, the snubber circuit gradually results in lower losses compared to using R_{goff}, but it still causes a little bit higher losses than the Multi-step V_{GG} method.

5.3.2.4 Total Losses Distribution

Fig.5.15 displays the distribution of total losses including switching losses and conduction losses using different methods in the drive region.

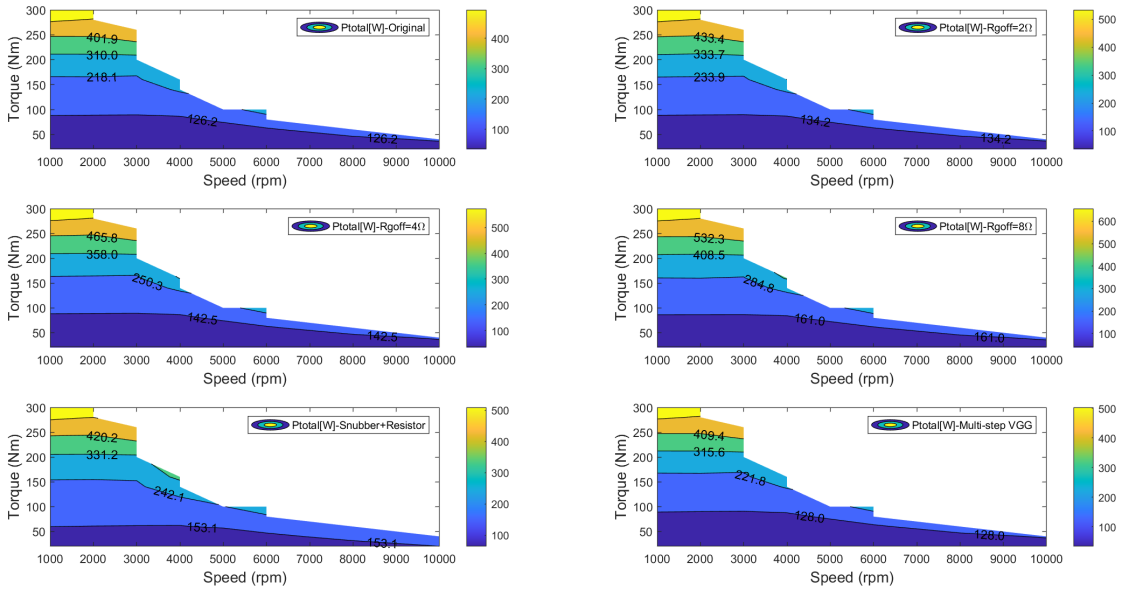

Figure 5.15: Distribution of Total Losses in the Drive Region Using Different Methods

From the color bar of each sub-figure in Fig. 5.15, it can be observed that as R_{goff} increases, the total losses also increase throughout the entire drive region. The multi-step V_{GG} method results in total losses that are essentially the same as those of the original circuit in the drive region. The snubber circuit causes the highest total losses among these methods in the very low torque region. As the torque increases, the snubber circuit gradually results in lower losses compared to using R_{goff}, but it still causes slightly higher losses than the Multi-step V_{GG} method.

The comparison of total losses,including the switching losses and conduction losses, using different methods in the drive region is shown in Fig.5.16.

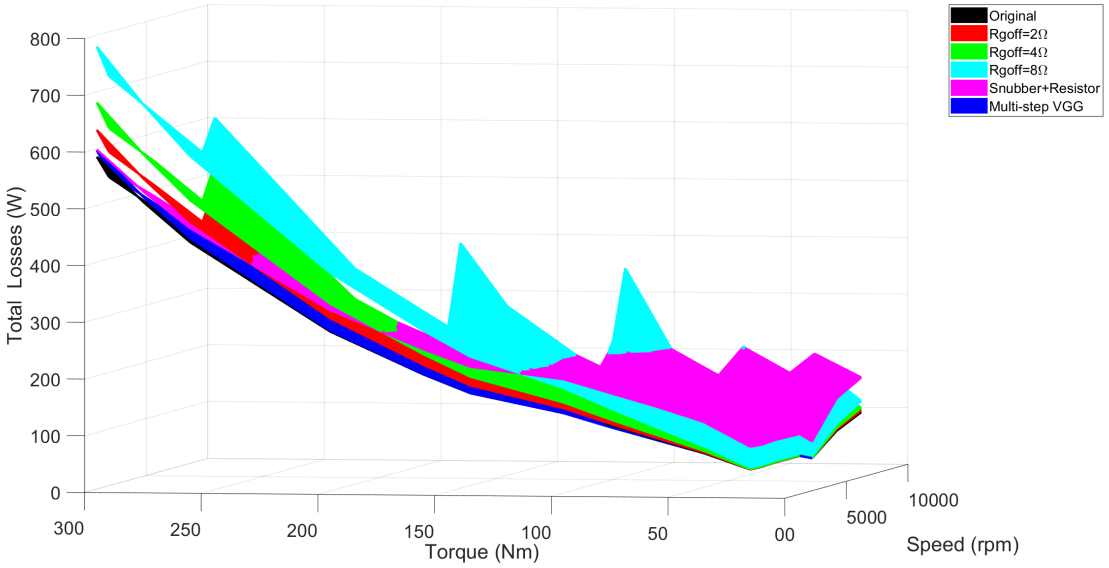

Figure 5.16: Comparison of Total Losses Under Different Methods in Drive Region

Fig.5.16 shows that the snubber circuit causes the highest total losses when the torque is below approximately 100 Nm compared to the other methods. As the torque increases, the snubber circuit gradually results in lower losses compared to using R_{goff}, but it still causes a little bit higher losses than the Multi-step V_{GG} method.

5.4 DC Link Effect

5.4.1 Analysis of Slew Rate During Turn-off at Different DC Link

Fig. 5.17 illustrates the effect of the DC link on the voltage slew rate.

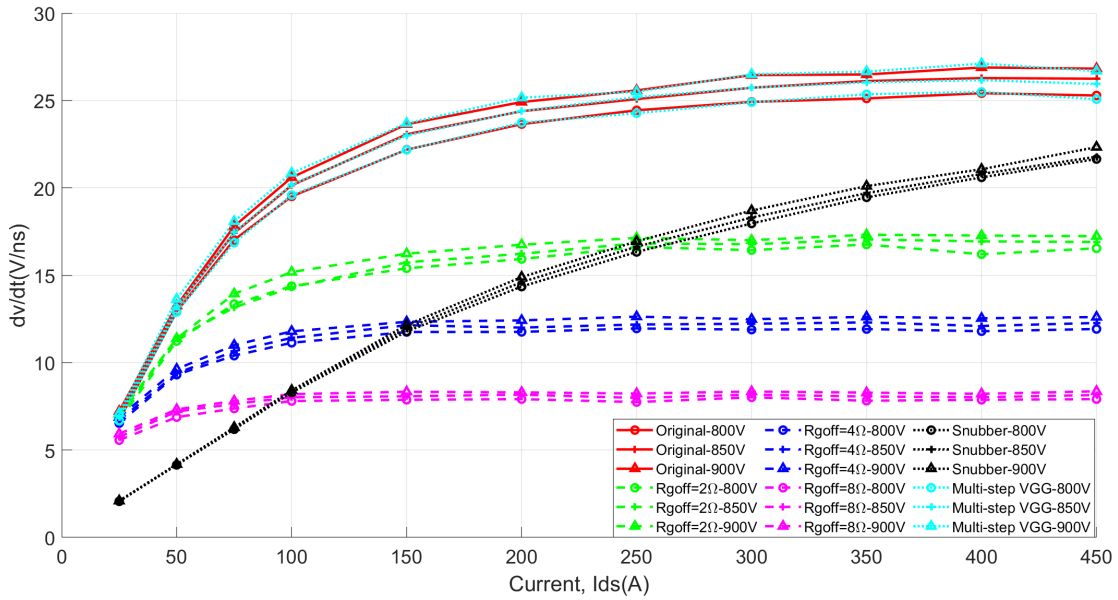

Figure 5.17: Comparison of the effects of different methods on voltage slew rate during turn-off at different DC Link

It can be observed that the DC link has minimal influence on the voltage slew rate. As the DC link increases, the voltage slew rate slightly increases among these different methods.

As shown in Fig. 5.18, the DC link's effect on the current slew rate is negligible except for the Multi-step V_{GG}. As the DC link increases, the current slew rate decreases when using the Multi-step V_{GG}.

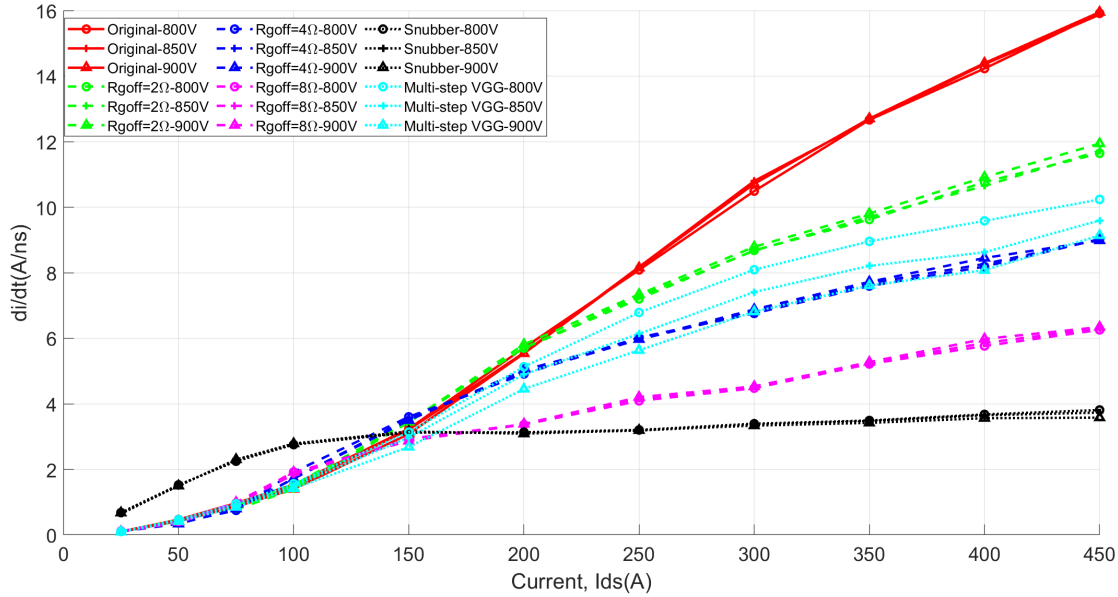

Figure 5.18: Comparison of the effects of different methods on current slew rate during turn-off at different DC Link

5.4.2 Analysis of voltage overshoot at Different DC Link

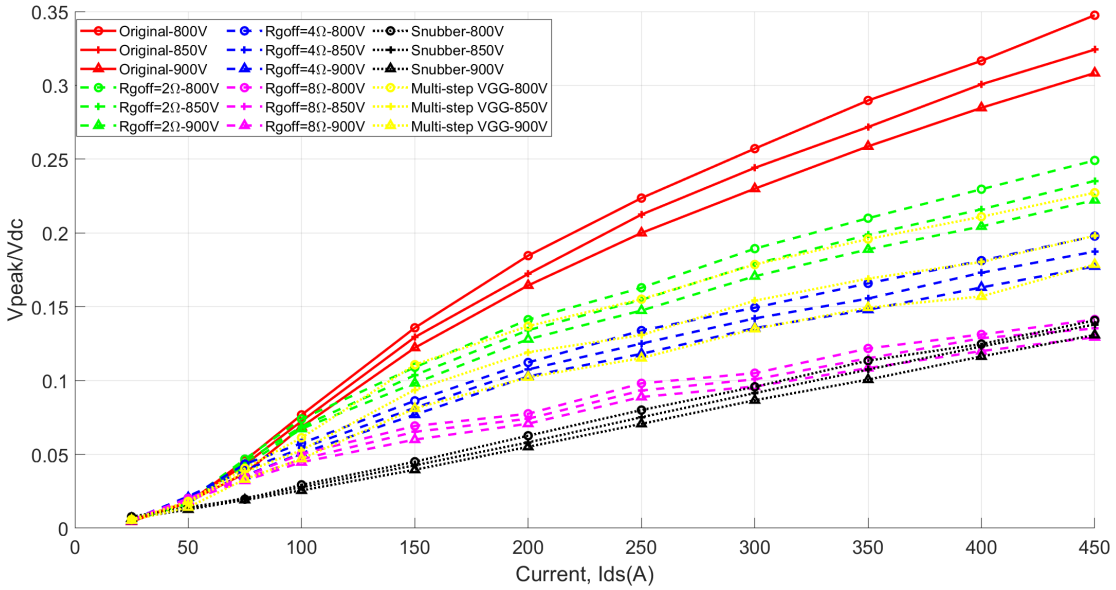

Figure 5.19: Comparison of the effects of different methods on voltage overshoot during turn-off at different DC Link

By limiting the overvoltage in relation to the DC link, transistors with lower voltage ratings can be utilized. The relationship between R_{DS} and the breakdown voltage of the component is

$$R_{\mathrm{DS}} = R_{\mathrm{DSnom}}(\frac{V_{\mathrm{max}}}{V_{\mathrm{nom}}})^2 \tag{5.1}$$

If the voltage overshoot is limited, transistors with a lower voltage rating can be used, leading to reduced conduction losses and, consequently, decreased total losses.

In Fig.5.19, the vertical axis represents the ratio of the peak voltage during turn-off to V_{dc}. As the DC link voltage increases, the ratio of the overvoltage to the reference DC link voltage decreases, indicating that this type of SiC module is capable of maintaining better overvoltage suppression at higher voltage levels. According to (5.1), R_{DS} can be reduced by increasing the DC link voltage.

5.4.3 Analysis of Switching Energy at Different DC Link

Fig. 5.20 and Fig. 5.21 illustrates the comparison of the effects of different methods on turn-off and turn-on energy at different DC Link.

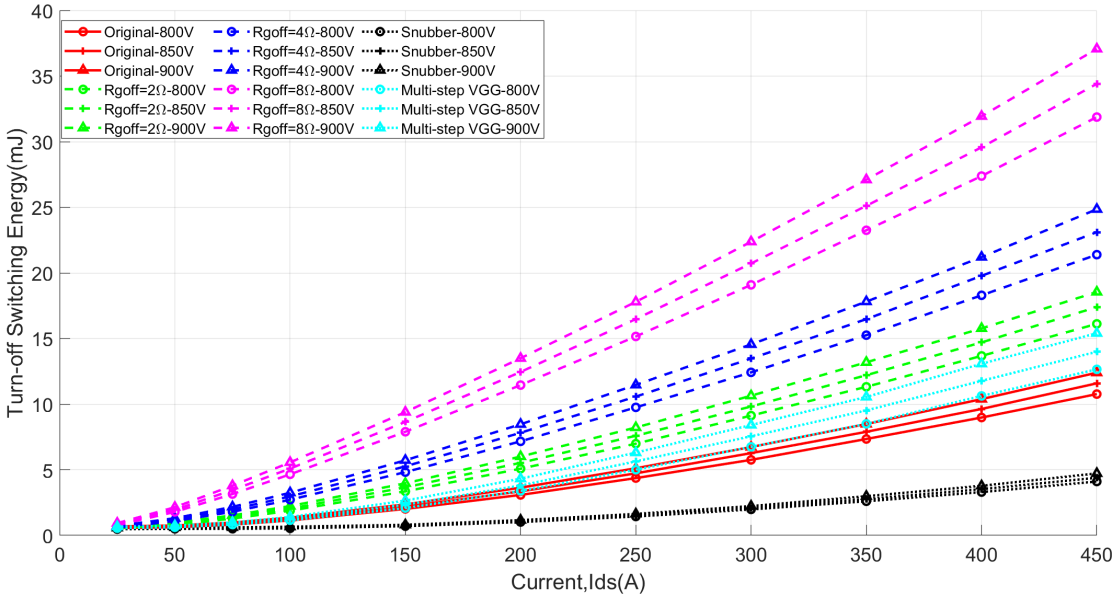

Figure 5.20: Comparison of the effects of different methods on turn-off energy at different DC Link

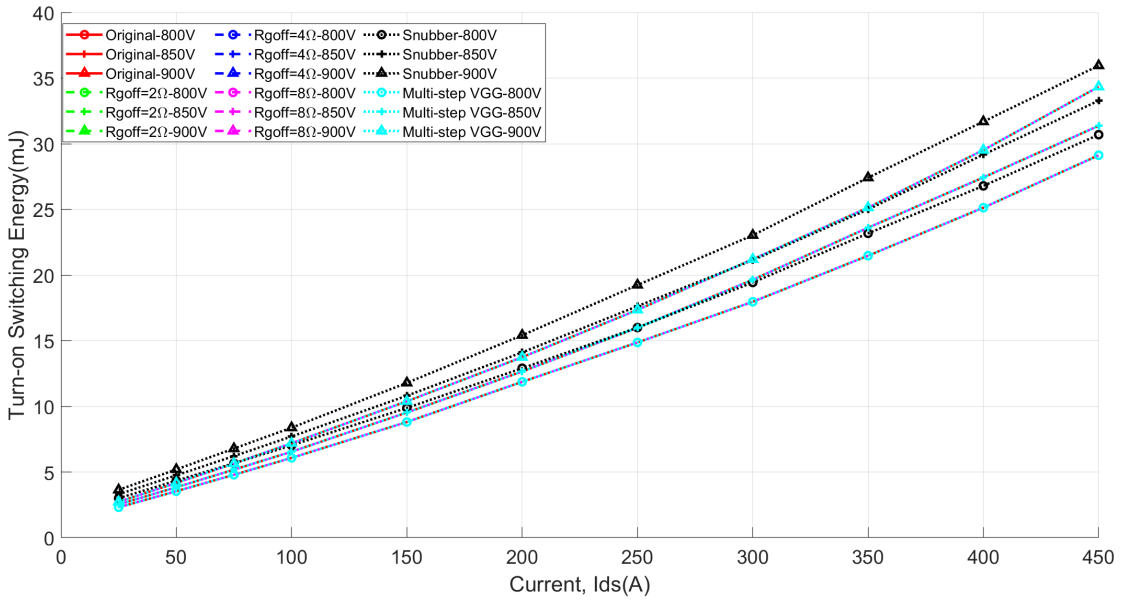

Figure 5.21: Comparison of the effects of different methods on turn-on energy at different DC Link

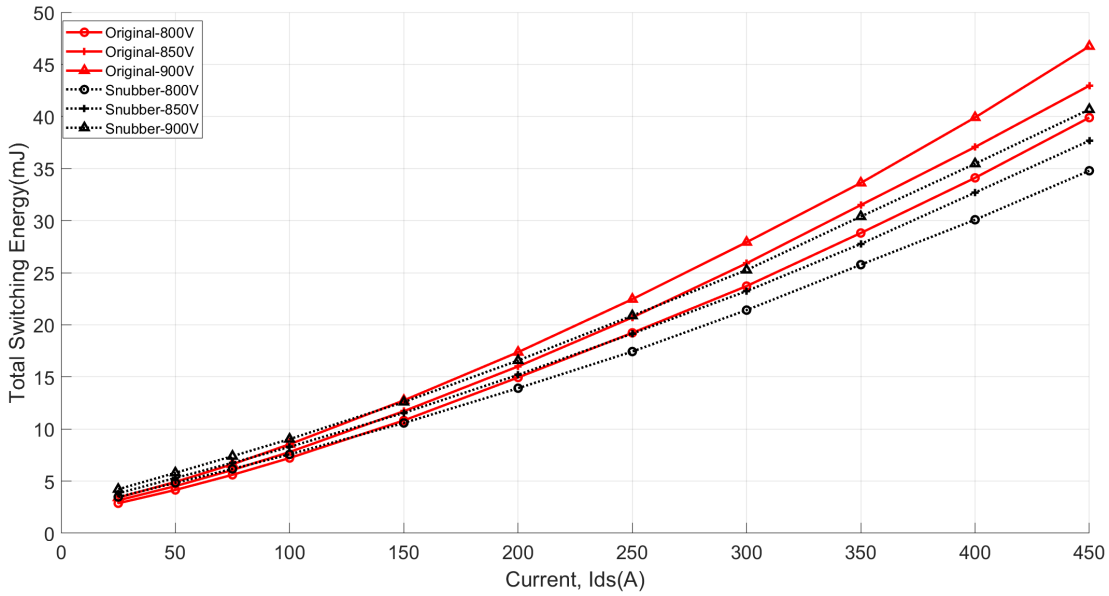

Figure 5.22: Comparison of the Effects of Snubber Circuit with Original Setup on Switching Energy at Different DC Link

From the perspective of total switching energy shown in Fig. 5.22, when the current is below approximately 100A, the snubber circuit causes the switching energy to be slightly higher than the switching energy of the original circuit at respective DC link voltages. As the current increases, the snubber circuit effectively reduces the switching energy, making them lower than the switching energy of the original circuit at corresponding DC link voltages. But this comparison only consider the snubber circuit transistors losses.

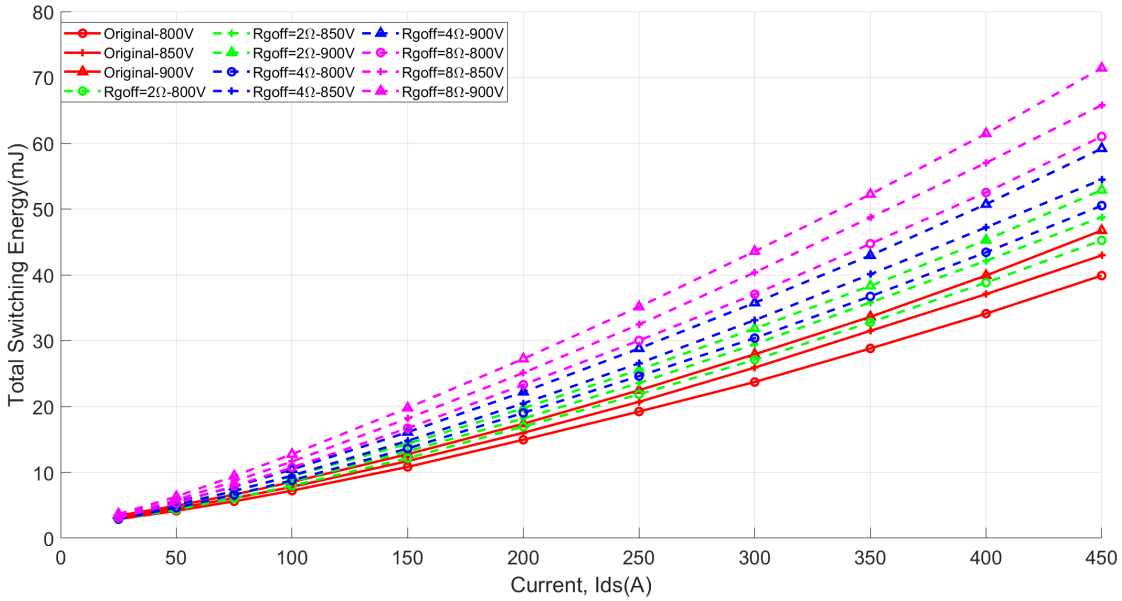

Figure 5.23: Comparison of the Effects of Different R_g with Original Setup on Switching Energy at Different DC Link

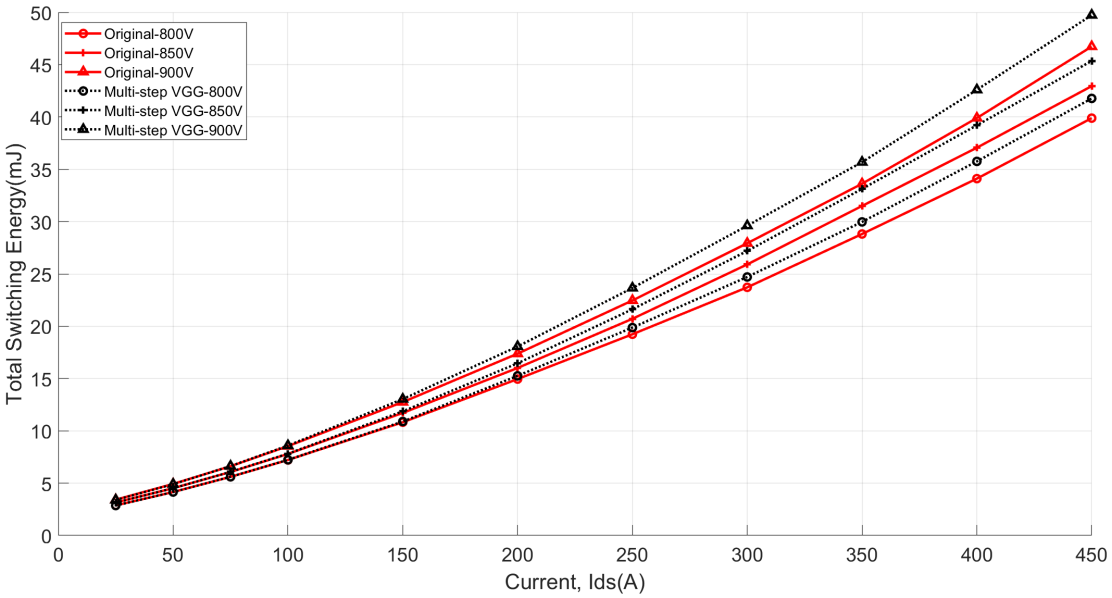

Figure 5.24: Comparison of the Effects of Multi-step V_{GG} with Original Setup on Switching Energy at Different DC Link

From Fig. 5.19 and Fig. 5.22 to Fig.5.24, it can be seen that, overall, from the perspectives of reducing voltage overshoot and managing switching energy under different DC link conditions, using a multi-step V_{GG} can be considered when the current is relatively low, specifically below approximately 150A. This approach maintains switching losses in the original circuit at comparable levels while effectively reducing voltage overshoot. As the current increases, the snubber circuit becomes more effective than other methods in minimizing the impact of voltage overshoot and switching energy.

5.4.4 Calculated Conduction Losses at Different DC Link Voltages

When the DC side voltage increases, assuming the system operates within the same modulation range, according to (5.2), the maximum AC output phase voltage of the inverter will increase,

$$V_{\mathrm{AC,max}} = \frac{M \cdot V_{\mathrm{DC}}}{2} \tag{5.2}$$

In the case of constant power and same power factor, the AC side current is inversely proportional to the AC side voltage, so it can be deduced that

$$P_{\mathrm{AC}} = 3 \cdot V_{\mathrm{AC}} \cdot I_{\mathrm{AC}} \cdot \cos\varphi \tag{5.3}$$

$$I_{\mathrm{AC,new}} = \frac{P_{\mathrm{AC}}}{V_{\mathrm{AC,new}} \cdot \cos\varphi} \tag{5.4}$$

$$I_{\mathrm{AC,new}} = I_{\mathrm{AC,old}} \cdot \frac{V_{\mathrm{AC,old}}}{V_{\mathrm{AC,new}}} \tag{5.5}$$

Therefore, the change in MOSFET conduction loss can be derived under constant power and reduced current conditions,

$$P_{\text{con}} = I_{\text{AC}}^2 \cdot R_{\text{on}} \tag{5.6}$$

$$P_{\text{con,new}} = P_{\text{con,old}} \cdot \left(\frac{I_{\text{AC,new}}}{I_{\text{AC,old}}} \right)^2 \tag{5.7}$$

$$P_{\text{con,new}} = P_{\text{con,old}} \cdot \left(\frac{V_{\text{AC,old}}}{V_{\text{AC,new}}} \right)^2 \tag{5.8}$$

In PLECS, since the motor's LUT is only available for 800V, the conduction loss at 850V and 900V is estimated based on the above analysis and the conduction loss at 800V. The calculation results are shown in Table 5.1.

Table 5.1: Conduction Losses at Different DC Link Voltages

Operating Point	Voltage [V]	Conduction Losses[W]
2000rpm, 200Nm	800	103.16
	850	91.38
	900	81.5
5000rpm, 100Nm	800	42.93
	850	38.02
	900	33.92

As shown in Table 5.1, increasing the DC voltage helps reduce conduction losses due to the decrease in current.

6

Conclusion

6.1 Results from present work

This thesis aims to investigate the turn-off switching losses and voltage overshoots of a SiC-based inverter in BEV by employing various techniques: different R_{goff}, Multi-step V_{GG}, and incorporating a snubber circuit.

According to the DPT results, applying a multi-step pulse at V_{GG} with a 2V magnitude and 30ns duration reduces current oscillation and voltage overshoot. When I_{ds} is 100A, this method essentially does not affect the current slew rate or turn-off switching losses. However, at 400A, this approach effectively decreases voltage overshoot and current slew rate but slightly increases turn-off losses.

Under an 800V DC link, a comparison between the original setup and these three optimization methods reveals that the snubber circuit is most effective in reducing overvoltage within a measured I_{ds} current range of 25A to 450A.

Regarding the total switching energy, the R_{goff} contributes to an increase in the total switching energy. A larger turn-off gate resistance results in greater switching energy. The Multi-step V_{GG} method maintains nearly the same switching energy as the original setup when the current is below 150A, but it increases switching energy as the current rises. Nonetheless, the increase in switching energy with the Multi-step V_{GG} method is smaller compared to that when using R_{goff} alone.

The snubber circuit increases switching energy when the current is below approximately 100A. But, as the current increases, the snubber circuit becomes the most advantageous. Despite this advantage, when accounting for the energy of the snubber resistor, the overall switching energy—including the total switching energy of the transistor and the energy caused by the snubber resistor—tend to increase when the current is below approximately 300A. Nevertheless, as the current continues to rise, these energy eventually become lower than those in the original circuit.

Additionally, the distribution of switching losses and conduction losses in the drive region was measured in PLECS. when considering the losses introduced by the snubber circuit resistors, the snubber circuit causes the highest switching losses and total losses when the torque is below approximately 100 Nm compared to the other methods. As the torque increases, the snubber circuit gradually results in lower

losses compared to using R_{goff}, but it still causes a little bit higher losses than the Multi-step V_{GG} method. In summary, when operating in the low-torque region, the Multi-step V_{GG} can be considered, as it not only reduces voltage overshoot but also does not significantly increase inverter losses. When operating at higher torque, the snubber circuit can be considered, as it effectively reduces voltage overshoot while the increase in switching losses is slight.

For the different DC link effects simulated in LTspice, the goal is to achieve the lowest losses for a given DC link voltage. Increasing the DC voltage helps reduce conduction losses due to the decrease in current. Additionally, depending on the method used, the voltage rating of the transistor can be reduced, resulting in lower conduction losses. Overall, the Multi-step V_{GG} method can be considered when the current is relatively low, below approximately 150 A. This approach maintains the switching energy at levels comparable to the original circuit while reducing voltage overshoot. As the current continues to increase, the snubber circuit minimizes the impact of voltage overshoot and switching energy compared to other methods.

6.2 Future work

The current DPT is conducted in LTspice simulations, but actual experiments would yield more accurate results. Additionally, the implementation of the Multi-step V_{GG} requires further refinement. For instance, if AGD is used to achieve Multi-step V_{GG}, consideration must be given to the selection of switches in the AGD and the design of the controller. Finally, To comprehensively evaluate the impact of increased DC voltage on total losses, the motor's LUT for 850V and 900V needs to be imported into PLECS. This will allow for the calculation of switching losses and accurate conduction losses at the corresponding voltages.

Bibliography

[1] S. Hou, H. Chen, H. Yin, J. Zhao, F. Xu and J. Gao, "Energy Management Based on Mixed-Integer Nonlinear Model Predictive Control for Hybrid Electric Vehicles," in IEEE Transactions on Intelligent Transportation Systems,2024.

[2] Shijie Zhang, Pranav Katta, "Efficiency Optimization of Electric Drives with Variable Switching Frequency using Wide-Bandgap Motor Drives", Master Thesis at Chalmers University of Technology, 2023.

[3] I. Aghabali, J. Bauman, P. J. Kollmeyer, Y. Wang, B. Bilgin and A. Emadi, "800-V Electric Vehicle Powertrains: Review and Analysis of Benefits, Challenges, and Future Trends," in IEEE Transactions on Transportation Electrification, 2021.

[4] S. Yunus, W. Ming and C. E. Ugalde-Loo, "Efficiency Improvement Analysis of a SiC MOSFET-based PMSM Drive System with Variable Switching Frequency," 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, 2021.

[5] M. M. Abualnaeem, S. A. B. M. Zulkifli, N. Z. Bin Yahaya and H. A. Soomro, "Comparison of Power Loss in SiC-MOSFET and Si-IGBT Traction Inverter with Variable Switching Frequency for Electric Vehicle Application," 2024 IEEE Symposium on Industrial Electronics & Applications (ISIEA), Kuala Lumpur, Malaysia, 2024.

[6] M. Nawaz and K. Ilves, "On the comparative assessment of 1.7 kV, 300 a full SiC-MOSFET and Si-IGBT power modules," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2016.

[7] S. Zhao, X. Zhao, Y. Wei, Y. Zhao and H. A. Mantooth, "A Review of Switching Slew Rate Control for Silicon Carbide Devices Using Active Gate Drivers," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2021.

[8] A. Dearien, S. Zhao, C. Farnell and H. A. Mantooth, "Slew Rate Control of High-Voltage SiC MOSFETs using Gate Resistance vs. Intermediate Voltage Level," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South), 2019.

[9] A. P. Camacho, V. Sala, H. Ghorbani and J. L. R. Martinez, "A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory," in IEEE Transactions on Industrial Electronics, 2017.

[10] D. Shin, S. -K. Sul, J. Sim and Y. -G. Kim, "Snubber Circuit of Bidirectional Solid State DC Circuit Breaker Based on SiC MOSFET," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 2018.

[11] D. Park, D. Shin, S. -K. Sul, J. Sim and Y. -G. Kim, "Overvoltage Suppressing Snubber Circuit for Solid State Circuit Breaker considering System Inductances," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South), 2019.

[12] W. Zhou, M. Diab, X. Yuan and C. Wei, "Mitigation of Motor Overvoltage in SiC-Based Drives Using Soft-Switching Voltage Slew-Rate (dv/dt) Profiling," in IEEE Transactions on Power Electronics,2022.

[13] Paul Mourges, "Evaluation of Voltage Controlled Active Gate-Drivers for SiC MOSFET Power Semiconductors", Master Thesis at Virginia Polytechnic Institute and State University, 2022.

[14] Lu, Y.; Yu, Y.; Huang, C.; Yan, J.; Wu, H. Optimization Method of SiC MOSFET Switching Trajectory Based on Variable Current Drive. Electronics 2024.

[15] Wolfspeed Datasheet-CAB450M12XM3.

[16] Ned Mohan, Tore M. Undeland, William P. Robbins, "Power Electronics: Converters, Applications, and Design".

[17] K. Yamaguchi, K. Katsura, T. Yamada and Y. Sato, "Comprehensive evaluation of gate boost driver for SiC-MOSFETs," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016.

[18] H. Li, Y. Jiang, Z. Qiu, T. Shao and Y. Wang, "A Multi-step Active Gate Driver for Suppressing Crosstalk of SiC MOSFET," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), Nanjing, China, 2020

[19] M. Blank, T. Glück, A. Kugi and H. -P. Kreuter, "Slew rate control strategies for smart power ICs based on iterative learning control," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, USA, 2014

[20] X. Sun, S. Zhi, Y. Hao, M. Ma and D. Xu, "An Active Gate Driver for SiC to Meet Requirements in EMI and Switching Loss by Slew Rate Control," 2023

11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia), Jeju Island, Korea, Republic of, 2023

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