Design of a 48 V three-phase inverter

For automotive applications

Master's thesis in Electric Power Engineering

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Abstract

This project presents a design and construction of a three-phase inverter, drive circuit and dc-link capacitor bank. The inverter should be able to supply an electrical machine with 48 V and 250 A. Initial calculations and simulations were made to get some base for the ordering of hardware. The inverter board consists of six MOSFETs in parallel for each phase and the PCB itself is made of aluminum to enable a thermal substrate technique. The inverter PCBs are mounted on an aluminum frame where liquid runs between them to cool the inverter. The drive circuit is controlled with a dSPACE system and the tests are made with a load consisting of cables and iron powder cores. Temperatures are measured with PT100 sensors for the water and an infrared camera for the surfaces.

Two different MOSFETs were investigated, one with higher switching losses and one with higher conduction losses. The two inverters were tested on an RL load and the cooling system picked up around 270 W at a phase current of 150 A_{rms}. Theoretical calculations, performed with measured parameters, represents the temperature measurements well. The thermal resistance between the case and the sink in the inverter, $R_{\theta cs}$, is measured to around 0.15 $[K/W]$.

Index Terms: Capacitor bank, cooling system, drive circuit, dSPACE, inverter, MOSFET, thermal evaluation.

Acknowledgements

I would like to start by thanking my examiner and supervisor Dr. Stefan Lundberg for all the help I have received during the project. Despite your high workload you always took the time to answer my questions and help me with measurements. Without all the help from you the project would not have been possible.

Another person whom also has given me invaluable help during the thesis is Robert Karlsson. His expertise within electronics has helped me to manage a lot of the problems that occurred. The assistance from your side is crucial for the results of the project.

Thanks to my opponents, Erik Johansson and Linus Khosravi, for their comments and thoughts about the project, also thanks to Jesper Wiig Sundelin and Henrik Dannetun for his help with the report.

Contents

List of Figures

viii

List of Tables

Glossary

BLDC Brushless dc

CAD Computer-aided design

emf Electromotive-force

MOSFET Metal oxide semiconductor field effect transistor

PCB Printed circuit board

PWM Pulse-width modulation

rms Root mean square

1

Background

The car industry is heading towards a 48 V system, which will replace the traditional 12 V system. This change would make an implementation of a mild hybrid system, with a small electrical motor, possible. An electrical motor rated around 10 kW would be able to regenerate most of the energy dissipated during braking in city driving and this could boost the fuel efficiency by as much as 17 % [1]. Using a 48 V system would also benefit and enable more efficient and advanced functions as heating, ventilation and air conditioning in the car [2].

Car generators of today are usually based on a multiphase electrically magnetized synchronous generator connected to a passive diode rectifier, where the field current is used to regulate the output voltage. But in order to run the generator as a motor in a mild hybrid system an active rectifier is needed. One common way to design active rectifiers, for this purpose, is by using MOSFET switches [1]. The space available in the motor area of a modern car is limited. This means that if new components are added in the same area they must be compact. To minimize the fuel consumption the new components should also be light so the extra weight of the vehicle does not affect the benefits of the added components. Both the generator and the inverter must be designed to be as compact as possible and, at the same time, have a high efficiency [3] [4]. One good solution would be to have small enough generator, inverter and control system so it could be

integrated into one unit [3] [4]. The size of the unit is dependent on the type of cooling system used. Usually a liquid cooled system takes up less space than an air cooled system [5].

1.1   Aim

The aim of this project is to investigate the possibility to build a compact MOSFET inverter with thermal substrate technique [6] and evaluate the thermal properties of the inverter while it is used in a drive system. The inverter will be build for a 48 V PMSM motor with a peak current of 250 A [7]. The project will also cover the design/selection of the capacitors for the dc-link and design the drive circuit.

1.2   Scope

The hardware designed in the project will be based on initial calculations and simulations. All parameters are not possible to simulate within the project, such as the water flow in the cooling frame. The theoretical calculations is based on parameters extracted form data sheets and other supplier information. Updates on the parameters will be made with measurements on the hardware to get more realistic values, but all parameters can not be measured so some of the parameters will be kept from the information in the data sheets. The inverter is designed for a specific electrical machine, but it can be used in other applications as long as the voltage and current limits are not exceeded.

2

Three-phase MOSFET inverter

Three-phase inverters are often used to supply three-phase loads, such as ac motors. The basic structure of a three-phase inverter is shown in Figure 2.1. Each of the three legs produces an output which is displaced by 120° with respect to each other. The output of each leg depends on the status of the switch and the input voltage, V_d. Since one of the two switches (MOSFETs) in each leg is always on, the output voltage is independent of the output load current [8].
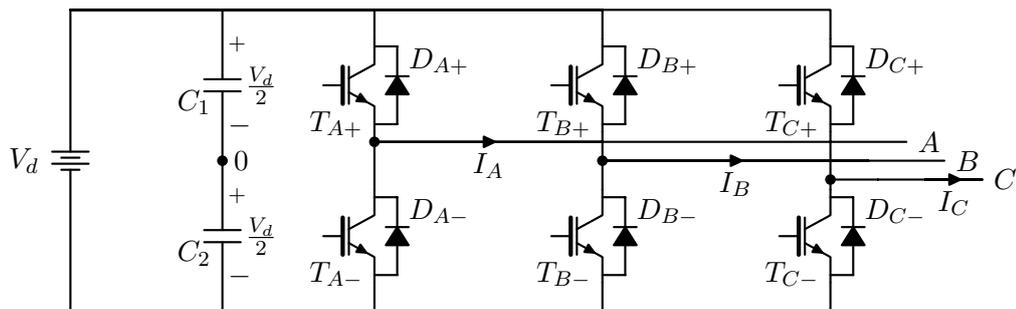
Figure 2.1: Schematic of a three-phase inverter.

In order to control the duration that each switch is open a method called *pulse-width modulation* (PWM) switching is used. A balanced three-phase output voltage is obtained from a PWM switching with a triangular wave

3

that is compared with three sinusoidal control voltages who are 120° phase shifted. Every switch in the inverter gets a duty ratio, D, from the PWM switching, and this duty ratio controls if the switch is opened or closed [8].

The principle of PWM for one phase is shown in Figure 2.2. In order to generate the switching signal a triangular wave (v_{tri}) is compared to a control signal ($v_{control}$). The comparison of these two signals decides when a certain switch in the phase leg is opened or closed. Since the principle of one leg is described the reference will be to leg A in Figure 2.1. When $v_{control} < v_{tri}$ T_{A-} is on and T_{A+} is off. The opposite is valid for when T_{A+} is on and T_{A-} is off, which is the case when $v_{control} > v_{tri}$. Note that the time-scale in Figure 2.2 is made to illustrate the principle and not to show a real case of switching. In most applications the switching frequency is selected to be either below 6 kHz or higher than 20 kHz, this is to be above the audible range. It is preferred to have a low switching frequency to reduce the switching losses, which is discussed further in Section 2.1.1. If the optimal switching frequency is between 6 and 20 kHz it is often raised to above 20 kHz rather than having it lowered [8].
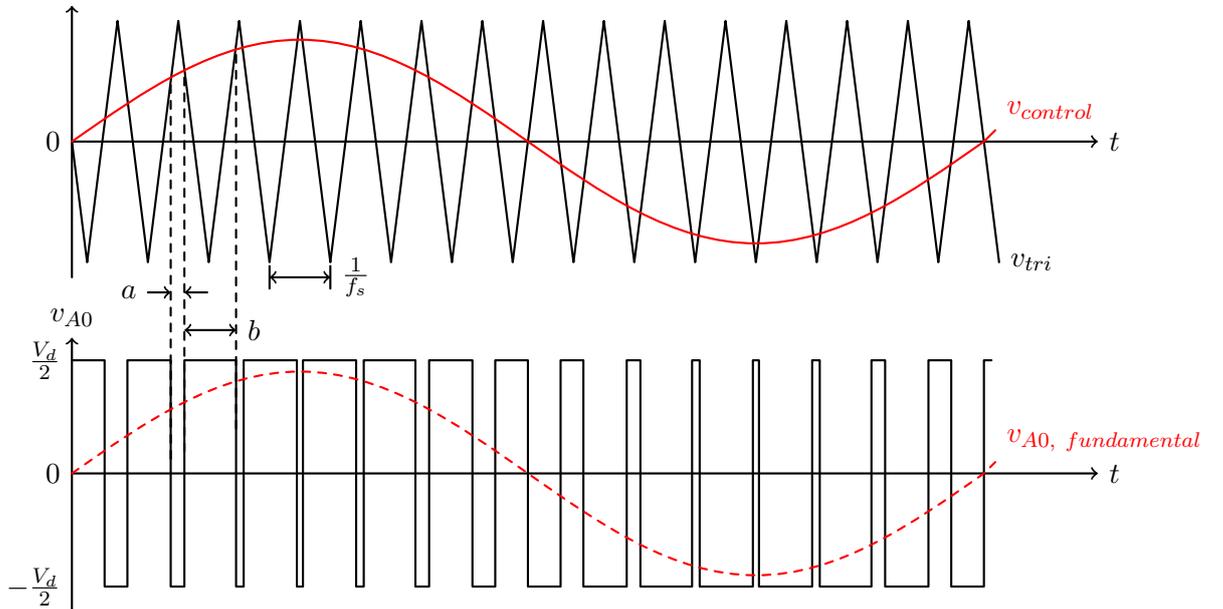
Figure 2.2: The principal of pulse-width modulation for one phase, where a is when $v_{control} < v_{tri}$ and b is when $v_{control} > v_{tri}$.

4

2.1   MOSFET

Metal oxide semiconductor field effect transistor (MOSFET) is a type of semiconductor which is applicable when fast switching is needed and it has an on-state current-carrying capability and off-state blocking voltage capability. The MOSFET has three ports; *gate*, *drain* and *source*. When a voltage is applied between the gate and source the MOSFET is conducting and a current can run between the drain and source. The internal doping of a power MOSFET is shown in Figure 2.3. Looking at the figure it seams like there will be reversed biased between any of the *pn* junctions, which will not allow a current to pas through the MOSEFT. To allow a current to run through the MOSFET a voltage is applied that biases the gate positive with respect to the source. This voltage will convert the silicon surface under the gate oxide into an *n*-type channel which connects the source to the drain which enables the current to flow in the MOSFET [8].
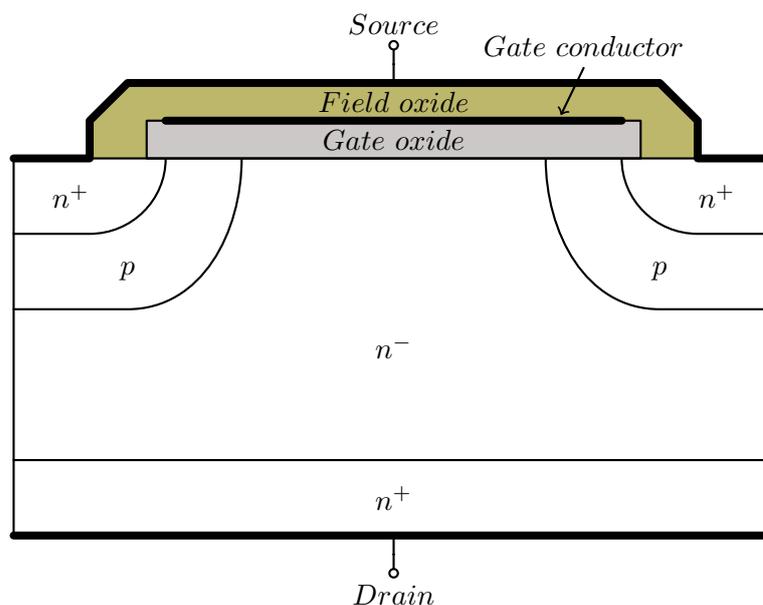
Figure 2.3: The internal doping in a power MOSFET.

There are two main losses in a MOSFET, the conduction and switching losses. These losses generates a temperature rise within the component and

if the temperature gets to high the component will break [9]. The conduction losses in the MOSFET occurs due to the internal on-state resistance (R_{DSon}) which is related to the differently doped regions. Usually there is a balance between highly doped regions and breakdown voltage. The higher doping in the regions, the lower the breakdown voltage and lower on-state resistance. The on-state resistance is also related to the junction temperature of the MOSFET, with increasing temperature the resistance gets higher. This occurs since the collision of charge carriers increases with the temperature which yields a lowered mobility and R_{DSon} is inversely proportional to the mobility [8]. The principle to calculate the conduction losses is presented in Section 2.1.3.

The output characteristics of a MOSFET, shown in Figure 2.4, is often described with the drain current (I_D) as a function of the voltage between drain and source (V_d) with the voltage between gate and source (V_{GS}) as a parameter. The operation points is dived into two regions called the *ohmic* region and the *active* region. Once V_d reaches a certain level the MOSFET leaves the active region and an avalanche occurs. This is referred to as the breakdown voltage (BV_d) of the MOSFET, i.e. the voltage rating of the MOSFET [8].
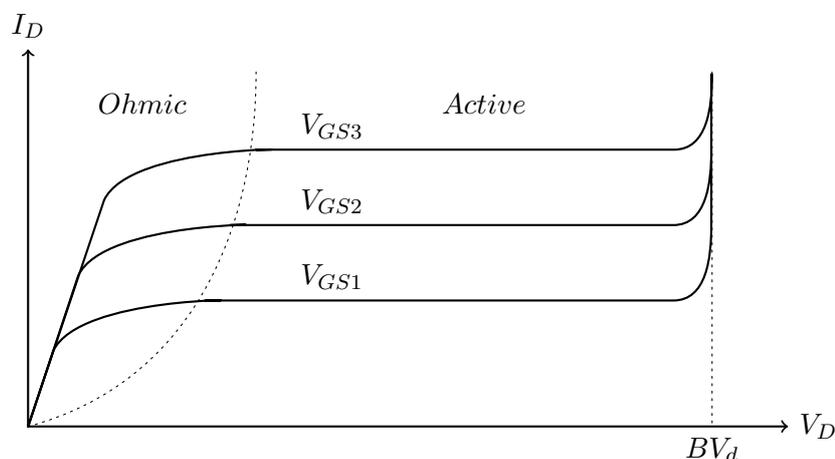
Figure 2.4: The output characteristics of a MOSFET for different V_{GS}.

As can be noticed in Figure 2.4 the MOSFET is acting as a resistance in the beginning of the ohmic region and as a current source in the active

region. Between those states there is a transition region. As also can be noticed from the figure the drain current for when the transition occurs is depending on the gate to source voltage of the MOSFET. For a higher gate-source voltage a higher drain current is needed before the MOSFET enters the active region. The two states can be modeled as is shown in Figure 2.5 with one model for the active region and one for the ohmic region [8]. In an inverter it is desired to operate the MOSFET in the ohmic region when it is on, because this gives the lowest losses. But during turn on and turn off the MOSFET is operated in the active region [8].

(a) For the active region.　　(b) For the ohmic region.
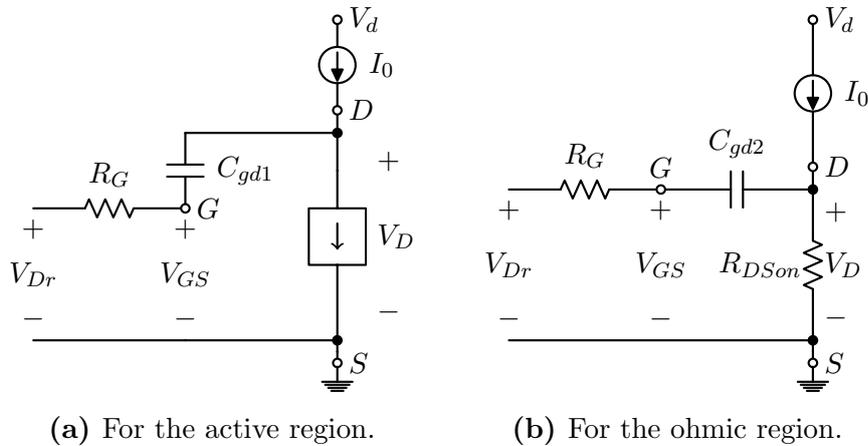
Figure 2.5: The equivalent circuits of the MOSFET.

2.1.1　Switching losses

In Figure 2.6 the principle waveform of the switching in the MOSFET is shown. The fall and rise time of the voltage is divided into two different intervals depending on when the MOSFET is in the active region (t_{fu1}) or in the ohmic region (t_{fu2}), see Figure 2.4. The equivalent circuits for the fall time of the voltage are shown in Figure 2.5, where Figure 2.5a corresponds to the active region and Figure 2.5b corresponds to the ohmic region. Similar reasoning is made for the rise time of the voltage, but then $V_{Dr} = 0$ [8] [9], and the MOSFET is first in the ohmic region (t_{ru2}) and then in the active region (t_{ru1}). As seen in Figure 2.5, V_{Dr} is the voltage with the reference before the gate resistor.
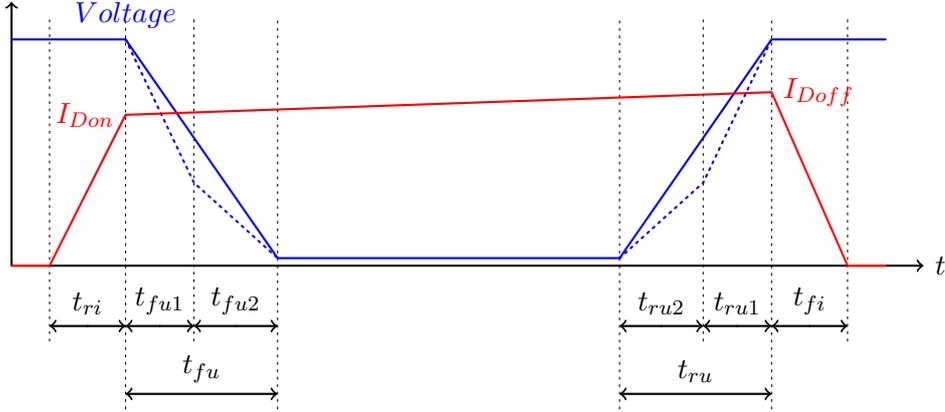
Figure 2.6: Voltage and current shapes during switching in a MOSFET.

In order to calculate t_{fu1}, t_{fu2}, t_{ru1} and t_{ru2} the following set of equations can be used

$$t_{fu1} = \frac{R_G(V_d - R_{DSon} \cdot I_{Don})}{2} \cdot \frac{C_{gd1}}{V_{Dr} - V_{plateau}}$$
$$t_{fu2} = \frac{R_G(V_d - R_{DSon} \cdot I_{Don})}{2} \cdot \frac{C_{gd2}}{V_{Dr} - V_{plateau}} \tag{2.1}$$

and

$$t_{ru1} = \frac{R_G(V_d - R_{DSon} \cdot I_{Don})}{2} \cdot \frac{C_{gd1}}{V_{plateau}}$$
$$t_{ru2} = \frac{R_G(V_d - R_{DSon} \cdot I_{Don})}{2} \cdot \frac{C_{gd2}}{V_{plateau}} \tag{2.2}$$

where the parameters R_G, R_{DSon}, C_{gd1}, C_{gd2} and $V_{plateau}$, for certain operation points, can be obtained in the data sheet. Before the switching loss can be calculated t_{fu} and t_{ru} must be determined by

$$t_{fu} = t_{fu1} + t_{fu2}$$
$$t_{ru} = t_{ru1} + t_{ru2} \tag{2.3}$$

which will yield an approximation the rise and fall time of the voltage shown in 2.6. To calculate the total, both in the MOSFET and the diode, losses during the switching the following equation can be used [9]

$$P_{sw} = V_d(I_{Don}\frac{t_{ri} + t_{fu}}{2} + Q_{rr} + \frac{1}{4} \cdot Q_{rr} + I_{Doff}\frac{t_{fi} + t_{ru}}{2})f_{sw} \tag{2.4}$$

8

where t_{ri} (rise time of the current), t_{fi} (fall time of the current) and Q_{rr} (switch on energy caused by the reverse-recovery if the free-wheeling diode) is given in the data sheet and $\frac{1}{4} \cdot Q_{rr}$ is the turn on energy in the diode. The switch off energy in the diode can be neglected according to [9].

In order to simplify the calculations for an application in a three-phase inverter the parameters I_{Don} and I_{Doff} in (2.1)-(2.4) can be replaced with the following equivalent dc current

$$I_{dc} = \frac{\sqrt{2}}{\pi} \cdot I_{0,\ rms} \qquad (2.5)$$

where $I_{0,\ rms}$ is the output rms current [9]. This yields an average power loss over one period of the output current.

In order to calculate the switching losses in a MOSFET the time parameters that are shown in Figure 2.6 needs to be verified [9]. Using (2.1) and (2.2) along with complimentary oscilloscope measurements of the voltage over the MOSFET enables a approximation of the switching losses. The parameters needed could also be found in the data sheet, but then they are specified for a certain operation point, which might differ for the application.

2.1.2 Blanking time

The commutations in Figure 2.2 is shown as ideal, but the current does not go straight from T_{A+} to T_{A-}, which is illustrated in Figure 2.6. In order to make sure only one switch is closed at the same time, a blanking time is introduced. During the blanking time the current runs through one of the diodes (D_A+ or D_A-), depending on the phase current direction, before it switches over to the MOSFET. There is also a voltage drop over the switch and the voltage does not change instant, it has a rise and fall time. In Figure 2.7 the wave form of the current is shown when the blanking time and voltage drop over the switch is considered. The solid black curve is for a positive phase current and the red dotted curve is for a negative phase current (with Figure 2.1 as reference for the current direction). Note that the voltage drop between T_A and D_A differs and that the blanking time is very small compared to a period and can therefore be neglected in the calculations [8].
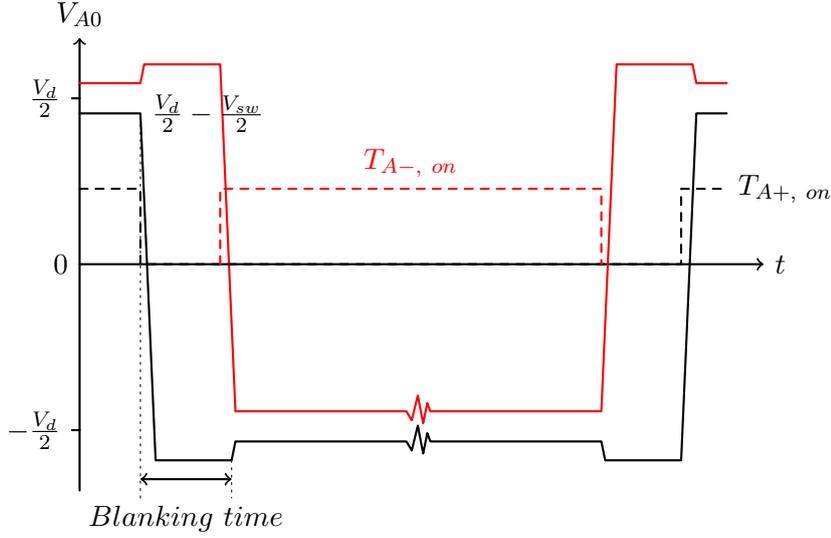
Figure 2.7: The switching when concerning the voltage drop over the switch and the blanking time. The black solid curve is for a positive phase current and the red dotted curve is for a negative phase current.

2.1.3 Conduction losses

The conduction losses in a MOSFET occurs due to the on-state resistance within the MOSFET. When the current runs through the MOSFET a power loss is obtained, and it is calculated by

$$P_{cond} = R_{DSon} \cdot \frac{I_{Drms}^2}{\sqrt{2}} \qquad (2.6)$$

where R_{DSon} is the on-state resistance and I_{Drms} is the rms value of the current through the component [9]. The conduction losses in the diode is not included in the conduction losses since the blanking time is much shorter than the period time. This is illustrated in Figure 2.7.

2.2 Temperature estimation

A maximum operation temperature is often given in the data sheets of a component. In order to estimate the temperature in a component the total thermal resistance between the junction and the ambient must be known. The equivalent circuit based on the thermal resistances is shown

10

in Figure 2.8 and the equation to calculate the total thermal resistance is given by

$$R_{\theta ja} = R_{\theta jc} + R_{\theta cs} + R_{\theta sa} \tag{2.7}$$

where $R_{\theta jc}$ is the thermal resistance between the junction and the case, $R_{\theta cs}$ between the case and the sink and $R_{\theta sa}$ between the sink and the ambient. The temperature in the component is then estimated by

$$T_j = P_{loss} \cdot R_{\theta ja} + T_a \tag{2.8}$$

where $P_{loss} = P_{cond} + P_{sw}$, i.e. (2.6) and (2.4) which is the total loss in the component and T_a is the ambient temperature [8].
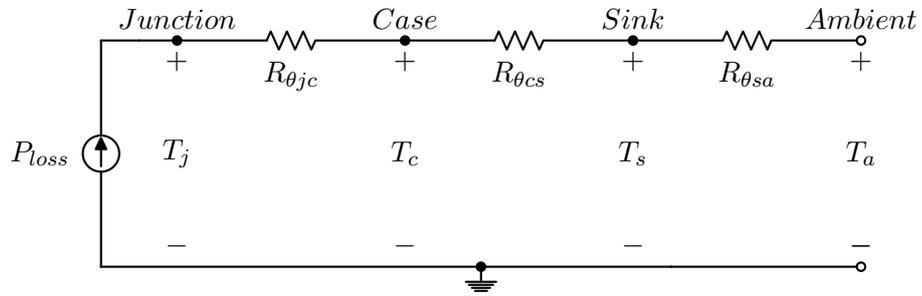
Figure 2.8: The equivalent circuit based on the thermal resistance in a MOSFET.

3

Design of three-phase inverter

3.1 Brushless dc motor

A *brushless dc* (BLDC) motor consists of a stator with windings and a rotor with permanent magnets. The phase currents feeds the stator windings and they induces a magnetic field in the machine. The induced magnetic field will then rotate around the stator due to the shape of the current fed from the inverter, see Figure 3.1. Since the rotor consists of permanent magnets it will rotate along with the magnetic field induced by the stator windings and the phase currents in normal operation [10].

The principle of driving a BLDC motor is to keep one of the phases floating and let the current flow in the other two phases. This makes six different states available for the machine and the principle is that one of the phases always should be positive and one of the phases should always be negative. Basically there is a positive current in one of the phases and during the same time the current is positive in that phase the other two phases has a negative current half of the time. When one of the two phases has a negative current the other one is zero and the other way around. The shape of the ideal back-*electromotive-force* (EMF), the currents in the phases and the states are shown in Figure 3.1 [11].

One factor that is not shown in the current wave forms in Figure 3.1 is the commutation time of the current. The rise, and fall, from zero to

13

the phase value is not instant, it has a certain commutation time until it reaches the conduction level. This commutation introduces a ripple in the torque, and this ripple can not be handled with a current controller [12].
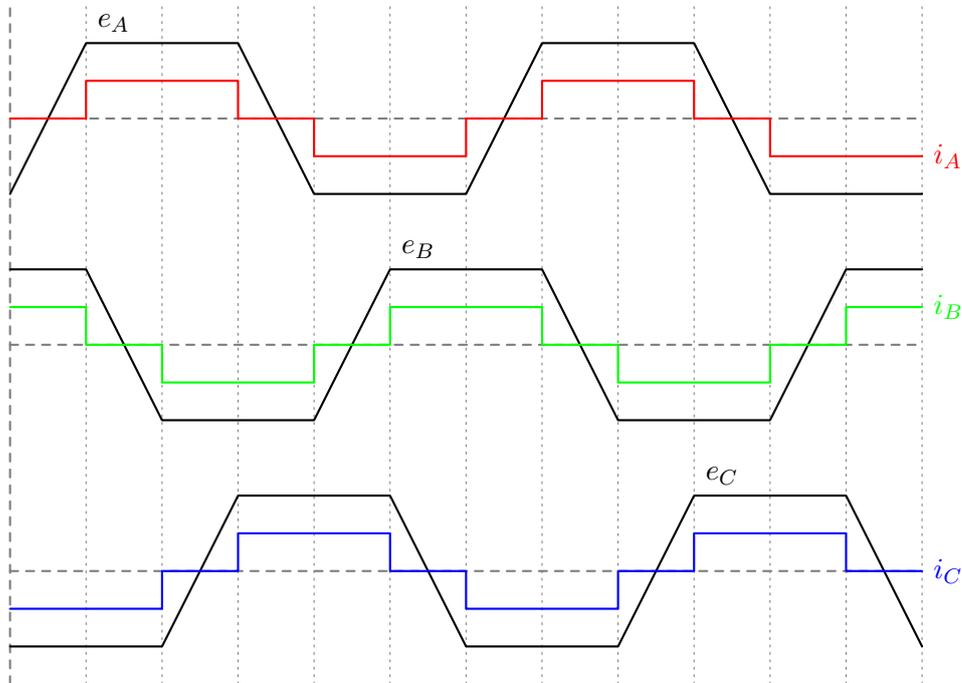
Figure 3.1: Ideal back-EMF shapes and phase currents in a BLDC.

Some of the motor parameters for the motor that the inverter is designed for were determined in a previous master thesis and some are provided by the supplier and are presented in Table 3.1 [7] [13]. The parameters will be used as a base for the inverter specifications. Since the electrical machine can not handle more than 70 V a suitable voltage to aim for would be 48 V so it can be applied in a mild hybrid automotive application.

3.2   MOSFET selection

MOSFETs classified for automotive applications were only available up to 50 V. Therefore MOSFETs in the same series with a 100 V rating are considered even though they miss the classification for automotive appli-

Table 3.1: Motor parameters in Y-connection.

Parameter	Notation	Value
No. of pole pairs	n_p	10
Resistance ($f = 0\ Hz$)	R	6.5 $m\Omega$
Self inductance	L_s	12.3 μH
Mutual inductance	L_M	0.7 μH
Permanent magnet flux linkage	Ψ	6.74 mWb
Inertia	J	2.13 $mkgm^2$
Damping	b	4.45 $mNms/rad$
ESC required	$I_{controller}$	250 A
Max Voltage	$V_{dc,\ max}$	70 V
Rpm per volt	Kv	150 rpm/V

cations. This is since it is a risk having the MOSFET rating to close to the operation point of the inverter at 48 V. Two different MOSFETs from the same supplier with a rating of 100 V were found suitable for the inverter. The main difference between the two MOSFETs is that one were chosen to have a low on-state resistance (R_{DSon}), which yields lower conduction losses. The other one were chosen to have low parasitic capacitance (C_{gd1} and C_{gd2}), which yields lower switching losses. Both of the MOSFETs have a TO-263 casing, which is a case for surface mounted components.

The parameters of the two different MOSFETs that will be used in the inverter are presented in Table 3.2 [14] [15]. Most of the parameters are defined at a certain operation point. In order to estimate the parameters at the specific operation point for the inverter a much deeper analysis must be made. The given values will only provide a rough estimation of the actual losses.

3.3 Inverter circuit board

The *printed circuit board* (PCB) for the inverter is made on a board with thermal substrate technique, meaning that the board consists of an aluminum plate with a thin dielectric layer on one of the sides. Over the

Table 3.2: MOSFET parameters.

Parameter	IPB025	IPB039
V_d $[V]$	100	100
I_D $[A]$	180	160
P_{tot} $[W]$	300	214
R_{DSon} $[m\Omega]$	2.5	3.9
Q_{rr} $[nC]$	232	135
t_{ri} $[ns]$	58	59
t_{fi} $[ns]$	28	14
$R_{\theta jc}$ $[K/W]$	0.5	0.7
C_{gd1} $[pF]$	16	13
C_{gd2} $[nF]$	1.728	1.225
$V_{plateau}$ $[V]$	4.3	4.6
R_G $[\Omega]$	1.9	1.4
$T_{op,\ max}$ $[^\circ C]$	175	175

dielectric layer there circuit layer is located. Since there only is a circuit layer on one of the sides of the board this types of PCB has to be single sided and it can only support surface mounted components [6]. The concept is illustrated in Figure 3.2. Note that there is no scale between the thickness of the different layers, the aluminum base plate is much thicker (approximately 7 mm) than both the dielectric (76 μm) and the circuit layer (70 μm) [20].

Since the dielectric layer is kept thin, the thermal resistance in the cooling system of the inverter is kept low. The dielectric layer, circuit layer and the solder to the component on the board together defines the thermal resistance $R_{\theta cs}$. The thermal resistance $R_{\theta sa}$ is in the aluminum board (0.58 $^\circ Ccm^2/W$) [20] and $R_{\theta jc}$ is the thermal resistance within the component (see Figure 2.8).

The layout of the inverter PCB is shown in Figure 3.3, where one horizontal row of the footprints refers to a phase leg of either the positive or negative switch in Figure 2.1. For example, if the row on the top refers to $A+$, the one in the middle refers to $B+$ and the one at the bottom

Surface mounted components
Circuit layer
Dielectric layer

Aluminum

Ambient
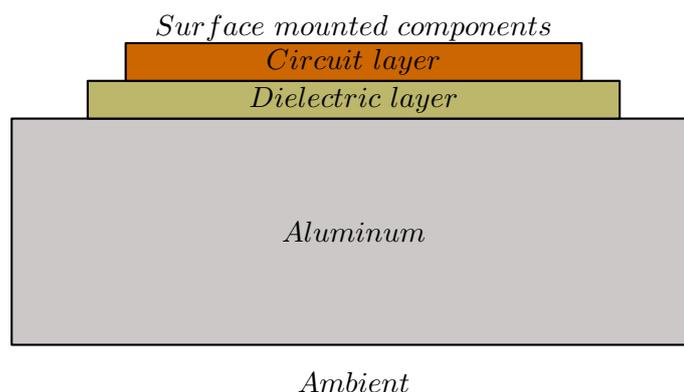
Figure 3.2: The different layers in a PCB with thermal substrate technique.

$C+$. One horizontal row of the six parallel footprints refers to one switch in Figure 2.1. The blue and green areas are where the copper trace of the PCB runs. The difference between the blue and the green area is that the blue are has an insulating layer over the copper trace while the green area has a tin layer so components could be soldered on to the trace. The green areas under the footprint of the MOSFETs and gate resistors are needed to be able to mount the components on the PCB. The green area that is not under a footprint is to enable mountings of cables for the phases and signals. The reason for having six MOSFETs in parallel is to make sure that the inverter can operate at a high enough current for the motor even if some of the MOSFETs are broken, or in any other way do not function. It is very hard to exchange MOSFETs on such type of PCB so an over dimension of the number of MOSFETs makes sense for this experimental design. One example of a type of experiment that might ruin the MOSFET is that if the plastic house over the silicon is removed to enable a thermal measurement directly on the silicon the MOSFET might not be able to function properly if to much material is removed.

The layout itself has a symmetric deigned so it can work on both the $+$ and the $-$ side, the difference is how the cables that feed current in and out of the PCB are mounted. If the trace at the top in Figure 3.3 refers to leg $A+$ in Figure 2.1 the middle one refers to $B+$ and the one at the bottom refers to $C+$, then the dc-current in should come on the upper

17

trace in each leg, and the three-phase current runs out in the lower trace of each leg. If the PCB is first turned 180 ° facing out of the paper, and then turned so it is facing in to the paper the PCB will work as the − side of the inverter once it is put under the + side and the phases are connected. The + side is shown in Figure 4.1 where the cables coming from under the inverter are connecting the − and the + side (the node before the phase in Figure 2.1).
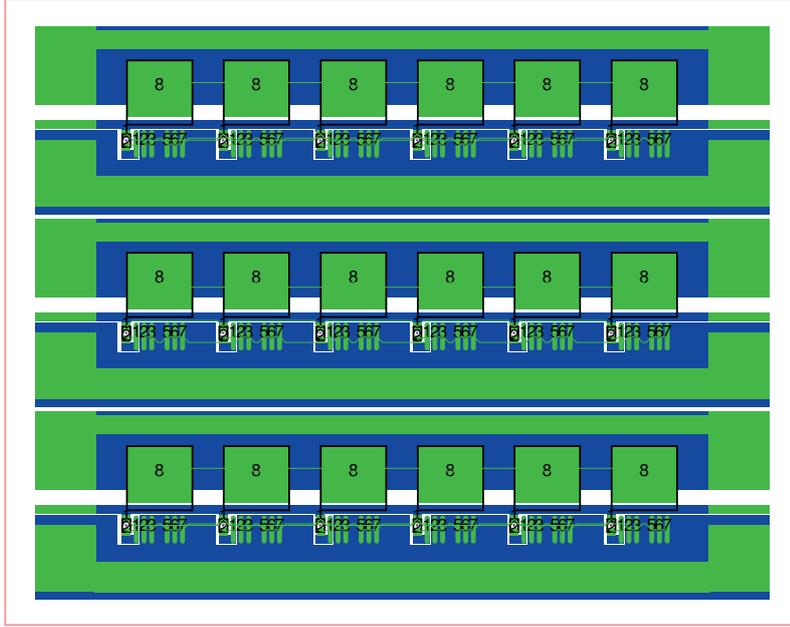
Figure 3.3: A CAD-drawing of the PCB layout.

When currents runs on a PCB the sheet resistance of the copper trace in the board must not be to high, this is to avoid losses in the trace. The width of the copper trace can be obtained through

$$w = \frac{l \cdot \rho_{Cu}(1 + \alpha_{Cu}(T - T_{20}))}{R \cdot d} \qquad (3.1)$$

where l is the length of the trace, ρ_{Cu} is the electrical resistivity of copper, α_{Cu} is the temperature coefficient of resistance in copper, T is the trace temperature, T_{20} is the temperature where ρ_{Cu} and α_{Cu} is defined, R is the resistance in the trace and d is the thickness of the trace [16].

18

The width of the copper trace can be calculated with (3.1). The resistance in the trace should be kept as low as possible, and in this application the lowest resistance of the two different MOSFETs is chosen to be a reference. The resistance used in the calculation of the trace width is set to the lowest R_{DSon} from Table 3.2. The length of the trace is set to 121 mm, according to [16] ρ_{Cu} (0.0175 $\Omega mm^2/m$) and α_{Cu} (0.00395 K^{-1}) is defined when $T_{20} = 20\ °C$ and the highest board temperature is taken from Table 3.4. The trace width can then be calculated to 12 mm. The reason for having such distance between the footprints of the MOSFETs is to enable thermal measurements in between the components on the board.

3.3.1 Cooling

A liquid cooling system will minimize the size of the inverter compared to an air cooled system [5]. The inverter PCBs are placed on both sides of an aluminum frame where the liquid will flow in between them. The reason for using the PCB as a lid for the liquid is to keep the thermal resistance in the inverter as low as possible since this will make sure the cooling medium is directly to the PCB. The PCBs are glued with silicone on the aluminum frame to make sure the liquid does not leak outside the inverter. A CAD-drawing of the frame is shown in Figure 3.4, where $h = 13\ mm$, $w = 114\ mm$ & $l = 141\ mm$ and the blue arrows indicates the liquid flow in the frame. The frame is designed to have a symmetrical flow of the cooling medium.

3.4 Dc-link capacitance

A three-phase inverter usually contains a dc-link capacitance, C_1 and C_2 in Figure 2.1. The function of this capacitance is to minimize the inductance to the MOSFET and to make sure the voltage ripple from the inverter out to the power source is kept under a certain level. This is to help keeping a pure dc voltage in case more components are connected to the same battery or local grid. The ripple currents occurs due to the PWM frequency of the inverter, the bus voltage and the load inductance. The capacitor bank must designed to withstand both a certain ripple current and also be large
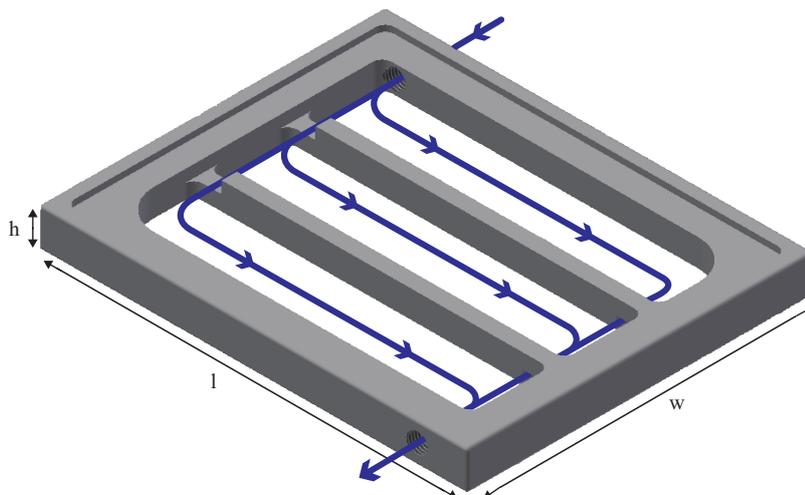
Figure 3.4: A CAD-drawing of the aluminum frame where the blue arrows shows the liquid flow through the frame.

enough to keep the voltage ripple under a certain level. The capacitance needed, with respect to the voltage ripple, can be calculated with

$$C = \frac{V_{bus}}{32 \cdot L \cdot \Delta V_{0.5t} \cdot f_{sw}^2} \qquad (3.2)$$

where L is the total phase inductance, $\Delta V_{0.5t}$ is the allowed peak to peak ripple voltage at 0.5 duty cycle, f_{sw} is the PWM frequency. The number, according to [17], 32 comes from a derivation of a three-phase motor drive circuit using a duty cycle of 0.5 and inserting the maximum dc ripple current in the voltage derivation. The duty cycle 0.5 is used in the derivations since this will give a maximum of the ripple [17].

According to (3.2) the capacitance can be calculated as long as the bus voltage and switching frequency are set, the inductance is known (see Table 3.1) and also an allowed voltage ripple is determined. In Figure 3.5 the capacitance in relation to the switching frequency is shown for a bus voltage at 48 V and an allowed voltage ripple at 5 %.

3.4.1 Hardware design

The capacitors in the dc-link must withstand the ripple current introduced in the system. To analyze the ripple current a Simulink® model, where
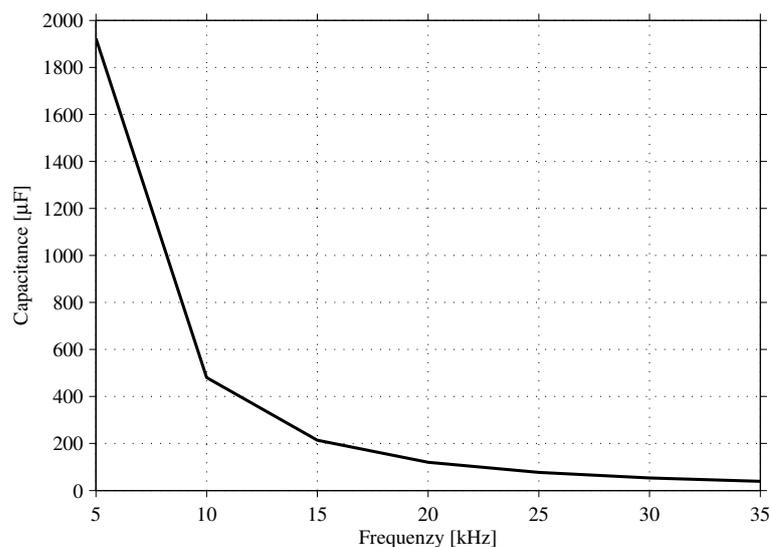
Figure 3.5: The capacitance in relation to the switching frequency at 5 % voltage ripple.

the electrical machine is modeled as a BLDC, is used. The simulations shows that the maximum rms ripple current will be around 100 A. This will yield two conditions for the dc-link capacitor bank, one is to have a total capacitance high enough to keep the voltage ripple under a certain level, 5 % in this case. The other criteria to fulfill is to be able to withstand the ripple current in the inverter circuit.

A PCB with room of 26 surface mounted capacitors, with a 2220 case, were designed. The dc-link capacitor bank can be partly seen in Figure 4.1. Ceramic capacitors with a capacitance of 22 μF would give the PCB a total capacitance of 572 μF. According to Figure 3.5 this would require a switching frequency around 10 kHz if the voltage ripple should stay under 5 %. A more accurate value of the lowest switching frequency needed to stay under 5 % voltage ripple can be calculated using (3.2), which is at 9.2 kHz. The reason behind choosing ceramic capacitors is to investigate its properties for this type of application, and also since the chosen type has a low ESR and ESL. Low values of those parameters makes the capacitor good to use in applications with a switching regulator that operates with a high switching frequency [18].

21

The capacitors chosen for the dc-link bank have a temperature rise around 15 $°C$ at a rms ripple current of 3.5 A and a switching frequency of 100 kHz. The switching frequency in the inverter will probably be lower than 100 kHz but this is the lowest frequency specified in [18]. If each capacitor can handle a rms ripple current of at least 3.5 A the dc-link bank will be able to handle $3.5 \cdot 26 = 91\ A$.

3.5   Drive circuit

The drive circuits, one for each leg in the inverter, is based on a standard drive circuit IC, $IR2010$, from International Rectifier. It has a floating channel design for bootstrap operation, fully operational to 200 V. The gate drive supply range is between 10 V and 20 V and it can drive a current of 3 A. The schematic of the drive circuit is shown in Figure 3.6 for one phase led and it is based on the typical circuit from the data sheet [19]. In Figure 3.6 the voltage source is illustrated with a battery since it is a probable solution if it is used in a dc-link voltage of 50 V. A schematic of the full circuit, including all three phases and the component values, but excluding the red components in Figure 3.6, is available in Appendix A.

The drive circuit for the MOSFETs is made to work both with 5 V and 15 V logic, which is enabled with two voltage regulators and a switch. The ports HIN and LIN from the driver chip is connected to a dSPACE system. The port SD is for shutting down the driver and it is connected to ground and 5 V on the PCB via a switch. It is operating when SD is connected to ground and it is shut down when it is connected to 5 V. Bootstrap capacitors is placed close to the outputs of the driver chip going to the top of the totem-pole. This is to make sure that the voltage can be pushed up to the operation point for the MOSFET with the help of the charged bootstrap capacitors. The output to the gate and source of the inverter is made with a totem-pole arrangement in order to use a lower gate resistor which will shorten the turn-on and turn-off times [8]. The gate and source cables that connects the drive circuit with the inverter PCB are twisted and spun four turns around a ferrite ring in order to get a common mode choke (shown in Figure 4.1). The zener diodes added to

the drive circuit is for additional over voltage protection.
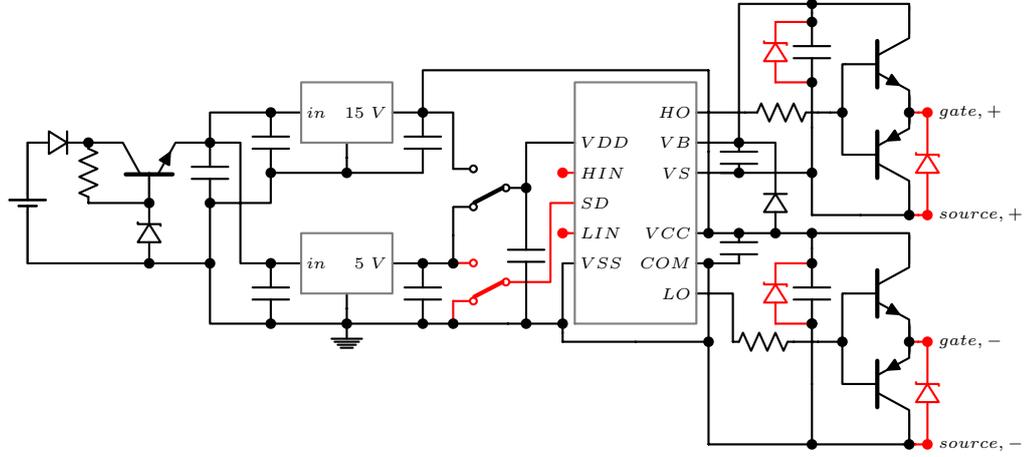
Figure 3.6: Schematic of the drive circuit with one phase, where the red components are added externally to the board.

3.6 Theoretical power loss analysis for the designed inverter

The power losses in the inverter is calculated with the parameters from the data sheets. The power losses are calculated for the highest output current of 300 A_{rms}, a dc-link voltage of 48 V and a switching frequency of 22.22 kHz. The conduction losses are calculated with (2.6) for a rms current of 300 A and the R_{DSon} values given in Table 3.2. The result of these calculations is presented in Table 3.3.

To calculate the switching losses the data from Table 3.2 are used along with (2.1)-(2.4), where I_{Don} and I_{Doff} is replace with I_{dc} from (2.5). The difference between the currents I_{Don} and I_{Doff} due to the current ripple, shown in Figure 2.6, is neglected so the current in the calculations is set to $\frac{300}{\sqrt{2}\cdot 6}$. The voltage is considered constant at 48 V, i.e. the voltage drop over the switch shown in Figure 2.7 are neglected. The result is presented in Table 3.3 and here it is shown that IPB025 has a lower conduction loss and higher switching loss than IBP039, which was discussed in Section 3.2.

23

Table 3.3: MOSFET losses.

Parameter	IPB025	IPB039
t_{fu1} $[ps]$	33	20
t_{fu2} $[ns]$	3.6	1.9
t_{fu} $[ns]$	1.8	0.95
t_{ru1} $[ns]$	0.34	0.19
t_{ru2} $[ns]$	37	18
t_{ru} $[ns]$	18	9
P_{sw} $[W]$	1.59	1.18
P_{cond} $[W]$	4.42	6.89
P_{tot} $[W]$	6.01	8.07

The temperature in the MOSFETs are calculated with (2.7) and (2.8), the ambient temperature used is set to 40 $°C$ and is referring to the temperature of the liquid in the cooling system. $R_{\theta jc}$ is taken from Table 3.2 and $R_{\theta cs}$ is estimated to be maximum 0.5 K/W in the initial calculations, but is to be changed when more data is gathered. $R_{\theta sa}$ is calculated to 0.7121 K/W with the thermal resistance of the board (0.58 $°Ccm^2/W$) [20] and the area of the MOSFETs (10.31 $\cdot$ 7.90 = 81.45 mm^2) [14] [15]. The results of the calculations are presented in Table 3.4.

Table 3.4: MOSFET temperature.

Parameter	IPB025	IPB039
$R_{\theta ja}$ $[K/W]$	1.71	1.91
T_j $[°C]$	50.28	55.43

According to the data in Table 3.2 the result of the calculations presented in Table 3.4 shows that the temperature in the MOSFETs are much lower than the maximum operation temperature. It can be noted that the temperature rise is 10.28 $°C$ respectively 15.43 $°C$ for the two different MOSFETs. This is, however, only rough calculations that were used to design the inverter.

4

Thermal investigation

4.1 Measurement setup

The main approach to validate the initial calculations were to measure the inlet and outlet water temperature of the frame, with the help of a *Fluke Hydra* $(2620A)$ and $PT100$ sensors, along with photos of the board taken with an infrared camera for thermal images. For this investigation three different rms-currents will be validated; 75, 100 and 150 A. The reason for not going higher is that the dc-link capacitor bank gets very warm. An image of the inverter, drive circuit and temperature sensors is shown in Figure 4.1. The temperature sensors are visible in the tubes at A in the figure. The inverter PCB glued on the frame is indicated with B. C refers to the dc-link capacitor bank, D to the ferrite rings around the gate signal cables and E the drive circuit.

The phase load for the tests consists of different cables with a total length of 12 m and a radius of 0.5 cm. The cables were also spun seven turns around a toroidal iron powder core with an A_L value of 260 nH. The three phases of the load is connected in a Y connection. The total phase-resistance of the cables can be calculated with

$$R = \frac{l \cdot \rho_{Cu}}{\pi r^2} \tag{4.1}$$

where l is the length of the cable, ρ_{Cu} is the electrical resistivity of copper
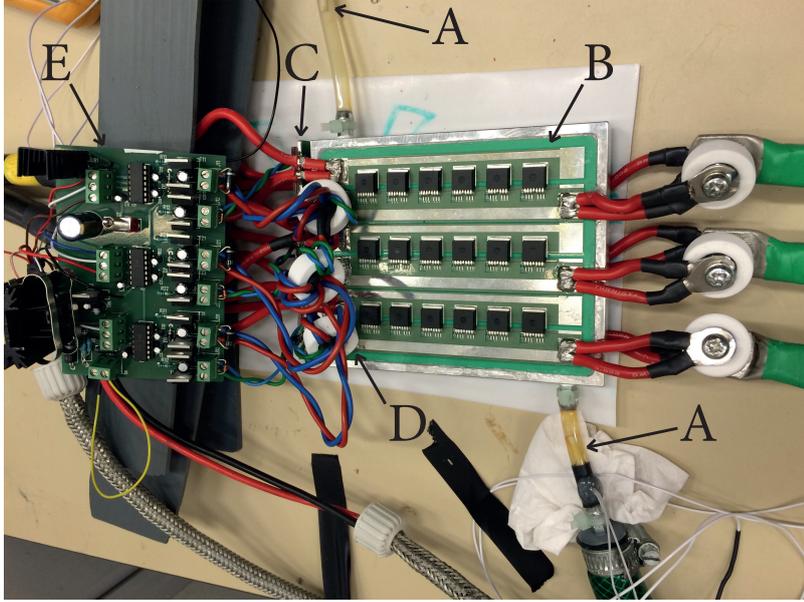
Figure 4.1: The setup for the measurements. A is the temperature sensors, B is the inverter PCB, C the dc-link capacitor bank, D is the ferrite rings and E is the drive circuit.

and r is the radius of the cable. The phase inductance from the toroidal core is obtained by

$$L = A_L \cdot N^2 \tag{4.2}$$

where N is the number of turns the cable is spun around the core. Using (4.1) and (4.2) will yield a phase load of 2.6 $m\Omega$ and 12.74 μH. The cables are spun seven turns around the toroidal cores since that will yield the inductance closest to the inductance in the motor presented in Table 3.1. The resistance from the cables will, however, yield a resistance that is about 2.5 times lower than in the motor.

The drive circuit is controlled with a dSPACE system where a three phase PWM is generated. The switching period time is set to 45 μs, which corresponds to a switching frequency of 22.22 kHz, and in order to get the currents closer to a sinusoidal shape dead band compensation [8] were implemented in the code. There are four different parameters that can be changed with a slider in the dSPACE window; a scaling of the voltage amplitude, the switching frequency, the angle of the dead band compensation

and the current amplitude. A plot of the three-phase currents with IPB039 MOSFETs, at $I_{rms} = 150$ and $f = 50\ Hz$, are shown in Figure 4.2. In the picture it can be noted that there are some switching ripple in the currents and that the shape is close to a sinusoidal shape.
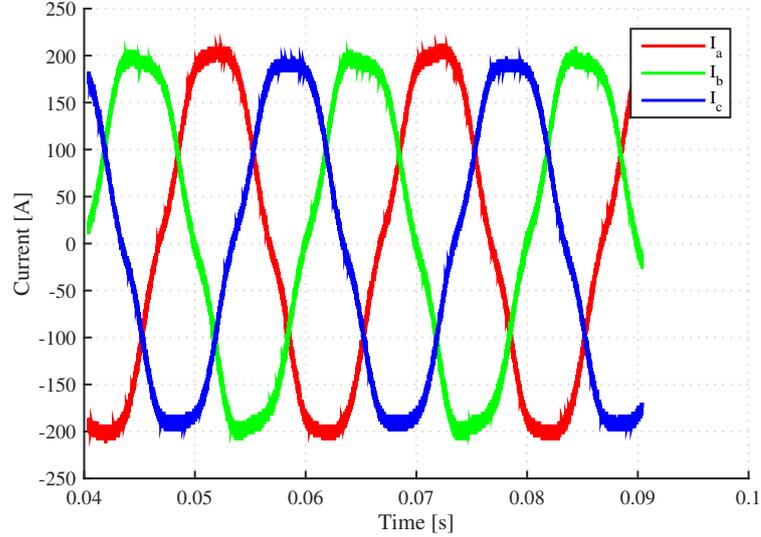
Figure 4.2: The shape of the three-phase currents with IPB039 MOSFETs at $I_{rms} = 150$ and $f = 50\ Hz$.

4.2 Temperature and power loss measurements

In Figure 4.1 the temperature sensors are indicated with A. In order to get an accurate value of the delta temperature between the inlet and the outlet a calibration must be made. The calibration will yield an offset between the two sensors. The calibration will not indicate if any of the temperature sensors shows the correct temperature but the interesting result will be to have an accurate temperature difference between the inlet and outlet to be able to estimate the heat (power loss) taken up in the cooling medium.

The temperature sensors were calibrated between each measurement to make sure that the offset is close to the same during the whole experiment.

The data from the series of measurements are presented in Table 4.1. The temperature difference, noted ΔT, is calculated

$$\Delta T = T_{out} - T_{in} - T_{offset} \tag{4.3}$$

where T_{out} is the value from the sensor at the outlet of the frame, T_{in} is from the sensor at the inlet and T_{offset} is the difference between the input and output when no current is running in the inverter. Using (4.3) will yield the results presented in Table 4.1.

Table 4.1: Data from temperature measurements on the MOSFETs, T_{offset} is the offset between the sensors and ΔT is resulting temperature difference.

I_{phase} [A_{rms}]	T_{in} [°C]	T_{out} [°C]	T_{offset} [°C]	ΔT [°C]
		IPB025		
0	39.36	43.06	3.70	-
75	39.26	45.04	-	2.08
0	44.55	48.32	3.77	-
100	46.05	52.93	-	3.11
0	41.04	44.82	3.78	-
150	42.66	52.78	-	6.34
		IPB039		
0	41.84	46.48	4.64	-
75	42.36	49.58	-	2.58
0	41.78	46.43	4.65	-
100	41.35	50.24	-	4.24
0	39.65	45.16	5.51	-
150	38.86	52.39	-	8.02

In order to estimate the efficiency of the liquid cooling system the water flow rate must be known. A test were performed where the time was measured when one liter of water were pumped trough the system. The data from the tests are presented in Table 4.2. The water flow determination test were made five times each for the two frames. The mean value of these measurements will be used when calculating the power loss. Along with

28

this information the thermal energy required to heat up one gram of water one degree Kelvin is used. This value depends on the temperature of the water but it is around 4.185 J [21]. This mean value should also be divided by 1000 in order to get the flow per gram instead of liter (assuming that one liter of water weights 1 kg). The power loss taken up by the water is then estimated by

$$P_{water} = \frac{\Delta T \cdot 4.185}{t_{mean}} \tag{4.4}$$

where t_{mean} is the mean value of the time in Table 4.2 divided by a factor of 1000.

Table 4.2: Data from the flow test where one liter of water were pumped trough the system.

Test	IPB025 $[s]$	IPB039 $[s]$
1	100.69	116.22
2	101.02	116.74
3	101.85	117.46
4	102.00	116.07
5	100.69	116.34
Mean	101.25	116.57

In Figure 4.3 the result of the calculations of the total power taken up by the water using (4.4) is presented. In the figure the theoretical power loss calculated with (2.1)-(2.4), where I_{Don} and I_{Doff} is replace with I_{dc} from (2.5), and by using the data from Table 3.3. The difference between the dashed and solid lines in the figure shows that the parameters presented in the data sheet probably are not true for the operation points used in the inverter. The result might also raise a doubt to the equations and method used to calculate the losses. There are also a risk for the measurements to differ from the actual power loss, for instance there can be errors in the actual water flow rate and also the accuracy of the delta temperature of the inlet and outlet of the frame. As discussed in Section 2.1.1 there is a need of measuring the time parameters, for the application, in order to get a better estimation of the switching losses.
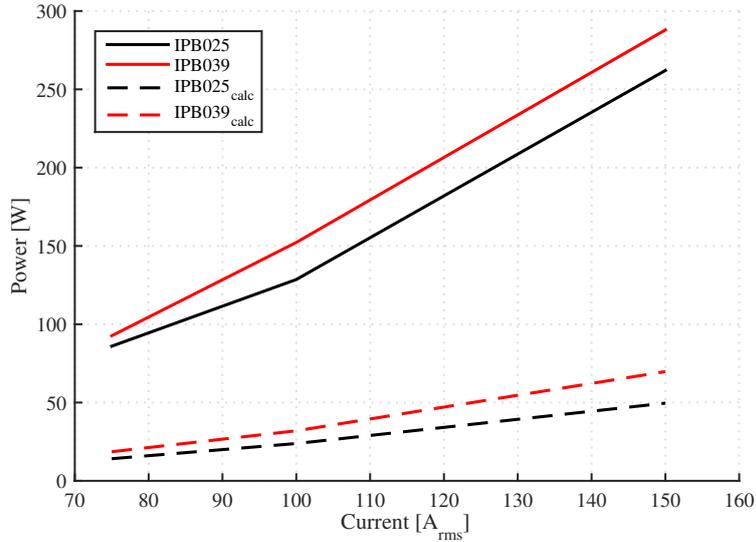
Figure 4.3: The power loss taken up by the water in the cooling system as solid lines. The dashed lines corresponds to calculations made with parameters from the data sheets.

An image taken with the infrared camera with $I_{phase} = 150\ A_{rms}$ on the inverter with IPB039 are shown in Figure 4.4. The transistor in the top left corner represents the calculations best since the water temperature is closest to 40 $^\circ C$ at the input of the frame. If the temperature is compared to the the value presented in Table 3.4 a clear difference in the power loss is obtained. There might also be an incorrect value of the thermal resistance, and the unclear parameter there would be $R_{\theta cs}$ since it is not a value specified in any data sheet. The temperatures from all the measurements are presented in Table 4.3, where MOSFET 1 is at the top left corner in Figure 4.4, and then the numbering goes on to the right and then down, MOSFET 18 is in the lower right corner.

Looking in Table 4.3 there can be noticed that the frame with IPB025 seams to have a temperature rise in the MOSFETs that is distributed with the lowest temperature close to the inlet and the highest close to the outlet. MOSFET 1 to 6 is leg $A+$, 7 to 12 is $B+$ and 13 to 18 is leg $C+$. Looking at IPB039 it can be obtained that leg $B+$ is contains the highest temperatures of the MOSFETs. There might be a difference in the

30

Figure 4.4: Thermal image of the inverter with IPB039 MOSFETs at phase current of 150 A_{rms}.

amount of silicon that were pushed down in the liquid channels. Since the frame with IPB039 has a lower water flow (see Table 4.2) there might be a difference in the flow in the channel under leg $B+$ in the two different frames, and this would influence the cooling.

4.2.1 Thermal resistance

The difference between the temperature of MOSFET 1 and the temperature of the inlet water is about the same as the temperature difference between MOSFET 18 and the outlet, seen in Table 4.3. This data can be used to investigate the thermal resistance of the system. By using (2.8), the inlet temperature as T_a, the temperature of MOSFET 1 as T_j and P_{loss} as a $\frac{1}{36}$ part of the total power loss from Figure 4.3 the total thermal resistance, $R_{\theta ja}$, can be estimated. For MOSFET 18 the outlet temperature is used as T_a and the MOSFET temperature as T_j.

Estimations were made for each current level and for each MOSFET type and in Figure 4.5 the average total thermal resistance of MOSFET 1 and 18 is shown as function of the measured average power loss. In Figure 4.5 also the remaining thermal resistance, when the MOSFET and the aluminum plate resistance is removed from the total, is plotted for the two

31

Table 4.3: Temperature measurements for IPB025 and IBP039.

$I_{phase}\ [A_{rms}]$	75	100	150	75	100	150
MOSFET	$T_{IPB025}[°C]$			$T_{IPB039}[°C]$		
$T_{in} + \frac{T_{offset}}{2}$	41.11	47.96	44.55	44.68	43.68	41.62
1	43.8	51.8	64.5	46.8	47.9	51.8
2	43.9	51.9	62.8	46.4	47.2	50.5
3	44.1	52.1	62.3	47.3	48.6	52.9
4	44.7	53.8	65.4	48.4	50.6	57.0
5	45.0	55.3	67.3	48.9	51.3	59.1
6	44.6	55.8	68.6	46.2	49.9	58.3
7	44.3	54.8	65.5	48.5	51.3	54.0
8	45.5	56.5	69.8	49.5	52.7	54.7
9	46.5	57.6	72.0	50.3	54.3	58.9
10	46.9	58.3	73.3	50.7	55.1	61.1
11	46.7	58.3	73.0	50.9	55.5	62.4
12	45.5	57.3	70.6	50.6	55.1	62.3
13	43.9	54.1	62.6	47.7	50.3	54.0
14	45.3	56.1	67.8	48.5	51.9	54.0
15	46.3	58.0	72.0	49.1	51.9	54.3
16	47.0	58.8	73.4	49.3	52.3	55.5
17	46.9	58.4	73.4	49.4	52.9	57.0
18	46.0	57.3	70.9	49.8	54.1	60.3
$T_{out} - \frac{T_{offset}}{2}$	43.19	51.05	50.89	47.26	47.92	49.64

MOSFET types.

As can be seen from the figure the thermal resistance is increasing with the power loss, it differs between the MOSFETs and the remaining resistance have negative values. The negative values are not reasonable but they can depend on measuring errors or that a too large value is used for the thermal resistance of the aluminum plate. This is due to that the MOSFET area is used to calculate the resistance, but in reality the heat would spread over a larger area which would reduce the resistance. The difference between the MOSFET types can be due to the difference in the

water flow between the two setups, see Table 4.2, or measuring errors.

Comparing to the data in Table 3.4 with the result in Figure 4.5 a difference is noticed. This indicates that the value of the thermal resistance used in the calculations is wrong, it is too high. Since $R_{\theta cs}$ should be approximately the same for the two boards (only a difference of the thermal resistance withing the actual MOSFET) the mean value of the two different MOSFETs is calculated to 0.15 $[K/W]$.
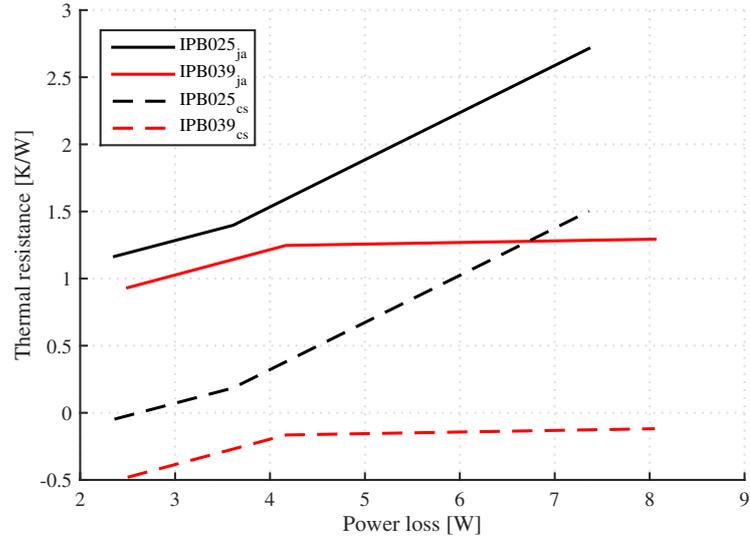

Figure 4.5: The average thermal resistance ($R_{\theta ja}$ and $R_{\theta cs}$) of MOSFET 1 and MOSFET 18 for different MOSFET power losses. The MOSFET power loss is taken as a $\frac{1}{36}$ part of the power loss in Figure 4.3.

4.3 Temperature calculation with measured values

The calculations presented in Figure 4.3 are based on the information provided in the data sheets of the MOSFETs. As was noticed, the calculated values do not agree with the measurements. To improve the temperature rise calculations the thermal resistance ($R_{\theta cs}$) between the component and the board is lowered to 0.15 K/W (see Section 4.2.1). To improve the

switching loss calculations, some of the parameters for the calculations in Section 3.6 were measured during the experiments and they are presented in Table 4.4. In Figure 4.6 the plots for MOSFET 13 (with reference to Section 4.2) of the fall and rise of the current and voltage that were used to extract t_{fu}, t_{ru}, t_{fi} and t_{ri} for the case with 150 A_{rms} phase current in the inverter with IPB039 MOSFETs and the measurement is shown. The rise and fall times of the voltage and current in Figure 4.6 are extracted by stepping between the values in the plot in MATLAB. The parameters t_{ri} and t_{ru} was measured after the first overshoot. The difference between the parameters from data sheet (in Table 3.2 and Table 3.3) and the values presented in Table 4.4 is probably due to difference in operation points along with ideal measurements from the supplier. The extracted values from the plot are probably not very accurate since it is hard to know how the supplier did their measurements.

Table 4.4: Updated parameters from the measurements.

I_{phase} [A_{rms}]	V_d [V]	t_{fu} [ns]	t_{ru} [μs]	t_{fi} [ns]	t_{ri} [μs]
		IPB025			
75	9.5	39.0	2.39	166	1.49
100	12	34.0	2.14	195	1.35
150	15	46.0	1.93	186	1.12
		IPB039			
75	10	39.0	1.62	167	1.96
100	12	22.0	1.52	102	1.20
150	16	34.8	1.42	194	0.85

The over voltage seen in Figure 4.6b is caused by the inductance in the inverter PCB, in the cables between the inverter PCB and also from a ferrite ring that is placed around the bolt connecting the load with the inverter (see Figure 4.1). This voltage spike is proportional to the inductance in this circuit according to

$$V = L\frac{di}{dt} \tag{4.5}$$

where L is the inductance. An RC snubber mounted over the ferrite ring would probably damp the voltage overshot. The RC snubber prototypes

34
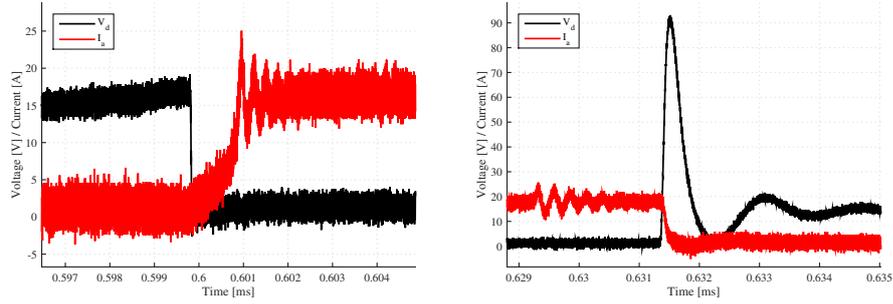
(a) The fall of the voltage and rise of the current.

(b) The rise of the voltage and fall of the current.

Figure 4.6: The switch on and off of the MOSFET IPB039 at a phase current of 150 A_{rms}. The measurment is done over MOSFET 13.

developed within the project did, however, not help very much. The resistors that can withstand higher power might be to inductive for this application.

In Figure 4.7 the result of the updated calculations are shown along with the mean value of MOSFET 1-3 from Table 4.3. The calculations are made to represent the temperature in one MOSFET since it is hard to know the temperature of the water when it flows in the frame. Therefore the measurement reference is the first MOSFETs when the water goes in to the frame, where the inlet temperature used is $T_{in} + \frac{T_{offset}}{2}$. The calculations shows that the MOSFET temperature should be around 50 $°C$ for IPB039 at a phase current of 150 A_{rms}, which is close to the temperature in Figure 4.4. Figure 4.7 also shows that the delta temperature between the measured and calculated values are about the same except for the measuring point at 150 A_{rms} for IPB025. For the rest of the measuring points the delta temperature is not more than 2 $°C$. A plot of the temperature difference is show in Figure 4.8.

The difference in the calculated and measured values are plotted in Figure 4.8. For IPB039 the difference is close to linear, but for IPB025 it does go up and down. It is hard to say if this is due to errors in the measurement with the infrared camera or errors while extracting the rise and fall times. One explanation that the difference is positive for most
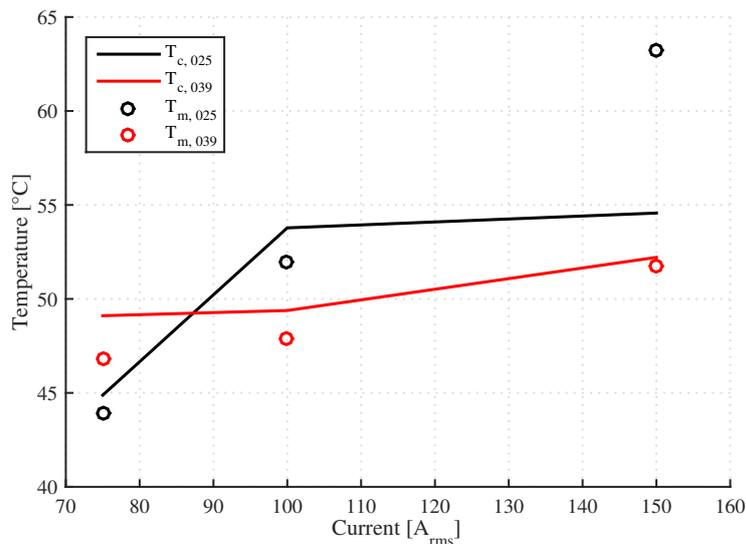
Figure 4.7: Calculated (T_c) and measured (T_m) MOSFET temperature.

cases might be that the calculation refers to the temperature in the silicon of the MOSFET and not the plastic cover which the infrared camera sees. If access directly to the chip in the MOSFET was enable the result might be closer to the calculated values. It is most likely that the cover over the chip has a lower temperature than the actual chip or junction.

4.4   Dc-link capacitor bank

During the measurements the dc-link capacitor bank were over 110 $°C$, which is the maximum temperature shown by the infrared camera. To investigate why the capacitors became this warm a measurement of the current right before and right after the capacitor bank were made. There were, however, not enough current probes available to measure on all three phases. This is because the short distance between the inverter PCB and the capacitor bank and the high current. Therefor the measurement were made on only one of the phases, which will not give the actual total ripple current. The current probes were placed around the thick red cables to the left and to the right of C in Figure 4.1, where it also is shown that the distance between the inverter PCB and the capacitor bank is short. A
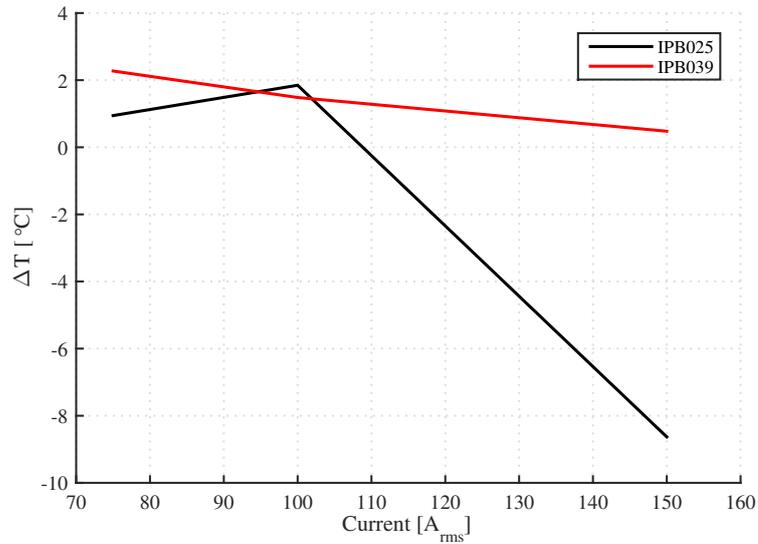
Figure 4.8: The temperature difference between the calculated and measured values.

calculation made from the measurement gives an rms current of 144 A and a plot of the measured current is shown in Figure 4.9. The figure shows the current going in to the capacitor bank, i.e. the current going in to C_1 in Figure 2.1.

The calculations and simulations presented in Section 3.4 shows a lower value of the ripple current but the measurement indicates that the actual ripple current could be higher. It is, however, hard to evaluate how much higher the ripple current is since the measurement only could be made on one phase. According to Figure 4.10, extracted from [18], a higher rms current, in this case the rms value of the ripple current, will yield higher temperature in the capacitors since the temperature rise in the capacitors is proportional to the rms current in square [18]. A temperature rise of around 90 $^{\circ}C$ would yield an rms current of around 8.3 A in each capacitor. The simulations and calculations showed a total rms current of around 100 A which would mean that the rms current in each capacitor would be around 3.8 A, corresponding to a temperature rise of around 20 $^{\circ}C$. The ambient temperature around the capacitor bank is probably higher than 20 $^{\circ}C$ since the capacitors itself heats up the ambient.
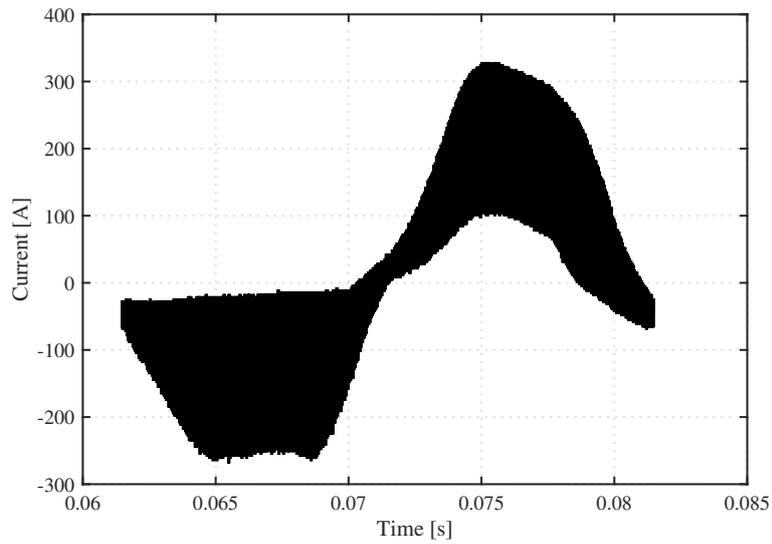
**Figure 4.9:** The data from the measurement of the ripple current.
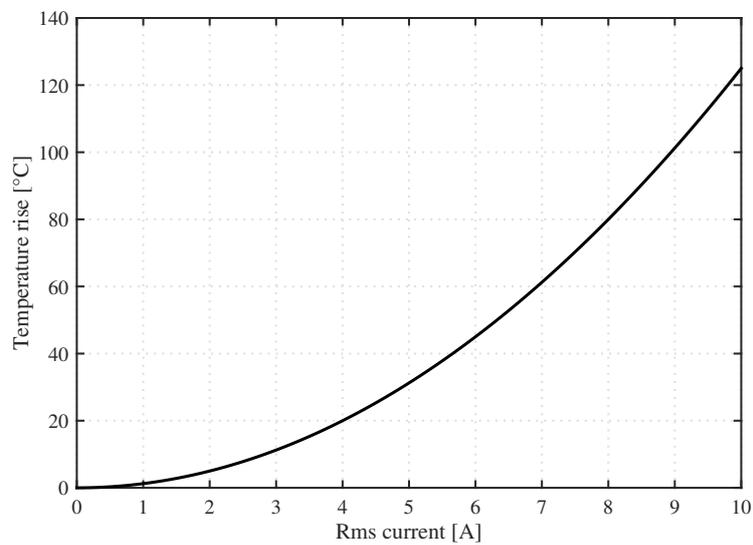
Figure 4.10: The relation between temperature rise and rms current in a capacitor from the dc-link bank.

5

Conclusion

The aim of this project was to build a compact inverter with thermal substrate technique, dc-link capacitor bank and drive circuit for the inverter. An evaluation of the hardware have been made along with calculations and simulations. The inverter can feed a sinusoidal current, shown in Figure 4.2, which shows that the drive circuit together with a dSPACE-system enables the inverter to operate properly.

The thermal properties of the inverter has been investigated and the results of the power loss taken up in the water running through the frame is shown in Figure 4.3 and they are increasing linearly with an increased current. At a phase current of 150 A_{rms} the cooling system takes up around 270 W. The difference, with updated measured time parameters, in the measured and calculated temperatures are shown in Figure 4.7. It is shown that the calculated values are a bit higher, not more than 2 $°C$ for most cases, than the measured, which might be due to that the infrared camera measures on the plastic cover of the MOSFET while the calculations refers to the silicon within the MOSFET. Using the time parameters from the data sheet did not reflect the actual rise and fall times of the voltage and current. The greatest difference is for the voltage rise where it is as high as 2.37 μs. The unknown parameter $R_{\theta cs}$ have been calculated from measurements to be around 0.15 $[K/W]$.

The dc-link capacitor bank gets warm when the inverter is in operation.

This depends on that the measured ripple current is much higher than the calculated ripple current that was used to design the dc-link capacitor bank. A higher ripple current will increase the losses and the temperature of the capacitors.

5.1 Future work

There are several possible ways to continue working with the inverter, some more critical than others. The voltage overshoot seen in Figure 4.6b must be dealt with since the MOSFETs are rated for 100 V and the voltage spikes were as high as 120 V. The RC snubbers iterated in the thesis did not damp the spikes so more work needs to be done here. The down side with using resistors rated for higher power is that they tend to be highly inductive. The balance between the resistance, capacitance and power dissipation in the RC snubber takes time to iterate, therefore simulations and theoretical calculations could be made to get a better base to work from.

The data sheet of the capacitors used in the dc-link did not give an accurate power dissipation. The surface temperature of the capacitors were above 110 $°C$ during the measurements. Since the ambient temperature increases when the capacitor temperature increases the inverter should be placed so the air can circulate, either by the help of a fan or by a natural placement. Soldering two dc-link PCBs together and double the number of capacitors and the total capacitance would also help to decrease the temperature.

All the modifications made on the drive circuit might not be needed so an investigation of which, if any, of the zener diodes that can be removed could be made. It is not necessary but if more drive circuits is about to be mounted together it is good to be sure which components to add and which components to skip. Since the ferrite rings between the inverter and the drive circuit were added after the zener diodes, the rings alone could solve the problem with overheated components in the drive circuit. This could be tested with a drive circuit where the additional zener diodes are not mounted. Zener diodes on the output of the drive circuit is, however,

good to have even if the ferrite rings is enough.

To make sure that the temperature in the MOSFET does not exceeds the rated maximum operation temperature the case must be removed. This is since the most smooth way to get the temperature in the MOSFET is to use an infrared thermal camera. The case of the MOSFETs are molded in one piece which will complicate the opening of them.

In parallel with the master thesis there have been projects developing a software that will control the inverter when it feeds the electrical motor. The software needs to be tested together with a well working drive circuit and when the voltage spikes over the MOSFETs can be damped.

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Appendices

Schematic of the drive circuit