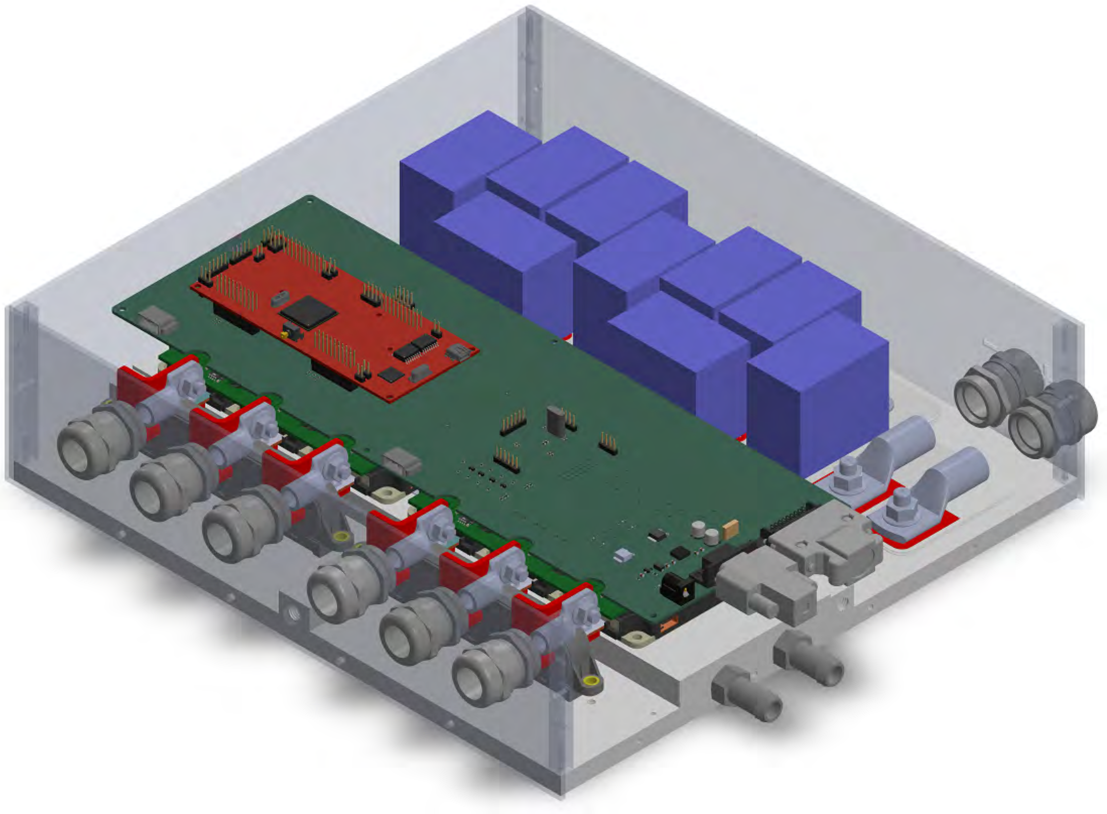

The Design and Performance Evaluation of a Double-three-phase Inverter

DC-Link Thermal Evaluation and Lifetime Estimation

Master's thesis in Electric Power Engineering

Jedsada Yodwong

DEPARTMENT OF ELECTRICAL ENGINEERING
CHALMERS UNIVERSITY OF TECHNOLOGY
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Cover: 3D model of the double-three-phase inverter.

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Abstract

This thesis presents the design, implementation, and experimental evaluation of a double–three–phase traction inverter based on silicon carbide (SiC) power modules for heavy-duty electric vehicle applications. The work focuses on achieving high power density and robust thermal performance through co-design of the DC-link capacitor bank and laminated busbar structure. Two alternative DC-link layouts were investigated: Case I, with capacitors mounted above the busbar, and Case II, with capacitors in direct contact with the housing.
A comprehensive methodology combining analytical modeling, MATLAB/Simulink simulations, and laboratory testing was employed. Open-loop SVPWM tests validated inverter functionality, while thermal performance was assessed under RMS ripple currents of 156 A_{rms} and 300 A_{rms} at 10 kHz under 2 thermal conditions: with and without liquid cooling. Results show that liquid cooling significantly reduces busbar temperatures (up to 67% in Case I), whereas capacitor hot-spot remain dominated by internal thermal paths, limiting improvements to 18–21%. Lifetime analysis, based on datasheet models, experimental data, and MATLAB/Simulink model, indicates that capacitor lifetime is highly sensitive to temperature. Under ideal assumptions, the lifetime at 55 °C ambient was estimated at 24.8 years, whereas experimentally adjusted scenarios ranged from 8.7 to 13.1 years. Liquid cooling improved lifetime by up to 50% at high ripple currents compared to the worst case, emphasizing the importance of accurate thermal modeling and integrated cooling strategies for next-generation traction inverters.
The findings underscore the importance of integrated electro–thermal design for reliability in high-power SiC-based traction inverters. Future work includes closed-loop control implementation, and EMI/EMC characterization.

Keywords: SiC MOSFET, double–three–phase inverter, DC-link capacitor, laminated busbar, thermal management, lifetime estimation, electric heavy-duty vehicles.

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I am very grateful to my wonderful team for welcoming me from the very beginning, making me feel a true sense of belonging, and supporting me throughout this journey.
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To all the friends I have met during this journey, thank you for making my experience in Sweden brighter and memorable.
Finally, I would like to thank my relatives for their trust and support in pursuing my ambitions abroad. Above all, I am deeply indebted to my mother, Supan Rattanated, for her unconditional love and belief in me, all that is good in me began with her.

Jedsada Yodwong, Gothenburg, September 2025

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

ADC	Analog-to-Digital Converter
BES	Battery Energy Storage (contextual; used generically)
CMRR	Common-Mode Rejection Ratio
DC	Direct Current
DCB	Direct Copper Bonded (substrate)
DC–Link	Intermediate DC energy buffer between source and inverter
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FEM	Finite Element Method
GaN	Gallium Nitride
HDT	Heavy-Duty Truck
HHDDT	Heavy Heavy-Duty Diesel Truck
HF	High Frequency
HV	High Voltage
IGBT	Insulated-Gate Bipolar Transistor
IR	Infrared (thermography)
LCR	Inductance–Capacitance–Resistance (meter)
LV	Low Voltage
MLCC	Multilayer Ceramic Capacitor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MPPF	Metallized Polypropylene Film (capacitor)
OC	Over-Current (flag)
PCB	Printed Circuit Board
PD	Partial Discharge
PI filter	Two-capacitor/one-inductor input filter (C–L–C)

PLECS	Piecewise Linear Electrical Circuit Simulation
PM	Permanent Magnet
PMSM	Permanent-Magnet Synchronous Machine
PWM	Pulse-Width Modulation
Q	Quality factor of a resonant network
RCG	Resonance Current Gain (multi-port DC-link metric)
RL	Resistive–Inductive (load)
Si	Silicon
SiC	Silicon Carbide
SNR	Signal-to-Noise Ratio
SOA	Safe Operating Area
SPI	Serial Peripheral Interface
SVPWM	Space-Vector Pulse-Width Modulation
TC	Thermocouple
TIM	Thermal Interface Material
VSI	Voltage Source Inverter
WBG	Wide-Bandgap (semiconductor)

Nomenclature

Below is the nomenclature of indices, sets, parameters, and variables that have been used throughout this thesis.

Symbols

A	Plate/electrode area of a capacitor	m^2
C	Capacitance	F
C_{busbar}	Distributed capacitance of a laminated/parallel-plate busbar	F
C_{DUT}	Capacitance of the device under test (DC-link under evaluation)	F
C_p	Dominant resonant capacitor in the parallel tank	F
C_{total}	Net series capacitance of C_p and C_{DUT}	F
$D(\alpha)$	Duty cycle as function of electrical angle α	–
$E_{\text{on}}, E_{\text{off}}, E_{\text{rr}}$	Turn-on, turn-off, and reverse-recovery energies	J
$\varepsilon_0, \varepsilon_r$	Vacuum permittivity, relative permittivity	–
δ	Skin depth	m
d	Dielectric thickness	m
f, f_r	Frequency; resonant frequency	Hz
$G_{T_a,h}(s)$	Ambient-to-hotspot thermal transfer (low-pass)	–
I, I_{rms}	Current; RMS current	A
$I_{\text{rp,max}}$	Permissible ripple current (SOA bound)	A
i_C, i_{inv}	Capacitor current; total inverter current	A
L	Inductance	H
L_{loop}	Commutation loop inductance	H
L_p	Parallel-tank inductance	H
M	Modulation index	–
P_{loss}	Average (electro-thermal) loss	W
Q	Tank quality factor	–
R_{TH}	Thermal resistance (hotspot to sink/ambient)	K/W

R_s	Series (ohmic) resistance in capacitor model (ESR)	Ω
R_p	Parallel insulation/leakage resistance in capacitor model	Ω
$R_{\mathrm{DS(on)}}$	MOSFET on-state resistance	Ω
T_a, T_h	Ambient temperature; capacitor hotspot temperature	°C
ΔT_{hot}	Hotspot temperature rise	K
τ_{th}	Thermal time constant	s
$v_C, V_{DC}, V_{\mathrm{out}}$	Capacitor voltage; DC-link voltage; output phase voltage	V
ω	Angular frequency $2\pi f$	rad/s
$Z_{T_h}(s)$	Hotspot thermal impedance transfer function	K/W

Capacitor–loss and EMI quantities

$\mathrm{ESR}(f, T)$	Equivalent series resistance (freq./temp. dependent)	Ω
ESL	Equivalent series inductance	H
$\tan\delta$	Dielectric loss tangent	–

Busbar / material parameters

w, l	Conductor width and length (busbar)	m
ρ	Electrical resistivity of conductor	$\Omega \cdot \mathrm{m}$
μ_0, μ_r	Vacuum and relative permeability	–

SVPWM and drive variables

ϕ	Load power-factor angle	rad
α	Electrical angle	rad
$\hat{V}_u$	Reference phase voltage amplitude	V

Subscripts / Indices

$(\cdot)_{\mathrm{DUT}}$	Refers to the DC-link/busbar device under test
$(\cdot)_{\mathrm{pk}}$	Peak value
$(\cdot)_{\mathrm{rms}}$	RMS value
$(\cdot)_{\mathrm{on}}/(\cdot)_{\mathrm{off}}$	Turn-on / turn-off quantity

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1
Introduction

1.1 Background

Inverter and motor drive systems are essential components of electric vehicles (EVs), enabling efficient energy conversion and precise control of electric machines. The rapid shift toward electrified transportation has driven advancements in power electronics, with a strong emphasis on improving efficiency, reliability, and power density [1].

Recent advancements in wide bandgap (WBG) semiconductor technologies, particularly silicon carbide (SiC) and gallium nitride (GaN), have delivered significant performance gains over traditional silicon devices. These materials provide higher breakdown voltages, lower switching losses, and superior thermal conductivity, enabling more compact designs and higher operating temperatures. SiC-based modules, incorporate advanced cooling structures and low-inductance layouts, reducing thermal resistance and enhancing overall efficiency [2],[3].

Table 1.1: Parameter Comparison of Si, SiC and GaN [16]

Parameter	GaN	SiC	Si
Electron mobility (cm^2/V*s)	1800	900	1400
Energy gap (eV)	3.5	3.26	1.12
Breakdown electric field (MV/cm)	3.3	3	0.3
Thermal conductivity (W/cm*K)	1.3	4.9	1.5
Saturation drift velocity (Mcm/s)	27	27	10

At the same time, multi-phase inverter topologies, such as six-phase and nine-phase systems, are emerging as alternatives to conventional three-phase configurations. By distributing power across additional phases, these systems improve fault tolerance, reduce harmonic distortion, and enable smoother torque generation [4]-[6]. The redundancy is achieved by allowing continued operation in the event of a phase failure, an advantage for safety-critical applications like heavy-duty EVs and autonomous vehicles. Multi-three-phase systems further optimize machine winding layouts, increasing power density. For inverters, the main benefit lies in the reduced size of the capacitor bank, though this comes at the cost of additional gate driver circuits. To fully leverage these benefits, Space Vector Pulse Width Modulation (SVPWM) with PWM carrier wave shifting is employed to optimize switching behavior, minimize losses, and improve voltage utilization.

This thesis is conducted within the framework of ongoing research at Chalmers University of Technology, including contributions to the Powerdrive project, which aims to develop next-generation, compact, and cost-effective power electronics solutions for electric vehicles.

1.2 Aim

This thesis aims to design, implement, and evaluate a control board and DC-link for a double–three–phase traction inverter based on SiC power modules for electric vehicle applications. The primary focus is on assessing the electro–thermal performance of the DC-link through co-design and experimental validation under controlled electrical and thermal conditions. Particular emphasis is placed on the influence of mechanical layout and cooling strategies on hot-spot temperatures and thermal gradients, given their critical impact on system lifetime and reliability.

1.3 Scope

This thesis encompasses modeling, hardware design, and laboratory validation of a six-phase inverter prototype. The scope includes:

- Electrical modeling of a two-level VSI, DC-link capacitor stress, and sizing.
- Hardware development of a SiC-based inverter with a laminated DC bus and integrated control board.
- Evaluation of two DC-link layouts: Case I: Capacitors mounted above the busbar. Case II: Capacitors mounted in direct contact with the housing.
- Experimental validation through open-loop SVPWM tests on an RL load
- Thermal performance assessment under RMS ripple currents of 156 A_{rms} and 300 A_{rms}, with and without liquid cooling for both layouts.
- Lifetime evaluation of the DC-Link design using a simulation model incorporating HHDDT drive profile

1.4 Methods

The methodology combines analytical modeling, simulation, and experimental testing:

- Modeling: MATLAB/Simulink and PLECS were used to model the inverter, capacitor RMS stress, and lifetime estimation.
- Hardware Design: Development of a laminated DC bus, two alternative DC-link layouts, and a six-layer control board integrating a TMS320F28379D DSP, resolver interface, gate drivers, and EMI filtering.
- Experimental Validation:
  - Open-loop SVPWM tests on an RL load at multiple DC-link voltages to verify modulation and waveform quality.
  - Thermal evaluation using a 10 kHz resonant current source at 156 A_{rms} and 300 A_{rms} for two hours per operating point, under both cooling conditions.
  - Temperature mapping via infrared thermography and thermocouples to assess hot-spot rise, thermal gradients, and cooling effectiveness.

2

Inverters in vehicles

This chapter establishes the electrical and thermal foundations for the traction inverter investigated in this thesis. It focuses on the two-level voltage source inverter (2L-VSI), the prevailing architecture in EV applications due to its simplicity, efficiency, and mature control strategies, and examines how component selection and parasitic elements influence switching behaviour, loss mechanisms, and thermal performance. The discussion is structured as follows:

1. Review of semiconductor devices for traction applications (Si IGBT vs. SiC/GaN MOSFET), with emphasis on conduction and switching losses as well as temperature dependence;
2. Survey of DC-link capacitor technologies (electrolytic, ceramic, and metallised film), including impedance and loss modelling, and quantification of RMS current stress and voltage ripple—highlighting reductions achievable in multi-three-phase systems;
3. Integration of capacitor loss models into thermal networks and reliability frameworks, addressing lifetime prediction, safe operating area (SOA), and bank-level thermal coupling;
4. Discussion of busbar dimensioning, focusing on the interplay among loop inductance, distributed capacitance, insulation and partial discharge constraints, and heat-spreading considerations in WBG-based layouts.

2.1 Electrical and Thermal Modeling

Among the various inverter topologies, the two-level voltage source inverter (2L-VSI) is the most widely adopted in electric vehicle (EV) applications due to its simplicity, cost-effectiveness, and well-established control strategies. An illustration of a typical 2L-VSI with inductance and resistance (RL) load configuration is presented in Figure 2.1. The fundamental function of a VSI is to convert a direct current (DC) input into an alternating current (AC) output suitable for driving a three-phase load, which in EV applications is typically an electric machine (e.g., induction motor or permanent magnet synchronous motor). The DC input is generally supplied either by a battery pack in battery electric vehicles (BEVs) or by a rectifier stage in hybrid configurations.

To ensure stable operation, a DC-link capacitor is placed between the input source and the inverter stage for voltage stabilization, energy buffering, and reactive power support functions. The midpoint of the DC-link capacitor is often considered a virtual neutral point, which can be useful for certain control and fault detection strategies.

On the output side, the inverter typically feeds a balanced three-phase inductive load, representing the stator windings of the electric machine. The inductive nature of the load influences current ripple, switching losses, and thermal behavior, making accurate modeling essential for performance prediction and thermal management.

Accurate electrical and thermal modeling of the losses is critical for predicting inverter performance, ensuring reliability, and designing effective cooling systems. Thermal modeling, in particular, is essential because excessive junction temperatures can degrade semiconductor lifetime and lead to failure.

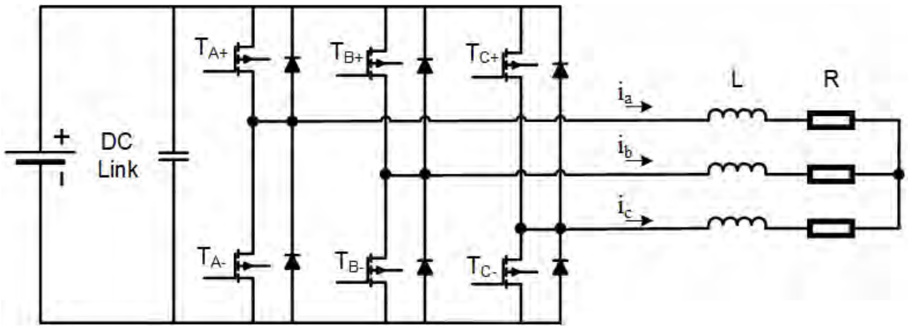

Figure 2.1: Three-phase two-level voltage source inverter (2L-VSI) topology.

2.1.1 Semiconductors

Semiconductor switches are the key active components in an inverter, playing an important role in determining its performance and power density. In traction drive applications, two dominant semiconductor technologies are widely used: silicon insulated-gate bipolar transistors (Si IGBTs) and silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs). The choice of semiconductor device, along with effective thermal management and operational optimization, is crucial for achieving high power density and overall system efficiency. Advancements in semiconductor manufacturing have pushed silicon-based switching technologies close to their physical limits. Figure 2.2 illustrates the evolution of Hitachi's IGBT device structure [1], highlighting how successive generations have reduced conduction losses by lowering the forward on-state voltage (V_{CE}). The first generation employed non-punch-through (NPT) designs, followed by punch-through (PT) devices in the second generation—where the depletion region extends through the drift region—and field-stop structures in the third generation, which introduced an additional layer to control the electric field and further reduce losses.
To address the inherent limitations of silicon-based devices, wide bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have emerged as promising alternatives. These materials exhibit superior properties, including reduced conduction losses under partial load, lower switching losses, higher thermal conductivity, and improved overall efficiency due to their wider energy bandgap [2]. Figure 2.3 and 2.4 illustrate a comparison of the material properties of Si, SiC, and GaN, emphasizing their respective advantages and suitability for applications [3], [6]. While silicon remains the most cost-effective option, GaN offers the lowest on-resistance, whereas SiC excels in thermal conductivity and maximum junction temperature—reaching up to 175 °C compared to 150 °C for both Si and GaN. It is important to note that thermal performance is also influenced by device packaging, not solely by the semiconductor material.
SiC MOSFETs, in particular, deliver superior thermal performance and significantly lower switching losses compared to conventional silicon IGBTs, making them highly suitable for three-phase converter applications. Comparative studies between SiC MOSFET- and Si IGBT-based converters demonstrate that SiC technology enables more compact inverter

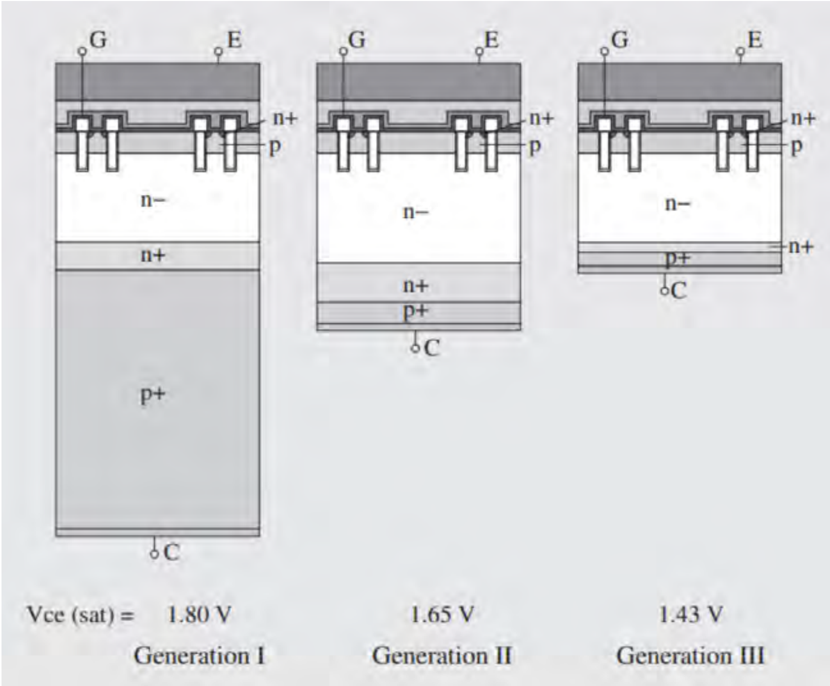

Figure 2.2: Evolution of IGBT device structures [1].

designs while enhancing overall system efficiency [7]. These advantages become especially pronounced at high switching frequencies and elevated junction temperatures, where SiC MOSFETs contribute to improved converter performance. Furthermore, MOSFET-based converters exhibit reduced conduction losses under partial load conditions [10].
Despite GaN's advantages in switching speed, efficiency, and frequency, it faces several challenges in practical applications. These include high electromagnetic interference (EMI), gate ringing, and oscillations caused by parasitics in the power circuit, and packaging. Additionally, GaN technology is still maturing, with limitations in voltage handling and complex control requirements due to its ultra-fast switching behavior.

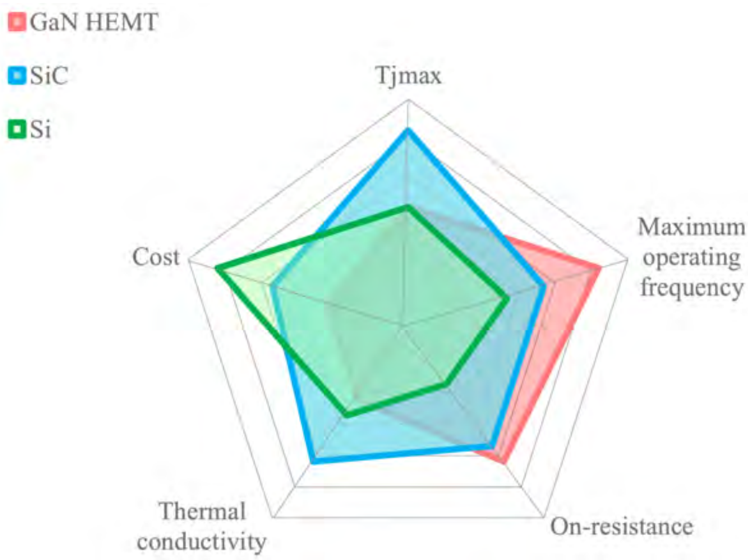

Figure 2.3: Material properties of GaN HEMT, SiC and Si. [16].

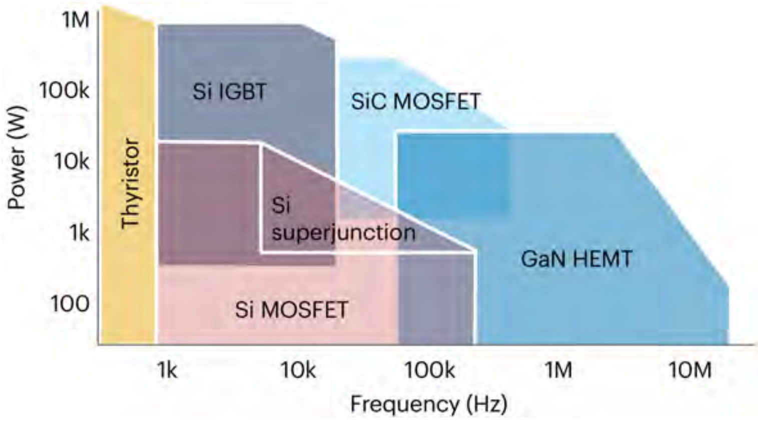

Figure 2.4: High voltage power device mapping [3].

Loss Modelling of Inverters

Primarily semiconductor switches such as IGBTs or MOSFETs incur power losses during switching operations, which manifest as heat. If the thermal dissipation is inadequate and the junction temperature exceeds the permissible limit, device failure may occur. Consequently, accurate modeling of power losses and thermal behavior is critical in the design and reliability assessment of power electronic systems. The availability of analytical models that enable rapid and precise loss estimation is therefore essential for efficient design optimization.
Losses in conventional IGBT/MOSFET-based inverter topologies can be broadly categorized into conduction (on-state) losses and switching losses. Additional losses, such as gate drive losses and off-state leakage currents, are typically negligible in high-power applications and may be excluded from thermal analysis [40].
During the off-state, semiconductor devices exhibit minor leakage currents, resulting in negligible power dissipation. In contrast, during the on-state, a voltage drop across the device leads to conduction losses, which can be significant even under partial load conditions. Switching losses occur during both turn-on and turn-off transitions and are particularly pronounced in IGBTs, often constituting the thermally limiting factor. Auxiliary losses, such as those associated with gate drivers, are generally insignificant from a thermal management perspective [40].
Accordingly, the total power loss of a single switching device can be expressed as:

$$P_{\text{loss}} = P_{\text{con}} + P_{\text{sw}} \tag{2.1}$$

where P_{loss} denotes the total power loss, P_{con} represents conduction losses, and P_{sw} corresponds to switching losses.

Conduction Losses in IGBTs

In an IGBT-based inverter bridge, conduction losses arise from both the IGBT and its anti-parallel diode. This modellng is presented in[40]. The losses can be expressed as:

$$P_{\text{con}} = P_{\text{con,T}} + P_{\text{con,D}} \tag{2.2}$$

where $P_{\text{con,T}}$ and $P_{\text{con,D}}$ denote the conduction losses of the IGBT and diode, respectively.

For a two-level pulse-width modulated (PWM) inverter delivering a sinusoidal output current, the conduction losses are influenced by the modulation index M, defined as:

$$M = \frac{\hat{V}_{\text{out}}}{V_{\text{dc}}/2} \tag{2.3}$$

where $\hat{V}_{\text{out}}$ is the amplitude of the fundamental component of the output phase voltage, and V_{dc} is the DC link voltage. When supplying inductive loads such as electric motors, the power factor is typically less than unity, i.e., $\cos(\varphi) < 1$.
The collector-emitter voltage across an IGBT can be modeled analogously to a diode, as:

$$V_{\text{CE}} = V_0 + R_{\text{on}} i_T \tag{2.4}$$

where V_0 is the threshold voltage and $R_{\text{on}} i_T$ represents the resistive voltage drop dependent on the on-state resistance and current magnitude.
Based on this model, the conduction loss of the IGBT can be formulated as [40]:

$$P_{\text{con,T}} = \left(\frac{1}{2\pi} + \frac{M\cos(\varphi)}{8}\right) V_{0,T} \hat{I}_1 + \left(\frac{1}{8} + \frac{M\cos(\varphi)}{3\pi}\right) R_{\text{on,T}} \hat{I}_1^2 \tag{2.5}$$

Similarly, the conduction loss associated with the anti-parallel diode is given by [40]:

$$P_{\text{con,D}} = \left(\frac{1}{2\pi} - \frac{M\cos(\varphi)}{8}\right) V_{0,D} \hat{I}_1 + \left(\frac{1}{8} - \frac{M\cos(\varphi)}{3\pi}\right) R_{\text{on,D}} \hat{I}_1^2 \tag{2.6}$$

where $V_{0,D}$ is the diode's threshold voltage and $R_{\text{on,D}}$ is its on-state resistance. In summary, the conduction losses in IGBT-based inverters are composed of both static voltage drops, dynamic resistive components, level of current $\hat{I}$, and power factor φ, as represented by the respective terms in equations (2.5) and (2.6).

Switching Losses in IGBTs

In the analysis of total power losses in a three-phase inverter system, switching losses constitute a significant component and must be carefully evaluated. These losses arise during the turn-on and turn-off transitions of the semiconductor devices. Manufacturers typically provide switching energy data in device datasheets, expressed as functions of current, voltage, and temperature. This data enables the estimation of switching losses using a look-up table approach that accounts for each individual switching event.
The switching losses for a single semiconductor device over one fundamental period T_1 can be expressed as:

$$P_{\text{sw}} = \frac{\sum_{j=1}^{n=T_1 f_{\text{sw}}} \left(E_{\text{on},j} i_T(t) + E_{\text{off},j} i_T(t) + E_{\text{rr},j}\right)}{T_1} \tag{2.7}$$

where f_{sw} is the switching frequency, $E_{\text{on},j}$ and $E_{\text{off},j}$ are the turn-on and turn-off energy losses for the j-th switching event, and $E_{\text{rr},j}$ represents the reverse recovery energy loss of the anti-parallel diode.
Since datasheet values for switching energies are typically provided at a reference DC link voltage, scaling is required to adapt these values to the actual operating voltage. The voltage scaling of switching energies can be approximated by:

$$E_{\text{on/off}}(i_T) = E_{\text{on/off,ref}}(i_T) \left(\frac{V_{\text{DS}}}{V_{\text{DC,ref}}}\right)^{K_{\text{v,on/off}}} \tag{2.8}$$

where V_{DS} is the actual drain-source voltage, $V_{\mathrm{DC,ref}}$ is the reference voltage from the datasheet, and $K_{\mathrm{v,on/off}}$ is the voltage scaling exponent, typically around 1.4 [12]. This exponent can be determined through interpolation of datasheet data.
In three-phase inverter applications, the output current is generally sinusoidal. For simplification, the AC current can be approximated by an equivalent DC current:

$$I_{\mathrm{DC}} = \frac{\hat{I}}{\pi} = i_T \tag{2.9}$$

where $\hat{I}$ is the peak value of the sinusoidal current.
Using this approximation, the total switching losses for one IGBT and its corresponding anti-parallel diode can be estimated as:

$$P_{\mathrm{sw}} = f_{\mathrm{sw}}\left(E_{\mathrm{on}}(I_{\mathrm{DC}}) + E_{\mathrm{off}}(I_{\mathrm{DC}}) + E_{\mathrm{rr}}\right) \tag{2.10}$$

This formulation provides a practical and efficient method for estimating switching losses in high-power inverter systems. However, the mentioned method does not include thermal effect in the system.

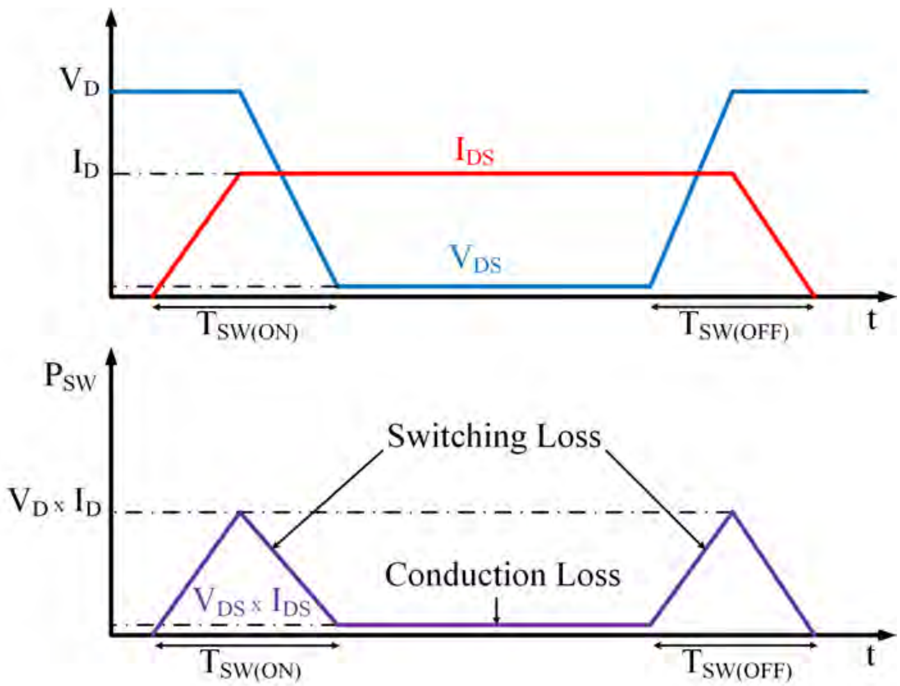

Figure 2.5: Typical switching and conduction losses.

Losses in MOSFET-Based Inverters

Research papers [19]-[23] have focused on developing analytical models for switching losses in MOSFETs. However, many of the comparative analyses found in the literature [7]-[31] and in semiconductor manufacturers' application notes [39], [40] primarily rely on conduction loss models [32]-[35]. These models often overlook the impact of reverse conduction in MOSFETs, commonly referred to as the third-quadrant operation [36]-[38]. Unlike IGBTs, MOSFETs inherently include a body diode that facilitates reverse conduction. Moreover, when a negative drain-source voltage is applied, the MOSFET channel can

also conduct if the gate-source voltage exceeds the threshold level [10]. In a three-phase inverter, this results in simultaneous conduction through both the body diode and the MOSFET channel when the output voltage and current are of opposite polarity.
The conventional control strategy for a two-level, three-phase inverter involves applying a pulse-width modulation (PWM) signal to the upper switch of each inverter leg and the complementary (inverted) PWM signal to the lower switch, with a short dead time inserted to prevent shoot-through faults [[11]. As a result, reverse conduction is inherently utilized in most MOSFET-based inverter designs. Neglecting this reverse conduction mechanism can lead to an overestimation of conduction losses, thereby compromising the accuracy of thermal and efficiency assessments.

Conduction Losses in MOSFETs

Assuming that the three-phase output currents are sinusoidal and balanced, it is sufficient to analyze the conduction losses in a single inverter leg. The results were generalized in [32]. The average conduction losses in the MOSFET can be estimated by approximating the drain-source characteristic with a linear on-state resistance, R_{on}, as follows:

$$P_{c,T} = \frac{1}{2\pi} \int_0^{2\pi} D(\alpha) R_{\text{on}} i_T^2(\alpha)\, d\alpha \tag{2.11}$$

where $\alpha = \frac{2\pi}{T}$ is the conduction angle, $D(\alpha)$ is the duty cycle, and $i_T(\alpha)$ is the instantaneous current through the MOSFET. Similarly, the conduction losses in the body diode can be modeled by approximating its forward characteristic as a combination of a constant voltage drop V_d and an on-state resistance R_d:

$$P_{c,D} = \frac{1}{2\pi} \int_0^{2\pi} D(\alpha) \left(R_d i_D^2(\alpha) + V_d i_D(\alpha) \right) d\alpha \tag{2.12}$$

Assuming a naturally sampled sine-triangle PWM scheme with third harmonic injection, the duty cycle can be expressed as a function of α [32]

$$D(\alpha) = \frac{1}{2} \left(1 + M \sin(\alpha) + \frac{1}{6} M \sin(3\alpha) \right) \tag{2.13}$$

where M is the modulation index. In a three-phase inverter, when the output voltage and current are of opposite signs, either the upper or lower diode becomes forward-biased. If the gate-source voltage of the corresponding MOSFET exceeds the threshold voltage, the MOSFET channel also conducts in parallel with the diode. The diode conducts only if the voltage drop across the MOSFET exceeds the diode's threshold voltage:

$$|i_T R_{\text{on}}| > V_d \tag{2.14}$$

This leads to three distinct conduction scenarios:
Case I – First Quadrant Operation ($i_{DS} \geq 0$): When the voltage and current are of the same polarity:

$$i_T = i_{DS} \tag{2.15}$$

$$i_D = 0 \tag{2.16}$$

$$v_{DS} = i_T R_{\text{on}} \tag{2.17}$$

Case II – Third Quadrant Operation without Current Sharing ($-\frac{V_d}{R_{\text{on}}} \leq i_{DS} < 0$): When the voltage and current are of opposite signs, but the current magnitude is insufficient to forward-bias the diode:

$$i_T = i_{DS} \tag{2.18}$$
$$i_D = 0 \tag{2.19}$$
$$v_{DS} = i_T R_{\text{on}} \tag{2.20}$$

Case III – Third Quadrant Operation with Current Sharing ($i_{DS} < -\frac{V_d}{R_{\text{on}}}$): When the current magnitude is large enough to forward-bias the diode, resulting in parallel conduction:

$$i_T = \frac{R_{\text{on}} i_{DS} - V_d}{R_d + R_{\text{on}}} \tag{2.21}$$
$$i_D = -\frac{R_{\text{on}} i_{DS} + V_d}{R_d + R_{\text{on}}} \tag{2.22}$$
$$i_{DS} = i_T - i_D \tag{2.23}$$

Based on these cases, the instantaneous conduction loss can be expressed as:

$$p_c = v_{DS} i_{DS} \tag{2.24}$$

Since the boundaries between these cases depend solely on device parameters and current magnitude, the average conduction loss over a sinusoidal cycle can be computed by partitioning the integral accordingly and applying the appropriate loss expression for each region.

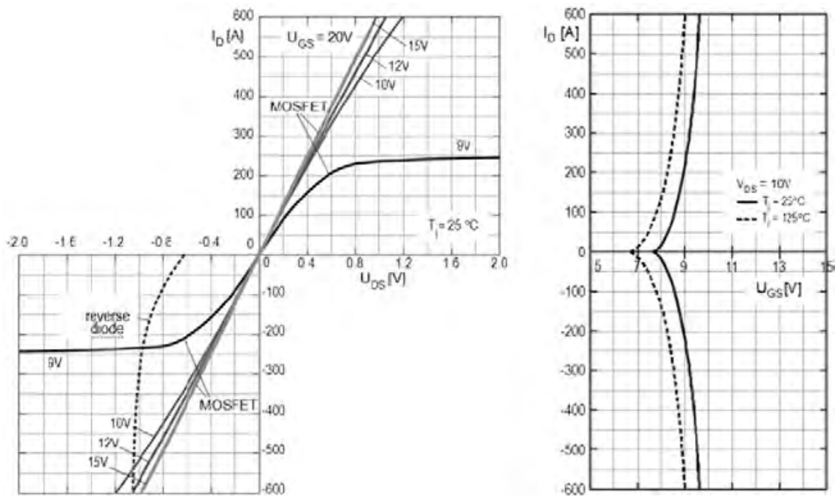

Figure 2.6: Fist and third quadrants of output static characteristics of MOSFET [9].

Effect of Blanking Time in MOSFET Inverters

Due to the finite switching times inherent to all semiconductor devices, a short delay, commonly referred to as the blanking time (t_{b1}), must be introduced between the conduction periods of the upper and lower switches within the same inverter leg. This precaution prevents shoot-through faults, where both switches conduct simultaneously. During this blanking interval, current is exclusively conducted through the body diode.

In IGBT-based inverters, reverse current always flows through the anti-parallel diode. In contrast, MOSFETs are capable of conducting in the reverse direction via their channel, making the blanking time particularly relevant for MOSFET-based designs. To account for its impact on conduction loss calculations, an equivalent duty cycle can be defined as:

$$D_{\text{eq}}(\alpha) = D(\alpha) - t_{b1} f_{\text{sw}} = \frac{1}{2}\left(1 - 2t_{b1} f_{\text{sw}} + M \sin(\alpha)\right) \tag{2.25}$$

where f_{sw} is the switching frequency and M is the modulation index.
To ensure physical validity, the equivalent duty cycle must remain non-negative:

$$1 - 2t_{b1} f_{\text{sw}} + M \sin(\alpha) > 0 \tag{2.26}$$

When third harmonic injection is employed, the condition becomes:

$$1 - 2t_{b1} f_{\text{sw}} + M \sin(\alpha) + \frac{1}{6} M \sin(3\alpha) > 0 \tag{2.27}$$

For modulation indices approaching the over-modulation boundary, careful consideration is required when applying the equivalent duty cycle method. Typically, a third harmonic component equal to one-sixth of the fundamental is added to extend the linear modulation range.
Since the diode conducts the full current during the blanking interval, its average conduction losses must be augmented by:

$$\frac{1}{2\pi} \int_{\pi}^{2\pi} 2t_{b1} f_{\text{sw}} \left(R_d \hat{I}^2 \sin^2(\vartheta) - \hat{I} \sin(\vartheta) V_d \right) d\vartheta \tag{2.28}$$

which simplifies to:

$$t_{b1} f_{\text{sw}} \hat{I} \left(\frac{1}{2} \hat{I} R_d + \frac{2}{\pi} V_d \right) \tag{2.29}$$

While the conduction loss models for the MOSFET and diode are derived without approximation, the inclusion of blanking time introduces a minor estimation error. The equivalent duty cycle approach effectively reduces the conduction interval by twice the blanking time, assuming this reduction is uniformly distributed across the electrical period.

Switching Losses in MOSFETs

Switching losses in MOSFETs are generally similar to those observed in IGBT devices. However, in MOSFETs, reverse conduction during switching events could theoretically increase switching losses. In practice, this effect is mitigated by the presence of the body diode, which conducts during the blanking time or in parallel with the MOSFET channel. During the initial phase of the switching transient, the voltage across the MOSFET is clamped to approximately

$$V_d + R_d \hat{I} \tag{2.30}$$

This creates a quasi zero-voltage switching (ZVS) condition, which significantly reduces energy dissipation during the transition. Consequently, switching losses due to reverse conduction in MOSFETs are typically minimal and can be neglected in loss modeling.

Temperature dependence of MOSFET loss parameters

The loss characteristics of MOSFETs are significantly influenced by temperature variations. The analytical expressions derived in previous sections can be refined by incorporating temperature-dependent parameters. Among the most critical parameters affected by temperature are the on-state resistance R_{on}, the switching energies E_{on}, E_{off}, and E_{rec}, as well as the diode threshold voltage V_{ct}. These dependencies are typically provided in the device datasheets, often in the form of characteristic curves.
To achieve accurate loss estimation under varying thermal conditions, these variations can be implemented in simulation models using lookup tables or interpolation methods. Figure 2.7 illustrates the typical variation of drain–source on-resistance with temperature, as specified by the manufacturer.

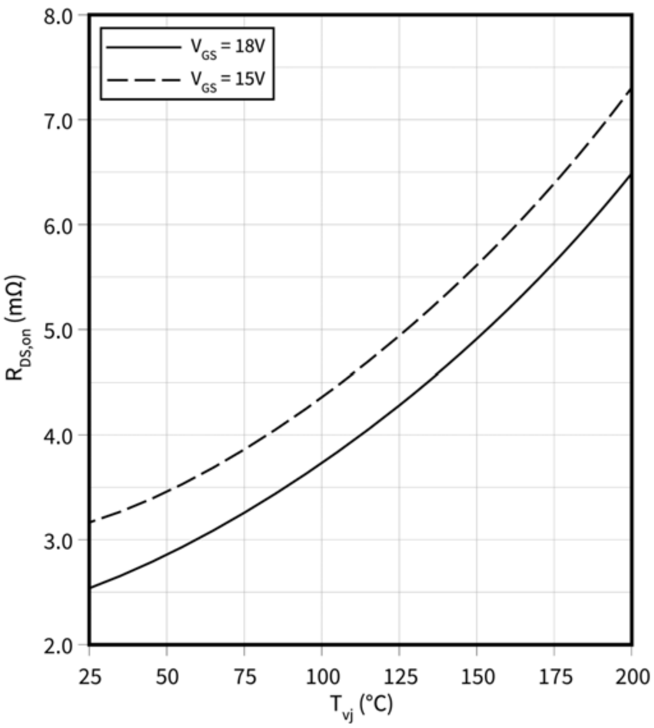

Figure 2.7: Drain–source on-resistance versus temperature for the selected MOSFET.

To develop a thermally dependent model, it is essential to consider the thermal network of the power semiconductor within the complete system, including the heatsink and thermal interface materials. This process generally requires an iterative engineering approach, where loss estimation and cooling system performance are evaluated together to achieve an optimal design.
In most inverter applications, thermal capacitances are neglected because the thermal time constants of power electronic devices are typically less than or equal to 1 s. As a result, the system reaches a steady-state thermal operating point relatively quickly from the inverter's perspective. The primary thermal boundary conditions for the system are the coolant temperature and the maximum allowable junction temperature of the MOSFET, denoted as $T_{J,\text{max}}$.
Figure 2.8 illustrates a simplified thermal network for a direct-cooled module SiC MOSFET-based inverter. In this representation, the MOSFET acts as a heat source, and its temperature rise is determined by the thermal resistances in the path from the junction

to the coolant. These include the junction-to-case thermal resistance R_{jc} and the heatsink thermal resistance R_{hs}, which are shown schematically between the chip and the coolant.

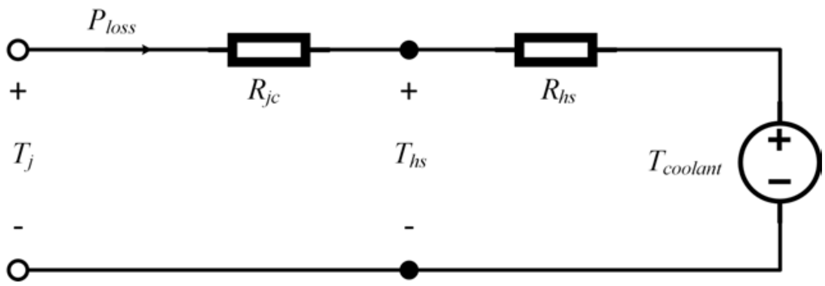

Figure 2.8: Simplified thermal network from junction to coolant for a SiC MOSFET-based inverter.

Cooling PCB mounted low-power components

For low-power semiconductor devices, such as discrete components in TO or SMD packages, heat dissipation is typically managed through the component casing, electrical terminals, and the printed circuit board (PCB) traces (see Figure 2.9). The thermal resistance from junction to ambient, denoted as $R_{\mathrm{th}(j-a)}$, is commonly specified for through-hole components assuming standard lead lengths and PCB trace widths of approximately 2–3 mm.
Certain low-power components, such as those in TO-220 packages, feature metal mounting surfaces that may be electrically connected to a terminal or internally isolated. For these components, the datasheet typically provides the junction-to-case thermal resistance, $R_{\mathrm{th}(j-c)}$, which is critical for evaluating thermal performance in mounted configurations.

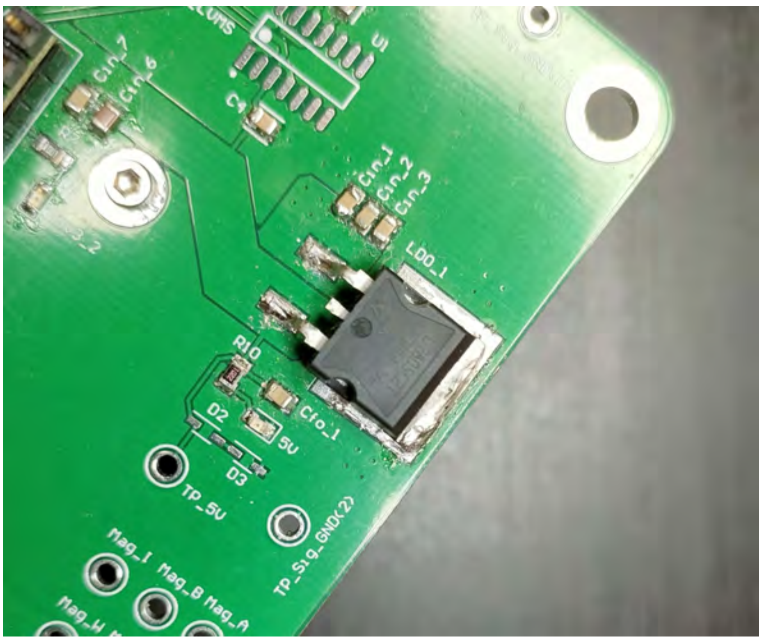

Figure 2.9: Heat dissipation through PCB-mounted components.

Cooling Plates

Semiconductor devices with moderately higher power ratings, typically up to 15 A mean forward current can be mounted onto cooling plates to effectively dissipate heat losses. If the component case is electrically connected to one of the terminals, the cooling plate must be electrically insulated. However, if the case (which may be a plastic enclosure with a metal base or mounting plate) is electrically isolated from the internal circuitry, the cooling plate can be integrated into the equipment housing or assembly chassis (see Figure 2.10).
Cooling plates are generally constructed from polished metal and shaped approximately square, with an edge length ratio not exceeding 2:3. The component is mounted centrally on the plate, and its contact area is considered small relative to the total cooling surface. For optimal thermal performance, the plate should be mounted vertically to allow natural convection airflow along its surface. Horizontal mounting can obstruct airflow and increase thermal resistance. Applying a black coating to the plate can enhance radiative heat transfer, reducing thermal resistance R_{th} by up to 15% [40].

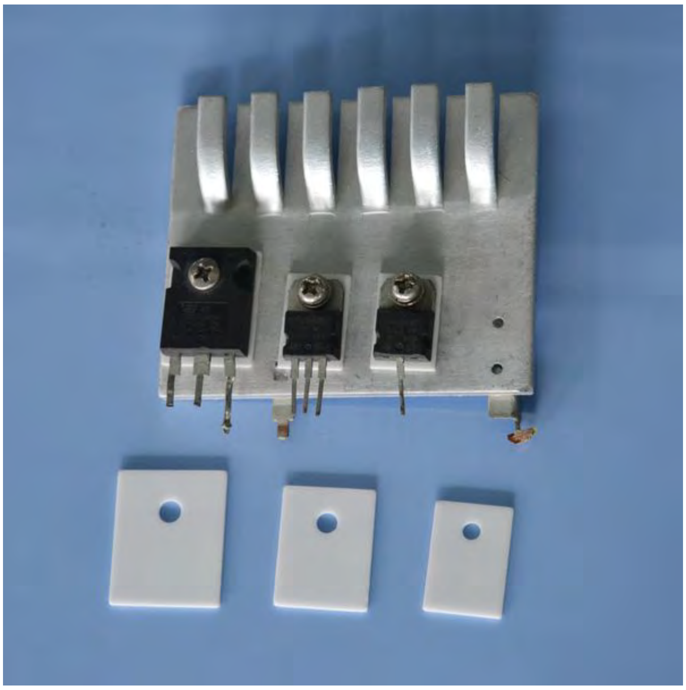

Figure 2.10: Example of a cooling plate for semiconductor devices.

Heatsinks

For high-power semiconductor components, typically those exceeding 15 A mean forward current, cooling plates alone are insufficient to fully utilize their current-carrying capacity. In such cases, heatsinks or cooling profiles made primarily of aluminum (and occasionally copper) with ribbed surfaces are employed. These profiles often feature thick mounting bases to enhance heat spreading and multiple fins oriented in various directions to increase surface area for both convection and radiation.
The thermal resistance of a heatsink is not a fixed value. Under natural convection, it depends on the temperature differential between the heatsink and ambient air, which in turn is influenced by the amount of power being dissipated. As power dissipation

increases, the heatsink temperature rises, effectively enlarging the heat exchange area. When multiple heatsinks are stacked vertically in space-constrained environments, care must be taken to ensure that upper units do not receive preheated air from lower ones, which would reduce cooling efficiency.
To estimate the thermal resistance of a heatsink profile with multiple components, the profile can be conceptually divided into segments, and the thermal resistance calculated for each section. Uniform distribution of components along the profile improves heat spreading and reduces the overall thermal resistance $R_{\text{th}(s-a)}$ compared to concentrating all power dissipation at a single point. Figure 2.11 illustrates $R_{\text{th}(s-a)}$ of a heat sink profile at different lengths for a centrally mounted heat source. Longer heat sink profiles can accommodate multiple semiconductor components. For non-isolated components, the configuration depends on the chosen circuit; only components sharing the same electrical potential can be mounted on a common heat sink, such as the cathodes connected to the positive DC rail in a bridge rectifier.
Datasheets for certain heatsink profiles include diagrams showing $R_{\text{th}(s-a)}$ as a function of profile length and power dissipation for n components mounted on the same profile. For disc-type semiconductor cells, double-sided cooling can be achieved by placing the cell between two heatsink profiles, effectively halving the junction-to-ambient thermal resistance $R_{\text{th}(j-a)}$. The clamping mechanism must ensure uniform pressure distribution across the entire surface of the disc to maintain effective thermal contact, which may require one of the heatsink fins to be movable.

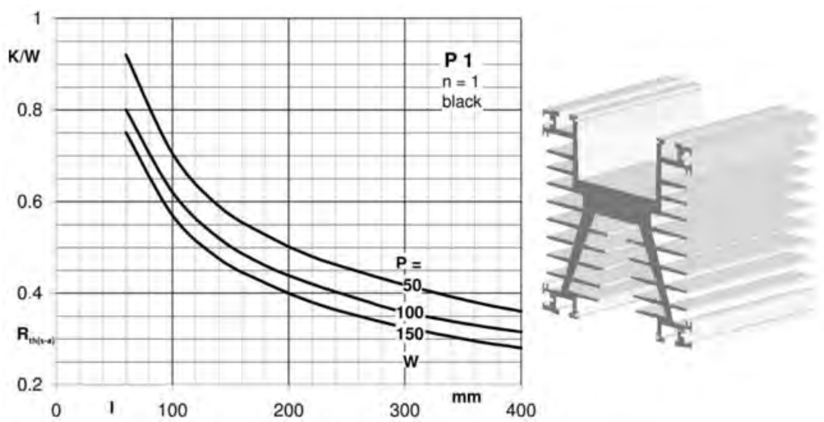

Figure 2.11: Variation of thermal resistance (Rth(s-a)) with P1 heat sink length under natural cooling for different power dissipation levels (50 W, 100 W, 150 W), with a single centrally mounted component [40].

Forced Air Cooling

For higher power dissipation levels, typically above 50 W, forced air cooling is commonly employed. In this method, air is directed through the heatsink profile using a fan or blower as shown in Figure 2.12. Depending on the airflow volume, the thermal resistance between the heatsink and the surrounding air, denoted as $R_{\text{th(s-a)}}$, can be reduced by a factor ranging from one-third to one-fifteenth [40]. Under forced convection, $R_{\text{th(s-a)}}$ becomes virtually independent of both the power dissipation and the temperature difference between the heatsink and the ambient air. Surface treatments such as coating or blackening the heatsink do not provide additional benefits in this case, since convection dominates the

heat transfer process.
The material used for heatsink profiles must combine high thermal conductivity with cost-effectiveness. Aluminum is widely used because it offers a favorable balance between thermal performance and manufacturing cost. While pure aluminum has a thermal conductivity of approximately 398 W/(m · K), practical values depend on alloy composition and manufacturing processes. In practice, aluminum heatsinks exhibit thermal conductivities ranging from about 150 W/(m · K) for die-cast alloys to approximately 220 W/(m · K) for AlMgSi extrusions [40].
The efficiency of a heatsink is also determined by its geometric design. Important factors include the thickness of the root section, which serves as the primary heat-spreading area where the power module is mounted; the number and height of fins, which increase the surface area for convective heat transfer; and the fin thickness, which affects both mechanical stability and thermal performance.

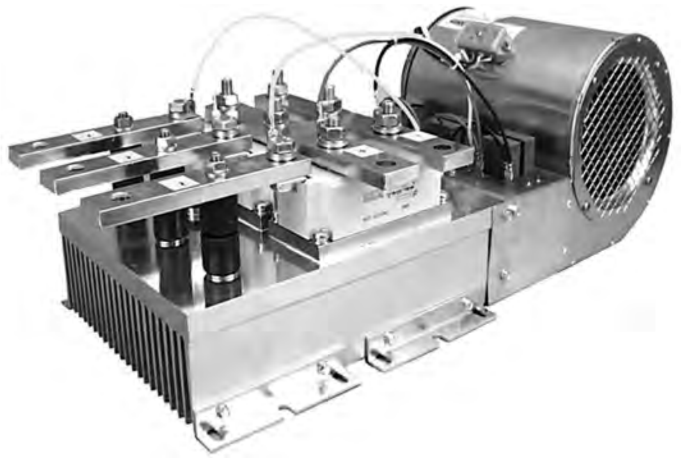

Figure 2.12: A three-phase rectifier circuit on a cooling profile with radial-flow fan [40].

Liquid Cooling

Liquid cooling is commonly applied to high-power inverters in the megawatt range and to medium-power devices where a liquid cooling circuit is already available, such as in automotive systems, galvanic installations, or inductive heating setups. Typically, the coolant inlet temperature ranges from 50–70 °C when heat is dissipated directly into the atmosphere [40]. In industrial systems equipped with active heat exchangers, the coolant temperature can be maintained around 25 °C. The smaller temperature differential between the heatsink surface and the coolant, compared to air cooling, can be leveraged in two ways: either to achieve higher power density, albeit with significant dynamic junction temperature variations (ΔT_j) per load cycle that may affect module lifespan, or to maintain lower junction temperatures, thereby enhancing device reliability.
Several parameters influence the thermal resistance of liquid-cooled systems. These include the contact area between the heatsink and coolant, which depends on the number of cooling channels; the volumetric flow rate, which is determined by the pressure drop; the heat capacity of the coolant; the degree of turbulence within the coolant flow; the thermal conductivity and heat spreading capability of the heatsink material; and the coolant temperature. Increasing the contact area between the heatsink and coolant improves heat transfer. Traditional coolers are limited by the number of available cooling channels,

whereas pin-fin coolers, which feature numerous small columns protruding into the coolant, significantly enlarge the contact area and promote sufficient turbulence, thereby enhancing thermal performance, as illustrated in Figure 2.13.
Unlike air cooling, liquid cooling benefits from a high heat transfer coefficient, approximately $1000\,\mathrm{W/(m^2 \cdot K)}$, allowing heat to be efficiently transferred to the coolant with minimal lateral conduction. Consequently, only the regions directly beneath the power semiconductor modules contribute to cooling. Using copper instead of aluminum for the heatsink material reduces volume resistance and improves lateral heat conduction, effectively enlarging the active cooling area. A copper-based cooler can reduce $R_{\text{th(j-a)}}$ by approximately 20% for standard IGBT modules [40].
Direct baseplate cooling eliminates the thermal resistance associated with the interface layer, such as thermal paste, by mounting the module directly over an opening in the heatsink. An O-ring is used to seal the interface. This method can reduce $R_{\text{th(j-a)}}$ by up to 25% compared to conventional water channel cooling [40]. The module's baseplate features a structured surface, such as pin fins or meandering channels, that is immersed directly into the cooling liquid within a trough.

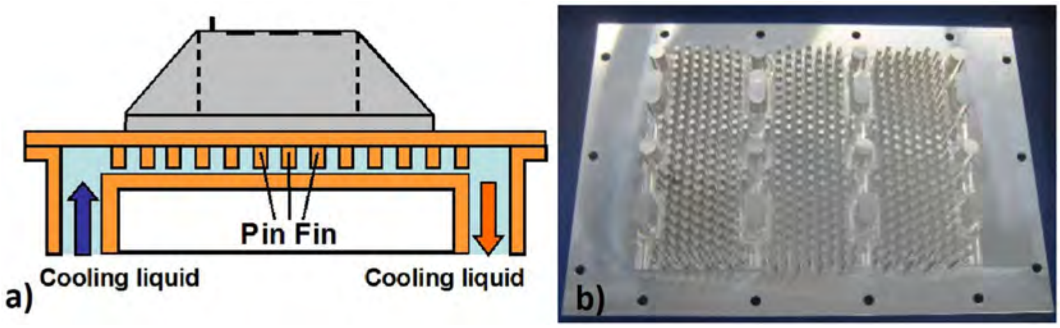

Figure 2.13: Pin-fin liquid cooler: a) schematic drawing; b) photograph of the cooling side [40].

Influence of Coolant Temperature, Flow Rate, and Glycol Concentration on $R_{\text{th(s-a)}}$ The relationship between the thermal resistance from heatsink to ambient, $R_{\text{th(s-a)}}$, and parameters such as coolant flow rate, temperature, and glycol concentration has been studied in [41]. Increasing the coolant flow rate is one of the most straightforward methods to enhance thermal performance. However, the benefit of increasing flow rate diminishes at very high values, as the reduction in thermal resistance becomes less significant.

Glycol Concentration The impact of glycol concentration on $R_{\text{th(s-a)}}$ is primarily due to its influence on fluid properties. Glycol exhibits a higher dynamic viscosity than water, which reduces the Reynolds number, a key indicator of turbulence. Lower turbulence results in a diminished heat transfer coefficient. Furthermore, glycol has lower thermal conductivity and specific heat capacity compared to water, which further impairs heat transfer. The influence of glycol concentration on thermal resistance remains nearly constant across different flow rates and fluid temperatures [40].

Fluid Temperature The effect of fluid temperature on $R_{\text{th(s-a)}}$ is governed by temperature-dependent material properties. For water, thermal conductivity increases with temperature,

whereas for glycol, it decreases. A 40:60 glycol-to-water mixture maintains nearly constant thermal conductivity across the 0–100 °C range. While the specific heat capacity of pure water remains nearly constant, that of glycol-water mixtures increases with temperature but remains lower than that of pure water. Dynamic viscosity also plays a critical role. Water has a lower viscosity than glycol, and viscosity decreases with rising temperature, which enhances the heat transfer coefficient.
Formulas for calculating $R_{\mathrm{th(s\text{-}a)}}$ and $Z_{\mathrm{th(s\text{-}a)}}$ under varying conditions based on a nominal operating point are provided in [41].

Pressure Drop and Test Pressure In closed-loop liquid cooling systems, circulation can be achieved either passively through thermosyphon effects or actively using a pump. In thermosyphon cooling, the heated liquid, being less dense, rises naturally to the heat exchanger, while the cooled liquid descends back to the heat source. However, in most practical applications, a pump is employed to ensure consistent and controllable coolant flow. This allows the system to maintain a desired flow rate, which directly influences thermal resistance and pressure drop. Increasing the coolant flow rate generally reduces the thermal resistance of the system, but this comes at the cost of a higher pressure drop across the cooling unit. The design of the cooling circuit must therefore balance thermal performance with hydraulic efficiency.
To maintain efficient coolant circulation with reasonable pumping power, the cooling system should be designed to minimize flow resistance. This can be achieved by using large-diameter pipes, avoiding sudden reductions in cross-sectional area, eliminating quick-release tube connectors where possible, and reducing the number of directional changes in the piping layout.

Coolant Properties, Cooling Circuit Design, and Chemical Requirements

The most commonly used coolant in liquid cooling systems is a water-glycol mixture, which combines good thermal performance with freeze protection. Less frequently, deionised water or non-conductive fluids such as fluorocarbons and polyalphaolefins (PAOs) are employed. Due to its high specific heat capacity ($c_p = 4.187\,\mathrm{kJ/(kg \cdot K)}$), pure water is generally preferred for heat dissipation compared to glycol or oil. Water can be circulated in a closed-loop system with an air-cooled heat exchanger or used as fresh water that is discharged after passing through the cooling unit. Although fresh water is electrically conductive, this is typically not a concern for internally insulated semiconductor components, as the coolant remains electrically isolated. However, for non-insulated components, conductivity becomes a critical factor.
The selected coolant must be chemically compatible with the cooling circuit materials and provide adequate corrosion protection. For aluminum heatsinks, a minimum glycol concentration of 10% is required to prevent corrosion, although some antifreeze manufacturers recommend even higher concentrations to maintain the effectiveness of corrosion inhibitors, particularly for non-ferrous metals. The hardness of the cooling water should not exceed 6°dH (degrees of German hardness), and for coolant temperatures above 60 °C, a closed-loop system is strongly recommended. Table 2.1 summarizes the compatibility of various heatsink materials with different coolant types.
Adding glycol decreases the heat retention capability of the coolant. For instance, at 50% glycol concentration and 40°C, the specific heat capacity drops to approximately 3–4 kJ/(kg · K). Increased glycol content also raises viscosity and density, which in turn

Table 2.1: Compatibility of Heatsink Materials with Coolants [40].

Material	Water	Glycol Mixtures	Deionised Water	Non-Conductive Liquids
Copper	X	X		X
Aluminum		X		X
Stainless Steel	X	X	X	

increases the thermal resistance from the heat sink to the coolant ($R_{\text{th(s-a)}}$). Compared to pure water, adding 10% glycol increases R_{th} by about 15%, while 50% glycol results in a 50–60% increase. At 90% glycol, R_{th} nearly doubles. These effects also depend on flow conditions and coolant temperature [40].

2.1.2 DC-Link Capacitor

A capacitor is a passive electrical component designed to store electrical energy for a short duration and release it almost instantaneously when needed. It consists of one or more conductive plates (electrodes) separated by an insulating material called the dielectric, as shown in Fig 2.14. When an external voltage is applied across the electrodes, the dielectric becomes polarized, aligning its molecules along the electric field lines. Since the dielectric is an insulator, its charged particles remain immobile, creating an electrostatic effect that attracts opposite charges to the electrode surfaces. This results in the accumulation of charge, forming a small reservoir of electrical energy. When the voltage source is removed, the capacitor discharges its stored energy back into the circuit, helping to maintain current flow briefly.

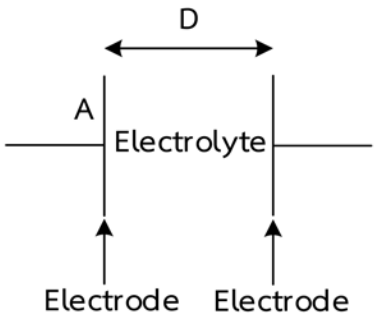

Figure 2.14: Simplified construction of a single layer parallel pate capacitor.

Capacitors play a vital role in power electronic systems, especially in traction inverters, where they act as energy buffers and filters to reduce voltage and current ripple caused by high-frequency switching. The choice of capacitor technology depends on factors such as energy density, equivalent series resistance (ESR), equivalent series inductance (ESL), thermal stability, mechanical strength, and long-term reliability. Based on the dielectric material, capacitors are generally classified into three main types: electrolytic, ceramic, and film capacitors, each offering unique advantages and limitations for specific applications.

The electrical behavior of DC-link capacitors is largely determined by their construction technology. Fundamentally, a capacitor operates as a parallel plate structure with a dielectric material between two conductive plates. The capacitance is given by:

$$C = \frac{\varepsilon A}{d} \tag{2.31}$$

where C is the capacitance, ε is the dielectric permittivity, A is the plate area, and d is the separation between plates. Capacitance increases with larger plate area and higher permittivity, and decreases with greater plate separation. However, the minimum thickness d is constrained by the dielectric strength required to withstand the operating voltage, making capacitance inversely proportional to voltage for a given dielectric material [65].
An ideal capacitor is assumed to exhibit only its capacitance (C). However, in practical applications, additional parasitic elements such as internal resistance and inductance arise due to construction imperfections and environmental factors. Electrically, these non-ideal characteristics can be modeled as a combination of components: C, ESR, and ESL, as illustrated in Fig 2.15. The equivalent circuit of a capacitor, illustrated in Fig. 1

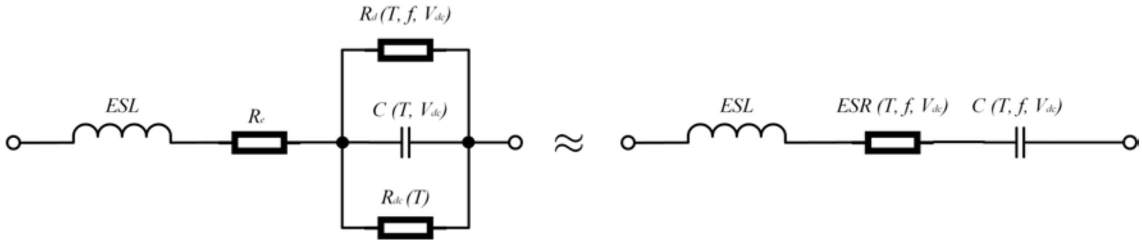

Figure 2.15: Capacitor circuit model of a capacitor (left) and a simplified model (right).

(left), demonstrates that the associated component values are not constant but vary with operating conditions such as temperature, frequency, and applied DC bias voltage. In this representation, the inductance and resistance of the electrodes and terminations are modeled as ESL and R_e, respectively, both of which are considered constant.
The resistance R_d accounts for hysteresis losses within the dielectric and is connected in parallel with the total capacitance C. Additionally, DC losses resulting from dielectric leakage current are represented by R_{dc}, which is also placed in parallel with C.
The simplified equivalent circuit is shown in Fig. 2.15 (right). In this configuration, ESL represents the total inductance contributing to the inverter's commutation-loop inductance, thereby degrading switching performance. The total losses can be consolidated and represented by an ESR. This transformation is expressed by the following equation [45], [46]:

$$\mathrm{ESR} = R_e + \frac{1}{\omega}\left(\frac{\alpha 2\pi}{1 + (\alpha 2\pi C)^2}\right) \tag{2.32}$$

where

$$R_d = \frac{\alpha 2\pi}{\omega} \tag{2.33}$$

In these equations, α denotes the dielectric material constant, and ω represents the operating frequency in radians per second. In the simplified equivalent circuit model, the ESR is connected in series with the ESL and the total capacitance C, accounting for all losses within the capacitor.
The parameters illustrated in Fig. 2.15 are highly dependent on operating temperature (T), DC bias voltage (V_{dc}), and operating frequency (f). Therefore, accurate extraction of these parameters is essential for optimizing the capacitor's volume in motor drive applications.

Each parameter influences the capacitor's behavior differently, which can be analyzed through its impedance characteristics across various frequency ranges:

- **Low-frequency region** ($f < \omega_1$): Impedance is dominated by the capacitance.
- **Mid-frequency region** ($\omega_1 < f < \omega_2$): ESR becomes the primary contributor.
- **High-frequency region** ($f > \omega_2$): ESL dominates the impedance response.

Figure 2.16 depicts the impedance profile of a capacitor. These impedance characteristics depend on the dielectric material and the construction technology used.

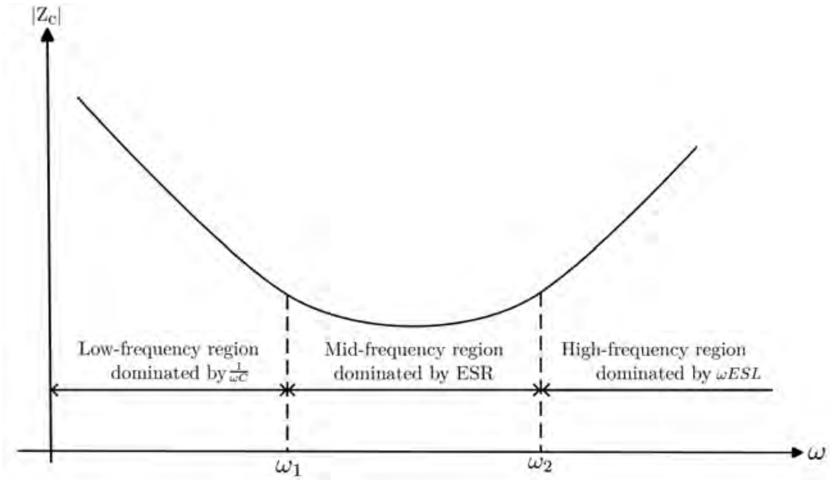

Figure 2.16: Impedance characterstics of a capacitor [43].

Electrolytic Capacitors

Electrolytic capacitors are widely used in power electronic systems because of their high capacitance-to-volume ratio and cost-effectiveness. Their construction typically consists of two metal foils separated by a paper spacer impregnated with an electrolyte, as shown in Fig. 2.17. One of the foils is anodized to form an oxide layer, which serves as the dielectric. The electrolyte-soaked paper acts as a separator while allowing ionic conduction. These layers are rolled into a cylindrical shape, and terminals are connected to each foil.

The anodization process makes electrolytic capacitors inherently polarized, restricting their use in AC applications. The presence of a liquid electrolyte significantly increases the effective surface area, especially when the anode is etched, resulting in higher capacitance and energy density. Aluminum electrolytic capacitors are commonly used in motor drive applications because of their high capacitance-voltage (CV) product and suitability for low-temperature environments. The dielectric is typically aluminum oxide (Al_2O_3), which allows minimal plate separation and high capacitance. However, the liquid electrolyte introduces aging mechanisms such as evaporation, which can degrade performance over time [42].

Only specific metals, known as valve metals (such as aluminum, tantalum, and niobium), can serve as the anode because of their ability to form a stable oxide layer that acts as the dielectric. The electrolyte composition depends on compatibility with the anode material and may be in liquid or solid form. Manganese dioxide is commonly used as a solid electrolyte for all three anodic materials.

Despite their high capacitance, electrolytic capacitors are limited by their root mean square (RMS) current capability. Ideally, a capacitor could handle infinite current; however, parasitic elements such as equivalent series resistance (ESR) introduce power losses in

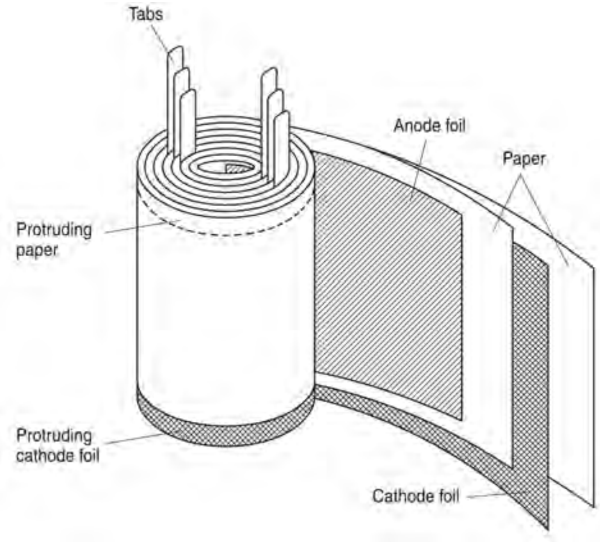

Figure 2.17: Winding construction of an aluminum electrolytic capacitor [47].

the form of heat. This heat accelerates electrolyte evaporation and increases the risk of thermal runaway. ESR is an undesirable property that impacts capacitor performance over time by accelerating chemical degradation of the dielectric. In electrolytic capacitors, ESR is influenced by the electrolyte resistance, internal contact resistance, and construction geometry. While electrolyte resistance depends on material conductivity and cannot be altered, ESR contributions from current collectors, terminals, and leads can be optimized. Typical ESR values range from 0.1 Ω to 2 Ω for standard electrolytic capacitors, while low-ESR variants exhibit values between 0.01 Ω and 0.05 Ω. Due to their cylindrical construction, these capacitors also exhibit significant self-inductance, typically between 10 nH and 1 μH, which lowers their resonant frequency. The relatively high ESR results in substantial energy dissipation as heat. The relationship between ESR, RMS current, and temperature rise is expressed in Eq. 2.34, indicating that temperature rise is directly proportional to ESR and the square of the RMS current. Consequently, even a small increase in RMS current can lead to a significant temperature rise, potentially causing dielectric breakdown, electrolyte vaporization, and catastrophic failure [43].

$$i_{\mathrm{RMS}} = \sqrt{\frac{\Delta T}{\beta \cdot R_{\mathrm{ESR}}}} \tag{2.34}$$

Here, i_{RMS} is the rated RMS current (A), ΔT is the temperature rise due to internal heating (°C), β represents the thermal resistance (°C/W), and R_{ESR} is the ESR value of the capacitor (Ω).

Ceramic Capacitors Ceramic capacitors use sintered ceramic materials such as barium titanate ($BaTiO_3$), titanium dioxide (TiO_2), and calcium zirconate ($CaZrO_3$) as dielectric media. These capacitors are typically constructed in a multilayer configuration (MLCC), where alternating layers of ceramic and metal electrodes are stacked to increase capacitance and achieve high volumetric efficiency, as illustrated in Fig. 2.18. This design supports miniaturization and enables operation at higher voltages.
Ceramic capacitors offer excellent high-frequency performance due to their inherently low ESR and ESL. However, they exhibit certain limitations. The dielectric properties of ceramics are highly sensitive to temperature and applied voltage, resulting in nonlinear

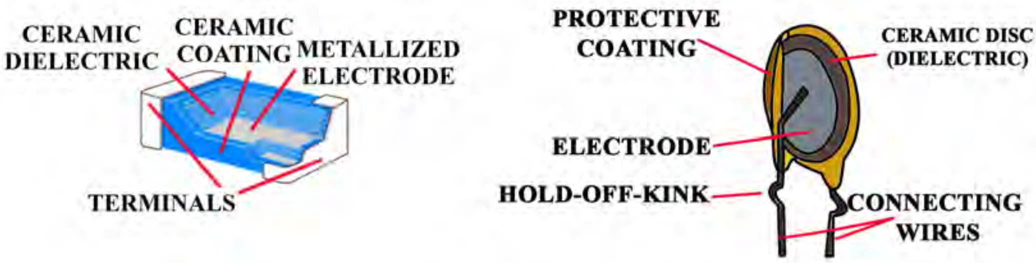

Figure 2.18: Detailed construction of a Multilayer Ceramic Capacitor (left) and a ceramic disc capacitor (right) [48].

capacitance behavior. Pure $BaTiO_3$ displays strong temperature dependence and nonlinearity; therefore, additives such as zinc, zirconium, magnesium, cobalt, and strontium (for TiO_2) or aluminum silicate, aluminum oxide, and magnesium silicate (for $BaTiO_3$) are incorporated to enhance dielectric stability and increase permittivity (ε), thereby improving capacitance.

Despite these improvements, ceramic capacitors typically exhibit large capacitance tolerances and are prone to piezoelectric effects, which can induce mechanical vibrations and audible noise. Furthermore, the brittle nature of ceramic materials makes them susceptible to cracking under mechanical stress. Voltage ratings generally range from 50 V to 3 kV, with specialized high-power variants capable of withstanding up to 100 kV [43]. However, due to the relatively low permittivity of ceramic materials, these capacitors offer lower capacitance compared to electrolytic or film capacitors. While stacking multiple layers improves volumetric efficiency, it often reduces the voltage rating. Losses in ceramic capacitors are primarily attributed to frequency-dependent dielectric losses, which can vary significantly with aging.

Ceramic capacitors are compact, compatible with surface-mount technology, and suitable for high-frequency operation. However, their nonlinear capacitance behavior and sensitivity to operating conditions limit their application in safety-critical environments such as traction inverters. At typical EV DC-link voltages (400–800 V), their low capacitance can result in significant voltage ripple. With the adoption of wide-bandgap semiconductors (SiC, GaN), which enable higher switching frequencies, ceramic capacitors may become increasingly viable in future inverter designs [42].

Film Capacitors

Film capacitors, particularly metallized polypropylene film (MPPF) types, are extensively utilized in traction inverter DC-link applications due to their superior electrical performance and high reliability. These capacitors are manufactured from thin polymer films coated with a metallic layer under vacuum conditions. The metallized films are either wound into cylindrical rolls or stacked to create alternating layers of electrodes and dielectric, as illustrated in Fig. 2.19. This structural configuration provides high volumetric efficiency and minimizes parasitic elements, which is essential for high-performance power electronic systems.

The capability to produce extremely thin polymer films and apply partial metallization enables film capacitors to achieve high voltage ratings without a significant increase in physical size. Sprayed metal ends are employed to facilitate terminal connections, while the large electrode surface area reduces resistance, resulting in low equivalent

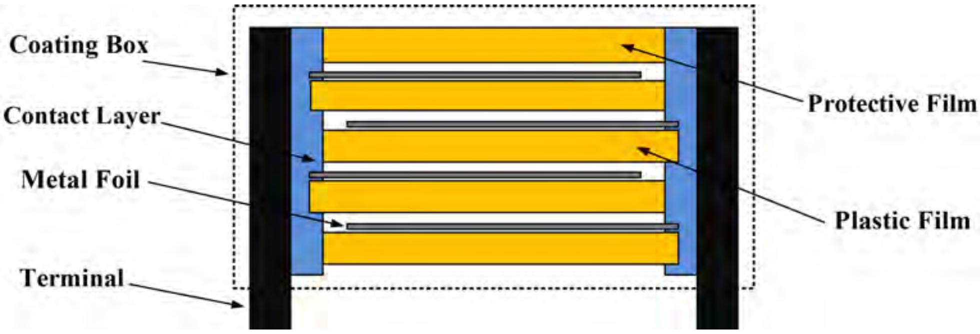

Figure 2.19: Cross-Sectional View of a Typical Plastic Film Capacitor [48].

series resistance (ESR). Furthermore, the close proximity of terminals to electrode layers minimizes equivalent series inductance (ESL), making these capacitors particularly suitable for high-frequency switching applications.

Common dielectric materials used in film capacitors include polypropylene (PP), polyester (PET), polycarbonate (PC), polystyrene (PS), and polytetrafluoroethylene (PTFE). These materials exhibit high dielectric strength, ranging from approximately 25 kV/mm for PET to 150 kV/mm for PTFE. Among these, polypropylene is the most widely adopted due to its excellent thermal stability and breakdown voltage (40–50 kV/mm), although it is more expensive than PET. PET offers a cost-effective alternative but has limited temperature tolerance, whereas PTFE provides superior dielectric properties and is reserved for high-end applications due to its high cost.

A distinctive characteristic of film capacitors is their self-healing capability. When a localized dielectric breakdown occurs, often due to manufacturing defects, a high-density current generates an arc that vaporizes the metallization surrounding the fault. This process isolates the defect and prevents catastrophic failure, as shown in Fig. 2.7. The self-healing mechanism occurs extremely rapidly, within approximately 10 μs, and affects only a microscopic region (approximately 50 nm), thereby ensuring continued operation without significant performance degradation [43].

Film capacitors also demonstrate excellent thermal stability, operating reliably across a wide temperature range. PP-based capacitors maintain performance from $-40°$C to $+125°$C, while PC and PTFE variants can withstand even higher temperatures. PET capacitors, although less stable, can be modified to tolerate up to 85°C or 105°C, depending on the application requirements.

Despite these advantages, film capacitors exhibit relatively low capacitance density, typically ranging from 1 nF to 100 μF, and therefore occupy more physical volume compared to ceramic or electrolytic capacitors. Additionally, their manufacturing process is more complex, which contributes to higher costs. Nevertheless, their combination of low ESR and ESL, high ripple current capability, and long operational life makes them the preferred choice for high-frequency switching applications in modern electric vehicle (EV) traction inverters. The absence of liquid electrolyte eliminates evaporation-related aging, further enhancing their reliability [43].

Applications

Electrolytic capacitors are widely employed in various electronic systems due to their simple construction and low cost. They are commonly used for filtering, bypassing, and decoupling purposes, as well as in applications requiring rapid energy discharge. Typical

examples include conventional motor drives, spot welding equipment, flashtube ignition circuits, airbag deployment systems, backup power supplies for microcontrollers, and camera flash units. In voltage regulator circuits, electrolytic capacitors play a critical role in suppressing ripple caused by load variations, thereby ensuring a stable output voltage. Their frequency-selective characteristics also make them suitable for use in audio amplifiers. The voltage ratings for these applications generally range from several tens to a few hundred volts [49], [42], [44]. Despite these advantages, electrolytic capacitors are constrained by their relatively low current-carrying capability and limited operational lifespan, which restrict their suitability for high-reliability applications.
Ceramic capacitors, which address many of the limitations associated with electrolytic types, are extensively used in integrated circuits, memory modules, and other electronic devices. However, their brittle dielectric material and susceptibility to mechanical and thermal stress present challenges for deployment in safety-critical systems such as traction inverters.
Film capacitors, owing to their high dielectric strength and low parasitic elements, are applied across a wide voltage spectrum. At low voltages (50 V to 250 V), they are commonly used in low-loss filtering applications. In the medium-voltage range (250 V to 630 V), they serve in analog-to-digital converters, signal processing circuits, timing circuits, and snubber networks. High-voltage film capacitors (630 V to 3 kV) are essential for industrial, high-power, and pulsed applications, while very high-voltage variants, capable of withstanding up to 20 kV, are employed in power generation and transmission systems. Their high current ratings, excellent thermal stability, and self-healing capability make metallized polypropylene film (MPPF) capacitors the preferred choice for DC-link applications in electric vehicles, despite their lower capacitance density.
The comparative analysis presented in Table 2.2 highlights the trade-offs among different capacitor technologies. While electrolytic capacitors offer high capacitance density at low cost, their high ESR and ESL, combined with limited thermal stability, restrict their use in high-performance environments. Ceramic capacitors provide low ESR and ESL but suffer from mechanical fragility and moderate thermal stability. Film capacitors, particularly MPPF types, exhibit superior thermal performance, very low parasitic elements, and self-healing capability, making them highly suitable for electric vehicle traction inverters and other demanding power electronic applications.

Table 2.2: Comparison of Capacitor Technologies.

Technology	Capacitance Density	ESR	ESL	Thermal Stability	Self-Healing	EV Suitability
Electrolytic	High	High	High	Low	No	Limited
Ceramic (MLCC)	Medium–High	Low	Low	Moderate	No	Conditional
Film (MPPF)	Medium	Very Low	Very Low	High	Yes	Excellent

In conventional three-phase inverters, the DC-link capacitor can occupy a substantial portion of the system volume up to 50%, particularly when electrolytic capacitors are used [49]. This spatial demand makes capacitor sizing a critical design consideration, as it directly influences the overall size and weight of the inverter system. The required volume for capacitors is primarily dictated by the energy storage capacity and the operating voltage. Therefore, optimizing the capacitor bank is essential for achieving high power density in drive systems. The stress on DC-link capacitors in three-phase inverters has been thoroughly investigated in studies [50], [51], which present analytical methods for calculating the root mean square (RMS) current stress in pulse-width-modulated (PWM) converter systems. These methods incorporate key system parameters such as switching frequency, load current, and DC-link voltage. Findings from these studies indicate that RMS current stress increases with higher load currents and lower switching frequencies, leading to a corresponding increase in the required capacitor size. This highlights the importance of accurately estimating RMS current stress to ensure optimal capacitor sizing and reliable inverter performance.

Capacitor Sizing for Electric Vehicles

A two-level inverter topology has been selected for this project due to its simplicity and compact capacitor bank design. Unlike multi-level inverters, which require additional voltage balancing circuitry for each level, two-level systems offer reduced complexity, improved power density, and, in many cases, higher efficiency. For DC-link voltages up to 800 V, film capacitors are particularly well-suited to two-level inverters, offering high reliability and excellent power density characteristics. The RMS current capability ensures that the capacitor can handle the reactive power demand of the load. In [50], a model for estimating the capacitor ripple current in a three-phase inverter with an inductive load is presented. The design of a capacitor bank is primarily determined by two key factors: RMS ripple current capability and voltage ripple suppression. For a space vector PWM (SVPWM) modulated three-phase inverter, the RMS capacitor current stress is given by:

$$I_{c,\mathrm{rms}} = I_{\mathrm{rms}}\sqrt{2M\left[\frac{\sqrt{3}}{4\pi} + \cos^2(\varphi)\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right]} \tag{2.35}$$

where I_{rms} is the RMS phase current, φ is the load power factor angle, M is the modulation index, defined as:

$$M = \frac{\hat{V}_u}{\frac{1}{2}V_{dc}}, \quad M \in \left[0, \frac{2}{\sqrt{3}}\right] \tag{2.36}$$

Here, $\hat{V}_u$ denotes the reference output voltage, and V_{dc} is the DC-link voltage. The resulting RMS current ripple stress, expressed in per-unit (p.u.) of the output current, is illustrated in Fig. 2.20. The global maximum current stress is approximately 0.65 p.u. at $\cos\varphi = 1$. Notably, the ripple current is independent of switching frequency and depends primarily on the modulation index and load power factor. The voltage ripple is related to the stored charge in the capacitor and can be expressed as:

$$Q(t) = CV_c(t) + \int_0^t i_c(t)\,dt \tag{2.37}$$

where $Q(t)$ is the capacitor charge, C is the capacitance, $V_c(t)$ is the instantaneous voltage, and $i_c(t)$ is the instantaneous current. Due to the integral term, voltage ripple is frequency-dependent—higher switching frequencies reduce the ripple amplitude.
The voltage ripple is typically defined as a percentage of the nominal DC-link voltage:

$$\frac{\Delta V_c}{V_{\mathrm{DC}}} = \frac{\Delta Q_c}{CV_{\mathrm{DC}}} \tag{2.38}$$

By integrating the capacitor current over time and rearranging the above expression, the minimum required capacitance to maintain the voltage ripple within acceptable limits can be determined for a given operating condition [55].

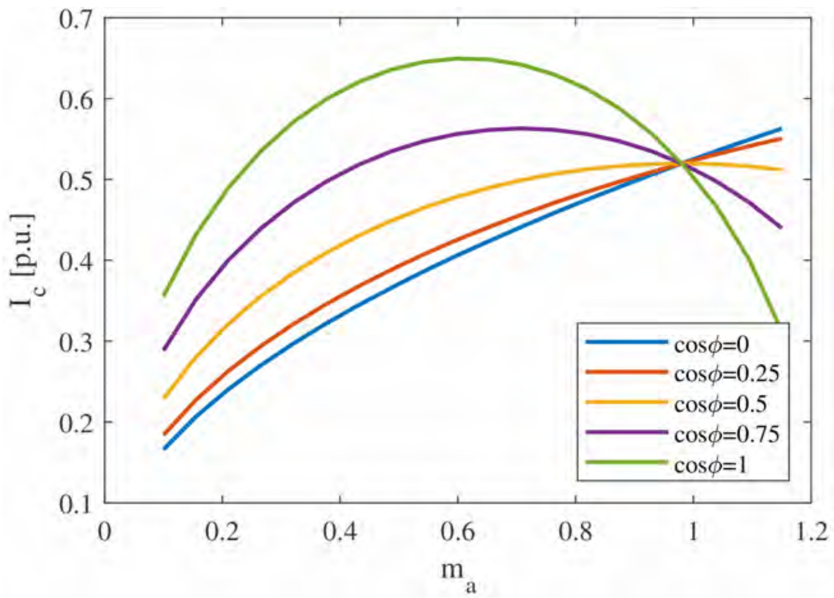

Figure 2.20: Capacitor RMS current stress in p.u. [52].

Recent developments have seen increased interest in multi-three-phase inverter architectures [3]-[5], as illustrated in Figure 2.21. These systems consist of multiple three-phase inverter bridges connected in parallel at the output, while sharing a common two-terminal DC input and a unified DC-link capacitor bank.

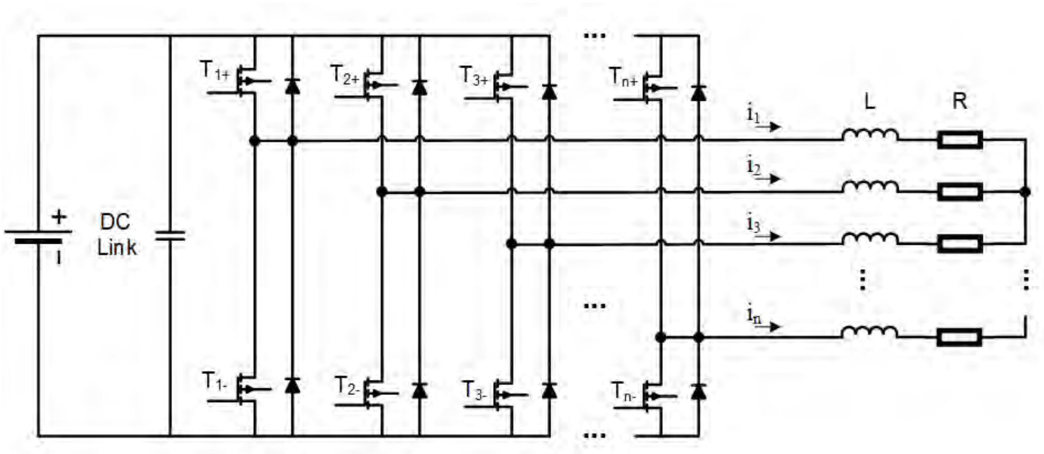

Figure 2.21: Multiphase voltage source inverter.

Although the total output power remains unchanged, the distribution of current across the phases is affected. Specifically, the output current per inverter leg is inversely proportional to the number of parallel systems:

$$I_n = \frac{1}{n} I_{3ph} \tag{2.39}$$

where n is the number of parallel three-phase bridges and I_{3ph} is the total output current. Despite the change in current distribution, the total semiconductor area required remains approximately constant across both conventional and multi-phase configurations. Studies have shown that multi-phase inverter topologies can reduce the current stress on the DC-link capacitor [54]-[57], thereby enhancing system power density. While capacitor sizing for multi-phase systems has been explored in the literature [53]-[54], many of these works lack a detailed analysis of power factor effects and often overlook the impact of DC-link voltage ripple. This omission is critical, as excessive ripple generated by the propulsion motor can adversely affect auxiliary systems connected to the traction battery. Similar analysis of the 6-phase equivalents performed in [52]. By employing PWM carrier wave shifting cancellation effects can be achieved in the capacitor bank, reducing the capacitor current stress further. The result of this study is shown in the next section.

Capacitor Current Modelling

In inverter systems, switching operations are typically governed by comparing a sinusoidal reference voltage with a high-frequency triangular carrier signal. The reference voltage for each phase can be expressed as:

$$v_{\mathrm{ref}}(t) = M \sin(\omega t + (n-1)\varepsilon), \quad n = 1, 2, 3, \ldots, N \tag{2.40}$$

where M is the modulation index, ε is the phase angle offset determined by the winding configuration, and N is the total number of phases.
To extend the voltage utilization range in modern drive systems, a zero-sequence component is often added to the reference waveform. This can be achieved either by injecting a third harmonic or by applying the min/max zero-sequence method, as described in [66]. The latter approach is adopted in this study due to its effectiveness in maximizing the DC-link voltage window.
The switching states of the inverter are determined by comparing the reference signal with the carrier waveform:

$$[s_1, s_2, \ldots, s_N]^{\mathrm{T}} = v_{\mathrm{ref}}(t) > v_{\mathrm{tri}}(t) \tag{2.41}$$

where s_n represents the state of the upper switch in phase leg n, assuming binary values of 0 or 1. The lower switch operates in the complementary state.
The output current for each phase is defined as:

$$i_{\mathrm{out},n}(t) = \hat{I} \sin(\omega t + (n-1)\varepsilon - \varphi), \quad n = 1, 2, 3, \ldots, N \tag{2.42}$$

where φ is the phase displacement between voltage and current.
The total inverter current is obtained by summing the contributions from all active phase legs:

$$i_{\mathrm{inv}}(t) = [i_1(t), i_2(t), \ldots, i_N(t)] \cdot [s_1, s_2, \ldots, s_N]^{\mathrm{T}} \tag{2.43}$$

This inverter current comprises two components: the DC current drawn from the source and the ripple current supplied by the capacitor:

$$i_{\mathrm{inv}}(t) = I_{\mathrm{DC}} + i_c(t) \tag{2.44}$$

Assuming the capacitor supplies only the AC component, the DC current can be extracted as the average value of $i_{\mathrm{inv}}(t)$. Rearranging the equation allows for the determination of the capacitor current $i_c(t)$. The root mean square (RMS) value of this current, I_c, is a key parameter in sizing the DC-link capacitor. For multi-phase inverter systems, the capacitor current modeling approach remains consistent with that of conventional three-phase systems, with phase currents scaled according to (2.39). The results reported in [52] are summarized in Table 2.3 and illustrated in Figure 2.22. It can be observed that

Table 2.3: Maximum capacitor current stress (p.u) vs PWM shift and cos φ

PWM Shift [%]	cosφ=0	cosφ=0.25	cosφ=0.5	cosφ=0.75	cosφ=1
0	0.56	0.55	0.52	0.565	0.65
10	0.48	0.47	0.435	0.42	0.5
20	0.42	0.4	0.37	0.345	0.34
30	0.35	0.35	0.34	0.34	0.34
40	0.325	0.325	0.36	0.425	0.5
50	0.27	0.27	0.37	0.5	0.65

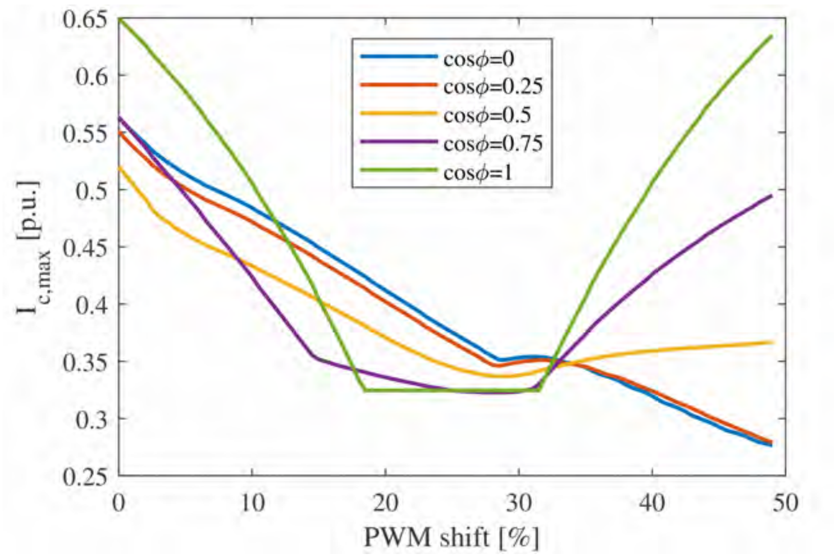

Figure 2.22: Capacitor current stress in a six-phase system (p.u.) as a function of PWM carrier shift [52].

the maximum capacitor current stress can be reduced from approximately 0.65 p.u. to 0.375 p.u. through an optimal selection of the PWM carrier wave phase shift.
Similarly, voltage ripple decreases monotonically with increasing carrier wave shift, as this effectively raises the switching frequency experienced by the capacitor bank. This trend is summarized in Table 2.4 and illustrated in Figure 2.23.

Table 2.4: Normalized capacitance requirement (p.u.) vs PWM shift and cos φ

PWM Shift [%]	cosφ=0	cosφ=0.25	cosφ=0.5	cosφ=0.75	cosφ=1
0	1	0.97	0.88	0.7	0.55
10	0.83	0.8	0.74	0.6	0.45
20	0.69	0.67	0.6	0.3	0.2
30	0.55	0.53	0.5	0.42	0.2
40	0.45	0.45	0.45	0.48	0.45
50	0.35	0.35	0.35	0.43	0.55

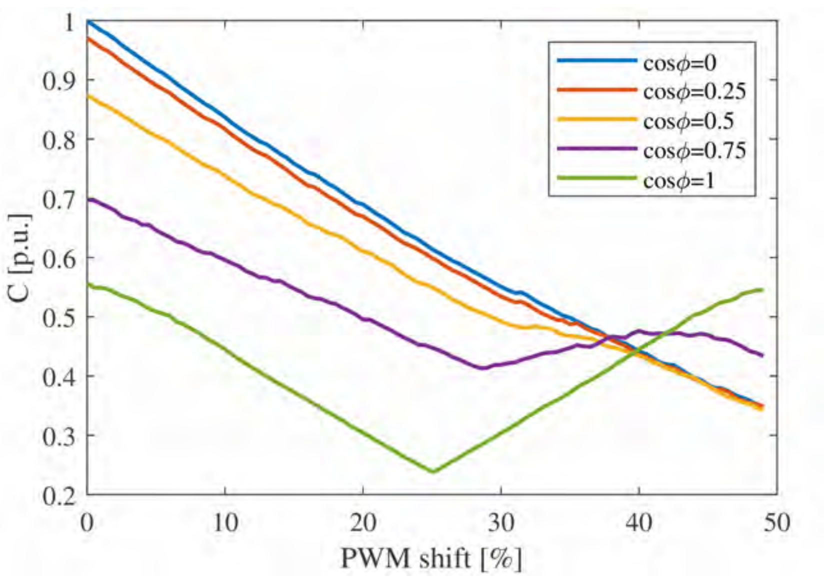

Figure 2.23: Reduction in DC-link capacitance requirement with increasing PWM carrier shift [52].

2.1.3 Electro–Thermal Loss Modeling and Reliability of DC–Link Capacitors

DC–link capacitors play a critical role in energy buffering, ripple current mitigation, and electromagnetic compatibility (EMC) in modern power electronic converters. However, they also represent a major contributor to system volume, cost, and field failure rates. A comprehensive *electro–thermal* framework for capacitor design and reliability assessment integrates: (i) loss and impedance modeling, (ii) thermal dynamics including ambient and bank-level coupling, (iii) physics-of-failure and lifetime prediction, (iv) safe operating area (SOA) boundaries, (v) EMI-aware tank optimization, (vi) mission-profile-based accelerated testing, and (vii) multi-drive reliability behavior. The following subsections synthesize key principles and findings relevant to electrolytic, metallized polypropylene film, and ceramic capacitors [58, 60, 64].

Loss and Impedance Modeling

A simplified capacitor model for pre-design and EMI analysis consists of a series C–ESR–ESL branch with a parallel insulation resistance R_p. The total power loss combines AC ripple and DC leakage components:

$$P_{\text{loss}} = i_C^2 R_s + \frac{v_C^2}{R_p}, \tag{2.45}$$

where R_s (ESR) dominates ripple loss and R_p governs leakage, both strongly dependent on temperature and voltage [58]. The hotspot temperature rise is estimated as:

$$T_h = T_a + R_{\text{TH}} \cdot P_{\text{loss}}, \tag{2.46}$$

where T_a is ambient temperature, R_{TH} is thermal resistance. The capacitor temperature can be calculated by:

$$T_{cap} = \Delta T_h + T_a + P_{loss} R_{TH} \tag{2.47}$$

forming the basis for SOA and lifetime calculations. ESR and ESL exhibit frequency dependence, and ESR also varies with temperature; however, a C–ESR–ESL model parameterized from datasheets or measurements is typically sufficient for ripple and EMI pre-design [59].

Thermal Modeling with Ambient Dynamics

Classical thermal models often assume instantaneous transmission of ambient fluctuations to the hotspot, which is unrealistic. A corrected representation is:

$$T_h(s) = Z_{T_h}(s)P_{\text{loss}}(s) + G_{T_a,h}(s)T_a(s), \tag{2.48}$$

where $G_{T_a,h}(s)$ behaves as a low-pass filter due to the large thermal capacitance of passive components [61]. This refinement avoids overestimating daily or seasonal T_h swings and improves long-term lifetime prediction accuracy.

Bank-Level Thermal Coupling and Thermal Matching

In capacitor banks, interior units often operate at higher temperatures due to reduced convection and mutual thermal coupling. Analytical or state-space models can capture these effects with less than 10% error compared to FEM simulations, while computing in seconds rather than minutes. Such models enable *thermal matching*—adjusting capacitance, ratings, or placement to equalize temperatures and extend weakest-link lifetime [62].

Degradation Mechanisms and Lifetime Prediction

Electrolytic capacitors (Al): Wear-out is dominated by electrolyte evaporation, leading to ESR increase; high ripple and temperature can induce thermal runaway [60]. **Metallized polypropylene film:** Self-healing clears local breakdowns, causing gradual capacitance decline; humidity can corrode ultra-thin metallization along edges [60]. **Ceramic capacitors (MLCC):** Intrinsic wear-out is negligible under normal conditions, but insulation degradation, flex cracking, and thermo-mechanical stress can dominate depending on voltage and temperature [60].
A widely used empirical lifetime model combines Arrhenius thermal acceleration with voltage stress:

$$L = L_0 \left(\frac{V}{V_0}\right)^{-n} \exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_h} - \frac{1}{T_0}\right)\right], \tag{2.49}$$

where $n \approx 3$–5 for electrolytics and $n \approx 7$–9 for film capacitors [60]. For dynamic operation, damage accumulation follows Miner's rule:

$$D = \sum_j \frac{\Delta t_j}{L_j}, \qquad \text{failure when } D = 1. \tag{2.50}$$

For ripple-dominated applications, a practical thermal link is:

$$T_h = T_a + R_{\text{TH}} \sum_i \text{ESR}(f_i, T)\, I_{\text{rms}}^2(f_i), \tag{2.51}$$

validated experimentally within a few degrees Celsius [64].

Safe Operating Area (SOA) of Film DC–Link Capacitors

An SOA map defines permissible operating points in (v_C, i_C) for given ambient conditions and degradation states [58]. Three primary boundaries apply:

$$\text{(Current)} \quad i_C = I_{\text{rp,max}}, \tag{2.52}$$

$$\text{(Thermal)} \quad i_C^2 R_s + \frac{v_C^2}{R_p(T_a, v_C)} = \frac{T_{h,\max} - T_a}{R_{\text{TH}}}, \tag{2.53}$$

$$\text{(Voltage)} \quad v_C \le \alpha V_{C,r}. \tag{2.54}$$

End-of-life parameter drift ($R_s \uparrow$, $R_p \downarrow$) and production tolerances should be propagated (e.g., via Monte Carlo) to obtain confidence bands. Leakage-driven thermal limits can precipitate runaway at high V and T_a [58].

2.1.4 Busbar Dimensioning

Busbars serve as the primary high-current interconnection elements that integrate power semiconductor switches, DC-link capacitors, and external terminals into compact commutation loops. Their electromagnetic, thermal, mechanical, and insulation characteristics critically influence voltage overshoot, switching losses, electromagnetic interference (EMI), and overall system reliability in high-power voltage-source inverters and multi-level converters. With the adoption of wide-bandgap devices such as SiC and GaN, which are capable of switching transitions exceeding 100 V/ns, busbar parasitics—particularly loop inductance and parasitic capacitance—have evolved from secondary considerations to primary design constraints [67]-[69].
This section synthesizes insights from eight key references, covering laminated planar busbars, PCB-based busbars, and non-laminated multi-port DC-link structures. The discussion addresses the modeling and minimization of parasitics, current density and thermal management, insulation and partial discharge (PD) considerations, DC-link capacitor integration, validation methodologies, and practical design guidelines for SiC-based converters [67]-[74]. The DC and AC current paths for different bus bar applications is illustrated in Figure 2.24.

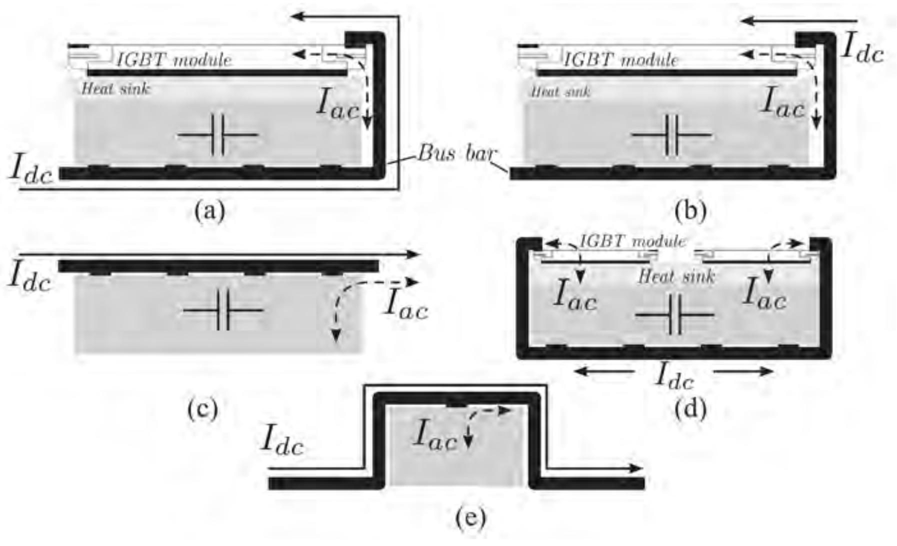

Figure 2.24: DC and AC current paths for different bus bar applications [67].

Performance Metrics and Dominant Parasitics

Loop inductance is a critical parameter because turn-off voltage overshoot is directly proportional to the commutation loop inductance L_{loop} and the current slew rate, as expressed by

$$\Delta V \approx L_{\text{loop}} \frac{\Delta I}{\Delta t}, \tag{2.55}$$

where

$$L_{\text{loop}} = L_{\text{package}} + L_{\text{busbar}} + L_{\text{connector}} + \text{ESL}_{\text{decoupling}}. \tag{2.56}$$

Busbar geometry and capacitor placement dominate the external inductance contribution. For SiC devices switching at 50 V/ns to 200 V/ns, even tens of nanohenries can result in overshoots of several hundred volts if not mitigated [67]-[69].
Stray capacitance also plays a significant role in EMI behavior. Laminated or parallel-plate busbars exhibit distributed capacitance, which can be approximated as

$$C_{\text{busbar}} \approx \varepsilon_0 \varepsilon_r \frac{w \cdot l}{d}, \tag{2.57}$$

where d is the dielectric thickness. While higher capacitance reduces differential-mode impedance at high frequencies and can improve noise shaping, it must be balanced against inductance and unwanted coupling to AC switching nodes [67], [68].
Thermal considerations are equally important. A widely accepted guideline limits copper current density to approximately $5\,\text{A/mm}^2$ under passive cooling to prevent hotspots and insulation degradation [67], [68]. At MHz-range harmonics, the skin depth

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \tag{2.58}$$

significantly reduces the effective cross-sectional area, making thickness increases ineffective. Instead, short vertical loops and multiple parallel layers are preferred for both electrical and thermal performance [67], [68].

Busbar Technologies: Laminated, PCB-Based, and Non-Laminated

Laminated planar busbars, considered the industry standard, consist of stacked copper plates separated by thin dielectric layers such as Kapton, Mylar, or FR-4. These structures provide strong mutual coupling, predictable impedance, and robust mechanical integrity. Proper edge sealing, with epoxy being more effective than molded or open edges, mitigates creepage and partial discharge risks at higher voltages [67], [69]. Laminated designs typically achieve inductances in the tens of nanohenries for two- and three-level VSIs, validated through impedance analysis and double-pulse testing [67]. Their main advantages include low inductance, good thermal spreading, and mature manufacturing processes, although they can be costly and complex to implement in multi-level topologies [67], [69].
PCB-based busbars have emerged as a promising alternative for WBG-based converters. By leveraging multilayer PCB technology, these designs minimize dielectric spacing, integrate sensors and gate drivers, and reduce assembly costs. In SiC converters rated between 50 kW to 200 kW, PCB busbars can achieve loop inductances as low as 10 nH, outperforming some laminated designs, while providing large built-in DC-link capacitance and minimal coupling to switching nodes [69], [68]. However, design considerations include ensuring that outer layers carry most of the current, avoiding overlapping of switching

and DC planes, and validating partial discharge performance under PWM stress rather than only at 50/60 Hz [68], [69].
For high-capacity converters, such as 315 kW photovoltaic systems, large laminated plates may be impractical. In these cases, non-laminated multi-port DC-link busbars, implemented as segmented copper networks, can be effective if resonance behavior is accurately predicted and mitigated. [71] introduced a matrix-admittance approach and the Resonance Current Gain (RCG) metric to quantify capacitor RMS current amplification. Optimized geometries reduced RMS current by up to 49 %, approaching the performance of laminated designs.

Current Distribution, Terminations, and Thermal Design

Current distribution is strongly influenced by terminal symmetry. Non-uniform current paths lead to localized heating and insulation stress, which can be mitigated by using symmetrically placed DC input tabs and evenly spaced module terminals. For distributed capacitor banks, symmetric terminal placement along the long axis yields the most uniform current distribution [67], [74]. The distribution of AC ripple currents, on the other hand, depends primarily on the relative positioning of switches and DC-link capacitors. Balanced AC loop lengths are essential to prevent capacitor overstress [72], [67].
At high frequencies, skin and proximity effects become dominant. At frequencies between 10 and 50 MHz, the skin depth can fall below 10 µm, making additional copper thickness ineffective. Multi-layer parallel planes, short vertical loops, and the use of outer layers with solder or copper jumpers enhance both high-frequency conduction and thermal performance in PCB busbars[67], [68].

Insulation, Partial Discharge, and Edge Treatment

The choice of dielectric material and its thickness plays a critical role in determining the insulation performance of busbars. Materials such as Kapton and Mylar provide high breakdown strength, whereas FR-4 and epoxy powder coatings offer a more economical solution with moderate electrical ratings. Increasing dielectric thickness enhances the withstand voltage capability; however, this improvement comes at the cost of higher loop inductance and reduced stray capacitance, creating a fundamental trade-off between insulation strength and electromagnetic performance [67], [68].
Edge treatment is another essential consideration for ensuring long-term reliability. Open edges, while cost-effective, are highly susceptible to contamination from moisture and dust, which can lead to insulation degradation and partial discharge (PD) activity. In contrast, epoxy-filled edges provide a robust protective barrier and are strongly recommended for harsh environmental conditions and applications involving higher DC voltages [69], [67].
Partial discharge behavior under PWM stress differs significantly from that observed in conventional 50/60 Hz sinusoidal testing. In WBG-based converters, the combination of high dv/dt, localized electric field intensification at cutouts, and voids within the insulation system can accelerate PD inception. Therefore, PD-free design requires careful attention to layout optimization, including the use of rounded corners, adequate creepage and clearance distances, and the elimination of sharp edges. Recent studies have demonstrated that laminated busbars can achieve PD-free operation in medium-voltage applications, such as aircraft power systems and renewable energy converters, provided that appropriate dielectric materials and edge treatments are employed [69], [68].

DC-Link Capacitor Selection, Arrangement, and Co-Design

Placing low-ESL decoupling capacitors as close as possible to the switching devices, specifically across the module DC+ and DC− terminals—significantly reduces the effective commutation loop inductance and confines high-frequency currents locally. PCB-based busbars facilitate this integration by allowing thin, multilayer decoupling boards to be interleaved between device leads and the main DC planes. This approach has been shown to achieve loop inductances in the range of 15–20 nH even when using discrete TO-247 packages [69], [68].

For traction inverters and other high-performance systems, distributing ceramic capacitor banks symmetrically above the power modules minimizes loop area and shortens high-frequency current paths. Experimental results have reported busbar inductances as low as 2–3 nH without connectors and approximately 16 nH with connectors, resulting in manageable turn-off overshoot of around 14% during double-pulse testing [74].

Reliability considerations further complicate capacitor selection. Lifetime degradation is influenced by temperature, voltage stress, ripple current spectrum, and the self-healing characteristics of the dielectric. A reliability-driven design approach should combine electrical-thermal modeling, including ESR variation with frequency and temperature, with lifetime prediction models based on voltage and Arrhenius stress exponents. Experimental validation through ripple injection and FFT-based characterization is essential to avoid unnecessary oversizing and to ensure predictable aging behavior [73].

Table 2.5: Qualitative comparison of busbar options.

Attribute	**Laminated Planar**	**PCB Busbar**	**Non-laminated (Segmented)**
Typical $L_{\mathbf{busbar}}$	Tens of nH [67]	10–20 nH [68]	Higher but tunable via RCG [71]
HF Current Handling	Good (short spacing)	Excellent (thin dielectric + multilayer)	Moderate; geometry-dependent
Current Capacity (DC)	High (thick Cu, 3D forms)	Limited by copper thickness and thermal constraints; outer layers preferred	High (bulk copper bars)
Insulation / PD	Mature; epoxy edge sealing	Requires PWM-PD validation	Needs careful creepage/clearance
Cost / Manufacturing	Medium–High	Low–Medium (automation)	Low–Medium (simple machining)

3
Design results

This chapter outlines the design of a double–three–phase SiC-based traction inverter for heavy-duty EV applications. The focus is on achieving high power density and reliable thermal performance through integrated design of the DC-link, laminated busbar, and control board. Two DC-link layouts are compared to assess the impact of mechanical placement on heat dissipation and capacitor lifetime.
The inverter employs a SiC power module for reduced losses and higher switching frequency, supported by a liquid-cooled housing for thermal stability. A six-layer control board with integrated DSP and EMI mitigation ensures compactness and robust control. The chapter covers system requirements, semiconductor selection, DC-link design, and prototype implementation.

3.1 Requirements

The inverter architecture consists of several integrated subsystems designed to ensure high performance, reliability, and thermal stability under demanding operating conditions. Figure 3.1 illustrated the overview of the experimental setup. The DC link provides energy buffering and stabilizes the DC voltage during dynamic load variations. A SiC-based gate driver enables fast and reliable switching of the power semiconductors, while the control board executes real-time control algorithms and signal processing tasks. Thermal management is achieved through a liquid-cooling system that uses a water–glycol mixture to maintain semiconductor junction temperatures within safe operating limits. The housing offers mechanical protection and facilitates integration with the vehicle chassis. Additionally, sensors and feedback channels provide accurate current and voltage measurements for closed-loop control, while a digital signal processor (DSP) coordinates control logic and communication functions.
The inverter is designed for heavy-duty truck (HDT) applications. Table 3.1 summarizes the key parameters of the vehicle model used in the simulation. The simulated drive cycle corresponds to the Heavy Heavy-Duty Diesel Truck (HHDDT) cruise mode, illustrated in Figure 3.2.
The target specifications for the inverter are summarized in Table 3.2. The primary design objective is to maximize power density through innovations such as integrated sensing, a reduced DC-link capacitor bank, and compact packaging.

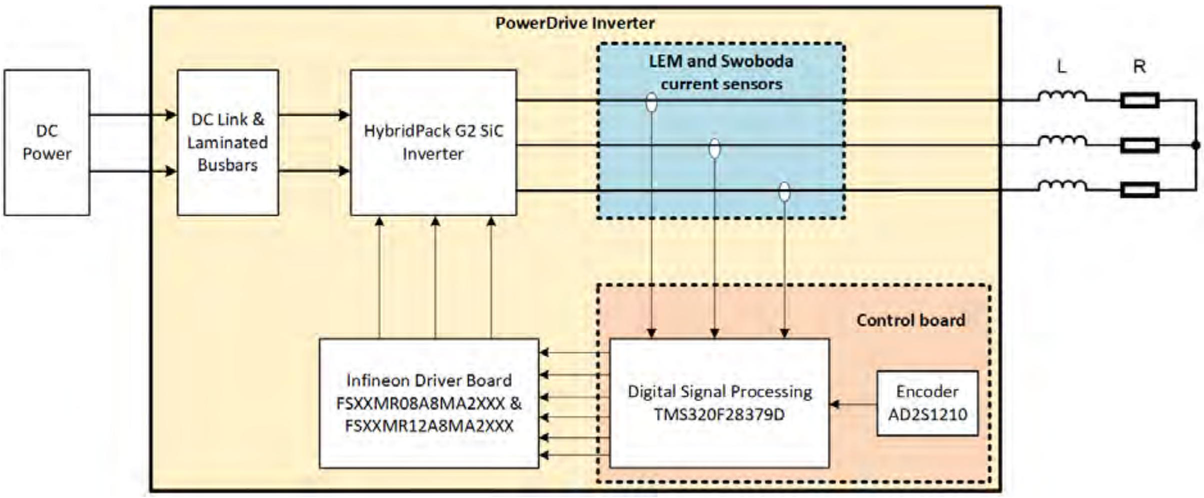

Figure 3.1: System overview of the experimental setup.

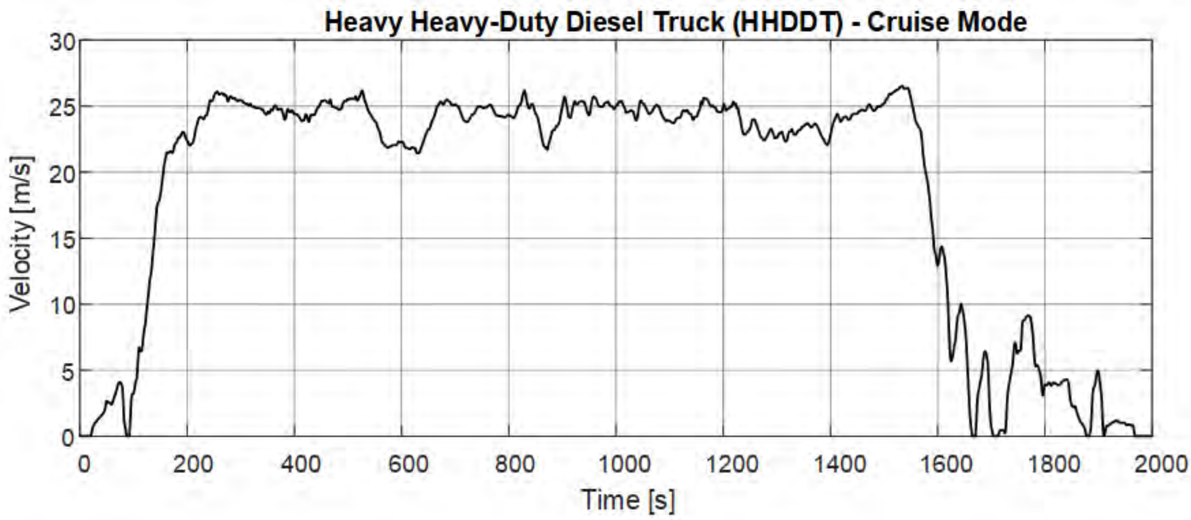

Figure 3.2: Drive cycle of the electric heavy-duty truck (HHDDT).

Table 3.1: Key parameters of the vehicle model used in the simulation.

Parameter	Value
Aerodynamic drag coefficient	0.53
Front cross-sectional area [m^2]	9.7
Rolling resistance coefficient	0.0051
Vehicle mass [kg]	40,000
Wheel radius [m]	0.5
Transmission ratio	19
Number of machines	2

3.2 Semiconductor Choice

The inverter design employs a six-pack SiC MOSFET power module, specifically the Infineon HybridPack FS03MR12A7MA2B, shown in Figure 3.3. This module integrates six SiC MOSFET switches in a compact automotive-grade package, optimized for high-

Table 3.2: Target specifications of the traction inverter.

Parameter	**Value**	**Unit**
DC link voltage	800	V
Maximum DC current	638	A
Maximum phase current (RMS)	260	A
Maximum power	450	kW
Volumetric power density	63	kW/L
Gravimetric power density	33	kW/kg
Switching frequency	20	kHz
DC-link capacitance	440	μF

efficiency traction inverters. The use of SiC technology offers significant advantages over conventional silicon IGBTs, including lower switching losses, higher allowable junction temperatures, and improved efficiency at high switching frequencies. These characteristics enable higher power density and reduced cooling requirements, which are critical for electric heavy-duty vehicle applications.

Figure 3.3: Infineon HybridPack FS03MR12A7MA2B SiC module used in the inverter design.

The choice of this SiC module was driven by several key factors:

- **High Voltage and Current Capability:** Rated for 1200 V and 360 A DC, the module supports the 800 V DC-link voltage and high current demands of heavy-duty traction systems.
- **Low Conduction and Switching Losses:** The low $R_{\mathrm{DS(on)}}$ (2.2 mΩ at 25°C) minimizes conduction losses, while the fast switching capability reduces switching losses, enabling operation at 20 kHz without excessive thermal stress.
- **Thermal Performance:** A low thermal resistance from junction to coolant (0.118 K/W) combined with a liquid-cooled baseplate ensures efficient heat removal, supporting continuous high-load operation.
- **Automotive Qualification:** The HybridPack family meets automotive standards for vibration, thermal cycling, and reliability, making it suitable for traction applications.

Table 3.3 summarizes the main electrical and thermal characteristics of the selected module. These parameters are critical for inverter design, influencing gate driver requirements, thermal management strategy, and overall system reliability.

Table 3.3: Key properties of the Infineon HybridPack SiC module.

Parameter	Value	Unit
Drain-source voltage rating	1200	V
Continuous DC current	360	A
On-state gate voltage	+18	V
Off-state gate voltage	-5	V
$R_{\mathrm{DS(on)}}$ at 25°C	2.2	mΩ
$R_{\mathrm{DS(on)}}$ at 175°C	4.7	mΩ
Thermal resistance (junction-to-coolant)	0.118	K/W
Maximum junction temperature	175	°C
Module weight	800	g

Design Implications

The adoption of SiC MOSFET technology allows the inverter to achieve:

- **Higher Switching Frequency:** Enables smaller passive components and improved current control bandwidth.
- **Reduced Cooling System Size:** Lower losses translate into reduced heat generation, allowing a more compact liquid-cooling system.
- **Improved Efficiency:** Particularly under partial-load conditions, which dominate real-world drive cycles.

These benefits collectively contribute to achieving the target power density and efficiency goals outlined in Section 3.2.

3.3 DC-Link Capacitor Bank Design

Based on the target specifications of the traction inverter and using (2.35), the calculated DC-link RMS current is approximately 165 A. Considering an appropriate safety margin, nine polypropylene film capacitors (TDK Part No. B32778Z9506K000) were selected for the DC-link capacitor bank.

Each capacitor has a maximum RMS current rating of 22.5 A, resulting in a combined RMS current capability of 202.5 A. Furthermore, each capacitor provides a capacitance of 50 μF, giving a total DC-link capacitance of 450 μF, which satisfies the inverter's design requirements.

The key specifications of the selected capacitors are summarized in Table 3.4.

Table 3.4: Key properties of the selected film capacitors

Parameter	Value	Unit
Rated DC voltage	900	V
Capacitance (total)	50×9	μF
Maximum RMS current	22.5×9	A
Equivalent series resistance (ESR)	5.6/9	mΩ
Self-inductance	15	nH
Rate of voltage rise	22	V/μs
Dimensions	$35 \times 50 \times 57.5$	mm

3.3.1 Busbar Selection

The rated DC voltage of the capacitor, relative to the system's peak operating voltage, is a critical factor influencing its lifetime, along with the internal hot-spot temperature. However, increasing the voltage rating generally reduces the capacitance, which can compromise the inverter's transient performance.
To address this trade-off, the design incorporates a low-inductance laminated busbar structure that minimizes parasitic inductance and mitigates voltage overshoot during fast switching events. This approach enables the selection of capacitors that achieve an optimal balance between electrical performance, thermal reliability, and long-term durability.
ROLINX laminated busbars from Rogers Corporation were selected for the DC-link interconnection. A laminated busbar consists of multiple conductive layers (copper or aluminum) separated by thin dielectric materials, laminated into a single structure. Similar to a multilayer PCB but with much thicker conductors, this design supports significantly higher current levels—ranging from tens of amps to several kiloamps for the thickest conductors.
The ROLINX CapLink series is specifically designed to integrate capacitors directly into the laminated busbar, resulting in a lightweight, extremely low-inductance assembly with high power density. Since these busbars are fully custom-made, their electrical ratings and physical layout can be tailored to accommodate the required number of capacitors. The typical specifications of the selected busbar are shown in Table 3.5.

Table 3.5: Rolinx Caplink typical values

Voltage rating [V]	400 to 1200
Peak voltage [V]	1600
I_{DC} or I_{AC} [A] (cont.)	60 to 500
Stray inductance [nH]	$<$ 10 (depending on terminal design)
No. of capacitors	2 to 10+
Operating temperature [°C]	+105 (typ., continuous)
Relative humidity [%]	95 (at +55 °C)
Conductor material	Copper, Aluminum
Plating	Sn, Ni
Insulation CTI [V]	$\leq$ 600

Two busbar configurations were manufactured and supplied by Rogers Corporation for evaluation:

- Case I: Capacitors mounted on the top side of the busbar, with the busbar surface in contact with the inverter housing (used as a cooling interface).
- Case II: Capacitors mounted on the bottom side, in direct contact with the inverter housing for improved thermal conduction.

Figures 3.4 and 3.5 illustrate the two configurations.

3.4 Prototypes

The inverter prototype is designed with an integrated liquid-cooling system that uses a water-glycol mixture and incorporates the Infineon six-pack SiC-based power module. The key specifications of this module are listed in Table 3.2. Leveraging wide-bandgap

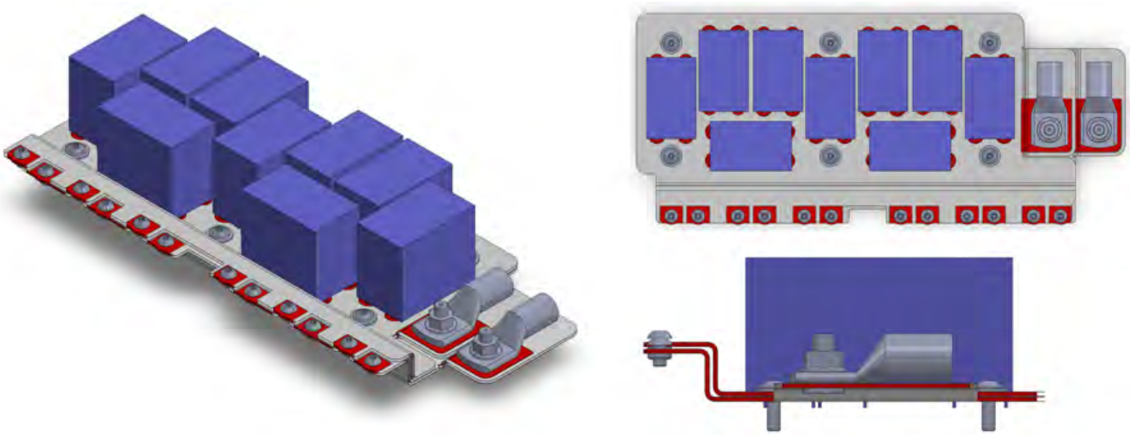

Figure 3.4: Case I: DC-link design with capacitors on the upper side

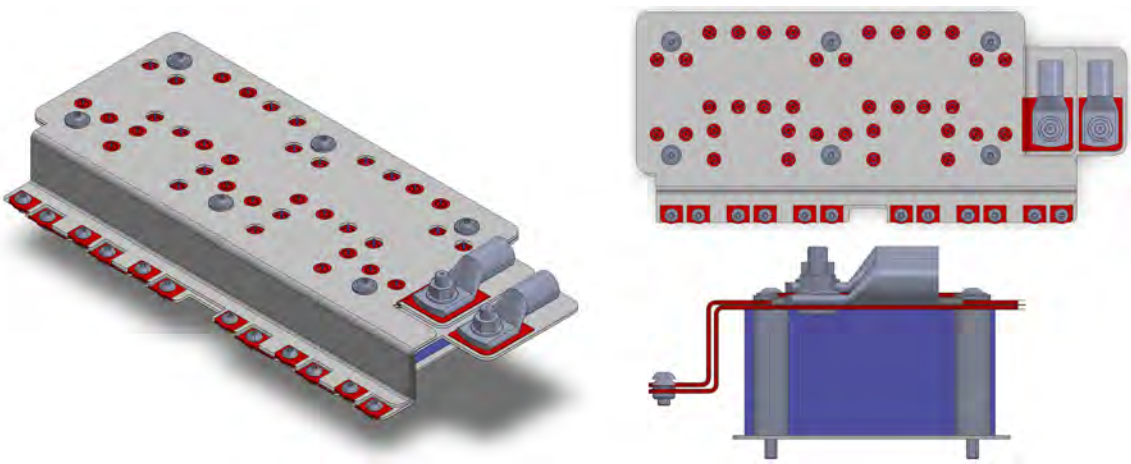

Figure 3.5: Case II: DC-link design with capacitors on the lower side

SiC technology, the module supports a blocking voltage of 1200 V while maintaining low on-state resistance and reduced switching losses. Its baseplate features a pin-fin structure that enhances heat transfer and minimizes thermal resistance between the semiconductor junction and the coolant. This design achieves a power density in the range of 200–250 kW/kg.

The prototyped inverter housing is designed so that the coolant channel and the bottom surface of the enclosure form a single integrated structure, improving thermal dissipation from both the power modules and the DC-link capacitors. To evaluate the thermal performance of different DC-link configurations, two versions of the inverter have been developed. The primary difference between these configurations lies in the placement of the DC-link capacitors relative to the laminated busbar.

Case I positions the capacitors on the upper side of the DC-link, with the busbar located beneath them. In this arrangement, the busbar is attached to a thermal interface pad and the bottom housing, enabling heat from the capacitors to be conducted through the busbar to the housing.

Case II places the capacitors on the lower side of the DC-link, in direct contact with the bottom housing, while the busbar is mounted on top. This configuration provides a more direct thermal path for capacitor cooling.

Both configurations are illustrated in Figures 3.6 and 3.7. These prototypes will be experimentally evaluated to compare the thermal performance of the two DC-link designs.

Case I: Upper-Side Capacitors

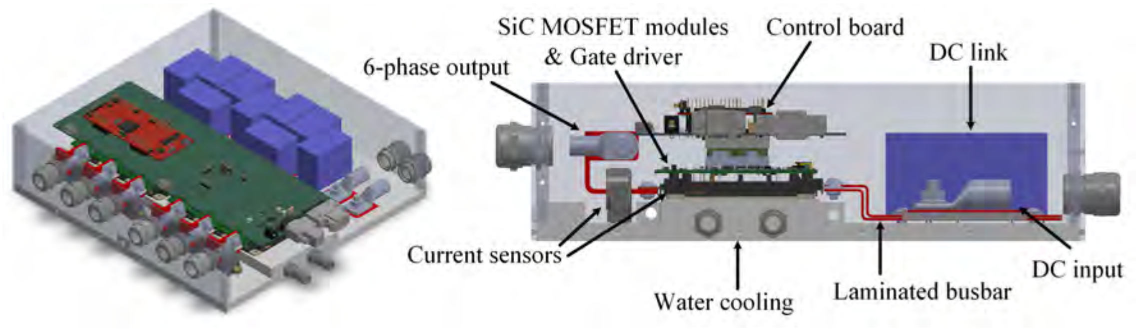

Figure 3.6: Prototype inverter with DC-link capacitors mounted on the upper side

Case II: Lower-Side Capacitors

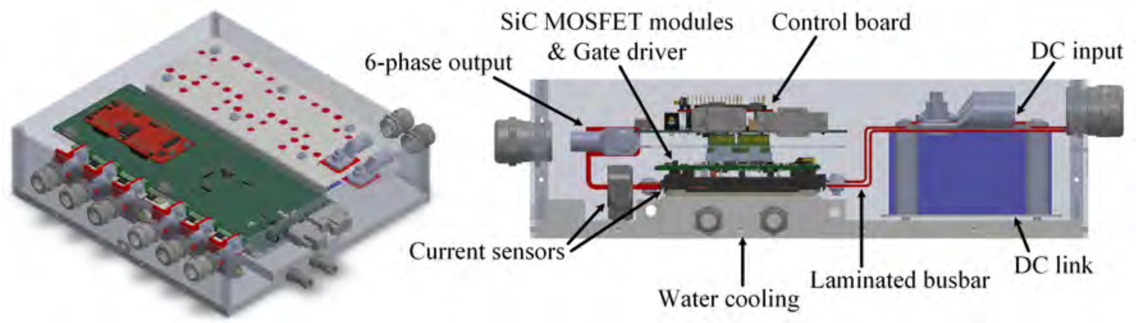

Figure 3.7: Prototype inverter with DC-link capacitors mounted on the lower side

3.4.1 Control Board

The control board has been developed to manage the HybridPack SiC MOSFET gate drivers and associated control functions. It integrates four primary subsystems: power supply regulation, resolver interface, digital signal processing (DSP), and PWM-based gate driver control. To achieve high power density, the control board is mechanically mounted directly above the gate drivers and power modules, which are significant sources of electromagnetic interference (EMI). To mitigate EMI and ensure signal integrity, the PCB employs a six-layer stack-up arranged as follows: signal, ground, 5 V, 12 V, ground, and ground layers from top to bottom. This configuration enhances EMI shielding and provides robust power distribution. The PCB was designed using KiCad, and its layout is shown in Figure 3.8, while the corresponding schematic is presented in Figure A.1.

Power Supply The Infineon gate driver requires a 12 V supply capable of delivering up to 25 W, as well as a 5 V rail for current sensors. The control board provides regulated outputs of 3.3 V, 5 V, and 12 V to power the DSP, resolver circuit, and gate driver

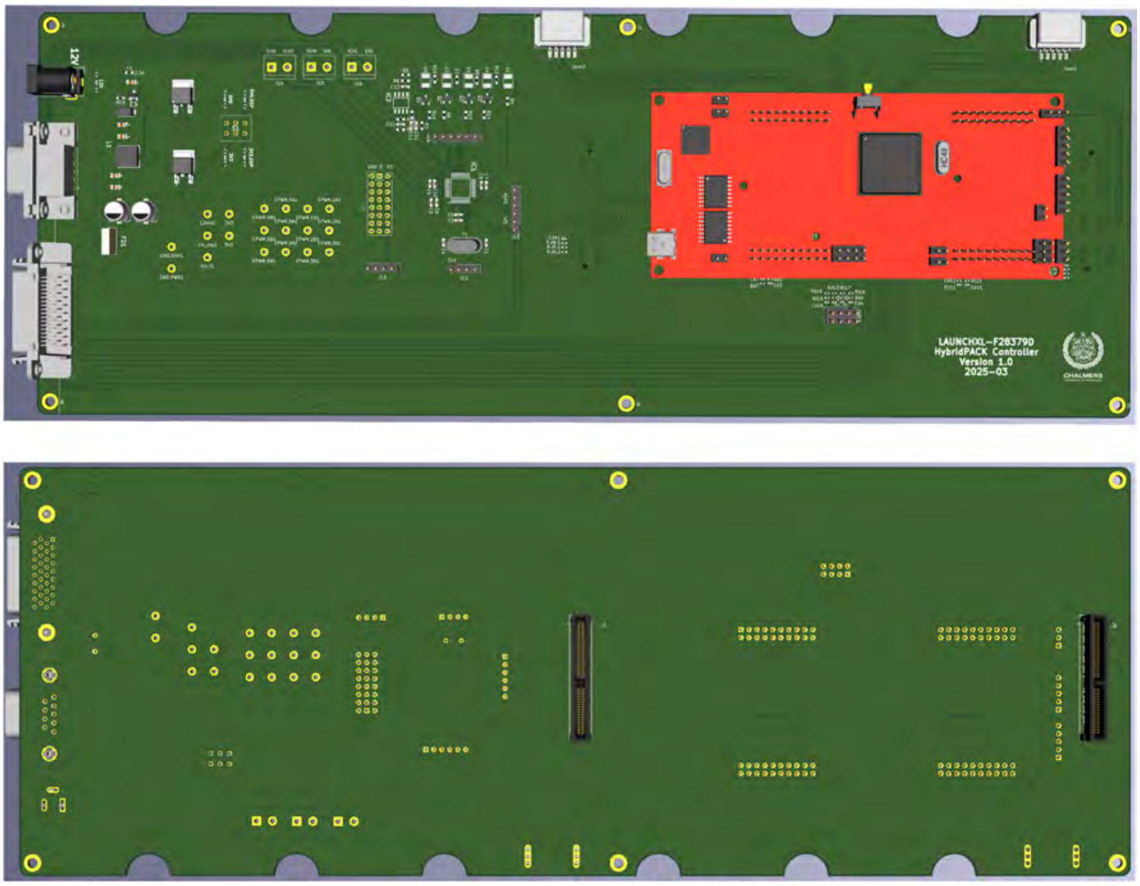

Figure 3.8: Top view (upper) and bottom view (lower) of the designed control board

board, respectively. To comply with CISPR 32 conducted emission standards, an input PI filter has been implemented to suppress EMI from the DC/DC converter. The emission performance was simulated using LTpowerCAD, targeting compliance with CISPR 32 Class B limits. The conducted emission requirement is shown in Figure 3.9, and the simulated filter response is presented in Figure 3.10.

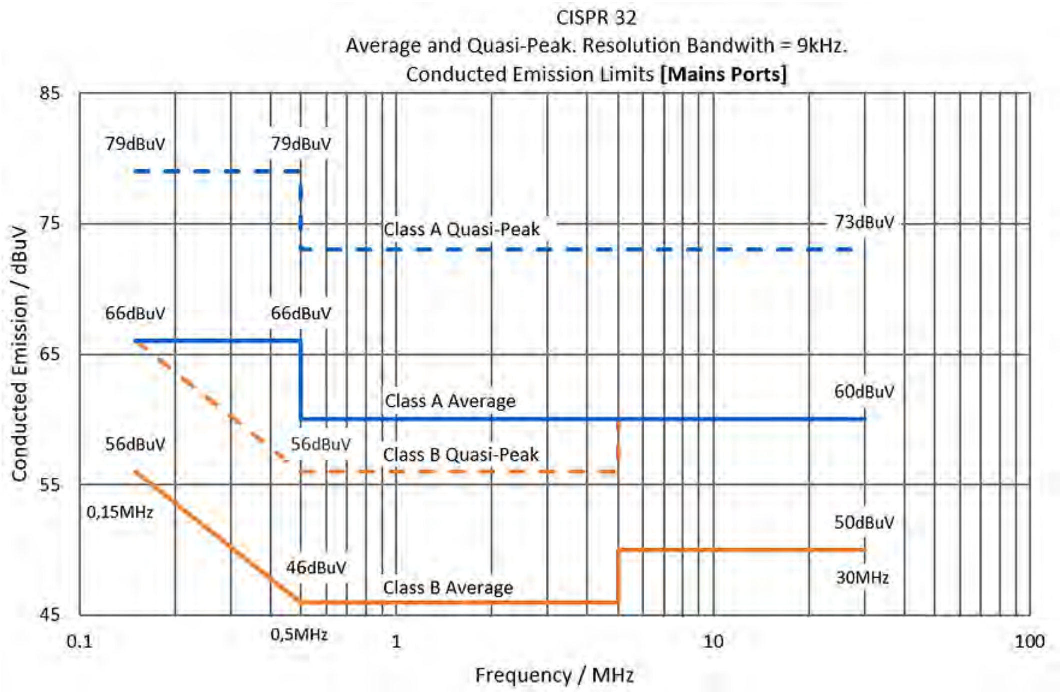

Figure 3.9: Conducted emission limits according to CISPR 32 standard

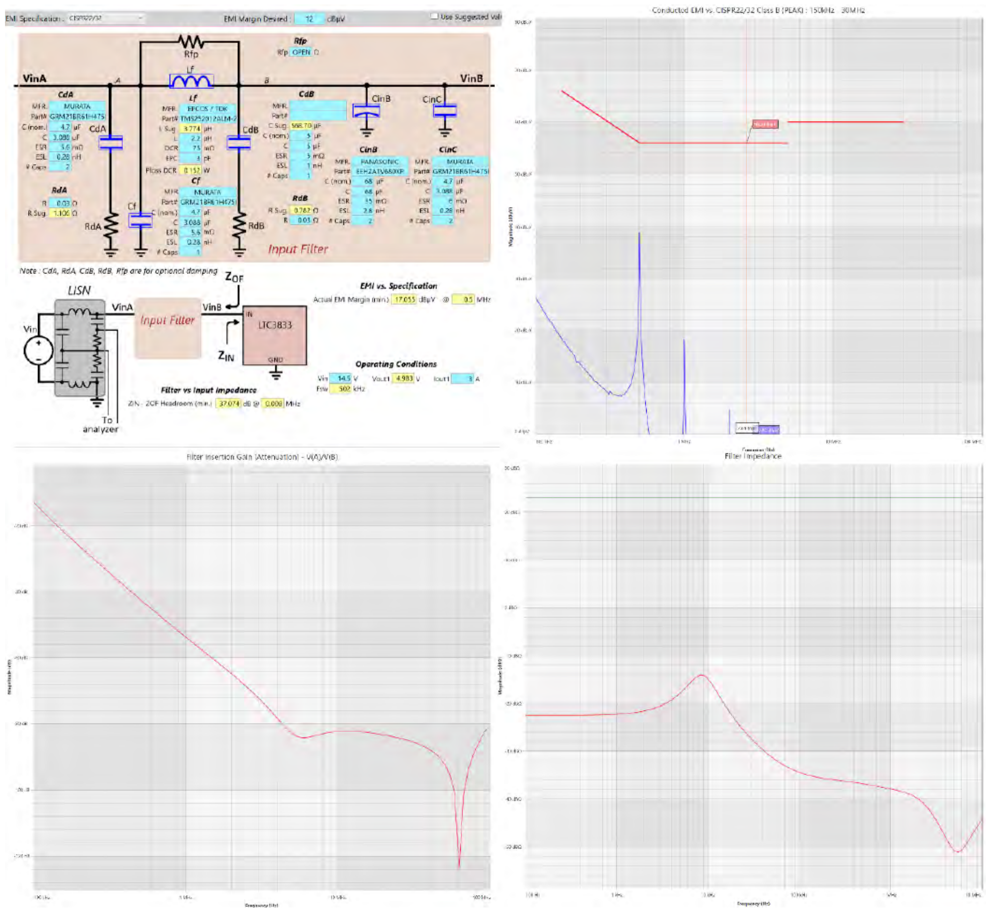

Figure 3.10: Simulation result of the input EMI filter design

Digital Signal Processor (DSP) The Texas Instruments TMS320F28379D microcontroller serves as the DSP core, providing high-performance computation for real-time control. It interfaces with the gate driver board, current sensors, and resolver through ADCs, SPI, and CAN communication protocols. The DSP executes control algorithms, including Space Vector Pulse Width Modulation (SVPWM), which offers superior DC bus utilization, reduced harmonic distortion, and improved efficiency compared to conventional sinusoidal PWM. The space vectors form a hexagonal structure in the α-β plane, as illustrated in Figure 3.11.

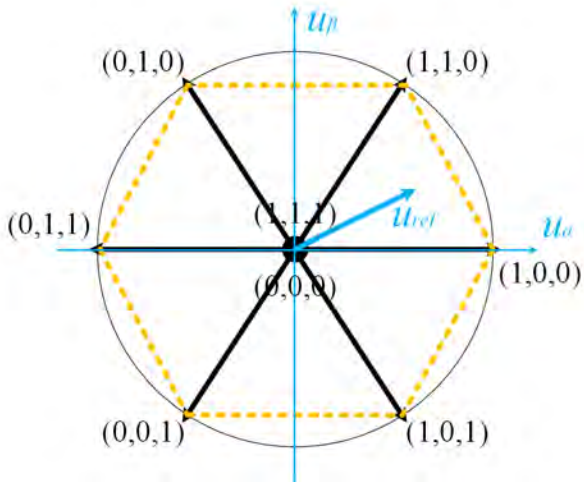

Figure 3.11: Space vector diagram for SVPWM modulation

The implementation of SVPWM involves four main steps: (1) calculating the reference voltage vector from the input voltage components, (2) determining the sector of the hexagon in which the reference vector lies, (3) computing the time intervals for applying adjacent active vectors and zero vectors, and (4) generating the corresponding switching signals for the inverter.

Encoder The resolver interface is implemented using the AD2S1210 resolver-to-digital converter, which offers a resolution range from 10 to 16 bits. This device excites the resolver through an integrated programmable sinusoidal oscillator and converts the sine and cosine feedback signals into a digital representation of rotor position and speed. The processed data is communicated to the DSP via an SPI interface, providing accurate position feedback for the control system [84].

Current Sensors Two types of current sensors are employed in the inverter for performance evaluation. The first is the Swoboda CSM510HP2x, an ultra-compact, galvanically isolated current sensor integrated into the gate driver board to achieve high power density [85]. The second is the LEM HAH3DR 900-S0D, a three-phase Hall-effect-based transducer added for comparative analysis of sensing performance, albeit at the expense of system power density[86].

Current Sensor Comparison Table 3.6 compares the two current-sensing approaches evaluated in this work. Values are taken from the respective manufacturer datasheets and product briefs.

Table 3.6: Comparison of Current Sensors Used in Inverter Prototypes

Attribute	Swoboda CSM510HP2x (CSM510HP2S / CSM510HP2D)	LEM HAH3DR 900-S0D
Sensing principle	Coreless Hall (dual differential Hall, TLE4973-based)	Open-loop Hall with magnetic core
Mechanical integration	Fits HybridPACK™ Drive G2 cavity (module-integrated)	Busbar-mounted module with cable connector (panel/chassis mount)
Supply / output	5 V; single-ended or differential analog output	4.75–5.25 V; ratiometric 0–5 V analog output
Current range (typ.)	Peak up to ±1600 A (application-dependent)	Nominal up to ±900 A (variant-dependent)
Bandwidth (typ.)	> 120 kHz	DC–40 kHz (typ.)
Response time / OC flag	OC indication $< 1.7\,\mu$s; high-speed analog chain	$\sim 6\,\mu$s typical analog response
Total error / linearity	Total error $< 2\%$ (module/IC), high linearity	Accuracy $\sim \pm 3.75\%$, linearity $\sim \pm 1\%$ (typ.)
Isolation	Galvanically isolated (coreless), ASIL–B (SEooC) capable	Galvanically isolated, automotive-grade family
Power-density impact	Minimal added volume; inside power module	Larger footprint; external to power module
Best fit	Highest power density, high f_{sw} / wide HF content, direct HybridPACK integration	Retrofit / busbar installs, tri-phase packaging options, ease of wiring and service

4

Experimental Results

This chapter presents the experimental validation of the proposed system. Two primary evaluations were conducted:

1. Functional test of the control board in open-loop operation with an RL load.
2. Thermal performance assessment of the DC-link for Case I and Case II under high-current sinusoidal excitation performed by Rogers Corporation.

4.1 Experimental Circuits

This section describes the test benches and measurement setups used in the study. It first outlines the three-phase open-loop test configuration and the associated modulation, sensing, and data-acquisition arrangement employed to evaluate open-loop operation and performance with an RL load. It then details the capacitor thermal test setup, including the resonant high-current source, excitation levels, cooling configurations, and instrumentation used to map temperatures on the busbar, capacitor surfaces, and inter-capacitor regions, which form the basis for the subsequent thermal performance evaluation.

4.1.1 Three-phase open-loop operation

To validate the functionality of the control board, gate driver, and SVPWM implementation, open-loop tests were conducted using an RL load to emulate inverter operating conditions. The primary objectives were to verify PWM signal integrity, evaluate current control response, and assess thermal and electrical stability under different DC-link voltages.

The test bench (Figure 4.1) consisted of a DC power supply, the control board interfaced with the HybridPack SiC module, and the RL load connected to the inverter output. Two DC-link voltage levels were applied: 100 V and 200 V, representing low- and medium-voltage operating points. The q-axis voltage reference was varied from 0 V to 30 V in incremental steps to observe the inverter's response under different modulation indices.

Key measurements included phase current waveforms and PWM switching patterns captured via a high-bandwidth oscilloscope. The DSP executed SVPWM at a switching frequency of 20 kHz, and the resulting line-to-line voltages were monitored to confirm correct space vector synthesis.

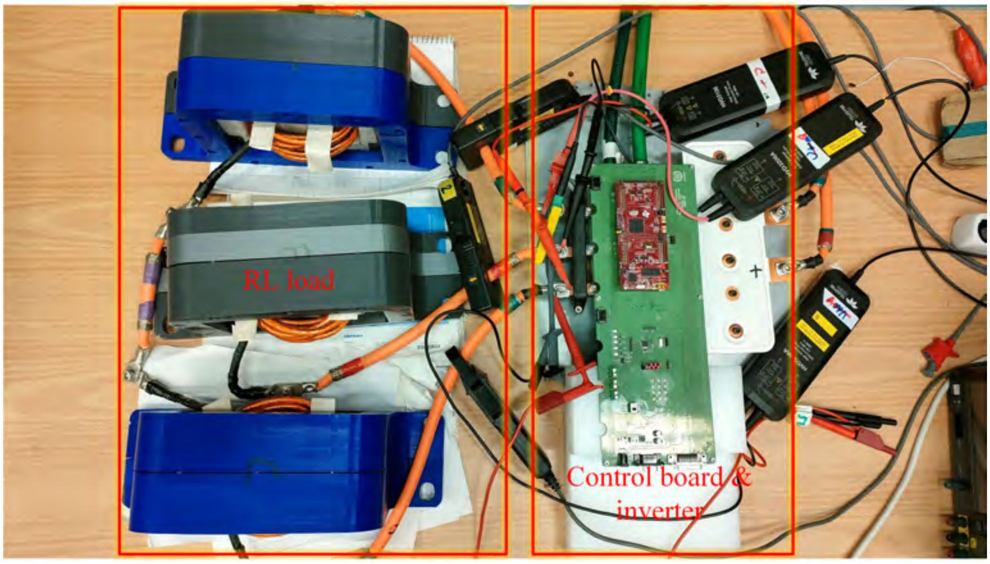

Figure 4.1: Test bench for three-phase open-loop operation

4.1.2 Open-Loop Operation Performance

Figures 4.2 and 4.3 illustrate the measured phase voltages and currents for different DC-link voltages and q-axis voltage references. The experimental results confirm the correct implementation of the SVPWM algorithm, demonstrating stable control performance across the tested operating range and compliance with expected modulation characteristics. At higher q-axis voltage references, the RL load draws larger current, which increases the di/dt in the power loop and exacerbates electromagnetic interference (EMI) arising from stray inductances (and associated parasitics). The resulting common- and differential-mode noise may couple into the control and sensing paths, perturbing the measured phase voltages and currents.

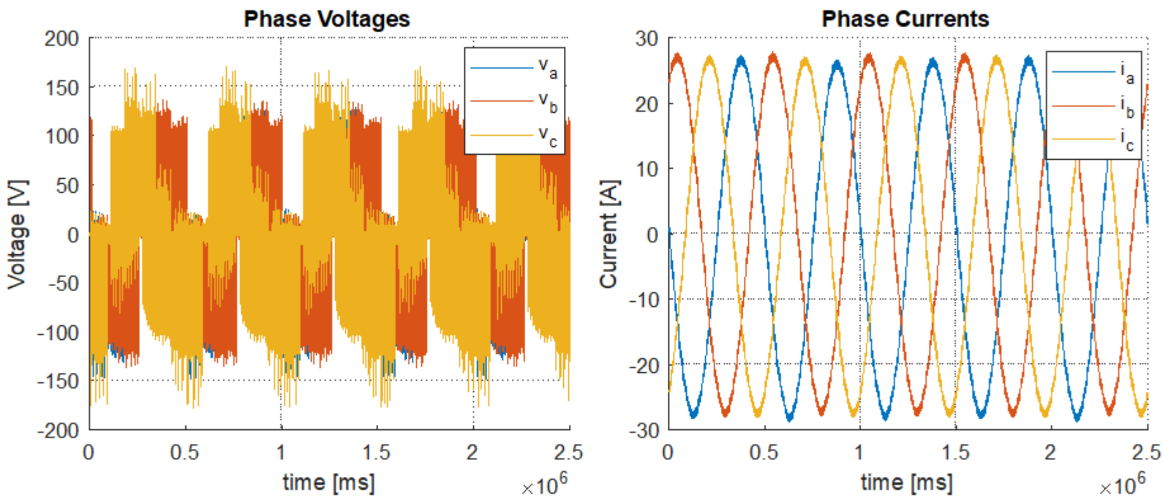

Figure 4.2: Phase voltages and currents with 100 V DC source and 1 V q-axis reference

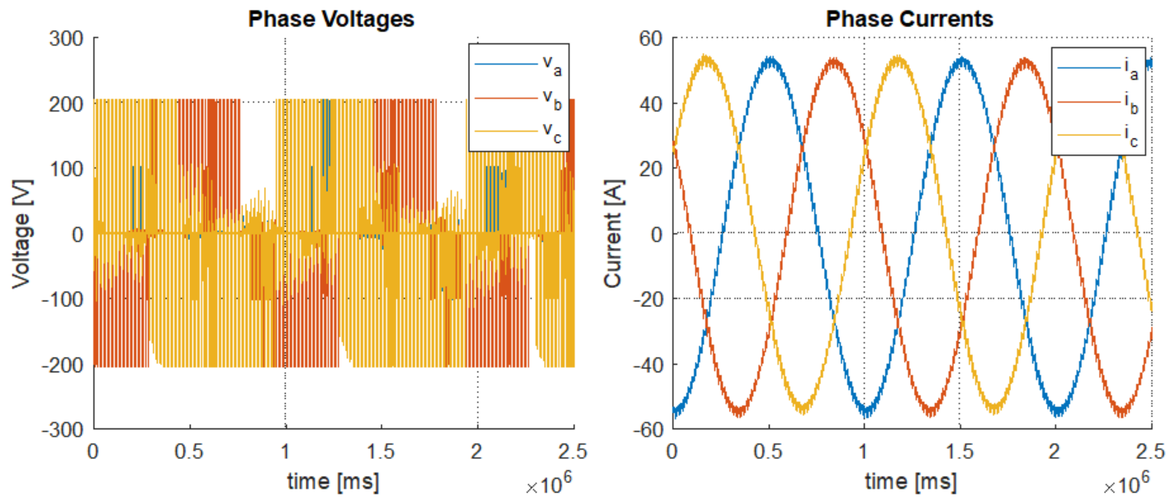

Figure 4.3: Phase voltages and currents with 200 V DC source and 0.2 V q-axis reference

4.1.3 Capacitor Thermal Test Setup

To evaluate the thermal performance of the proposed busbar concepts, a test rig was developed to replicate realistic operating conditions encountered in traction inverter applications. The setup excites the device under test (C_{DUT}) with a high-current sinusoidal signal, imposing both thermal and electrical stresses representative of real-world scenarios. The thermal evaluation was carried out in collaboration with Rogers Corporation as part of the Powerdrive project. The primary objective of these tests is to assess the thermal behavior of the DC-link under high ripple-current stress and to compare the effectiveness of the two mechanical layouts in dissipating heat.

The C_{DUT} is connected to a resonant current source designed to deliver large sinusoidal currents at low voltage. Two RMS current levels were applied: 156 A and 300 A, each at a frequency of 10 kHz and maintained for two hours. Both configurations were tested under two thermal boundary conditions: (i) with active liquid cooling and (ii) without cooling. This approach enables a comparative analysis of thermal dissipation efficiency and its implications for capacitor aging and reliability.

The excitation circuit, shown in Figure 4.4, applies a low-voltage, high-current sinusoidal signal to the busbar and capacitor assembly. The current source operates on the principle of parallel resonance, defined by the inductance L_p and capacitance C_p. The C_{DUT} is placed in series with the dominant resonant capacitor C_p, forming a resonant tank circuit. The total capacitance is given by:

$$\frac{1}{C_{\mathrm{total}}} = \frac{1}{C_p} + \frac{1}{C_{\mathrm{DUT}}}. \tag{4.1}$$

The resonant frequency is calculated as:

$$f_r = \frac{1}{2\pi\sqrt{L_p C_{\mathrm{DUT}}}}. \tag{4.2}$$

Depending on the value of C_{DUT} (ranging from 200 µF to ∞), the resonance frequency varies between 8.5 kHz and 10.5 kHz. At resonance, the system behaves as a purely resistive load, which is verified using an oscilloscope during low-amplitude tuning.

A Class-D amplifier drives the resonant system, amplifying the input from a function generator. The system's quality factor Q is approximately 30, meaning that for a peak 400 A resonance current, the amplifier supplies only about 13 A of input current. The active power delivered by the amplifier corresponds to the resistive losses in the system, primarily in the inductors and C_{DUT}. Losses in C_{DUT} include resistive heating in the busbar and capacitors, which are monitored to assess thermal performance. The C_{DUT} is connected via thick litz wires to minimize parasitic losses and is mounted on a heatsink to limit hotspot temperatures.
Figure 4.5 shows the overall experimental setup. Figures 4.6 and 4.7 present the measured waveforms for the 156 A_{rms} and 300 A_{rms} test conditions, respectively. Finally, Figures 4.8 and 4.9 illustrate the laboratory setups for Case I and Case II, corresponding to the upper- and lower-mounted DC-link capacitor configurations.

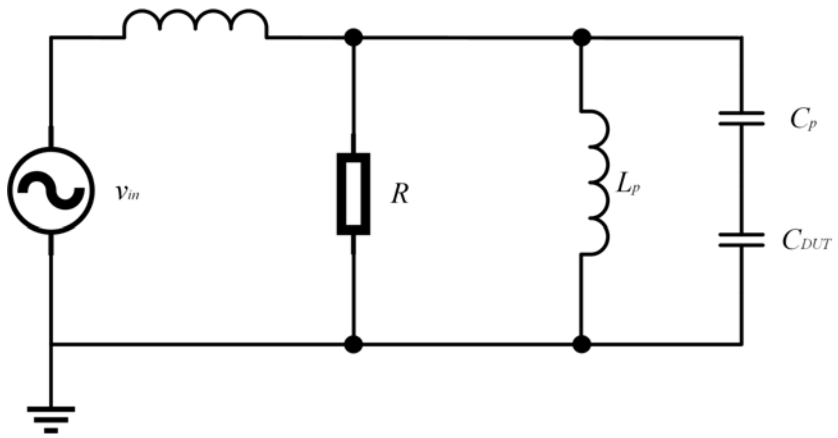

Figure 4.4: Test circuit: 0–400 A parallel resonant current source for busbar load (C_{DUT})

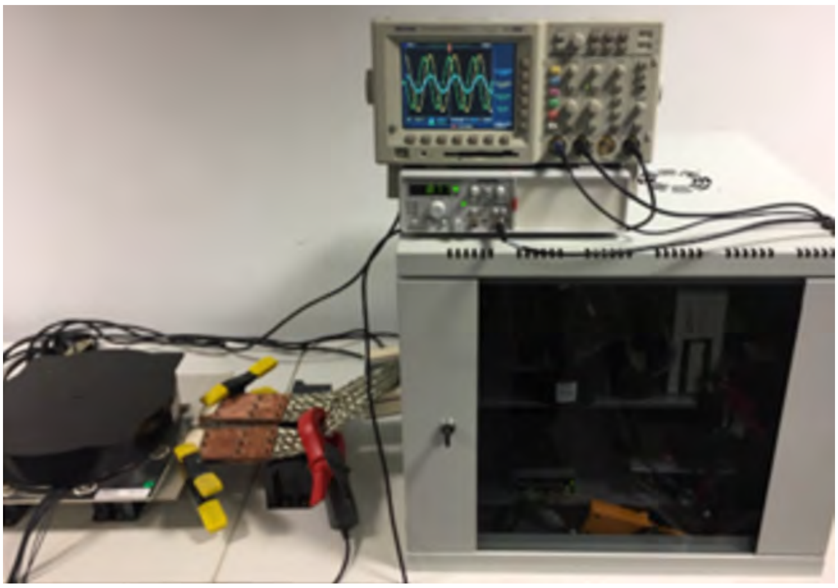

Figure 4.5: Experimental setup: 10 kHz system with connections to C_{DUT} performed by Rogers corporation

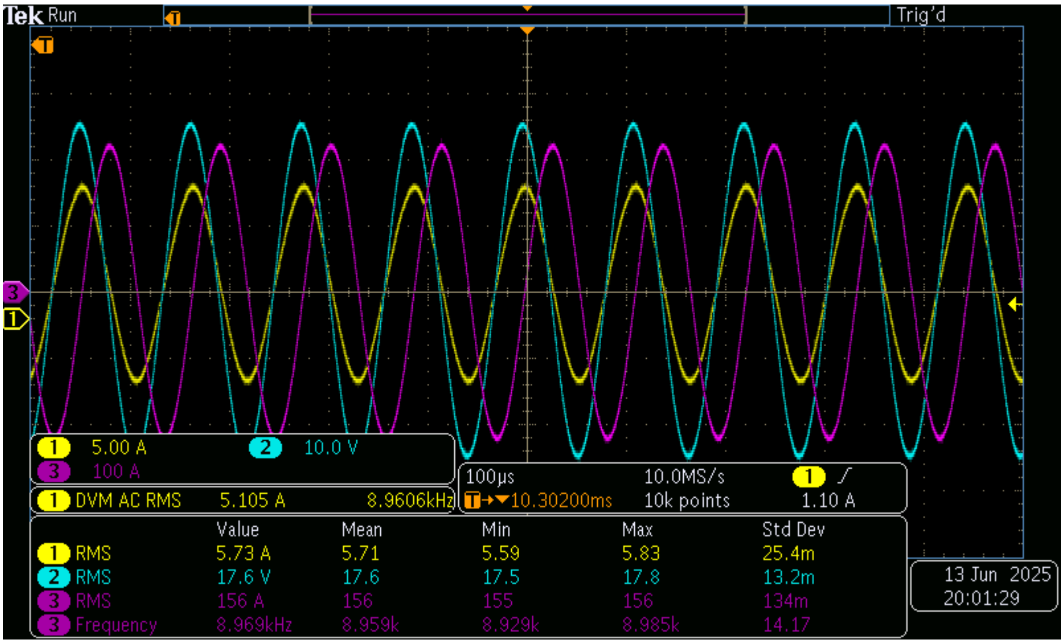

Figure 4.6: Measured waveform of the 156 A_{rms} sinusoidal test signal

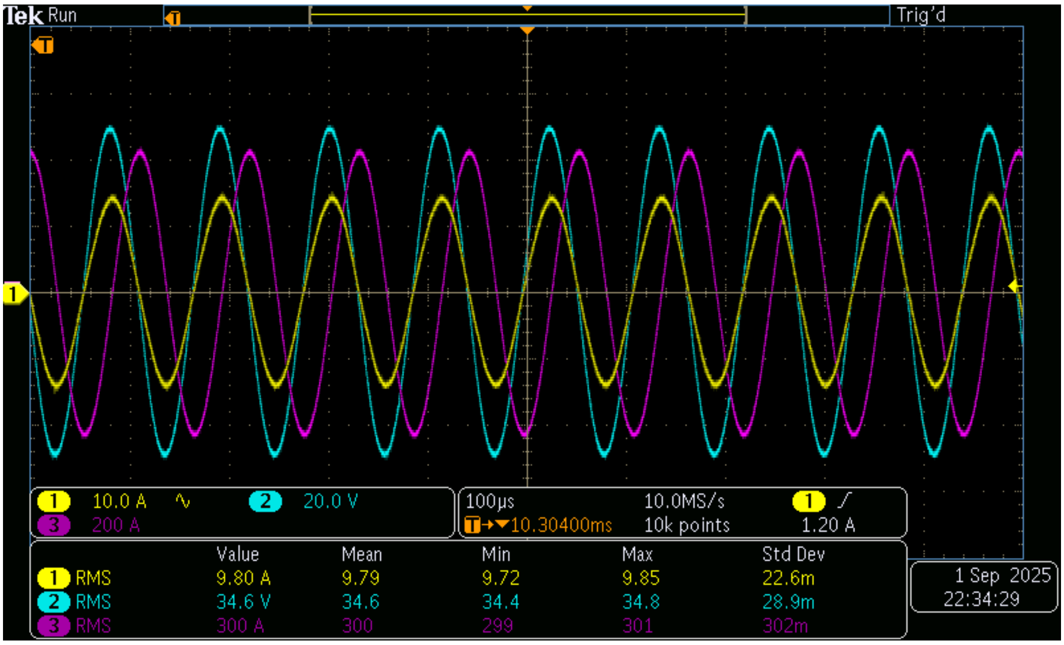

Figure 4.7: Measured waveform of the 300 A_{rms} sinusoidal test signal

Under high ripple-current excitation, the dominant heat generation in metallized polypropylene film capacitors arises from the frequency- and temperature-dependent equivalent series resistance (ESR). The average power loss can be expressed as 2.45 where the first term accounts for foil and termination losses (including skin and proximity effects), and the second term represents dielectric losses. The resulting hot-spot temperature rise is governed by the thermal path from the capacitor core to the heat sink as expressed in 2.46
Elevated temperatures accelerate several degradation mechanisms: (i) *ohmic aging* due to ESR growth from termination stress and localized heating; (ii) *self-healing erosion* of metallization, reducing electrode area and increasing ESR; (iii) *partial discharge (PD)*

at edges or voids under high dv/dt stress; and (iv) *thermo-mechanical fatigue* from load cycling, causing microcracks and contact resistance increase. These processes typically follow Arrhenius-type acceleration, where a 10°C rise approximately doubles the reaction rate. Therefore, minimizing ΔT_{hot} and ensuring uniform temperature distribution are critical for long-term reliability.

Case I introduces an intermediate thermal interface (busbar) between the capacitors and the housing, which may increase thermal resistance but improve lateral heat spreading. Case II provides a direct thermal path to the housing, reducing thermal resistance and expected hot-spot temperatures, particularly under no-coolant conditions.

Table 4.1 summarizes the electrical excitation, environmental conditions, configurations, and measured quantities used for the comparative thermal evaluation. Each operating point was held for 2 hours. The current source is the 0–400 A parallel resonant stage in Fig. 4.4; the overall bench is shown in Fig. 4.5. Waveforms for the two current levels are provided in Figs. 4.6 and 4.7. Case I and Case II setups are shown in Figs. 4.8 and 4.9, respectively.

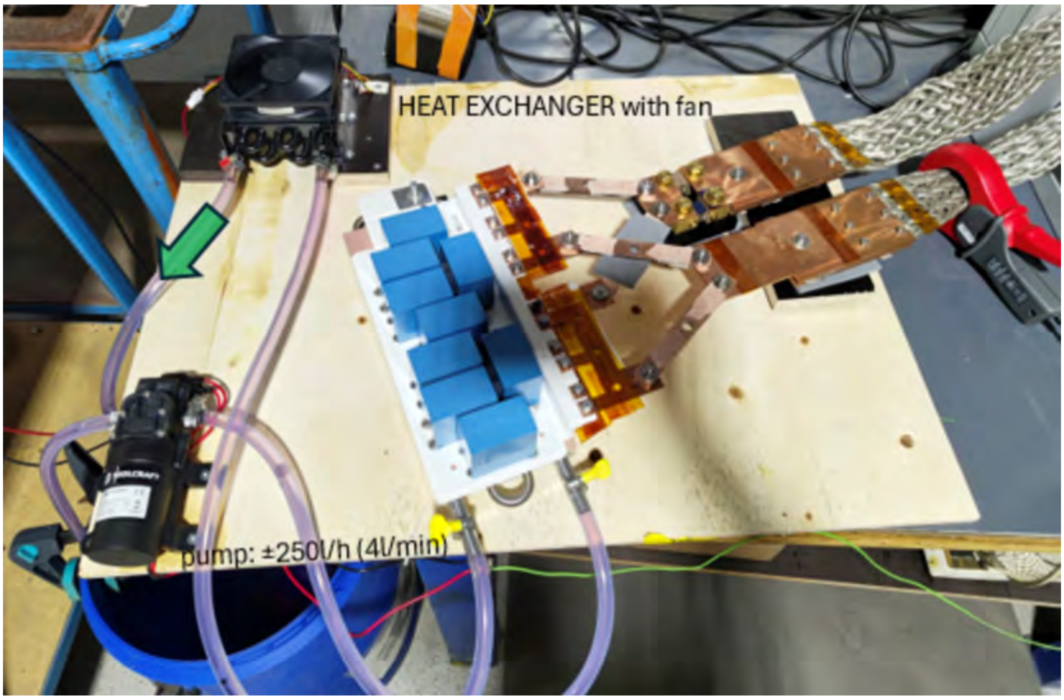

Figure 4.8: Experimental setup for Case I: capacitors mounted on the upper side

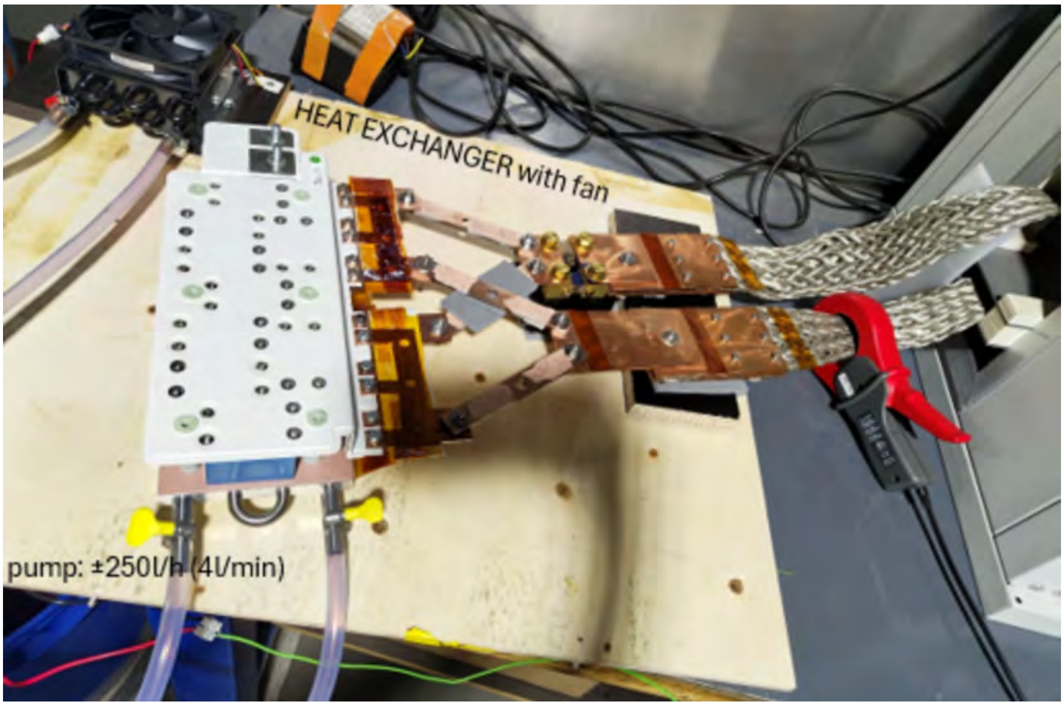

Figure 4.9: Experimental setup for Case II: capacitors mounted on the lower side

Table 4.1: Thermal test conditions and parameters for DC-link evaluation

Parameter	**Symbol / Unit**	**Value / Setting**	**Notes**
Waveform / frequency	f / kHz	10	Sinusoidal current injection (parallel resonant source)
Ripple current level 1 (RMS)	I_1 / A	156	Held 2 h per cooling condition (Case I and Case II)
Ripple current level 2 (RMS)	I_2 / A	300	Held 2 h per cooling condition (Case I and Case II)
Duration per operating point	t_{hold} / h	2	Temperature monitored to steady-state plateaus
Cooling condition	–	On / Off	Water–glycol loop when On; identical ambient for Off
Coolant setpoints (when On)	T_{in}, $\dot{m}$	Recorded per run	Inlet temperature and flow logged; used for normalization
Ambient temperature	T_a / °C	Recorded per run	Measured near DC-link; used for reporting ΔT
DC-link configuration	–	Case I / Case II	Case I: caps above busbar; Case II: caps direct to housing
Temperature sensing	–	IR camera + TCs	Hot-spot, average, and gradient across bank (define TC map)
Electrical characterization	–	ESR(f, T), C	Pre-/post-stress LCR at defined f and V_{ac}
Acceptance indicators	–	ΔT_{hot}, ΔESR, $\Delta C/C_0$	Compared across cases/cooling at each I

4.1.4 Thermal Performance Evaluation

The thermal performance of the DC-link was assessed by injecting high-amplitude sinusoidal currents into the busbar-capacitor assembly using the resonant test setup described in Chapter 4. Two configurations were tested:

- **Case I:** Capacitors mounted above the busbar.
- **Case II:** Capacitors mounted directly on the housing.

Each case was evaluated under two RMS ripple current levels (156 A and 300 A) and two cooling conditions (with and without liquid cooling). The objective was to quantify the impact of mechanical layout and cooling on hot-spot temperature rise, thermal gradients, and overall thermal resistance. The experimental tests were conducted at an ambient temperature of 20 °C.

Case I Results

Figures 4.10–4.13 present thermal maps for Case I under the four operating conditions. The highest capacitor surface temperatures recorded at 156 A_{rms} were 47.56 °C with cooling *off* and 43.10 °C with cooling *on*; at 300 A_{rms}, the corresponding values were 78.70 °C and 71.00 °C. These peak values indicate a reduction of approximately 9.4% at 156 A_{rms} and 9.8% at 300 A_{rms} in maximum capacitor surface temperature with liquid cooling.

Figure 4.14 summarizes the temperature-rise (ΔT) distributions by location. At 156 A_{rms}, the busbar ΔT decreased from approximately 16 °C (cooling off) to 6 °C (cooling on), while the capacitor surface dropped from 24 °C to 19 °C and the inter-capacitor region from 29 °C to 23 °C. At 300 A_{rms}, the corresponding values were 36 °C vs. 12 °C (busbar), 55 °C vs. 45 °C (capacitor), and 67 °C vs. 55 °C (inter-capacitor). In relative terms, liquid cooling reduces the busbar ΔT by approximately 62.5% at 156 A_{rms} and 66.7% at 300 A_{rms}, whereas reductions at the capacitor surface and inter-capacitor region are more modest (about 18–21%), indicating that the dominant thermal bottleneck for the capacitor bank lies within the internal conduction path and interfaces.

Table 4.2: Case I: Temperature rise (ΔT) under different conditions

Ripple Current	Cooling	Busbar (°C)	Capacitor (°C)	Inter-Capacitor (°C)
156 A_{rms}	Off	16	24	29
	On	6	19	23
300 A_{rms}	Off	36	55	67
	On	12	45	55

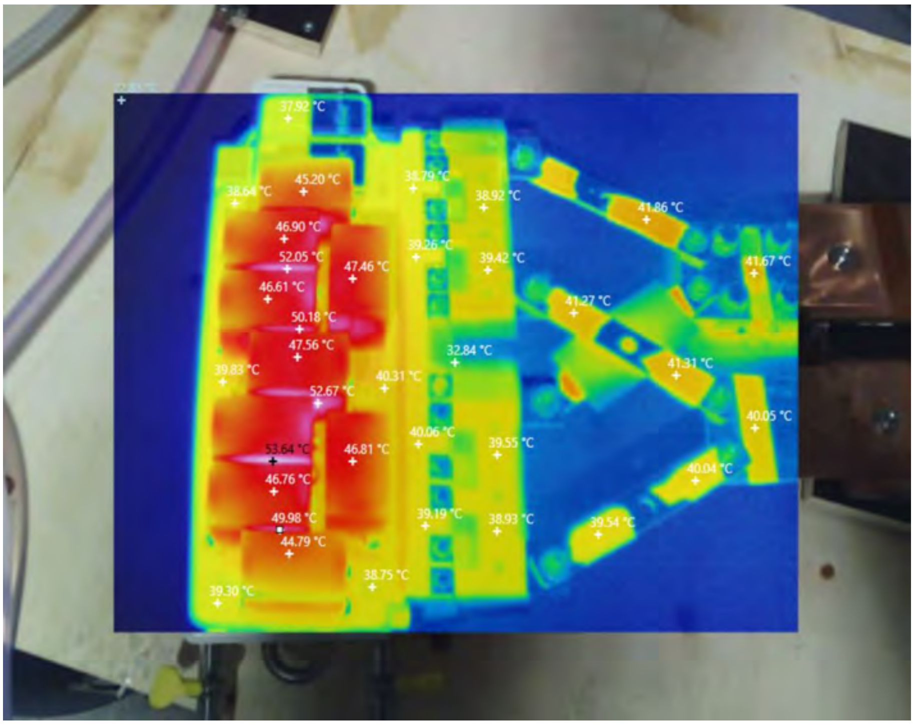

Figure 4.10: Case I: 156 A_{rms}, no cooling.

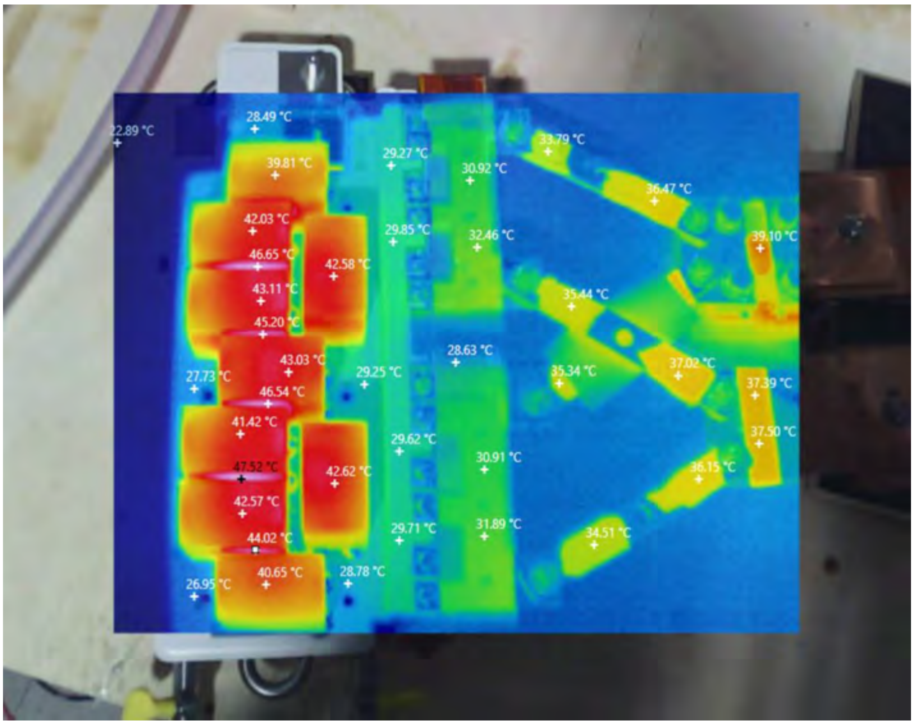

Figure 4.11: Case I: 156 A_{rms}, with cooling.

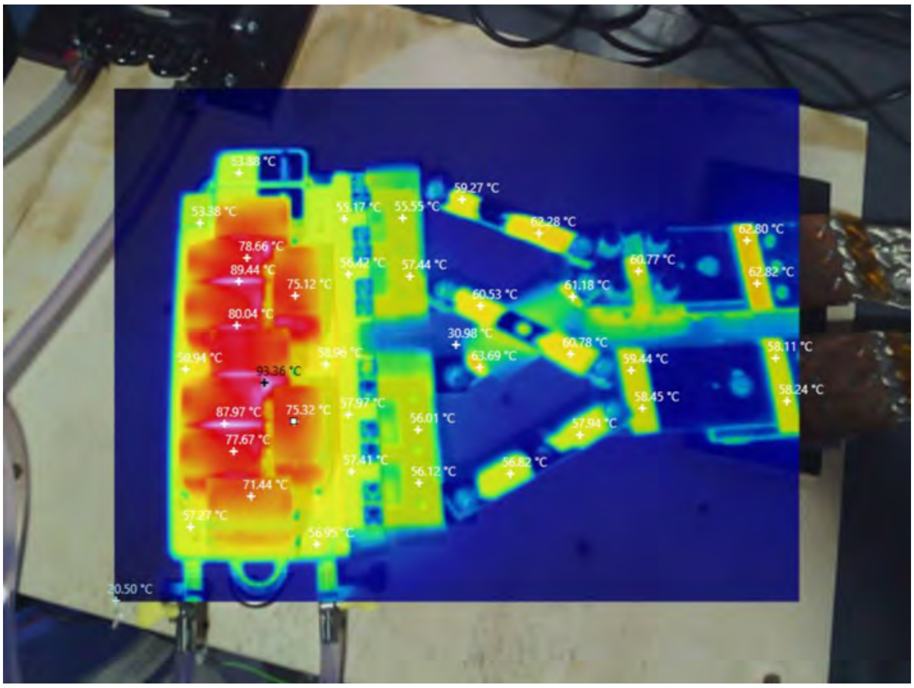

Figure 4.12: Case I: 300 A_{rms}, no cooling.

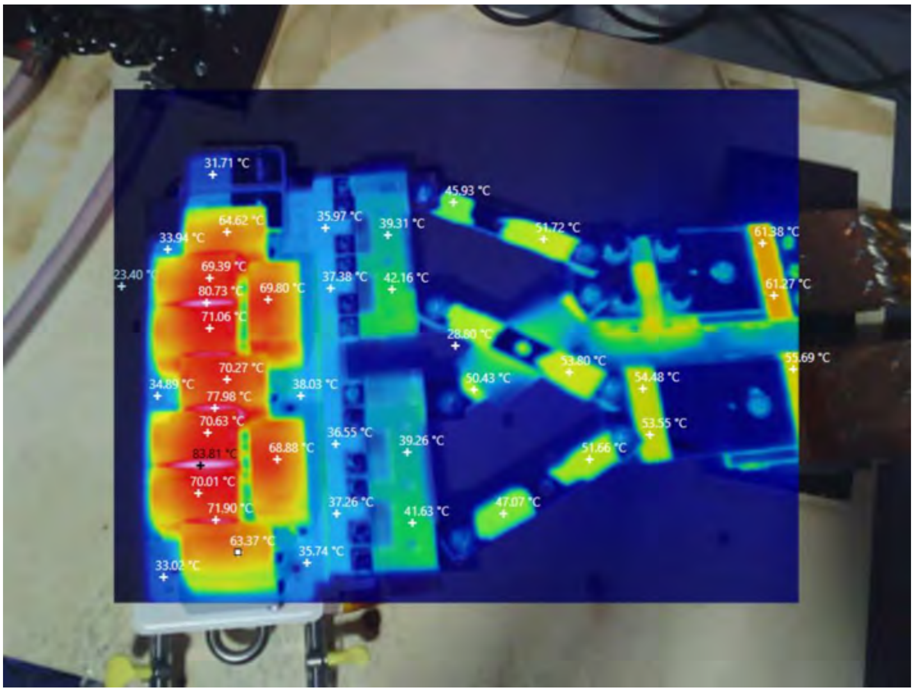

Figure 4.13: Case I: 300 A_{rms}, with cooling.

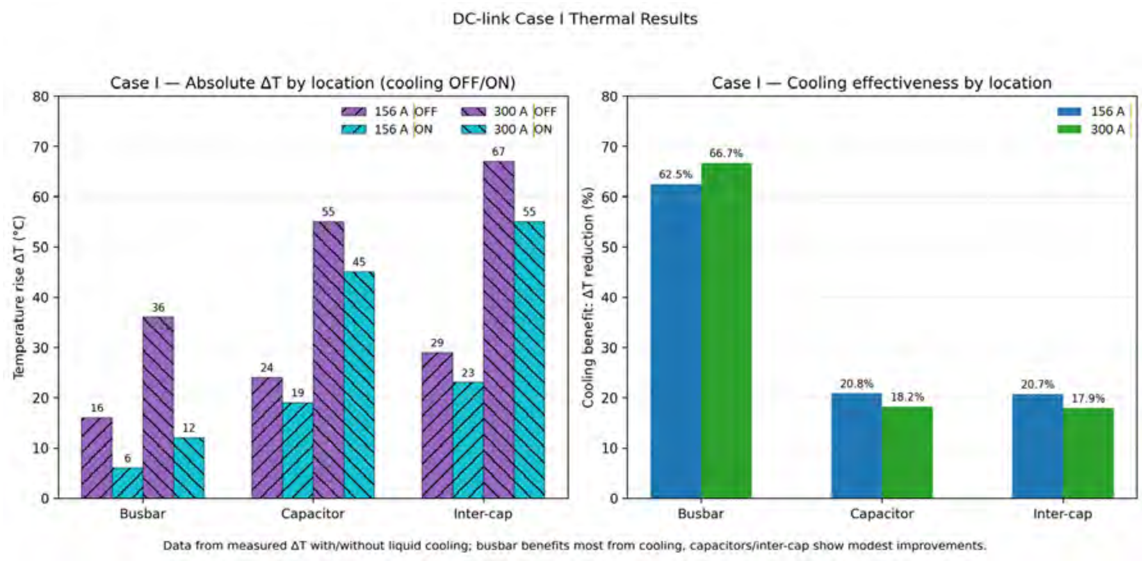

Figure 4.14: Case I thermal results at 156 A_{rms} and 300 A_{rms}. **Left:** absolute temperature rise (ΔT) by location with cooling OFF vs. ON. **Right:** cooling effectiveness as percent ΔT reduction.

Case II Results

Figures 4.15–4.18 present thermal maps for Case II under the four operating conditions. The highest capacitor surface temperatures recorded at 156 A_{rms} were 47.52 °C with cooling *off* and 45.28 °C with cooling *on*; at 300 A_{rms}, the corresponding values were 80.37 °C and 74.19 °C. These peak values indicate reductions of approximately 4.7% at 156 A_{rms} and 7.7% at 300 A_{rms} in maximum capacitor surface temperature with liquid cooling.

Figure 4.19 summarizes the ΔT distributions by location. At 156 A_{rms}, the busbar ΔT was 19 °C without cooling and 16 °C with cooling. On the capacitor surface, ΔT decreased from 26 °C to 23 °C, while the inter-capacitor region dropped from 36 °C to 30 °C. At 300 A_{rms}, the corresponding values were 41 °C vs. 37 °C (busbar), 55 °C vs. 50 °C (capacitor), and 68 °C vs. 65 °C (inter-capacitor). Compared to Case I, Case II exhibits slightly higher busbar temperatures and similar or marginally higher capacitor temperatures, indicating that direct housing contact improves heat spreading but does not fully eliminate localized hot spots without enhanced interfaces and coolant proximity.

Table 4.3: Case II: Temperature rise (ΔT) under different conditions

Ripple Current	**Cooling**	**Busbar (°C)**	**Capacitor (°C)**	**Inter-Capacitor (°C)**
156 A_{rms}	Off	19	26	36
	On	16	23	30
300 A_{rms}	Off	41	55	68
	On	37	50	65

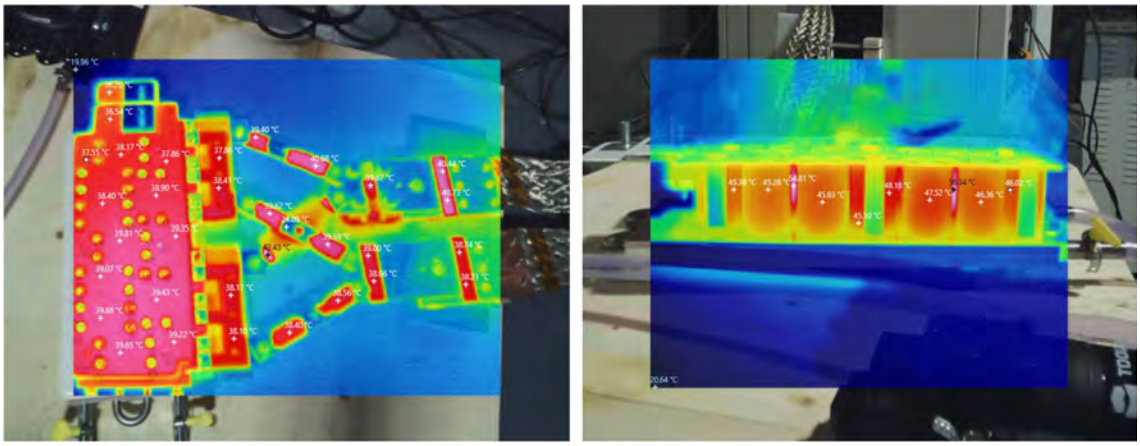

Figure 4.15: Case II: 156 A_{rms}, no cooling.

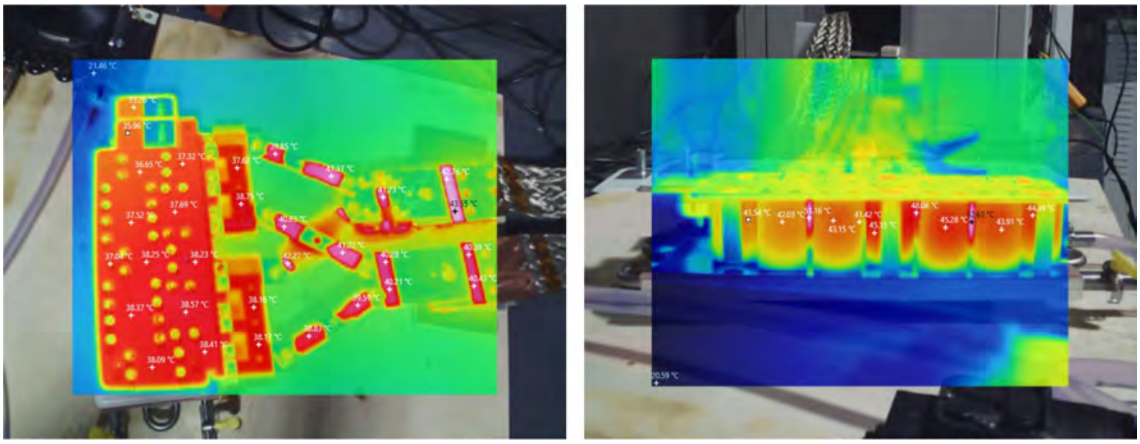

Figure 4.16: Case II: 156 A_{rms}, with cooling.

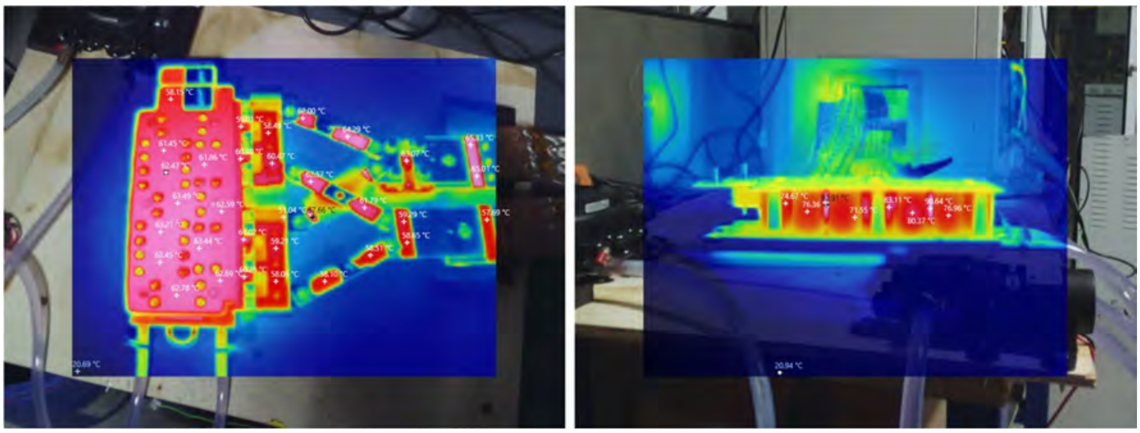

Figure 4.17: Case II: 300 A_{rms}, no cooling.

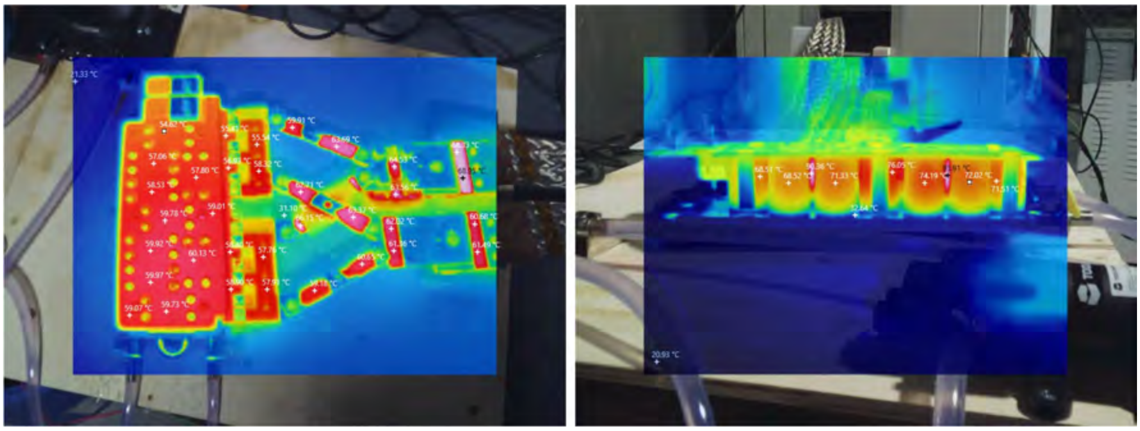

Figure 4.18: Case II: 300 A_{rms}, with cooling.

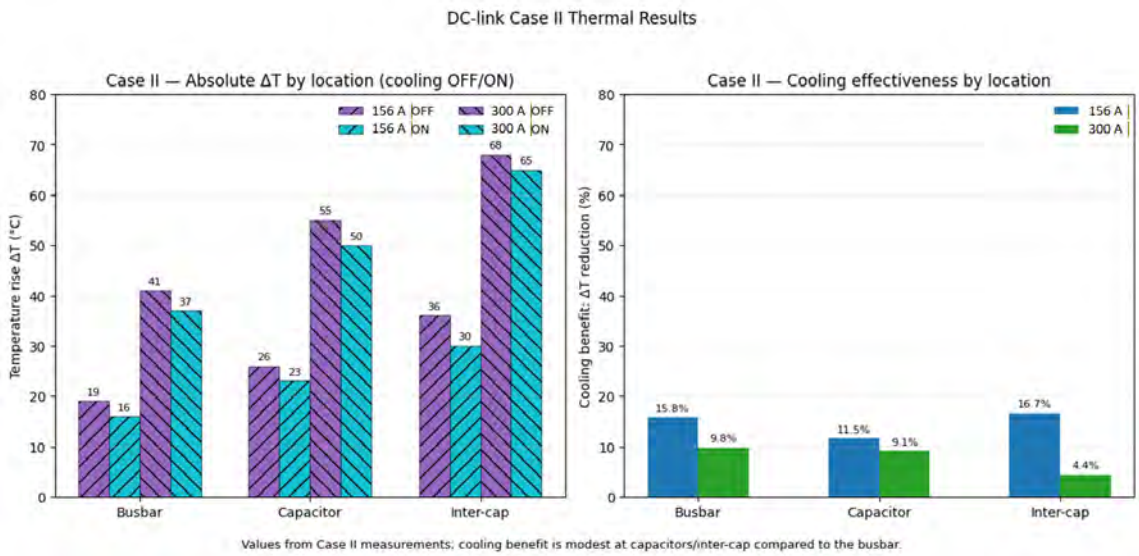

Figure 4.19: Case II thermal results at 156 A_{rms} and 300 A_{rms}. **Left:** absolute temperature rise (ΔT) by location with cooling OFF/ON. **Right:** cooling effectiveness as percent ΔT reduction.

Results and Discussion

Both configurations benefit from liquid cooling, but the *magnitude* of improvement and the *location* of benefit differ. For the busbar, Case I achieves a ΔT reduction of approximately 62.5% at 156 A_{rms} and 66.7% at 300 A_{rms}, compared to 15.8% and 9.8% for Case II. In contrast, the capacitor surface and inter-capacitor regions exhibit only modest improvements (Case I: ∼18–21%; Case II: ∼9–17%), indicating that internal capacitor thermal paths dominate hot-spot behavior regardless of external cooling. Peak temperatures remain highest in the inter-capacitor region at elevated ripple currents for both cases, underscoring the need for improved thermal interfaces and direct heat extraction from the capacitor core rather than relying solely on housing contact or bulk cooling.

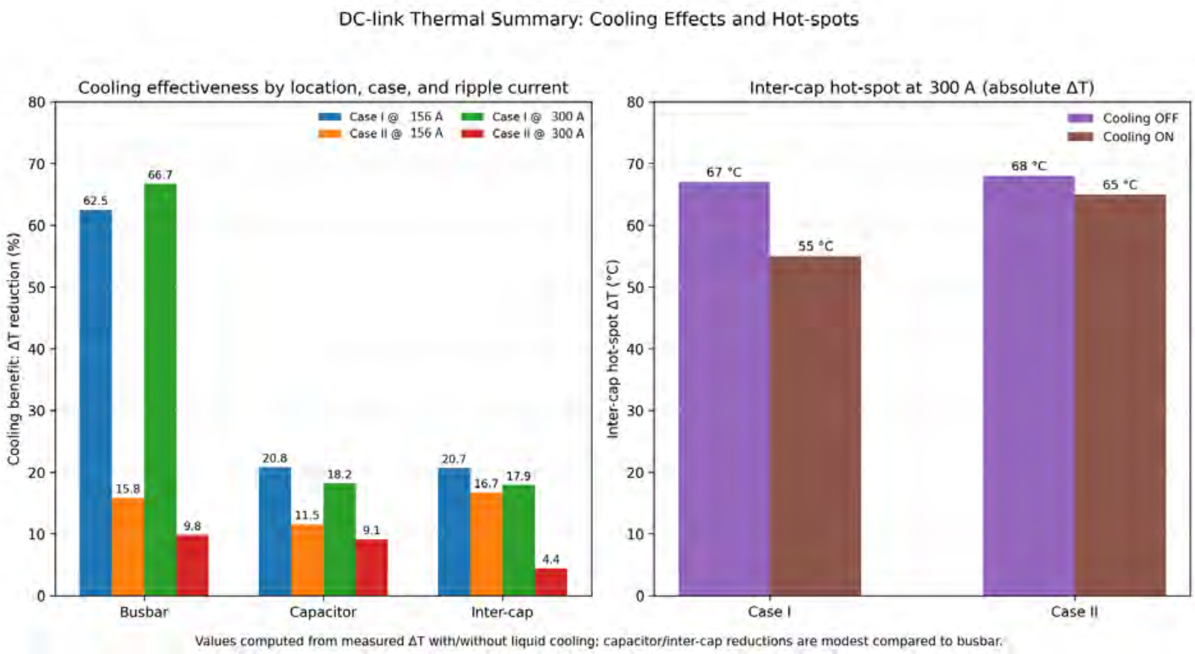

Figure 4.20: DC-link thermal summary under liquid cooling. **Left:** Cooling benefit (ΔT reduction, %) by location for Case I and Case II at 156 A_{rms} and 300 A_{rms}. Busbar gains dominate, especially in Case I. Capacitor and inter-capacitor regions show modest reductions, indicating internal thermal paths limit hot-spot relief. **Right:** Absolute inter-cap hot-spots at 300 A_{rms} (OFF/ON). Case I: 67/55 °C; Case II: 68/65 °C.

4.1.5 Capacitor Lifetime Analysis

To estimate the capacitor lifetime, a simulation model incorporating the drive profile was developed. The model included a vehicle dynamics model, a three-phase machine model, an analytical inverter model, and a capacitor current model.

Capacitor stress analysis based on the drive cycle

The machine data are presented in Table 4.4. The electric machine is represented in the DQ reference frame, where the d- and q-axis voltages are calculated as:

$$u_d = R_s i_d + L_d \frac{di_d}{dt} - \omega_e \psi_q \tag{4.3}$$

$$u_q = R_s i_q + L_q \frac{di_q}{dt} - \omega_e \psi_d \tag{4.4}$$

where R_s is the stator resistance, while u, i, L, ω, and ψ denote the voltages, currents, incremental inductance, angular frequency, and flux linkage, respectively. The electromagnetic torque is expressed as

$$t_e = \frac{3}{2} p(\psi_d i_q - \psi_q i_d) \tag{4.5}$$

where p is the number of pole pairs.
The phase current RMS, modulation index, and power factor for each operating point in the torque-speed plane can be calculated by using the reference voltages and current as follows

$$I = \frac{i_{d,\mathrm{ref}}^2 + i_{q,\mathrm{ref}}^2}{2} \tag{4.6}$$

$$M = \frac{u_{d,\mathrm{ref}}^2 + u_{q,\mathrm{ref}}^2}{U_{DC}^2/\sqrt{3}} \tag{4.7}$$

$$\cos\phi = \frac{(u_{d,\mathrm{ref}} i_{d,\mathrm{ref}} + u_{q,\mathrm{ref}} i_{q,\mathrm{ref}})}{\sqrt{u_{d,\mathrm{ref}}^2 + u_{q,\mathrm{ref}}^2} \cdot \sqrt{i_{d,\mathrm{ref}}^2 + i_{q,\mathrm{ref}}^2}} \tag{4.8}$$

A drive cycle analysis is employed to estimate capacitor stress under real-world conditions. The simplified system model integrates the vehicle dynamics, transmission model, electric machine maps, and capacitor current estimation. The traction force is computed as:

$$F_t = m_v g C_r + \frac{1}{2} \rho C_d v^2 A + m_v \frac{dv}{dt} \tag{4.9}$$

where m_v is the vehicle mass, g is the gravitational acceleration, ρ is the air density, C_d is drag coefficient, v is speed, A is the frontal area.
The electric HDT truck is modeled in the simulation, the vehicle parameters are presented in Table 3.1. The electric machine torque and rotor speed are determined by:

$$T_m = \frac{F_t r_w}{k_g} \tag{4.10}$$

$$\Omega_e = \frac{v}{r_w k_g} \tag{4.11}$$

where r_w is wheel radius and k_g is the transmission ratio.

The electric machine model is a look-up table of reference currents and voltages. Then, the phase current, modulation index, and power factor are calculated using equation (4.6)–(4.8). The capacitor current is then estimated using equation (2.35). The HHDDT Cruise cycle is used to simulate electric HDT.

The simulation diagram is shown in Figure 4.21 and the Simulink model is shown in Figure 4.22.

The HHDDT cruise cycle simulation results are presented in Figure 3.2, and the capacitor RMS current stress during a load cycle for the electric HDT is shown in Figure 4.23.

The capacitor RMS current stress is then used to calculate capacitor power loss using equation (2.45).

Table 4.4: Key parameters of the Traction Motors

Parameters	Value	Unit
Torque	600	Nm
Power	250	kW
DC voltage	800	V
Peak current	335	A

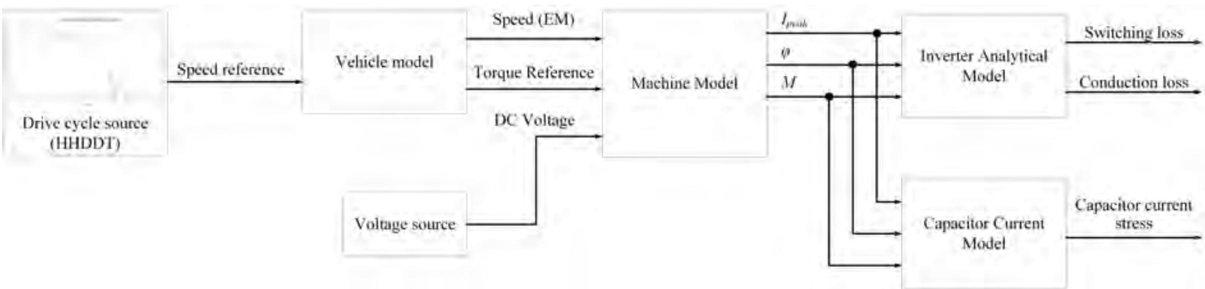

Figure 4.21: Simulation diagram for lifetime estimation under the HHDDT drive cycle.

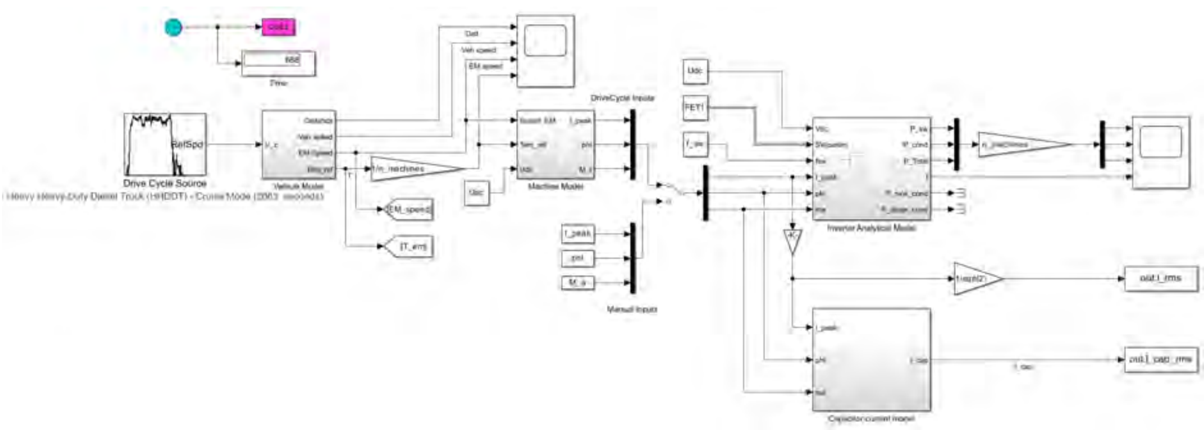

Figure 4.22: Simulation model in MATLAB/Simulink.

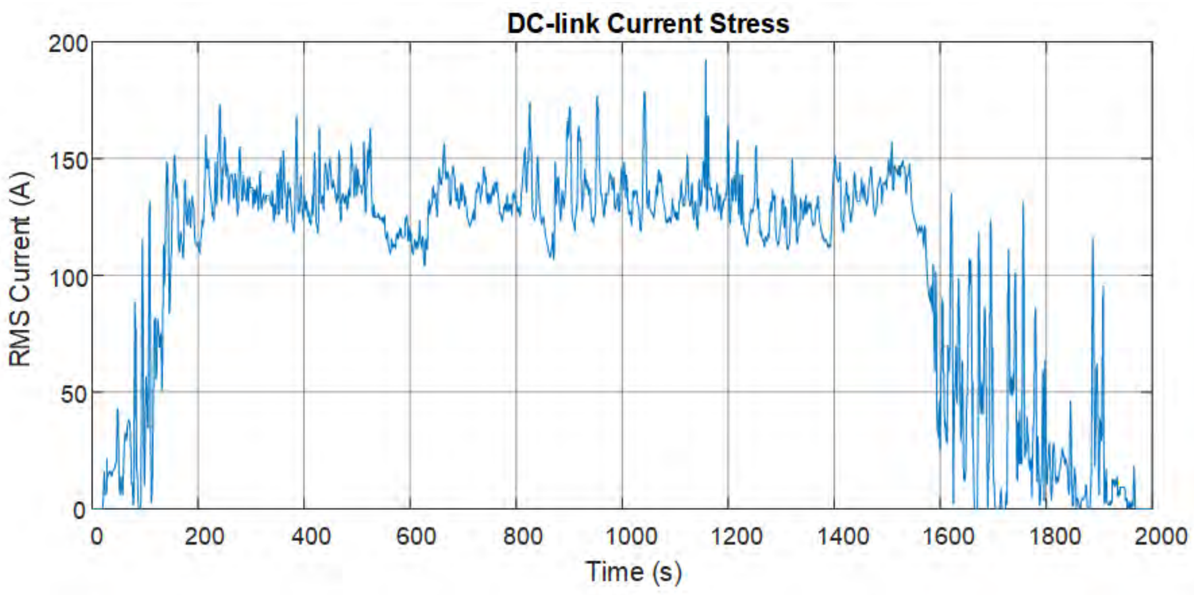

Figure 4.23: DC-link current profile from the HHDDT drive cycle simulation.

Lifetime evaluation of the DC-Link design

In this work, the lifetime model provided by the manufacturer in the datasheet is used for lifetime estimation. The baseline lifetime was first estimated using the lifetime expectancy curve provided in the datasheet of the B32778Z9506K000 film capacitor. Figure 4.24 illustrates the manufacturer-specified relationship between operating temperature and expected lifetime. The normalized voltage stress for this study is expressed as

$$n_V = \frac{V_{DC}}{V_{\text{rated}}} \approx 0.9 \tag{4.12}$$

where V_{DC} is the DC-link voltage, and V_{rated} is the rated voltage of the capacitor. The figure shows that the lifetime is sensitive to hot-spot temperature and voltage stress. The hotspot (T_{HS}) temperature can be estimated by using equation (2.47).
The lifetime model shown in Figure 4.24 provides the number of hours the capacitor can operate before being considered failed as a function of hot-spot temperature and voltage stress.
This lifetime model is implemented as a look-up table map in simulations and combined with the presented drive cycle. Then, the lifetime at each operating point can be calculated

$$L_h = f(T_{HS}, n_V) \tag{4.13}$$

Where L_h is lifetime in hours, f is an interpolation function. The total damage D can be calculated as

$$D = \frac{T_s}{3600 \times L_h} \tag{4.14}$$

Where T_s is the simulation time step in *second*. The remaining useful lifetime (T_{RUL}) can then be calculated by accumulation of the damage as normalizing for the entire drive cycle as follows

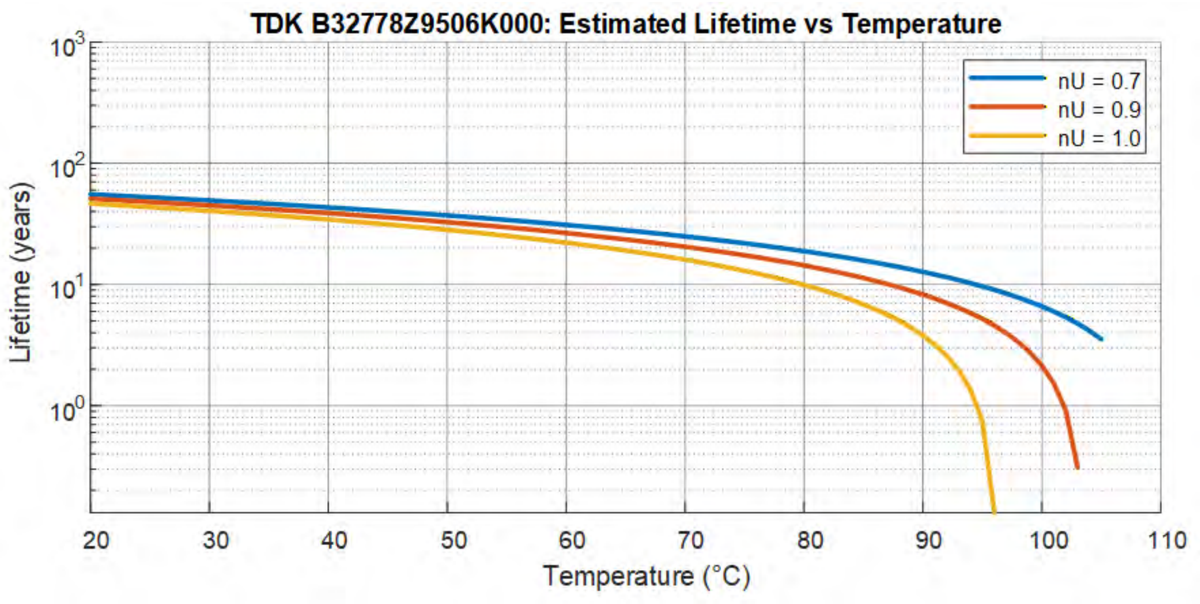

Figure 4.24: Estimated lifetime versus temperature based on the capacitor datasheet.

$$T_{RUL} = \frac{T_{\text{cycle}}}{3600 \times \sum_{i=1}^{n} D_i} \tag{4.15}$$

Where T_{cycle} is the duration of the drive cycle in seconds.
The thermal resistance value derived from the 156 A_{rms} experimental case was adopted due to its similarity to the simulated current profile. According to automotive standards, maximum ambient temperatures typically range from 60 °C to 70°C [87], [88]. In this study, for Case 2: Cooling OFF, the resulting hot-spot temperature at 60°C exceeded the breakdown threshold, reaching approximately 102°C, which led to capacitor failure. Therefore, a maximum ambient temperature of 55°C was selected to provide a reasonable comparison range for lifetime analysis between the cases.
To evaluate sensitivity, the simulated ambient temperature was varied from 20°C to 55°C. The estimated lifetime at an ambient temperature of 55°C is presented in Table 4.5.

Table 4.5: Lifetime estimation from the HDDDT simulation at 55 °C ambient temperature.

Case	Water Cooling	Surface Temperature (°C)	Estimated Lifetime (Years)
Datasheet (Ideal)	-	-	24.8
I	Off	24	10
	On	19	13.1
II	Off	26	8.7
	On	23	10.6

Under ideal datasheet-based assumptions and an ambient temperature of 55°C, the calculated lifetime was approximately 24.8 years. However, simulation-based estimates using experimental thermal constraints ranged from 8.7 to 13.1 years, significantly lower

than the ideal case. This discrepancy originates from simplified assumptions in the ideal model, which neglect thermal bottlenecks and assume perfect heat dissipation. In contrast, experimental results capture real thermal limitations, leading to higher operating temperatures and accelerated aging. These findings underscore the importance of incorporating accurate thermal models and cooling system characteristics into lifetime prediction frameworks.
Figure 4.25 shows the capacitor temperature profiles over the HDDDT cycle at 55°C ambient. In the ideal case (Using datasheet parameters and assumed perfect cooling), temperatures were approximately 26% lower than Case I: Cooling ON, which was the best experimental scenario. The worst case (Case II: Cooling OFF) reached peak temperatures near 100°C, approaching the capacitor's limit of 105°C.

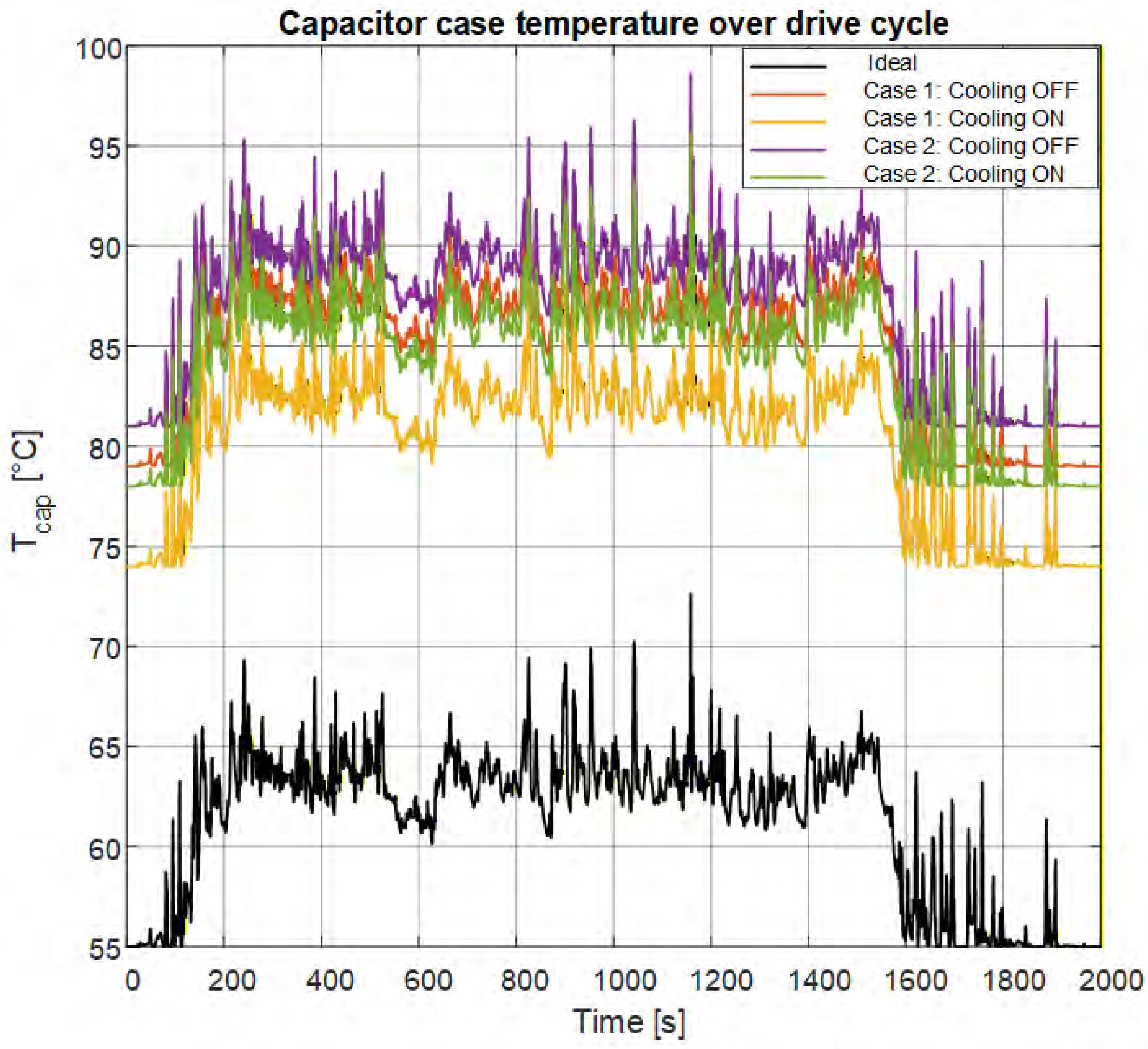

Figure 4.25: Capacitor temperature over drive cycle for each case at 55 °C ambient temperature.

Figure 4.26 illustrates the instantaneous damage rate over the same cycle. Damage increases exponentially with temperature. The best experimental case (Case I: Cooling ON) shows the peak damage rate roughly 2 times higher than the ideal case, while the worst case (Case II: Cooling OFF) shows the peak damage rate about 5 times higher than the best case and nearly 20 times higher than the ideal case.

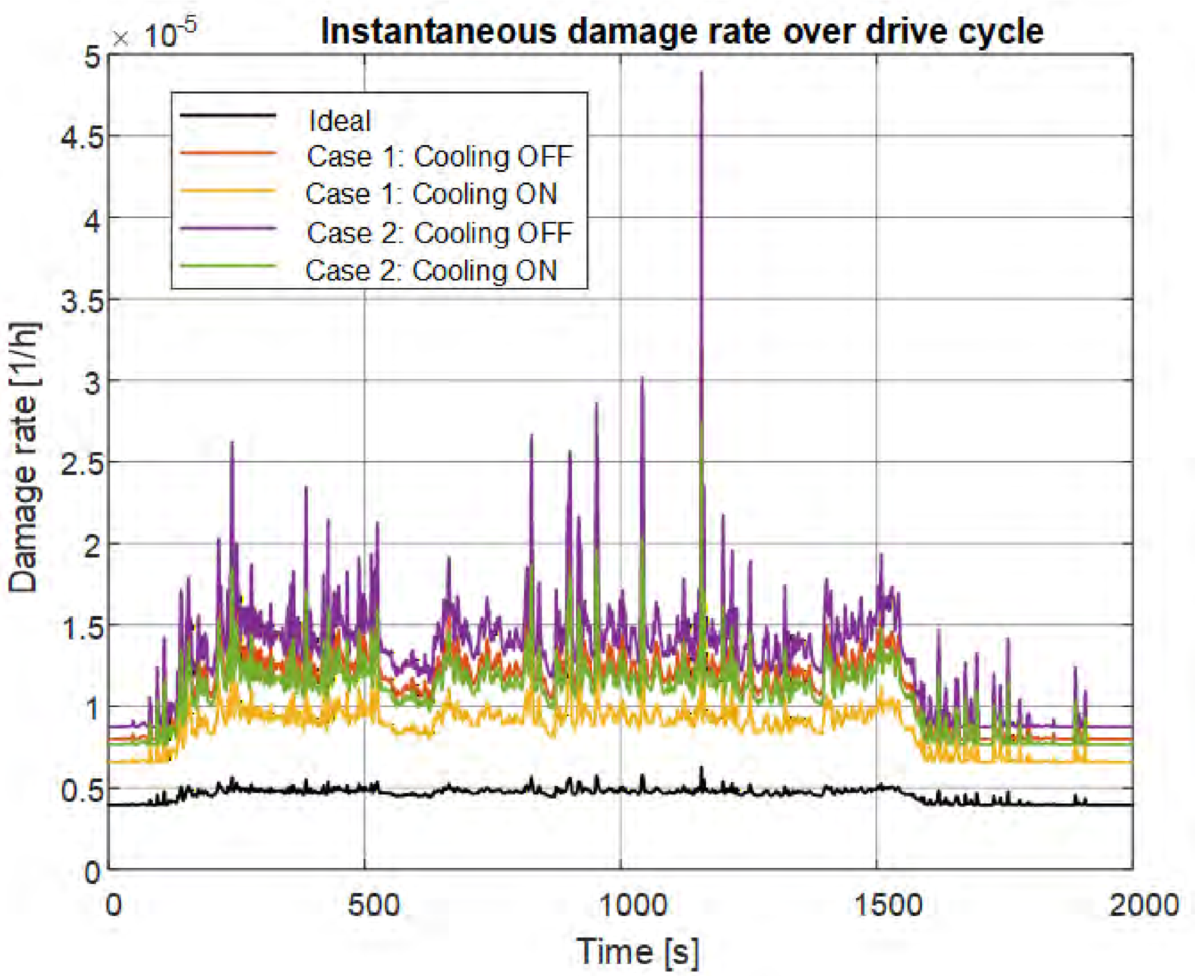

Figure 4.26: Capacitor instantaneous damage rate over drive cycle for each case at 55 °C ambient.

Figure 4.27 compares the capacitor's total damage per drive cycle as ambient temperature varies from 20°C to 55°C, while Figure 4.28 illustrates the corresponding lifetime trend. Total damage increases exponentially with ambient temperature, resulting in a linear decrease in estimated lifetime. In the ideal case, lifetime drops from approximately 46 years at 20°C to 25 years at 55°C. By comparison, the worst case (Case II: Cooling OFF) decreases from about 30 years at 20°C to roughly 8 years at 55°C.

Figure 4.29 presents the relative lifetime of each cooling scenario versus ambient temperature, normalized to the worst case (Case II: Cooling OFF). The results show a strong improvement with rising ambient temperature: the best case (Case I: Cooling ON) achieves about 11.5% longer lifetime at 20°C and nearly 50% longer lifetime at 55°C compared to the baseline.

Summary: The analysis shows that capacitor lifetime is highly sensitive to operating temperature, with ambient conditions and cooling effectiveness playing a critical role. Total damage per drive cycle increases exponentially with temperature, resulting in a linear reduction in lifetime. Under ideal datasheet assumptions, lifetime at 55°C ambient

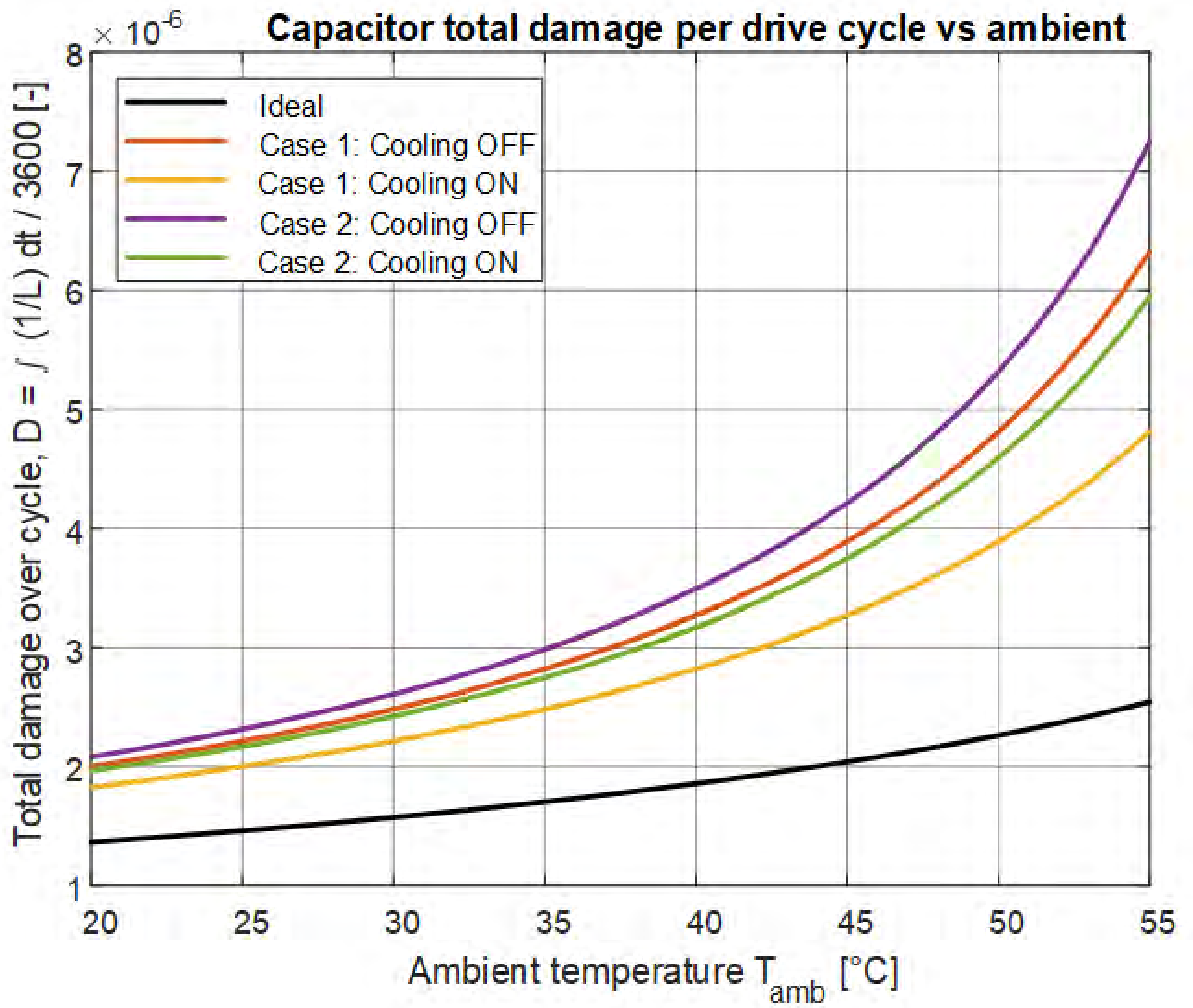

Figure 4.27: The capacitor total damage per drive cycle versus ambient temperature.

was estimated at 24.8 years, whereas experimentally adjusted scenarios ranged from 8.7 to 13.1 years, highlighting the impact of thermal bottlenecks.

Liquid cooling significantly improves thermal performance and lifetime. At high ripple currents, the best cooling configuration (Case I: Cooling ON) achieved up to 50% longer lifetime at 55°C ambient compared to the worst case (Case II: Cooling OFF). However, reductions in capacitor temperature were modest (approximately 18–21%), indicating that the capacitor remains the dominant factor.

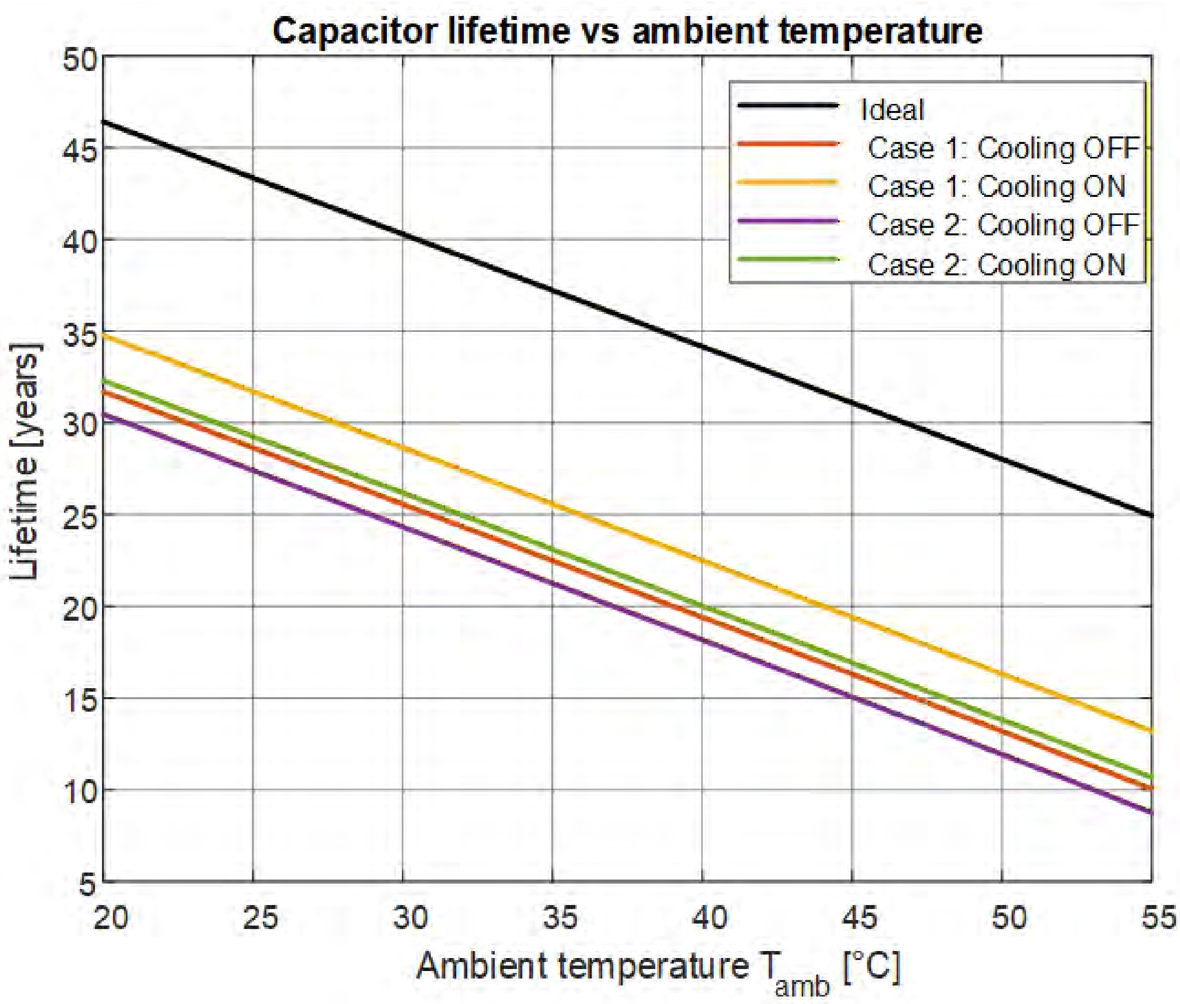

Figure 4.28: The capacitor lifetime versus ambient temperature.

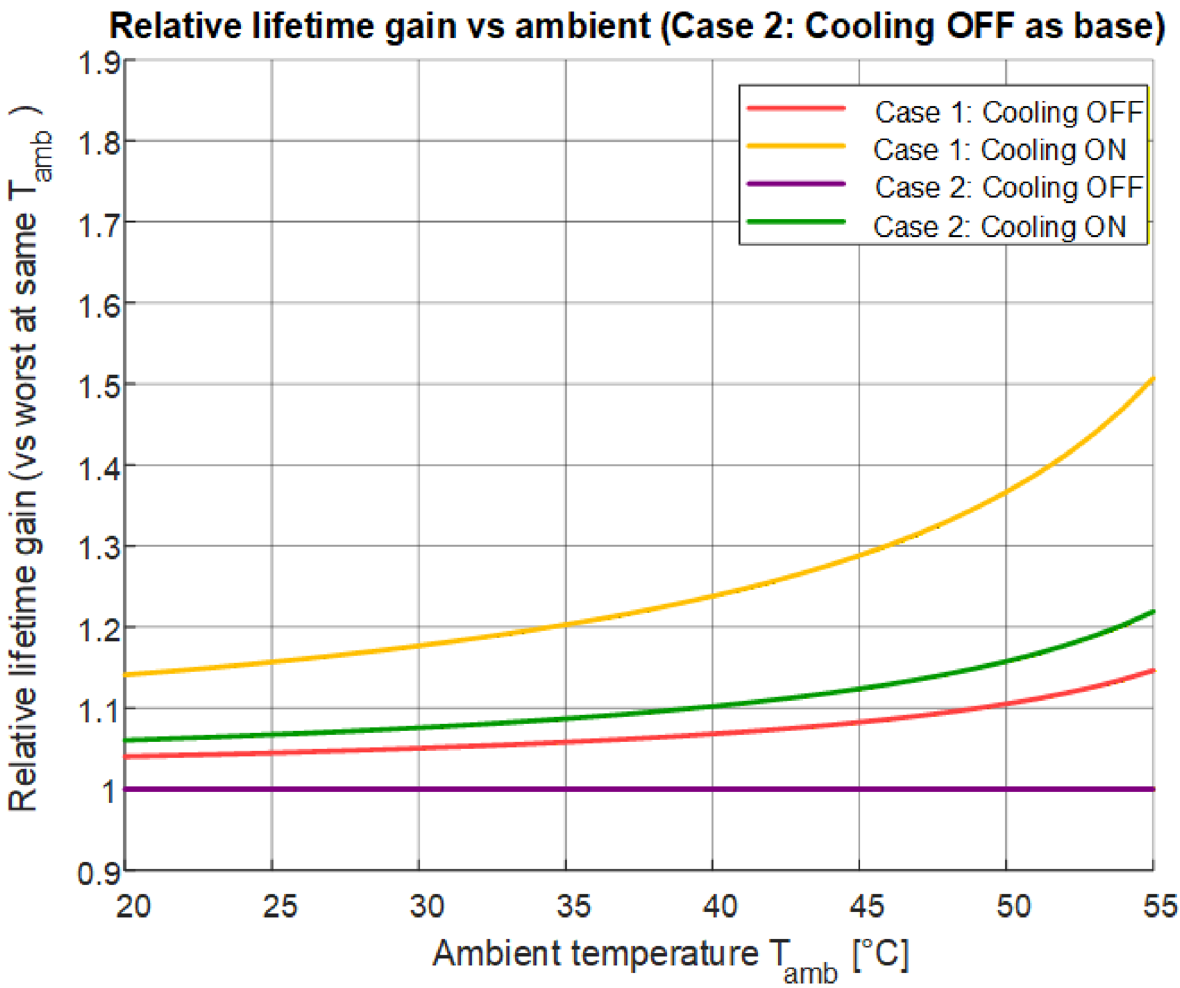

Figure 4.29: The capacitor relative lifetime in each cooling case versus ambient temperature.

5

Conclusion

This thesis presented the design and experimental evaluation of a double–three–phase SiC-based traction inverter, with emphasis on the electro–thermal performance of the DC-link. Two DC-link configurations were tested under varying ripple currents and cooling conditions to quantify their impact on thermal performance and capacitor lifetime.

- **Inverter Design and Validation:** A two-level six-phase inverter with a laminated DC bus and integrated control board was implemented. Open-loop SVPWM tests on an RL load confirmed correct space-vector synthesis and stable operation across DC-link voltages. Minor waveform irregularities at high q-axis references suggest EMI effects, requiring further study.
- **DC-Link Thermal Performance:** Ripple currents of 156 A_{rms} and 300 A_{rms} were applied to two layouts: **Case I:** Capacitors above the busbar; **Case II:** Capacitors in contact with the housing. Liquid cooling reduced busbar temperature significantly by up to 67% in Case I, while improvements at capacitor surfaces were modest (approximately 18–21%), indicating that internal thermal paths remain the dominant bottleneck.
- **Capacitor Lifetime Analysis:** Lifetime analysis combining datasheet curves, experimental thermal data, and HHDDT drive-cycle simulations revealed that capacitor lifetime decreases sharply with temperature. At 55 °C ambient temperature, under ideal conditions, the lifetime was estimated at 24.8 years, whereas real-world scenarios ranged from 8.7 to 13.1 years. The best cooling configuration (Case I: Cooling ON) achieved up to 50% lifetime improvement at 55 °C ambient compared to the worst case. These findings underscore the need for integrated thermal design, improved internal heat extraction, and accurate mission-profile-based modeling to ensure reliability in high-power, multi-phase traction inverters.

Future Work

- Closed-loop control and full six-phase machine testing.
- EMI/EMC characterization and layout optimization.

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A

Schematic Diagram of the Control Board

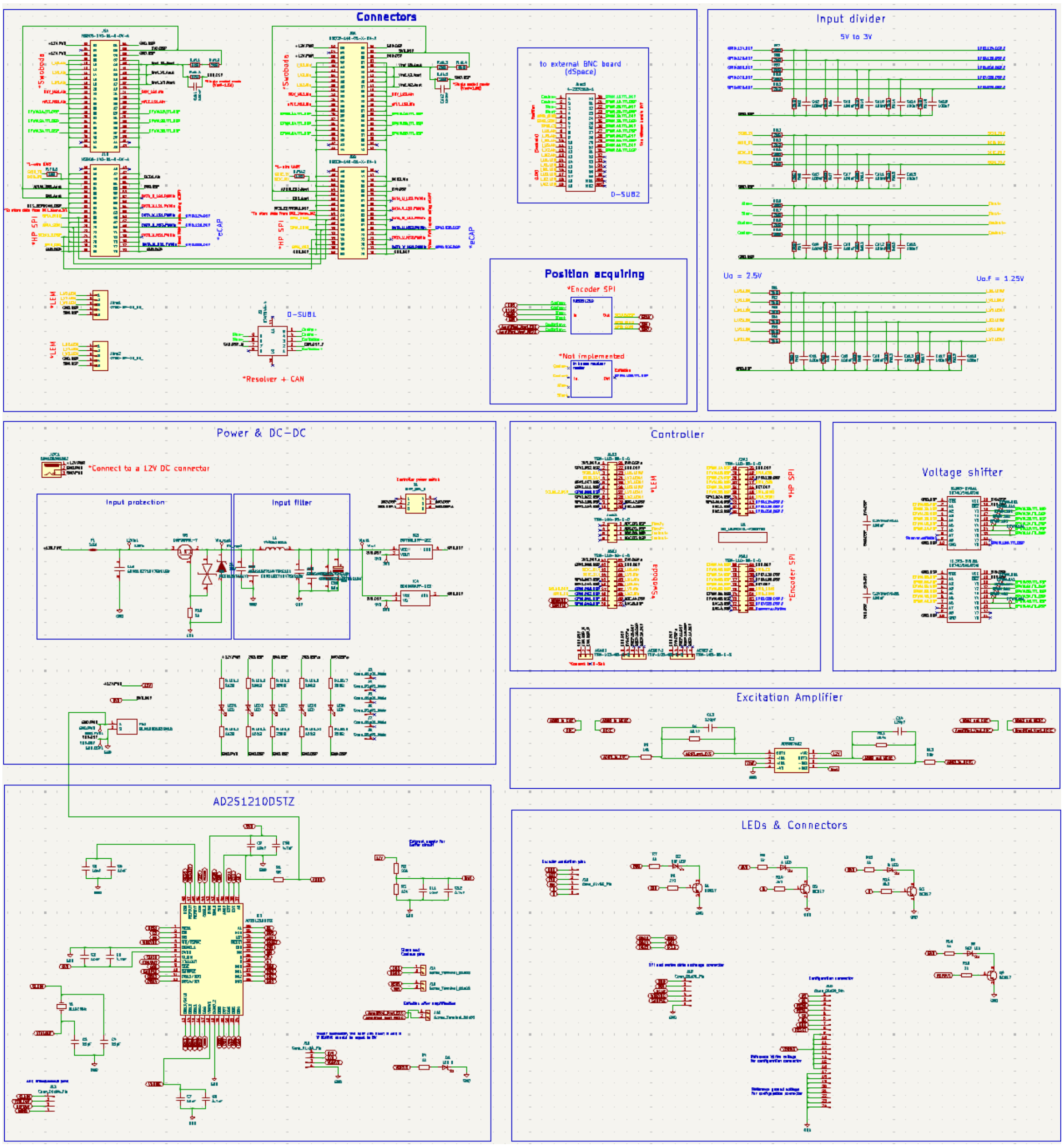

Figure A.1: Schematic diagram of the control board

B

Matlab Code for the Lifetime Analysis

```
close all
clc
clear

load('PMSM - CTRL.mat')
T_coolant   = 55;

Udc         = 800;
I_peak      = max(max(sqrt(CTRL.I_s_d.^2+CTRL.I_s_q.^2)));

% %Vehicle specifications   - Truck
Cd = 0.53;          % Drag coefficient
Af = 9.7;           % Frontal area in m2
Rho_air = 1.225 ;   %Air density kg/m3
Cr = 0.0051 ;        % Friction coefficient
m_veh = 40e3;       % Vehicle mass
g = 9.8 ;           %m/s^2
F_RR = m_veh*g*Cr;  % Rolling resistance force
Wr = 0.5 ;          % Wheel radius, in m
Tr = 19 ;           % transmission ratio 19:1
T_eff = 0.94 ;      % transmission efficiency
n_machines = 2;

%Manual inputs for loss calculation
I_peak      = 335;      %Peak current
M_a         = 0.3;      %Modulation Index
pf          = 0.2;      %Power factor
phi         = acos(pf); %power factor angle
f_sw        = 20e3;     %Switching frequency
dT_lim      = 0.05;     %convergence temperature for inverter iteration
Rth         = 0.144;

% load('PMSM - CTRL.mat')
define_FS03MR12A7MA2BA; %MOSFET Specifications

Simulink.Bus.createObject(FET1)
```

```
T_stop = 2000;
Tem_amplification = 1;
sim_data = sim('DriveCycleAnalysis_V1.slx',[0, T_stop]);

Distance = sim_data.X_Tot(length(sim_data.X_Tot))/1000; %Distance in km

% P_SW_L = trapz(sim_data.t(1500:1800),ans.P_SW(1500:1800));
% P_Cond_L = trapz(sim_data.t(1500:1800),ans.P_Cond(1500:1800));

P_SW_L = trapz(sim_data.t,sim_data.P_SW);
P_Cond_L = trapz(sim_data.t,sim_data.P_Cond);

% P_SW1 = max(sim_data.P_SW);
% P_Cond1 = max(sim_data.P_Cond);
% Total_losses = max(sim_data.P_SW)+max(sim_data.P_Cond);
Total_losses = (P_SW_L+P_Cond_L)/3600;
E_100km = 100*Total_losses/Distance;

%%
N = length(sim_data.I_cap_rms.Data);
Nlife       = 50; % assume a random lifetime
dc_time_step = sim_data.t(2)-sim_data.t(1);
dc_time     = max(sim_data.t);% Drive cycle time
dc_time_h   = dc_time/3600;

T_amb       = T_coolant; % automotive standard %21
ESR         = 5.6e-3; % per cap
n_C_par     = 9;
R_th        = 6.9; % C/W
uN          = 800/900;

P_closs     = ESR * (sim_data.I_cap_rms.Data./ n_C_par).^2 ;

% Ideal
deltaT      = R_th * P_closs;
T_cap       = deltaT + T_amb;
mean_T_cap = mean(T_cap)
lifetimes   = lifetime_mpodel_TDK_MPF(T_cap, uN);
dmg         = dc_time_step ./ 3600 ...
    ./ lifetime_mpodel_TDK_MPF(T_cap, uN);
dmg_tot_dc  = sum(dmg);
lifetime    = 1 / dmg_tot_dc * dc_time_h; % lifetime in hours
lifetime_yrs = lifetime/(24*365)

%%

T_max = 105;
```

```
dT_hotspot = [24 19 26 23]; %
Rthcap = 1/145*1000;
Pcap = ESR * (sim_data.I_cap_rms.Data./ n_C_par).^2 ;
for i=1:length(dT_hotspot)
    T_cap = Rthcap * Pcap + T_amb + dT_hotspot(i);

    T_cap(T_cap>T_max)=T_max;

    T_cap_max(i) = max(T_cap)
    lifetime =  lifetime_mpodel_TDK_MPF(T_cap, uN); %
    dmg = dc_time_step ./ 3600 ./ lifetime_mpodel_TDK_MPF(T_cap, uN);
    dmg_tot = sum(dmg);
    lifetime = 1 / dmg_tot * dc_time_h;
    lifetime_yrs(i) = lifetime/24/365;

    figure
    subplot(3,1,1)
    plot(T_cap)
    ylabel('Tcap')
    subplot(3,1,2)
    plot(Pcap)
    ylabel('Pcap')
    subplot(3,1,3)
    plot(dmg)
    ylabel('dmg')
end
lifetime_yrs
lifetime_rel = lifetime_yrs./min(lifetime_yrs)
T_cap_max

%%

% extract from sim_data:
 t = sim_data.t(:);
 I_cap_rms_v = sim_data.I_cap_rms.Data(:);

% Sanity checks and defaults
if exist('t','var') ~= 1, error('Provide time vector t.'); end
if exist('I_cap_rms_v','var') ~= 1
    if exist('I_cap_rms','var') == 1 && isstruct(I_cap_rms)...
            && isfield(I_cap_rms,'Data')
        I_cap_rms_v = I_cap_rms.Data(:);
    else
        error('Provide I_cap_rms_v or I_cap_rms.Data.');
    end
end
t = t(:); I_cap_rms_v = I_cap_rms_v(:);
assert(numel(t)==numel(I_cap_rms_v),'t and I_cap_rms_v must match.');
```

```
if exist('R_th_cap','var') ~= 1
    if exist('R_th','var') == 1, R_th_cap = R_th;...
    else, R_th_cap = 6.9; end  % K/W
end
if exist('ESR','var') ~= 1, ESR = 5.6e-3; end
if exist('n_C_par','var') ~= 1, n_C_par = 9; end
if exist('dT_hotspot','var') ~= 1, dT_hotspot = [24 19 26 23]; end
if exist('T_coolant','var') ~= 1, T_coolant = 60; end
if exist('Udc','var') ~= 1, Udc = 800; end
uN = Udc/900;

% Power loss in capacitor bank (W)
P_cap_W = ESR * (I_cap_rms_v ./ n_C_par).^2;

% Drive cycle duration (hours)
dc_time_h = (t(end) - t(1)) / 3600;

%% ---------- Ambient sweep ----------
T_amb_vec = (20:55).';  % °C
nT = numel(T_amb_vec);

% Choose whether coolant follows ambient
coolant_follows_ambient = true;

% Preallocate
nCases = numel(dT_hotspot);
lifetime_yrs_no_cool = zeros(nT,1);
lifetime_yrs_cases   = zeros(nT, nCases);
T_cap_max_no_cool    = zeros(nT,1);
T_cap_max_cases      = zeros(nT, nCases);

for k = 1:nT
    T_amb_k = T_amb_vec(k);

    % --- No-cool: Tcap = Tamb + Rth*Pcap ---
    T_cap_nc = T_amb_k + R_th_cap * P_cap_W;
    L_nc_h   = lifetime_mpodel_TDK_MPF(T_cap_nc, uN);
    dmg_nc   = trapz(t, 1 ./ L_nc_h) / 3600;
    life_nc_h = (1 / dmg_nc) * dc_time_h;
    lifetime_yrs_no_cool(k) = life_nc_h / (24*365);
    T_cap_max_no_cool(k) = max(T_cap_nc);

    % --- Cooling cases: Tcap = Rth*Pcap + Tcoolant + dT_hotspot ---
    if coolant_follows_ambient
        T_coolant_k = T_amb_k;
    else
        T_coolant_k = T_coolant;
```

```
    end

    for i = 1:nCases
        T_cap_i = R_th_cap * P_cap_W + T_coolant_k + dT_hotspot(i);
        L_i_h   = lifetime_mpodel_TDK_MPF(T_cap_i, uN);
        dmg_i   = trapz(t, 1 ./ L_i_h) / 3600;
        life_i_h = (1 / dmg_i) * dc_time_h;
        lifetime_yrs_cases(k,i) = life_i_h / (24*365);
        T_cap_max_cases(k,i) = max(T_cap_i);
    end
end

%% ---------- Build datasets ----------
% Absolute lifetime (years)
% Col 1 = No-cool; Cols 2..(1+nCases) = cooling cases
lifetime_yrs_all = [lifetime_yrs_no_cool, lifetime_yrs_cases];

% Relative lifetime ONLY among cooling cases (exclude No-cool)
% Normalize per T_amb to the worst (minimum) among the cooling cases
min_life_cases = min(lifetime_yrs_cases, [], 2);
lifetime_rel_cases = lifetime_yrs_cases ./ min_life_cases;

%% ---- Plot: Absolute lifetime vs T_amb (includes No-cool) ----
figure('Name','Capacitor Lifetime vs Ambient');
plot(T_amb_vec, lifetime_yrs_all, 'LineWidth', 1.6);
grid on; xlabel('Ambient temperature T_{amb} [°C]');
ylabel('Lifetime [years]');
title('Capacitor lifetime vs ambient temperature');
legend_labels_abs = [{'Datasheet'}, ...
    {'Case 1: Cooling OFF'}, ...
    {'Case 1: Cooling ON'}, ...
    {'Case 2: Cooling OFF'}, ...
    {'Case 2: Cooling ON'}];
legend(legend_labels_abs, 'Location', 'northeast');
%% ---- Plot: Relative lifetime vs T_amb (EXCLUDES No-cool) ----
figure('Name','Relative Lifetime gain vs Ambient (Cooling Cases Only)');
% Set the color order: [red, yellow, purple, green]
ax = gca;
ax.ColorOrder = [ ...
    1.0 0.25 0.25; ...
    1.0 0.75 0.0; ...
    0.5 0.0 0.5; ...
    0.0 0.6 0.0 ...
];
ax.NextPlot = 'replacechildren';

plot(T_amb_vec, lifetime_rel_cases, 'LineWidth', 1.6);
grid on;
```

```
xlabel('Ambient temperature T_{amb} [°C]');
ylabel('Relative lifetime gain (vs worst at same T_{amb})');
ylim([0.9 1.9])
title('Relative lifetime gain vs ambient (Case 2: Cooling OFF as base)');

legend_labels_rel = { ...
    'Case 1: Cooling OFF', ...
    'Case 1: Cooling ON', ...
    'Case 2: Cooling OFF', ...
    'Case 2: Cooling ON'};
legend(legend_labels_rel, 'Location', 'northeast');

%%

% Preallocate
dmg_tot_no_cool = zeros(nT,1);      % scalar damage per T_amb
dmg_tot_cases   = zeros(nT,nCases); % one column per case
Tcap_max_nc     = zeros(nT,1);
Tcap_max_cases  = zeros(nT,nCases);

%% ---------- Compute total damage per T_amb ----------
% Damage per cycle = \int (1 / Lifetime(T)) dt / 3600   (dimensionless)
for k = 1:nT
    T_amb_k = T_amb_vec(k);

    % --- No-cool baseline: Tcap = Tamb + Rth*Pcap ---
    T_cap_nc = T_amb_k + R_th_cap * P_cap_W;         % °C
    L_nc_h   = lifetime_mpodel_TDK_MPF(T_cap_nc, uN);% hours
    dmg_tot_no_cool(k) = trapz(t, 1 ./ L_nc_h) / 3600;
    Tcap_max_nc(k) = max(T_cap_nc);

    % --- Cooling scenarios: Tcap = Rth*Pcap + Tcool + dT_hotspot ---
    if coolant_follows_ambient
        T_coolant_k = T_amb_k;
    else
        T_coolant_k = T_coolant;
    end

    for i = 1:nCases
        T_cap_i = R_th_cap * P_cap_W + T_coolant_k + dT_hotspot(i);
        L_i_h   = lifetime_mpodel_TDK_MPF(T_cap_i, uN);
        dmg_tot_cases(k,i) = trapz(t, 1 ./ L_i_h) / 3600;
        Tcap_max_cases(k,i) = max(T_cap_i);
    end
end

%% ---------- Legends (as requested) ----------
legend_labels_abs = [{'Ideal'}, ...
```

```
    {'Case 1: Cooling OFF'}, ...
    {'Case 1: Cooling ON'}, ...
    {'Case 2: Cooling OFF'}, ...
    {'Case 2: Cooling ON'}];

legend_labels_rel = { ...
    'Case 1: Cooling OFF', ...
    'Case 1: Cooling ON', ...
    'Case 2: Cooling OFF', ...
    'Case 2: Cooling ON'};

%% ---- Plot: Total damage vs ambient (includes No-cool) ----
figure('Name','Total Damage vs Ambient');
plot(T_amb_vec, [dmg_tot_no_cool, dmg_tot_cases], 'LineWidth', 1.6);
grid on; xlabel('Ambient temperature T_{amb} [°C]');
ylabel('Total damage over cycle, D = \int (1/L) dt / 3600 [-]');
title('Capacitor total damage per drive cycle vs ambient');
legend(legend_labels_abs, 'Location', 'northwest');

%%
Tcap_no_cool = T_amb + R_th_cap * P_cap_W;
nCases = numel(dT_hotspot);
Tcap_cases = zeros(numel(t), nCases);
for i = 1:nCases
    Tcap_cases(:,i) = R_th_cap * P_cap_W + T_coolant + dT_hotspot(i);
end

%% ==== Compute instantaneous damage rate and total damage ====
L_no_cool_h = lifetime_mpodel_TDK_MPF(Tcap_no_cool, uN);
dmg_rate_no_cool = 1 ./ L_no_cool_h;            % [1/h]
dmg_tot_no_cool  = trapz(t, dmg_rate_no_cool) / 3600;

L_cases_h = lifetime_mpodel_TDK_MPF(Tcap_cases, uN);
dmg_rate_cases = 1 ./ L_cases_h;
dmg_tot_cases  = trapz(t, dmg_rate_cases) / 3600;


%% ====== Plot T_cap(t) in its own figure ======
figure('Name','Capacitor Temperature vs Time');
plot(t, Tcap_no_cool, 'k-', 'LineWidth', 1.0); hold on;
plot(t, Tcap_cases, 'LineWidth', 1.0);
grid on; xlabel('Time [s]'); ylabel('T_{cap} [°C]');
title('Capacitor case temperature over drive cycle');
legend({'Ideal', 'Case 1: Cooling OFF', 'Case 1: Cooling ON',...
    'Case 2: Cooling OFF', 'Case 2: Cooling ON'}, ...
       'Location','best');

%% ====== Plot damage rate(t) in its own figure ======
```

```
figure('Name','Damage Rate vs Time');
plot(t, dmg_rate_no_cool, 'k-', 'LineWidth', 1.0); hold on;
plot(t, dmg_rate_cases, 'LineWidth', 1.0);
grid on; xlabel('Time [s]'); ylabel('Damage rate [1/h]');
title('Instantaneous damage rate over drive cycle');
legend({'Ideal', 'Case 1: Cooling OFF', 'Case 1: Cooling ON',...
    'Case 2: Cooling OFF', 'Case 2: Cooling ON'}, ...
       'Location','best');


%% ====== Interpolation from datasheet parameters ======
function lifetime_hr = lifetime_mpodel_TDK_MPF(T, nU)

% Based on TDK D2663 xE series film capacitor e.g., B25632E0906K900
% T = hotspot temperature
% nU = U_DC / U_rated

intercept = 814750.000000;
coef_T    = -5350.000000;
coef_nU   = -300000.000000;
lifetime_hr = intercept + coef_T .* T + coef_nU .* nU;

end
```

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