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Design of mm-wave Front-end for Multi-antenna Communication Systems

Master's thesis in Wireless, Photonics and Space Engineering

Han Zhou

Department of Microtechnology and Nanoscience, MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

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Abstract

A Ka-band (desired frequency band: 27.5 GHz − 32.5 GHz) receiver front-end is designed in a 130 nm BiCMOS process. A triple balanced capacitive mixer with varactor diodes is demonstrated and it achieves an IIP3 of 45 dBm, with a conversion loss of 20 dB. In order to support the proposed mixer, an inductive emitter-degenerated cascode LNA cascaded with a differential pair active balun is proposed. The LNA has a reflection coefficient of less than -20 dB, an available gain of more than 17 dB, a noise figure of less than 2.4 dB, an IIP3 of 10 dBm and a power consumption of 12 mW. The active balun has a maximum phase error of 0.5° and an amplitude imbalance of 40 mdB. In addition, self biasing and bandgap reference circuits are studied and simulated. Finally, a layout prototype of the receiver front-end is presented, with a total area of 0.9 mm×0.7 mm.

Keywords: Ka-band, BiCMOS, capacitive mixer, triple balanced mixer, cascode LNA, SNIM, active balun, bandgap reference.

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Han Zhou, Gothenburg, June 2018

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1

Introduction

Wireless communication technologies immensely benefited from semiconductor integrated circuit advancement. Nowadays, CMOS technologies are undergoing rapid development, which has enabled circuits to be integrated on the same die to achieve lower cost. However, the performance of CMOS technologies at high frequencies still has limitations compared to bipolar technologies, though they are more integration friendly. Therefore BiCMOS technologies are preferred to maintain a high integration level and have a promising high frequency performance at the same time.

As 5G technologies are developing, higher data rate and more reliable latency for wireless communication are required. More importantly, millimeter wave, massive MIMO and ultra-densification are the three key technologies for 5G[1].

In this thesis, a Ka band (desired frequency band: 27.5 GHz − 32.5 GHz) receiver front-end within a 130 nm BiCMOS process will be studied and designed for a future multi-antenna communication systems.

1.1 Receiver Front-end Challenges

Receiver front-ends are responsible for the linearity and noise performance, as well as sensitivity of the overall receiver architecture. Generally, the first block of the receiver architecture, which is an LNA, plays an important role in receiver sensitivity and noise performance. However, it is often difficult to minimize the reflection coefficient and at the same time maintain a promising noise performance of the LNA.

In addition, mixers are a critical block that is dominant in linearity performance of a receiver architecture. In order to improve the linearity performance of mixers, distortion cancellation topologies are required. Besides, a balanced structure is preferred for mixers because it provides a mixer with a good isolation among its three ports. Therefore, the device that converts between a balanced signal and an unbalanced signal i.e. a balun, is also needed. However, in Radio Frequency Integrated Circuits (RFIC) design, the conventional passive balun is too bulky and lossy. Therefore, active implementations are preferred whenever possible.

1.2 Thesis Contributions

A distortion cancellation structure of mixers has been studied and designed. The proposed mixer topology consists of varactor diodes and it is called capacitive mixers. The Volterra series has been used to analyze the distortion performance of the capacitive mixers. Thus, under the special case, when the grading coefficient of the varactor diodes equals 0.5, the capacitive mixers have distortion-free performance. Meanwhile, double and triple balanced topologies for the capacitive mixers have been proposed. In addition, an emitter-degenerated cascode LNA with Simultaneous Noise and Input Matching (SNIM) has been designed. A differential pair active balun with a feedback network has been studied and designed. Further more, the self-biasing and bandgap reference circuits have been studied and simulated. Finally, a receiver front-end layout prototype has been designed and presented.

1.3 Thesis Outline

The thesis is organized as follows. In Chapter 2, a mixer with a distortion cancellation topology is presented. An analysis of the varactor diodes mixer by using Taylor and Volterra series are presented. The balanced mixer circuit prototype is introduced and the simulation results are shown and compared with the theoretical results. Chapter 3 focus on the design of the LNA with SNIM technique, simulation results for the given process technology are shown and discussed. Chapter 4 presents the design of a differential active balun, the challenges for the balun to operate at high frequency are explained and solutions are proposed. Besides, simulation for the given process technology are shown and discussed. In Chapter 5, an overview and study of the self-biasing circuit and bandgap reference circuit are presented, simulation results are shown to verify the theory. In Chapter 6, a complete layout prototype design of the front-end is shown. Finally, Chapter 7 concludes the presented work and discusses the future work.

2

Capacitive Mixers

In a wireless communication system, mixers are the critical block in the receiver architecture. It plays a dominant role in the distortion performance of the receiver. In order to improve the linearity of mixers, a specific varactor diodes topology will be introduced. This topology utilizes the inherent nonlinearity of the varactor diodes for frequency mixing. The proposed mixer topology has ultra low distortion, as the grading coefficient, n, of varactor diodes equals 0.5. This means that, theoretically there would not be any distortions at the RF and LO ports. While at the IF port, there is no third or higher order distortion.

2.1 Theory

2.1.1 Non-linear Distortion Fundamentals

2.1.1.1 Single-tone and Two-tone Excitation

As mentioned in [2], for a non-linear device, when the signal $x(t)$ with amplitude A at frequency f is applied at its input, the output signal $y(t)$ from the device can be derived by Taylor series expansion,

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + ..., \tag{2.1}$$

Where a_n are the Taylor coefficients, which are dependent on the bias point X_0,

$$a_n = \frac{1}{n!}\frac{d^n y(X_0)}{dx^n}. \tag{2.2}$$

When the signal at the input of a non-linear device is sinusoidal, which means $x(t) = Acos(\omega t)$, the output signal from the device derived according to equation (2.1) can be written as:

$$y(t) = \frac{1}{2}a_2A^2 + (a_1A + \frac{3}{4}a_3A^3)cos(\omega t) + \frac{1}{2}a_2A^2cos(2\omega t) + \frac{1}{4}a_3A^3cos(3\omega t) + ... \tag{2.3}$$

The obtained output signal above has different frequency components, for example, the DC component $\frac{1}{2}a_2A^2$, the linear gain and gain compression component $(a_1A + \frac{3}{4}a_3A^3)$, also second and third order harmonic component, which are $\frac{1}{2}a_2A^2$ and $\frac{1}{4}a_3A^3$ respectively.

If a two-tone sinusoidal signal is added at the input of a non-linear device with the same amplitude, which means $x(t) = Acos(\omega_1 t) + Acos(\omega_2 t)$, the output signal from the device according to equation (2.1) can be expressed as:

$$\begin{aligned} y(t) = a_2A^2 + (a_1A + \frac{9}{4}a_3A^3)cos(\omega_{1,2}t) + \frac{1}{2}a_2A^2cos(2\omega_{1,2}t) + \\ \frac{1}{4}a_3A^3cos(3\omega_{1,2}t) + a_2A^2cos(\omega_2 \pm \omega_1) + \\ \frac{3}{4}a_3A^3cos(2\omega_{1,2} \pm \omega_{2,1}) + ... \end{aligned} \tag{2.4}$$

The same as the scenario from single-tone excitation, the output signal $y(t)$ contains: DC component a_2A^2, linear gain and gain compression component $(a_1A + \frac{9}{4}a_3A^3)$, second and third order harmonic component. Besides, there are new components showing up, they are second order intermodulation product (IM2) and third order intermodulation product (IM3), which are $a_2A^2cos(\omega_2 \pm \omega_1)$ and $\frac{3}{4}a_3A^3cos(2\omega_{1,2} \pm \omega_{2,1})$ respectively. In addition, it is these second order mixing components that are fundamental to the operation of an RF mixer, as will be shown in the next section.

2.1.2 Mixer Fundamentals

A mixer is a three-port device, which contains two input ports and one output port. When it comes to wireless communication applications, there are two kinds of mixers in general, i.e. down-conversion and up-conversion mixers. For down-conversion mixers, the input signals are local oscillator (LO) and radio frequency (RF) signals and the output signal is the intermediate frequency (IF) signal, while for up-conversion mixers, the input signals are IF signal and LO signal and the output signal is RF signal. The input and output frequency relation can be written as:

$$f_{out} = |f_{in1} \pm f_{in2}| \tag{2.5}$$

For down-conversion mixers, the image frequency can also be converted to IF, which should be avoided. Therefore, the image rejection topology or external filters are usually included into the down-conversion mixer designs. Figure 2.1 shows the spectrum of a down-conversion mixer.

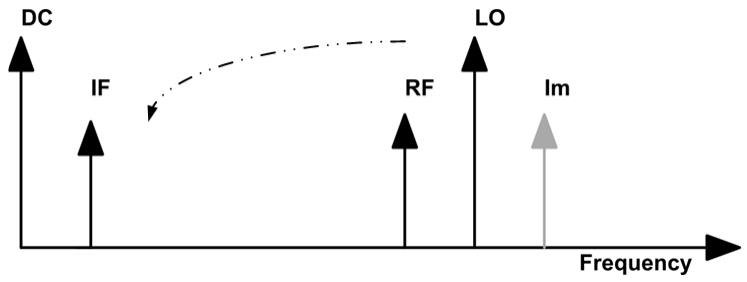


Figure 2.1: Spectrum showing frequency mixing of down-conversion mixers.

When it comes to mixer configurations, there are two categories of mixers in general. The first category is the mixers with strong non-linearity, these kind of mixers have

a strong input LO signal which controls the on and off rates of the transistor. This results in a square-wave signal that is modulated by the input LO signal and these classes of mixers are also called switching mixers. In contrast we propose to use the weakly nonlinear mixers, which utilize the second-order nonlinear behavior of the mixers to generate the output signal.

2.1.3 Proposed Mixer Topology

As the figure 2.2a shows, the nonlinear components in the proposed circuit are varactor diodes. The distortion performance of this circuit will be analyzed in the next sections.

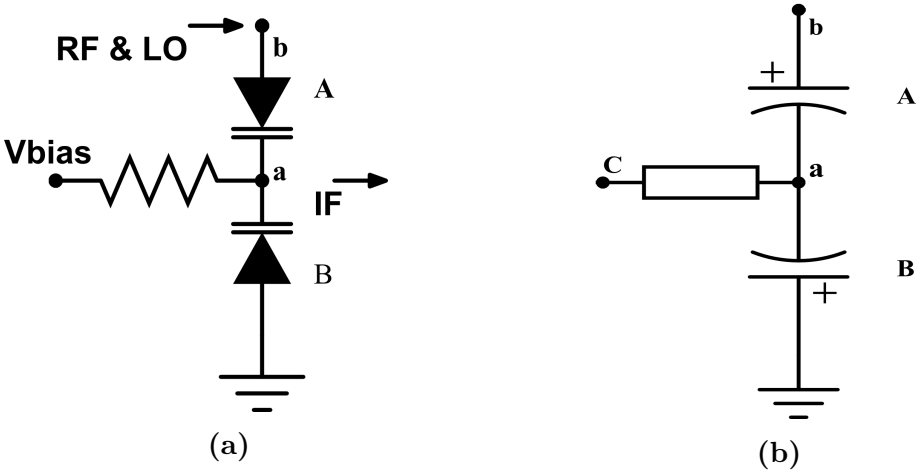


Figure 2.2: (a) Proposed mixer topology with reverse-biased varactor diodes. (b) Anti-series connected nonlinear capacitors.

2.1.3.1 Taylor Series Analysis

The following derivation is demonstrated in [3]. For a reverse-biased or nonlinear capacitor, the current through them can be expressed by a Taylor expansion as:

$$i = C_0 \cdot \frac{dv}{dt} + \frac{C_1}{2} \cdot \frac{dv^2}{dt} + \frac{C_2}{3} \cdot \frac{dv^3}{dt} + ..., \tag{2.6}$$

$$C(v) = \frac{d}{dv}(C_0 \cdot v + \frac{C_1}{2} \cdot v^2 + \frac{C_2}{3} \cdot v^3 + ...) = C_0 + C_1 \cdot v + C_2 \cdot v^2 + ..., \tag{2.7}$$

where $C_0, C_1/2$, $C_2/3, ...C_n/n$ are Taylor coefficients, which correspond to a_n from equation (2.1). In addition, distortion from a nonlinear circuit can be represented by $C_1, ...C_n$, among which C_1 and C_2 are the coefficients that are responsible for the second and third order distortion respectively. Therefore, during the design of the mixer circuit, these coefficients should be minimized.

Figure 2.2b shows the anti-series connected nonlinear capacitors, according to this configuration, the $C(v)$ expressions can be written as:

$$C_A(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot v_A^2 + ..., \tag{2.8}$$

$$C_B(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot v_B^2 + ..., \tag{2.9}$$

where v_A and v_B are the voltage across nonlinear capacitor A and B respectively.

Since the incremental charge from capacitor A and B are the same, the following expression can be derived:

$$C_t = T_0 + T_1 \cdot v_t + T_2 \cdot v_t^2 ... = \frac{1}{g_0} - \frac{2g_1}{g_0^3} \cdot v_t + \frac{6g_1^2 - 3g_0 g_2}{g_0^5} \cdot v_t^2 ..., \tag{2.10}$$

where v_t and C_t are the total voltage and capacitance of the circuit, which is analyzed at the node b from figure 2.2b, and

$$g_0 = \frac{1}{C_{A0}} + \frac{1}{C_{B0}}, \tag{2.11}$$

$$g_1 = \frac{C_{B1}}{2C_{B0}^3} - \frac{C_{A1}}{2C_{A0}^3}, \tag{2.12}$$

$$g_2 = \frac{C_{A1}^2/2 - C_{A0}C_{A2}/3}{C_{A0}^5} + \frac{C_{B1}^2/2 - C_{B0}C_{B2}/3}{C_{B0}^5} \tag{2.13}$$

According to [4], the mathematical model of an ideal single varactor diode, i.e. the relation of capacitance and the applied voltage, can be written as:

$$C(V) = \frac{K}{(\phi + V)^n}, \tag{2.14}$$

where ϕ is built-in potential, n is grading coefficient, $K = C_{j0} \cdot \phi^n$ and C_{j0} is zero-bias capacitance. When the bias voltage is V_C and the voltage of the applied signal is v, then

$$C(v) = \frac{K}{(\phi + V_C)^n} \cdot (1 + \frac{v}{\phi + V_C})^{-n} \tag{2.15}$$

According to equation (2.1), (2.2), (2.6), (2.7) and (2.15), the coefficients of $C(V)$ can be derived and expressed as:

$$C_0 = 1 \cdot (\frac{1}{1!} \cdot \frac{d^0 C(v)}{dv^0}|_{v=0}) = \frac{K}{(\phi + V_C)^n}, \tag{2.16}$$

$$C_1 = 2 \cdot (\frac{1}{2!} \cdot \frac{d^1 C(v)}{dv^1}|_{v=0}) = -C_0 \cdot \frac{n}{\phi + V_C}, \tag{2.17}$$

$$C_2 = 3 \cdot (\frac{1}{3!} \cdot \frac{d^2 C(v)}{dv^2}|_{v=0}) = C_0 \cdot \frac{n(n+1)}{2(\phi + V_C)^2}. \tag{2.18}$$

Set the diode area ratio to be r yielding

$$r = \frac{D_A}{D_B} = \frac{C_A}{C_B} = \frac{C_{A0}}{C_{B0}} = \frac{C_{A1}}{C_{B1}} = \frac{C_{A2}}{C_{B2}}, \tag{2.19}$$

then follow the same procedure as equation (2.8)-(2.13), yielding

$$T_0 = \frac{rK_A}{(1+r)(\phi+V_C)^n}, \tag{2.20}$$

$$T_1 = C_0 \cdot \frac{(1-r)n}{(1+r)(\phi+V_C)}, \tag{2.21}$$

$$T_2 = C_0 \cdot \frac{n[(r^2+1)(n+1) - r(4n+1)]}{2(1+r)(\phi+V_C)^2}. \tag{2.22}$$

By making some mathematical manipulation, T_2 can be set to be zero, under the condition of

$$r = \frac{4n+1+\sqrt{12n^2-3}}{2(n+1)}. \tag{2.23}$$

Therefore, when diode ratio $r = 1$ and grading coefficient $n = 0.5$, the second order (T_1) and third order (T_2) distortion at the input (node b) of the proposed structure in figure 2.2a are equal to zero. Also, higher order distortions are eliminated as mentioned in [5].

2.1.3.2 Volterra Series Analysis

As mentioned in [6], for weakly nonlinear circuits, the input signal can be correctly expressed by the first three terms of a Volterra series expansion. Meanwhile, in order to determine the transfer functions of the nonlinear circuits, the calculation of the kernels is required. According to equation (2.1), (2.6) and (2.15), the input current of the circuit in figure 2.3a can be written as:

$$i_{in} = \frac{d}{dt}(K_{1A} \cdot v_A + K_{2A} \cdot v_A^2 + K_{3A} \cdot v_A^3) = \frac{d}{dt}(K_{1B} \cdot v_B + K_{2B} \cdot v_B^2 + K_{3B} \cdot v_B^3), \tag{2.24}$$

where

$$K_{1A,B} = \frac{1}{1!} \cdot \frac{d^0 C(v)}{dv^0}|_{v=0} = \frac{K}{(\phi+V_C)^n}, \tag{2.25}$$

$$K_{2A,B} = \frac{1}{2!} \cdot \frac{d^1 C(v)}{dv^1}|_{v=0} = -K_{1A,B} \cdot \frac{n}{2(\phi+V_C)}, \tag{2.26}$$

$$K_{3A,B} = \frac{1}{3!} \cdot \frac{d^2 C(v)}{dv^2}|_{v=0} = K_{1A,B} \cdot \frac{n(n+1)}{6(\phi+V_C)^2}. \tag{2.27}$$

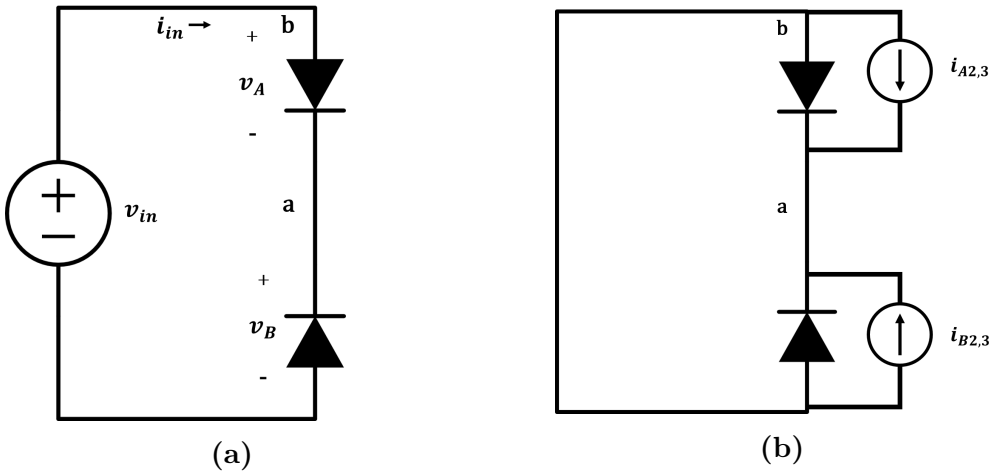


Figure 2.3: (a) First-order kernels calculation for the proposed mixer topology. (b) Second-order and third-order kernels calculation for the proposed mixer topology.

First-order Kernels are the transfer function of the linearized circuit, which should be analyzed with the externel excitations applied. Applying Kirchoff's current law at node a from figure 2.3a yields

$$sC_A \cdot (v_a - v_{in}) + sC_B = 0, \tag{2.28}$$

from the equation above, the following relation can be derived:

$$v_a = \frac{sC_A}{sC_A + sC_B}, \tag{2.29}$$

then, the first-order kernels at node a of the proposed mixer circuit can be written as:

$$H_{1a} = \frac{1}{r+1}. \tag{2.30}$$

Therefore, when $r = 1$, $H_{1a} = \frac{1}{2}$.

Second-order and Third-order Kernels use the same linearized circuit as the circuit that is used to calculate the first-order kernels, however, instead of external excitations, the excitations of the circuit are nonlinear current source of order two and three from the nonlinear capacitors, as figure 2.3b shows.

Table 2.1: Overview of the expression for nonlinear current source of order two and three[6].

Basic nonlinearity	Nonlinear current source of order two (i_2)	Nonlinear current source of order three (i_3)
Capacitance	$(s_1 + s_2)K_2H_2(s_1)H_2(s_2)$	$(s_1 + s_2 + s_3)K_3H_1(s_1)H_1(s_2)H_1(s_3)+$ $\frac{2}{3}(s_1 + s_2 + s_3)K_2[H_1(s_1) + H_2(s_2, s_3)$ $H_1(s_2H_2(s_1, s_3)) + H_1(s_3H_2(s_1, s_2))]$

Follow the same procedures above with Kirchoff's current law at node a yields

$$(sC_A + sC_B)v_a + i_{A2} + i_{B2} = 0, \tag{2.31}$$

thus the second-order kernels at node a of the proposed mixer circuit can be expressed as:

$$H_{2a} = \frac{r \cdot n}{2(\phi + V_C)(r+1)^2}, \tag{2.32}$$

therefore, under the same conditions as used in Taylor series analysis, which is $r = 1$ and $n = 0.5$, the equation above can be simplified to

$$H_{2a} = \frac{1}{16(\phi + V_C)}. \tag{2.33}$$

Similarly, the third order kernels are able to be calculated by the same procedure as equation (2.31)-(2.33), so that $H_{3a} = 0$.
Therefore, if a voltage excitation v_i is applied at the input (node b) from figure 2.2a, the center-tap voltage v_o at the output (node a) can be expressed as:

$$v_o = \frac{v_i}{2} + \frac{v_i^2}{16(\phi + V_C)}, \tag{2.34}$$

this result was also presented in [3]. When the two-tone signal $v_i = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$ is applied at the input of the circuit, the output signal can be written as:

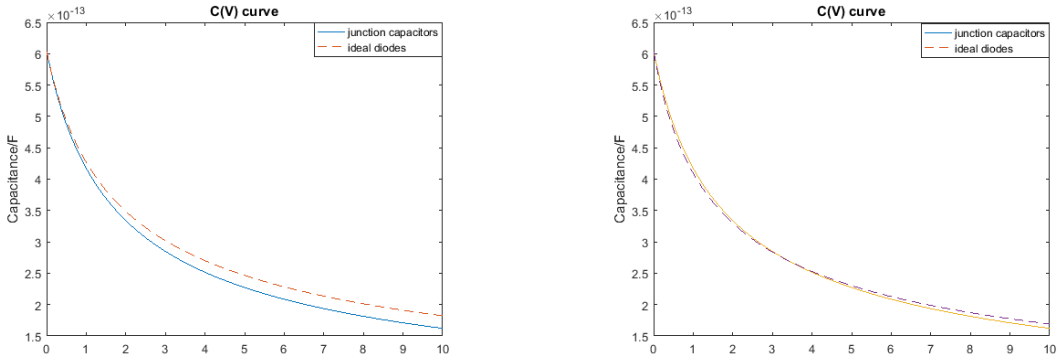
$$\begin{aligned} v_o = \frac{1}{2}[A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)] + \frac{1}{16(\phi + V_C)} \cdot [\frac{A_1^2}{2} + \frac{A_2^2}{2} + \frac{A_1^2}{2} cos(2\omega_1 t) + \\ \frac{A_2^2}{2} cos(2\omega_2 t) + A_1 A_2 cos((\omega_1 + \omega_2)t) + A_1 A_2 cos((\omega_1 - \omega_2)t)]. \end{aligned} \tag{2.35}$$

From the equation (2.35), signal components such as DC shift, first and second order harmonics and second order intermodulation products can be identified. In addition, there is no higher order harmonics or intermodulation products within the circuit.

2.2 Circuit Design

2.2.1 Process Investigation

As mentioned previously, the 130 nm BiCMOS process has been used in this design. This process provides varactor diodes, pin diodes and junction capacitors. The initial step was to simulate the C(V) curve of each device to check its deviation compared with the ideal C(V) curve. Among all these devices, the C(V) curve of a junction capacitor has the least deviation from the ideal analytical C(V) curve. Therefore, it has been chosen in the mixer design.



(a) **(b)**

Figure 2.4: (*a*) C(V) curve of junction capacitors. (*b*) Line fit for junction capacitors, in which $\phi = 0.85$, $n = 0.5$.

As shown in figure 2.4, it can be seen that, the C(V) curve of the junction capacitors can be accurately estimated by the C(V) curve of the analytical diode model if the $\phi = 0.85$ and $n = 0.5$. Therefore, according to figure 4.9 in [3], the third order intermodulation products of the proposed mixer structure with junction capacitor can be estimated, which is still reasonably small.

2.2.2 Balanced Mixers

2.2.2.1 Double Balanced Mixers

As described previously, in an ideal case, there are no higher order harmonics or intermodulation products from the proposed mixer structure. In addition, the RF and LO signals applied at the input of a mixer should be suppressed at its IF port, therefore a double balanced mixer topology is often applied, as shown in figure2.5.

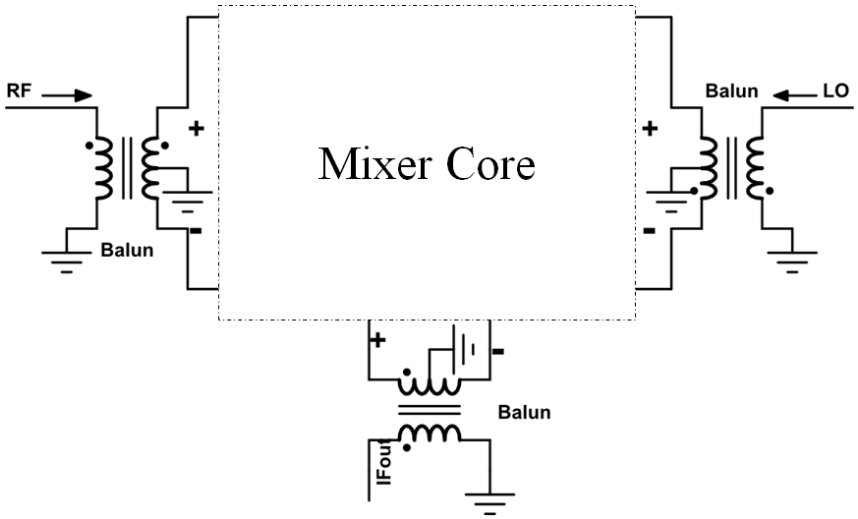


Figure 2.5: Double balanced mixer topologies with the proposed anti-series diode connection.

2.2.2.2 Triple Balanced Mixers

As described in last chapter, the double balanced mixer topology is able to suppress the RF and LO signals at its IF output port. However, there is no isolation between RF port and LO port, which means there will be LO leakage at RF port and vice versa. This problem has to be avoided, thus a triple balanced mixer topology has been designed, as shown in figure 2.6. Futhermore, one of the baluns at the input of the mixer has been swapped, so that both RF and LO signals are 180° out of phase before reaching the power combiner, thus yielding isolation between RF and LO ports.

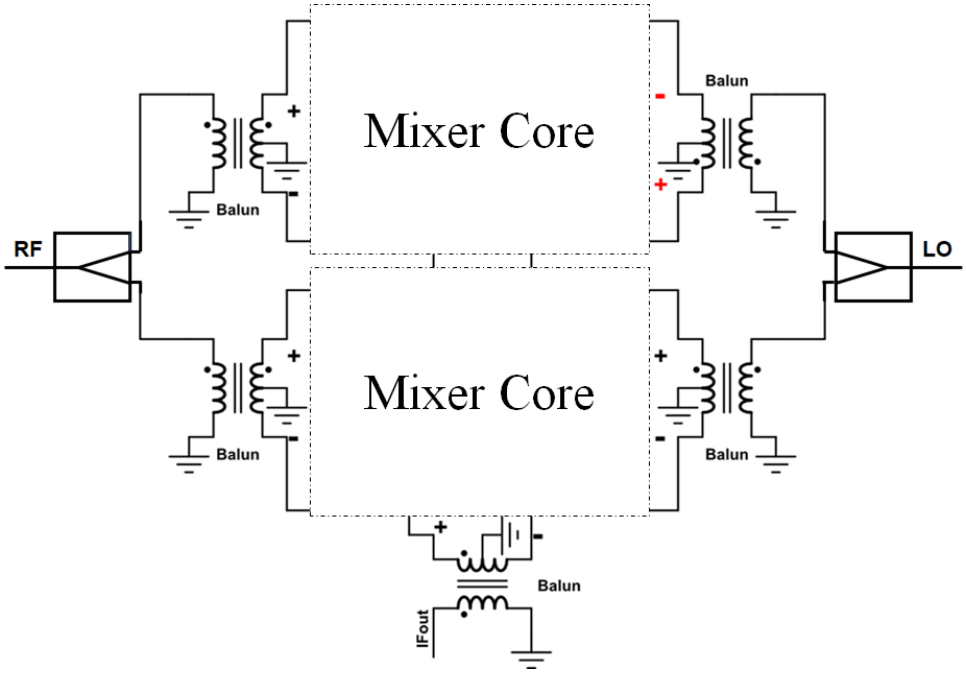


Figure 2.6: Triple balanced mixer topologies with the proposed anti-series diode connection.

2.3 Results and Discussion

In the harmonic balance simulation, the LO frequency is 29 GHz, the two-tone RF frequency is at 30.01 GHz and 30 GHz respectively. Besides, ideal varactor diodes are used, having equal size with a grading coefficient of 0.5.

2.3.1 Verification of Proposed Mixer Theory

2.3.1.1 Single Stack Varactor Diodes

Figure 2.7 shows the simulation results of the circuit (figure 2.2a). The simulation environment is ADS and the varactor diode model is ideal. According to figure 2.7a and 2.7b, there are only fundamental tones at the input ports, which are RF and LO. The higher order distortion and intermodulation products are less than 300

dBm, which is numerically zero. Therefore, the single stack varactor diode topologies are totally distortion-free at the input as mathematically shown in the Taylor series analysis chapter previously.

In addition, according to figure 2.7c and 2.7d, at the IF output port, there are only fundamental tones (RF and LO), second order harmonics and second order intermodulation products (including IF). The higher order harmonics and intermodulation products have been completely canceled out as proven in the section on Volterra series analysis.

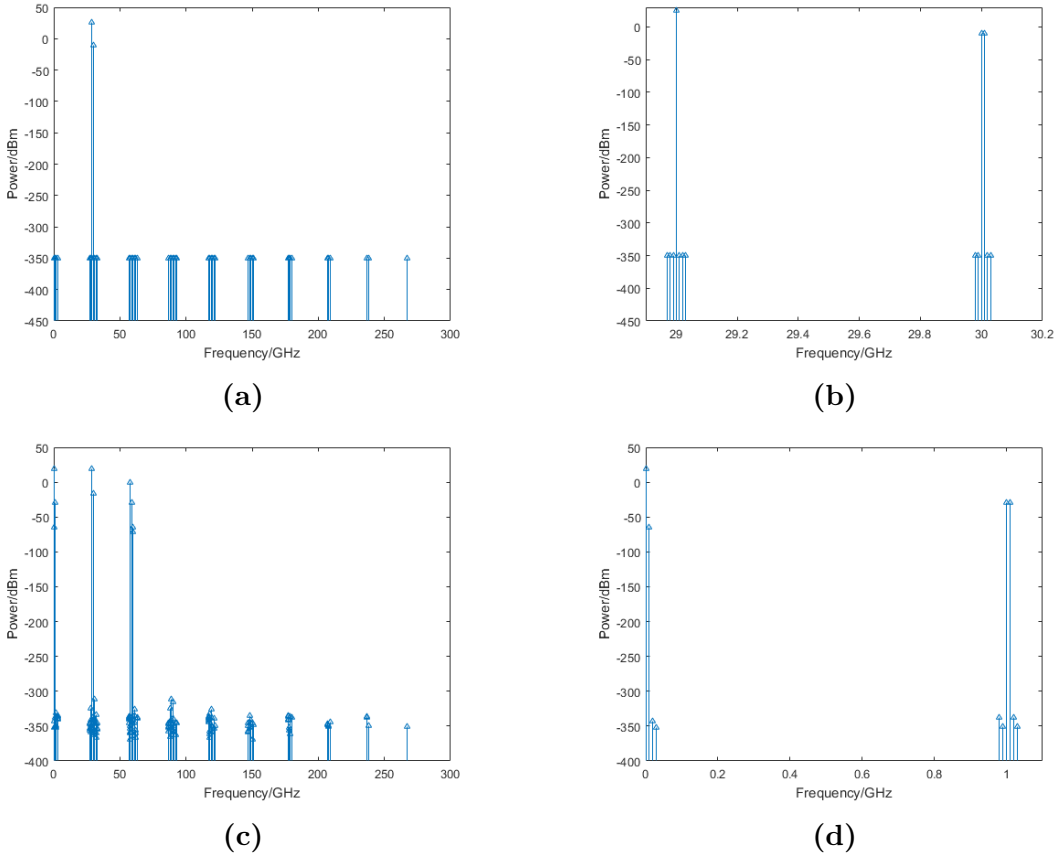
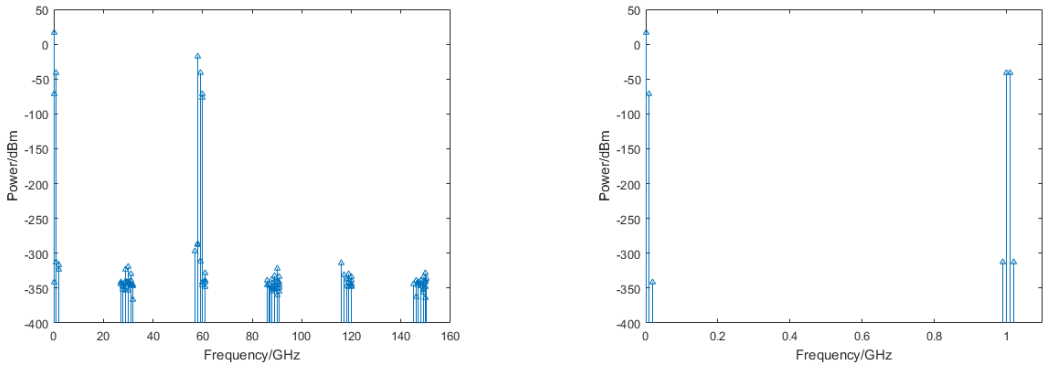


Figure 2.7: (*a*) Spectrum at the RF and LO port for single stack varactor diode topologies. (*b*) Spectrum near the RF and LO frequencies. (*c*) Spectrum at the IF port for single stack varactor diode topologies. (*d*) Spectrum near the IF. (Simulator: ADS)

2.3.1.2 Double Balanced Mixers

Figure 2.8 shows the spectrum at the IF port of the double balanced mixer. According to the spectrum, it can be found out that the RF and LO signals have been compressed. Besides, the second-order frequency components such as $2f_{RF}$, $2f_{LO}$ and $f_{RF} + f_{LO}$ exist at the IF port as well.



(a) **(b)**

Figure 2.8: (a) Spectrum at the IF port for double balanced mixers. (b) Spectrum near the IF . (Simulator: ADS)

2.3.1.3 Triple Balanced Mixers

Figure 2.9 shows the simulation results of the triple balanced mixer. And figure 2.9a is the spectrum at the RF port of the triple balanced mixer. According to this spectrum, it cam be concluded that the LO signal is suppressed at the RF port of the triple balanced mixer. Similarly, as shown in figure 2.9b, it can be found out that the RF signal is suppressed at the LO port of the triple balanced mixer. Therefore, for the triple balanced mixer, the isolation between its RF and LO ports are perfect. Meanwhile, figure 2.9c and figure 2.9d are the spectrum at the IF port of the triple balanced mixer, it can be seen that RF and LO signals are compressed at its IF port. In addition, as shown in the spectrum at the IF port of triple balanced mxiers, most of the second-order frequency components are canceled out due to the triple balanced topologies, the remaining second-order frequency component is $f_{RF} + f_{LO}$.

2.4 Triple Balanced Mixer with Junction Capacitor Diodes

Figure 2.10 shows the simulation results of the triple balanced mixer with junction capacitor diodes. As can be seen from the spectrum, the distortion performance degrades compared with ideal case. However, the mixer still has an IIP3 of 45 dBm, with a conversion loss of 20 dB . Besides, as can be found out from 2.10a, the triple balanced mixer topologies are responsible for the cancellation of all the odd-order harmonics.

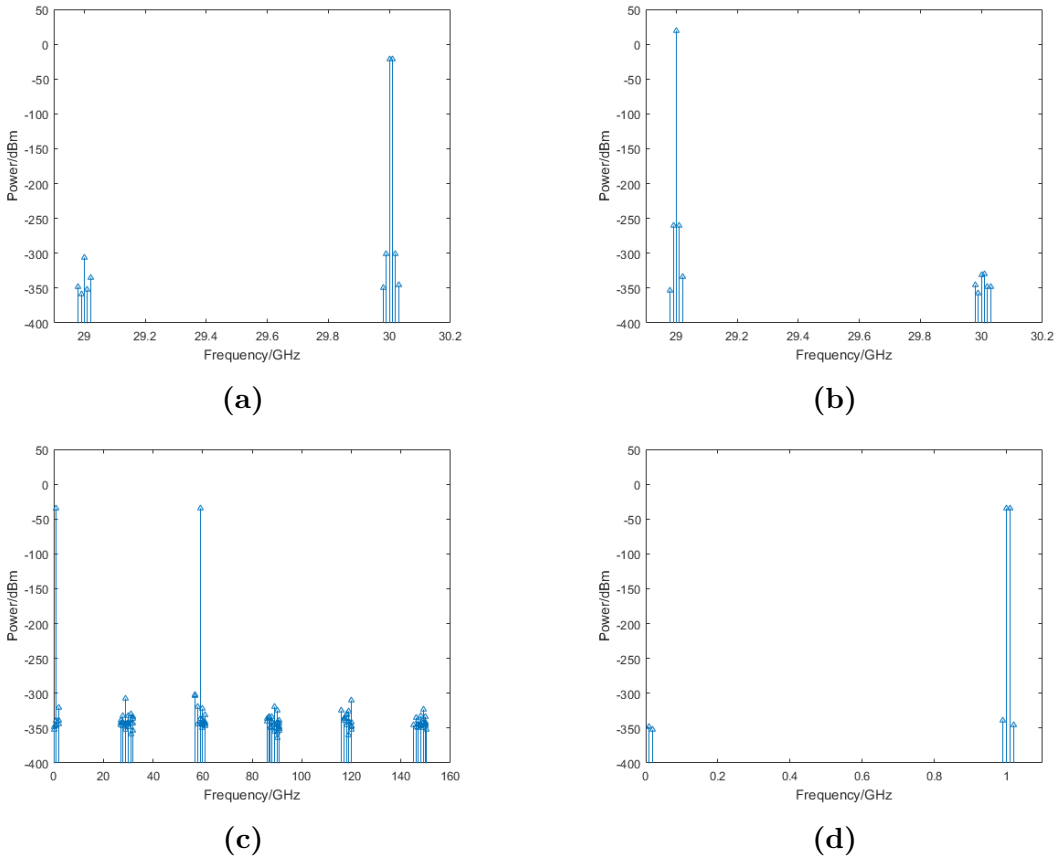


Figure 2.9: (*a*) Spectrum at the RF port for triple balanced mixers. (*b*) Spectrum at the LO port for triple balanced mixers. (*c*) Spectrum at the IF port for triple balanced mixers topologies. (*d*) Spectrum near the IF. (Simulator: ADS)

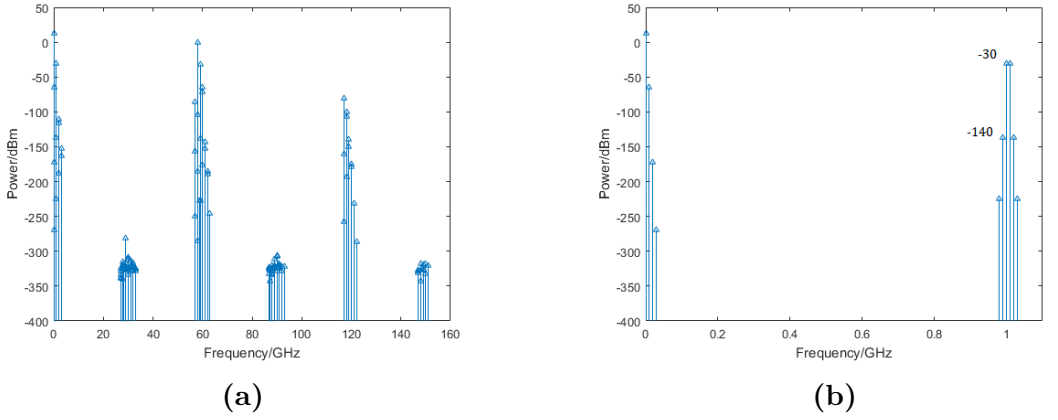


Figure 2.10: (*a*) Spectrum at the IF port for triple balanced mixers. (*b*) Spectrum near the IF. (Simulator: Cadence Virtuoso)

3

Low Noise Amplifiers

3.1 Theory

An LNA is a first circuit block in the receiver architecture, it plays an important role in receiver sensitivity, noise performance and linearity. In order to realize the noise and input matching simultaneously, an inductive emitter-degenerated topology with SNIM technique will be investigated. A cascode structure will also be included in the LNA design to avoid Miller Effect and provide better isolation.

3.1.1 LNA Input Matching Topologies

The input matching is vital for LNA design because an LNA deals with the small signal directly. Since the input of an LNA needs to be connected with an antenna or an external filter, the input impedance of an LNA should be matched to 50Ω. As shown in figure 3.1, resistive termination, shunt-series feedback, common-base input and inductive emitter degeneration are the most common input matching topologies for an LNA.

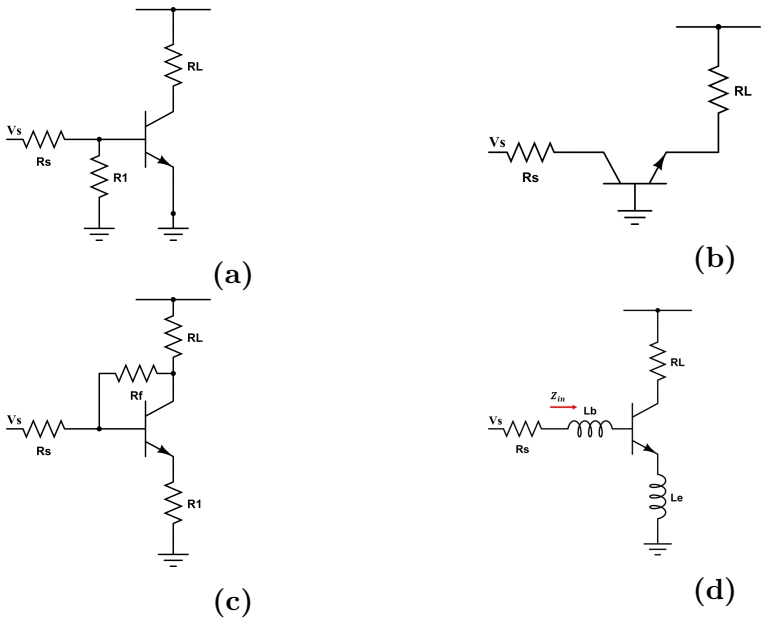


Figure 3.1: (*a*) Resistive termination. (*b*) Common-base input. (*c*) Shunt-series feedback. (*d*) inductive emitter degeneration.

However, for the resistive termination and shunt-series feedback topologies, the noise performance is not promising, due to the thermal noise generated from their input and feedback resistors. While for the common-base input topologies, the impedance looking into their emitter is $1/g_m$, which is determined by the common-base amplifiers' size and bias conditions. The drawback is once the input impedance of a common-base amplifier is fixed, which is 50Ω mostly, its size and bias conditions are fixed too. Unlike the input matching topologies introduced above, the inductive emitter-degenerated topologies have a better input match and noise performance, without the restrictions on g_m [7]. Therefore, it has been implemented in this design.

3.1.1.1 SiGe HBT Noise Figure

As mentioned in [8], for a SiGe HBT, its optimal noise impedance and minimal noise figure can be expressed as:

$$R^{\circ}_{s,opt} = \frac{f_T}{f} \cdot \frac{1}{L_E} \cdot \sqrt{\frac{2r_b L_E kT}{J_C W_E q}}, \tag{3.1}$$

$$NF^{\circ}_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_b} \cdot \sqrt{\frac{1}{\beta} + (\frac{f}{f_T})^2}, \tag{3.2}$$

$$Z^{\circ}_{s,opt} = R^{\circ}_{s,opt} + j \cdot X, \tag{3.3}$$

where L_E and W_E are the emitter length and width respectively, f is the operating frequency, f_T is the cut-off frequency, r_b is the base resistor, J_C is the collector current density, β is the current gain and g_m is the transconductance.

Therefore, by properly choosing the emitter length and width, as well as the bias conditions, the optimal input impedance of an HBT can be tuned to be around 50Ω. However, in order to improve the noise match and the input match of an LNA at the same time, a more complicated technique is often applied.

3.1.2 Simultaneous Noise and Input Matching Technique

As described in last section, SNIM technique is preferred to make input match and noise match simultaneously for LNAs. And this technique can be realized by properly designing the base and emitter inductors of an LNA. As shown in figure 3.1d, by doing nodal analysis, the input impedance of the topology can be expressed as:

$$Z_{in} = \frac{g_m L_e}{C_\pi} + s(L_b + L_e) + \frac{1}{sC_\pi}. \tag{3.4}$$

Therefore, L_e is able to tune the real part of the input impedance closer to 50Ω, meanwhile, L_b helps to cancel out the imaginary part of the input impedance. Also, the optimal noise impedance and minimal noise figure can be re-expressed as:

$$Z_{s,opt} = Z^{\circ}_{s,opt} - s(L_b + L_e) - m \cdot \frac{1}{sC_\pi}, \tag{3.5}$$

$$NF_{min} = NF^{\circ}_{min}, \tag{3.6}$$

where m here is a constant varied with different devices[9].

Therefore, the SNIM technique helps the optimal noise impedance match conjugately to the input impedance of the LNA, i.e. $Z_{s,opt} = Z_{in}^*$.

3.2 Circuit Design

In order to alleviate the Miller Effect and provide better isolation between the input and output of an LNA, the cascode structure is often applied. As mentioned in [9], an external capacitor C_{ex} can be added to an LNA to trade off the noise and gain performance for power dissipation, as shown in figure 3.2b. Thus, it is called Power-constrained Simultaneous Noise and Input matching technique (PSNIM).

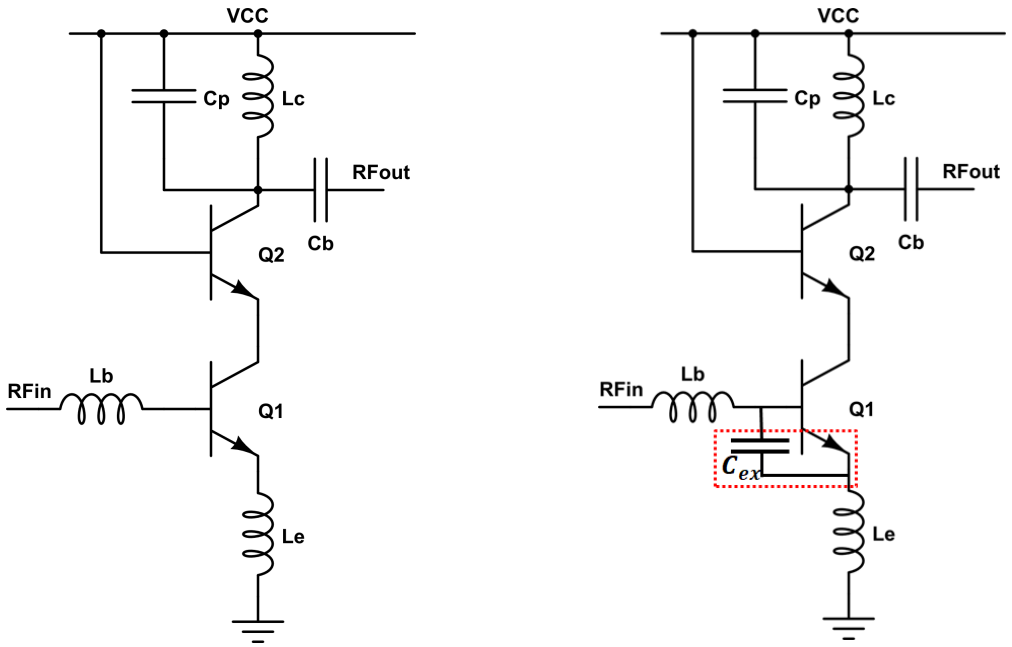


Figure 3.2: (a) Cascode LNA with SNIM technique. (b) Cascode LNA with PSNIM technique.

Table 3.1: Values of components in the circuit shown in figure 3.2

Component	Values
L_e	80 pH
L_b	200 pH
L_c	100 pH
C_p	150 fF
C_{ex}	50 fF

3.3 Results and Discussion

3.3.1 Noise Handling of Multi-finger Transistors

The 130 nm BiCMOS process provides different types of multi-finger transistors. In order to investigate the noise performance of those transistors, noise simulations have been carried out. Meanwhile, the collector current of those transistors was fixed at 6 mA during the simulations. And as shown in figure 3.3, it can be seen that CBEBEBC multi-finger transistor has the best noise performance. Therefore, it has been used in the LNA design.

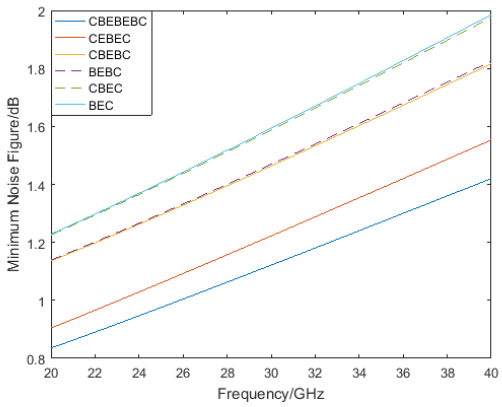
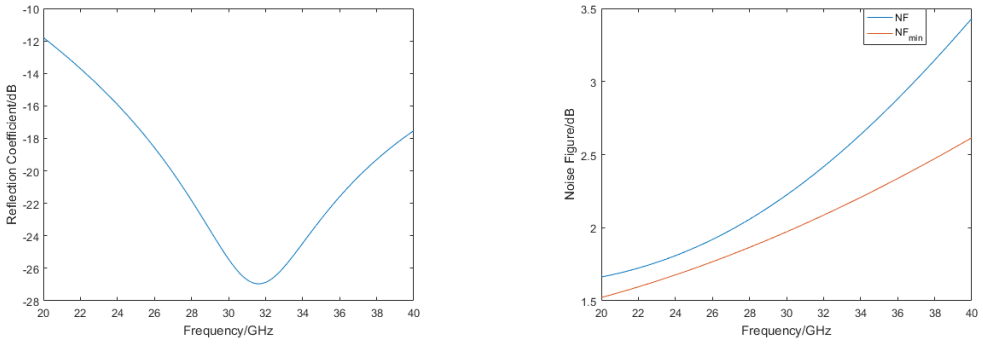


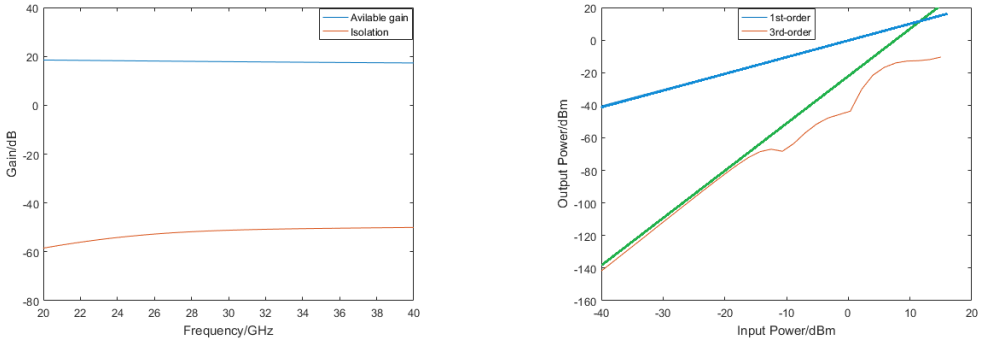
Figure 3.3: Investigation on the noise handling of different multi-finger transistors in the process.

3.3.2 Performance of Cascode LNA with SNIM Technique



(a) **(b)**

Figure 3.4: (*a*) Reflection coefficient of the proposed LNA. (*b*) Actual noise figure and minimal noise figure of the proposed LNA.



(a) **(b)**

Figure 3.5: (a) Available gain and isolation of the proposed LNA. (b) Input $IP3$ of the proposed LNA.

Figure 3.4 and figure 3.5 are the simulation results of the proposed LNA (figure 3.2), as can be found out from the simulation results, within the desired frequency band, the reflection coefficient of proposed LNA is less than -20 dB, the noise figure is less than 2.4 dB, the available gain is more than 17 dB, the isolation is more than 50 dB, the IIP3 is 10 dBm and the power consumption is 12 mW. The results are shown by the table 3.2 as well.

Table 3.2: Performance of Cascode LNA with SNIM Technique

Reflection Coefficient	Available Gain	Isolation	Noise Figure	IIP3	Power Consumption
<-20 dB	>-17 dB	>50 dB	<2.4 dB	10 dBm	12 mW

4

Active Baluns

In a balanced RFIC design, baluns are a critical block. An ideal balun generates differential signals with equal amplitude and 180° phase difference, from the single-ended input signal. In general, there are two types of baluns, i.e. passive and active baluns. For a passive balun, it has been widely used with LC networks or transmission lines. However, for RFIC design, inductors and transmission lines are bulky and lossy. Therefore, an active balun is preferred.

4.1 Theory

As mentioned in [10], there are several types of active balun circuits, namely single FET, common-base common-emitter and differential pair. While the single FET active balun circuits only work for low frequencies. As shown in figure 4.1, two conventional topologies for active balun circuits are introduced. For a common-base common-emitter active balun, its bias conditions are more complicated because its two transistors (Q_1 and Q_2) share the connection of their emitter and base. In addition, these two transistors have to work in a different operating region. Therefore, the differential pair type of active balun has been chosen to be used in the design.

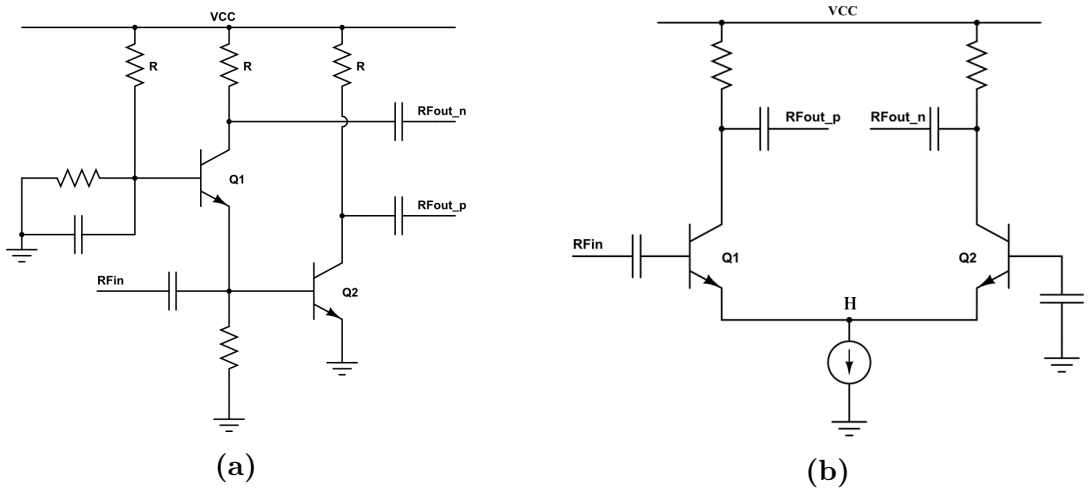


Figure 4.1: (a) Common-base common-emitter active balun. (b) Differential pair active balun.

As shown in figure 4.1b, the differential pair amplifiers are able to convert the single-ended RF input signals to well-balanced output signals, under the conditions

of infinite current source impedance (at node H). However, at high frequencies, due to parasitic effects and finite current source impedance, the amplitude imbalance and the phase error in a differential pair active balun will take place. Therefore, further improvement to this topology to compensate for the amplitude imbalance and the phase error is required. As described in [11] and [12], an active balun with a feedback network has been introduced.

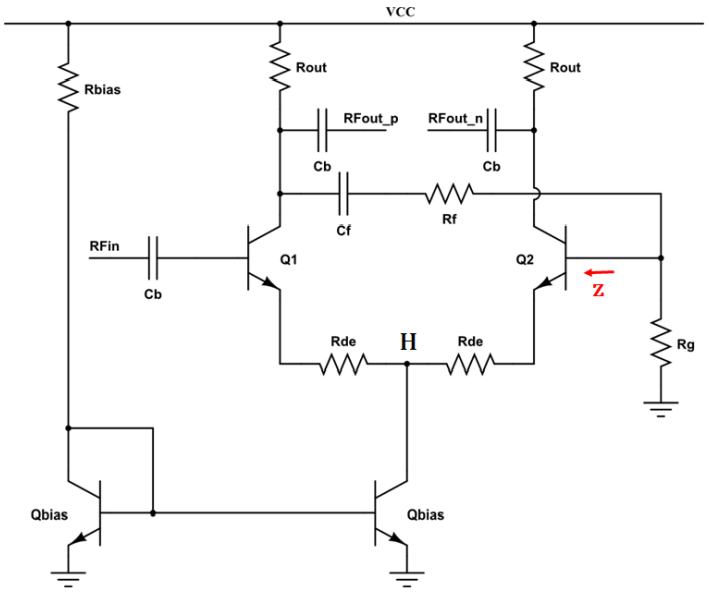


Figure 4.2: Proposed active balun topology with a feedback network.

As shown in figure 4.2, the RC feedback circuit can provide a phase shift to compensate the phase error at the output of the active balun, yielding

$$PhaseShift = 90° - tan^{-1}(R_g C_f \omega). \tag{4.1}$$

Besides, the RC feedback network is able to compensate the amplitude imbalance of a differential pair active balun as well. By doing nodal analysis, the following equation can be obtained:

$$v_{b2} = \frac{R_g//Z}{(R_g//Z) + \frac{1}{\omega C_f} + R_f} \cdot v_{c2}, \tag{4.2}$$

where v_{b2} and v_{c1} are the AC signals at the base of transistor Q_2 and the collector of transistor $Q1$ respectively.

Therefore, from the equations above, the value of C_f and R_g can be set to minimize the phase error at the output of the active balun. And in order to achieve the amplitude balance, properly selection for the value of R_g, C_f and R_f are vital.

4.2 Circuit Design

As described previously, the proposed triple balanced mixer requires two differential RF input signals. However, the passive power splitter is too bulky to be used in

this process. Alternatively, the proposed active balun topology could be duplicated. Therefore, it is able to generate two differential RF signals at its output, as shown in figure 4.3.

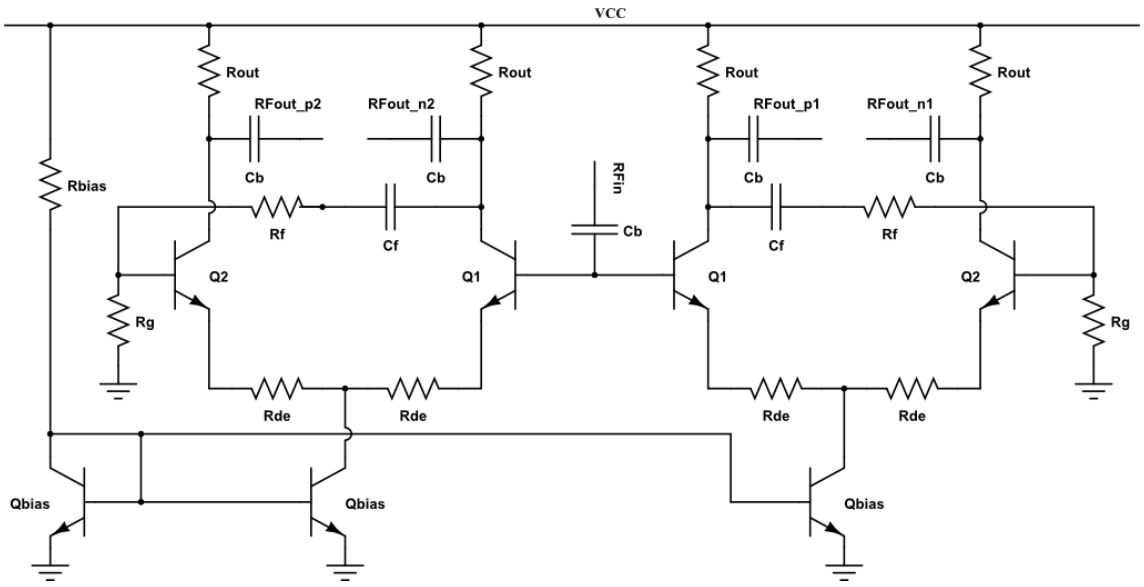


Figure 4.3: Proposed active balun topology with a duplicated structure.

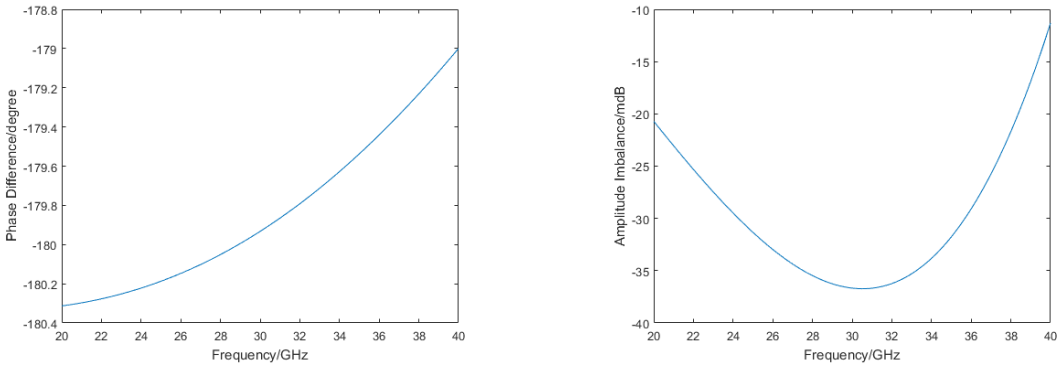
Table 4.1: Values of components in the circuit shown in figure 4.3

Component	Values
R_{out}	170 Ω
R_{bias}	175 Ω
R_g	30 Ω
R_f	50 Ω
R_{de}	5 Ω
C_f	18 fF

4.3 Results and Discussion

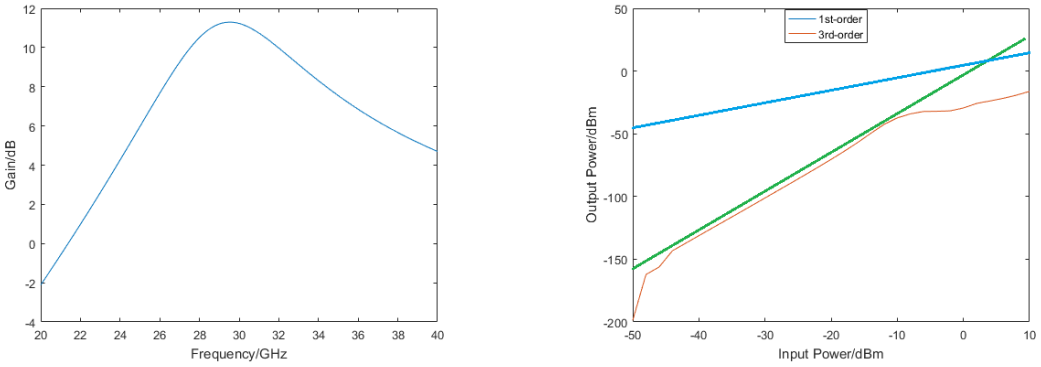
4.3.1 Performance of the Proposed Active Balun

Figure 4.4 shows the simulation results of the proposed active balun, within the 130 nm BiCMOS process. According to the simulation results, it can be concluded that the phase error at the output of proposed active balun is less than 0.5° within the desired frequency band. And the amplitude imbalance is less than 40 mdB. Therefore, the proposed active balun is able to generate differential signal with negligible phase error and amplitude imbalance. In addition, according to the simulation results shown in figure 4.5, the proposed active balun is able to provide more than 8 dB gain and at the same time maintain an IIP3 of 5 dBm.



(a) **(b)**

Figure 4.4: (*a*) Phase difference at the output of the proposed active balun. (*b*) Amplitude imbalance at the output of the proposed active balun.



(a) **(b)**

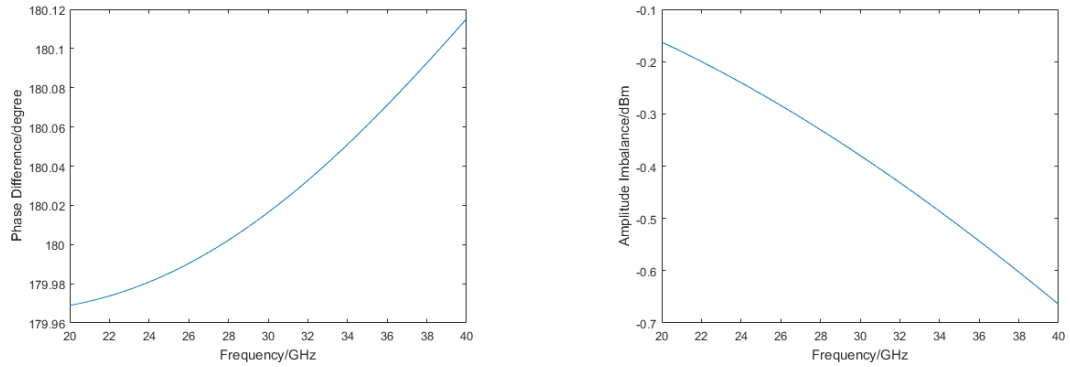
Figure 4.5: (*a*) Gain of the proposed active balun. (*b*) Input $IP3$ of the proposed active balun.

Table 4.2: Performance of the Proposed Active Balun

Phase Error	Amplitude Imbalance	Gain	IIP3
<0.5	<40 mdB	>8 dB	5 dBm

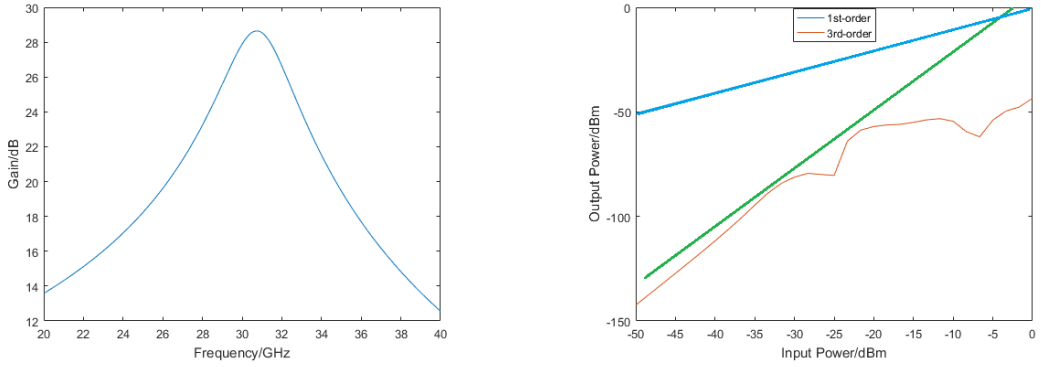
4.3.2 Performance of the Proposed Active Balun with LNA

Figure 4.6 shows the simulation results of the proposed active balun cascaded with the proposed LNA. According to the simulation results, the phase error is less than 0.5° within the desired frequency band. And the amplitude imbalance is less than 500 mdB. Besides, from the simulation results figure 4.7, the proposed active balun cascaded with the proposed LNA is able to provide more than 22 dB gain and at the same time maintain an IIP3 of -4 dBm.



(a) **(b)**

Figure 4.6: (*a*) Phase difference at the output of the proposed active balun. (*b*) Amplitude imbalance at the output of the proposed active balun.



(a) **(b)**

Figure 4.7: (*a*) Gain of the proposed active balun. (*b*) Input $IP3$ of the proposed active balun.

Table 4.3: Performance of the Proposed Active Balun Cascaded with LNA

Phase Error	Amplitude Imbalance	Gain	IIP3
<0.5	<500 mdB	>22 dB	-4 dBm

5

Biasing Techniques

In a receiver front-end circuit design, biasing techniques are vital, because the power-supply variation is able to significantly affect the DC operating point of an LNA, thus affecting its gain, linearity and noise performance. Besides, the temperature variation could also degrade its performance. Therefore, it is important to create a reference voltage and current with well defined values in analog integrated circuit design.

5.1 Theory

5.1.1 Self-biasing

As demonstrated in [13], there are some supply-insensitive biasing circuits such as the Widlar current source, the base-emitter referenced current source and the threshold referenced current source. However, those circuits are not completely power-supply independent. In order to design a circuit with power-supply independent characteristics, the self-biasing circuit is required.

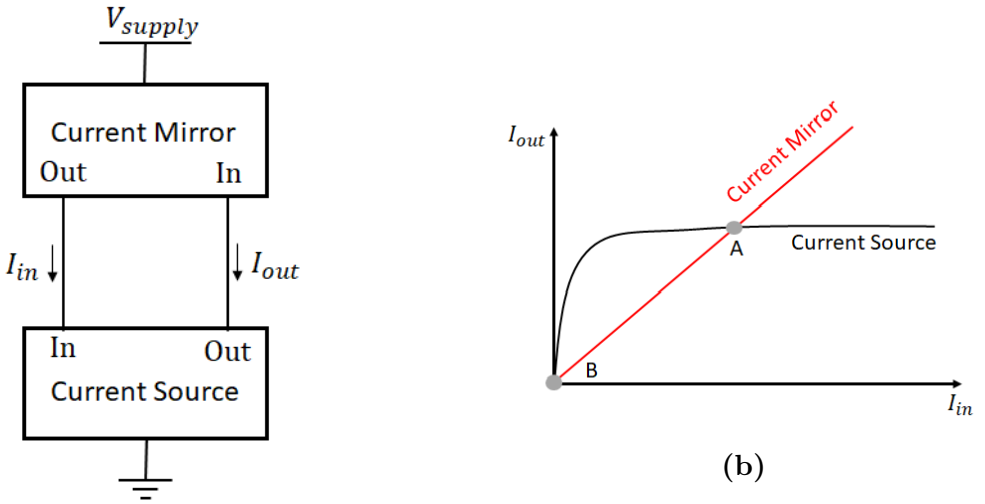


Figure 5.1: (a) Block diagram of self-biasing reference circuit. (b) Operating point of self-biasing reference circuit.

When the I_{out} from figure 5.1a increases, the unit-gain current mirror will increase

the I_{in} by the same amount, then the current source will also increase its output current. Therefore, the output current generated by the current source is able to compensate for the initial change.

As figure 5.1b shows, there are two operating points in a self-biasing circuit, where point A is the desired operating point. However, in practice, a self-biasing circuit tends to work at operating point B, which will cause the self-biasing circuit operate in a zero-current condition. Therefore, a start-up circuit is often applied to help the self-biasing circuit to avoid working under this condition.

5.1.2 Bandgap Reference

Bandgap reference circuits utilize Proportional to Absolute Temperature (PTAT) and Complementary to Absolute Temperature (CTAT) to generate the constant reference, independent of temperature as shown in figure 5.2. In addition, it contains self-biasing circuits, thus the bandgap reference circuits is also independent of power supply.

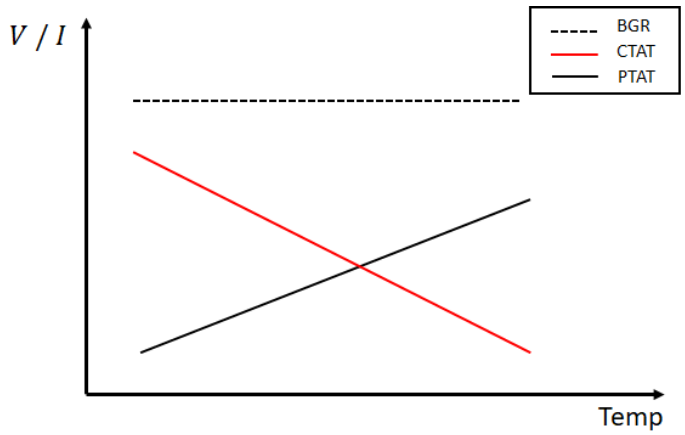


Figure 5.2: Demonstration of proportional to absolute temperature (PTAT), complementary to absolute temperature (CTAT) and bandgap reference (BGR).

As shown in figure 5.3a, the diode voltage can be written as:

$$V_D = iV_T ln(\frac{I_D}{I_S}), \tag{5.1}$$

where $V_T = \frac{kT}{q}$ is the thermal voltage, i is the ideal factor, which is typically between 1 and 1.5 in diodes[13], so i will be assumed to be unit in the following context and I_s is the reverse bias saturation current.

By differentiating V_D over T, it can be easily found out that V_D is a CTAT voltage. In addition, from figure 5.3b, PTAT voltage can be generated by:

$$V_D - V_{D1} = V_T ln(\frac{I_D}{I_S}) - V_T ln(\frac{I_D}{nI_S}) = V_T ln(n), \tag{5.2}$$

Based on the PTAT and CTAT topologies shown in figure 5.3, the bandgap voltage reference circuit can be designed.

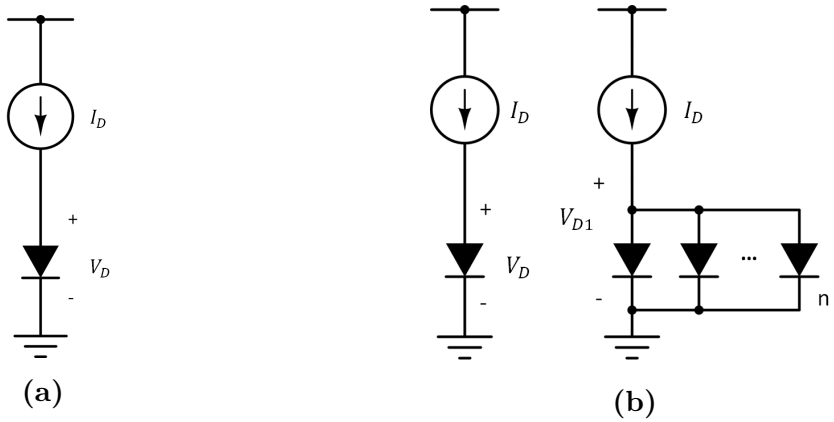


Figure 5.3: (a) Block diagram of self-biasing reference circuit. (b) Operating point of self-biasing reference circuit.

5.2 Circuit Design

From figure 5.4, similar with quation (5.2), I_0 can be written as:

$$I_0 = \frac{V_D - V_{D1}}{R_1} = \frac{V_T ln(n)}{R_1}, \tag{5.3}$$

yielding

$$V_{R2} = \frac{R_2}{R_1} V_T ln(n). \tag{5.4}$$

Therefore, V_{R2} is a PTAT voltage and by properly selecting the value of R_1 and R_2, the bandgap voltage reference V_{ref} can be determined, which is around $1.2V$.

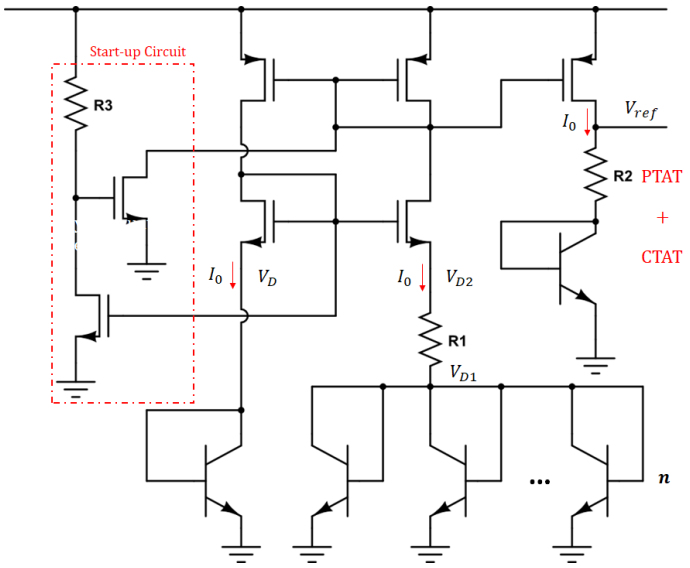


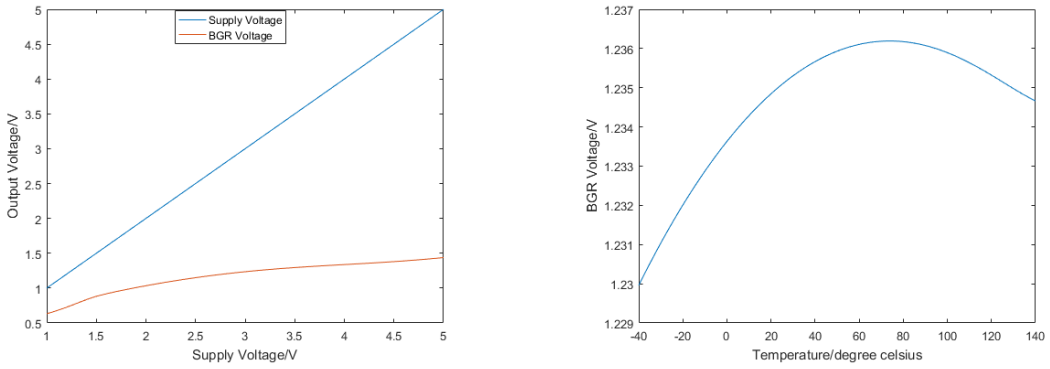
Figure 5.4: Demonstration of proportional to absolute temperature (PTAT), complementary to absolute temperature (CTAT) and bandgap reference (BGR).

Table 5.1: Values of components in the circuit shown in figure 5.4

Component	Values
R_1	500 Ω
R_2	5000 Ω
R_3	1000 Ω
n	2

5.2.1 Results and Discussion

Figure 5.5 is the simulation results of the proposed bandgap reference circuit, the bandgap reference voltage is almost independent of supply voltage and temperature variation, with the value of 1.23 V. Furthermore, the bandgap reference circuit can be utilize to bias the LNA and the active balun. Because they deal with the small receiving signals directly, and the small receiving signals are sensitive to the drift of bias conditions from the amplifiers, caused by the supply power or temperature variation.



(a) **(b)**

Figure 5.5: (*a*) Bandgap reference voltage versus voltage supply. (*b*) Bandgap reference voltage versus temperature.

6
Final Layout

The final layout prototype has been designed by using Cadence Virtuoso Layout Editor under the 130 nm BiCMOS process. The size of the chip is 0.9 mm×0.7 mm.

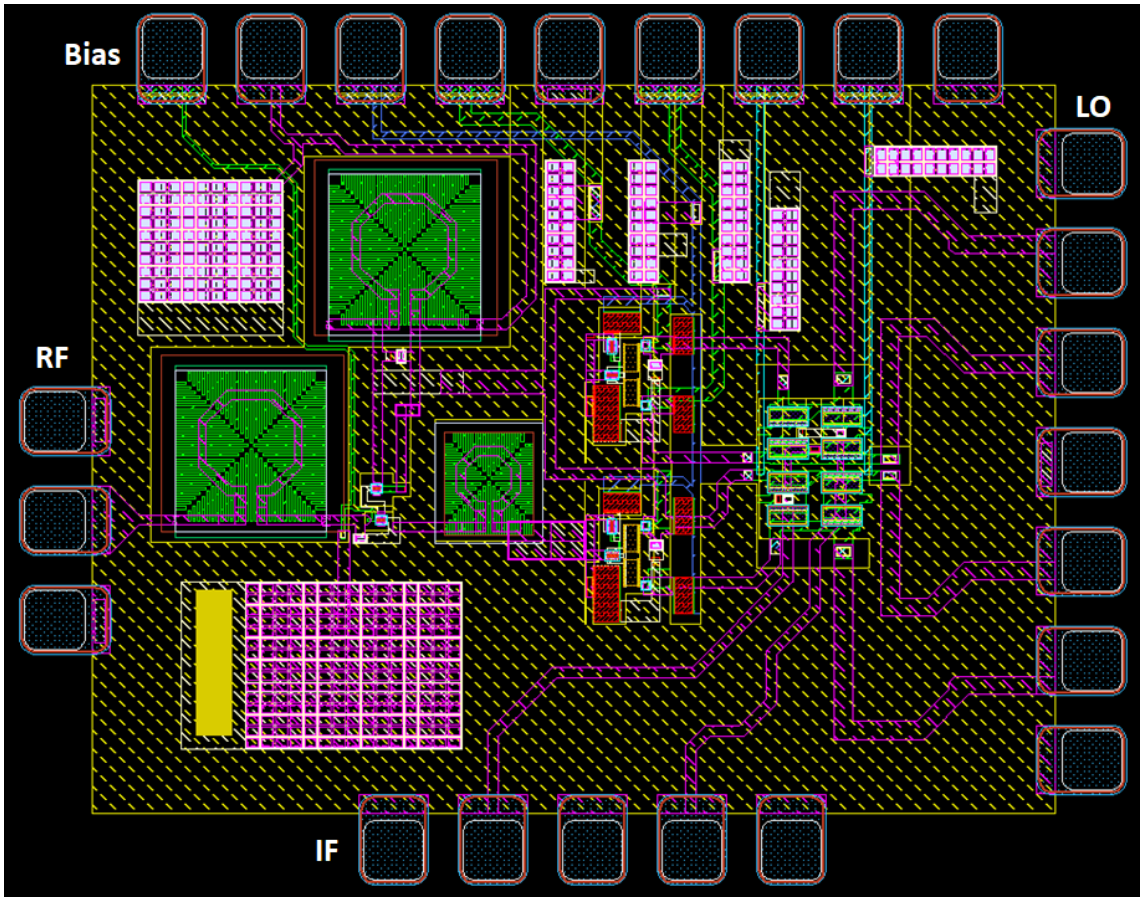


Figure 6.1: Final layout of the receiver front-end.

7

Conclusion and Future Work

7.1 Conclusion

This thesis has aimed to improved the linearity performance of mm-wave receiver front-ends for future multi-antenna communication systems. A 130 nm BiCMOS process has been used in all the designs. Besides, the desired frequency band is 27.5 GHz−32.5 GHz.

A distortion cancellation topology of mixers has been demonstrated in chapter 2. The mixer has been realized by using stack varactor diodes with a triple balanced topology. The analysis of the mixer circuit using Taylor and Volterra series has been presented. Furthermore, the mixer has been implemented in a BiCMOS process and the simulation results of its IIP3 and conversion loss are 45 dBm and 20 dB respectively.

In Chapter 3, an inductive emitter-degenerated cascode LNA with SNIM technique has been investigated and designed. Simulation results show that the LNA achieves a reflection coefficient of less than -20 dB, an available gain of more than 17 dB, a noise figure of less than 2.4 dB, an IIP3 of 10 dBm and a power consumption of 12 mW.

In order to support the balanced mixer topology, a differential-pair active balun with a feedback network has been studied and designed in chapter 4. The active balun has a maximum phase error of 0.5° and an amplitude imbalance of less than 40 mdB. In addition, it provides a gain of more than 8 dB and an IIP3 of 5 dBm. Furthermore, simulation results show that the active balun cascaded with LNA achieves a maximum phase error of 0.5° and an amplitude imbalance of less than 500 mdB. And it provides a gain of more than 22 dB and an IIP3 of -4 dBm.

Biasing techniques including self-biasing and bangap reference circuits have been studied and simulated in Chapter 5. Finally, in Chapter 6, the final layout prototype of the front-end has been designed with Cadence Virtuoso Layout Editor, the total size of the chip is 0.9 mm×0.7 mm.

7.2 Future Work

An IF amplifier with high input impedance and a LO amplifier with focus on creating largest voltage swing are important to be co-designed. In addition, to further improve the linearity of the receiver front-end, an LNA with distortion cancellation topologies should be investigated and designed.

The work done in the biasing techniques requires further expansion. Integrating the presented bandgap reference circuit with the front-end and investigating the performance are of importance.

Further improvements and refinement are required for the layout to pass the DRC and EM simulations.

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