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Investigation of different 12V DC/DC Topologies and optimum selection for Automotive

Evaluation of improvements for unidirectional and bidirectional DC/DC converters

Master's Thesis in Electrical Power Engineering

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CHALMERS UNIVERSITY OF TECHNOLOGY
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Abstract

In the past decade, the focus on technology for a sustainable society has accelerated, leading to new advancements in the automotive sector. Due to the strict emission reduction rules in the European union (EU), the transportation industry shifts toward electric vehicles which have driven significant technological advancements and increased the importance of DC/DC converters for energy conversion.

In this thesis, an extensive research has been conducted to investigate both resonant converters and non-resonant DC/DC converters suitable for the low voltage side. The focus was primarily on several topologies based on the full-bridge configuration, namely the Dual Active Bridge (DAB), Phase-Shifted Full-Bridge (PSFB), and Phase-Shifted Full-Bridge with Current Doubler Rectification (PSFB-CDR). The analysis included a comprehensive investigation of the losses associated with these topologies under various load conditions. Furthermore, the study investigated the impact of using different semiconductor materials, such as Gallium Nitride (GaN) and Silicon Carbide (SiC), on the losses experienced in the converters. This investigation highlighted the behavior of the losses and their relationship to the semiconductor material selection. Based on the findings, a range of potential improvements were suggested to enhance the overall efficiency of the converters. These recommendations aimed to optimize the performance and minimize losses, taking into account the specific characteristics of each topology. Lastly, the thesis included a comprehensive cost analysis of all the investigated topologies. This analysis involved evaluating the unit costs of individual components as well as calculating the total cost considering the entire system. By considering cost implications alongside performance improvements, a comprehensive understanding of the feasibility and economic sustainability of each topology was achieved.

Keywords: Electric vehicles, resonant & non-resonant DC/DC converters, PLECS, Semiconductors, Gan, SiC, DAB, PSFB, CDR.

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Valdrin Thaqi & Abshir Omar Hasan, Gothenburg, June 2023

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

ADAS	Advanced Driver Assistance Systems
APM	Auxiliary Power Module
CDR	Current Double Rectifier
DAB	Dual Active Bridge
ECU	Electronic Control Unit
EMI	Electromagnetic Interferenc
EPS	Extended Phase Shift
EV	Electric Vehicle
HV	High Voltage
LCC	Life Cycle Cost
LV	Low Voltage
MFPT	Medium-Frequency Power Transformer
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PSFB	Phase Shifted Full-Bridge
PWM	Pulse Width Modulation
SOC	State-of-charge
SPS	Single Phase Shift
SR	Synchronous Rectification
THD	Total Harmonic Distortion
TIM	Thermal Interface Material
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Contents

1

Introduction

1.1 Problem background

Over the past ten years, the technology behind a sustainable society has been a crucial issue. A worldwide climate change agreement was reached in Paris in 2015 by a large number of countries, with the goal of limiting global warming considerably below 2°C compared to pre-industrial levels, with a 1.5°C target [1]. As one of the largest users of fossil fuels, the transportation industry significantly contributes to the global overall greenhouse gas emissions [1]. To fulfil the climate agreement, decision makers have emphasized to automobile manufacturers to focus on electric vehicles (EV) in response to rising demand for environmentally friendly and improved fuel economy automobiles [2]. Thus, the automotive sector is undergoing significant technology improvements in order to transit to pure electric propulsion and bring, safe, comfortable and environmental friendly vehicles [3].

The fundamental parts of the EV are battery systems, charging stations, and power electronics [3]. The development of power electronic converters is essential to ensure smaller, lighter, and less expensive converters while maintaining high efficiency and high reliability [4]. Power electronics are key factors for the creation of propulsion systems for electric and hybrid vehicles, hence the power converter have a significant influence in improving performance [5].

The classification of power electronic converters is wide, as shown in Figure 1.1. Consequently, this master's thesis will focus on the study of different power electronic topologies suitable for EV applications on the low voltage (LV) side, with an emphasis on both bidirectional and unidirectional galvanic isolated DC/DC converters. These converters play a crucial role in the EV system as they enable energy transmission between different components of the vehicle by connecting various voltage busses. They not only ensure efficient energy transfer but also protect the LV electronic system from potentially hazardous excessive voltage [6]. The high voltage (HV) battery in figure 2.1 discharges through the low voltage DC/DC converter which in turn charges the auxiliary battery, which is referred to as an auxiliary power module (APM) in the literature [7]. The APM provides power to lighting, electronic control units, wiper and window system, and other accessory loads [7].

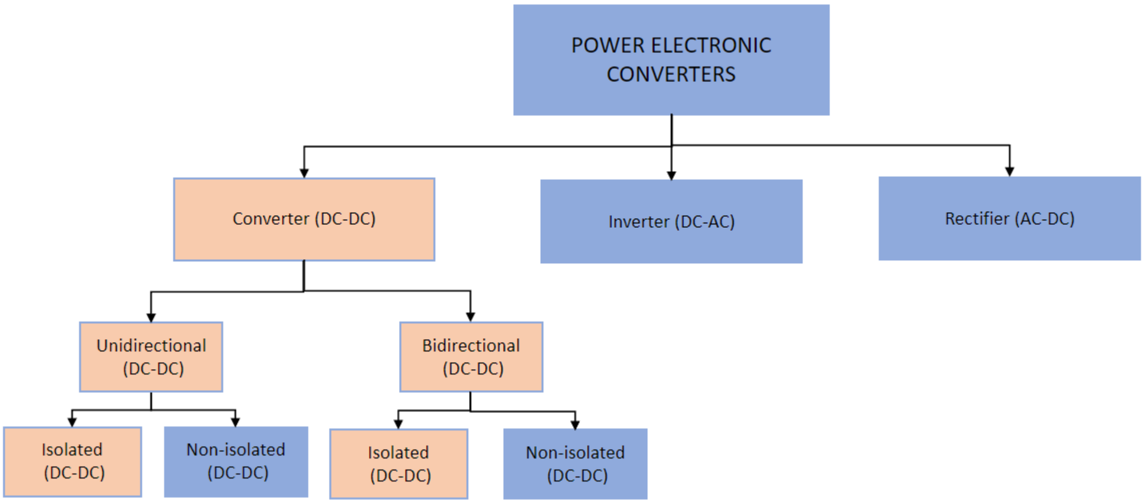


Figure 1.1: Classification of power electronic converters

1.2 Aim

The aim of the project is to investigate galvanicly isolated DC/DC topologies for the low voltage side of the EV DC/DC conversion unit and develop a model which investigates improvements that can be made. Evaluation of topology, semiconductor devices and transformers will be made through simulations with data to meet the requirements from CEVT.

1.3 Scope

A model of a battery discharging through the low voltage DC/DC converter will be made and evaluated with PLECS for an autonomous vehicle. Different topologies with different power electronic devices will be tested and compared to find suitable improvements which increases efficiency or reduces cost. A closed loop control will be designed to keep the output voltage to a fixed 12V regardless of the power demand. The model of the battery will reflect the decrease in voltage output as the state-of-charge (SOC) decreases to get a more realistic model.

Delimitation's of the project will be to not investigate thermal stress on the semiconductor devices, which means that lifetime will not be taken into consideration in the cost evaluation.

1.4 Previous work

Ongoing research and development in the field of auxiliary DC/DC converters for automotive applications reflects the increasing demand for auxiliary power in modern cars, which varies depending on the specific features and systems installed. Generally, newer cars tend to have more advanced and power-demanding systems, such as infotainment systems, and advanced driver assistance systems (ADAS), which require more auxiliary power to operate effectively [6, 7].

Given the high power requirements of the APM, current research primarily focuses on designing APMs with power ratings around 3kW [6]. Moreover, due to their higher power density, current DC/DC converter development for APMs is based on the phase-shifted full-bridge topologies, such as Resonant Converters, Dual Active Bridge and Triple Active Bridge [7].

2

Theory

2.1 Overview of the model

The overview of the model is seen in figure 2.1. The HV battery is discharged through the bus and feeds the LV system and the propulsion motor. The HV battery is connected to the LV system through a 400V/12V unidirectional DC/DC converter with galvanic isolation. It keeps the SOC of the auxiliary battery between 80-100% at all times since it is intended to work when the vehicle is turned off. The possibility of using the 12V auxiliary battery to feed the electric machine (EM) at the worst case scenario for propulsion will be investigated, which is at HV battery failure. Thus, the topologies for bidirectional power converters are also covered in the project.

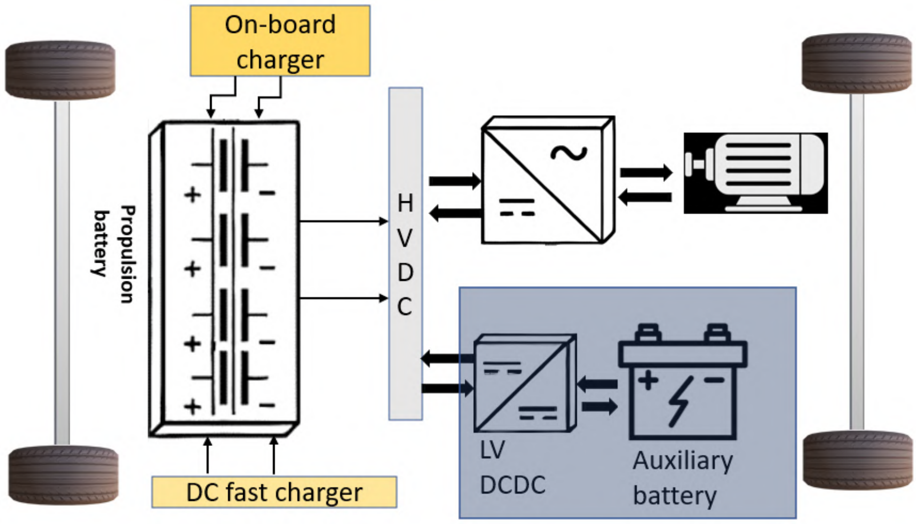


Figure 2.1: Overview of the electrical power-train

2.2 Unidirectional & Bidirectional

Unidirectional DC/DC topologies are power converter configurations that enable power flow in a single direction, typically from the input to the output. These converters have mainly active devices (MOSFETs) on the primary side and passive components (diodes) on the secondary side.

While bidirectional power converters allows power transfer from HV to LV side and vice versa. They are composed of additional active semiconductor devices and a more complex control system. This project focuses on the phase shifted full-bridge topologies, since they are commonly used in the industry at high voltage levels.

2.2.1 Full-Bridge converter

The full-bridge converter is derived from the buck converter [8]. It utilizes a transformer to provide a galvanic isolation and the working concept is stepping up or down the input voltage. Since the full-bridge is suitable for high power applications requiring more than 1 kW and concurrently offers great efficiency and outstanding reliability, high density of power and efficiency, it is preferred in EV applications [9, 10]. The full-bridge converter's circuit is illustrated in figure 2.2, which includes a voltage source, four switches on the primary side, two diodes, an inductor, a capacitor and a load resistance and the secondary side of the transformer. The switches operate in pairs, which is also called bipolar switching. Thus, S1 and S4 operate concurrently during a particular duty ratio, and S2 and S3 operate concurrently during a particular duty cycle ratio [9]. The output voltage can be adjusted by adjusting the phase shift between the switches and the transformers turns-ratio. The diodes D1 and D1 conduct alternately and block when the switch pairs are on alternately, while when both switch pairs are off, both diodes conducts. By utilizing a pulse width modulation (PWM) signal, a carrier wave with a constant reference voltage is sent to the switch pairs as shown in figure 2.3. When the carrier wave is greater than the reference voltage, the switches are off, while they conduct during the period the carrier wave is lower than the reference voltage. The following equations describes the necessary steps to carry out calculations for the crucial parameters in the full-bridge converter:
The value of the filter inductance is calculated as follows

$$V_L = L\frac{di_L}{dt} \Rightarrow L = \frac{V_L}{\frac{di_L}{dt}} = \frac{V_L}{\frac{\Delta i_L}{\Delta t}} \tag{2.1}$$

where the Δi_L & Δt represent the ripple current and the on-state time respectively. The filter inductance can be further simplified to

$$V_L = \frac{N_2}{N_1}V_{in} - V_0 \tag{2.2}$$

Where V_0 is the voltage across the load which can be expressed as

$$V_0 = \frac{1}{T_s}\int_0^{T_s} V_{oi}(t)\,dt = \frac{1}{T_s}(2\int_0^{DT_s} \frac{N_2}{N_1}V_{in}\,dt + \int_{DT_s}^{T_s} 0\,dt) = 2\frac{1}{T_s}\frac{N_2}{N_1}V_{in}DT_s = 2V_{in}\frac{N_2}{N_1}D \tag{2.3}$$

Further, the duty cycle D and voltage ripple ΔV_0 are calculated as

$$D = \frac{1}{2}\frac{V_0}{V_{in}}\frac{N_1}{N_2} \tag{2.4}$$

$$\frac{\Delta V_0}{V_0} = \frac{1-D}{8LC(2f)^2} \tag{2.5}$$

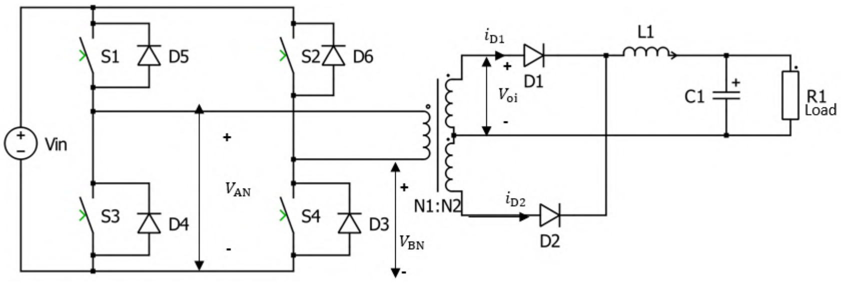


Figure 2.2: Full-bridge converters,

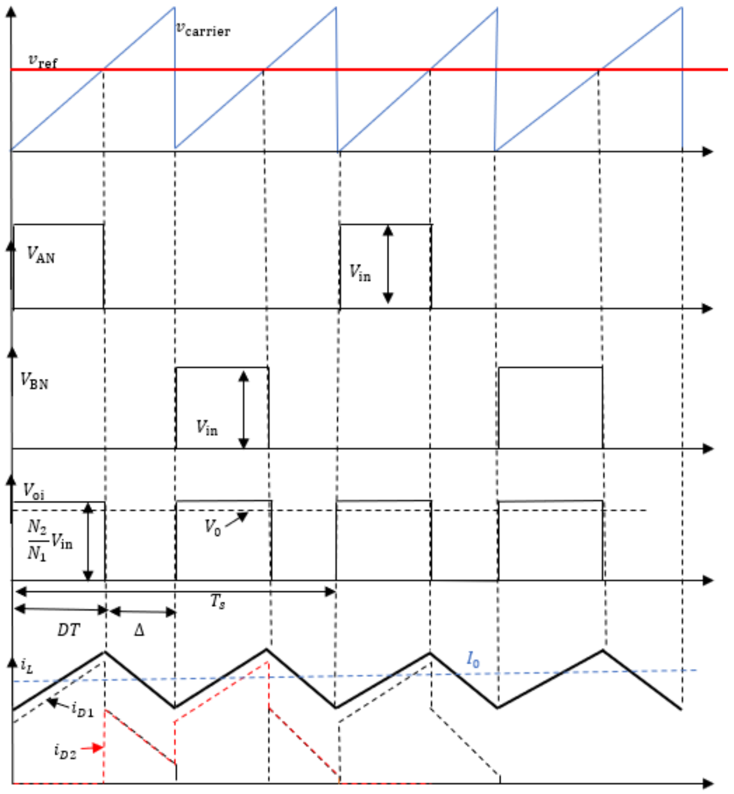


Figure 2.3: Full-bridge converters operational waveforms

2.2.2 Dual Active Bridge - DAB

The 1ϕ -DAB consists of active semiconductor devices in parallel with passive which are further connected in either a half-bridge or full-bridge configuration on both the primary and secondary side of the medium-frequency power transformer (MFPT). This provides the possibility to operate in bidirectional power flow and gives a reduced size of the power converter. It also allows zero voltage switching (ZVS) which reduces the switching losses at turn off. The transistors operate in pairs with a duty cycle of 0.5 in single phase shift (SPS) to get square-wave operation on both the primary and secondary side of the MFPT, with an introduces phase shift, α. In figure 2.4, a full-bridge configuration is seen.

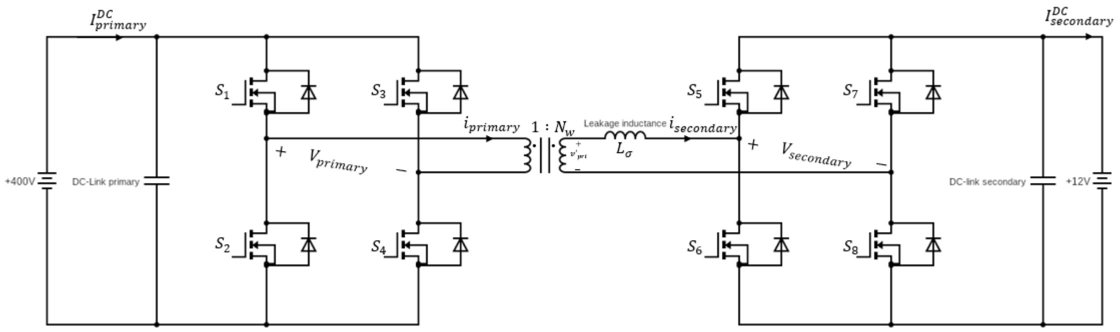


Figure 2.4: Schematic of a full-bridge DAB

The power flow principle of the DAB is easily explained with the lossless and simple figure 2.5 where the magnetizing inductance of the transformer is assumed to be much bigger than the leakage inductance meaning that the no current flows through the magnetizing inductance.

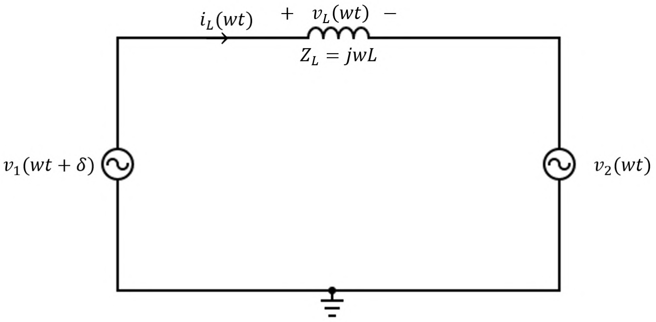


Figure 2.5: Lossless AC-link simplified circuit of DAB

The average power flow is

$$P = \frac{1}{2}\frac{V_1 V_2}{wL} sin(\delta) \tag{2.6}$$

meaning that at $\delta = 0°$ there is no active power flow but only reactive power flowing back and forth as long as $V_1 \neq V_2$. P_{max} is achieved at $\delta = 90°$ when $V_1 \neq V_2$ and by assuming constant voltages where $V_1 > V_2$, the direction of the power flow depends on the phase angle which is controlled with modulation techniques with up to three degrees-of-freedom.

2.2.2.1 Modulation techniques

There are four main modulation techniques used for the DAB with up to three degrees-of-freedom.

- Single Phase Shift(SPS) - 1-DoF
- Extended Phase Shift(EPS) - 1-DoF
- Double Phase Shift(DPS) - 2-DoF
- Triple Phase Shift(TPS) - 3-DoF

This project focuses on the SPS and EPS modulation techniques.

2.2.2.1.1 SPS The SPS is the simplest to control but also the one with the most circulating currents leading to greater losses. It has one degree-of-freedom which is controlling the switches on only the primary or secondary side of the MFPT.

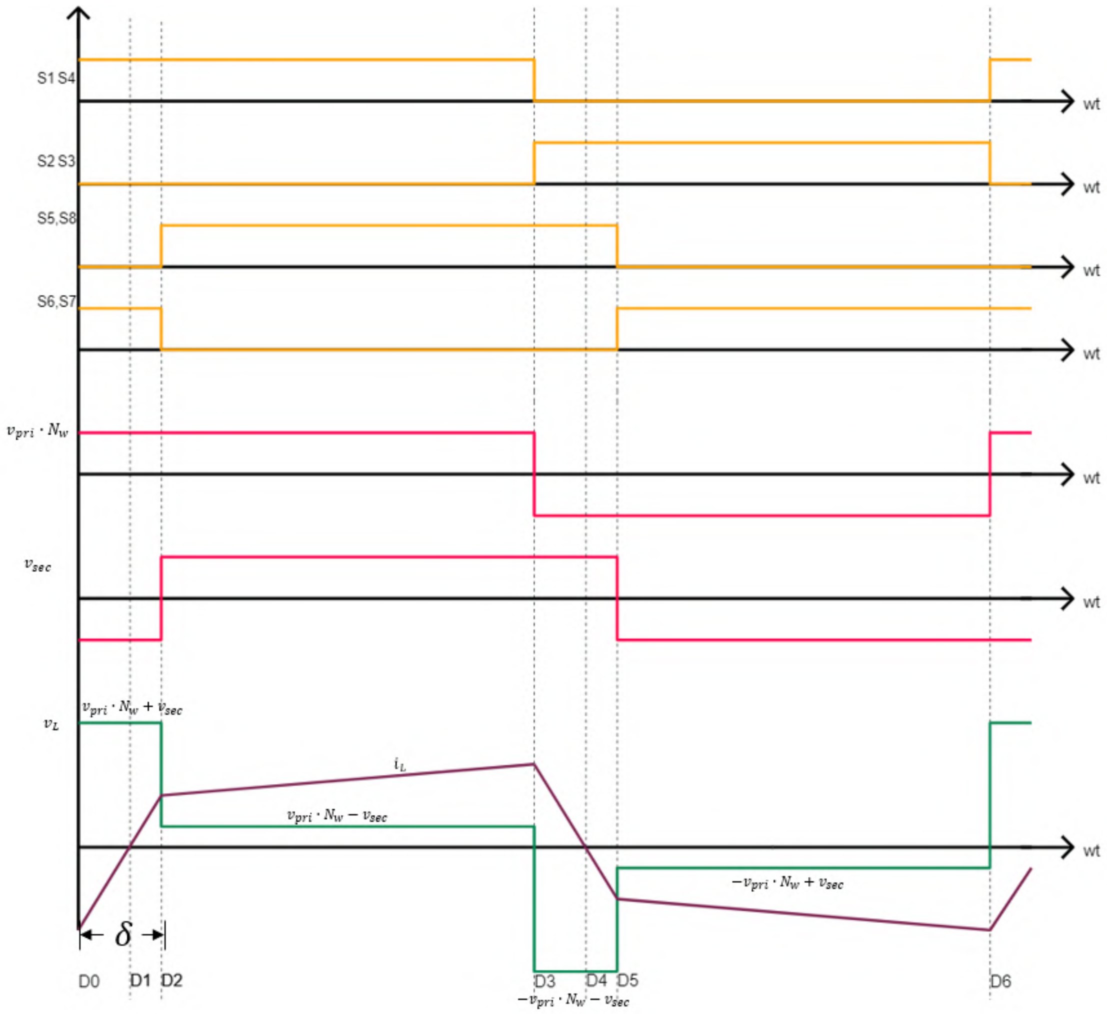


Figure 2.6: Waveforms for 1ϕ-DAB operating in SPS when $N_w \cdot V_1 > V_2$

The SPS operates with a duty cycle of 0.5 on both the primary and secondary side as seen in figure 2.6. The AC-link voltages are the red curves which gives the green voltage curve over the leakage inductance.

$$v_L = N_w \cdot v_{primary} - v_{secondary} \tag{2.7}$$

The current flowing through the transformer, i_L, has four $\frac{di}{dwt}$ corresponding to the voltage across it.

- **Region I:** $0 \leq wt \leq \delta$

$$i_L(wt) = i_L(0) + \frac{N_w \cdot V_{pri} + V_{sec}}{wL}(wt - 0) \tag{2.8}$$

- **Region II:** $\delta \leq wt \leq \pi$

$$i_L(wt) = i_L(\delta) + \frac{N_w \cdot V_{pri} - V_{sec}}{wL}(wt - \delta) \tag{2.9}$$

- **Region III:** $\pi \leq wt \leq \pi + \delta$

$$i_L(wt) = i_L(\pi) + \frac{-N_w \cdot V_{pri} - V_{sec}}{wL}(wt - \pi) \tag{2.10}$$

- **Region IV:** $\pi + \delta \leq wt \leq 2\pi$

$$i_L(wt) = i_L(\pi + \delta) + \frac{-N_w \cdot V_{pri} + V_{sec}}{wL}(wt - \pi - \delta) \tag{2.11}$$

The operation principle is described and divided into six segments.

- **Segment I:** D1-D0
  The primary voltage is positive during this segment meaning that the switches S1 and S4 should be conducting. However, the switches are not immediately conducting during this instance since the current i_L is negative meaning that it flows through the diodes D1 & D4. The same logic follows for the secondary side, meaning that the diodes D6 & D7 are conducting.
- **Segment II:** D2-D1
  The current now changes direction and becomes positive while $V_{pri} > 0$ & $V_{sec} < 0$ still has the same polarity since the gate signal have not changed. Since the diodes that were conducting during Segment I now are reversed biased, the switches will take over the current meaning that the voltage across the switches will be zero and ZVS is obtained on both the primary and secondary side.
- **Segment III:** D3-D2
  With the operation mode of $N_w \cdot v_{pri} > v_{sec}$, it is seen from figure 2.6 that the voltage across the inductor still is positive as in the previous segments. The slope $\frac{di}{dwt} = \frac{N_w \cdot v_{pri} - v_{sec}}{wL}$ is reduced due to the changed polarity on the secondary side. The change of polarity implies that the current on the secondary side now flows through the diodes D5 & D8 while S1 & S4 are still on.
- **Segment IV:** D4-D3
  The gate signals on the primary are changed and $\frac{di}{dwt} = \frac{-N_w \cdot v_{pri} - v_{sec}}{wL}$ is negative. The current on the primary now flows through diodes D2 & D3 due to the negative polarity of V_{pri} and the positive current flowing through the transformer. Diode D5 & D8 remains in the same state as in segment III.
- **Segment V:** D5-D4
  The current through the transformer changes direction going from positive to negative. That implies that the switches in parallel to the already conducting diodes takes over the current at zero voltage across them achieving a soft turn-on switching.
- **Segment VI:** D6-D5
  The polarity of the secondary voltage changes to positive and the current on the secondary flows through the diodes D6 & D7. The primary side is unchanged and S2 & S3 still conducts.

The output power using SPS is calculated as

$$P = \frac{N_w V_{pri} V_{sec}}{wL_\sigma}(\delta - \frac{\delta^2}{\pi}) \tag{2.12}$$

The main issues with this modulation technique is as mentioned the circulating currents or the reactive currents due to the magnetic components as the transformer, as well as the condition for soft switching. Thus, EPS modulation technique is more practical due to the partial cancellation of the circulating currents and a wider range of ZVS.

2.2.2.1.2 EPS For the EPS, either the primary or the secondary has a duty cycle D<0.5 meaning that there will be a reduction of voltage across the inductor for a given period. The circulating currents occur when the primary voltage has an opposite polarity compared to the current through the transformer[11]. As seen in the EPS waveforms in figure 2.7, the angle β represents the time where the primary voltage is zero meaning that there will not be any current going back through the transformer. The circulating currents only appears from D1 to D1' for the EPS while for the SPS, they appear through the whole duration of the phase shift, δ.

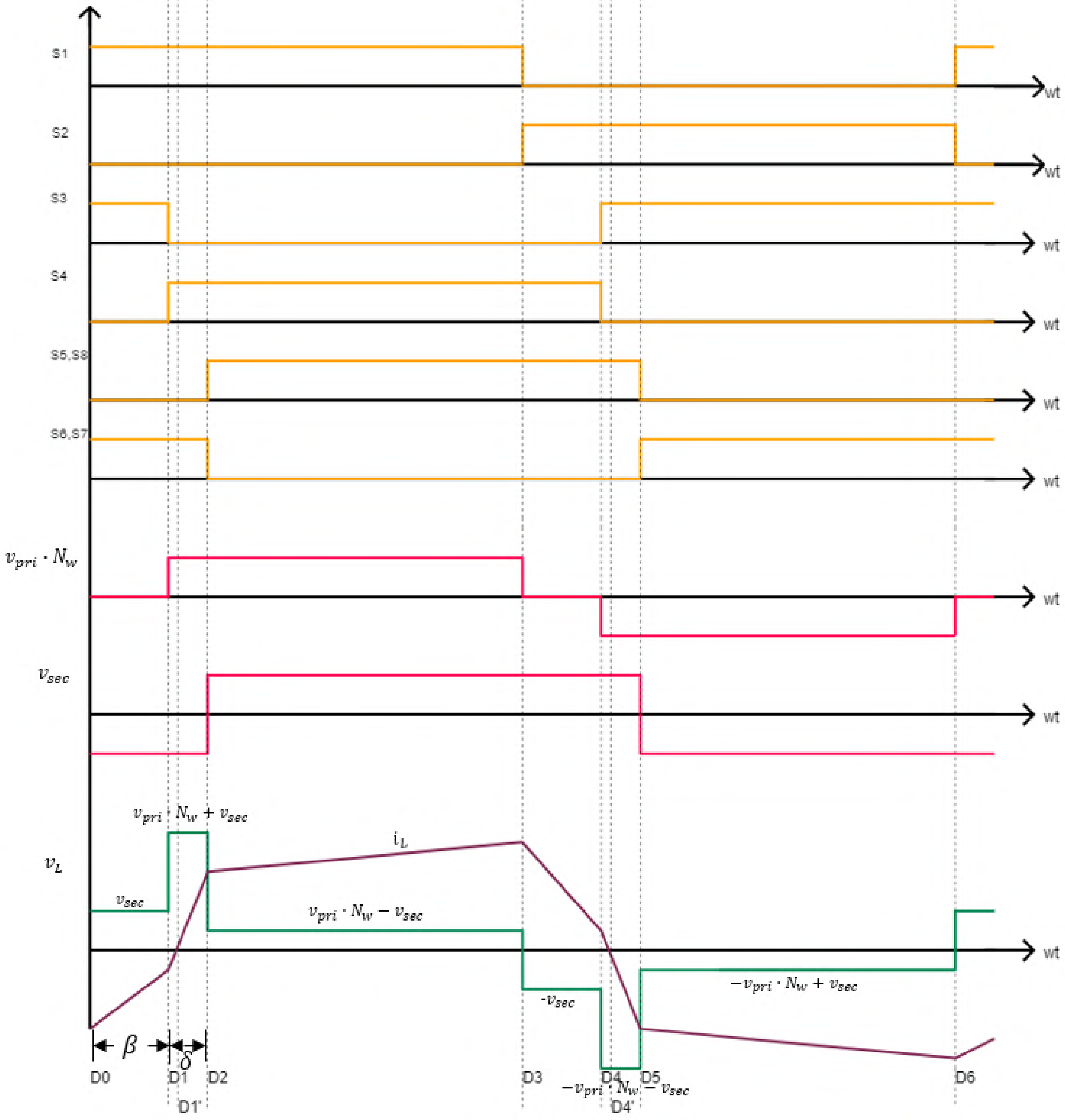


Figure 2.7: Waveforms for 1ϕ-DAB operating in EPS when $N_w \cdot V_1 > V_2$

2.2.3 Phase Shifted Full-bridge

The Phase-Shifted Full Bridge (PSFB) is designed as the full-bridge converter but with different control signal at the gates. The PSFB converter is suitable for applications that require high power. It has a centre-tapped transformer and utilizes the usage of synchronous rectification (SR) by using MOSFETs, as shown in figure 2.8. The SR on the secondary side enables zero voltage switching (ZVS) for all switching components, leading to decreased switching losses [12]. The main advantage of the PSFB compared to the DAB is that it has lower conduction losses since it only passes through one semiconductor at the secondary instead of two. As demonstrated in figure 2.9, with the Phase Shifted method, a delay is added between the turn-on of the two diagonal full bridge switches instead of controlling them simultaneously. Thus, S1 & S2 are 180° phase shifted, similarly for S3 & S4.

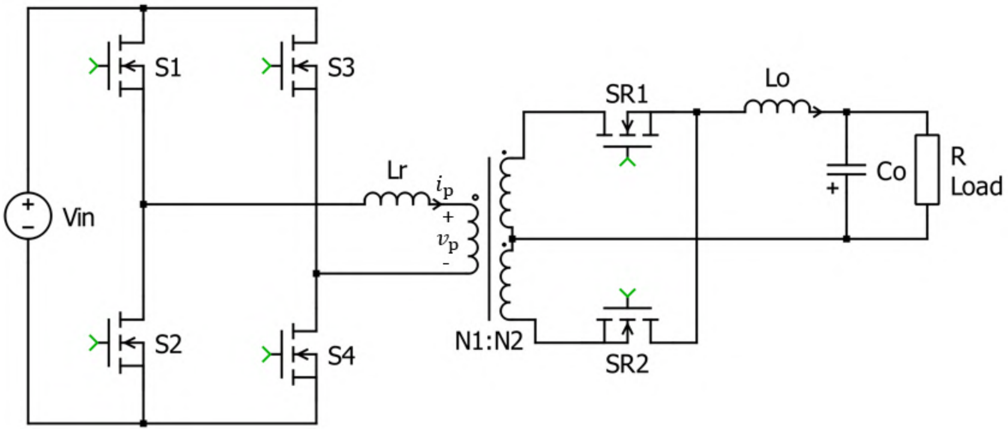


Figure 2.8: Phase shifted Full-bridge circuit,

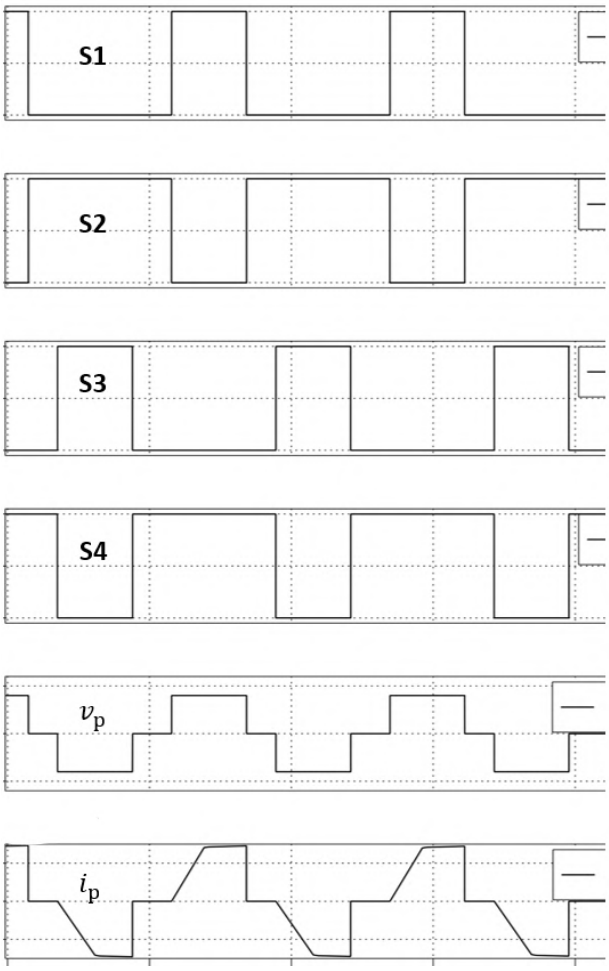


Figure 2.9: Phase shifted Full-bridge circuit,

2.2.3.1 Phase shifted full bridge with Current doubler rectifier

It is commonly known that the PSFB can handle large power output while providing high efficiency, high output current, and low output voltage. However, it introduces high copper losses and switching losses due to its low duty cycle or high turns ratio transformer. In order to overcome these challenges the PSFB is combined with a current double rectifier (CDR) on the secondary side which is demonstrated in figure 2.10. Different designs can be achieved depending on the desired operation where it is possible to exchange the MOSFETs SR1 & SR2 with diodes.

The operational principle and the fundamental waveforms of the converter are demonstrated on figure 2.11. During the time period t_0 & t_1 mode (a) in figure 2.11 is active, the switchers S1 & S4 are thus conducting, and a positive voltage arises on the secondary side of the transformer. During the period when S1 & S4 are conducting, SR1 is off and SR2 is conducting, causing the inductor L_1 to be charged and L_2 to be discharged. Between t_1 & t_2 the freewheeling period is active which is shown in figure 2.11 (b) as a result of S1 and S4 being turned off, this causes that the voltage v_p over the transformer becomes zero. On the load, due to the freewheeling of both L_1 & L_2, SR1 and SR2 are conducting. During t_2 & t_3 S2

& S3 are on as shown in mode (b), resulting in a negative voltage over the secondary side of the transformer. In accordance with this time period, SR1 is active and SR2 is inactive, thus L_2 is being charged and L_1 being discharged. In mode (d) which occur during the time frame t_3 & t_4, S2 & S3 are turned off. During this period t_3 & t_4 the voltage v_p is zero, and due to the freewheeling of L_1 & L_2, SR1 and SR2 are turned on.

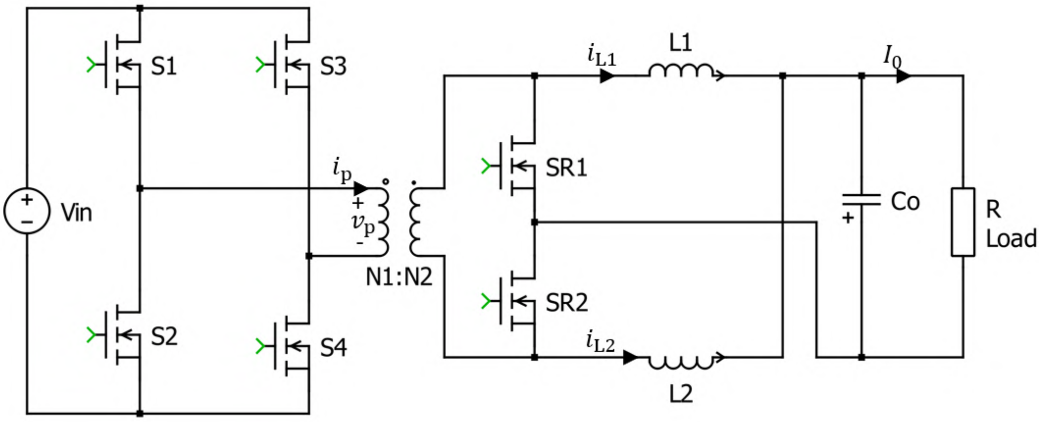


Figure 2.10: Phase shifted Full-bridge CDR converters,

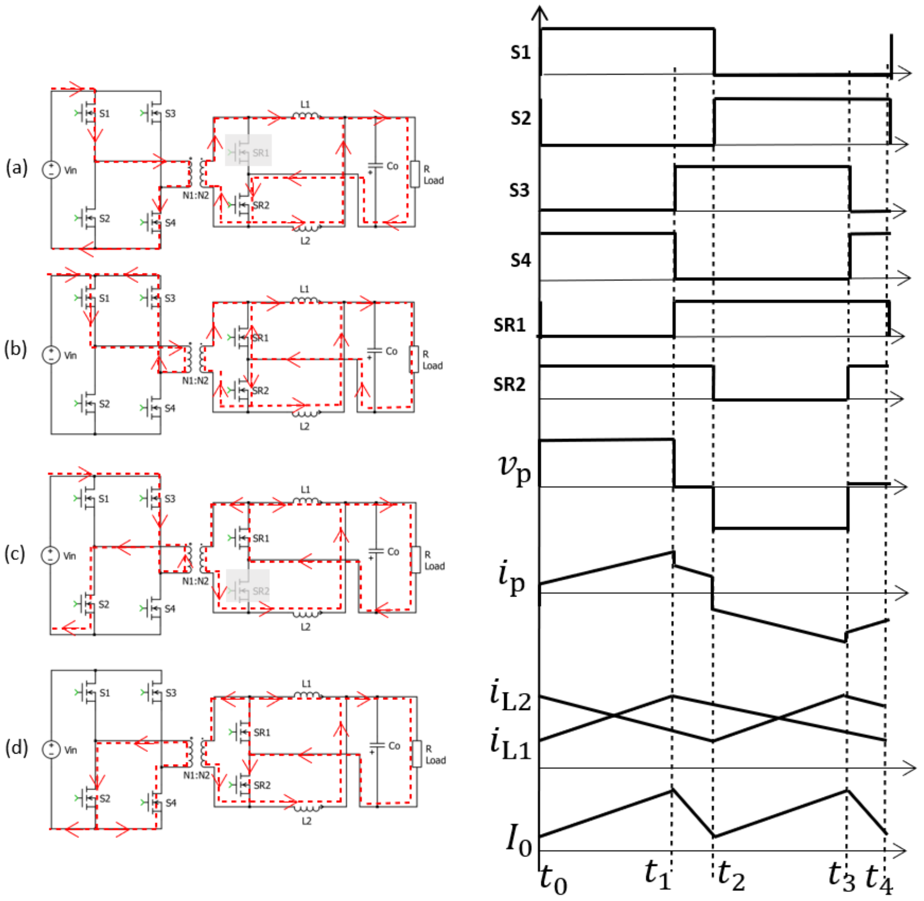


Figure 2.11: Phase shifted Full-bridge CDR operation principle and waveforms,

The design equation of the PSFB and PSFB-CDR are obtained from [13], which are expressed as follows

$$\frac{V_0}{V_{in,min}} = ph\frac{N_s}{N_p} - I_0(\frac{N_s}{N_p})^2\frac{L_{leak}}{V_{in,min}}f \tag{2.13}$$

where

$$I_0(\frac{N_s}{N_p})^2\frac{L_{leak}}{V_{in,min}}f \tag{2.14}$$

represents the duty cycle loss.

The effective phase shift of the converter is calculated as

$$ph_{eff} = \frac{V_0}{V_{in}}\frac{N_p}{N_s} \tag{2.15}$$

In a phase-shifted full-bridge converter, effective phase shift refers to the phase difference between the primary-side voltage waveform and the secondary-side voltage waveform. This phase shift is achieved by controlling the timing of the switching of the high-side and low-side switches in the converter. The effective phase shift is an important parameter that affects the converter's performance, particularly its efficiency and output voltage ripple.

Duty cycle loss, on the other hand, refers to the power loss that occurs in the converter due to the finite on-resistance of the high-side and low-side switches. When the switches are turned on, they have a non-zero resistance, which causes them to dissipate some power. The amount of power dissipated is proportional to the duty cycle of the converter, which is the ratio of the on-time of the switches to the total switching period.

Both effective phase shift and duty cycle loss are important parameters to consider when designing a phase-shifted full-bridge converter. The optimal values for these parameters depend on the specific requirements of the application and the constraints of the converter design.

The primary number of turns are expressed as the following equation

$$N_p = \frac{V_{in}ph_{eff}}{2B_{max}A_{core}f} \tag{2.16}$$

The filter inductance of the converter are assumed to have the same value which are calculated as follows:

$$L_1 = L_2 = \frac{1}{\Delta i_{L1}}V_0(1 - ph_{eff})T_s \tag{2.17}$$

Where Δi_{L2} is the ripple current which is calculated as:

$$\Delta i_{L1} = \Delta i_{L2} = ripple \cdot \frac{I_0}{2} \tag{2.18}$$

The output capacitor on the other hand ,is given by the following expression

$$C_{out} = \frac{V_0(1 - 2 \cdot ph_{eff}T^2)}{16L_1\Delta V_{Cout}} \tag{2.19}$$

2.2.4 Resonant converter

The resonant LLC full-brigde converter is heavily favored in the automotive industry due to its high power density, high efficiency, and uncomplicated design [14]. In addition, the resonant LLC converter has the ability to regulate the wide input variation of the voltage while providing ZVS on the primary side and ZCS on the secondary side of the transformer [15, 16]. Due to the utilization of frequency modulation the LLC converter has three operation modes [17]. The switching frequency f_s is equal to the resonant frequency f_r in the first mode, f_s is greater than f_r in the second mode, and f_s is lower than f_r in the third mode. Different design approaches can be achieved when modeling the LLC converter, however, the converter shown in figure 2.12 is a combination of full-bridge, resonant circuit and a single phase bridge rectifier.

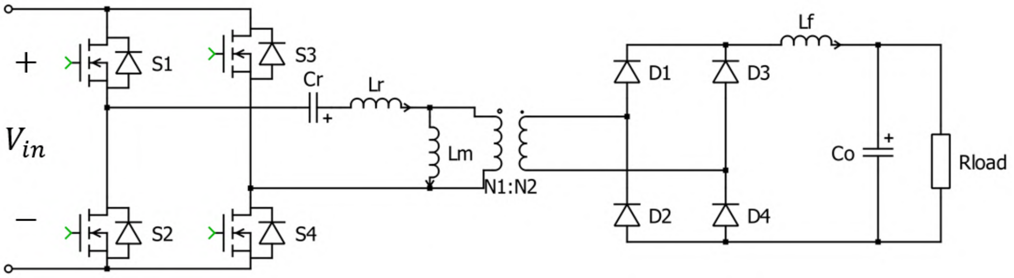


Figure 2.12: LLC resonant Full-bridge converter

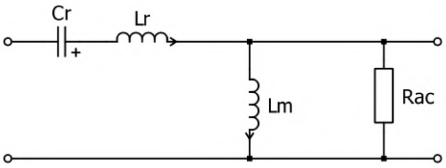


Figure 2.13: Equivalent resonant tank circuit

The determination of the resonant tank parameters in figure 2.13 are important in order to achieve soft switching and obtain high efficiency [18, 17]. Due to the voltage in the magnetizing inductance L_m and the excitation current in L_r, the resonant converter has two resonant frequencies [19]. Thus, these resonant gain curves can be expressed as

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2.20}$$

The parameter R_{ac}, represent the reflected load resistance at maximum load, which is expressed as

$$\frac{8}{\pi^2} \cdot (\frac{N_p}{N_s})^2 \frac{V_o^2}{P_{o,max}} \tag{2.21}$$

The proportion of resonant inductance compared to all primary inductance is formulated as

$$m = \frac{L_r + L_m}{L_r} \tag{2.22}$$

where L_m represents the magnetizing inductance on the primary side. Another important factor is the Quality factor which determines the quality of the resonant tank. The expression for the quality factor is

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \tag{2.23}$$

Additionally, the resonant gain curves are plotted utilizing the normalized frequency, which is the ratio between the switching frequency and the resonance frequency. Thus, the equation for the resonant gain curves are expressed as

$$\frac{F_{norm}^2(m-1)}{\sqrt{(mF_{norm}^2-1)^2+F_{norm}^2(F_{norm}^2-1)^2(m-1)^2Q^2}} \tag{2.24}$$

The operation principle of the converter is demonstrated in figure 2.14 and figure 2.15. As seen in figure 2.14(a), the primary winding receives the input voltage through the resonant tank when the switches S1 & S4 are turned on, and the energy is then transferred to the load on the secondary side via the diode bridges D_1 and D_4. When the switches S2 & S3 are conducting, a negative voltage excites the resonant tank, as presented in Figure 2.14(b). Thus, the diodes D_2 and D_3 on the secondary side are conduction during the operation time of S2 & S3. During the operation modes shown in figure 2.14(c,d) the magnetizing inductance is participating the resonance thus the output on the load side is separated from the primary side.

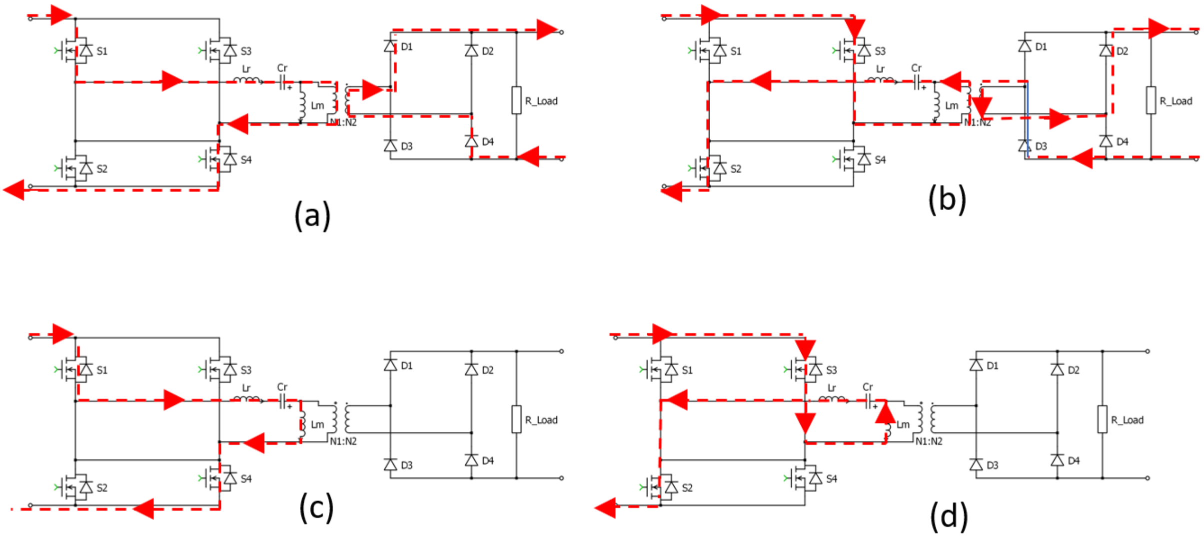


Figure 2.14: LLC operation

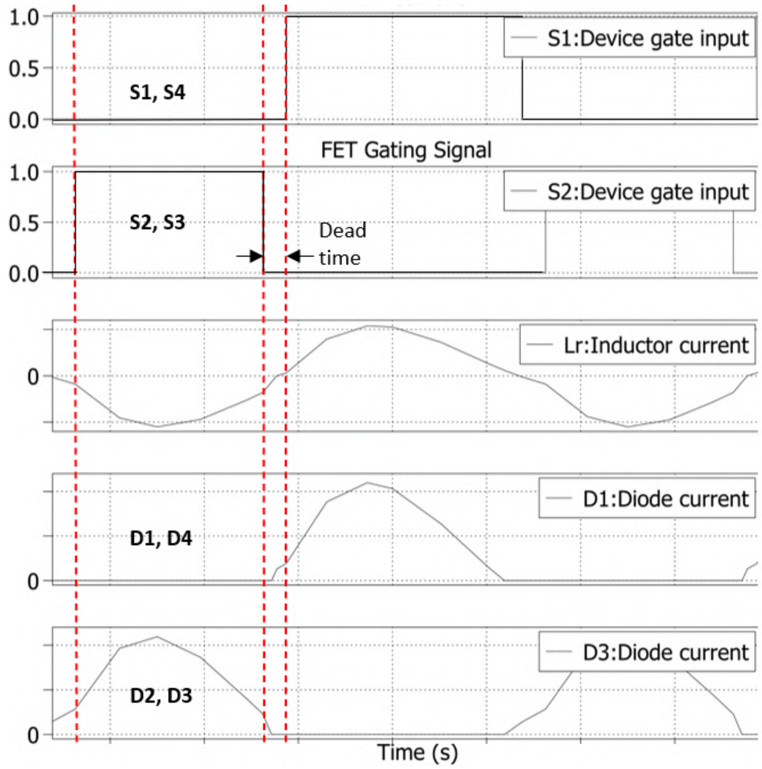


Figure 2.15: LLC operation

2.3 Transformer design

In isolated power electronic topologies, transformers perform essential roles. They perform functions such stepping up/down the voltages and currents that fluctuate over time, as well as providing galvanic isolation, which enhances safety of the circuit [9]. The transformer can be described as an electromagnetic device that is composed of two or more windings that are magnetically connected through an iron core [20]. The windings consist of a primary winding coil and a secondary winding coil. A demonstration of the equivalent circuit of the real transformer is presented in figure 2.16(a) and the ideal transformer in figure 2.16(b). Since the conductors in the ideal transformer are perfect, there are no resistance losses. Further, the magnetizing inductance, L_m, is infinite due that the core has infinite permeability, and the leakage inductances, L_1 and L_2, are both zero since there is no leakage flux in the core. However, the practical transformer does not have ideal parameters and thus it has losses, its B-H profile is shown in figure 2.17. The real transformer has two considerable losses due to the flux variation in the core, which are the iron losses and also copper losses that occurs in the conductors [21].

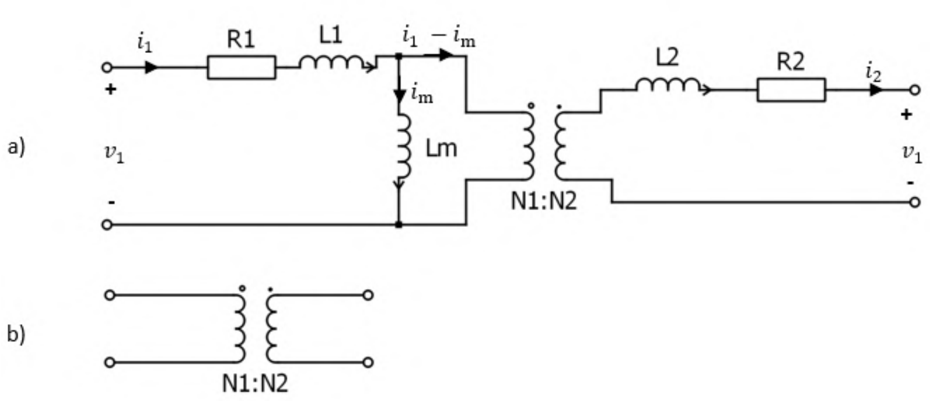


Figure 2.16: Equivalent circuit of the transformer

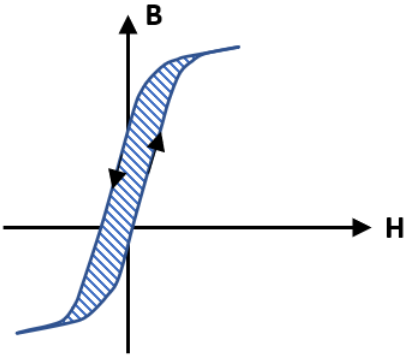


Figure 2.17: Hysteresis loss of the transformer

The transformer losses can be expresses as

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c l_m \tag{2.25}$$

$$P_{cu} = I_{rms}^2 R \tag{2.26}$$

where P_{cu} and P_{fe} are the coppers losses and the iron losses respectively.

The maximum flux of the transformer is calculated with help of the magnetic flux and area of the core [20] and is expressed as

$$\Phi_{max} = B_{core} A_{core} \tag{2.27}$$

According to [20], the maximum flux density can be expressed as

$$B_{max} = \frac{V_{in}}{4 A_{core} N_p f_s} \tag{2.28}$$

where N_p is the primary number of turns.

The winding resistance of the transformer, according to [20] is determined as

$$R = \rho \frac{l}{A_w} \tag{2.29}$$

where ρ, l, & A_w represents the wire length, resistivity and the wire area respectively. The wire area consist of two wire areas which are the winding conductor of the primary and the secondary [20]. The wire areas for both primary and secondary are express as

$$A_{w,p} = \frac{N_p A_{Cu,p}}{k_{Cu,p}} \qquad A_{w,s} = \frac{N_s A_{Cu,s}}{k_{Cu,s}} \tag{2.30}$$

where $A_{Cu,p}$ & $k_{Cu,p}$ are the copper conductor area and the filing factor of the conductor.

The current density of the wire which is also crucial factor for the transformer design is also determined with help of the RMS current and the copper area of the conductor [20], as expressed in the following the equation

$$J_{rms} = \frac{I_{rms}}{A_{cu}} \tag{2.31}$$

Finally, based on [20], Litz wire can be used in order to reduce winding loss and regulate eddy current losses. The litz wires consists of many thin strands of wire which are then braided or twisted together in a specific pattern to form the litz wire. The application of Litz wire reduces the skin effect, whereby high-frequency currents tend to travel primarily along the conductor's surface. This is because the individual strands in Litz wire are insulated from each other, allowing the current to flow through the entire cross-section of the wire and also distributing the current over the multiple number of strands, thereby reducing the resistance and improving the efficiency of the winding.

2.3.1 Semiconductor power devices

Incredible breakthroughs in semiconductor technology have significantly contributed the development of the power electronics sector, in terms of switching speed and power capabilities [8]. The majority of semiconductor power devices on the market today are Silicon-based (Si). However, the Si-based semiconductors have a narrow band gap in terms of critical electric field for breakdown, electron velocity voltages, frequencies, and temperatures [22]. With regard to EV applications wide band gap semiconductors such as Silicon Carbide and Gallium Nitrate (SiC and GaN) are preferred [22]. SiC and GaN switches minimize the conduction losses while operating at high frequencies. The higher frequencies also make it possible to reduce the size of the passive elements which also reduces the size of the switch and heat sinks [22]. Despite having superior advantages and unique characteristics, SiC and GaN have also disadvantages which lessens their popularity. In comparison to Si-based semiconductors drawbacks such as a higher cost, less development, and lower reliability exist.

2.3.1.1 MOSFET

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a switching semiconductor device which is considered one of the most essential component in a power electronic system due its wide range frequency and voltage capabilities [8]. The MOSFETs are divided into two types which consist of three terminals respectively [20]. As depicted in figure 2.18, there is two MOSFET types N-channel shown in figure 2.18a and P-channel shown in figure 2.18b. Due to the fact that P-channel MOSFETs require more space on the silicon wafer in order to perform similarly to the N-channel, N-channel MOSFETs are preferred in current power electronics devices [20]. The terminals are an input terminal called gate and two output terminals named Drain and the Source . The function of the gate terminal is to control the current flowing the through the output sources. Figure 2.18c shows the characteristic of the drain current as functions of the drain-source voltage v_{DS}.

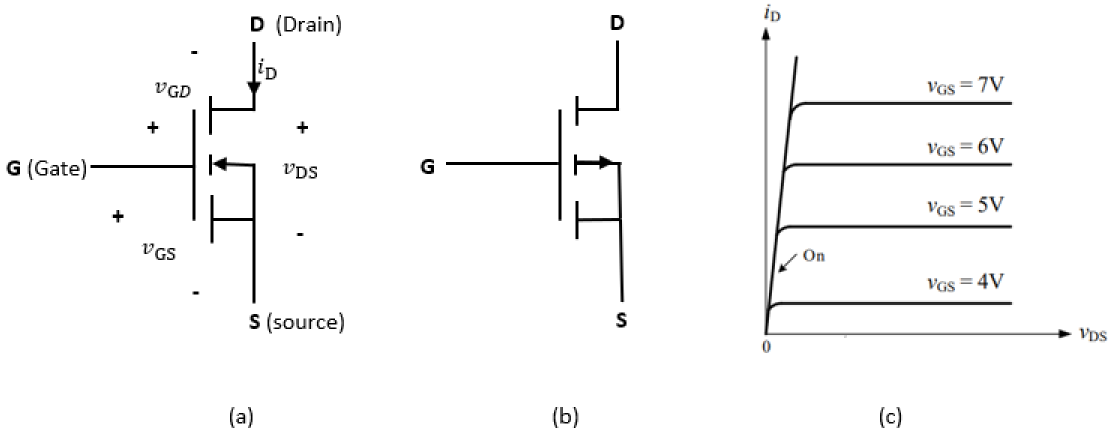


Figure 2.18: MOSFET and characteristics, (a) N-channel, (b) P-channel, (c) I-V characteristics of drain voltage v_{DS} and current i_D in N-channel MOSFET

Internal diode and internal capacitors are the crucial parameters of the MOSFETs switching characteristics [8]. The internal diode which is also named body diode is between the source and drain. When a bidirectional switch is desired, the drain current can be reversed directed by utilizing the body diode [8]. The internal parasitic capacitance are connected between the gate-to-source C_{gs}, gate-to-drain C_{gd} and drain-to-source C_{ds} [8]. These parasitic capacitances are important to determine the time constant for the rate of increase of v_{GS} in the ohmic region and the rate of the voltage decrease for the v_{DS}. They also have a crucial role in minimizing the gate losses and the output capacitance losses. As the gate signal is applied, the miller capacitance's C_{gs} and C_{ds} starts to get charged resulting in an increase of the gate voltage. Drain current will start flowing through the device as soon as v_{GS} hits the threshold voltage and will continue to increase proportionally until it reaches I_D meaning that the MOSFET is fully conducting. With consideration of a non-ideal MOSFET, there will be reverse-recovery current flowing meaning that the current through the device will reach $I_D + I_{rr}$ before the voltage v_{DS} starts to decrease. As the voltage v_{DS} decreases, the gate voltage v_{GS} gets clamped at the miller plateau voltage level until the voltage across the device reaches its final value $I_D r_{(DS)on}$. At this time instance the switching is complete and the the v_{GS} rises to its rated voltage [23].

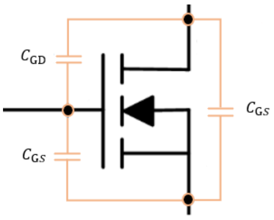


Figure 2.19: MOSFET characteristic with Miller capacitance's

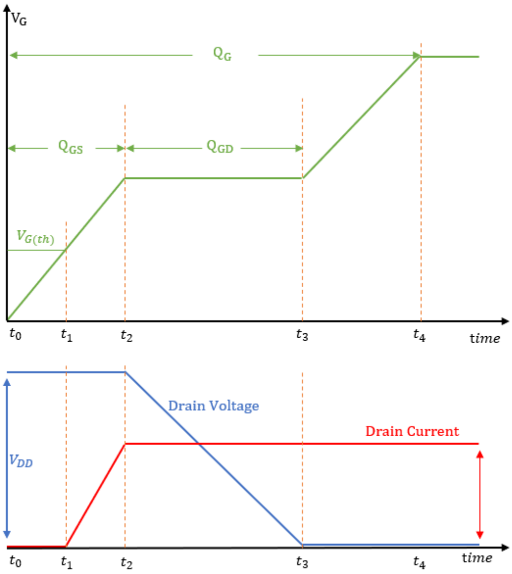


Figure 2.20: Switching characteristic of MOSFET

The MOSFET operates during the linear region when the difference between the gate source voltage v_{GS}, and the threshold voltage v_{th} is equal to or less than the drain source voltage v_{DS}. When v_{GS} becomes constant the MOSFET enters the saturation region. During the operation in the linear region the power dissipation occurs via on-state resistance $r_{DS(on)}$.

The following equations which are derived for the MOSFET parameters are obtained from [20].

The time constant for the exponential rise of v_{GS} before the drop of drain-to-source voltage is described as

$$\tau_1 = R_G(C_{gs} + C_{gd1}) \tag{2.32}$$

where R_G is the series resistance of the gate. Likewise, the time constant for the exponential rise of v_{GS} when the switching is completed and when the gate current ceases to zero is

$$\tau_2 = R_G(C_{gs} + C_{gd2}) \tag{2.33}$$

The gate current can be calculated as

$$i_G = \frac{V_{GG} - V_{GS,I_0}}{R_G} \tag{2.34}$$

Knowing that i_G passes through C_{gd}, the rate of change of v_{DS} can be derived to

$$\frac{dv_{DG}}{dt} = \frac{dv_{DS}}{dt} = \frac{i_G}{C_{gd}} = \frac{V_{GG} - V_{GS,I_0}}{R_G C_{gd}} \tag{2.35}$$

Further, the on-state conduction losses of the MOSFET can be calculated as

$$P_{CMosfet} = I_0^2 r_{DS(on)} \tag{2.36}$$

where I_0 is the RMS current through the device. The I-V curve for the body diode is a bit different since a forward voltage drop is needed for the diode to start conducting current through it while in the MOSFET the current through it is controlled by the applied gate voltage. Taking this into consideration, voltage drop of the body-diode is

$$v_D = V_f + i_D(t) R_D \tag{2.37}$$

which further gives the conduction losses of

$$P_{CDiode} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_D i_D(t)\, dt \ = V_f i_{Davg} + i_{Drms}^2 R_D \tag{2.38}$$

where V_f is the forward voltage of the diode and i_D the current through it.

2.3.1.2 Switching losses

Power losses in semiconductor devices,which are also known as conduction losses and switching losses are caused when a device switches from the blocking state to the conducting state and vice versa [20]. Higher switching losses can result in switch device malfunction which could damage critical components in the device [20]. Figure 2.21 demonstrates the waveforms of the instantaneous switch and the switching power losses that occurs in the switch.

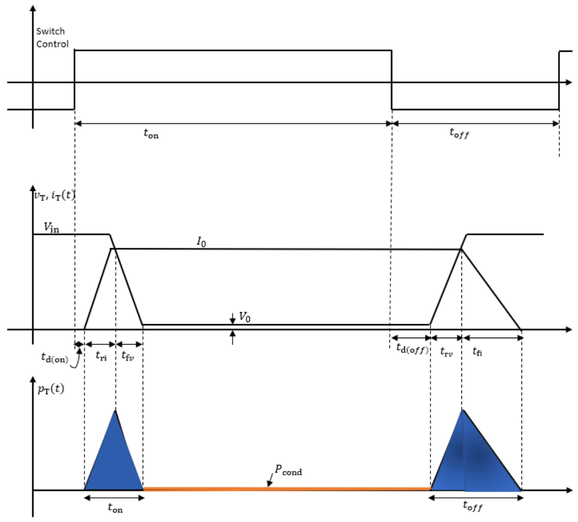


Figure 2.21: Waveforms of the switch and switching power loss

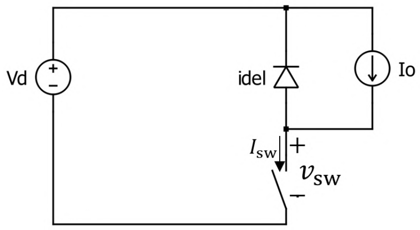


Figure 2.22: Ideal switch circuit

On-state losses and switching losses are two significant losses generated by the transistor [20]. The switching losses consist of turn-on and turn-off losses and are frequency dependent [20]. As presented in figure 2.22, the current I_0, goes through the switch when it is turned on while the diode is only forward biased during the off-period of the switch. During the off-period the voltage across the switch is V_{in}, however it drops to the on-state voltage V_{on} when I_0 completely passes the switch.

The waveforms in figure 2.21 shows that it takes a dead time of $t_{d(on)}$ and a rise time t_{ri} for the current to reach the steady-state the current I_0. When the current reached I_0 the voltage falls from V_{in} to V_{on} during a period time of t_{fv}. Thus, the turn-on losses occurs during the transition time t_{ri} and t_{fv} where the voltage and the current are not zero. Similar to turn-on losses, turn-off losses occur during voltage increases, which is made up of a dead time $t_{d(off)}$ and a rising time t_{rv}, and a falling time t_{fi} for the current. The conduction losses p_{on} occur during the on-state when the voltage across the switch is V_0, thus utilizing the output current, on-state voltage and the duty cycle the p_{on} loss could be determined.

The following equations describes the switching power dissipation and the conduction losses.

The energy losses during the turn-on can be computed

$$e_{sw} = \frac{1}{2} V_{in} I_0 t_{(on)} \tag{2.39}$$

$$t_{(on)} = t_{ri} + t_{fv} \tag{2.40}$$

The energy losses during the turn-off can be computed

$$e_{sw} = \frac{1}{2} V_{in} I_0 t_{(off)} \tag{2.41}$$

$$t_{(off)} = t_{rv} + t_{fi} \tag{2.42}$$

Where $t_{(on)}$ & $t_{(off)}$ are the total time of the rising/falling of the voltage and the current respectively.

Since the switching losses are frequency dependent, they will increase as the frequency increase which results in a frequency cutoff that cannot be exceeded. In order to improve the switch and increase the efficiency, soft switching techniques such as Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS) are utilized [21]. According to figure 2.21 the hard switching occurs due to the crossing of non-zero voltage and current. The ZVS and ZCS provides a zero crossings turn-on and/or turn-off transitions, which reduces the switching losses practically to zero as demonstrated in figure 2.23.

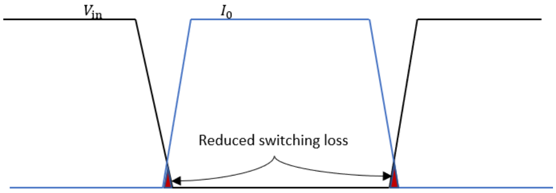


Figure 2.23: ZVS & ZCS waveforms

The additional losses that needs to be accounted for are the ones depending of the internal capacitances of the MOSFET such as

- Input capacitance ($C_{iss} = C_{gs} + C_{gd}$)
- Output capacitance ($C_{oss} = C_{ds} + C_{gd}$)
- Reverse transfer capacitance ($C_{rss} = C_{gd}$)

which contributes to losses at turn-on, turn-off of the MOSFET when either the charge in the miller capacitance's needs to be charged or discharged. The output capacitance losses are usually neglected when there is ZVS.

The gate driver losses are expressed as

$$P_{gate} = V_{gs} Q_g f_{sw} \tag{2.43}$$

where Q_g it the total gate charge. In case the output capacitance losses are computed, they are expressed as

$$P_{oss} = \frac{1}{2} Q_{oss} V_{ds} f_{sw} = \frac{1}{2} C_{oss} V_{ds}^2 f_{sw} \tag{2.44}$$

3

Case set-up

3.1 Requirements for DC/DC

The requirements for all the topologies that will be studied are stated in table 3.1.

Table 3.1: Requirements for DC/DC

Primary DC voltage	290V - 410V
Secondary DC voltage	9V - 16V
Continuous output power	2.9kW - 3.1kW
Continuous output current	245A at 13.8V
Efficiency	>95%
Switching frequency	100kHz

3.2 Setup for DAB

The determination of the leakage inductance of the MFPT for the DAB plays an important role for minimizing circulating currents, thus also minimizing the losses. Especially when the DC-link voltage at the sending side deviates from the nominal voltage meaning that the conversion rate, $\frac{V_{sec}}{N_w \cdot V_{pri}}$, also deviates and soft-switching can not be attained at both bridges any longer [24], see figure 3.1. Having a high leakage inductance will lead to better switching performance, but also increase the RMS current on both sides of the MFPT [25]. The focus will be kept to keeping the secondary RMS current as low as possible since the main losses for the specified requirements will be the conduction losses on the secondary side.

By inserting the values as specified in table 3.1, the desired leakage inductance of the MFT is calculated to be

$$L_\sigma = D(1-D)n_w V_{pri}\frac{V_{sec}}{2f_{sw}P_{cont.}} = 31.3nH \tag{3.1}$$

where the phase shift is set at 20 degrees for transfer of nominal power, meaning that the calculation of D is as

$$D = \frac{\frac{20° \cdot \pi}{180°}}{\pi} = \frac{1}{9} \tag{3.2}$$

The RMS current on the secondary side H-bridge is expressed as

$$I_{sec}(\delta) = \frac{\pi V_{sec} - (\pi - 2\delta) N_w V_{pri}}{2wL_\sigma} = 245.7A \tag{3.3}$$

$$I_{sec}(\pi) = \frac{\pi N_w V_{pri} + (2\delta - \pi) V_{sec}}{2wL_\sigma} = 245.7A \tag{3.4}$$

when assuming that $\frac{V_{sec}}{N_w V_{pri}} = 1$ meaning that the current waveform through the transformer is close to rectangular.

The primary RMS current is therefore

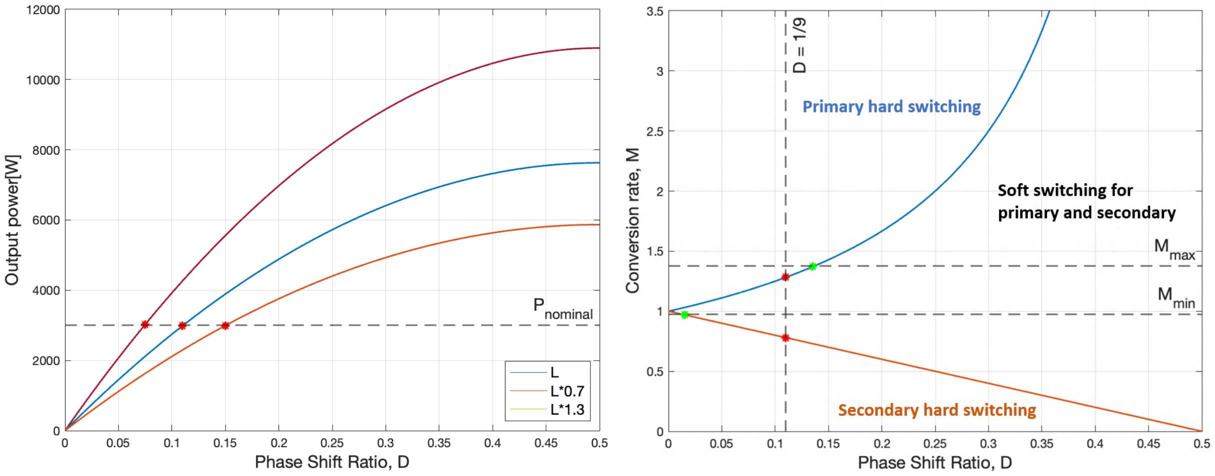
$$I_{pri}(\pi) = N_w I_{sec}(\pi) = 8.5A \tag{3.5}$$

when the primary voltage is set at 400V and the secondary at 13.8V.

As specified in table 3.1, both the input and output voltage will be varying meaning that the conversion ratio will be deviating from 1. It is assumed that the outer voltage will be fixed at either 12V or 13.8V and that the input voltage will be the only thing varying with the SOC of the HV battery. The variation will give the following limited conversion ratios

$$M_{max} = \frac{13.8V}{N_w \cdot 410V} = 1.3793 \qquad M_{min} = \frac{13.8V}{N_w \cdot 290V} = 0.9756 \tag{3.6}$$

which are marked in figure 3.1b.



(a) Output power as a function of phase shift ratio

(b) Soft switching region for DAB

Figure 3.1: Impact of varying conversion rate and leakage inductance

The borderlines of the hard switching are derived mathematically as

$$M \leq \frac{1}{1-2D} \qquad (Primary) \tag{3.7}$$

$$M \geq 1-2D \qquad (Secondary) \tag{3.8}$$

when assuming ideal operations such as neglecting parasitic elements and not taking the dead-time at turn on into consideration[26].

The complete model of the DAB in PLECS is presented in figure 3.2. The transformer of the DAB converter is similar to the PSFB converter one, which is presented in table 3.2. In the DAB it is also necessary to have an output filter inductance, L_O to give better control of the output power and also reduce the ripple of the current by limiting the $\frac{di}{dt}$ at the switching instances.

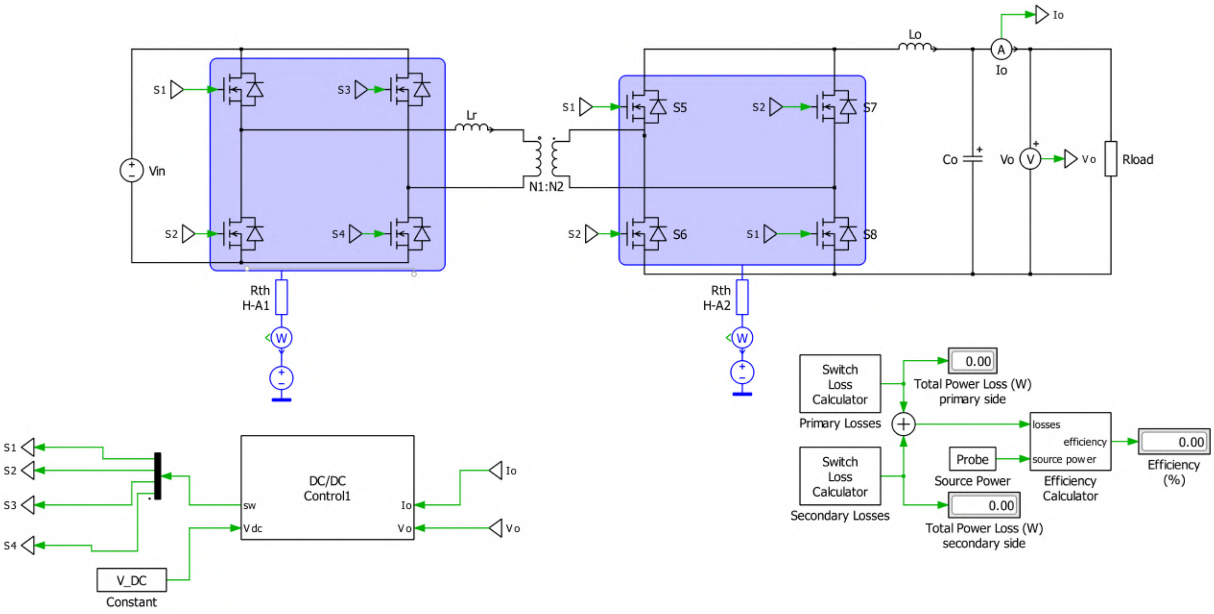


Figure 3.2: DAB model in PLECS

3.3 Setup for PSFB and PSFB-CDR

By utilizing (2.13) and neglecting the duty cycle loss, while assuming maximum phase shift of 0.5 at minimum input voltage of 290V. The ratio between the number of turns are obtained as follows

$$\frac{12}{290} = 0.5\frac{N_s}{N_p} \Rightarrow \frac{N_p}{N_s} = 12 \tag{3.9}$$

According to (2.15), the effective phase shift can be calculated for the maximum output voltage as

$$Ph_{eff} = \frac{16}{400} \cdot 12 = 0.48 \tag{3.10}$$

By selecting a transformer with core area of 368 mm^2 and maximum flux density of 100 mT, the primary number of turns are obtained from (2.16) at maximum input voltage as

$$N_p = \frac{400 \cdot 0.48}{2 \cdot 0.100 \cdot 368 \cdot 10^{-6} \cdot 100 \cdot 10^3} = 26 turns \tag{3.11}$$

In order to verify the obtained number of turns, (2.28) is utilized which gave number of turns of 27 turns, thus the number of turns are taken as 27 turns. The number of turns at the second side are calculated to 2 turns.

The desired filter inductance of the converter is calculated to 24.96μH by utilizing (2.17) and the leakage inductance is selected arbitrary. The capacitance value of the filter capacitor has been determined to be 59.7μF using (2.19) with the objective of reducing the ripple voltage and achieving a stable output voltage. This calculation is based on the principle that a larger capacitor can store more charge and therefore can better smooth out variations in voltage. By selecting an appropriate capacitance value, the filter capacitor can effectively reduce the ripple voltage and deliver a more consistent voltage output. Further adjustments have been done where the number of turns are also adjusted for the PSFB-CDR as can be seen in table 3.2. The parameters are implemented in PLECS which is seen in figure 3.3 and figure 3.4.

Table 3.2: Requirements for PSFB and PSFB-CDR

Parameters	**PSFB**	**PSFB-CDR**
Maximum flux density	100 mT	100 mT
Switching frequency	100 kHz	100 kHz
Core type	ETD 59/31/22	ETD 59/31/22
Effective core area	368 mm^2	368 mm^2
Effective core length	139 mm	139 mm
Winding cross section	365.6 mm^2	365.6 mm^2
Average length of turn	106.1 mm	106.1 mm
Inductor ripple current	1 %	1 %
Capacitor ripple voltage	2 mV	2 mV
Leakage inductor	10 μH	10 μH
Filter inductor	24.96 μH	24.96 μH
Filter capacitor	59.7 μF	59.7 μF
Number of turns primary side	27	27
Number of turns secondary side	2	3

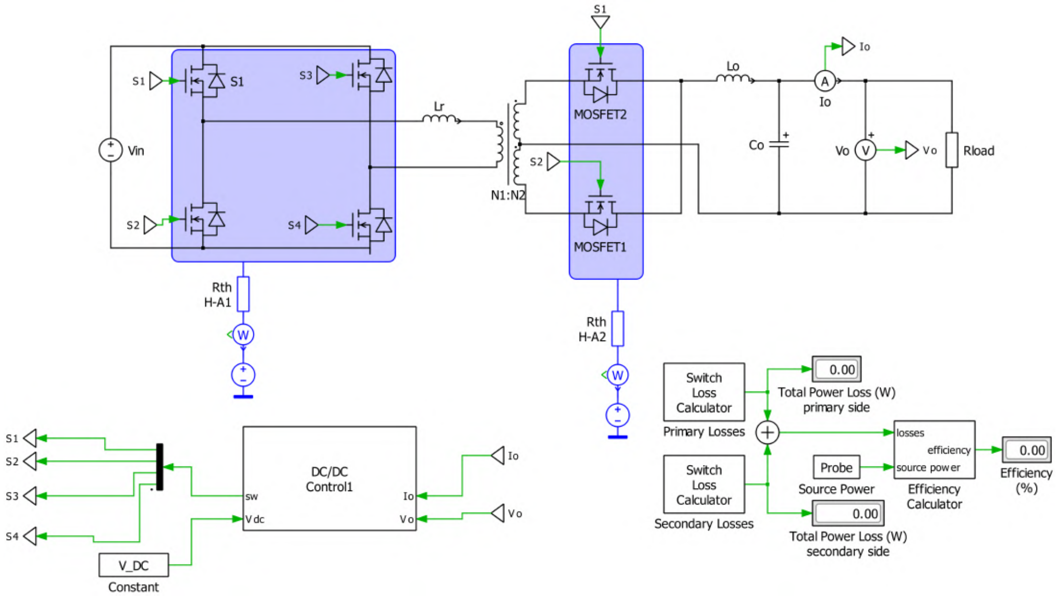


Figure 3.3: Phase shifted full-bridge model in PLECS

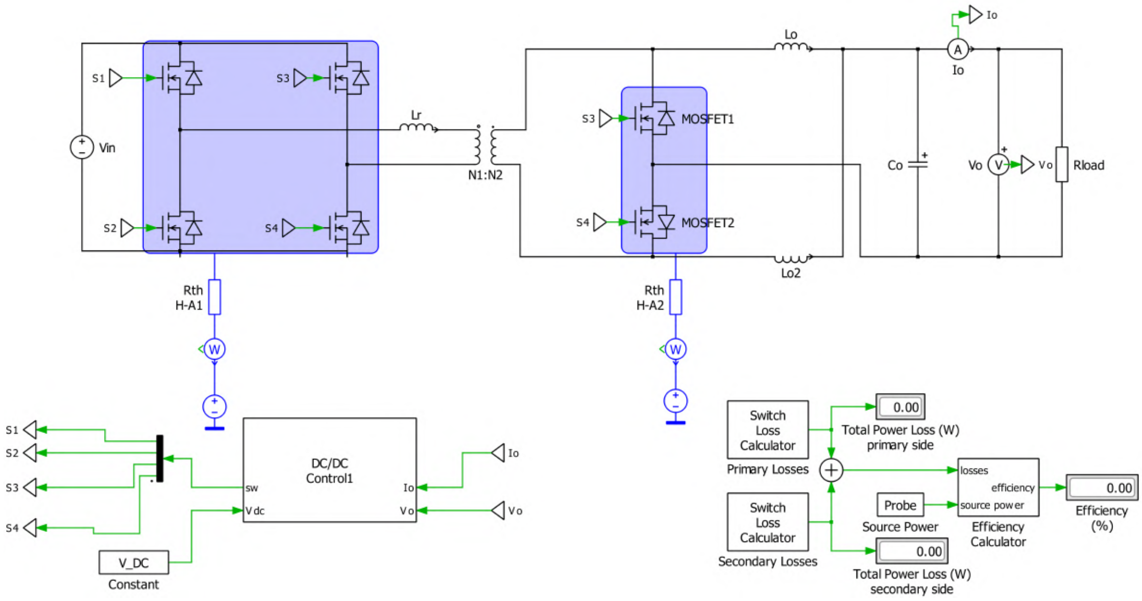


Figure 3.4: Phase shifted full-bridge with current doubler rectifier model in PLECS

3.4 Setup for the resonant converter

The PSFB and PSFB-CDR are extended with a resonant capacitor and a magnetizing inductance in order to form the resonant tank circuit presented earlier in figure 2.13. According to [18], the determination of the desirable Q-factor and the m-value require iterative processes, where physical experiments and extensive computations are needed to select the best-possible value. Further, according to [17], larger m-value which result larger magnetizing inductance is desired in order to achieve higher efficiency, while assuming operation at resonant frequency of 100kHz.

Table 3.3: Resonant tank parameters for PSFB and PSFB-CDR

Parameters	PSFB	PSFB-CDR
C_r	1.12 μF	1.12 μF
L_r	2.24 μH	2.24 μH
L_m	100 μH	100 μH

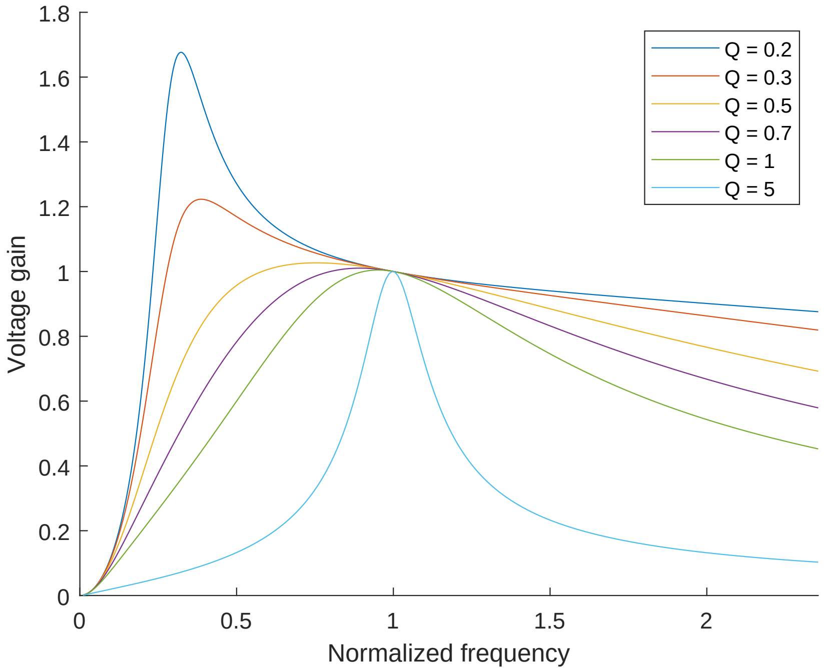


Figure 3.5: Voltage gain at different Q-factors

The resonance gain curve plays a crucial role in optimizing the resonant converter design by determining the values of resonant components such as inductors and capacitors, which are required to achieve the desired resonant frequency and gain characteristics. Thus, utilizing (2.24), the gain values at different Q-factors are presented in figure 3.5. Since Q and m required complex computations, the quality factor is chosen to 0.2 while m is chosen to 46 in order to maintain higher magnetizing inductance for better efficiency. Finally, (2.20), (2.21), (2.23) and (2.22) are used to calculate the resonant tank parameters in table 3.3.

3.5 Transformer setup

According to [27], the size of a single litz wire is between 0.05 – 0.1mm for DC/DC transformer operation in a frequency range of 100 – 500kHz. Further, the skin dept of the litz wire at 100kHz frequency is determined to

$$\delta = 0.21mm \tag{3.12}$$

where the single wire diameter should be less than or equal to almost one-third of skin depth, shown in the following equation

$$d = \frac{1}{3}\delta \tag{3.13}$$

In this case a wire with diameter of 0.07mm is chosen with current density of $4.5A/mm^2$. Since a single wire is too thin, many wires has to be bundled in order to be able to carry the large currents on the primary and the secondary of the transformer. Thus the bundle area on the primary side is calculated as

$$A_{bundle,pri} = \frac{I_{rms,pri}}{J} = \frac{11}{4.5} = 2.44mm^2 \tag{3.14}$$

similarly, the bundle area on the secondary side can be calculated as

$$A_{bundle,sec} = \frac{I_{rms,sec}}{J} = \frac{250}{4.5} = 55.6mm^2 \tag{3.15}$$

Subsequent to the determination of the bundle area, the subsequent step involves the computation of the winding area and evaluating its compatibility with the winding window of the transformer. Utilizing (2.30) and assuming fill factor of 0.5, the total winding area can be simplified to

$$A_{wtot} = \frac{A_{bundle,pri}N_p + A_{bundle,sec}N_s}{k_{cu}} \tag{3.16}$$

On the other hand regarding the transformer losses, (2.29) is used to determine the copper losses, which can be simplified to

$$R_{pri} = \rho\frac{N_pL_N}{A_{bundle,pri}} \qquad R_{sec} = \rho\frac{N_sL_N}{A_{bundle,sec}} \tag{3.17}$$

where L_N is the average length of one turn, which is found in the transformer datasheet. While the iron losses, P_{fe} is given in the datasheet. The winding resistances and the winding window are presented in table 3.4.

Table 3.4: Transformer loss parameters

Primary winding resistance	19.72 mΩ
Secondary winding resistance	0.1 mΩ
Winding window	354.16 mm^2
Relative core losses	4.5 W

3.6 MOSFET selection

The MOSFETs in the HV H-bridge will have to withstand a maximum voltage of 420V and a RMS current around 10A. Using the thumb-rule of having approximately 1.5 times higher voltage, a 650V SiC MOSFET was chosen from Wolfspeed Inc. with series number E3M0060065D [28]. For the secondary H-Bridge, the maximum current is below 300A and has a voltage ranging from 9V-16V. The conduction losses will be of huge importance and therefore a SI MOSFET with a low $r_{DS(on)}$ will be prioritized. The Si MOSFET chosen for the secondary side is therefore from ON Semiconductors which provides the necessary data for simulations on PLECS, and has a series number of NVMTS0D4N04C [29]. For unidirectional power flow, ON Semiconductor's SiC Schottky diode with series number FFSH5065B-F085 is selected, the diode has a current rating of 50A. Further, for the purpose of comparing switching devices in the primary, the GS-065-030-2-L GaN from GAN systems with a voltage rating of 650V was selected.

Due to the design of having the secondary side in the region of soft switching more frequently than the primary side, a SiC MOSFET on the primary is more suitable since it provides lower switching losses due to its wide bandgap which also has a lower reverse recovery time than a Si MOSFET. The downside with wide bandgap is although higher $r_{DS(on)}$ meaning that a decent amount of SiC MOSFETs in parallel would be required to get as low conduction losses as a Si MOSFET.

Table 3.5: Characteristics of the MOSFETs

	Primary SiC	**Secondary Si**
Total gate charge(nC)	46	251
Gate to source charge(nC)	13	49.2
Gate to drain charge(nC)	16	62.4
Reverse transfer capacitance(pF)	6	390
Internal gate resistance(Ω)	4	0.9
Gate threshold voltage(V)	2.8	3.0
Plateau Voltage(V)	8.4	4.09

3.7 Thermal modelling

For the thermal modelling, there are two main network used when describing the heat flow in an electrical circuit which are the Cauer network and Foster network. Both options are available for use on PLECS where the Cauer network is seen as more physically related, while the Foster network is more mathematically related. The conversion from the electrical domain to the thermal domain is as explained in table 3.6.

Table 3.6: Conversion from electrical to thermal

Electrical	**Thermal**
Voltage(V)	Temperature(℃)
Current(A)	Heat flow(W)
Charge(C)	Heat(J)
Resistance(Ω)	Resistance(K/W)
Capacitance(F)	Capacitance(J/K)

The design of the heat sink is of big importance to be able to transport as much thermal energy away from the semiconductor and by doing that lowering the total losses. As for any conductor, the on resistance of the MOSFET increases with the temperature and for a voltage conversion as in the case presented in this thesis, it will lead to huge conduction losses due to the high current on the 12V system bus. In figure 3.6 a sketch of a heat sink is presented.

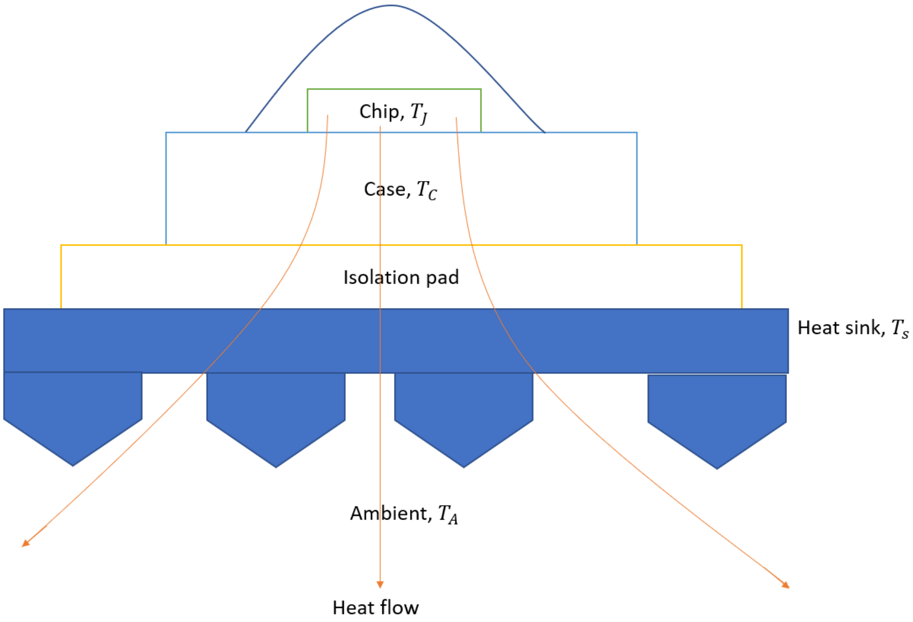


Figure 3.6: Sketch of the heat sink

The amount of thermal power that is dissipated is explained with the following equation

$$P_D = \frac{T_J - T_A}{R_{\theta JA}} \tag{3.18}$$

where T_J is the junction temperature, T_A the ambient temperature and $R_{\theta JA}$ the total thermal resistance from junction to ambient. The total thermal impedance is expressed as

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \tag{3.19}$$

giving the equivalent thermal circuit in figure 3.7.

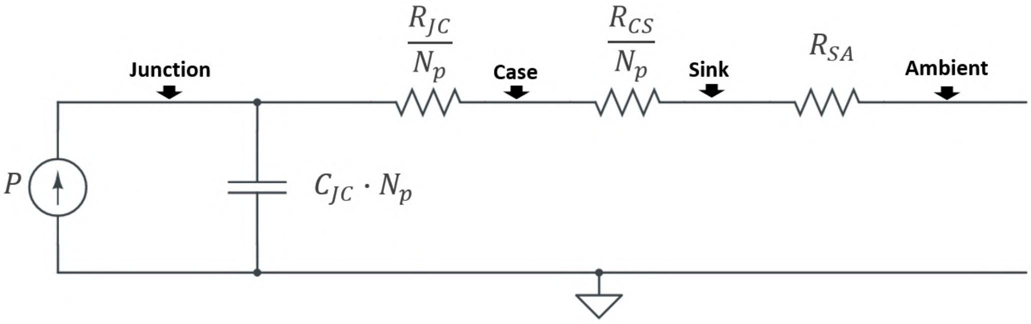


Figure 3.7: Equivalent circuit of the thermal impedance

The lower the total thermal resistance is, the more thermal power can be dissipated meaning that the thermal conductivity of a material is of great importance. For the heat sink, the most common materials are aluminium and copper where copper provides a better performance due to its higher thermal conductivity which also comes with a higher price. A Thermal Interface Material (TIM) is also used to lower the thermal impedance since it fills out the air gap of the irregular shapes between the case and heat sink. The TIM is usually made from silicone polymer with ceramic particles to increase the thermal conductivity which ranges from 1W/mK to 5W/mK [30]. The thermal resistance from case to sink is calculated as

$$R_{\theta CS} = \frac{t}{kA} \tag{3.20}$$

where t is the thickness of the TIM pad, A is the cross-sectional area and k the thermal conductivity of the material.

From the datasheet of each MOSFETs the junction-to-case thermal resistance is found and is 1.02°C/W for the primary SiC MOSFETs and 0.62°C/W for the secondary Si MOSFETs. The TIM chosen is from Saint-Gobain with a thermal conductivity of 1.1W/mK and a thickness of 0.1in [31]. The cross-sectional area of the TIM is the same as for the heat sink which is assumed to be around 300x200mm after using an existing 3kW 400/12V liquid-cooled DC/DC converter as reference [32].

Using (3.20), the case-sink thermal impedance is calculated to be

$$R_{\theta CS} = \frac{0.00254}{0.2 \cdot 0.3}\frac{1}{1.1} = 0.0385°C/W \tag{3.21}$$

The dissipated power is calculated at the rated output power of 3kW and 400V input voltage. The junction temperature of both the SiC and Si MOSFET is assumed to be at 70°C at continuous 3kW output power and therefore the drain-source internal resistance will be multiplied by a factor which is extracted from the respective datasheet.

Table 3.7: Hand calculated losses of one device at primary and secondary side of the PSFB-CDR

	Pri. SiC MOSFET	**Sec. Si MOSFET**
Conduction losses(W)	6.08	13.31
Switching losses(W)	3.89	0
Gate losses(W)	0.09	0.50
Total losses of one MOSFET(W)	**10.06**	**15.81**
Total losses of all MOSFETs(W)	**40.22**	**31.63**

Given the losses from table 3.7, the total dissipated power is 71.83W which gives the thermal sink-ambient resistance of

$$R_{\theta SA} < \frac{T_J \cdot 0.85 - T_A}{P_{total,dissipated}} - R_{\theta JC} - R_{\theta CS} < 0.664°C/W \tag{3.22}$$

To fit the requirement, one air-cooled heat sink with the thermal resistance of $0.3°C/W$ at natural convection will be compared to a liquid-cooled heat sink with the thermal resistance of $0.016°C/W$ at a flow rate of 0.2 gallon/min [33, 34]. An alternative air-cooled heat sink will also be studied to see how much the losses will increase when using a cheaper and more economically heat sink. The alternative heat sink has a thermal resistance of $1.65°C/W$ at natural convection [35].

3.8 HV Li-ion battery modelling

The li-ion battery modelling using PLECS will be a R-only based model which is made for dynamical simulations [36]. The model will reflect the voltage of the battery module as a function of the SOC. The most accurate way to model a li-ion battery would be using a FEM based software which accurately solves for all the electrochemical phenomenas occurring in the cell. That is although very time consuming and not convenient to use in this thesis. An electrical model is therefore used and implemented in the simulations. The battery of choice is Sunwoda 246Ah battery [37] and its specifications are in table 3.8.

Table 3.8: Specification of the li-ion battery module

Minimum cell voltage	2.8V
Maximum cell voltage	4.35V
Nominal cell voltage	3.6V
Nominal capacity	246Ah
SOC usage window	3%-97%
Cells in parallel	1
Cells in series	94
Internal resistance of one cell	0.44mΩ

The mount of cells needed in series are

$$N_s = \frac{Maximum\ module\ voltage}{Maximum\ cell\ voltage} = \frac{410V}{4.35V} \approx 94 \tag{3.23}$$

and in parallel is one. This will give a resulting energy of

$$E_{battery} = 246Ah \cdot 3.6V \cdot 94 = 83.2kWh \tag{3.24}$$

and an internal resistance of

$$R_{module} = R_{cell} \cdot N_s = 0.44m\Omega \cdot 94 = 41.36m\Omega \tag{3.25}$$

Since the nominal load in this project is 3kW, it will mean that the time for fully discharging the battery will be roughly 28 hours. To reduce the time, the nominal capacity in the R-only model will be decreased so that the SOC of the battery can go from 97% to 3% in seconds.

3.8.1 Battery model evaluation

With the parameters determined in section 3.8, the R-only model was implemented in PLECS on all topologies and its characteristics is seen in figure 3.8.

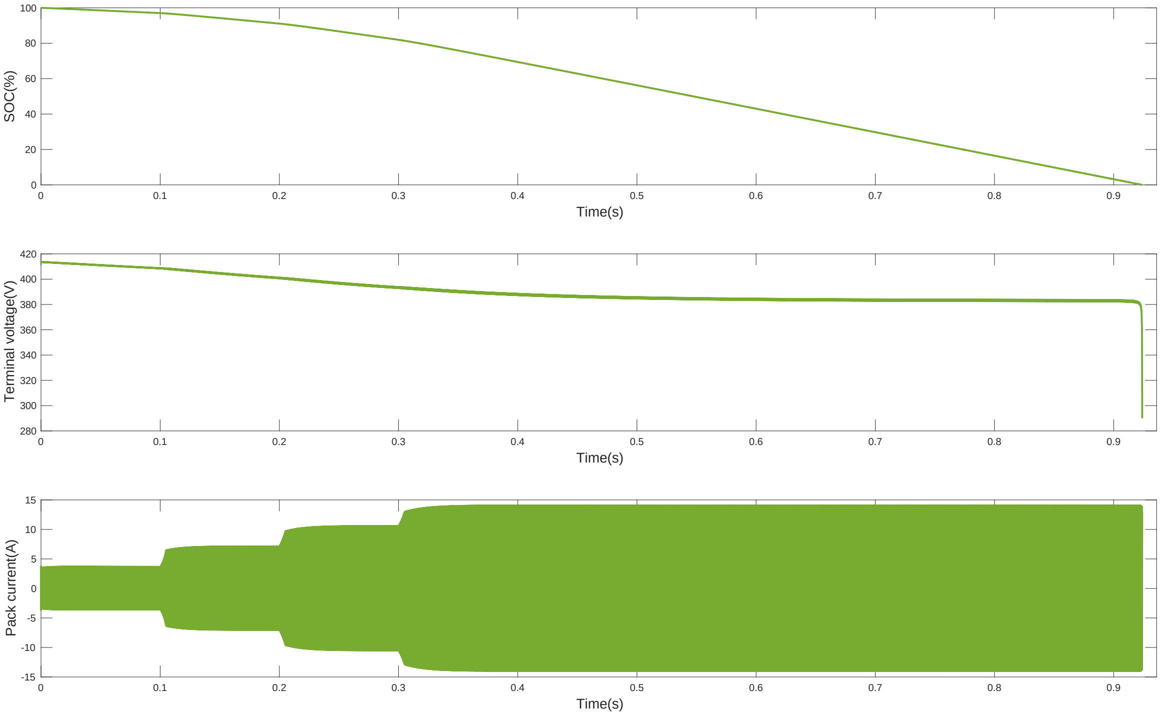


Figure 3.8: R-only model at four different load conditions

A stop condition was implemented so that the terminal voltage of the battery model would not go lower than 290V resulting in an inaccurate voltage characteristic as the SOC charge drops below 5%. The voltage has a very steep response at the low SOC which in not wanted. Instead, a lookup table with SOC and the corresponding voltages is made and implemented in the model initialization in PLECS where the values in between are interpolated using "Piecewise Cubic Hermite Interpolating Polynomial" to get a more non-linear profile. The result is seen in figure 3.9. When used for simulations in PLECS, the total simulation time is set as another vector in the lookup-table where T_{start} is set at 0% SOC and T_{final} is set at 100% SOC.

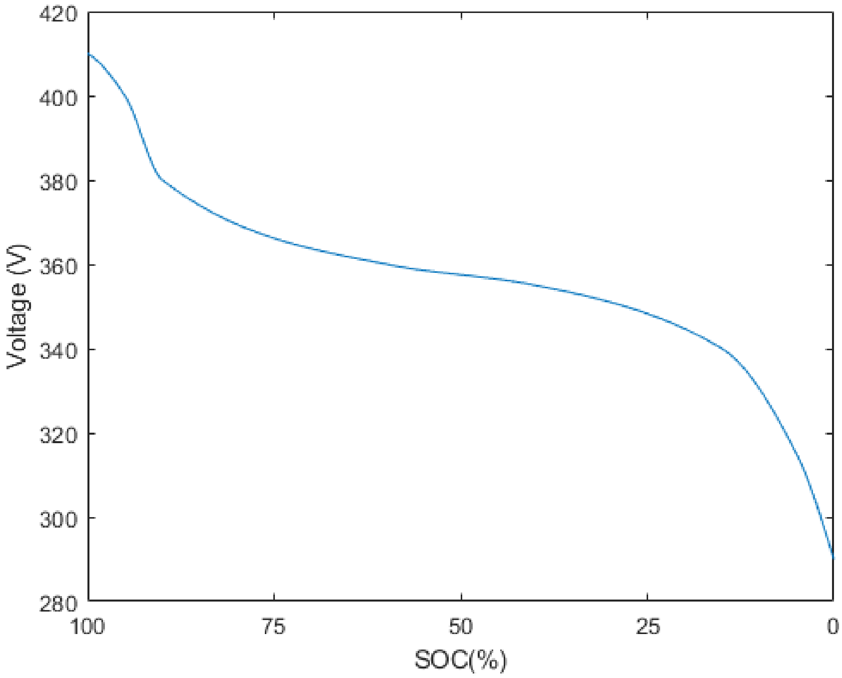


Figure 3.9: DC-link voltage as a function of SOC

3.9 Design of closed-loop control

The aim of the closed-loop control is to regulate the output power and the output voltage to a fixed value. To design a feedback controller of the DC/DC converter the transfer function of the model is needed. There are two methods to obtain the transfer function of the model, state-space modeling or small-signal modeling [20]. The state-space modeling approach involves describing the dynamics of the converter in terms of its state variables, inputs and outputs, where the state variables represent the internal states of the converter. Further, the state-space model is transformed into the frequency domain using Laplace transforms [20], which converts the time-domain differential equations into algebraic equations in the s-domain. Finally, the transfer function can be obtained by taking the ratio of the output to the input in the Laplace domain. The small-signal modeling technique is based on linearizing the DC/DC converter around its operating point [20]. To analyze the small-signal response of the converter, it is necessary to perturb both its inputs and states, in order to derive the small-signal model of the converter. Which involves writing the small-signal equations for the perturbations in terms of the small-signal inputs and states. By using the Laplace transform the small-signal model is transformed into the frequency domain, where the transfer function of the model is obtained by the ratio of the output to the input in the Laplace domain [20].

These methods require a detailed understanding of the converter's dynamics and extensive mathematical calculations to derive the transfer function. This can be a challenging task, particularly for complex converters with non-linear behavior.

To simplify the process and save time, the project uses a PI controller inspired by PLECS demo models, where a pre-built model is re-modified. PLECS offers pre-built models and libraries of components that can be customized for specific applications. These models are designed to be easily modified, making it simple for users to create and test their control algorithms. By adjusting the proportional and integral gain of the controller shown in figure 3.10, the system performance could be monitored continuously. Using the voltage and current sensors, the controller could continuously regulate the output power to the desired value by adjusting the phase shift modulation of the PWM signals. The controller is a cascaded discrete PI controller with an outer voltage loop and an inner current loop. The outer loop adjusts the voltage, while the inner loop adjusts the current, allowing for precise control of the output power.

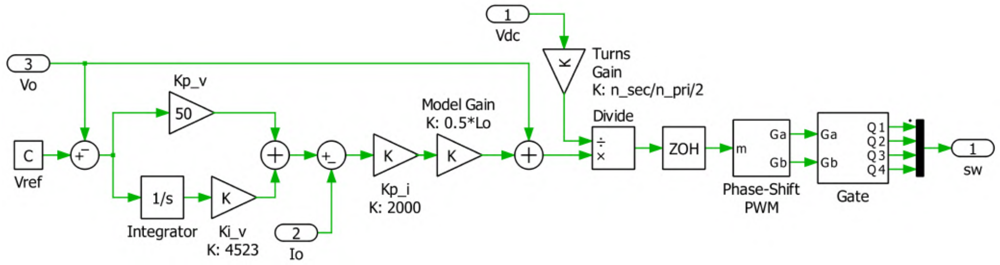
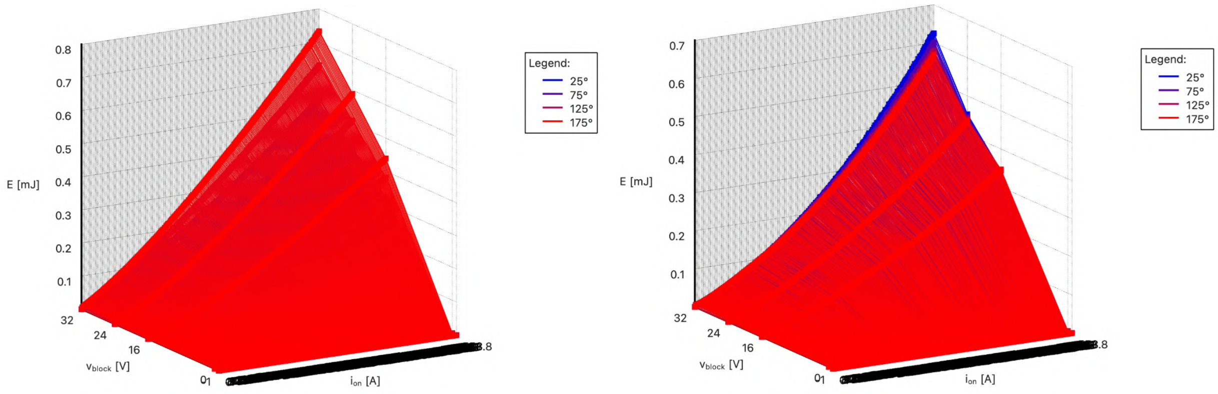


Figure 3.10: Feedback controller model

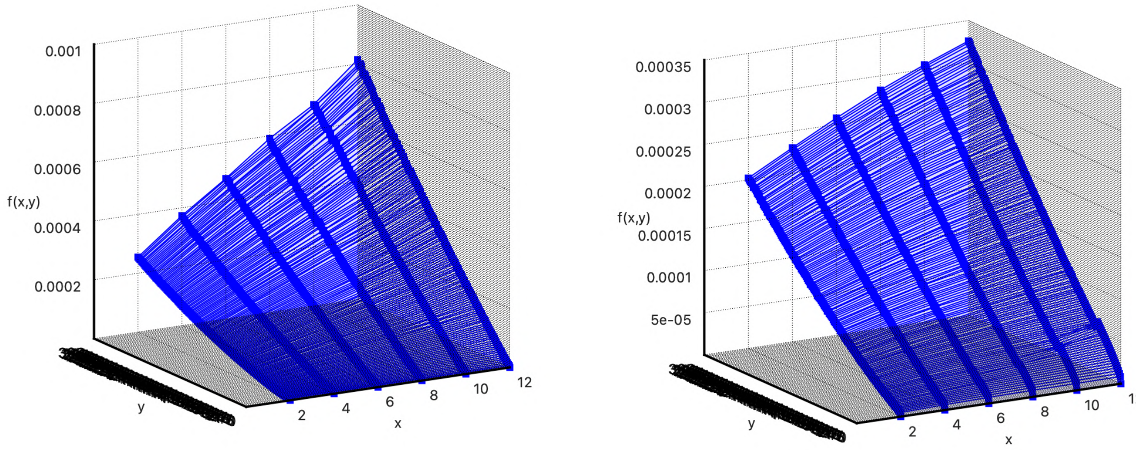
3.10 Determination of losses

The PLECS Component Library is utilized to compute the switching losses, and through the PLECS software, power loss data for the Switch MOSFET and Diode can be imported from standardized (.XML) files. As seen in figure 3.11, 3.13 and 3.14a, the conduction losses, turn-on & turn-off losses of the MOSFET and body diode are specified using the xml files of the component provided by the datasheet of the product. The switching losses are calculated with the help of the 3D lookup tables where the losses in mJ are expressed as a function of the current through it, voltage across it as well as the temperature. PLECS uses interpolation by default to estimate a point which is not explicitly defined. The lookup table is combined with a formula which includes customized lookup tables of the turn-on and turn-off losses as a function of the gate resistance and current through the device, see figure 3.12. The losses in figure 3.11 are then multiplied by a factor coming from the customized tables. Further, the losses are seen as impulses at the switching instance and therefore the average of the impulses is computed with a sampling time of 1/f.



(a) Turn-on losses **(b)** Turn-off losses

Figure 3.11: Turn-on & Turn-off losses of the MOSFET

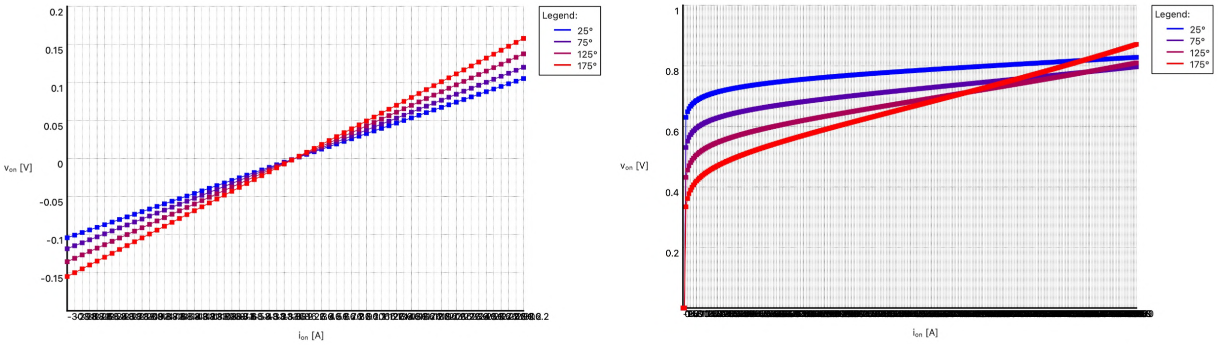


(a) Turn-off losses as a function of R_G & I_{DS} **(b)** Turn-on losses as a function of R_G & I_{DS}

Figure 3.12: Custom table where x-R_G, y-I_{DS} ranging from 0A-307A and f(x,y) is E in Joule

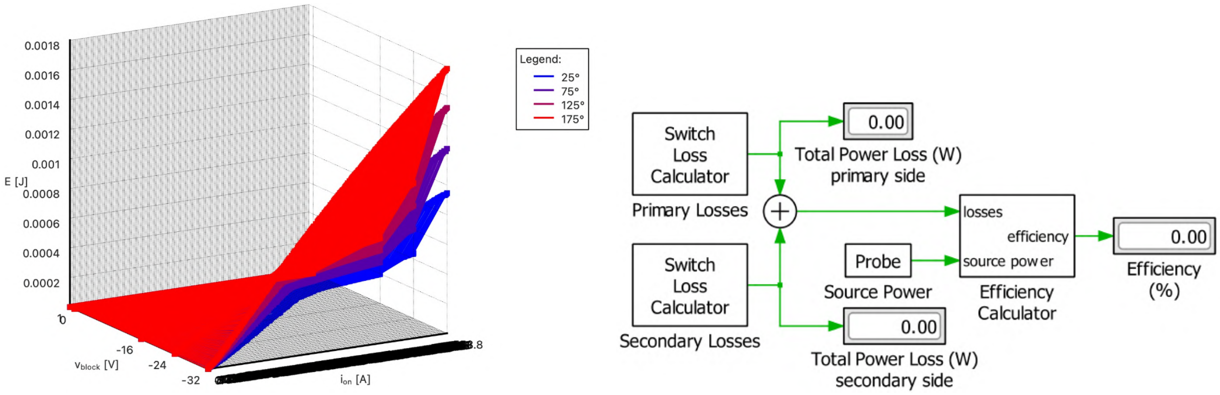
For the determination of the conduction losses there are two main approaches one can take to accurately include the on-state resistance as a function of the junction temperature. The first method is to input a variable resistance in series with the semiconductor. The junction temperature is then connected to a 2D lookup table of the normalized drain-to-source resistance which provides a resistive value for a specific temperature. The second approach is to use the I-V curves provided by the manufacturer for different temperatures and input them in the thermal library browser in PLECS which also uses linear interpolation as default. This method is supported by PLECS and gives more accuracy since the dependence of the gate voltage is also included and is therefore used in this project.

In figure 3.14b the switching loss calculator used in PLECS is seen. It is modified so that the core losses together with the probed copper losses are added to it as well as the gate driver losses for each MOSFET. The modified loss calculator is seen in Appendix 1.



(a) MOSFET conduction losses **(b)** Diode conduction losses

Figure 3.13: Conduction losses of the Diode and MOSFET



(a) Turn-off losses of the Diode **(b)** Switching loss calculator

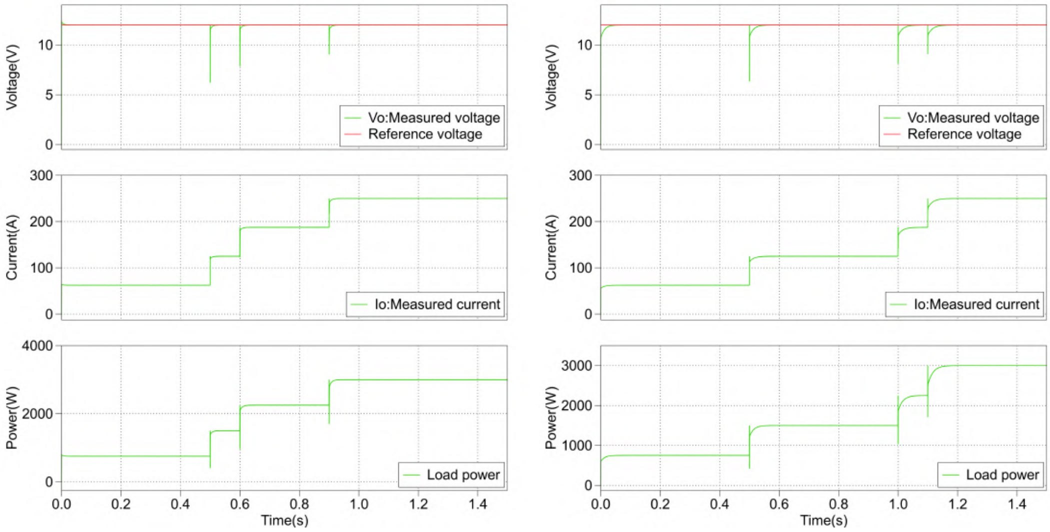
Figure 3.14: Turn-off losses of the Diode and loss calculator

Due to the temperature dependency, all the active semiconductor devices should be within a heat-sink which continuously calculates and updates the junction temperature and uses it for extraction of losses from the lookup tables.

3.11 Transient response analysis

Model verification is a crucial stage in the design and development of a DC/DC converter in order to ensure both the accuracy and dependability of the converter's performance predictions. As a result, the transient response is investigated in this subsection, which is a crucial step in determining the converter's transient response to input and load changes. Its well known that if the transient response is slow, it may cause the output voltage to deviate from the desired value for a period of time, leading to potential issues such as system instability or incorrect operation of the converters components. Conversely, if the transient response is too fast, it may lead to an overshoot or undershoot, which can cause stress on the converter and other components in the system. This will help to determine the converter's stability and how it responds to different types of input and load conditions.

To evaluate the stability of the converter models, an initial test was conducted by maintaining a constant input voltage while varying the load. As seen in figure 3.15 & figure 3.16, despite the stepwise increases in load, the desired output voltage remains constant for both PSFB & PSFB-CDR and the DAB.



(a) PSFB **(b)** PSFB-CDR

Figure 3.15: Voltage, Current and Power curves for the PSFB & PSFB-CDR

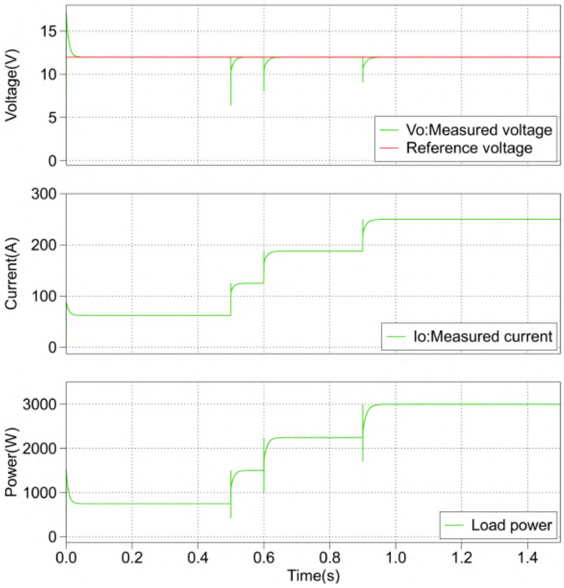
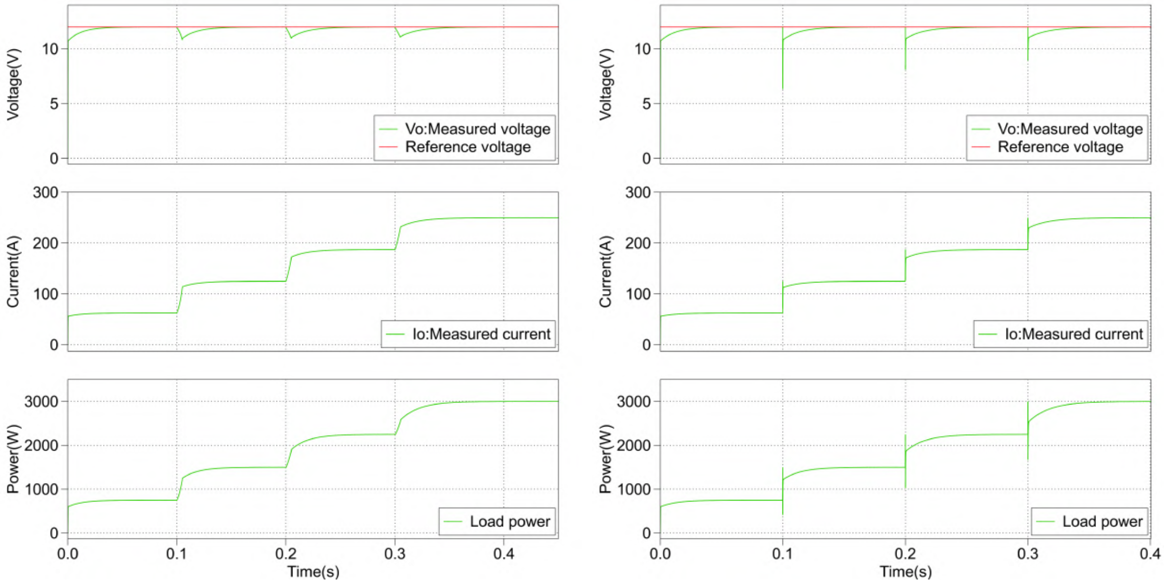


Figure 3.16: Voltage, Current and Power curves for the DAB

However, the step loading, can cause a significant voltage drop at the output of a DC/DC converter. For instance, when the load current suddenly increases from a nominal value, the output voltage drops from 12V to almost 6V, as illustrated in figure 3.15 and figure 3.16. Even if the duration of the voltage drop is short, it could cause some components in a vehicle to disconnect, leading to instability and potential damage. To prevent such voltage drops and ensure stable operation of electronic devices, it is important to gradually ramp up the load instead of applying sudden step changes. A gradual increase of the load allows the system to adjust to the changing load more smoothly, reducing transient stresses and preventing large voltage drops. Figure 3.17a demonstrates a steady ramp up of the load, while figure 3.17b describes step change of the load.

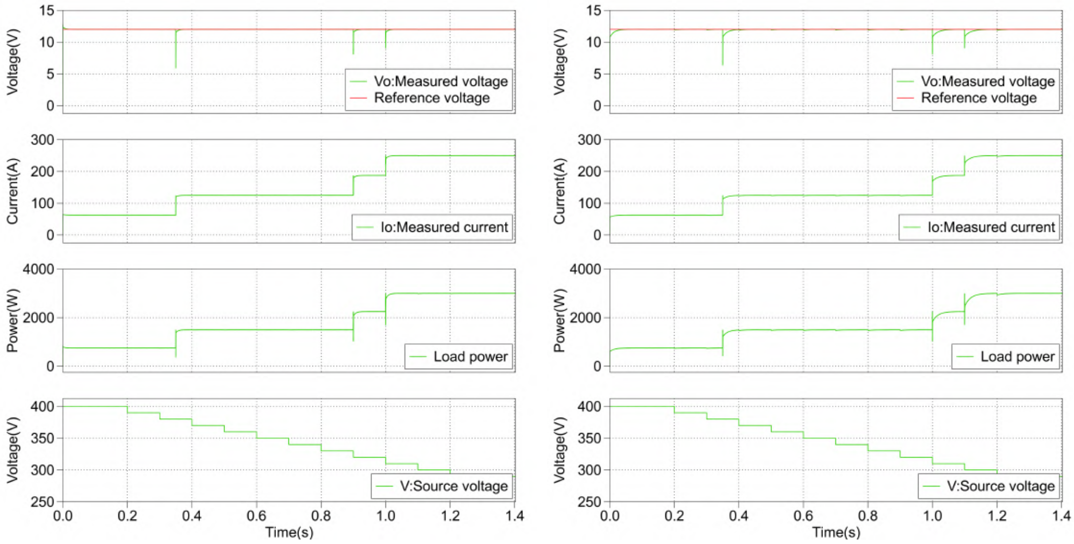


(a) Ramp loading **(b)** Step loading

Figure 3.17: Step loading and ramp loading

3.11.1 Transient response to input and load changes

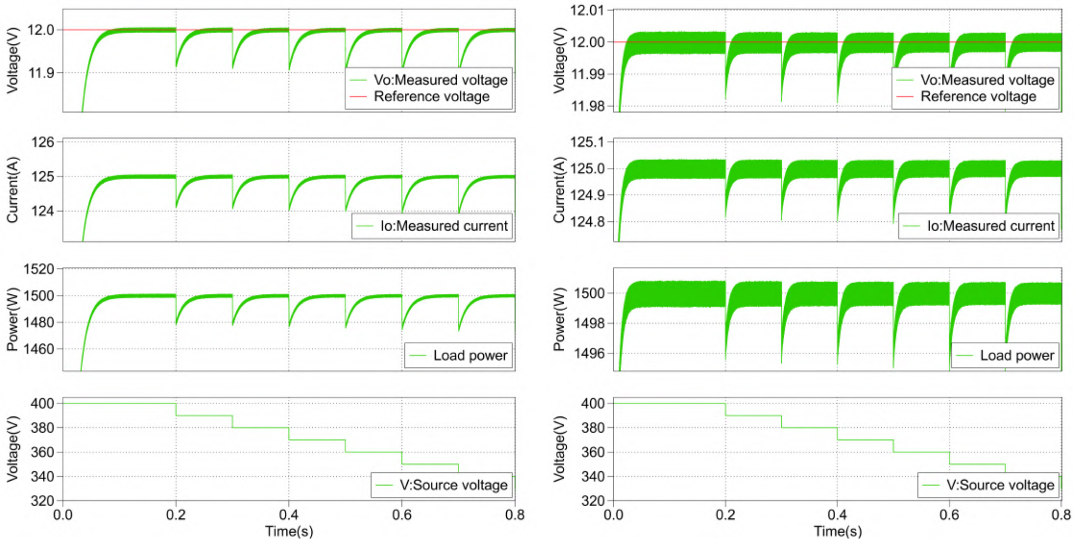
The next step was to do a test close to real-world operating conditions in order to ensure that the converter can maintain stable operation in a variety of real-world conditions, which may not be accurately reflected in the previous analysis where only the load was varied. In this test, the input voltage is decrease by 10V in every 100ms in order identify any potential stability issues or limitations of the converter. The models remain stable as can be seen in figure 3.18 & figure 3.20b, despite being subjected to various stress conditions, such as changes in load or input voltage.



(a) PSFB **(b)** PSFB-CDR

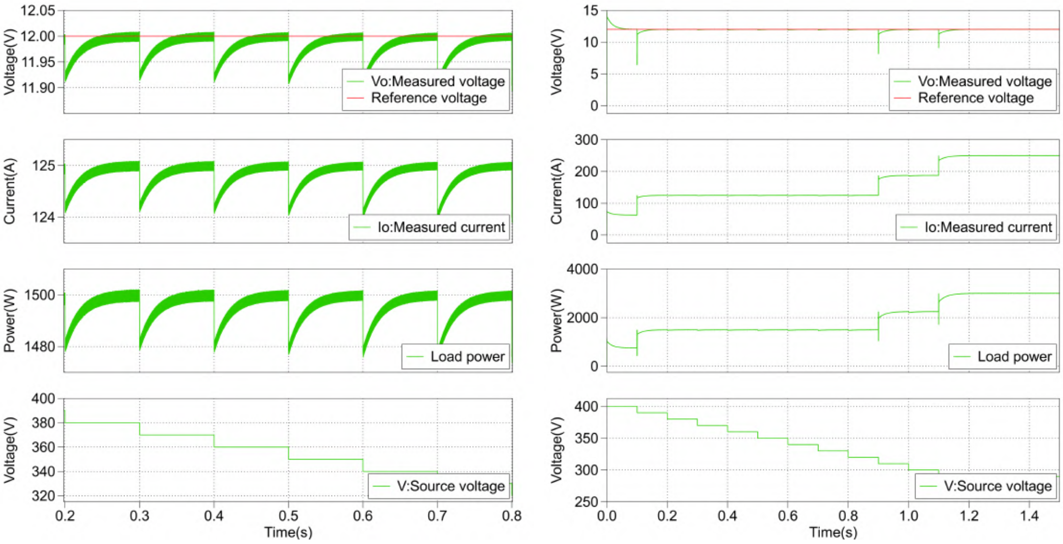
Figure 3.18: Voltage, Current and Power curves for the PSFB & PSFB-CDR

Upon closer examination of figure 3.19 and 3.20a, it is observed that the PSFB-CDR demonstrates the highest undershoot, measuring 100mV, whereas the PSFB and DAB exhibit undershoots of 20mV and 50mV, respectively. Thus, the converter is able to maintain a stable output voltage despite a small drop in voltage below the desired level before returning to the steady-state voltage. This suggests that the converter's control loop is well-designed and able to prevent instability or potential damage to both the converter and the equipment being powered.



(a) PSFB-CDR **(b)** PSFB

Figure 3.19: Enlarged image of the Voltage, Current and Power curves for the PSFB-CDR & PSFB



(a) DAB zoomed waveforms

(b) DAB waveforms

Figure 3.20: Varying input voltage with varying load for the DAB

3.11.2 Test data for evaluation of control system and losses

In figure 3.21, the handmade test data that will be used for examining the response behaviour of the control system and give a better picture of the losses in a more realistic simulation is seen. Here it is assumed that the EV has an Electronic Control Unit (ECU) where data from sensors all around the vehicle is sent to and handled for autonomous driving. At "Driver mode ON", the ECU is expected to require a minimum of 1800W for autonomous driving.

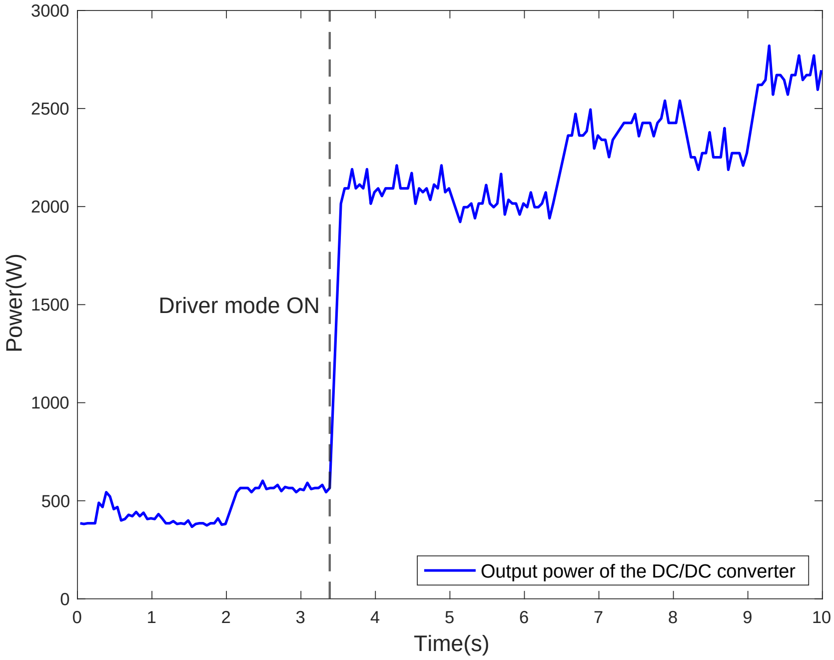


Figure 3.21: Output power of the DC/DC converter with respect to time

4

Results

4.1 Efficiency-load curves

To see at what load conditions the different topologies operates in with the highest efficiency, the load in PLECS is ramped from 300W corresponding to 10% of the load to 3000W corresponding to 100% of the load. The power level of the highest efficiency is highlighted in the efficiency-output power level graphs with a deviation of ±5% for $V_{in} = 400V$ and $V_{in} = 290V$. The apportionment of losses is shown and compared to determine the power levels for best usage and to later discuss further improvements that could help to reduce some specific loss.

4.1.1 DAB

As seen in figure 4.1, the DAB operates with higher efficiency on lower input voltage and at lower load conditions. The main contributors to that are the primary switching losses which are almost doubled at 100% load looking at figure 4.2 and also a significant increase in the secondary conduction losses at high power levles. As expected though, the primary conduction losses are lower at higher voltage ratings due to lower current flowing through the devices at a specific load condition.

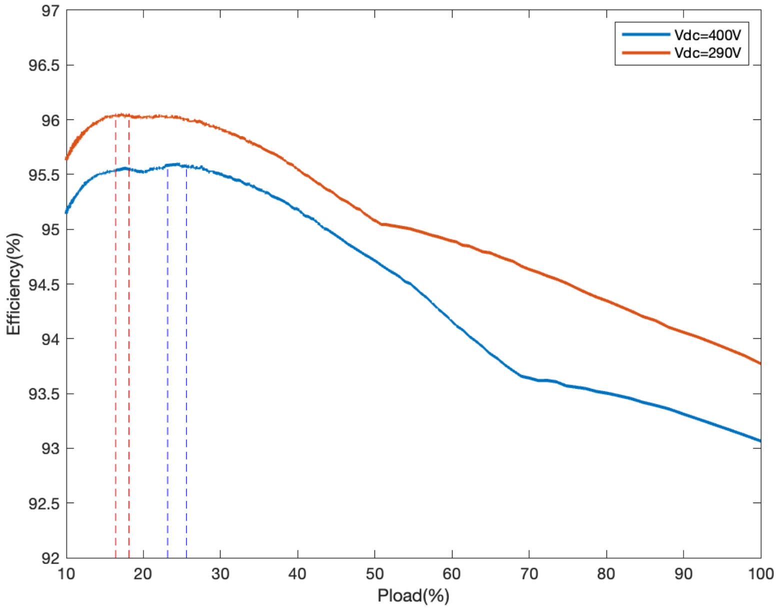


Figure 4.1: Efficiency-Load curve for DAB

The expectation was that the efficiency of the DAB would be the lowest from 10% to somewhere around 40% due to the methodology of the parameter calculations and overall model design. As expected though, the DAB has the lowest efficiency at higher loads due to the high secondary current through four Si MOSFETs instead of two as for the other topologies.

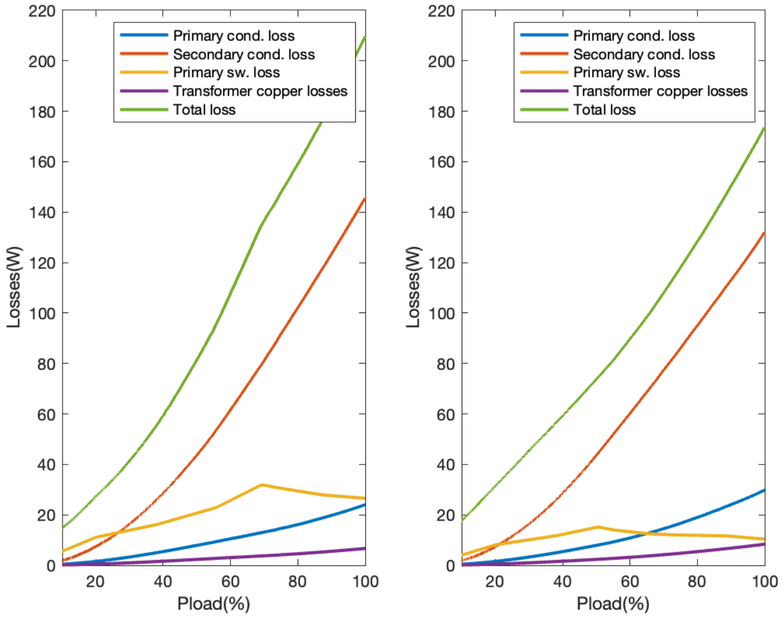


Figure 4.2: Contribution of losses for the DAB at 400V(left) and 290V(right)

4.1.2 PSFB

For the PSFB, the same result is seen where the secondary conduction losses and primary switching losses increases at higher input voltage. Having higher switching losses on the primary side is expected since higher voltage across the switches causes higher voltage stress during both turn-on and turn-off. The reason for higher secondary losses is that the body-diode on the synchronous rectification MOSFETs is conducting for a longer period of time leading to overall higher losses. To reduce the conduction time of the MOSFETs body-diode, the leakage inductance of the transformer is increased which leads to a longer time for the current to ramp up or down due to the decreased $\frac{di}{dt}$.

The results of that is seen in the waveforms in figure 4.4 which leads to a reduction of 31.7% on the secondary conduction losses. Using a three times larger leakage inductance was not suitable for the control system at lower voltage levels meaning that the leakage inductance was selected at a value 1.7 times larger resulting in the decrease of secondary conduction losses by 7.2%. The downside of increasing the leakage inductance is as mentioned the effect it has on the control system and its inability to handle transients well, as well as increased switching losses. Since SR is used on the secondary side, the switching losses there remain zero. But on the primary side, they are increased by roughly 6% which in comparison to the amount of power that the reduced conduction losses provides, it is still small and gives a better overall efficiency.

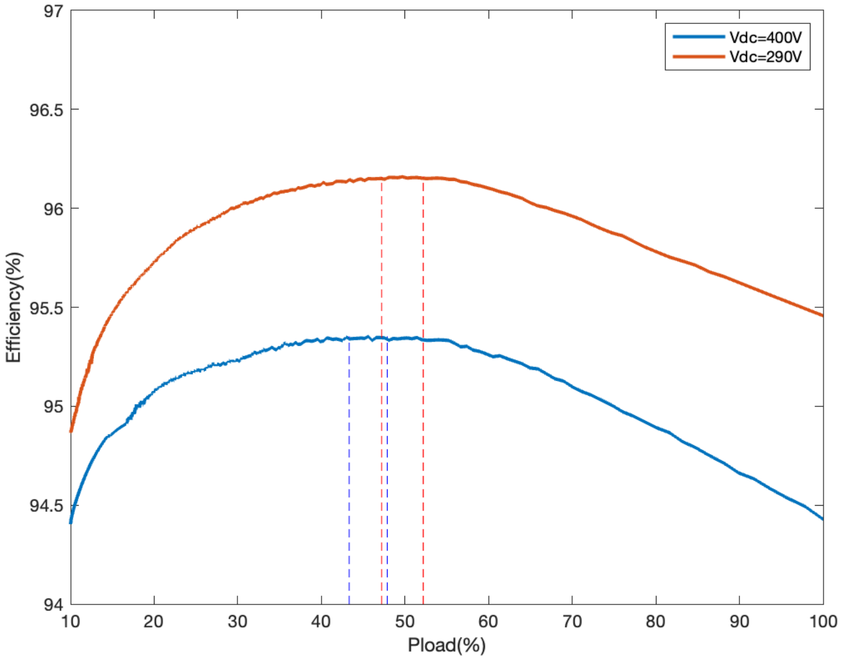
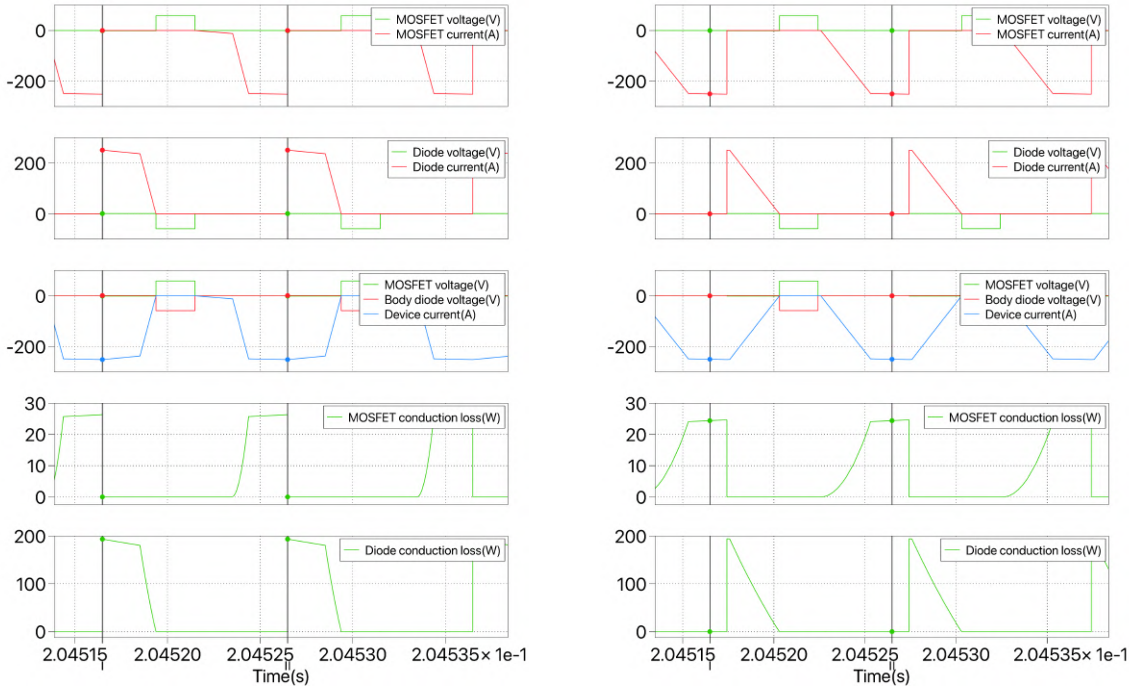


Figure 4.3: Efficiency-Load curve for PSFB



(a) Waveforms at Lr

(b) Waveforms at Lr·3

Figure 4.4: PSFB waveforms at different leakage inductances

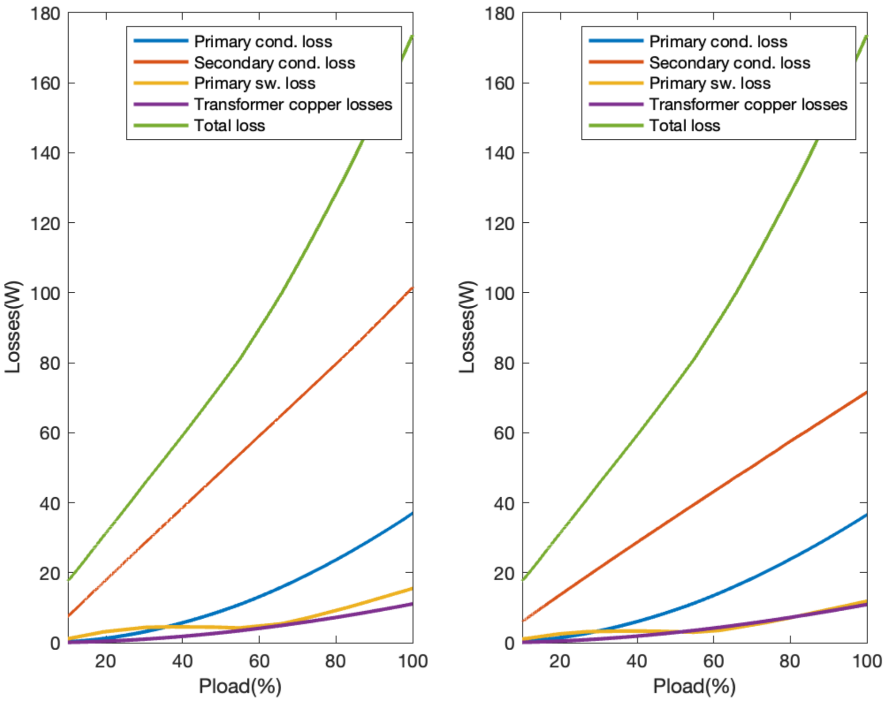


Figure 4.5: Contribution of losses for the PSFB at 400V(left) and 290V(right)

4.1.3 PSFB-LLC

For the PSFB-LLC it is seen that the secondary conduction losses are reduced due to lower body-diode conduction time as stated previously, but it is also seen that the switching losses on the primary side are increased roughly twice as much which is not wanted for an LLC configuration. This proves that the design of the series capacitor and inductor are not sufficient enough to decrease the switching losses.

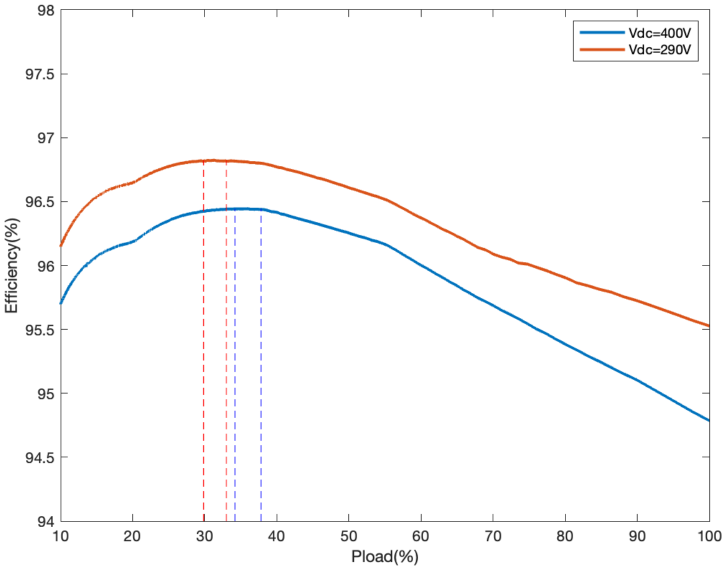


Figure 4.6: Efficiency-Load curve for PSFB-LLC

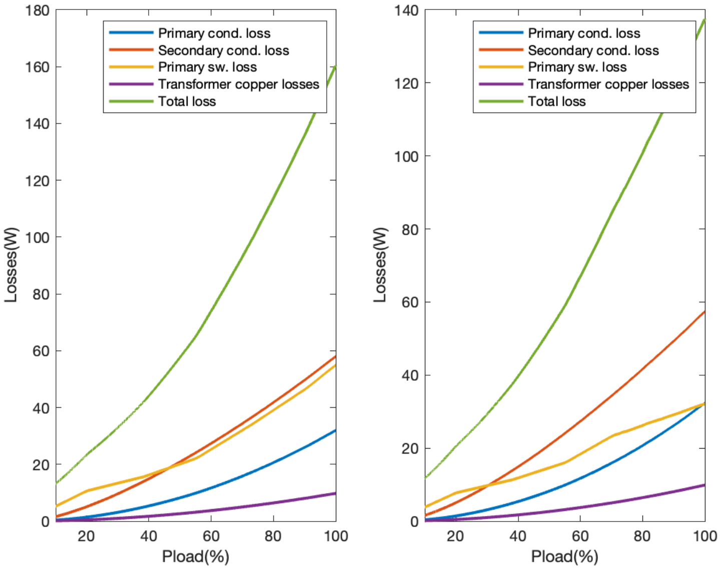


Figure 4.7: Contribution of losses for the PSFB-LLC at 400V(left) and 290V(right)

4.1.4 PSFB-CDR

As seen in figure 4.3, the difference in efficiency at 400V and 290V is not remarkable as for the other topologies which is mainly due to a better design of the model and a more suitable control system. In figure 4.9 it is notable that the secondary conduction losses are decreased at higher input voltage in comparison for the cases of DAB and PSFB.

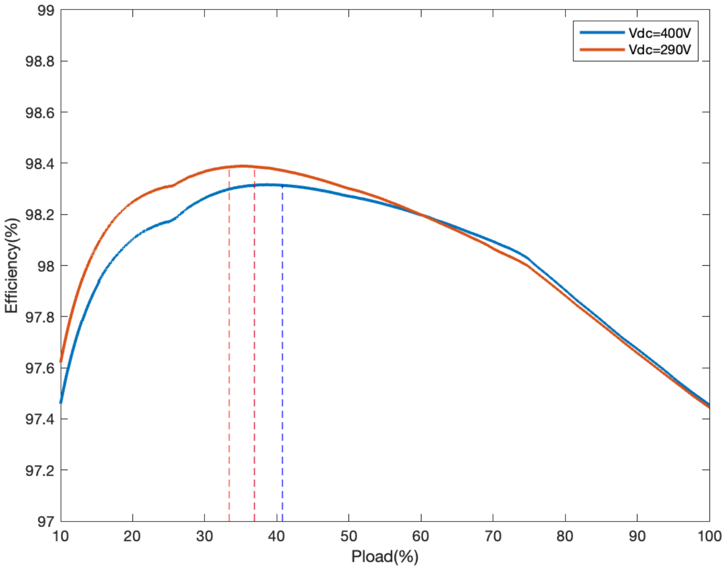


Figure 4.8: Efficiency-Load curve for PSFB-CDR

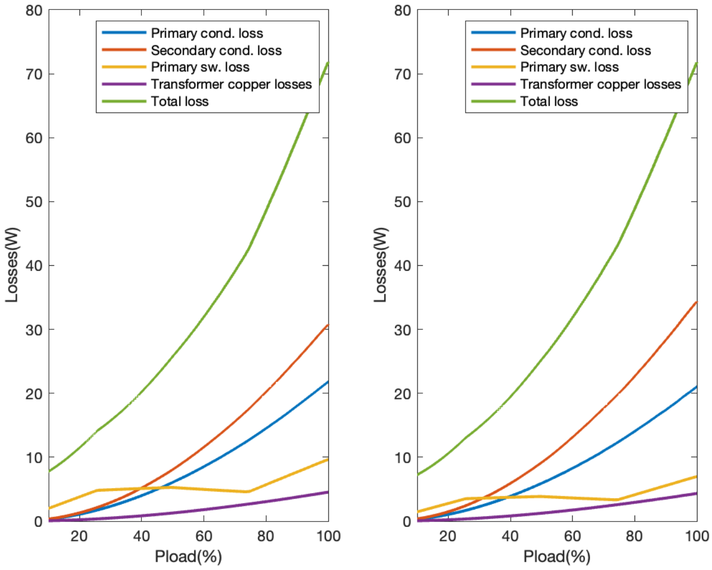


Figure 4.9: Contribution of losses for the PSFB-CDR at 400V(left) and 290V(right)

4.1.5 PSFB-CDR-LLC

As seen in figure 4.10, the PSFB-CDR-LLC model attains the highest efficiency over the whole range of operation from 10% to 100% load condition. In comparison to the PSFB-CDR, the main difference is the reduction of primary switching losses at load condition >75% seen in figure 4.11. This is due to the improvement of soft switching where the parameters of the series connected inductor and capacitor were designed for higher output levels meaning that it would provide the best improvements on those levels.

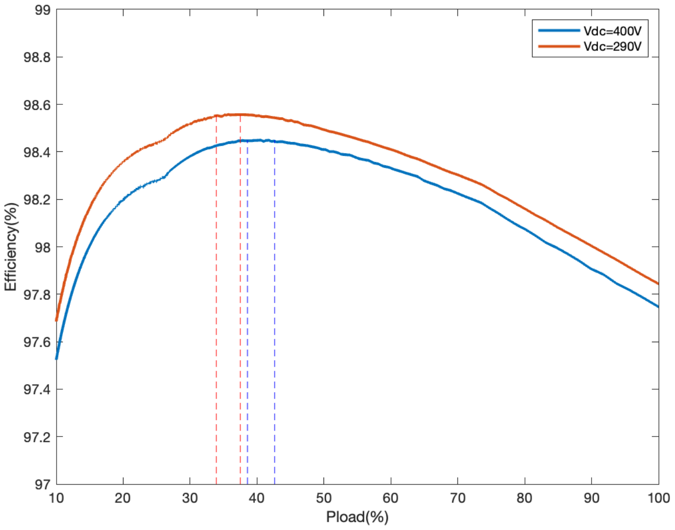


Figure 4.10: Efficiency-Load curve for PSFB-CDR-LLC

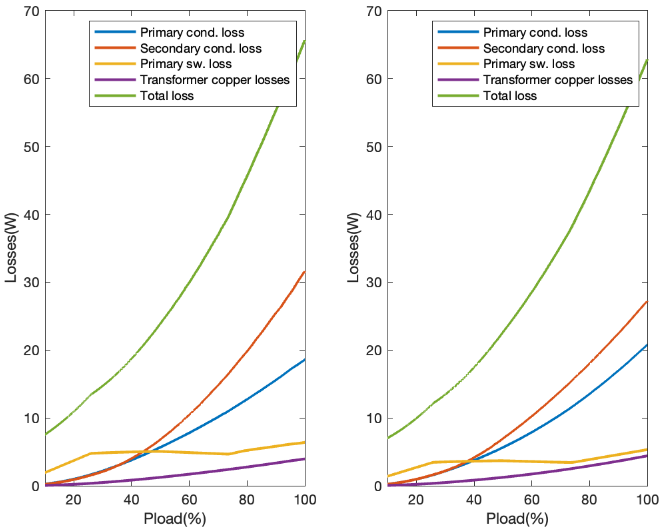


Figure 4.11: Contribution of losses for the PSFB-CDR-LLC at 400V(left) and 290V(right)

4.1.6 Comparison of losses for the different topologies

As seen for the majority of topologies, the efficiency is higher over the whole operating range at lower input voltage. During the investigation it was seen that the input power at 290V was a bit lower than at 400V which affects the calculation of efficiency and that the actual MOSFET losses on the secondary side reduced when the input voltage increased, but that the conduction losses of the body-diode increased due to higher $\frac{di}{dt}$ at higher input voltage meaning it conducted for a longer period of time. The explanation for this could be the reverse recovery losses of the body-diode which are higher at high $\frac{di}{dt}$ due to a bigger dip and more oscillations before the current through the body-diode reaches zero.

The comparison of the topologies at 3kW output is seen in figure 4.12 where it is clear that the PSFB-CDR-LLC has the lowest losses throughout the whole circuit. The impact of having a better utilised transformer in the CDR configuration is seen by having both the primary and secondary copper losses reduced in comparison to the centre-tapped transformer used in the PSFB. The higher amount of semiconductor devices results in higher secondary losses meaning that there will be a drastic decrease of efficiency at high output power levels as can be seen for the DAB. Using the LLC configuration on the PSFB-CDR reduces all the losses expect the secondary conduction losses which is a good accomplishment and implemented design. The switching losses decreases with 38% and the primary conduction losses with around 15% in comparison to not having any LLC configuration.

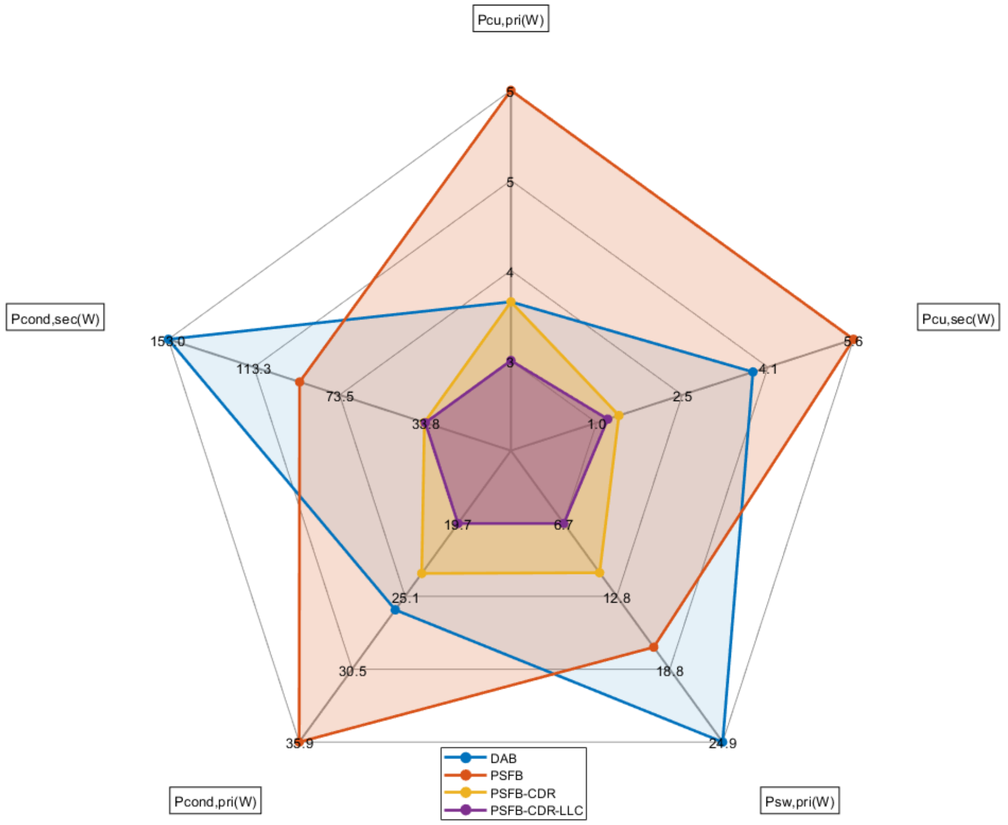


Figure 4.12: Comparison of the loss distribution at $V_{in} = 400V$ and $P_{out} = 3kW$

A comparison of the Total Harmonic Distortion(THD) of each topology is also made which is seen in figure 4.13. The THD is computed from the current waveforms of the primary and secondary transformer, primary and secondary MOSFETs and the output current.

Consideration of harmonic content flowing in the DC/DC converter is of great importance since they cause additional transformer losses which results in excessive heating. The addition temperature rise due to the harmonic content directly affects the wearing of the insulation materials in the transformer which reduces the lifetime of it. The additional losses are mainly copper losses in the windings due to the joule effect and the eddy current losses in the transformer core. Harmonic content over the switches is also important since higher harmonic content results in higher stress at the switching instance which also reduces lifetime of the device in the long run. High THD also increases the Electromagnetic Interference (EMI) which has to be kept within the IEC regulations in CISPR 25:2021 since it affects reliability and stability of the ECU.

It is seen that the PSFB-CDR has the highest THD in the transformer currents and that there is an improvement with the LLC configuration. For the output current it is the opposite where the PSFB and DAB has the highest THD. The THD in the currents flowing through the MOSFETs is divided where the PSFB-CDR with and without LLC has low THD on the primary while for the PSFB and DAB it is the opposite.

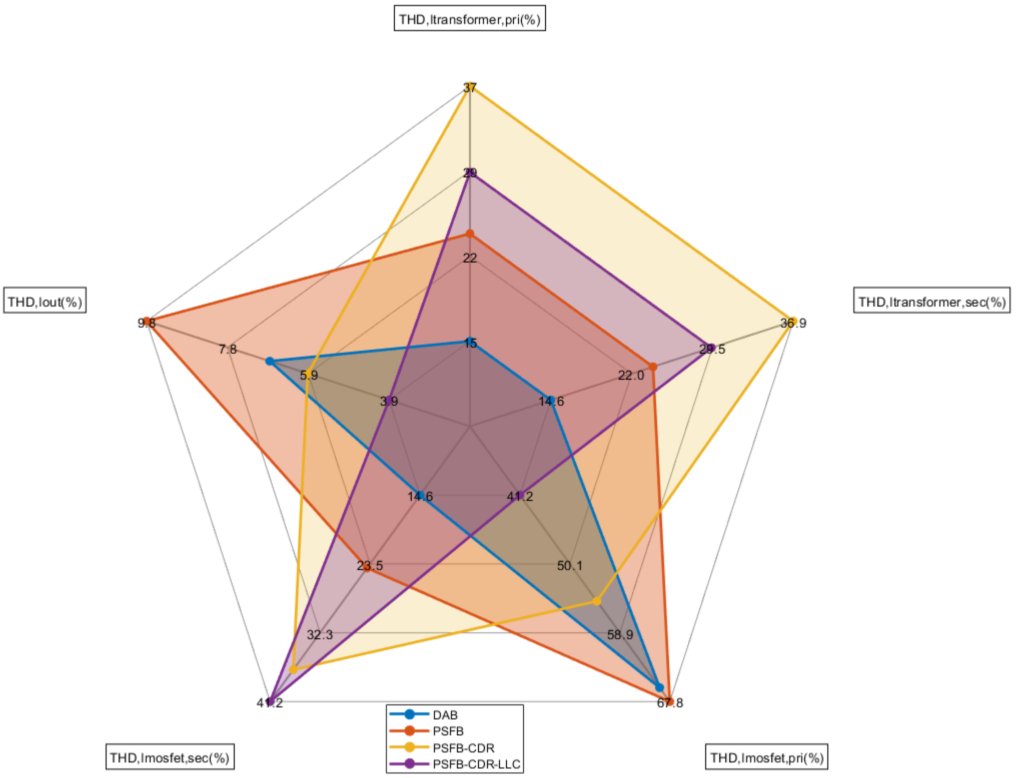


Figure 4.13: THD at $V_{in} = 400V$ and $P_{out} = 3kW$

4.2 Losses of the topologies at different cases

In order to get a good understanding of the converters, testing was conducted using GaN, SiC and Si semiconductor devices. The following four test cases were carried out:

- Case 1: GaN MOSFETs on primary & Si MOSFETs on secondary
- Case 2: SiC MOSFETs on primary & Si MOSFETs on secondary
- Case 3: GaN MOSFETs on primary & SiC schottky diodes on secondary
- Case 4: SiC MOSFETs on primary & SiC schottky diodes on secondary

Due to the high secondary current, which reached a maximum rating of 250A, the GaN devices could only be used on the primary side. The available GaN devices had high voltage rating and low current which made them a great fit for the primary side. On the other hand, the secondary side was tested with both Si MOSFETs and SIC schottky diodes. However, the schottky diodes had a low current rating of 50A, therefore a parallel connection of 6 diodes was needed in order to carry the large load current.

Figure 4.14 illustrates the obtained losses during the four test cases together with the converters efficiency under each test case. From the figure it can be seen that the converter efficiency worsens going from case 1 to case 4. The primary loses are mainly reduced when the GaN is used on the primary in case 1 and case 3. When SiC Schottky diodes are used in case 3 and case 4, there has been an evident increase in secondary losses. This can be explained by the fact that SiC diodes are typically designed for higher voltage applications. Meanwhile, the transformer losses are mainly remained the same for all test cases.

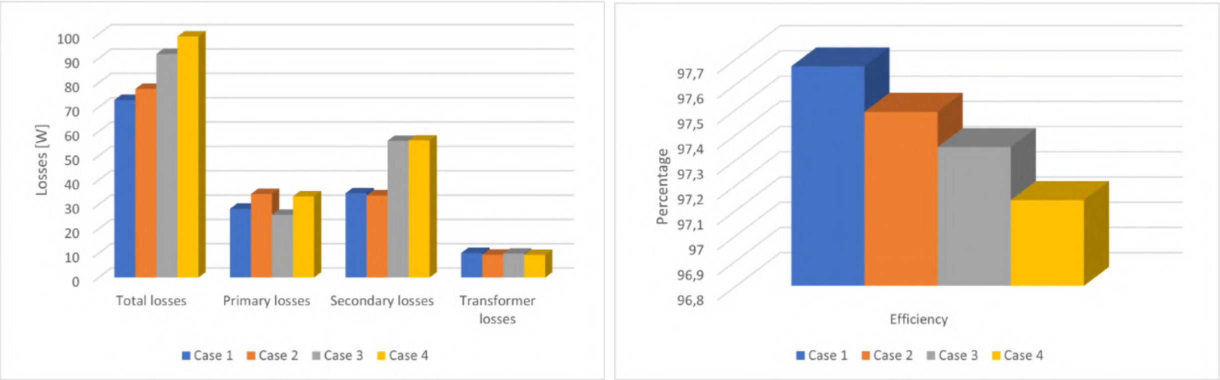


Figure 4.14: Loss analysis of the PSFB-CDR under four different operating conditions

Despite having increased losses as going from case 1 to case 4, the obtained efficiency is 97.14% at worst case and 97.67% at the best case, as shown in figure 4.14.

Similarly, the same test scenario are conducted for the PSFB-center-tapped topology, where its results for the losses and efficiency are presented in figure 4.15. The highest losses occur during case 2, when SiC MOSFETs are used in the primary and the Si MOSFETs on the secondary. It is also notable that the total losses of the secondary side decreases when the SiC schottky diodes are used. Also, when GaN is used in the primary side, the losses on the primary are almost halved, while the transformer losses remains similar across all the test cases.

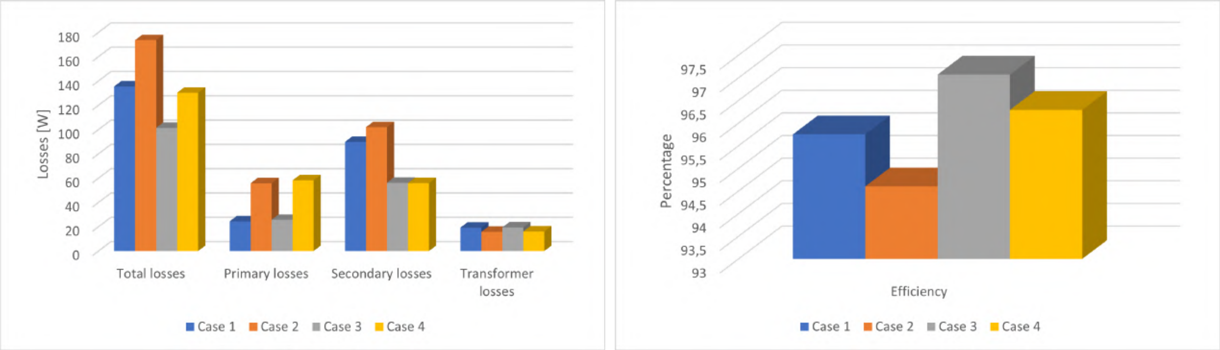


Figure 4.15: Loss analysis of the PSFB-center-tapped under four different operating conditions

Based on the result presented in figure 4.15, the center-tapped topology achieved a maximum efficiency of 97.07% during test case 3 where GaN MOSFETs were combined with SiC schottky diodes. While the lowest efficiency of 94.6% was obtained during test case 2.

Figure 4.16 presents the result of the case scenarios for the series resonant PSFB-CDR-LLC. The PSFB-CDR-LLC topology had similar characteristic in terms of the losses in the primary, secondary, and transformer as the previous current doubler rectifier which it result presented in figure 4.14. The result worsens as going from case 1 to case 4. However, the efficiency is slightly better for the series resonant in the first three cases. The series resonant is best at case 1 with an efficiency of 97.95% and worst in case 4 with efficiency of 97.03%.

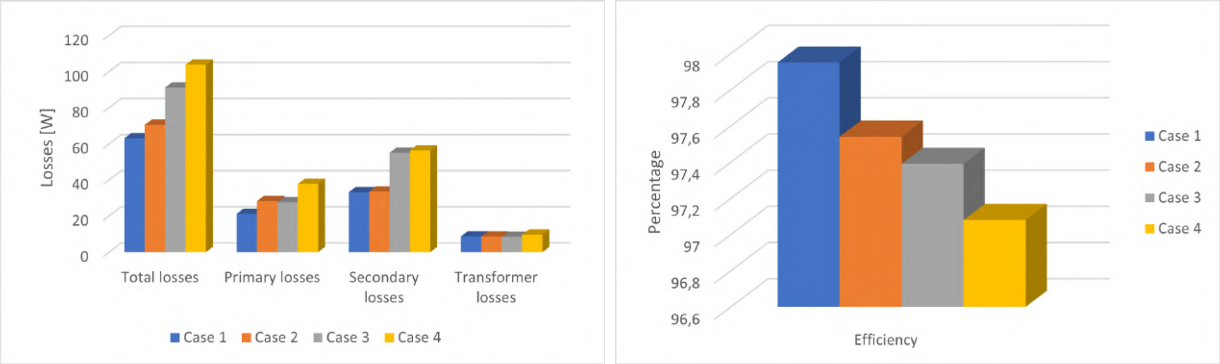


Figure 4.16: Loss analysis of the PSFB-CDR-LLC under four different operating conditions

The result of the series resonant center-tapped topology during the varying operating conditions are presented in figure 4.17. When comparing the obtained result with the non resonant topology in figure 4.15, the LLC PSFB-center-tapped shows reduced losses for case 1 and case 2, while the losses are slightly increased for case 3 and case 4. Thus, the highest efficiency occur in case 3 and lowest efficiency is observed at case 2, similar to its previous non resonant topology. However, the losses of the primary, secondary and the transformer have similar behaviour as the previous non resonant center-tapped topology.

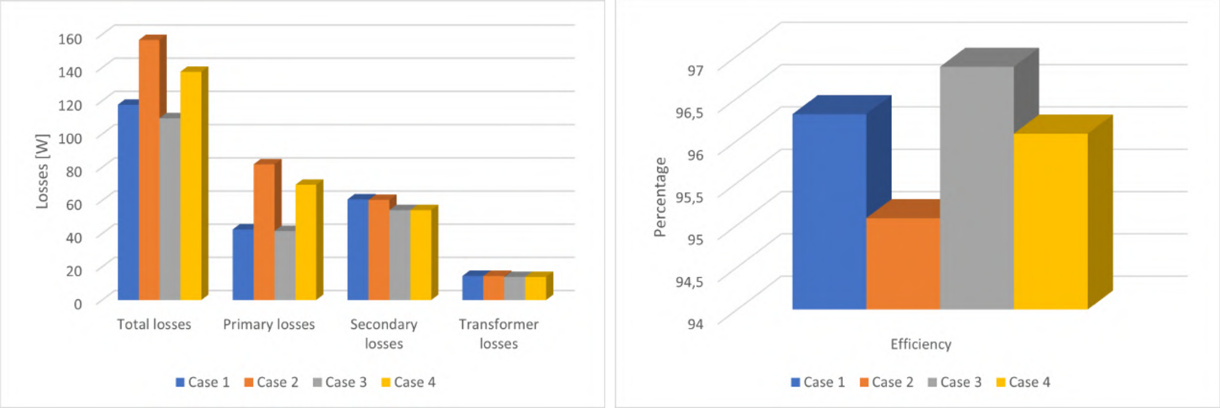


Figure 4.17: Loss analysis of the LLC PSFB-center-tapped under four different operating conditions

The result of the DAB during the operation conditions are presented in figure 4.18. For cases 3 and 4, the DAB was transformed into a single active bridge (SAB), since only the primary side utilized active switches (MOSFETs) and the secondary utilized diodes, resulting in unidirectional power flow. The total losses are highest for the DAB and the SAB when compared to the other topologies during the case studies. However, the secondary losses are highest for the DAB and the SAB, even though the lowest efficiency obtain is during case 2 which is 94.45% while the best efficiency is observed during case 3. Despite achieving a maximum efficiency of 95.79% in case 3, both the DAB and SAB experience the highest secondary losses. Moreover, even in the scenario with the lowest efficiency, which occur in case 2 with an efficiency of 94.45%, the secondary losses remain the highest for the topologies.

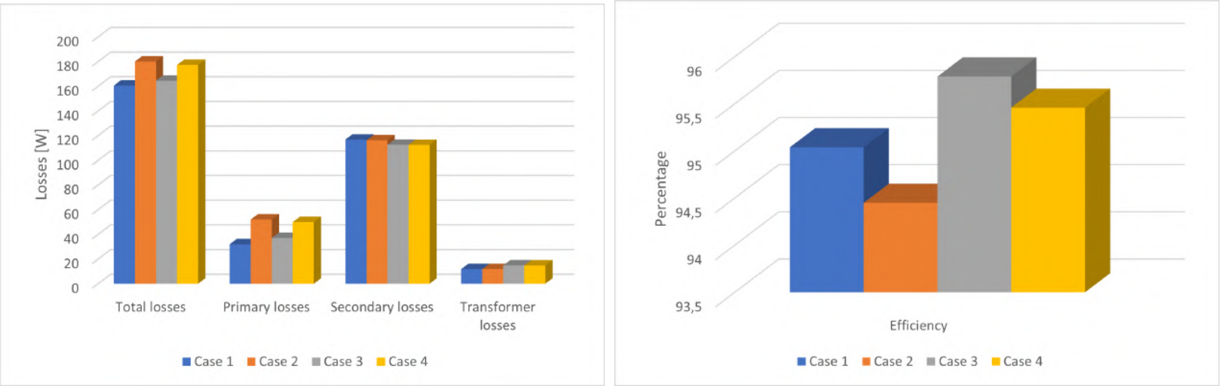


Figure 4.18: Loss analysis of the DAB/SAB under different operating conditions

Table 4.1, summarizes the total losses and the total efficiency obtained during the case approaches, and table 4.2 analyzes in detail the primary losses. The use of synchronous rectification and the achieving of ZVS on the secondary side significantly minimized switching losses, which became negligible. As a result, the secondary side mainly experienced conduction losses, which were mainly created by the low on-state resistance of the Si MOSFET. Furthermore, because there is little minority carrier injection, the SiC schottky diode mainly experiences conduction losses. In addition, the peak reverse recovery current is significantly reduced, which causes the active switch's turn-on switching losses to be negligible [38]. However, in the case of primary losses, both conduction and switching losses were observed. The GaN and SiC MOSFETs shared a comparable on-state resistance of 50 mΩ and 60 mΩ, respectively, resulting in similar conduction losses. However, upon reviewing Table 4.2, it becomes clear that the SiC MOSFET has higher switching losses compared to the GaN MOSFET.

Table 4.1: Obtained losses & efficiency during the case approaches

		Case 1	**Case 2**	**Case 3**	**Case 4**
Center-tapped	Tot.Loss(W)	135.57	173.72	101.46	130.35
	Tot.Eff(%)	95.75	94.60	97.07	96.29
CDR	Tot.Loss(W)	72.97	77.54	91.86	99.05
	Tot.Eff(%)	97.67	97.49	97.35	97.14
DAB	Tot.Loss(W)	160.63	180.1	164.49	177.28
	Tot.Eff(%)	95.04	94.45	95.79	95.46
LLC center-tapped	Tot.Loss(W)	117.68	156.61	109.57	137.5
	Tot.Eff(%)	96.31	95.08	96.87	96.08
LLC CDR	Tot.Loss(W)	63.08	70.54	91.22	103.81
	Tot.Eff(%)	97.95	97.71	97.39	97.03

Table 4.2: Primary losses

		Case 1	**Case 2**	**Case 3**	**Case 4**
Center-tapped	Cond.loss(W)	22.8	39.78	23.22	41.21
	Sw.loss(W)	3.63	16.06	2.5	17.01
CDR	Cond.loss(W)	24.6	23.64	23.32	23.2
	Sw.loss(W)	3.65	10.72	2.5	10.18
DAB	Cond.loss(W)	24.36	28.23	33.49	37.67
	Sw.loss(W)	8.53	24.97	3.59	12.32
LLC center-tapped	Cond.loss(W)	30.5	36.16	31.74	36.18
	Sw.loss(W)	12.01	46.64	9.8	33.19
LLC CDR	Cond.loss(W)	17.74	20.78	22.02	24.84
	Sw.loss(W)	3.43	7.52	5.49	12.94

4.3 Hand calculated losses and comparison

The hand calculated losses are used to make sure that the software gives reasonable results and are therefore used as a standpoint to make necessary adjustments. The total power dissipated from the semiconductor device is needed for the design of the heat-sink to determine the appropriate sink-ambient thermal resistance which will keep the junction temperature within an acceptable range. All the hand calculated losses are made at $V_{in} = 400V$, $P_{out} = 3kW$ and at $T_{junction} = 70°C$.

For calculation of the PSFB-CDR losses, the total losses on the primary side MOSFET are expressed as

$$P_{tot,pri} = P_{cond,pri} + P_{sw,pri} + P_{gate,pri} \tag{4.1}$$

when assuming that we have hard switching. The transformer losses taken into consideration are the DC copper losses and the iron core losses. For the DC copper losses, the RMS current through primary and secondary side of the transformer is calculated with (3.10)

$$I_{trafo,pri} = \frac{I_{out}}{2}\frac{N_s}{N_p} = 13.9A \tag{4.2}$$

$$I_{trafo,pri} = \frac{I_{out}}{2}\sqrt{2Ph_{eff}} = 122.5A \tag{4.3}$$

meaning that the DC copper losses are

$$P_{Cu,pri} = R_{Cu,pri} I^2_{trafo,pri} = 3.8W \tag{4.4}$$

$$P_{Cu,sec} = R_{Cu,sec} I^2_{trafo,sec} = 1.5W \tag{4.5}$$

Before using (2.36) for the conduction losses of the MOSFETs, the RMS current through them is determined as

$$I_{M,pri} = \frac{I_{trafo,pri}}{\sqrt{2}} = 9.82A \tag{4.6}$$

$$I_{M,sec} = I_{out}\sqrt{\frac{Ph_{eff}}{2} + \frac{1}{4}} = 175A \tag{4.7}$$

which gives the conduction losses of

$$P_{M,cond,pri} = I^2_{M,pri} r_{DS,on,pri(70°C)} = 6.08W \tag{4.8}$$

$$P_{M,cond,pri} = I^2_{M,sec} r_{DS,on,sec(70°C)} = 15.31W \tag{4.9}$$

where $r_{DS,on,pri(25°C)}$ is multiplied by a factor of 1.05 to account for temperature dependency extracted from the datasheet and a factor of 1.25 for $r_{DS,on,sec(25°C)}$.

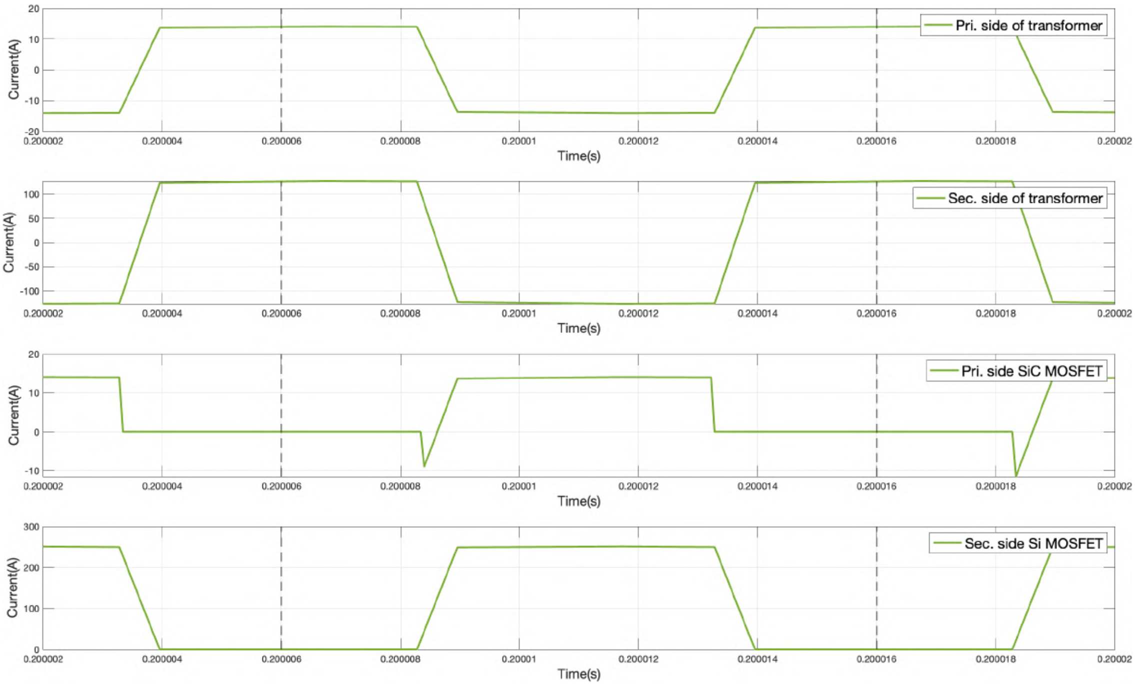


Figure 4.19: Current waveforms of the PSFB-CDR

From the current waveforms in figure 4.19, the RMS currents are extracted and compared to the hand calculated currents, see table 4.3.

Table 4.3: RMS currents from simulation

Primary transformer RMS current	13.3A
Secondary transformer RMS current	119.6A
Primary MOSFET RMS current	9.4A
Secondary MOSFET RMS current	172.7A

As seen, the calculated and the ones from the simulation are close to each other meaning that the conduction losses given in PLECS are valid.

On the primary side of the DC/DC, the turn-on switching losses and output capacitance losses are neglected due to ZVS meaning that only the turn-off losses are considered. The turn-off losses are calculated as in (2.41) where t_{off} is more precisely calculated to be

$$t_{off} = Q_{gd}\frac{R_g}{V_{plateau}} + Q_{gs}\frac{V_{plateau} - V_{threshold}}{V_{plateau}}\frac{2R_g}{V_{plateau} + V_{threshold}} = 13.8ns \tag{4.10}$$

resulting in turn-off switching loss to be

$$P_{sw,pri} = \frac{1}{2}V_{in}I_{DS}f_{sw}t_{off} = 3.8W \tag{4.11}$$

Further, using (2.43) the gate driver losses are

$$P_{gate,pri} = V_{gs,pri}Q_{g,pri}f_{sw} = 0.09W \tag{4.12}$$

$$P_{gate,sec} = V_{gs,sec}Q_{g,sec}f_{sw} = 0.50W \tag{4.13}$$

Similarly, the losses for the PSFB and DAB are calculated and summarized in table 4.4.

Table 4.4: Comparison of hand calculated losses and losses from PLECS

	DAB	**PSFB**	**PSFB-CDR**
Hand calculated $P_{sw,tot}(W)$	10.8	12.8	15.6
Simulated $P_{sw,tot}(W)$	24.9	17	10.8
Hand calculated $P_{cond,pri,tot}(W)$	23.2	33.2	24.4
Simulated $P_{cond,pri,tot}(W)$	26.3	35.8	23.2
Hand calculated $P_{cond,sec,tot}(W)$	150.4	91.2	30.6
Simulated $P_{cond,sec,tot}(W)$	152.8	92	34
Hand calculated $P_{cu,pri,tot}(W)$	3.8	5	5
Simulated $P_{cu,pri,tot}(W)$	3.8	5.5	3.5
Hand calculated $P_{cu,sec,tot}(W)$	3.5	5.8	2.9
Simulated $P_{cu,sec,tot}(W)$	3.5	5.6	1.4

From the table it is seen that there are some differences especially for the switching losses. Switching losses are difficult to get accurate by doing hand calculation since the characteristics of the MOSFET are dependant on some many factors making it very various at different conditions. The other losses as the primary and secondary conduction losses matches better meaning that the consideration of temperature from the normalized $r_{DS,on} - temperature$ curves provided in the datasheets provides a good and accurate input.

4.4 Further suggested improvements

4.4.1 Paralleling of MOSFETs

Paralleling of devices brings many advantages as well as complexity to the circuit. The expression of conduction losses with parallel devices becomes

$$P_{M,cond,tot} = N_p(\frac{I_{M,pri}}{N_p})^2 r_{DS,(on)} \tag{4.14}$$

when assuming that the current is evenly divided through all the MOSFETs in parallel. As seen, this is a huge advantage on the secondary side of the transformer where the conduction losses of a single MOSFET are the highest. In a physical application, the MOSFETs are not identical due to the manufacturing process meaning that the internal resistance of each device in parallel is not equal which makes the distribution of current through them uneven. The difference of threshold voltage is also an issue when using the same gate driver to power them at turn-on since the one with lower threshold voltage will start conducting current earlier and therefore will experience a transient of high current for a short period of time. Therefore, all devices are assumed to be perfectly identical which is also the case for the simulation in PLECS. Using the same gate driver for all the MOSFETs in parallel gives the gate driver losses of

$$P_{gate} = N_p V_{gs} Q_{g,pri} f_{sw} \tag{4.15}$$

In figure 4.20, the results of paralleling primary and secondary MOSFETs in a total of 16 combinations is seen. The results are obtained for the PSFB-CDR-LLC which proved to have the best overall efficiency. The simulations were conducted at $V_{in} = 400V$ and at 3kW output for a longer period of time to let the junction temperature of the devices reach steady state.

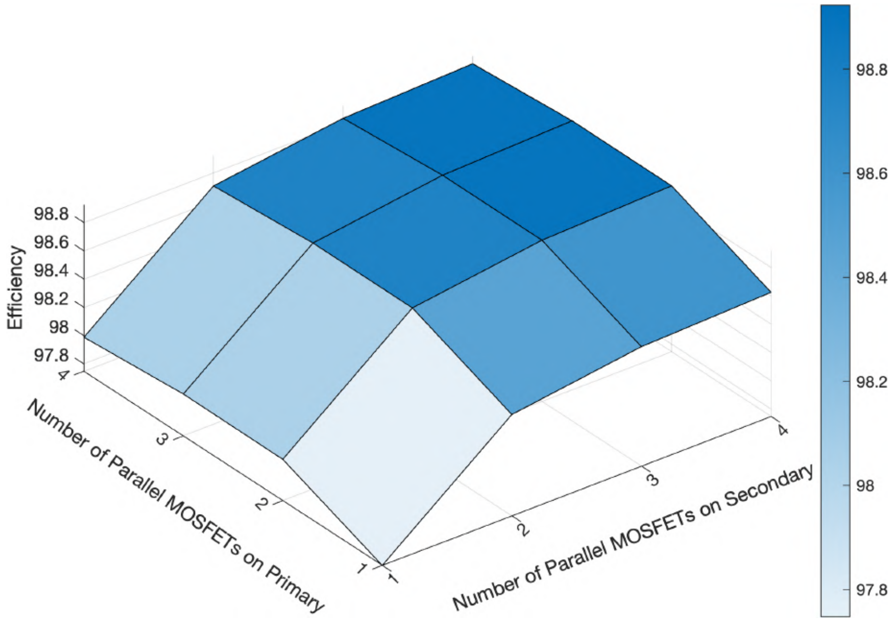


Figure 4.20: Efficiency vs Number of Parallel MOSFETs

The benefit of paralleling secondary MOSFETs over primary is clearly seen by the increase of efficiency which makes the best improvement when going from one to two MOSFETs in parallel. The improvement of efficiency after further increasing the amount of MOSFETs on the secondary is not as big due to mainly higher gate driver losses which in (4.13) are seen to be fairly big.

The combinations providing the best efficiency is seen to be having 2x4 and 3x4 paralleled MOSFETs on primary and secondary, giving an efficiency of 98.92%.

4.4.2 Comparison of heat-sinks and its effect on the total losses

The study of having a liquid-cooled heat sink to reduce the sink-ambient thermal resistance was examined and the results are seen in figure 4.21.

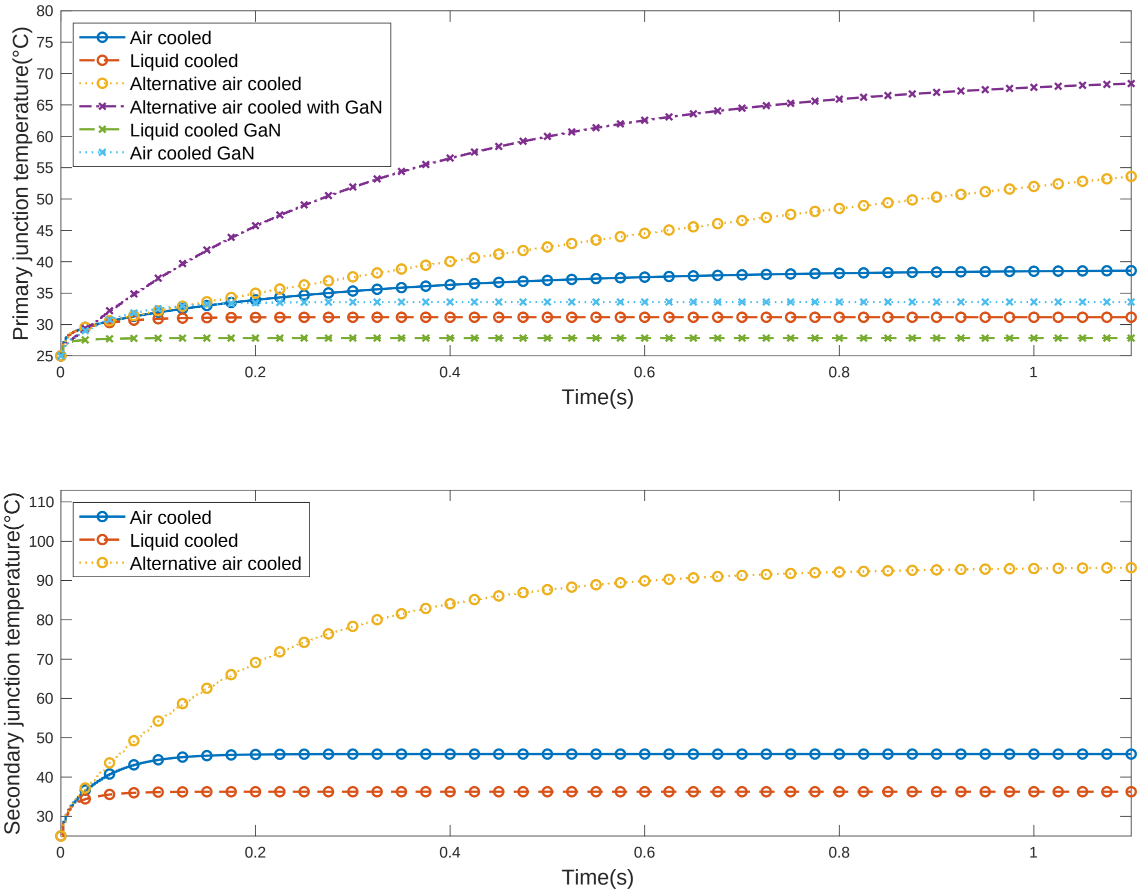


Figure 4.21: Junction temperature at various heat sinks

The simulations have been conducted for both SiC and GaN to make a loss comparison for the different heat sinks and to find a suitable design in terms of both efficiency and cost. It is seen that the difference in junction temperature both on the primary and secondary side for air-cooled and liquid-cooled is not big for both SiC and GaN meaning that the air-cooled heat sink is a good option in the design to lower the total cost. The alternative air-cooled heat sink increases the junction temperature with roughly double for both the primary and secondary devices but in terms of the total losses, it is seen in figure 4.22 that the combination of GaN with the alternative air-cooled heat sink is better than SiC with the liquid-cooled heat sink. The best performing combination is the GaN with the liquid-cooled heat sink and the worst is SiC with the alternative air-cooled heat sink. The difference between these two combination is 17.4% in total losses.

The difference in total losses in the comparison of GaN with air-cooled and liquid-cooled is 1.6% and between the air-cooled and alternative air-cooled it is 10.5%.

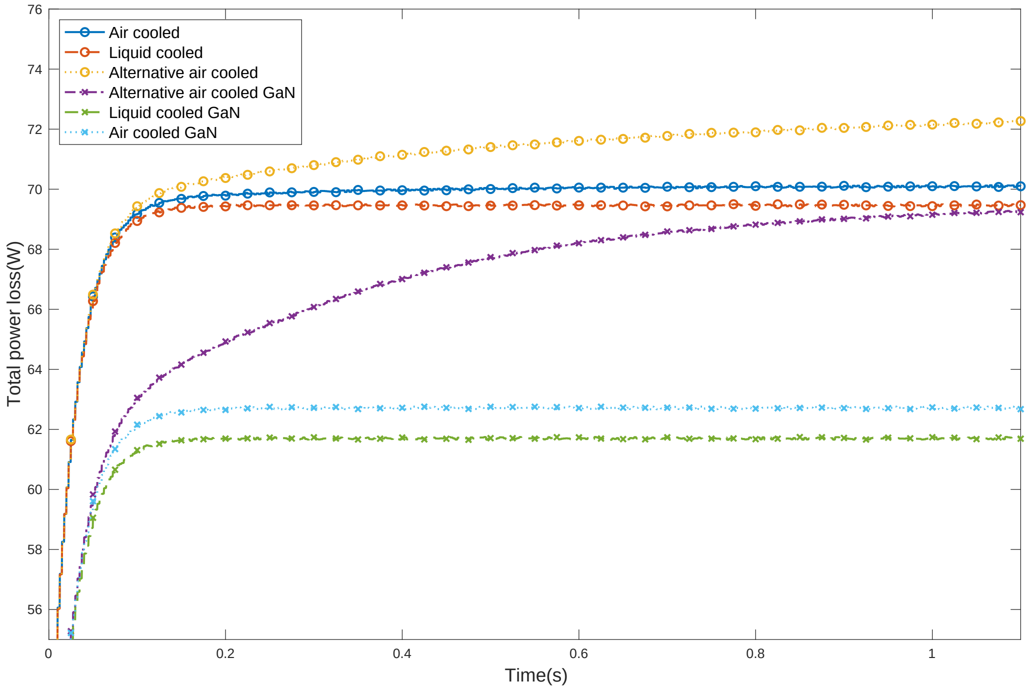


Figure 4.22: Total losses for SiC and GaN at the various heat sinks

4.4.2.1 Efficiency-load curve with parallel devices on secondary

In figure A.1 the impact of paralleling Si MOSFETs in the secondary is seen. The low load losses are seen to be higher for higher number of parallel devices due to the additional gate losses meaning that depending on where the main operating range is, the number of parallel devices can be chosen.

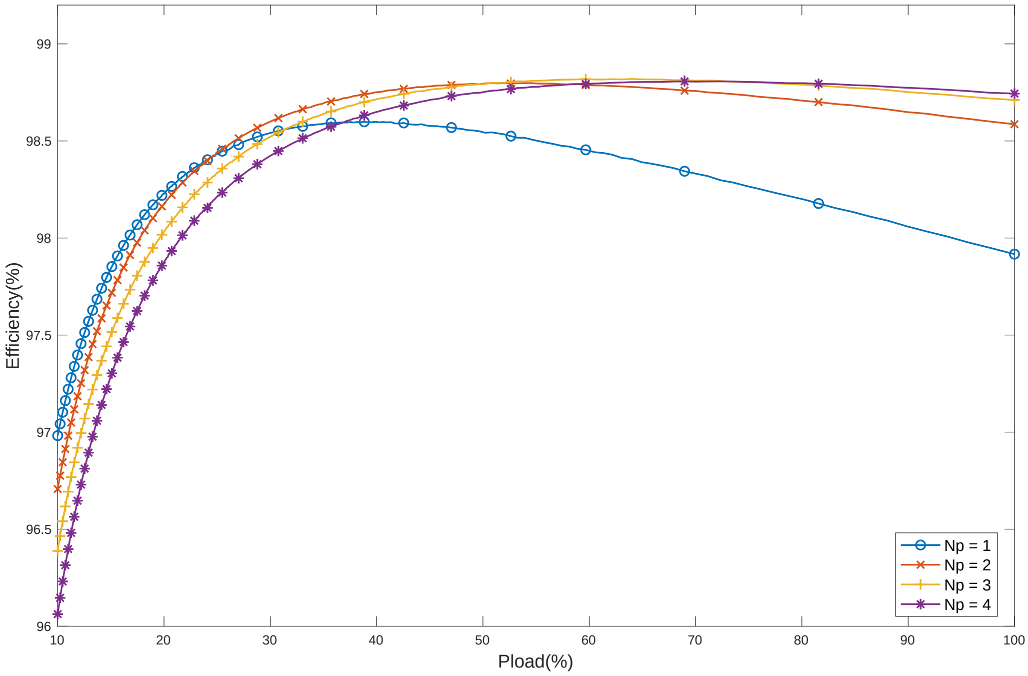


Figure 4.23: Efficiency - load curve for up to four parallel secondary MOSFETs

4.4.2.2 Evaluation of proposed DC/DC converter with test data

Based on the results in section 4.1, 4.2 and 4.4, the proposed DC/DC converter is the PSFB-CDR-LLC with GaN and two Si MOSFETs in parallel on the HV and LV side of the transformer. The test data is presented in section 3.11.2 and the battery model in section 3.8.1. The results of losses, efficiency and junction temperature is seen in figure 4.24, and the response of the control system in figure 4.25.

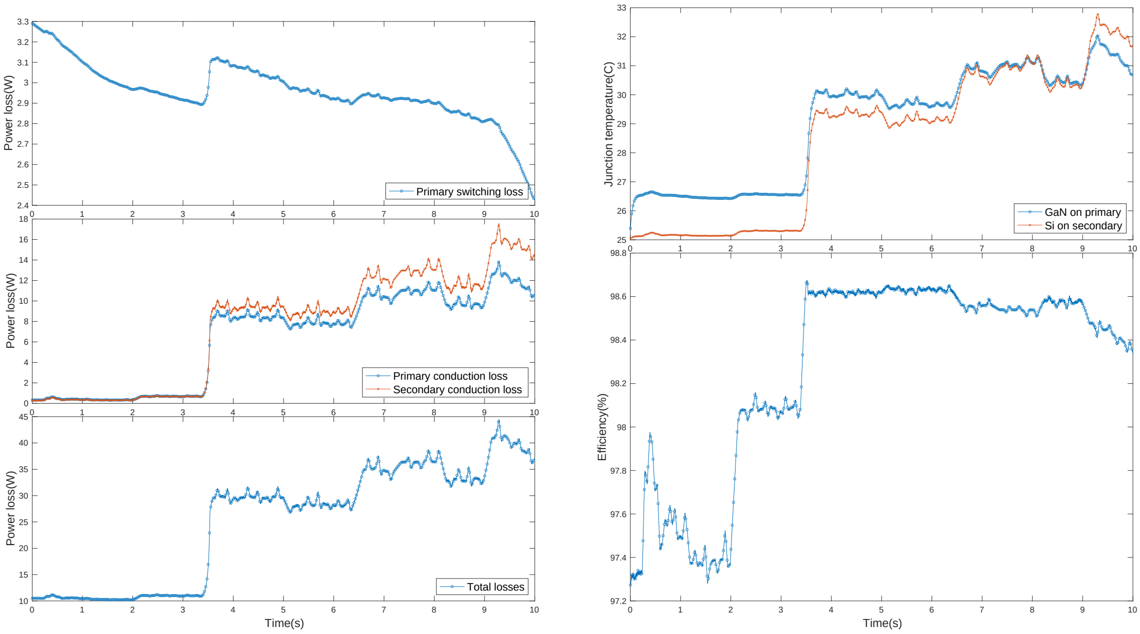


Figure 4.24: Results from the proposed DC/DC converter with the test data and battery model

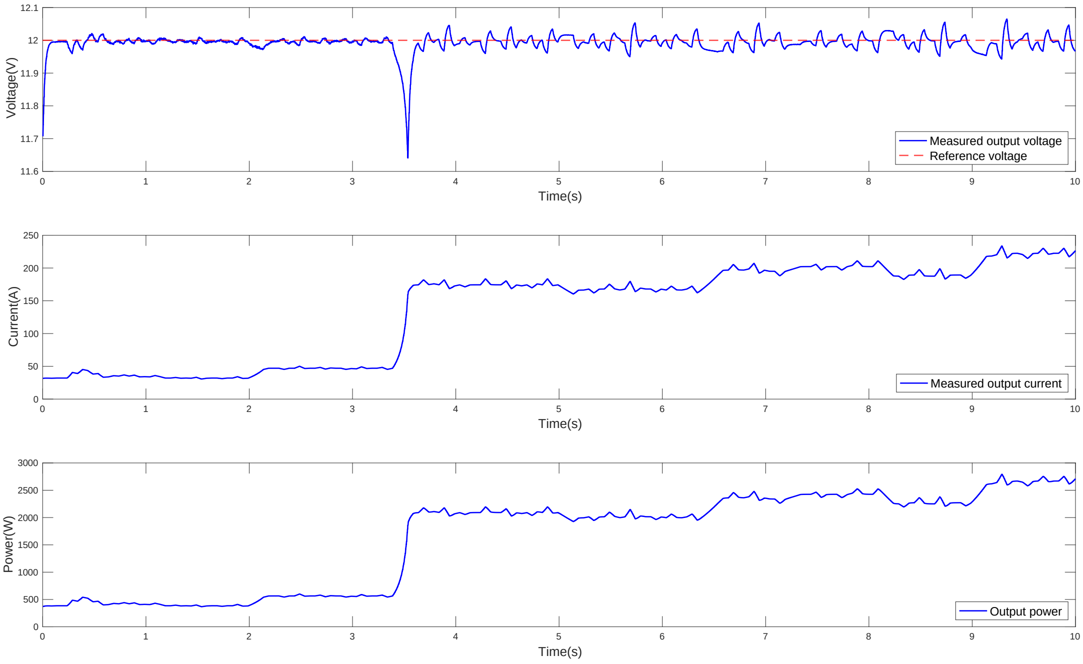


Figure 4.25: Response and behaviour of the control system

4.5 Cost analysis

Cost is a key factor when designing DC/DC converters. In this section, the cost of the components are analyzed by evaluating the unit costs of each component and the total cost when considering the entire topology. To determine the cost of the components, the price data are sourced from leading electronic components distributors such as Farnell, RS Components, Mouser, and Elfa. These distributors offer a wide range of electronic components, and their pricing data is used to analyze the cost of the individual components required for the DC/DC converter design. However, both the transformer and the filter inductance are custom-designed. While the price of the transformer remains constant across all topologies and is therefore not considered. The cost of the inductance was determined by utilizing online software tools which estimated the required core size and wire length. Subsequently, the cost of inductance was then estimated by looking into relevant products from electronic component distributors. As depicted in figure 4.26, the inductor consists of two main components: copper wire and a toroidal core. The software takes the desired inductance value as input and subsequently select the suitable core material and calculates its dimensions, including the height (h), outer diameter (OD), and inner diameter (ID). Further, this software assists in determining the required number of turns, length per turn, based on the selected ferrite toroidal core material, which in this case is FT-23-43. These parameters for the core material and the winding can then be used to locate the appropriate core/wire size from electronic distributors.

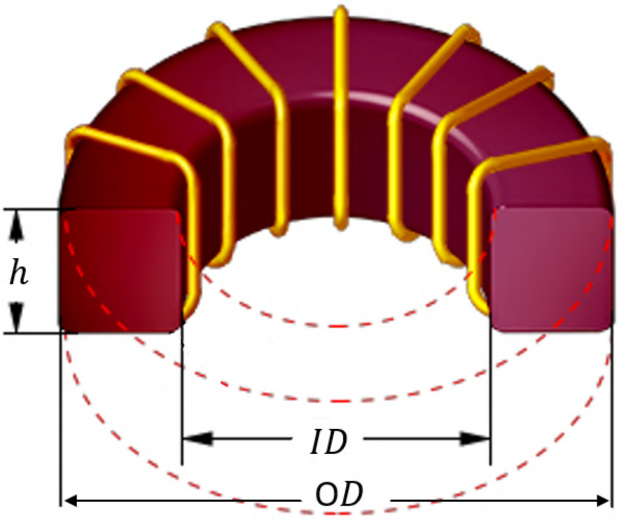


Figure 4.26: Toroidal core inductor dimensions

The price data is summarized in table 4.5 where the unit prices is based on when buying more than 1000 units. Additionally, table 4.6 presents the cost of each topology across each case. Figure 4.27, illustrates the relationship between topology and cost, providing insights into the financial implications associated with different case approaches. By analyzing the data presented, it becomes clear that using parallel connections of Schottky diodes increases the system's cost significantly, additionally, the increased number of components results in higher costs.

Table 4.5: Cost each component unit

Component	Price/unit
MOSFET E3M0060065D	98.90 SEK
MOSFET NVMTS0D4N04C	62.37 SEK
MOSFET GS-065-030-2-L	100.17 SEK
DIODE FSH5065B-F085	76.32 SEK
Transformer	– SEK
Liquid-cooled heatsink	2812.9 SEK
Air-cooled heatsink	1001.0 SEK
Alternative air-cooled heatsink	255.81 SEK
Output capacitor	0.70 SEK
Filter inductance	130 SEK
Resonant inductance	41.28 SEK
Resonant capacitor	2.78 SEK

Table 4.6: Total cost of each topology during case each approach

		Case 1	Case 2	Case 3	Case 4
Center-tapped	Tot.cost	656 SEK	651 SEK	1447 SEK	1442 SEK
CDR	Tot.cost	786 SEK	781 SEK	1577 SEK	1572 SEK
DAB	Tot.cost	781 SEK	776 SEK	2363 SEK	2358 SEK
LLC center-tapped	Tot.cost	700 SEK	695 SEK	1491 SEK	1486 SEK
LLC CDR	Tot.cost	830 SEK	825 SEK	1621 SEK	1616 SEK

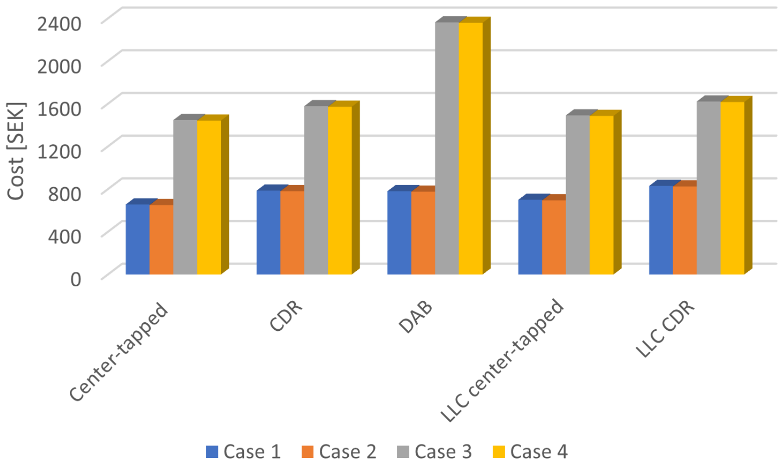


Figure 4.27: Analysis of topology costs across different case approaches

Furthermore, the life cycle cost (LCC) is investigated for the PSFB-CDR-LLC configuration as it has demonstrated the highest efficiency. According to [39] the LCC can be estimated as

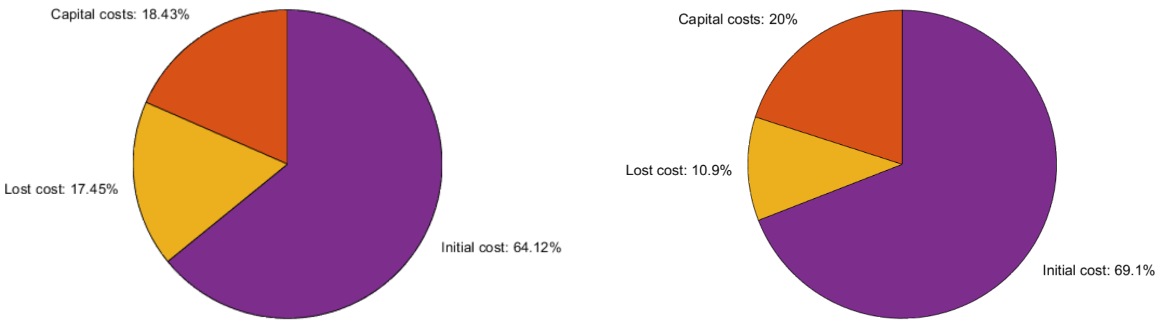
$$LCC = \Sigma_{tot} + \sum_{n=1}^{N_{life}} \left\{\Sigma_{cap}(q) + \Sigma_{rev}\right\} \cdot \frac{1}{(1+q)^n} \tag{4.16}$$

where Σ_{tot}, Σ_{cap}, Σ_{rev}, q and N_{life} represents, the initial cost, capital cost, costs of lost operating revenues, the interest rate and the expected life time in number of years, respectively. The capital cost is calculated by multiplying the interest rate and the initial cost. Additionally, the costs of lost operating revenue can be determined by multiplying the energy loss (in kWh) of the converter with the energy cost per kWh. Further, the interest rate is assumed to be 5%. the parameters for the LCC estimation are summarized in table 4.7

Table 4.7: Parameter value for LCC

	With air-cooled	**With liquid-cooled**
Initial cost	1956 SEK	3756 SEK
Energy loss	41.3 kWh	40.85 kWh
Electricity price	2.5 SEK/kWh	2.5 SEK/kWh
q	5%	5%
LCC over 15 years	4043 SEK	6765 SEK

The LCC analysis was conducted for both the air-cooled heat sink and the liquid-cooled heat sink configurations. The results of both LCC estimations are presented in figure 4.28.



(a) With air-cooled **(b)** With liquid-cooled

Figure 4.28: LCC analysis of the PSFB-CDR-LLC with Air-cooled and Liquid-cooled heat sink

5

Discussion

When comparing load conditions from light load to full load, the efficiency of a DC/DC converter improves during light loads due to lower conduction losses resulting from smaller load currents. However, when considering different input voltages (290V and 400V) under varying load conditions, it is observed that the 290V input voltage provides better efficiency than the 400V input voltage. From a theoretical standpoint, the conduction losses on the secondary side should be the same since the load current and voltage remain constant. However, the conduction losses on the primary side vary as they depend on the input voltage. Higher input voltages lead to smaller currents, resulting in reduced conduction losses. On the other hand, lower input voltages result in higher currents, leading to increased conduction losses. This relationship arises from the fact that power is the product of voltage and current. Switching losses, on the other hand, are higher during light loads and decrease as the load becomes heavier. Due to the fact, that during light loads, the switching transitions occur more frequently compared to the load requirements, which explains the reason switching losses are higher compared to conduction losses. As the load increases, there is a reduction in switching losses on the primary side of the DC/DC converter, while the conduction losses on the secondary side become higher due to the increased load current.

The loss analysis during varying case approaches suggest that GaN devices on the primary side offer advantages in terms of reducing losses. Because GaN MOSFETs switch more quickly, the switching loss is reduced. Since conduction losses are heavily dependant on on-state resistance, GaN has improved conduction losses due to its lower on-state resistance. While the choice of devices on the secondary side, particularly Schottky diodes, needs to be carefully considered to avoid increased losses. Since the SiC diode could only handle lower current, the parallel connection of 6 schottky diodes increased the cost significantly. However, it was assumed that in the future, SiC schottky diodes that are able to handle larger current and lower voltages that are suitable for the load will be available. Despite the higher secondary losses for the CDR when using SiC diodes, it is lower for the center tapped, and quite equal for the DAB/SAB when SiC MOSFETs/diodes are used. One reason of obtaining such result could be due to that the center-tapped configurations full-wave rectification arrangement, which enables the use of both sides of the secondary winding during each cycle. Thus the secondary voltage is used more effectively, which reduces the voltage stress on the diodes. As a result, the center-tapped design of diodes has lower losses than other configurations.

GaN MOSFETs were not useful on the secondary side due to their high on-state resistance. They could handle the high load current by being connected in parallel, but their resistance was still much greater than that of Si MOSFETs and the cost increased. Additionally, the PLECS modeling software failed to identify the transient oscillations, making the snubber circuit unusable, despite the possibility of using snubber circuit to reduce switching losses on the primary side.

The suggested improvements come with an increased cost, mainly due to the paralleling of MOSFETs, which increases the overall cost. Also, when considering the three heat sinks, liquid-cooled, air-cooled, and the alternative air-cooled. Among these, the alternative air-cooled heatsink is the most cost-effective and provides better efficiency, especially when used in combination with GaN MOSFETs compared to liquid-cooled with SiC MOSFETs. However, the alternative air-cooled heatsink has a higher junction temperature which may reduce the lifetime of the converter, making it less favorable in the long run. On the other hand, the liquid-cooled heatsink maintains the lowest junction temperature and best efficiency, which also increase the converters lifetime. However, it may not be practical due to the high cost of the liquid-cooled heatsink. Thus, the air-cooled heatsink is the best choice when both the cost and the converters lifetime are taken into account. It achieves a beneficial outcome for the functioning of the power converter by maintaining an appropriate balance between cost-effectiveness and maintaining a reasonable junction temperature.

The feasibility of the cost estimations has several limitations. Even though the pricing data are obtained from relevant sources, the cost of DC/DC converter for the APM depends on several factors thus providing an exact cost figure is challenging. Since the same transformer and heatsink were used across all topologies, they were excluded from the cost calculations. Although the cost of the heatsink was available, it was difficult to calculate an appropriate price for the transformer because of its complicated design. As a result, the choice to use the same transformer across all topologies made it possible to exclude it from the cost analysis. When considering the LCC analysis for the PSFB-CDR-LLC, it is recommended to choose for the air-cooled option due to its lower total life cycle cost compared to the liquid-cooled alternative. Although the liquid-cooled option may have lower losses cost, over a 15-year period, the air-cooled option proves to be more advantageous in terms of cost. Further, in order to get a precise cost estimation, it is best to consult with suppliers or manufacturers who can provide tailored pricing based on the specific requirements. However during this thesis project, due to confidentiality it was not possible to get supplier pricing data.

Overall, designing specialized transformers and control loops for each topology with the goal of determining whether comparable result can be obtained might make for interesting additional research on the project. Further, the controller design should be based on either small-signal modeling or state-space modeling, as these approaches offer more tailored control loops, optimizing the control scheme more effectively. It is also needed to extend the investigation, since this was only based on simulations. It would also be interesting to conduct tests on a practical converter and compare the results obtained there to the ones from the simulations.

5.1 Future work

For future research and improvements, several points require additional investigation. The following points highlights key areas that require additional research:

- Optimize the control strategy used in the topologies, such as the modulation scheme, phase-shift control, and feedback control loop, for each topology
- Investigating other frequencies, especially higher frequencies up to 250 kHz
- Build a practical model and see how it acts in accordance with the simulations
- Investigate low voltage, high current SIC diodes for the secondary side
- Analyze the effect of GaN with low on-state resistance on the secondary side
- Implement both RC & RCD snubber in order to reduce the switching losses
- Investigate the impact of using active clamping SiC MOSFETs on component cost as well as efficiency
- Investigate other topologies such as CLLC resonant converter
- Simulate a magnetic model of the transformer to get a more precise view of the core losses

5.2 Sustainability impact

The energy sector has a significant impact on the environment due to the usage of fossil fuels, such as coal, oil, and natural gas for transportation and electricity production. The transport sector is a major contributor to CO2 emissions within the EU, accounting for approximately 12% of the total emissions [40]. Because of the importance of this industry, the EU has put strict emission reduction rules into place. For instance, manufactures are required to reduce their emissions by 37.5% between 2021 and 2030 [40]. This resulted in a significant amount of electrification in the transportation sector, where DC/DC converters are essential for effective energy conversion. The semiconductor materials such as GaN and SiC used in the power electronics, will make it possible to reduce emissions by a significant amount. Studies reveal that only GaN-based technology might prevent the emission of more than 1 billion tonnes of greenhouse gases by 2041 [41]. Hence, we can significantly advance our efforts to tackle climate change and create a more sustainable future by utilizing the benefits of GaN and SiC. As these semiconductor materials are used in everything from smartphones to wind turbines, in addition to being useful in the automotive industry.

5.3 Ethical aspects

The authors carefully followed the principles outlined in the IEEE Code of Conduct [42] throughout the thesis work. Taking into account the third code point, which reads *"to avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;"*. To ensure confidential information remained protected and not used against the company's interests, the authors shared a copy of the thesis report with the company before submitting it to the university.

Moreover, the authors included the fifth code point of the IEEE code of conduct, which which read as *"to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, to be honest, and realistic in stating claims or estimates based on available data, and to credit properly the contributions of others;"*. The authors had continuously discussions with the supervisor, enabling the identification and correction of any shortcomings in the work. Further, the contributions from external parties, such as PLECS and Onsemi, were properly acknowledged and credited.

Furthermore, the authors upheld the seventh, eighth, and ninth principles of the IEEE Code of Conduct, which read as *"To treat all persons fairly and with respect, to avoid harassment or discrimination, and to avoid injuring others."*. These principles encouraged a collaborative and innovative environment within the group while upholding legal and ethical standards.

Lastly, the tenth code point, which says *"to support colleagues and coworkers in following this code of ethics, to strive to ensure the code is upheld, and to not retaliate against individuals reporting a violation."* has also been taken into account. It is crucial to consciously sustain professional integrity, ethical behavior, and a respectful working environment in order to comply with the IEEE Code of Conduct. These activities not only make sure that set rules are followed, but they also help to build a culture of trust, creativeness, and respect among colleagues.

6

Conclusion

To assess the efficiency of different converter topologies, load conditions were varied from 10 % to 100 % in PLECS simulations. The DAB demonstrated higher efficiency at lower input voltages and lower load conditions due to reduced primary switching losses. The PSFB topology showed higher losses at higher input voltages, primarily due to increased primary switching losses and the extended conduction time of body diodes. Increasing the leakage inductance reduced secondary conduction losses, but the control system could not handle it at lower voltages. On the other hand, the PSFB-LLC topology showed reduced secondary conduction losses but had higher switching losses on the primary. While, the PSFB-CDR topology showed stable efficiency between the input voltages, proving the model and control system are well-designed. In comparison to other topologies, it also showed less efficiency variability. However, the PSFB-CDR-LLC topology demonstrated the highest efficiency across the entire load range.

Further, testing was conducted using GaN, SiC, and Si semiconductor devices in four different cases. GaN MOSFETs were used on the primary side due to their high voltage rating, while Si MOSFETs and SiC Schottky diodes were used on the secondary side. The efficiency and losses were evaluated for each case, with the PSFB-CDR-LLC topology achieving highest efficiency ranging from 97.95% to 97.03% across all cases.

Regarding improvements, the study focused on two key areas of improvement. It was found that paralleling the secondary MOSFETs significantly improved the efficiency. Additionally, various heat sink options for SiC and GaN devices were compared. The findings indicated that the air-cooled heat sink was an optimal choice in terms of efficiency and cost in combination with GaN MOSFETs on the primary and two parallel Si MOSFETs on the secondary.

Lastly, the study evaluated component costs by analyzing unit prices sourced from leading distributors. The cost of the transformer and the heatsink remained constant across all topologies and was not taken into account.

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Appendix 1

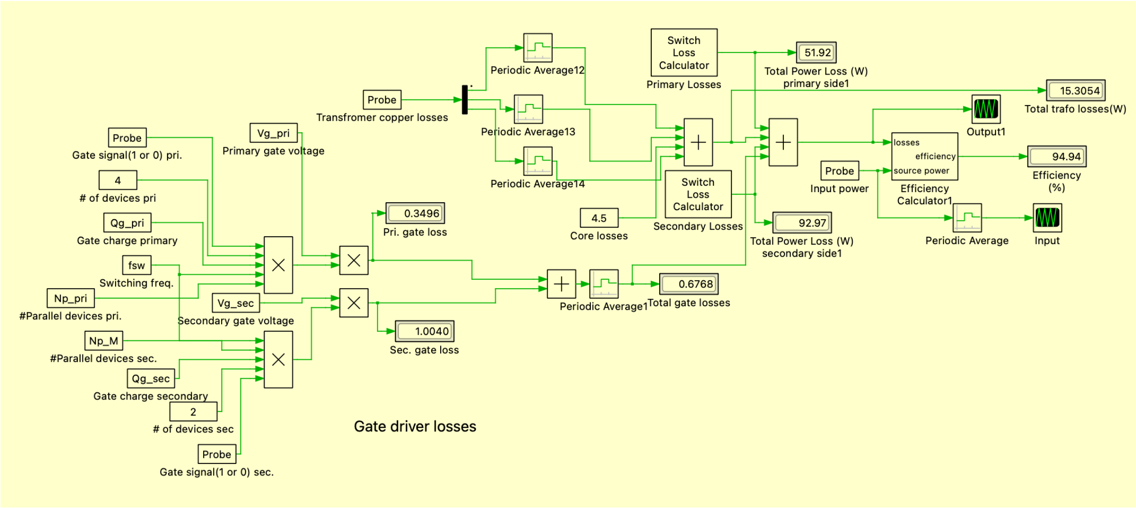

Figure A.1: Modified loss calculator used in PLECS for the PSFB

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