CHALMERS

PIN diode drive circuits optimized for fast switching

Master of Science Thesis

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Abstract

The use of RF and microwave switches based on PIN diodes is widely spread. In a radar system the switch directs transmit and receive signals to and from the antenna. In scenarios where the target is small and in close range there is a need for high output power and fast switching. But there is one fundamental problem: High power handling capability and fast switching speed are conflicting parameters in a PIN diode. In order to bridge the gap, between power handling capability and speed, the PIN diode drive circuit currently in use at SAAB has been studied. The PIN diode drivers control the biasing of the PIN diodes and thus affects the speed of the switch.

Several modifications was made to the driver design. The fastest PIN diode driver is able to switch two PIN diodes with a carrier lifetime, τ_L, of $2000ns$ in just $237ns$. This is an improvement of $963ns$ over the original design.

It has been proven that small changes in the driver design can improve the time response of a switch while still maintaining the same power handling capability.

Acknowledgements

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Finally I would like to thank Christian Fager, my examiner from Chalmers University of Technology, for his guidance in the academic part of the thesis.

Nomenclature

A	Cross-sectional area
C_j	Junction capacitance
D	Duty cycle
E_{BD}	Electric breakdown field
ρ	Electric resistivity
I_F	Forward current
ϵ	Electric permittivity
Q	Electric charge
τ_T	Carrier lifetime
V_{BD}	Breakdown voltage
x_I	Width of intrinsic region
μ_N	Electron mobility
μ_P	Hole mobility

Contents

Chapter 1

Introduction

1.1 Background

To alternate between transmitting and receiving information from the same antenna, a duplexer must be used. The duplexer allows both the transmitter and the receiver to be connected to the antenna. Another role of the duplexer is to provide isolation between the transmitting and receiving side of the system. This is very important since the power handling capability of the receiver usually is several orders of magnitude lower than the output power from the transmitter. This feature is needed in communication links and radars. In a radar system which is a half-duplex system, where the transmitter and receiver operates sequentially, duplexing can be handled by a transmit-receive (T/R) switch (Figure 1.1) [1]. In scenarios where the

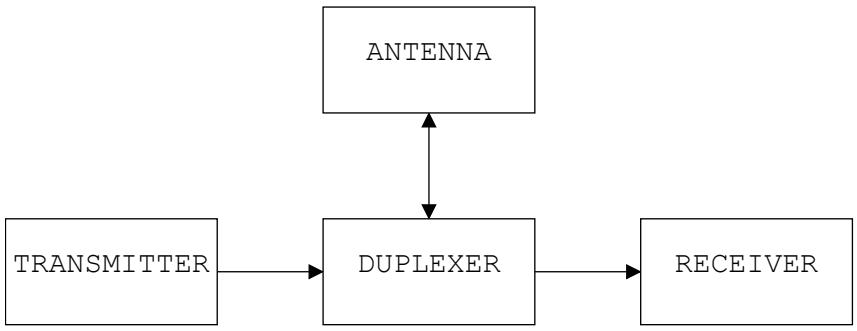


Figure 1.1: *Block diagram overview of a simplified radar system.*

target is small and in close range the need for fast switching and high output

power arises. For this kind of application switches based on PIN diodes are well suited due to good power handling capability and speed. PIN diode switches for a variety of frequencies and applications manufactured in a variety of processes have been reported [2, 3, 4]. But there is one fundamental problem: High power handling capability and fast switching speed are conflicting parameters in a PIN diode. To make this trade-off as favourable as possible it is important to choose an appropriate PIN diode that matches the requirements. The trade-off can be further improved with the use of an optimized PIN diode drive circuit. A well designed drive circuit can improve the switching speed considerably.

There are several applications other than radar systems where PIN diodes are used e.g. reconfigurable antennas [5, 6, 7], optically activated pin diode switches [8], variable gain amplifiers [9]

1.2 Objective

The purpose of this master thesis is to design and evaluate a driver for a PIN diode microwave transmit-receive switch. Since the switch is based on PIN diodes the capabilities and limitations of these should be studied. The drivers for the PIN diode biasing should be designed and optimized for fast switching. Finally, a prototype of the optimized drive circuits should be constructed and characterized.

1.3 Problem definition

- How fast can the switch alternate between transmitting and receiving at specified bias conditions?
- What are the underlying physical limitations of the switching speed?
- How does the driver affect the performance of the switch?

1.4 Limitations

There are several options for the microwave switch designer. This thesis will however only consider switches based on PIN diodes and no other solid state, MEMS or mechanical switches.

The thesis will not cover any other parts of a radar system other than the PIN diode switch and the PIN diode drivers.

The requirements for the PIN diode driver are:

- Forward bias current: $100mA$
- Reverse bias voltage: $-40V$
- Switching time: Optimized for fast switching.
- A robust design, cross conduction should be avoided.

The chip area of the PIN diode driver should be small, this limits the amount of components and the complexity of the driver. Also, the driver design will be limited to the use of bipolar transistors.

Chapter 2

Theory

In this chapter theory surrounding PIN diode switches and their use in RF and microwave applications will be presented. To begin with, a microwave switch topology will be presented. Secondly, a section focusing on PIN diode theory will be presented. This will be followed by a section concerning the PIN diode driver.

2.1 The Transmit-Receive switch

The Transmit-Receive switch allows both the transmitter and the receiver to be connected to a single antenna. Figure 2.1 shows a simple T/R switch, the switch consists of two PIN diodes and a quarter-wave transmission line[1]. The PIN diodes are biased through an inductor, which is isolating the bias supply from high power RF signals in the transmitter. The capacitors make sure no DC signal is entering the transmitter and receiver. To switch between the transmitter and the receiver the bias of the diodes is simply changed from forward to reverse. When forward biased, the diodes present a very low impedance. Thus, the transmitter will see a direct connection to the antenna. When looking towards the receiver the quarter wave transmission line will transform the short circuit to ground to an infinite impedance. Therefore the receiver will be protected from high power RF signals from the transmitter. When the PIN diodes are reverse biased they present an infinite impedance. Looking from the receiver, Diode 2 will block the ground path and Diode 1 will block the transmitter. Thus, the receiver will be connected to the antenna.

An ideal switch only has two positions: ON or OFF. In the ON state

[1]For theory on the quarter wave transmission line consult a textbook on microwave theory e.g. [10]

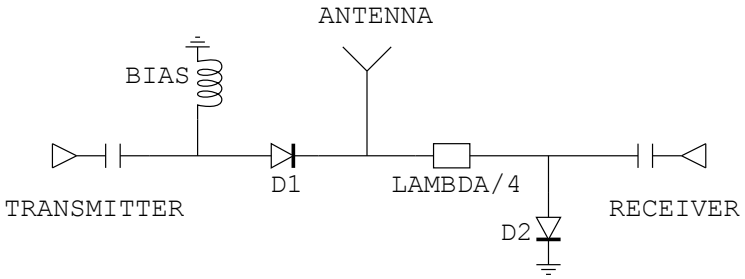


Figure 2.1: *Circuit schematic of a simple transmit-receive switch.*

the switch should present zero impedance and in the OFF state the switch should present infinite impedance. The switch should also be able to switch between the states instantaneously. This is very stringent and unrealistic requirements for a microwave switch. The ideal switch does however serve as a benchmark for characterization of switches.

2.1.1 Characteristics

To be able to evaluate the performance of a switch some figures of merit, usually provided by manufacturers or presented in research papers, will be defined.

As stated, when the switch is in the ON state it should present zero impedance and no power should be dissipated in the switch. To characterize the power loss in the ON state the term **insertion loss** is used. Insertion loss is defined as:

$$IL = 10log\frac{P_D}{P_O} \tag{2.1}$$

Where P_D is the power output of the switch in the ON state and P_O is the power output of the short circuited switch.[11]

The ratio of output power of the switch between the ON and OFF state is called the **isolation** and is defined as:

$$ISO = 10log\frac{P_{ON}}{P_{OFF}} \tag{2.2}$$

The speed of a switch is determined by the physical properties of the PIN diodes as well as the capabilities of the driver. ON and OFF times usually

differs and are defined from 50% of the drive control signal to 90% and 10% of the detected RF power for the respective states. As can be seen from

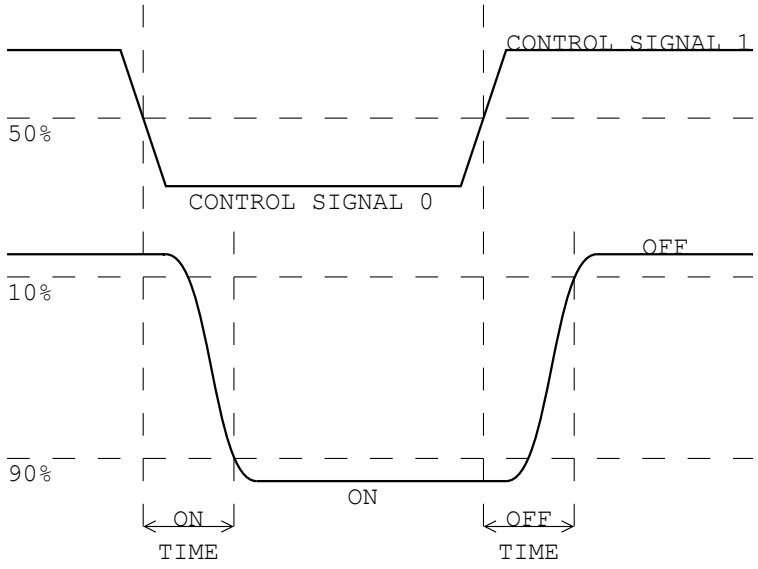


Figure 2.2: *Definitions of the ON and OFF time.*

Figure 2.2, the ON and OFF times are affected by both the lag time in the drive circuit as well as the time to fill and deplete the I-region in the PIN diodes.

2.2 The PIN diode

In the previous section the transmit-receive switch was presented. The PIN diodes in the switch presented either a short circuit or an open circuit, depending on the bias condition. In this chapter we will see that this ideal case is not what one can expect from real devices.

The PIN diode is a semiconductor device that consists of three regions: an intrinsic region is layered between an n-doped and a p-doped region. In practical devices the intrinsic region is usually realized by a highly resistive p-layer or a highly resistive n-layer. The width, x_I, of the intrinsic layer (I-layer) is an important attribute of the PIN diode and is illustrated in Figure 2.3. The width of the I-layer influences switching speed, capacitance and breakdown voltage [12]. A very useful property of the PIN diode is the fact that it can control large RF and microwave signals with comparably small dc signals [13]. It is this property that is exploited in PIN-diode switches.

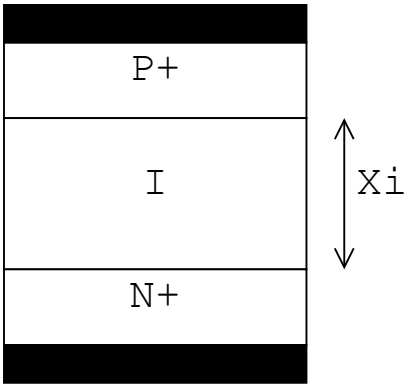


Figure 2.3: *Structure of a PIN diode with metal pads (black) where x_I is the width of the I-region.*

When designing circuits with PIN diodes a few important parameters of the PIN diode should be regarded. These are often presented in product specifications and include: breakdown voltage (V_{BD}), junction capacitance (C_j), series resistance (R_S) and carrier lifetime (τ_L).

The breakdown voltage is defined as the maximum voltage that can be applied to the PIN diode without failure. Since there is almost no free charge in the intrinsic region the electric field is constant and the breakdown voltage is determined by the breakdown field (E_{BD}) and the width of the intrinsic region (x_I), according to (2.3) [14].

$$V_{BD} = E_{BD} x_I \tag{2.3}$$

If the breakdown voltage is exceeded permanent damage might be caused to the intrinsic layer of the device.

When the PIN diode is reverse biased the I-region is depleted of carriers, this result in the junction capacitance. The junction capacitance is dependent on the electrical and geometrical properties of the device, according to [14].

$$C_j = \frac{\epsilon A}{X_I} \tag{2.4}$$

where ϵ is the electrical permittivity, A is the area perpendicular to the current and x_I is the width of the intrinsic region.

The series resistance at RF frequencies of the PIN diode is dependent on the forward bias current. The series resistance given in product specifications is usually close to the minimum resistance of the device. To get a

fair comparison between PIN diodes it is important to specify at witch bias current the resistance is measured.

The carrier lifetime is the mean lifetime of free carriers in the semiconductor. Free charge does not exist forever due to recombination between electron and holes. The process of recombination often occurs when carriers encounter structural defects or foreign atoms in the semiconductor. The rate of recombination is thus dependent on the amount of impurities in the semiconductor and the concentration of free carriers. The carrier lifetime is inversely proportional to the recombination rate and the concentration of carriers.

2.2.1 Structural properties

Two main fabrication methods of PIN diodes exist, namely epitaxial growth and diffusion. The manufacturing process of epitaxial PIN diodes starts with a highly doped n^+-wafer. On top of this layer the I-layer, a highly resistive n- or p-layer, is deposited by epitaxy. The next step in the process is the deposition of the p-layer, and the PIN structure is complete. The epitaxial technology can produce very thin I-layers of a couple of micrometers. The combination of a thin I-layer and recombination centres (diffused impurities i.e. gold) results in very fast devices [15]. Because of the thin I-layer the breakdown voltage, V_{BD}, according to (2.3) is comparably low.

In the fabrication of diffused PIN diodes the process starts with a low doped wafer. A p- and n-layer is diffused on each side of the wafer. The thickness of the I-region is determined by the thickness of the wafer and the depth of the diffused p- and n-layers. Since it is difficult to handle thin wafers this fabrication method is better suited for thick I-layer PIN diodes. Therefore diffused PIN diodes usually have higher breakdown voltages than their epitaxial counterpart [15].

2.2.2 I-V characteristics

The PIN diode is somewhat different from the ideal diode. When forward biased the lowly doped I-layer is flooded with carriers from the highly doped n- and p-layers. Now the PIN diode is conducting current and the RF resistance varies with the bias point. That is, the PIN diode behaves as a current controlled resistor for RF signals. This characteristic is exploited in linear attenuators and modulators [16]. The equivalent circuit of a PIN diode can be seen in Figure 2.5 and consists of an inductor and a resistor in series. Electrical resistance in an object is proportional to resistivity and length, and inversely proportional to the cross-section area:

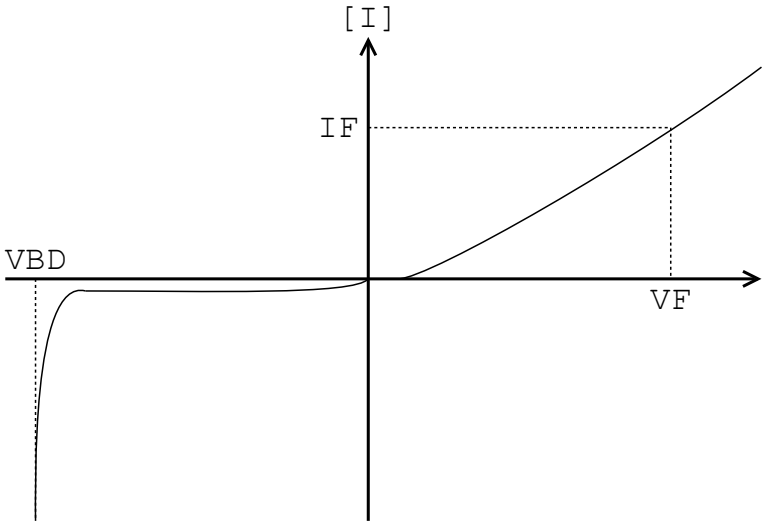


Figure 2.4: *Approximative I-V curve of a PIN diode where V_{BD} is the breakdown voltage and V_F and I_F is the forward voltage and current.*

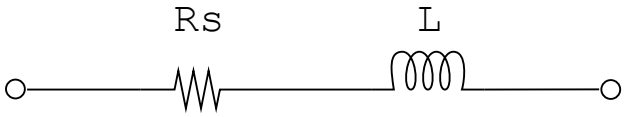


Figure 2.5: *Equivalent circuit of a forward biased PIN diode.*

$$R = \rho \frac{x}{A} \tag{2.5}$$

The resistivity in a semiconductor and hence in the I-layer of the PIN diode can be expressed as:

$$\rho = \frac{1}{q(\mu_N N + \mu_P P)} \tag{2.6}$$

Where q is the elementary charge - μ_N and μ_P is the mobility of electrons and holes - and N and P is the electron and hole concentrations. The mobile charge in the I-layer can be expressed as

$$\frac{dQ}{dt} = I_F - \frac{Q}{\tau_T} \tag{2.7}$$

where Q is the mobile charge, I_F the forward bias current and τ_T the carrier lifetime of the mobile charge. Under steady state conditions $I_F = I_{DC}$ and (2.7) reduces to

$$I_F = \frac{Q}{\tau_T} \tag{2.8}$$

where Q is the total charge in the I-layer:

$$Q = q(N + P)x_I A \tag{2.9}$$

If the concentration of electrons and holes is assumed to be the same (2.8) and (2.9) can be combined and reduces to

$$I_F = \frac{2qx_I NA}{\tau_T} \tag{2.10}$$

The forward resistivity of the device can now be expressed as

$$R_F = \frac{x_I^2}{2\mu\tau_T I_F} \tag{2.11}$$

where μ is the average mobility for electrons and holes. Equation (2.11) confirms that an increased forward bias will lower the resistance of the device. According to (2.11) zero bias would result in infinite resistance. This is not the case in a realistic device. Thus, (2.11) should be seen mainly as an estimate to help aid the understanding of the device physics. Also, it can be seen that the I-layer width, x_I, and the carrier lifetime, τ_L, are important factors to consider.

A reverse biased PIN diode can be modelled as a shunt capacitor and resistor. The equivalent circuit of the reverse biased PIN diode can be seen in Figure 2.6. In an ideal device the shunt resistance would be infinite be-

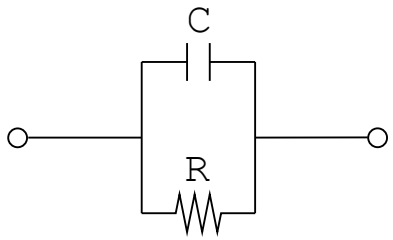


Figure 2.6: *Reverse biased equivalent circuit of a PIN diode.*

cause there is no free charge in the I-layer. In a practical device however,

impurities and other problems in the manufacturing process cause a small leakage current.

2.2.3 Switching behaviour

PIN diodes behave rather differently when the bias is changed from forward to reverse or from reverse to forward. The switching times are therefore different as well.

Forward to reverse bias - Reverse recovery

The process that arises when the bias of a PIN diode is changed from forward to reverse is called reverse recovery. The initial condition is a PIN diode with a forward bias current. In this state the I-region is filled with charge proportional to the carrier lifetime and forward bias current. The bias is then changed by applying a negative bias voltage over the PIN diode. The negative bias gives rise to a reverse current depleting the PIN diode of stored charge. In the beginning of this process there is a lot of free charge in the I-region and the charge is withdrawn rapidly. The process is limited by the voltage applied and the current limitations of the driver. As the charge is removed the resistance of the I-region increases. Since the resistance is increased the current is decreased. The resistance will soon increase to a level where the driver no longer influences the process. At this stage the charge withdrawal process is dominated by the carrier lifetime of the carriers. As high voltage diodes can have carrier lifetimes of several microseconds this can pose a problem if fast switching is required. After a finite time the I-region will be depleted of free charge.

Reverse to forward bias

When the PIN diode is reverse biased there is almost no free charge in the I-region. When a forward bias is applied over the PIN diode the I-region is flooded with charge from the P- and N-region. The forward bias current soon reaches a steady state. For most PIN-diodes this process is usually faster than the reverse recovery.

2.2.4 Power handling capability

The power handling capability of a PIN-diode is limited either by power dissipation capability or by breakdown voltage. The temperature limitation for a PIN diode is usually close to $175°C$. At higher temperatures the metal

pads used to connect the semiconductor to the package might diffuse into the semiconductor ruining its properties. Before this critical temperature is reached, a change in temperature might alter the characteristics of the device since many physical processes in semiconductors are temperature dependent. Mentioned earlier, is the fact that PIN diodes have a flat I-V curve when reverse biased and a linear resistance when forward biased. This is only true as long as the frequency is sufficiently high, the I-region is sufficiently wide and the power is sufficiently low. Otherwise the charge distribution in the I-region will be altered. This can occur both in the ON and OFF state. When the PIN diode is biased in the high impedance OFF state the region is depleted of carriers. If a high power low frequency sinusoidal signal is applied to the diode the positive part of the cycle will inject carriers into the I-region. Some of the injected carriers might interact and recombine, resulting in a small DC current altering the bias point of the diode. The change in bias will result in a change of the impedance owing to harmonics generation [17]. When the PIN diode is biased in the ON state the I-region is flooded with carriers resulting in a low impedance. If a high power low frequency sinusoidal signal is applied to the diode the negative part of the cycle will extrude charge from the I-region. Since the charge concentration determines the RF resistance of the I-region it is important that the charge removed is small compared to the total charge in the I-region. To quantify this process, the total charge in the I-region can be expressed as

$$Q_{tot} = I_{DC}\tau_L \tag{2.12}$$

where I_{DC} is the bias current and τ_L is the carrier lifetime. The amount of charge extruded from the negative part of the cycle is

$$Q_{tot} = \frac{I_P}{\pi f} \tag{2.13}$$

where I_P is the peak RF current and f is the frequency. The ratio between the removed and total charge is then

$$\frac{Q_{rf}}{Q_{tot}} = \frac{I_P}{I_{DC}\tau_L \pi f} = \frac{\Delta R_S}{R_S} \tag{2.14}$$

and since the amount of charge in the I-region is inversely proportional to the resistance a relation for the change of resistance is also included in (2.14).

2.2.5 PIN diode selection

PIN diodes are manufactured with a broad variety of physical properties in order to meet different demands e.g. limiter diodes, attenuator diodes, fast

switching diodes and high power handling diodes. For the RF and microwave switch designer the physical attributes that affects the behaviour of the PIN diode is carrier lifetime, I-layer width, junction area and I-layer resistivity. The problem lies in the fact that none of these parameters are totally independent of each other [17].

Carrier lifetime

The carrier lifetime influences the speed and the sensitivity to distortion. A long carrier lifetime makes for a PIN diode with slow switching speed but the device will cause less distortion. On the other hand a short carrier lifetime will produce a fast PIN diode but will be sensitive to distortion.

I-layer width

The width of the I-layer will influence the behaviour of the PIN diode in many ways. A thin I-layer will produce a fast device with low forward resistance. A thicker I-layer will produce a slower device with lower junction capacitance and better power handling capability.

Junction area

A PIN diode with depleted I-region is basically a capacitor. Thus the junction area will affect the capacitance of the device. The junction area also affect many other parameters. A small junction area will produce a fast device with low capacitance, high forward resistance, high reverse loss and poor power handling capability. A larger junction area will result in a slower device with a larger capacitance, lower forward resistance, lower reverse loss and better power handling capability.

I-layer resistivity

The resistivity of the I-layer is dependent on the doping concentration. A heavily doped low resistance I-layer will result in a fast PIN diode with low capacitance but some reverse loss. A high resistivity I-layer will produce a slower PIN diode with higher capacitance but with lower reverse losses.

2.2.6 Bias conditions

Proper biasing of the PIN diodes is required to ensure stable operation of the switch. The reverse bias has to be large enough to make sure the PIN diode is not conducting current in the positive part of the RF cycle but not so large

that the breakdown voltage is exceeded in the negative part of the RF cycle. The conservative approach is to choose the reverse bias slightly larger than the peak RF voltage. At high RF power this approach will be costly and the required reverse bias might be hard to realize. The more resource saving approach would imply that a portion of the positive RF signal will enter the forward conducting state. This results in charge injection to the depleted I-region but not necessarily forward conduction. If the transit time through the I-region is longer than half a period of the RF signal conduction will be prohibited. During the negative part of the RF signal most of the injected charge will be removed. But some residual charge will be stored and this stored charge builds up and stabilizes during the cycles. The stored charge will create a high impedance conducting path through the PIN diode. The reverse bias voltage must be larger than the DC voltage developed across this path in order to ensure stable operation. A prediction of the generated DC voltage can be found with

$$|V_{DC}| = \frac{|V_{AC,peak}|}{\left\{1 + \left[\frac{\pi f x_I^2}{0.95\mu V_{AC}\sqrt{D}}\left(1 + \sqrt{1 + (\frac{0.95\mu V_{AC}\sqrt{D}}{x_I V_{SAT}})^2}\right)\right]^2\right\}^{1/2}} \tag{2.15}$$

where f is the frequency, D is the duty cycle, μ is the carrier mobility, x_I is the width of the I-region and V_{SAT} is the saturation velocity of the carriers [13]. From (2.15) it can be seen that a number of device parameters and operation conditions affect the generated DC voltage. Lower operation frequency will result in a larger DC voltage as the time period charge is injected is increased. A higher power level and thus a higher signal voltage will increase the generated DC voltage. The signal voltage is also affected by the voltage standing wave ratio. Also, a reduced I-region thickness will increase the generated DC voltage. When the generated DC voltage, for the intended operation conditions, has been found the reverse bias voltage can be established. It is important to note that the sum of the applied reverse bias and the peak RF voltage must never exceed the breakdown voltage of the PIN-diode or the device will likely fail.

The forward bias current controls the amount of charge in the I-region. In accordance with (2.11) the RF resistance of a PIN diode is inversely proportional to the forward bias current. Thus, the RF loss in the PIN diode can be controlled by the bias. Another important aspect of the amount of forward bias current is modulation. Since the applied RF signal injects and withdraws some charge from the I-region the resistance is also changed. It is thus important to supply the PIN diode with enough forward bias current in

order to avoid modulation. Equation (2.14) states the change in resistance as a function of forward bias current and RF peak current. As can be seen there will always be some modulation but the amount can be controlled by the forward bias current.

2.2.7 Distortion

Although the modulation of resistance is what makes a PIN diode so useful, undesired modulation can occur. If the RF frequency is low and the power is high relative to the bias current and carrier lifetime the amount of charge in the I-layer will vary. Thus the resistance of the PIN diode will wary with time resulting in harmonics generation and intermodulation. Harmonics is undesired multiples of the fundamental frequency. Since harmonics are far from the fundamental frequency they can be filtered rather easily. If multiple signals with different frequencies are used intermodulation between the signals will occur. Of special interest is the third order modulation product, IP3, which is closely spaced in frequency to the desired signal. Thus third order modulation products is hard to filter from the signal [18].

The reverse biased PIN diode is also susceptible to distortion. Contrary to the forward biased PIN diode distortion increases with increasing frequency. The distortion occurs as a result of varying capacitance with varying reverse bias voltage [19].

2.3 PIN diode driver

The purpose of the PIN diode driver is to switch the PIN diodes between two impedance states, a forward biased low impedance state and a reverse biased high impedance state. The switching of the impedance states is controlled by a TTL signal. The driver transforms the TTL signal into a bias condition; either a forward bias current or a reverse bias voltage. To change between these states the driver has to fill and deplete charge from the I-layer in the PIN diodes. Thus for fast switching it is important that the driver can supply large enough currents.

To translate the TTL signal into the bias conditions transistors are used. The transistors in the driver can supply more current than the low level TTL circuit. The transistors in the driver affect the characteristics considerably. There exists a multitude of transistors intended for a broad spectrum of applications. When considering transistors for a PIN diode driver there are a couple of important parameters. The PIN diode biasing requirements will translate into requirements on transistor voltage and current handling. If

switching speed is of importance the driver transistors need to be fast. In a switching application this translates to low parasitic capacitances in the transistors. As a smaller capacitance has to be charged before the transistor can change state between on and off the driver will be faster.

Chapter 3

PIN diode driver design

In this chapter the design of three drive circuits will be presented. The first drive circuit, driver A, is based on [16] and similar to a design currently in use at SAAB. The subsequent designs, driver B and C, are based on driver A but with improvements over the original design. The measurements of the drivers will be presented in Chapter 5.

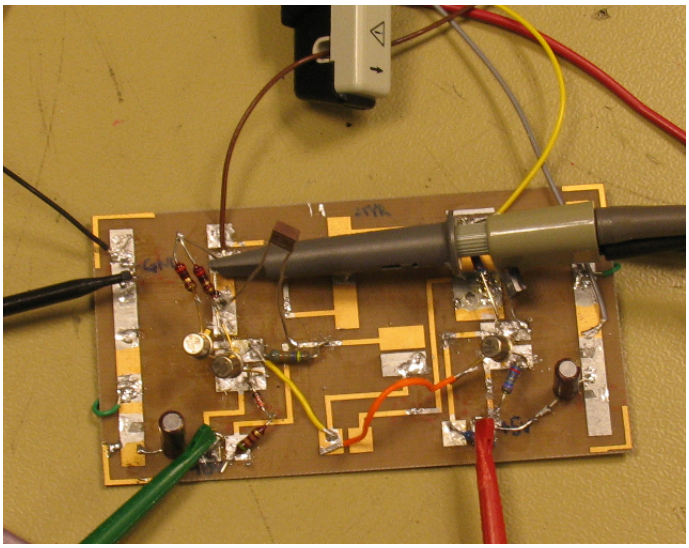


Figure 3.1: *Photograph of driver C with two parallel connected transistors. The current and voltage probes are also visible in photograph.*

3.1 Driver A

The first driver, driver A, was designed around two 2N2907 PNP transistors. The transistors were chosen partly because of their low intrinsic capacitances - enabling fast switching - and partly because they can supply the required bias current and reverse voltage. The circuit schematic of driver A can be seen in Figure 3.2. A TTL signal controls whether the driver should forward

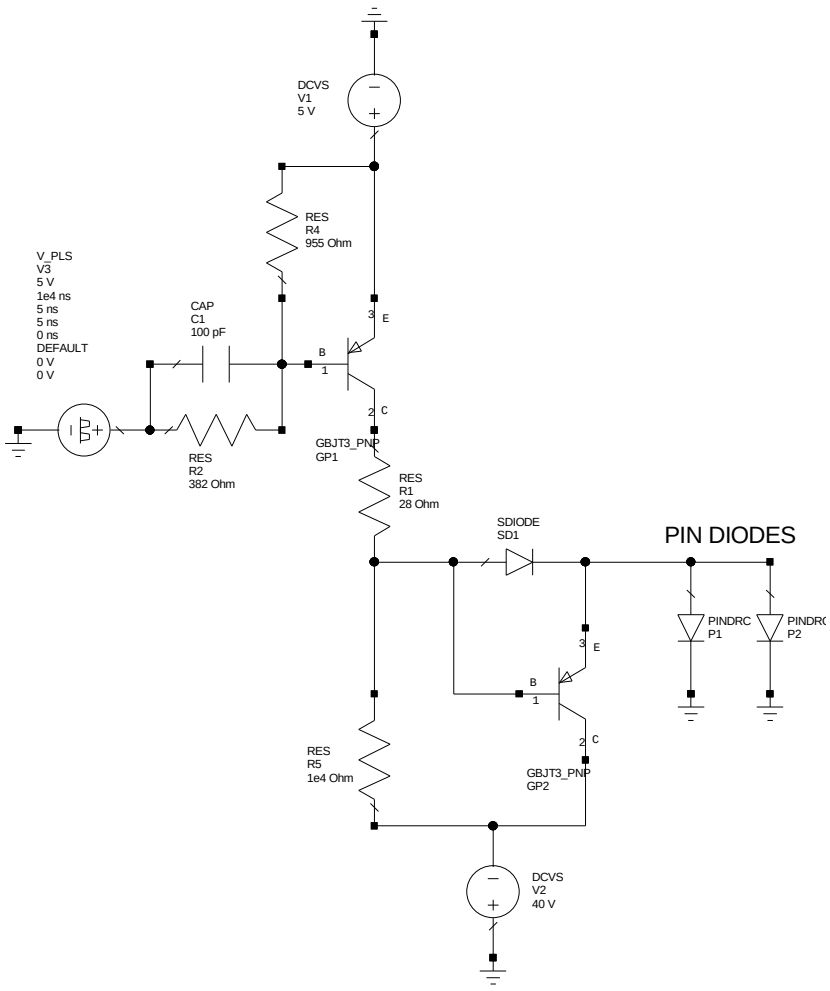


Figure 3.2: *Circuit schematic of driver A connected to two PIN diodes.*

or reverse bias the PIN diodes. This function is handled by the driver's

transistors. The transistors are biased in order to supply the correct forward current and reverse voltage. The driver thus transforms the TTL control signal into the required bias conditions.

When the TTL signal is low transistor Q1 is in the conductive state. Therefore a current flows through resistor R3 and diode D2 into the PIN diodes. At the same time transistor Q2 is in the non conducting state due to the reverse biased emitter-base junction caused by the voltage drop over diode D2. This is important since it prohibits both transistors from conducting at the same time. This would give rise to a low resistive path between the positive and negative rail leading to device failure. Resistor R3 limits the forward bias current to the specified $100mA$.

When the TTL signal is high transistor Q1 is in the non conducting state due to the reduced voltage drop over the emitter-base junction and therefore no current flows through resistor R3 and diode D2. Since diode D2 no longer reverse biases the emitter-base junction of transistor Q2, it enters the conductive state and a negative voltage is applied over the PIN diodes depleting it from stored charge.

The time response was simulated with the driver connected to two PIN diodes. The model of the PIN diodes consisted of physical parameters from the data sheet of Aeroflex MMP7069 PIN diodes. These PIN diodes have a carrier lifetime, τ_L, of $2\mu s$ and an I-layer width, x_I, of $80\mu m$. The simulated time response can be seen in Figure 3.3. The simulation results show that driver A is able to supply the required forward bias current and the reverse voltage. The time required to reverse bias the diode to 90% according to the simulations is about $1150ns$.

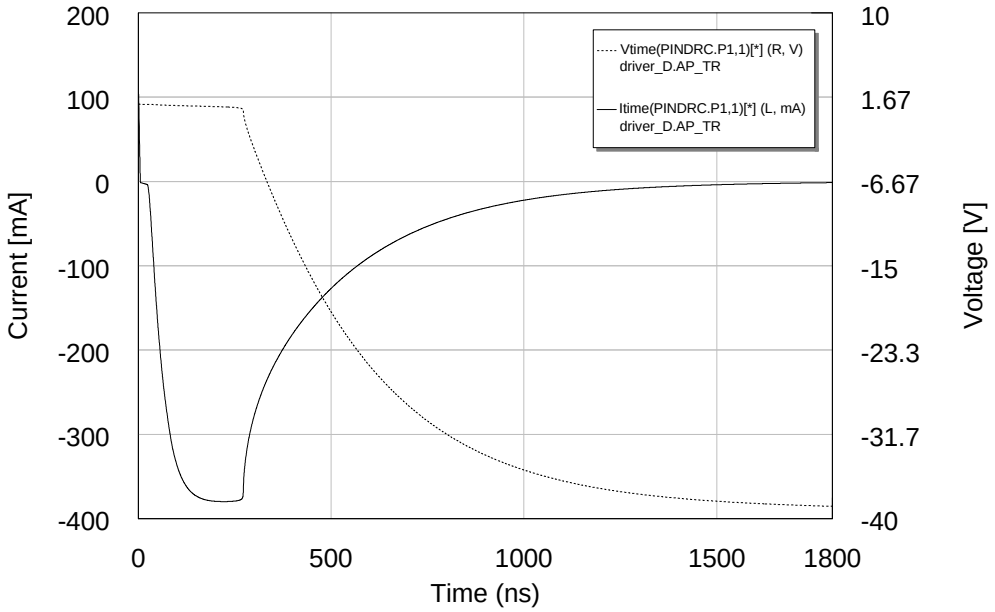


Figure 3.3: *The simulated voltage time response of driver A at* $-40V$ *reverse bias is presented on the right y-axis. The simulated time response of the reverse current is presented on the left y-axis.* $T = 0$ *indicates the time the control signal voltage reaches* 50%.

3.2 Driver B

Driver B was designed similar to driver A but bootstrapping of transistor Q2 was added. The bias resistor R4 is split into R4 and R5 and at the common terminal of the resistors a capacitor, C4, is connected to the emitter of Q2 according to Figure 3.4. Also a diode, D3, is used to ensure that the charge stored in C4 is not removed through R5. In order for the driver to function properly capacitor C4 has to be fully charged during the forward biased part of the cycle. The time needed to charge C4 is dependent on the product $C4 \cdot R5$. When Q2 is switched off capacitor C4 is charged through R5 and D2. When Q2 is on C4 maintains the voltage over R4 and thus the bias current in Q2 is maintained despite of the voltage drop over the PIN diodes. A second change is capacitor C3 connected between the input of the driver and the base of transistor Q1. When Q1 is on, charge is stored in the base region of the transistor. This charge has to be extracted from Q1 before it can switch off. In a similar manner, when Q1 is off charge needs to be injected in order for the transistor to turn on. This capacitor is used as a

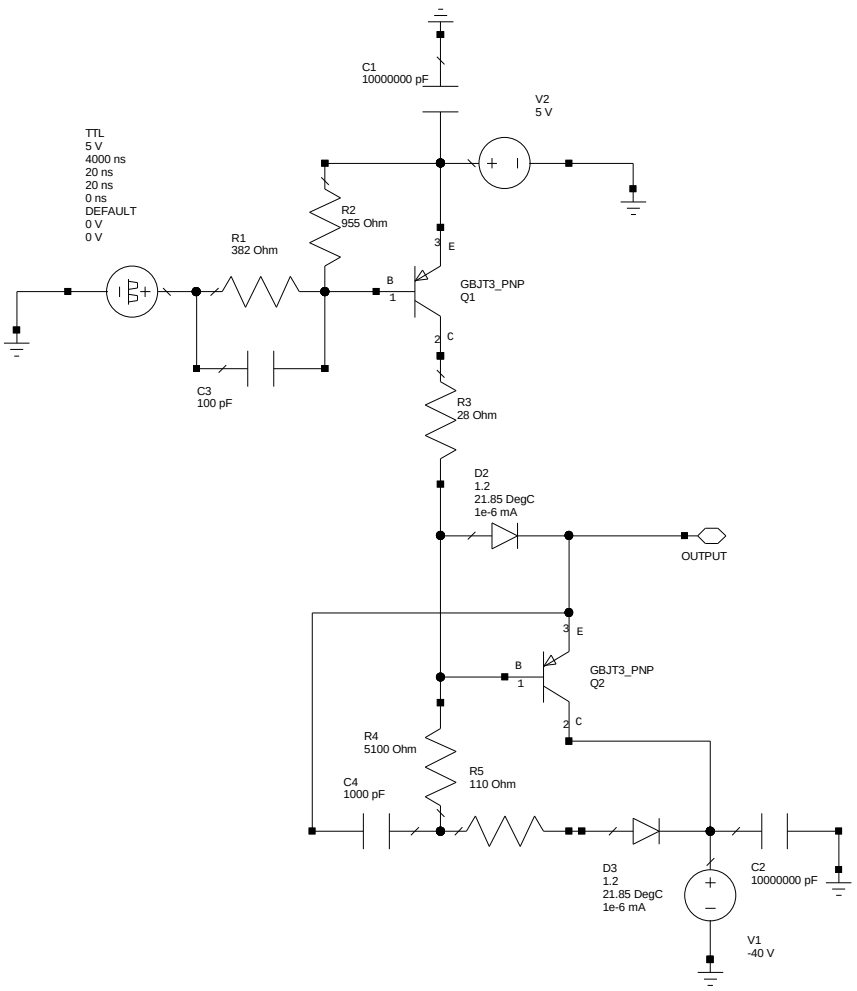


Figure 3.4: *Circuit schematic of driver B.*

speed-up component, aiding the control signal to extract and inject charge into Q1.

3.3 Driver C

In the design of driver C the biasing of transistor Q1 was revised. In other regards the design was kept the same as Driver B. To improve the biasing

of Q1 a Schottky diode was connected between the base and collector of Q1, a baker clamp configuration, according to Figure 3.5. The Schottky diode

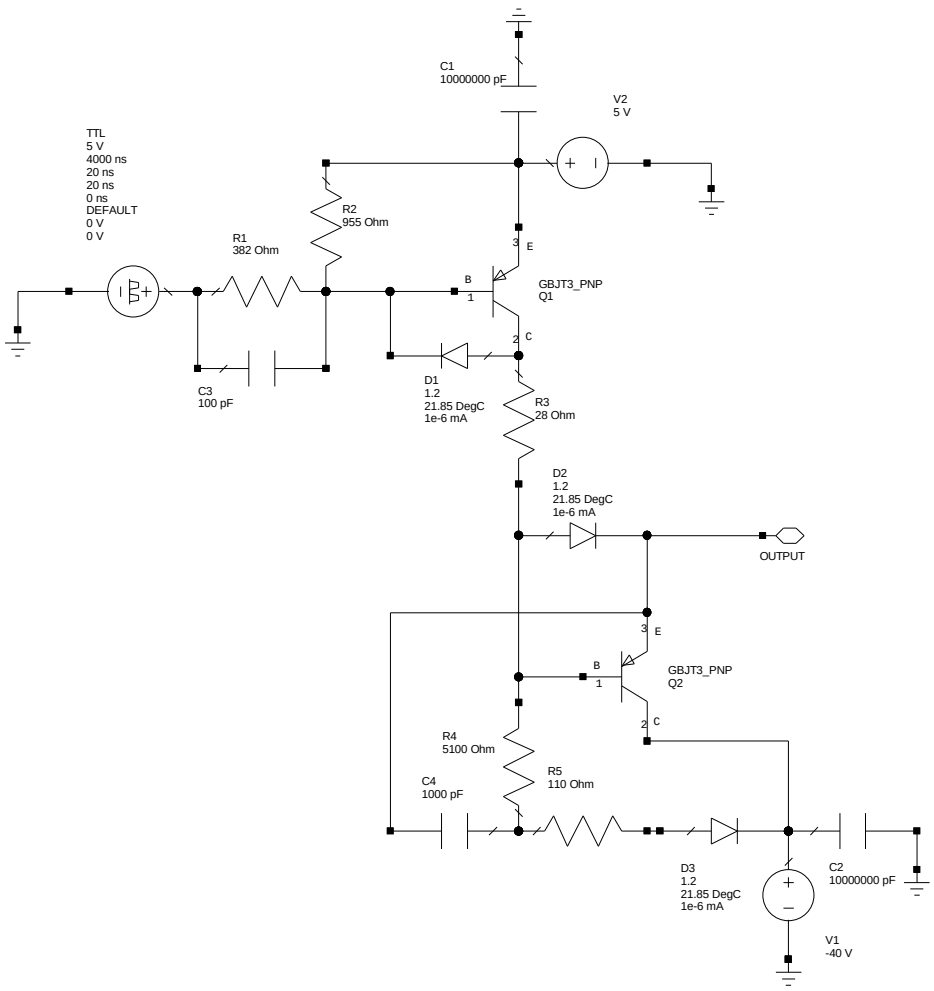


Figure 3.5: *Circuit schematic of driver C.*

limits the voltage drop over the collector-base junction to about $0.4V$, which is the built in junction voltage, and thus prevents saturation of Q1. This was done in order to reduce the switching time of Q1.

Simulation results from both Driver B and C are omitted due to the poor agreement between simulations and measurements.

Chapter 4

Measurement setup

The performance of the drivers in the time domain were measured by connecting the drivers to four parallel Aeroflex MMP7069 PIN diodes (a model of these diodes were used in the simulations). The drivers were biased through an Oltronix B703DT power supply and the TTL control signal was supplied by an Agilent 33220 signal/arbitrary waveform generator. A $10\mu s$ voltage pulse with a period of $100\mu s$ and a rise time of $5ns$ was supplied to the drivers. The voltage across the diodes was monitored with an Agilent DSO-X-2029A oscilloscope through a Tektronix P6131 10:1 voltage probe. The PIN diode current was also monitored using a Tektronix A6302 current probe and a AM503B probe amplifier. The RF source for the measurements was a HP8350B sweep oscillator with a HP8359 RF-plug in. The frequency of operation was $3GHz$, since this was the frequency the RF PIN diode circuit board was designed for. The RF power at the output was measured with a diode detector. The diode detector converts the RF voltage into a DC voltage, corresponding to the RF RMS voltage amplitude, which is monitored by the oscilloscope. The measurement setup is depicted in Figure 4.1. Both the time it takes for the RF power to reach $1dB$ from the final power level and the time it takes to reach 90% of the reverse voltage will be measured. The switching time will be defined as the longest of these two, because both these requirements needs to be satisfied.

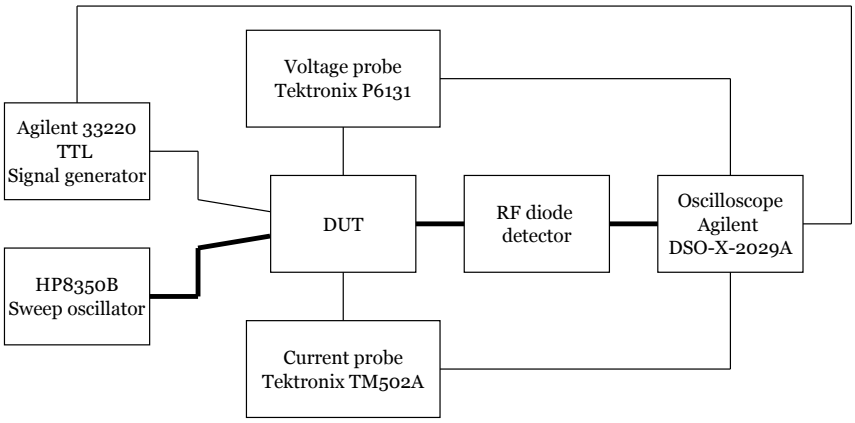


Figure 4.1: *Measurement setup for time domain characterization of the PIN diode drivers(DUT). The thicker line represents the RF path. The inputs to the DUT is the control signal supplied by the Agilent 33220 signal generator and the RF input signal is supplied by the HP8350B sweep oscillator. The RF output is then fed to the Agilent DSO-X-2029A oscilloscope via an RF diode detector.*

Chapter 5

Measurements

In this section three PIN diode drivers will be measured and characterized according to the procedure presented in the previous chapter.

The measurements of the three drivers can be seen in Figure 5.1, 5.2 and 5.3. In Figure 5.1 the voltage time response of the three drivers is presented. Then, in Figure 5.2 the RF power time response of the three drivers is presented. Lastly, in Figure 5.3 the current time response of the three drivers is presented.

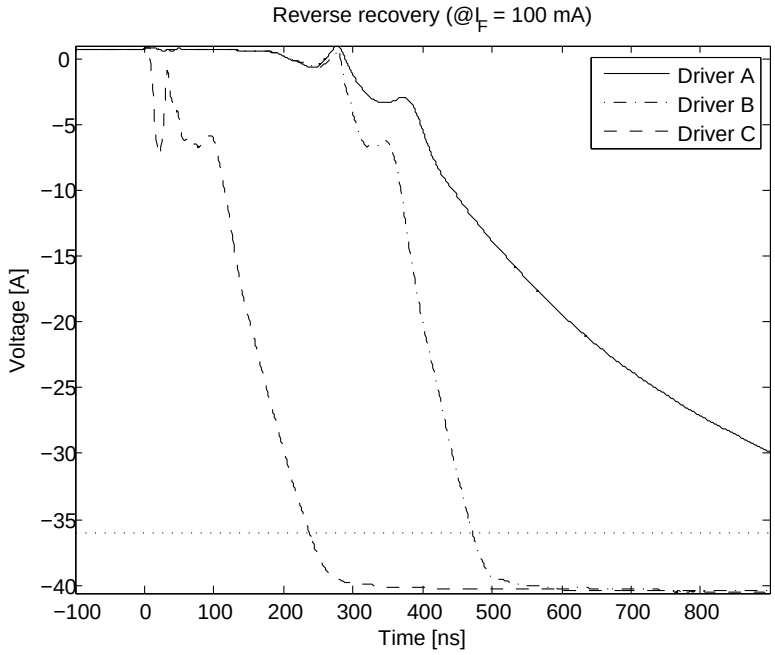


Figure 5.1: *The voltage time response of driver A, B and C. The dotted line is* 90% *of the reverse voltage.*

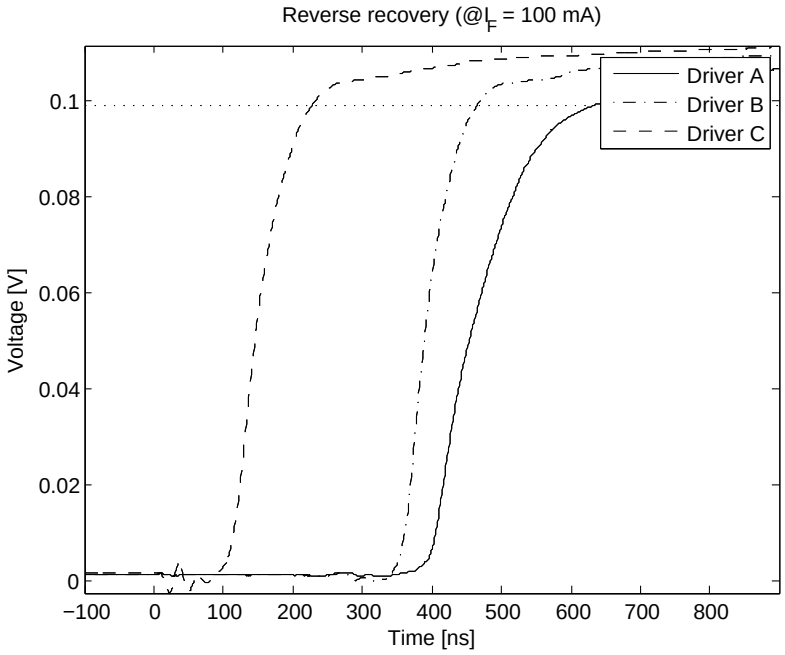


Figure 5.2: *The voltage time response from the RF power detector of driver A, B and C. The dotted line is* $1dB$ *from full RF power.*

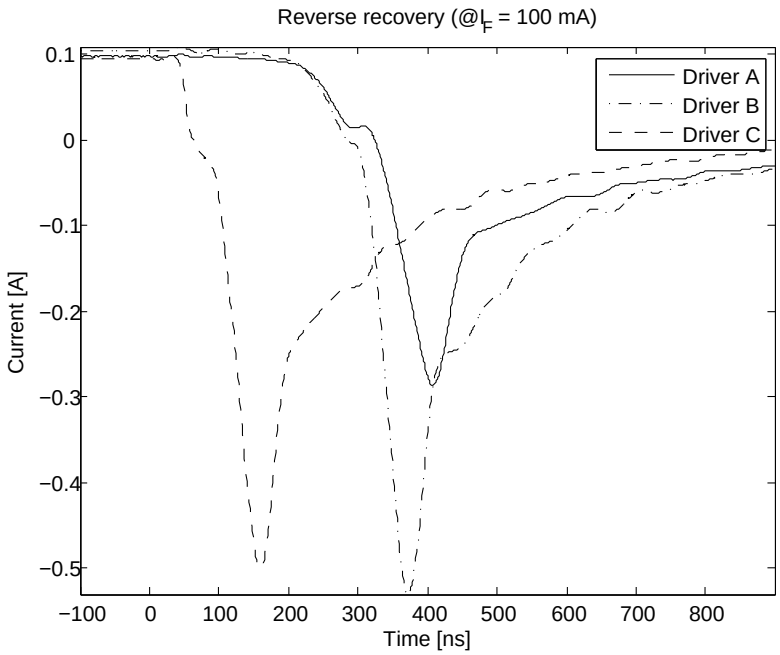


Figure 5.3: *The current time response of driver A, B and C.*

5.1 Driver A

The first $200ns$ after the control signal was switched there is little response from the driver. This depends largely on transistor Q1 which is saturated during forward bias. The charge in the transistor has to be removed before it can switch off. When transistor Q1 has switched off Q2 has to be filled with charge in order for the reverse current to start flowing. Then a large negative current spike removes charge from the PIN diodes. Until this spike has reached its maximum of $280mA$ the voltage across the PIN diodes is more or less constant and the PIN diodes are still in the low impedance state. When enough charge has been removed the impedance of the PIN diodes changes to the high impedance state and the voltage drop across the PIN diodes follows. The change in impedance can also be seen in Figure 5.2. The RF power level changes rapidly as soon as the peak of the current occurs. As the impedance of the PIN diodes get larger the driver is not able to withdraw as much current as during the spike. After the PIN diodes have reached the high impedance state the charge removal process is largely dependent on the carrier lifetime, τ_L, of the PIN diodes rather than the driver. Driver A is able to switch the PIN diodes from forward to 90% of reverse bias in $1200ns$.

Comparing the measurements of driver A to the simulations there are some major differences. The delay time before the current starts to fall is almost instant in the simulations compared to a delay time of about $200ns$ in the measurements. Also, there seems to be more stored charge in the simulated results. Due to the poor coherence between simulations and measurements the design process will continue through hardware design.

Driver A is able to switch between the two impedance states in $1200ns$. This is $800ns$ faster than the specified carrier lifetime of the PIN diodes. There seemed to be room for improvement of Driver A. Since the voltage over the bias resistor drops as the reverse voltage over the PIN diodes increases the base current of Q2 also decreases. Therefore it would be preferable to maintain the voltage over the biasing resistor. This can be achieved using a technique called bootstrapping, a technique useful for pulsed signals.

5.2 Driver B

The switching characteristics of driver B was measured with the same test setup as driver A and the results are also presented in Figure 5.1, 5.3 and 5.2.

From Figure 5.3 it can be seen that the time delay before the current falls

is identical to driver A. Driver B was able to switch from a forward bias of $100mA$ to 90% of the $-40V$ reverse bias in $456ns$. Compared to driver A the current peak through the PIN diodes of driver B is about $100mA$ larger and sustained for a longer time. As more current is extracted from the PIN diodes at a faster pace it is only natural that the impedance of the diodes and hence the reverse voltage over the PIN diodes changes faster. This can be attributed to the bootstrapping circuitry's ability to sustain the bias current in transistor Q2.

5.3 Driver C

From Figure 5.3 it is evident that the delay before the current drops is reduced compared to driver A and B. The delay time for driver C is $50ns$ compared to $200ns$ for driver A and B. As the driver is able to withdraw current at an earlier stage this also affects the switching time.90% of reverse bias is reached in $250ns$.

To further improve the performance of the driver different values of capacitors C3 and C4 was tested. The capacitance of C3 was varied between $56pF$ and $560pF$ and the capacitance of C4 was varied between $50pF$ and $2000pF$. A capacitance of $220pF$ for C3 and a capacitance of $180pF$ for C4 yielded the fastest response.

The change of C3 and C4 further improved the performance of the driver. The original values was optimized with Microwave Office. It is evident that there are major differences between the measurements and the simulations. The time before the current dropped in the load is reduced to $40ns$. Considering the requirements on the driver this time delay is probably close to the limit of the 2N2907 transistors. The transistors' emitter-base and collector-base capacitances are specified at $30pF$ and $8pF$ respectively.

To further improve the speed of driver C the resistance values of R4 and R5 could be reduced. These resistors control the base current in transistor Q2 and thus limits the collector current. This configuration reaches a reverse voltage of $-40V$ in just $150ns$ and the time delay is unchanged. All though a faster driver is achieved a larger current will be drawn through the resistors when transistor Q2 is cut off. To be able to supply the same forward bias current to the load the bias point of transistor Q1 has to be changed in order to increase the collector current. This will increase heat development and reduce the efficiency of the driver.

Evident in driver C and present in all the drivers' time response is the irregular behaviour of the voltage at the beginning of the voltage drop. This behaviour probably stems from the layout (or lack there of) of the drivers in

combination with the fast change in voltage and current.

5.4 Driver C with different loads

Driver C with optimized capacitances and resistor $R4 = 5.1k\Omega$ was tested with different loads. Four PIN diodes with different characteristics was tested.

Table 5.1: *Electrical characteristics for the PIN diodes used in this study as specified by the manufacturers.*

Item	$V_B[V]$	$R_S[\Omega]$	$C_T[pF]$	$R_P[k\Omega]$	$\tau_L[\mu s]$	$x_I[\mu m]$
MA-COM MA4P4002B-402	200	0.5	2.2	20	20	175
MA-COM MA4P7104F-1072	400	0.5	1.0	100	2.5	100
Aeroflex MMP7069	500	6.0	0.2	–	2	80

First the driver was connected to a MA-COM MA4P7104F-1072 PIN diode. The time response can be seen in Figure 5.4. The results are very similar to the Aeroflex MMP7069 PIN diode measured earlier. Evident though, is the lower peak current. Theoretically a PIN diode with longer lifetime should have more stored charge.

A MA4P4002B-402 PIN diode with a lifetime of $20\mu s$ was connected to the driver, the time response can be seen in Figure 5.5. It can be seen from the figure that the driver was saturated at a reverse current of about $580mA$. The limiting factor is the finite DC current gain in transistor Q2. To improve the performance two transistors were connected in parallel, with two low value resistors between the emitters to ensure equal current sharing, in order to be able to withdraw more current.

The time response of the driver, connected to the same MA4P4002B-402 PIN diode but with two parallel connected transistors in the position of Q2, is plotted in Figure 5.6. Compared to Figure 5.5 the peak reverse current is improved to $750mA$. It can also be seen that the voltage over the diode drops considerably faster due to the faster current extraction. The circuit still shows some signs of saturation, probably due to finite DC current gain. But since the reverse peak current is split between two transistors it is improved some due to the higher DC current gain at lower collector current.

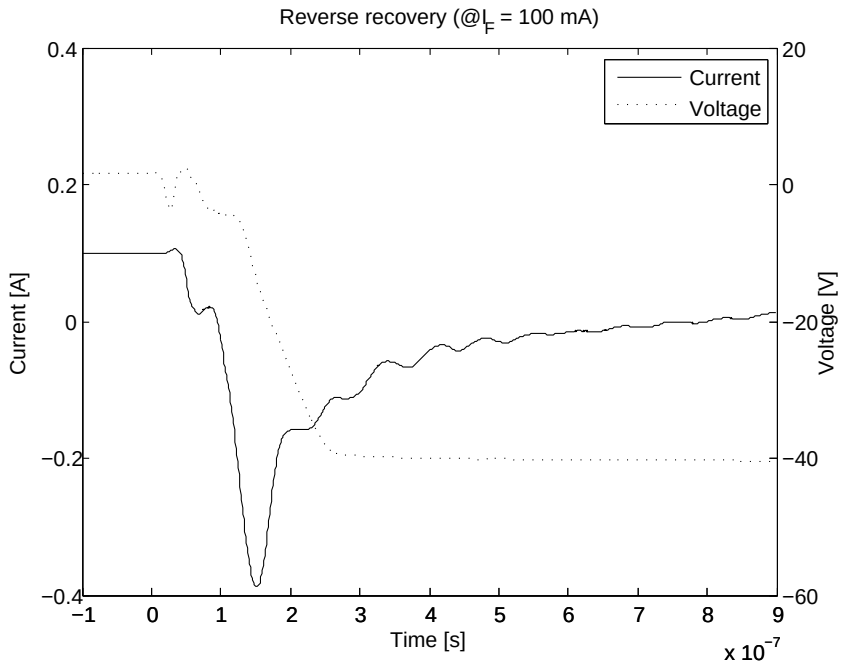


Figure 5.4: *The voltage time response of driver C, with a* $2.5\mu s$ *MACOMMA4P7104F-1072 PIN diode, at* $-40V$ *reverse bias and* $100mA$ *forward bias is presented on the right y-axis. The time response of the reverse current is presented on the left y-axis.* $T = 0$ *indicates the time the control signal voltage reaches* 50%*.*

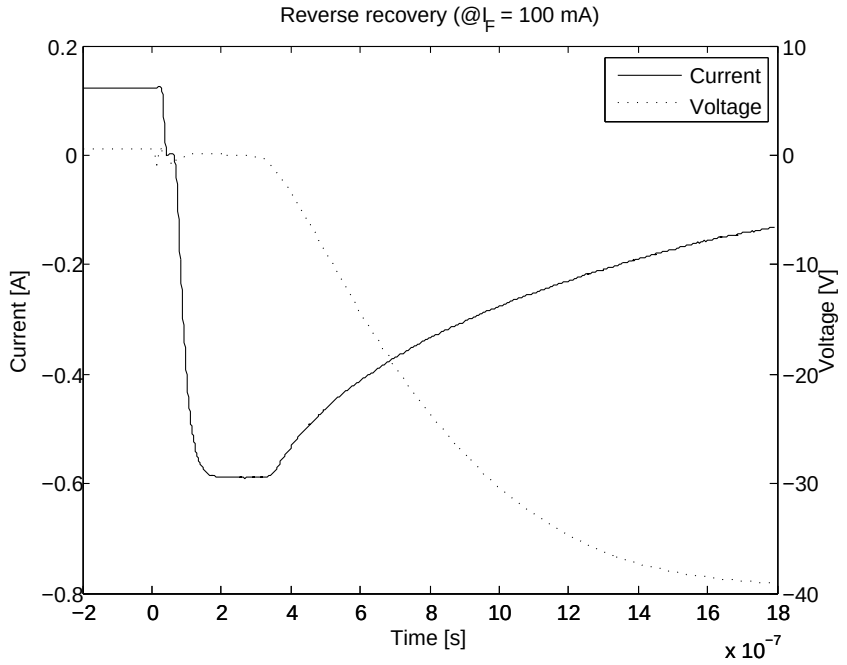


Figure 5.5: *The voltage time response of driver C, with a* $20\mu s$ *MACOMMA4P4002B-402 PIN diode, at* $-40V$ *reverse bias and* $100mA$ *forward bias is presented on the right y-axis. The time response of the reverse current is presented on the left y-axis.* $T = 0$ *indicates the time the control signal voltage reaches* 50%*.*

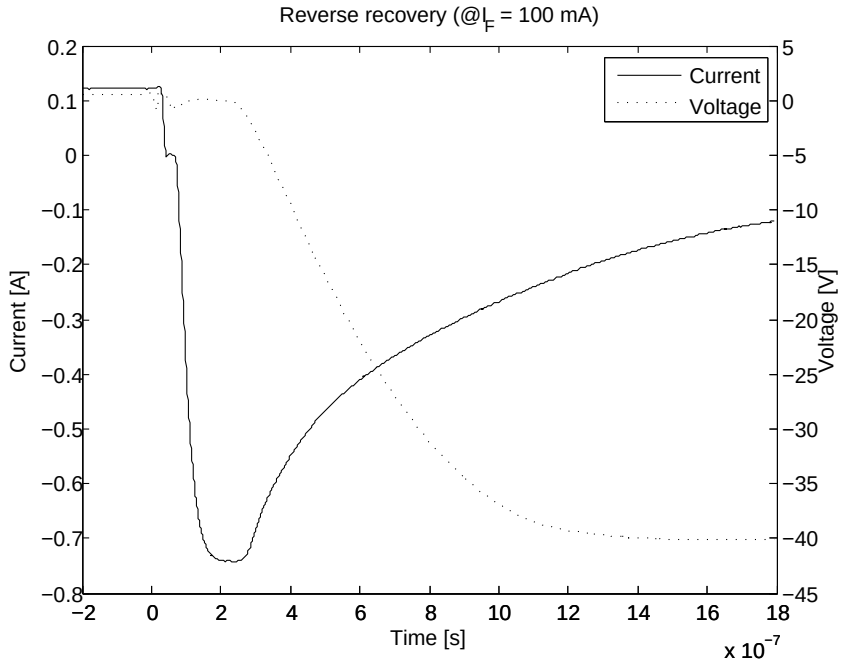


Figure 5.6: *The voltage time response of driver C with two parallel transistors, with a* $20\mu s$ *MA-COMMA4P4002B-402 PIN diode, at* $-40V$ *reverse bias and* $100mA$ *forward bias is presented on the right y-axis. The time response of the reverse current is presented on the left y-axis.* $T = 0$ *indicates the time the control signal voltage reaches* 50%*.*

5.5 Bias conditions

The drivers' behaviour under different reverse bias conditions were also studied. Driver B was biased with a forward current of $100mA$ and the reverse bias was varied from $-5V$ to $-40V$. The time response of the device under the different bias conditions is presented in Figure 5.7. It is evident that

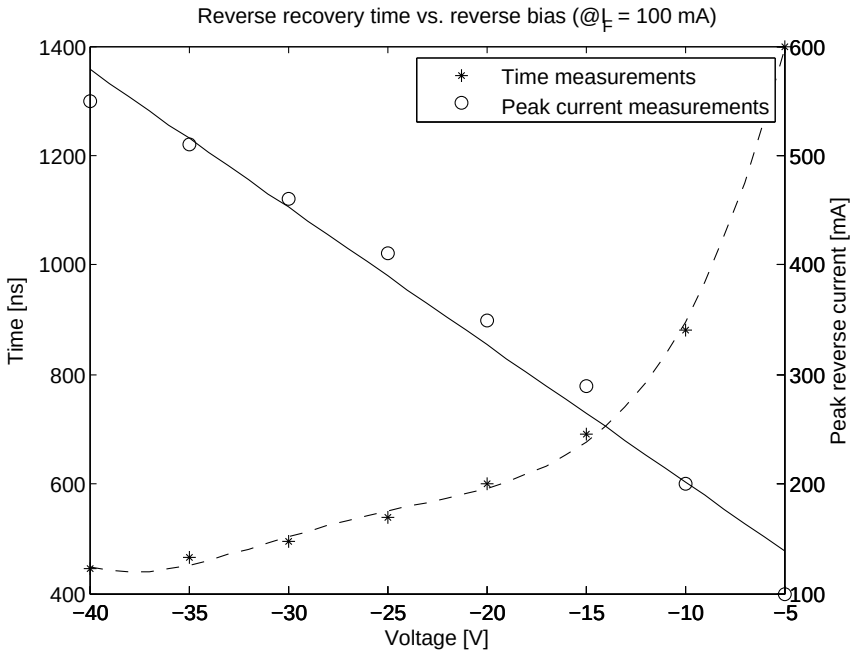


Figure 5.7: *The time response of driver B at different reverse bias is presented on the left y-axis. The peak reverse current is presented on the right y-axis.*

a larger peak current results in a faster time response. However, the effect of a large peak current saturates as the peak current reaches $300mA$. At which peak current level the saturation appears will be dependent on the parameters of the PIN diode.

Figure 5.7 seems to indicate that a larger reverse voltage produces a faster driver. This is probably not the case, but due to the design of the biasing circuit transistor Q2 receives a larger bias current at a larger reverse voltage and thus is able to remove more charge from the PIN diodes.

5.6 Driver transistors

The transistors in the drivers are the 2N2907 intended for medium power switching and general purpose applications. The 2N2907 emitter-base and collector-base capacitances are specified at $30pF$ and $8pF$ respectively, for fast switching these should be as small as possible. The behaviour of the driver using different transistors was studied. Both BF423 high voltage PNP transistor and MPSA93 high voltage PNP transistor was studied. Both of these transistors slowed down the driver considerably This can probably be attributed to large parasitic capacitances at $-40V$.

5.7 Result summary

The time response of the drivers is summarized in table 5.2. It is evident that a large reverse current peak produces a fast time response and the results correlates well with this statement.

Table 5.2: *Compilation of the different drivers' time response parameters: time for reverse recovery = t_{rr}, time delay = t_d and peak reverse current = I_{peak}. The drivers delivered* $100mA$ *forward bias current to two shunt Aeroflex MMP7069 PIN diodes.*

DUT	$t_{V90\%}[ns]$	$t_d[ns]$	$I_{peak}[mA]$	$t_{P1dB}[ns]$
Driver A	1200	200	280	633
Driver B	456	200	390	464
Driver C	237	40	530	227
Driver C ($R4 = 1000\Omega$)	133	40	830	177

In Figure 5.1 and 5.2 there is a difference in time delay between driver A and driver B compared to driver C. As mentioned this time delay is inherent from charge storage in transistor Q1. The superior biasing of driver C eliminates unnecessary charge storage and thus reduces the time delay. This bias arrangement could be applied to driver A as well but this would still produce a relatively slow driver because of the small reverse current peak produced. The biasing of Q1 is not the only thing that determines the time delay, the characteristics of the transistor also affects the time delay. In bipolar transistors charge storage phenomenon induces time delay in the devices. This phenomenon can be modelled as a capacitance. These are often specified in

data sheets and should be as low as possible for fast operation. To summarize, in order to get the time delay as small as possible a transistor with low internal capacitances should be selected and the transistor should be biased efficiently.

The biasing of transistor Q2 has a large impact on the peak reverse current. A smaller resistance increases the base current and thus the reverse peak current. The reverse peak current will however be limited by the current gain of Q2. The drawback with a high base current in Q2 is the leakage current through the small biasing resistors when Q2 is off. Thus, the biasing network has to be designed as a trade-off between power consumption and switching speed.

It has been shown that a large reverse current peak translates to fast switching between the PIN diodes low and high impedance states. This is in agreement with the theory previously presented. To be able to produce this current peak the driver transistors have to be able to handle the current and be biased properly. In order to utilize the effect of such a current peak the driver has to be able to supply the peak as quickly as possible as this changes the impedance of the PIN diode in the fastest manner. However, a transistor that switches fast rarely handles large currents well. Thus, a trade-off between time delay and peak current handling capability exists. The problem is then to match the transistors in the driver to best suit the PIN diodes used. As the options might be limited, parallel connection of several fast transistors with relatively low current handling capabilities has been shown to improve the peak current and still keep the time delay short. If a PIN diode with a long carrier lifetime in combination with a large forward bias current has to be used the time delay might only be a small fraction of the time required to remove the stored charge. Thus, a slower transistor with better current handling capabilities may be the better option.

Evident from the results reported is the trade-off between a large base current to transistor Q2 and efficiency, a weakness in the studied driver topology. In order to optimize the ratio between the peak reverse current and the leakage current a transistor with a DC current gain as high as possible should be selected.

There were some major differences between the measurements and the simulations of driver A. The delay time before the current starts to fall is almost instant in the simulations compared to a delay time of about $200ns$ in the measurements. This discrepancy is probably caused by the inaccuracy of the transistor model used in the simulations. Also evident from the comparison is the fact that there seems to be more stored charge in the simulated results. This discrepancy could be caused by the PIN diode model used in the software, the model is based on [20]. But since the accuracy of

the model depends on both the model equations and the model parameters the problem might as well stem from the parameters given by the PIN diode manufacturer.

Chapter 6

Conclusions

Several similar driver topologies have been designed and measured. The results show that rather small changes in the driver design affects the performance of the device considerably. It was possible to reach these improvements by adding relatively few components to the original design, thus maintaining a small footprint.

Since the PIN diode impedance is a function of stored charge in the device the charge has to be removed and injected as fast as possible in order to achieve a fast time response. This implies that the driver has to supply a large current in a short amount of time with a short time delay. To realize this a number of improvements was added to the driver design.

The most significant improvement came from the addition of the bootstrap circuitry, in driver B, which maintains an adequate base current despite the increasing voltage drop over the PIN diodes. This modification resulted in a voltage time response that was $836ns$ faster than driver A.

The addition of a more efficient forward bias circuitry, limiting transistor saturation and thus an unnecessary amount of stored charge in the transistor, further improved the performance of the driver.

The fastest prototype, driver C, utilized both of the mentioned improvements which resulted in a switching time of $237ns$.

It was found that the base current bias resistor, $R4$, of transistor $Q2$ greatly influences the time response of the driver. Since this resistor controls the peak current through $Q2$ there is an obvious gain with a low resistance. Despite this performance gain the driver should not be designed with $R4$ to low since a low resistance degrades the driver efficiency. A transistor with higher DC current gain would improve this issue, although high DC current gain in a transistor is rarely seen in combination with switching performance and power handling capability. This is an area of the design that needs further work, as a circuit that would enable both a large biasing current and

a low leakage current would be very advantageous.

Despite the limited usefulness of a driver with small biasing resistor it still proved to be the fastest. A switching time of just $177ns$ was obtained with the biasing resistor, $R4 = 1000\Omega$.

The driver design has been proven to work with a number of PIN diodes with different characteristics, although some modifications were applied in order to optimize the speed. This implies that the driver design is suitable for applications with a wide variety of requirements.

The comparison between the simulated circuit and the measured result indicate that the agreement between the two is uncertain. Although no rigorous comparison was made it is still recommended to use the software only to get a rough estimation of the time response.

In applications where fast switching speed is not critical a fast driver can still improve the performance of the switch. Because a faster driver enables the use of a PIN diode with higher carrier lifetime, while still maintaining the same switching speed, which implies a lower forward resistance. For the performance of the switch this would result in a lower insertion loss. With the same approach, a faster driver could be used to drive more diodes as more current can be delivered in the same time. This would result in a smaller footprint for the switch.

Bibliography

[1] D. M. Pozar, *Microwave and RF Wireless Systems.* John Wiley & Sons, Inc., 2001.

[2] J.-L. Lee, D. Zych, E. Reese, and D. Drury, "Monolithic 2-18 ghz low loss, on-chip biased pin diode switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 2, pp. 250 –256, feb 1995.

[3] J. Putnam, M. Fukuda, P. Staecker, and Y.-H. Yun, "A 94 ghz monolithic switch with a vertical pin diode structure," in *16th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, oct. 1994, pp. 333 – 336.

[4] A. Klaassen and J.-M. Dieudonne, "77 ghz monolithic mmic schottky- and pin-diode switches based on gaas mesfet and silicon simmwic technology," in *IEEE MTT-S International Microwave Symposium Digest*, may 1995, pp. 1631 –1634 vol.3.

[5] Q. Chen, M. Kurahashi, and K. Sawaya, "Dual-mode patch antenna switched by pin diode," in *IEEE Topical Conference on Wireless Communication Technology*, oct. 2003, pp. 148 – 149.

[6] R. Caverly and A. Hoorfar, "Reconfigurable hilbert antennas using high speed pin diodes," in *Radio and Wireless Symposium, 2009. RWS '09. IEEE*, jan. 2009, pp. 151 –154.

[7] J.-H. Lim, G.-T. Back, Y.-I. Ko, C.-W. Song, and T.-Y. Yun, "A reconfigurable pifa using a switchable pin-diode and a fine-tuning varactor for uspcs/wcdma/m-wimax/wlan," *IEEE Transactions on Antennas and Propagation*, vol. 58, no. 7, pp. 2404 –2411, july 2010.

[8] A. Rosen, P. Srabile, W. Janton, A. Gombar, J. McShea, R. Buckingham, A. Rosenberg, P. Herczfeld, and A. Bahasadri, "Optically activated pin diode switch," in *IEEE Conference Record of the 1988 Eighteenth Power Modulator Symposium*, jun 1988, pp. 223 –226.

[9] K. Kobayashi, A. Oki, L. Tran, and D. Streit, "A novel baseband-1.5 ghz monolithic hbt variable gain amplifier with pin diode gain control," in *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, may 1995, pp. 181 –184.

[10] D. M. Pozar, *Microwave Engineering.* John Wiley & Sons, Inc., 2005.

[11] T. K. Ishii, *Handbook of microwave technology.* S.l: Academic Press, 1995.

[12] S. M. Sze and N. Kwok, *Physics of semiconductor devices 3rd ed.* Interscience, 2006.

[13] R. H. Caverly and G. Hiller, "Establishing the minimum reverse bias for a p-i-n diode in a high-power switch," *IEEE Transactions on microwave theory and techniques*, vol. 38, pp. 1938–1943, 1990.

[14] N. Kwok, *Complete Guide to Semiconductor Devices.* Wiley-IEEE Press, 2010.

[15] J. Lutz, H. Schalangenotto, U. Scheuermann, and R. D. Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability.* Springer, 2009.

[16] W. E. Doherty and R. D. Joos, *The PIN diode circuit designers' handbook.* Microsemi Corporation, 1999.

[17] *Application Note 80200: PIN Diode Basics.* Alpha Industries Inc., 1990.

[18] R. Caverly and G. Hiller, "Distortion in p-i-n diode control circuits," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 35, no. 5, pp. 492 – 501, may 1987.

[19] ——, "Distortion in microwave and rf switches by reverse biased pin diodes," in *IEEE MTT-S International Microwave Symposium Digest*, jun 1989, pp. 1073 –1076 vol.3.

[20] R. Caverly, N. Drozdovski, L. Drozdovskaia, and M. Quinn, "Spice modeling of microwave and rf control diodes," in *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, vol. 1, 2000, pp. 28 –31 vol.1.

Appendix A

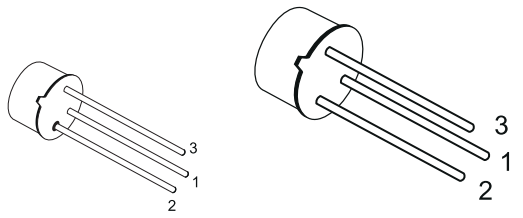
2N2907 transistor datasheet

2N2905A
2N2907A

SMALL SIGNAL PNP TRANSISTORS

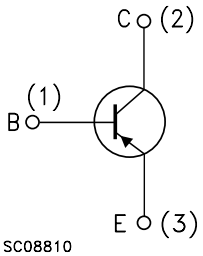
DESCRIPTION

The 2N2905A and 2N2907A are silicon Planar Epitaxial PNP transistors in Jedec TO-39 (for 2N2905A) and in Jedec TO-18 (for 2N2907A) metal case. They are designed for high speed saturated switching and general purpose applications.



TO-18 **TO-39**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	-60	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	-60	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	-5	V
I_C	Collector Current	-0.6	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	-0.8	A
P_{tot}	Total Dissipation at $T_{amb} \leq 25\ ^oC$		
	for **2N2905A**	0.6	W
	for **2N2907A**	0.4	W
	at $T_C \leq 25\ ^oC$		
	for **2N2905A**	3	W
	for **2N2907A**	1.8	W
T_{stg}	Storage Temperature	-65 to 175	^oC
T_j	Max. Operating Junction Temperature	175	^oC

THERMAL DATA

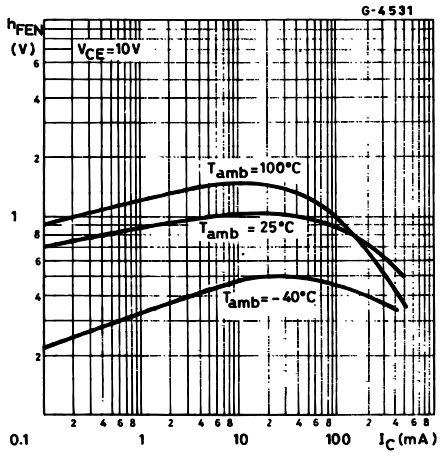
		TO-39	TO-18	
$R_{thj\text{-}case}$	Thermal Resistance Junction-Case Max	50	83.3	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-Ambient Max	250	375	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

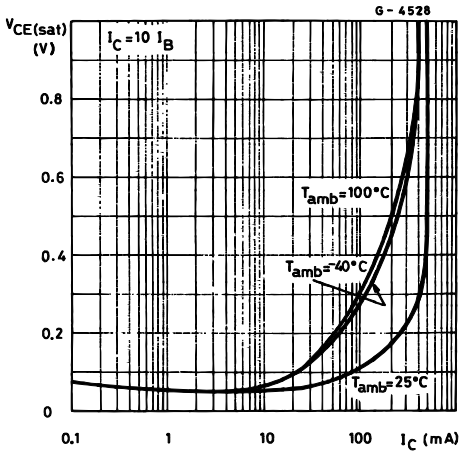
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-off Current (I_E = 0)	V_{CB} = -50 V V_{CB} = -50 V T_j = 150 °C			-10 -10	nA µA
I_{CEX}	Collector Cut-off Current (V_{BE} = 0.5V)	V_{CE} = -30 V			-50	nA
I_{BEX}	Base Cut-off Current (V_{BE} = 0.5V)	V_{CE} = -30 V			-50	nA
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_E = 0)	I_C = -10 µA	-60			V
$V_{(BR)CEO}$*	Collector-Emitter Breakdown Voltage (I_B = 0)	I_C = -10 mA	-60			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage (I_C = 0)	I_E = -10 µA	-5			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = -150 mA I_B = -15 mA I_C = -500 mA I_B = -50 mA			-0.4 -1.6	V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = -150 mA I_B = -15 mA I_C = -500 mA I_B = -50 mA			-1.3 -2.6	V V
h_{FE}*	DC Current Gain	I_C = -0.1 mA V_{CE} = -10 V I_C = -1 mA V_{CE} = -10 V I_C = -10 mA V_{CE} = -10 V I_C = -150 mA V_{CE} = -10 V I_C = -500 mA V_{CE} = -10 V	75 100 100 100 50		 300	
f_T	Transition Frequency	V_{CE} = -20 V f = 100 MHz I_C = -50 mA	200			MHz
C_{EBO}	Emitter-Base Capacitance	I_C = 0 V_{EB} = -2 V f = 1MHz			30	pF
C_{CBO}	Collector-Base Capacitance	I_E = 0 V_{CB} = -10 V f = 1MHz			8	pF
t_d**	Delay Time	V_{CC} = -30 V I_C = -150 mA I_{B1} = -15 mA			10	ns
t_r**	Rise Time	V_{CC} = -30 V I_C = -150 mA I_{B1} = -15 mA			40	ns
t_s**	Storage Time	V_{CC} = -6 V I_C = -150 mA I_{B1} = -I_{B2} = -15 mA			80	ns
t_f**	Fall Time	V_{CC} = -6 V I_C = -150 mA I_{B1} = -I_{B2} = -15 mA			30	ns
t_{on}**	Turn-on Time	V_{CC} = -30 V I_C = -150 mA I_{B1} = -15 mA			45	ns
t_{off}**	Turn-off Time	V_{CC} = -6 V I_C = -150 mA I_{B1} = -I_{B2} = -15 mA			100	ns

* Pulsed: Pulse duration = 300 µs, duty cycle ≤ 1 %
** See test circuit

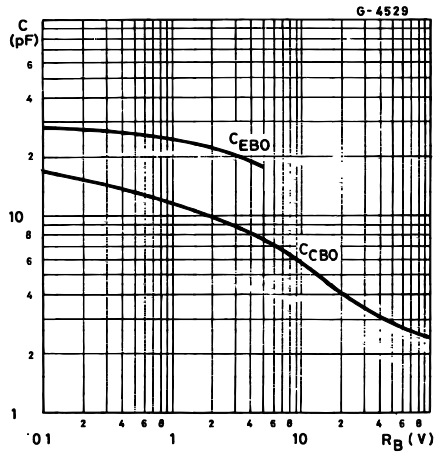
Normalized DC Current Gain.



Collector Emitter Saturation Voltage.



Collector Base and Emitter-base capacitances.



Switching Characteristics.