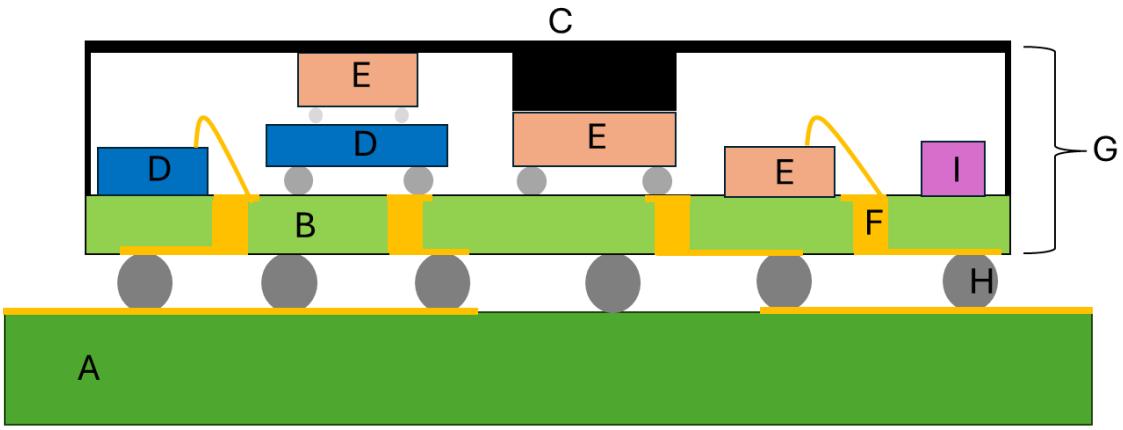

Towards a High Power RF System-in-Package Technology

Enabling Future RF SiP Development Through Simulation, Integration, and Measurement Capability

Master's thesis in Master Programme Wireless, Photonics and Space engineering

Viktor Engström

DEPARTMENT OF MICROTECHNOLOGY AND NANOSCIENCE
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2026
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Cover: A arbitrary System in Package solution.

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Abstract

This thesis investigates a System-in-Package (SiP) solution for future Radio Frequency (RF) applications. The work focuses on the development of a design and evaluation methodology for future RF-SiP implementation using electromagnetic simulation. The study includes the investigation of different material properties and their impact on important SiP building blocks and overall RF performance. A particular focus is placed on the evaluation of a novel silicon carbide (SiC) interposer technology currently under development. Passive RF components, including inductors and filters, were designed and implemented on the interposer in order to evaluate its suitability for RF applications. MultiTech simulations in ADS RFPro were used as a design tool and method for evaluating RF-SiP structures, material properties, and flip-chip integrated components. In addition, an evaluation board with a calibration kit for future RF-SiP measurements was designed as part of the work. The results provide insights into the design and development of future RF-SiP systems. The findings indicate that ADS and MultiTech provide support for RF-SiP development and evaluation, although several limitations were identified during the design and simulation process. Furthermore, the investigated interposer and the investigated passive components demonstrates promising characteristics for RF applications, while flip-chip integration affects needs to be accounted for. Overall, the findings contribute to a broader understanding of RF-SiP design process and provide insights to the development of future broadband and high-power RF-SiP solutions.

Keywords: SiP, ADS, Interposer, Flip-chip, Filter, Inductor, FEM

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Viktor Engström, Gothenburg, June 2026

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1
Introduction

Modern electronic systems demand increasingly more functions and greater capacity in society today. The need to transfer larger amount of data across vast distances is one of the main driving forces. In recent years this has become even more important in a rapidly changing world. When products become increasingly connected, the demands on both the products themselves and the communication system increase. Because of this, modern RF and wireless systems are moving towards compact platforms that combine sensing, communication, and processing functions. This is the case for both land- and air-based systems where requirements of size and power consumption has become important metrics. Increased integration density has introduced new challenges for the electronics when better performing circuits needs to be cheaper and implemented on a smaller area with lower power consumption and weight. These metrics can be described using the concept of Size, Weight, Power, Price and Performance ($SWaP^3$). This has become an important benchmark in the design and evaluation of modern electronic systems [1].

For digital integrated circuits, reductions in size and weight have historically been accomplished by scaling semiconductor process nodes, i.e. reducing the minimum feature size and gate length of transistors during manufacturing. This transistor scaling has enabled advances in digital technologies such as Central Processing Units (CPU), Graphics Processing Units (GPU) and memory devices. This has laid the foundation of modern digital infrastructure. However, further scaling of process nodes has become increasingly difficult, while the computational demands of modern electronic systems continue to increase [2].

One way to overcome this computational problem is by integrating multiple chiplets into the same package. A chiplet is a semiconductor chip with multiple transistor nodes designed for a specific purpose that is placed inside a package. One important package technique for chiplets is the so-called System-in-Package (SiP) [3], which is an important technology for advanced electronic systems. SiP is a method where multiple chiplets can be placed in a compact package and thereby improve the overall $SWaP^3$. An example of a SiP is when memory and processing chiplets are vertically stacked in the same package instead of being placed side by side, which reduces signal path lengths, minimizing footprint, and improving overall system performance [4],[5].

Chiplet integration has moved from digital systems into mixed signal applications combining analog and digital circuits. Examples of this include the integration

of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and FPGA chiplets within the same package [6]. The integration technique has also expanded to the optical domain where input/output interfaces are being integrated into SiP packages [7].

Moving forward in the development of SiP solutions, the next step is to integrate radio-frequency (RF) functions directly into the package. This is achieved by placing RF circuits on a chiplet, creating a RF-chiplet that is incorporated into an SiP. An SiP solution has the potential to enable compact communication systems with better SWaP^3 metrics compared to regular RF systems. RF integration within SiP architectures has to some extent been explored [8],[9],[10],[11] but this research has only focused on a small part of a whole SiP solution. Still, many challenges remain before the technology is mature. These challenges include broadband signal transmission between different SiP building blocks since it is needed for multiple SiP implementations. The electromagnetic environment, including signal leakage surrounding conductors and transitions between materials must be characterized. Implementation of active components on RF-chiplets and passive components on both a RF-chiplet and interposers is needed to be evaluated. Material capabilities for the different building blocks requires to be examined, this includes thermal capabilities and cooling solutions. Bonding techniques between RF-chiplets and interposer within a SiP needs to be evaluated. Another large challenge is simulation tools for RF-SiP design since there is no program capable of simulating a heterogeneous RF-SiP system. Characterization through measurements also remains a challenge. In summary there are still a lot of research gaps to fill.

The aim of this thesis is therefore to contribute to this research gap by investigating a broadband SiP concept for RF modules through electromagnetic simulations of transmission lines, material transition and signal leakage. This includes evaluating both the RF-SiP concept itself but also the MultiTech as a tool for future SiP simulations and design. The investigated simulation environment consists of signal transmission between four material levels inside the SiP: An evaluation board implemented as a Printed Circuit Board (PCB), micro-PCB (mPCB), interposer and RF-chiplets within the frequency range of 1–40 GHz. In this thesis, the evaluation board that enables future measurements of SiPs is fully developed from scratch compared with the other materials. Interposer and chiplets designs are implemented from existing Product Development Kits (PDK) in ADS. For the mPCB, the material stack-up and footprint were predefined by the manufacturer, but is manually recreated in ADS using provided documentation.

The thesis will also evaluate a novel Silicon Carbide (SiC) interposer technology currently under development, with the aim of assessing its potential for future SiP implementation. An interposer is a material used for integration and interconnection of passive RF components within a SiP. It is of high interest to integrate passive components using it, such as inductors and filters, since these components tend to become large when designing RF circuits. An interposer is cheaper to produce compared to a regular RF-chiplet, making it suitable for integrating components taking

up large area. To investigate this interposer, different inductor topologies will be investigated. In addition, microstrip filters in X-band (8-12 GHz) and Ku-band (12-18 GHz) are designed to further examine the RF characteristics and integration potential of the interposer. Flip-chip mounted RF-chiplets are also investigated in the SiP environment. All this together will create a toolbox for future SiP development.

2
Theory

In this section, the theoretical background of this report is presented. First, the concept of SiP, including the interposer and transmission line theory, is explained. This is followed by an explanation of the simulation and measurement techniques used in the thesis. Lastly, theory relevant to the passive components discussed in the report is presented.

2.1 System in Package Technology

An SiP solution for RF applications can be seen in Figure 2.1. It is a technique to combine integrate RF-chiplets often made of Gallium Nitride (GaN) or Gallium Arsenide (GaAs) with passive components placed on an interposer, into a single package [12]. This technique can also be applied to a single RF-chiplet or with Surface Mount Device (SMD) components. The package can then be placed onto a micro Printed Circuit Board (mPCB) that is placed onto a printed circuit board (PCB). The SiP itself is the mPCB together with the components integrated in it. Meanwhile, the PCB is an enabler to connect the SiP to other electronic components. There are a few ways to implement interconnections between RF-chiplets and the rest of the SiP. Two common ways to do it are either with bondwires or with flip-chip bonding [13].

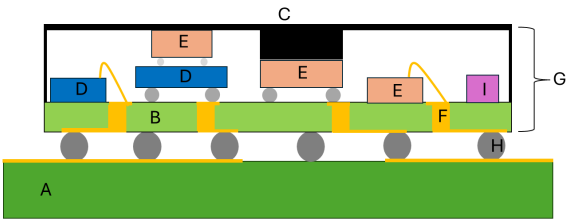


Figure 2.1: SiP solution for different types of components and mounting style. A is a PCB, B is a micro-PCB, C a cover including the big black box, D is an interposer, E is an RF-chiplet, F the signal path from components to PCB, G the package, H solder bumps, and I is an SMD component. Two wires from bondwire connections can be seen from both an interposer and an RF-chiplet. Flip-chip mounting can be seen for an RF-chiplet in two different ways, one placed on an interposer and one directly on an mPCB.

Flip-chip mounting makes it possible to stack components on top of each other. In order to make this possible the RF-chiplet needs to be flipped i.e. the bottom ground plane (GND) is placed against the cover of the package which can be seen for two RF-chiplets in Figure 2.1. This makes the cover act as GND but also a heat sink for the RF-chiplet. In a bond wire solution, the RF-chiplet is not flipped and the GND is facing down to the micro-PCB. The components can not be stacked on top of each other making it take up more space when multiple components need to be integrated [14]. Flip-chip mounting also has good electrical performance and costs less to produce than wire bonding [15]. These things make SiP with flip-chip mounting a highly interesting alternative to wire bonding.

In this thesis only flip-chip mounted RF-chiplets will be considered. The mounted components used to describe the SiP stack-up investigated in this thesis can be seen in Figure 2.2. In this figure both a solution where the RF-chiplet is placed on an interposer and directly onto the mPCB can be observed. These two different ways of implementation will be considered throughout this work.

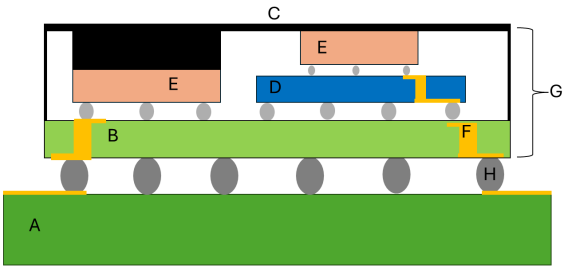


Figure 2.2: SiP solution for flip-chip mounted RF-chiplets. A is a PCB, B is a micro-PCB, C a cover including the big black box, D is an interposer, E is an RF-chiplet, F the signal path from components to PCB, G the package, and H is solder bumps.

2.2 Interposer Technology

An interposer is a material that has a core of dielectric media, usually made of silicon, glass, or an organic substrate [16]. On top of the dielectric material, multiple metal layers can be stacked. This enables signal transmission and placement of passive components such as inductors, resistors, and capacitors on the substrate. An overview of an arbitrary interposer stack-up can be seen in Figure 2.3. In this report, an novel interposer technology is used meaning it will be evaluated both in terms of capabilities but also implementation and usability within ADS. This interposer has four metal layers, in the following order: met1, met2, met3, and met4. The metal layers can be combined in multiple ways by removing or etching the insulating layer between them in the manufacturing process, thereby enabling thicker signal traces. However, due to the manufacturing process, there are design rules on which metal layers can be combined. These restrictions also dictate the width and height of the signal traces for the different layers. Since the conductor layers have various

material properties, they are associated with different conductivities and losses. Another technology available for the interposer is the so-called hot-via technique. It is a process where holes are made in the dielectric substrate, making it possible to transmit signals through the substrate. This is a key technology that makes it possible to stack flip-chip mounted components on top of the interposer [17]-[18]. Among other applications, it also enables the possibility of making so-called 3D inductors where the signal trace loops around the substrate, making it the core of the inductor [19].

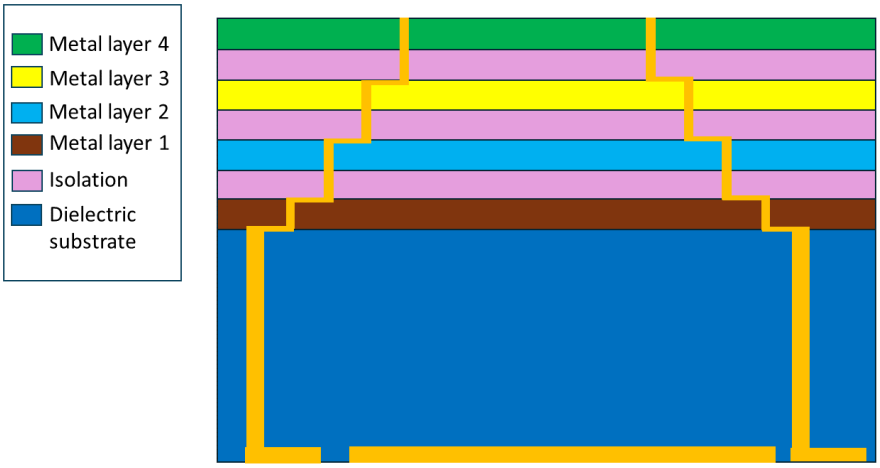


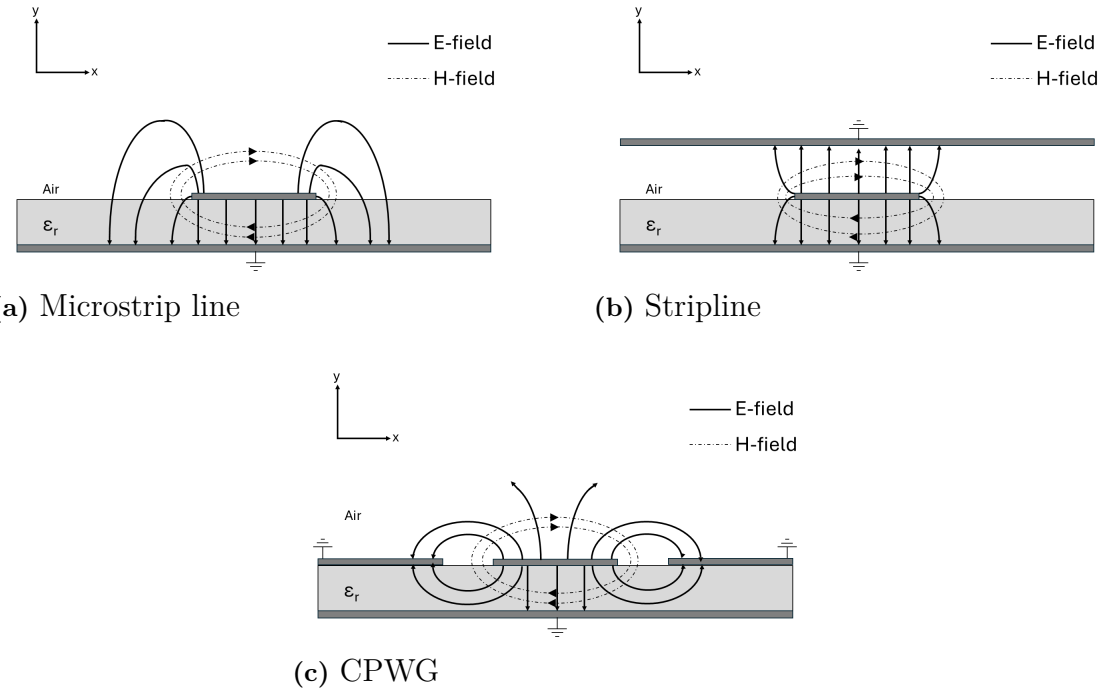
Figure 2.3: Stackup of interposer with the different metal layers, isolation layers and the dielectric substrate marked out. The isolation layers can be erased during manufacturing process making it possible to combine different metal layers into thicker traces. Gold colored parts are the signal path which include vias through the different layers, they also mark the bottom plane of the interposer that can be used as GND or for signal traces. The long vias throughout the dielectric substrate are the so-called hot vias.

2.2.1 Semiconductor Technology

A semiconductor substrate is the physical material on which electronic devices are fabricated. Common substrate materials for RF and microwave applications are silicon (Si), silicon carbide (SiC), and gallium arsenide (GaAs). Common semiconductor technologies used in RF-chiplet design are often based on gallium nitride (GaN) or gallium arsenide (GaAs). Depending on the application, GaN and GaAs technologies can be implemented on different semiconductor substrates. GaN has in general good power-handling capabilities, making GaN transistors commonly used in transceiver applications [20]. GaAs is also used in the same applications [21], but compared to GaN it has a lower operating voltage. It is also commonly used in low-noise amplifier (LNA) designs because of its low noise figure (NF) [22]. Active components integrated on a RF-chiplet are called integrated circuits (ICs), and if they are specifically designed for microwave and millimeter-wave applications, they are instead called monolithic microwave integrated circuits (MMICs). In this thesis, two fully developed PDKs, one GaN PDK and one GaAs PDK for MMIC development, are used to demonstrate SiP capabilities for these technologies.

2.2.2 Transmission Line Characteristics

In order to propagate a signal on either the interposer or RF-chiplet in a SiP, different types of transmission lines can be used. Common ones are microstrip lines, striplines, and coplanar waveguides (CPWG). The most commonly used transmission line for MMIC desing is microstrip since it is easy to implement in RF designs. A microstrip consists of a conducting trace with a GND plane underneath. A stripline is similar to a microstrip, but has an additional GND plane above its conductive strip. A CPWG has additional GND planes on the sides of the conducting trace. The field distribution for the electric field (E) and the magnetic field (H) can be seen in Figure 2.4.



(a) Microstrip line

(b) Stripline

(c) CPWG

Figure 2.4: Field distribution for the E and H field for three different types of transmission lines. Light grey is the substrate where dark grey conductors are placed.

The substrate on which the traces are placed has a specific relative permittivity ϵ_r. In the case where fringing effects are present, i.e. the E-field is spread across multiple substrates as in Figure 2.4, the effective permittivity ϵ_{eff} can be used instead. This is a conceptual value of the permittivity surrounding the trace, showcasing the complex electromagnetic environment for a case with different materials present. Since the fringing effect is dependent on what type of transmission line that is used, ϵ_{eff} varies between them. The frequency of the propagated wave also affects the fringing fields and, consequently, the ϵ_{eff} of the transmission line [23]. As a result, the properties of the transmission line become frequency dependent. The phase velocity v_p for a propagating wave on a transmission line can be calculated using the following equation

$$v_p = \frac{c_0}{\sqrt{\epsilon_{eff}}} \tag{2.1}$$

where c_0 is the speed of light in vacuum. The wavelength of the propagating wave λ_g is also affected by ϵ_{eff} governed by the following equation

$$\lambda_g = \frac{\lambda_0}{\sqrt{\epsilon_{eff}}} \tag{2.2}$$

where λ_0 is the wavelength in free space. Another effect that can degrade a signal is the coupling effect where two closely placed traces or conductors interfere with each other by picking up unwanted signal. If a microstrip trace is placed on a RF-chiplet that is flip-chip mounted onto another material, the electromagnetic properties change [24]. This placement of the filp-chip mounted RF-chiplet in SiP can be seen marked red in Figure 2.5.

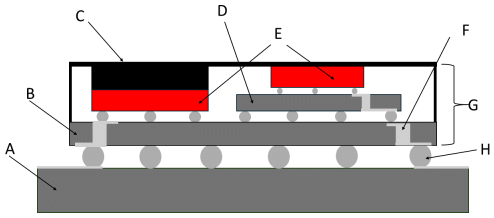


Figure 2.5: SiP solution for flip-chip mounted RF-chiplets marked in red. Since the microstrip lines are turned upside down the electromagnetic environment starts to resemble a stripline.

In that case, the microstrip assumption no longer holds. Instead, the microstrip line can be approximated as a stripline since a GND plane, either on the mPCB or on the interposer, is introduced above the trace. In that case, ϵ_{eff} changes, and with that, v_p and λ_g affect the electromagnetic environment of the signal trace.

2.3 Simulation in ADS

In this section the theory needed for simulations to characterize the electromagnetic environment for a SiP is presented. Keysight ADS is used in this report in order to perform simulations. The program supports two different electromagnetic field solvers (EM solvers): Momentum and finite element method (FEM) simulations.

2.3.1 Momentum simulations

Momentum simulation is an EM solver based on the Method of Moments (MoM) technique where the following equation is solved in order to simulate the structure

$$\iint dS'\, G(\mathbf{r}, \mathbf{r}') \cdot \mathbf{J}(\mathbf{r}') = \mathbf{E}(\mathbf{r}), \tag{2.3}$$

where $\mathbf{J}(\mathbf{r}')$ is the unknown surface current of the material, $\mathbf{E}(\mathbf{r})$ is the known excitation of the structure and $G(\mathbf{r}, \mathbf{r}')$ is the Green's dyadic function of the layer stack. By discretizing the surface using basis functions, the two following equations can be derived

$$L_{i,j} = \iint_S d\mathbf{S}\, \mathbf{B}_i(\mathbf{r}) \cdot \iint_{S'} d\mathbf{S}'\, G^A(\mathbf{r}, \mathbf{r}')\, \mathbf{B}_j(\mathbf{r}') \tag{2.4}$$

$$\frac{1}{C_{i,j}} = \iint_S dS\, \nabla \cdot \mathbf{B}_i(\mathbf{r}) \iint_{S'} dS'\, G^V(\mathbf{r}, \mathbf{r}')\, \nabla' \cdot \mathbf{B}_j(\mathbf{r}'). \tag{2.5}$$

In the equations $\mathbf{B} * i(\mathbf{r})$ is the point where the basis function is tested and $\mathbf{B} * j(\mathbf{r}')$ is the point influencing it. From equation 2.4-2.5 a model for each part of the mesh with capacitors to ground and inductors can be constructed [25]. The S-parameters of the structure can then be derived from the model.

2.3.2 Finite element method simulations

FEM simulations calculate the electromagnetic fields within the simulated structure. The FEM solver divides the structure into a mesh of tetrahedra and solves Maxwell's equations for each element

$$\nabla \times \left(\frac{1}{\mu_r} \nabla \times \mathbf{E}(x, y, z) \right) - k_0^2 \epsilon_r \mathbf{E}(x, y, z) = 0 \tag{2.6}$$

where μ_r is the complex relative permeability, ϵ_r is the complex relative permittivity, k_0 the free space phase constant and $\mathbf{E}(x, y, z)$ is a complex vector representing an oscillating electric field [26] . The program then finds an initial mesh depending on the FEM solver and the settings used. Then the so-called ΔS determines how fine this mesh becomes. ΔS is the difference of the S-parameters for each mesh segment after each iteration. After the mesh condition is satisfied, the solver starts to compute a solution for the structure.

In ADS it is possible to simulate different technologies at the same time using FEM. This technique is called MultiTech and gives the ability to simulate, for example an RF-chiplet flip-chip mounted on a mPCB. For a SiP solution this means that the different materials included can be designed individually, then be put together and simulated. In figure 2.6 all the different materials and transitions that can be simulated using this technique are shown marked in red.

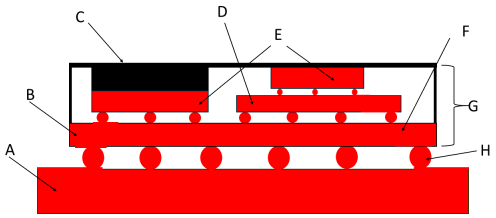


Figure 2.6: SiP solution for materials and transitions simulated using MultiTech marked in red.

2.4 S-parameters of a Two Port Device

By performing simulations the S-parameters for a device can be obtained. An arbitrary two-port device can be seen in Figure 2.7.

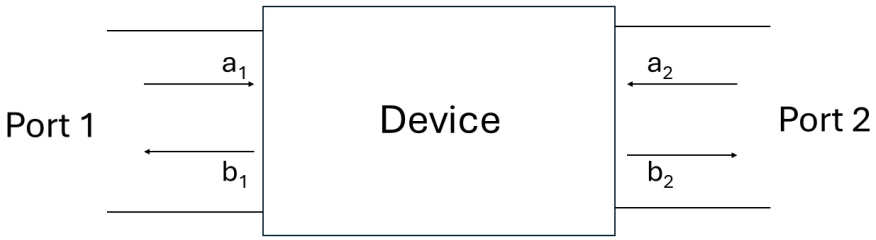


Figure 2.7: An arbitrary two-port device. a_1 is the incident wave on port 1, a_2 is the incident wave on port 2, b_1 is the reflected wave on port 1 and b_2 is the reflected wave on port 2.

From this setup, the S-parameters can be derived from the incident and the reflected waves of the two-port. The scattering matrix can then be written as

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.7}$$

where S_{11} is the input reflection coefficient at port 1, S_{22} is the input reflection coefficient at port 2, S_{21} is the forward transmission coefficient from port 1 to port 2 and S_{12} is the reverse transmission coefficient from port 2 to port 1. The S-parameters are defined by the following equations

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \tag{2.8}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{2.9}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{2.10}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.11}$$

where it's assumed that the impedance at port 1 Z_1 is perfectly matched to the impedance at port 2 Z_2. From the obtained S-parameters the impedance of the two-port device can be calculated using the following equations

$$Z_{11} = Z_0 \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \tag{2.12}$$

$$Z_{21} = Z_0 \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \tag{2.13}$$

$$Z_{12} = Z_0 \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \tag{2.14}$$

$$Z_{22} = Z_0 \frac{(1+S_{22})(1-S_{11}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}. \tag{2.15}$$

In these equations it is also assumed that the impedance Z_1 is equal to Z_2 . The admittance Y can be calculated and obtained in a similar way. The inductance L, the capacitance C and the quality factor Q of a simulated device, such as the one in Figure 2.7 can then be obtained using the following equations

$$C = \frac{\mathrm{Im}(Y)}{\omega} \tag{2.16}$$

$$L = \frac{\mathrm{Im}(Z)}{\omega}. \tag{2.17}$$

$$Q = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \tag{2.18}$$

2.5 Calibration for measurement of a SiP using Transmission, Reflection and Line kit

To obtain S-parameters and characterize a physical RF-SiP, a vector network analyzer (VNA) is commonly used for measurements. The measurement setup can be realized by placing the SiP on a PCB evaluation board and connecting the VNA to the ports of the PCB. In order to perform adequate measurements, the reference plane at which the measurements are conducted needs to be shifted from the PCB ports to the SiP ports. The different reference planes can be seen in Figure 2.8

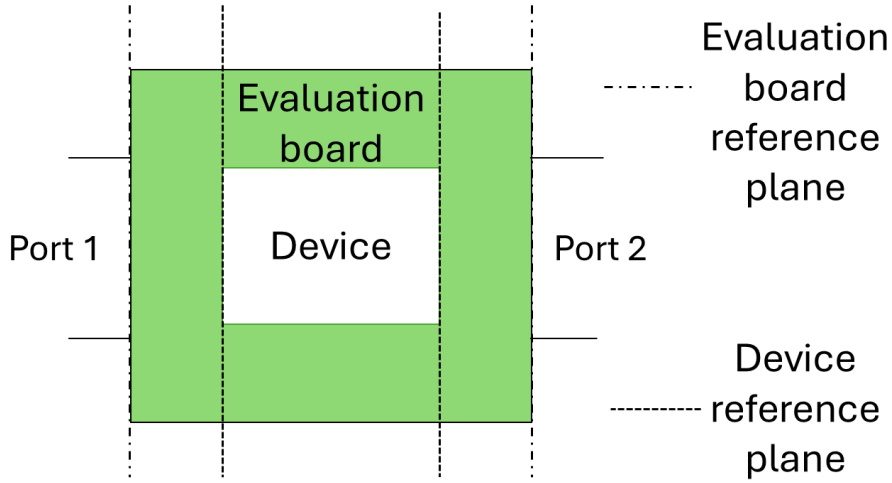


Figure 2.8: Reference planes for measurements of a two-port device. With a calibration kit, the reference plane can be shifted from the evaluation board ports to the device ports.

The shift in the reference plane can be done using multiple techniques [27], [28]. A common one is the so-called Thru-Reflect-Line (TRL) calibration that consists of a through line (T_{TRL}), an open or short-circuited stub (R_{TRL}), and a long transmission line (L_{TRL}) [29]. L_{TRL} should have an extra length of transmission line that gives the signal an additional phase shift of that meets the requirement $20° < \Delta\phi < 160°$ compared to the signal phase of the T_{TRL} line. This gives a frequency range ratio of 8:1 for a line [30], [31], meaning that if a signal has $\Delta\phi = 20°$ at 1 GHz, the highest frequency that the L_{TRL} segment can cover is 8 GHz. If the TRL kit should work for a large frequency range, multiple L_{TRL} components can be added in order to cover multiple frequencies.

2.6 Inductors

Inductors are electrical components designed to store energy in a magnetic field. When current flows through a conductor a magnetic field is generated around the conductor. If the current varies with time, the resulting changing magnetic field induces a voltage in the conductor according to Faraday's law. This self inducted voltage opposes the change in current, in accordance with Lenz's law. This is governed by the inductor equation

$$v(t) = L\frac{di(t)}{dt} \tag{2.19}$$

where L is the inductance in Henry (H) for the structure. Different inductor topologies can be used depending on the application. For MMIC design the planar inductor is a crucial component [32]. It can have different shapes such as circular, octagonal or square. A simple structure of an arbitrary square inductor can be seen in figure 2.9.

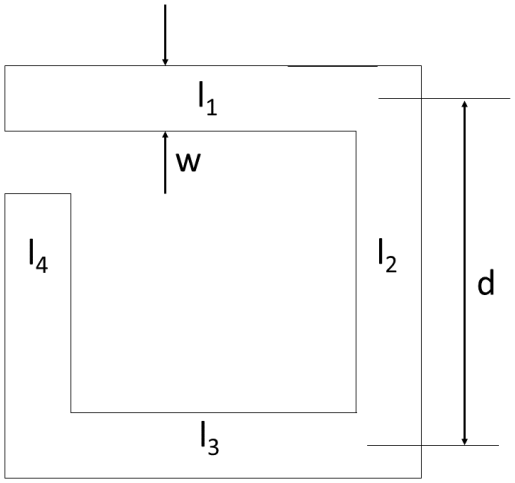


Figure 2.9: Figure of an arbitrary four-segment square planar inductor where l_1-l_4 are the lengths of the different segments, w is the width of the conductor and d is the distance between the centers of two segments.

With multiple inductor segments, such as in 2.9 both the self inductance and the mutual inductance need to be taken into account to get the total L_{tot} of an inductor. The mutual inductance is the effect that one section has on another in terms of inductance, contributing to the total inductance. The total inductance of a planar inductor can be calculated using the following equations [33]. The self-inductance for one segment, L_i, can be calculated using

$$L_i = 0.002 l_i \left[\ln\left(\frac{2l_i}{\mathrm{GMD}}\right) - 1.25 + \frac{\mathrm{AMD}}{l_i} + \frac{\mu}{4} T \right] \tag{2.20}$$

where l_1 is the length of the segment, GMD is the geometric mean distance of the conductor cross section, AMD is the arithmetic mean distance of the conductor cross section, μ is the conductor permeability and T is a frequency-correction value. Assuming a thin conductor and high operating frequency f, T can be assumed to be 1. With a rectangular conductor cross section equation 2.20 can be approximated as

$$L_i = 0.002 l_i \left[\ln\left(\frac{2l_i}{\mathrm{a+b}}\right) + 0.25049 + \frac{\mathrm{a+b}}{3l_i} + \frac{\mu}{4} \right]. \tag{2.21}$$

where a and b are the height and width of the cross section. For two parallel conductors i and j with the same current direction, the mutual inductance $M_{i,j}$ has a positive M_+ contribution to the total inductance. With opposite current directions it contributes negatively with M_- to the total inductance. In figure 2.9 there is only a negative contribution to the total inductance since parallel segments has opposite current direction. $M_{i,j}$ can be calculated using the following equation

$$M_{i,j} = 2l_1 K \tag{2.22}$$

where K is the mutual inductance parameter calculated using the equation

$$K = \ln\left\{\frac{l_1}{\mathrm{GMD}} + \sqrt{1+\left(\frac{l_1}{\mathrm{GMD}}\right)^2} - \sqrt{1+\left(\frac{\mathrm{GMD}^2}{l_1}\right)^2} + \frac{\mathrm{GMD}}{l_1}\right\}. \tag{2.23}$$

To simplify equation 2.23 GMD can be approximated as the distance d between the centers of two segments. This calculation of $M_{i,j}$ is only valid when the segments are equally long. Knowing the contribution of all self and mutual inductances the total inductance L_{tot} can be calculated using the following equation

$$L_{tot} = \sum_{i=1}^{N} L_i + \sum_{i=1}^{N}\sum_{\substack{j=1 \\ j\neq i}}^{N} M_{i,j} \tag{2.24}$$

where N is the number of segments in the inductor.

2.6.1 3D-inductor using hot via technique

The hot-via technique included in the interposer makes it possible to construct a 3D inductor [34] which can be seen in Figure 2.10.

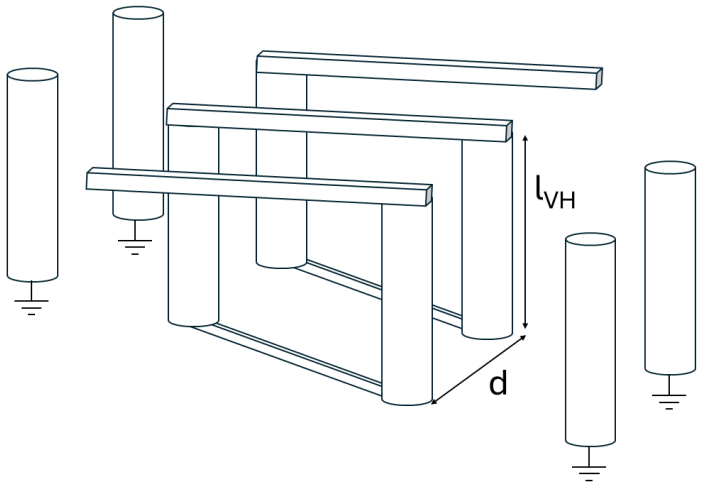


Figure 2.10: An arbitrary 3D-inductor using the hot-via technique. The inductor can be seen in the middle with via height l_{VH} and distance d between the vias. Ground vias are placed around it to shield the structure.

The total inductance of the rectangular part of the 3D inductor can be calculated using equation 2.20-2.24 and the self inductance L_{VH_i} and the mutual inductance $M_{VH_{i,j}}$ for the hot vias can be calculated using the following equations [35], [36]

$$L_{VH_i} = \frac{\mu}{2\pi} l_{\mathrm{VH}_i} \ln\left(\frac{l_{\mathrm{VH}_i} + \sqrt{l_{\mathrm{VH}_i}^2 + r^2}}{r}\right) + 0.25 - \sqrt{1+\left(\frac{r}{l_{\mathrm{VH}_i}}\right)^2} + \frac{r}{l_{\mathrm{VH}_i}} \tag{2.25}$$

$$M_{VH_{i,j}} = \frac{\mu}{2\pi} l_{\mathrm{VH}_i} \left(\ln\left(\frac{l_{\mathrm{VH}_i} + \sqrt{l_{\mathrm{VH}_i}^2 + d^2}}{d}\right) - \sqrt{1+\left(\frac{d}{l_{\mathrm{VH}_i}}\right)^2} + \frac{d}{l_{\mathrm{VH}_i}}\right) \tag{2.26}$$

where d is the center distance between two vias, l_{VH_i} is the height of a via and r is the radius. In order to get the total inductance of the inductor, the self inductance and the mutual inductance contributions from both the rectangular traces and hot-vias is added together using equation 2.24. Ground vias are placed around the structure in order to minimize coupling to other components [37]. In order to maximize the inductance of the inductor the GND vias should be placed far away from the inductor to minimize coupling between them [35].

2.6.2 Q-value

Another important metric for characterizing inductors and other structures such as filters is the Q-value. It is defined by the following equation

$$Q = 2\pi f \frac{\text{Energy stored}}{\text{Energy dissipated per cycle}} \tag{2.27}$$

where f is the operating frequency. It is a measure of how well a structure can store energy. Since the equation takes dissipated energy into account can it also be seen as a metric of a structures losses. For a resonant component placed on a substrate the total Q can be divided into three different parts [23], [38] using the equation

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_r} \tag{2.28}$$

where Q_c is the Q-value associated with the conductor material, Q_d is associated with the dielectric media and Q_r is associated with the radiation from a component. Q_c can be calculated using the following equation

$$Q_c = \frac{\pi}{\alpha_c \lambda_g} \tag{2.29}$$

where α_c is the conductor attenuation in nepers per unit length i.e. a measure of how fast a signal attenuates and λ_g is the guided wavelength in meters. Q_d can be calculated using the following equation

$$Q_d \geq \frac{\epsilon'}{\epsilon''} = \frac{1}{\tan(\delta)} \tag{2.30}$$

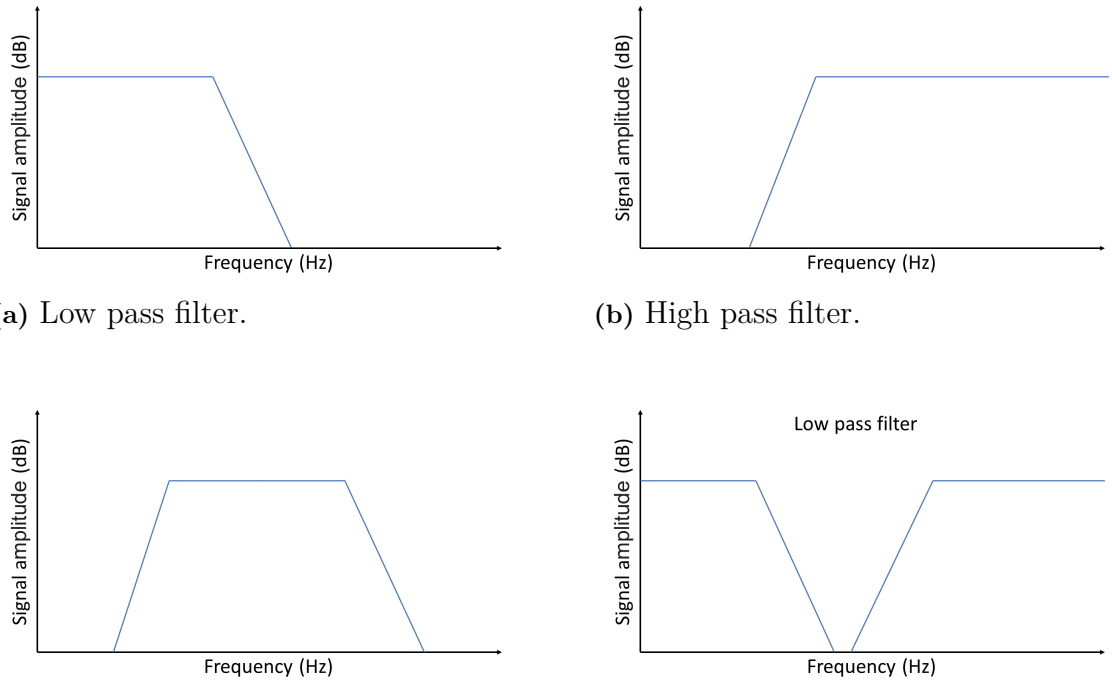
where ϵ' is the lossless real part of ϵ and ϵ'' is the complex part which accounts for the losses of the substrate. δ is the angle between these two parts. The metric $\tan(\delta)$ is usually given as a loss parameter for substrates, it is frequency dependent and increases with higher frequencies. Q_r can be defined as

$$Q_r = \omega \frac{\text{Time-average energy stored in resonator}}{\text{Average power radiated}}. \tag{2.31}$$

When the Q-value is obtained for a component, for example an inductor the unloaded Q_U is obtained. If it is extracted for a inductor placed in a system the loaded Q-value Q_L is obtained instead [23]. A higher value of Q corresponds to an increased ability to select a narrow band of frequencies.

2.7 Filter Design

There are four main types of filters: low-pass, high-pass, band-pass and band-stop [38], [23]. Figure 2.11 illustrates the general characteristics of these filters.



(a) Low pass filter.

(b) High pass filter.

(c) Band pass filter.

(d) Band stop filter.

Figure 2.11: Characteristics for different filters.

To construct these types of filters different approximations can be used. One commonly used approximation is the Chebyshev filter. It is based on Chebyshev polynomials and has the following transfer function

$$|S_{21}(j\omega)|^2 = \frac{1}{1 + \epsilon^2 T_n^2\left(\frac{\omega}{\omega_0}\right)} \tag{2.32}$$

where ϵ is the ripple factor that determines the passband ripple of the filter, $T_n(\frac{\omega}{\omega_0})$ is the Chebyshev polynomial of degree n, ω the angular frequency and ω_0 the angular cutoff frequency. Two key metrics when designing filters is the so-called insertion loss (IL) which is the loss added to the signal by the filter structure itself and the returnloss (RL) which is the loss due to the reflected wave. IL can be calculated using the following equation

$$IL = -20\log_{10}|S_{21}| \tag{2.33}$$

where S_{21} is the forward transmission coefficient of the filter. RL can be calculated using the following equation

$$RL = -20\log_{10}|S_{11}| \tag{2.34}$$

where S_{11} is the reflection coefficient of the filter. In order to realize a filter either microstrip lines or lumped components can be used. Lumped components are generally more compact and simpler to implement, but suffer from parasitic effects at higher frequencies. Microstrip lines generally provide better high-frequency performance and higher Q [38]. To realize a microstrip filter different topologies can be used depending on design and requirements. A component related to a filter is a resonator. They have the same fundamental function but a resonator selects a small band of frequencies compared to a filter that generally selects a broader frequency range. Resonators can have different resonance conditions depending on the structure used. For a microstrip resonator, consisting of a single piece of trace, the physical length l_{res} of the trace either needs to be equal to $\lambda_g/2$ or $\lambda_g/4$.

3
Design and Simulation Process

This section presents the design and simulation process carried out for the thesis. The work focused on establishing a toolbox to support future SiP development and evaluation. As part of this process, electromagnetic characterization was performed through simulations and design of electrical components. Instead of representing isolated developments, the tools and design elements presented in this work form a toolbox to support future design and simulation for SiP solutions. Within the scope of this work, a literature review was conducted. It consisted of finding material about current SiP technologies and what has previously been done in the field. A special focus was placed on interposer technology and passive components integrated into the interposer material.

After the literature review, an evaluation board for future SiP measurements was designed as part of the toolbox developed in this work. Then, a simulation environment was developed in ADS using MultiTech to enable evaluation of signal propagation in materials and structures relevant to SiP designs. Different passive structures were evaluated to assess design possibilities and establish building blocks for SiP implementations. Inductors and filters were designed and evaluated on the interposer. Already existing resonators and filters was simulated in the developed MultiTech environment to see the effect of flip-chip mounting within a SiP.

3.1 Evaluation Board Design

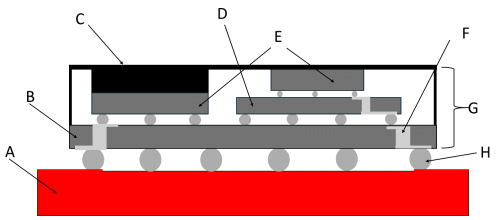


Figure 3.1: SiP solution where the evaluation board, A, is marked in red.

As a part of this work, an evaluation board was developed to provide a platform for mounting and physically evaluating future SiP packages. The objective of the design was to create an interface capable of supporting future testing and thereby

characterize the electromagnetic environment of a SiP through measurements. The footprint for the mPCB was predetermined, and from that a two-layer test card was designed. First, the substrate of the PCB was chosen to be I-Tera MT40. It was selected for its low $\tan(\delta)$ compared to more common materials such as FR4. Initial simulations were performed using the LineCalc tool in ADS for two different substrate heights and two different conductor heights provided by the manufacturer. From this, the thinnest substrate height and conductor height were selected in order to minimize the trace width. The trace was then simulated using the MoM EM solver with standard settings in ADS to confirm the trace width. The simulations were conducted with a stackup in ADS where the conductor layers were embedded in a solder mask to replicate realistic conditions.

To fit all the traces needed on the evaluation board, they were placed on the bottom side. Hence, vias were used to access the bottom layer from the top layer where the SiP mounting pads were placed. Vias with different diameters and distances to the ground plane were simulated in order to find the best option to minimize signal degradation through transitions between layers. It was found that as small a diameter, within the design rule of the PCB, as possible together with a short distance to the GND plane gave the best performance. After the traces were simulated, the final layout of the evaluation board was realized. This can be seen in Figure 3.2.

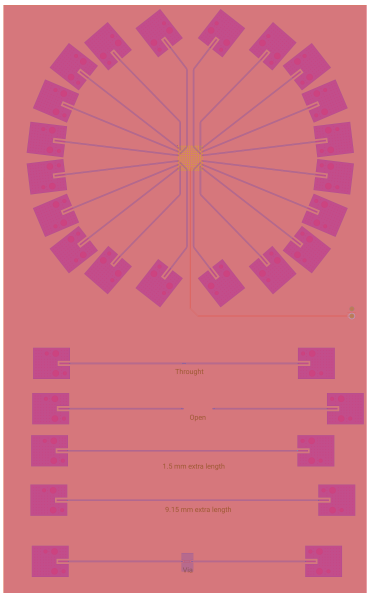
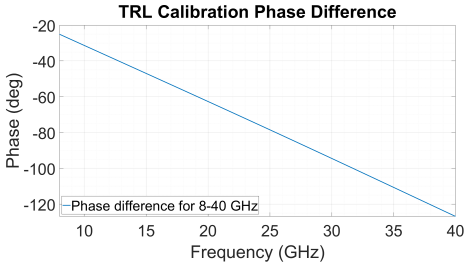


Figure 3.2: Final two-layer evaluation board with signal ports and a TRL kit included on the bottom of the board. The purple squares are the pads for the SMA connectors. The yellow dots in the middle are the pads for the SiP.

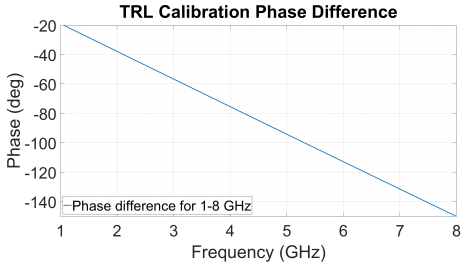
To ensure signal integrity on the board, several layout considerations were included. The traces were drawn straight to the extent it was possible in order to avoid discontinuities. All the traces were set to the same electrical length to minimize the phase shift of the signal. The coupling effect between the two closest traces was also investigated by simulation to exclude any impact on the signal. The footprint for the SMA connectors used in the design was manually drawn on the card.

3.1.1 TRL Calibration Kit Design

After the design of the test card had been confirmed, a TRL kit was constructed. It was done by placing a through line equal to twice the electrical length of one trace with a port on each side. The open line was implemented similarly but with a gap between the two traces. In order to cover the desired frequency range of 1–40 GHz, two different lengths of the calibration line, L_{TRL}, were implemented. One covered the range 1–8 GHz and the other 8–40 GHz. The lengths were found using the LineCalc tool in ADS, where the additional electrical length at the lower frequency in both cases was larger than 20° and smaller than 160° at the upper frequency limit. These values was then confirmed with simulations which can be seen in Figure 3.3.



(a) Phase difference relative to the through line of the TRL kit for the added transmission line over the 8–40 GHz frequency range.



(b) Phase difference relative to the through line of the TRL kit for the added transmission line over the 1–8 GHz frequency range.

Figure 3.3: Phase difference for the two different line segments included on the evaluation board.

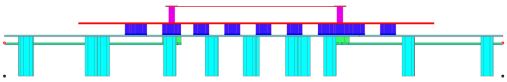
3.2 Evaluation of MultiTech Simulations

As part of the toolbox developed in this work, the MultiTech simulation technique was evaluated for its capabilities to perform simulations for SiP solutions. First, a brief explanation of how it works is given. This is followed by an investigation of the effects of different simulation settings.

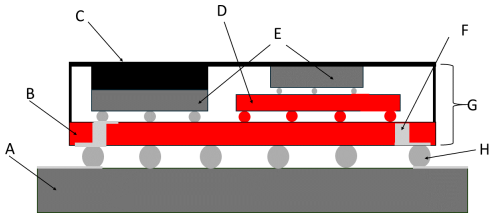
3.2.1 Setup for MultiTech Simulations in ADS

The following setup shows how a MultiTech simulation environment was constructed in ADS. The transition between the mPCB and the interposer is used as an example to demonstrate the simulation workflow. The setup was created using a new workspace in ADS with a substrate stackup where libraries from different workspaces could be imported. For example, when simulating the transition between the mPCB and the interposer, the substrate of the mPCB was used in the workspace. Separate workspaces were then created for the interposer and the solder bumps between the mPCB and the interposer. The designs of the interposer and solder bumps were imported into a layout in the mPCB workspace. The Smart Mount Instance Editor was used to define the mounting layers and stacking order of the different designs. Signal traces, additional components, and ports were then added for the mPCB. The

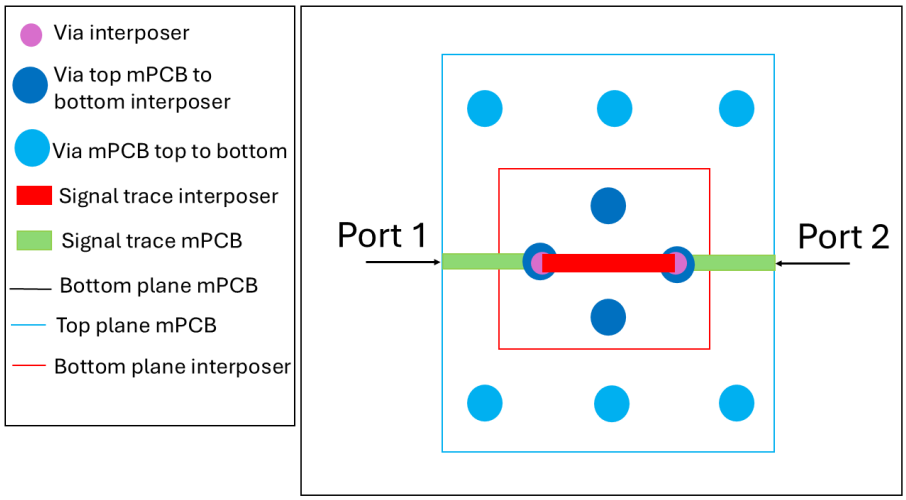
final design was opened in ADS RFPro, where the simulations were conducted using the signal layer on the mPCB to place the ports. An example of the assembled structure and the simulation interface can be seen in Figure 3.4. The simulation setup that can be seen in Figure 3.4c uses the bottom plane of the mPCB as the GND for the whole simulation. The ports connected to the signal trace is transmission line (TML) ports. Vias not connected to the signal traces act as GND vias. This simulation setup is used for all the MultiTech simulations but with different materials depending on whats being evaluated.



(a) Side view of a simulation stack-up in RFPro.



(b) Simulation interface for evaluating MultiTech for SiP simulations, marked in red. B is the mPCB, D is the interposer and H is the solder bumps.



(c) Top view of the MultiTech simulation setup.

Figure 3.4: Simulated structure seen from the side beside the simulation interface for a SiP for evaluation of MultiTech simulations. Light blue is the interposer, dark blue represents the solder bumps and red and pink components represent the interposer. The bottom Figure shows the simulation setup from above.

3.2.2 Initial Simulation Settings in ADS

The initial simulation settings used for FEM simulations in ADS RFPro can be seen in Table 3.1. These settings correspond to commonly used simulation settings

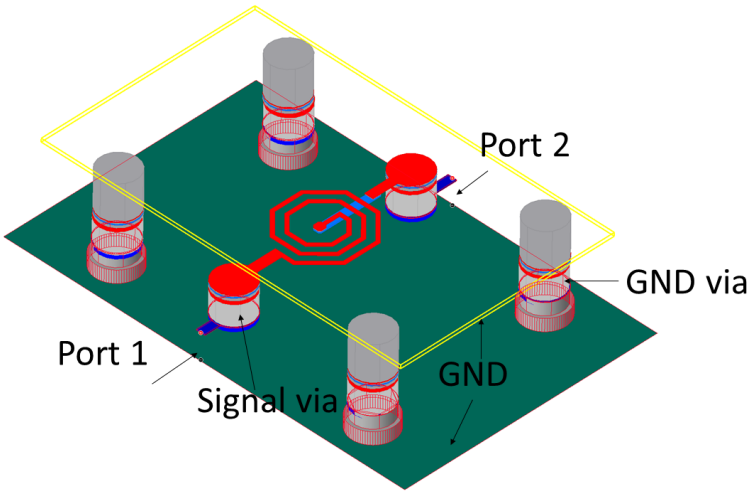
in RFPro and most of the settings were set to automatic, allowing the program to determine the settings based on the simulated structure. The refinement frequency was set to the maximum frequency in order to generate a mesh suitable for all simulated frequencies. ΔS (delta error) provided a good trade-off between simulation time and accuracy. These settings were used as the starting point for evaluating different simulation settings.

Table 3.1: FEM simulation settings in ADS RFPro. The initial mesh settings determine the initial mesh of the structure and the adaptive refinement settings control the simulation accuracy.

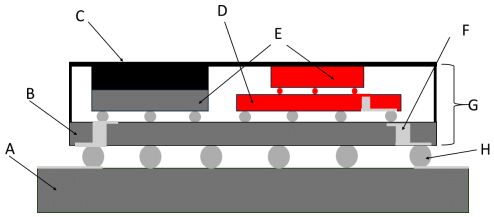
Category	**Setting**	**Value**
Solver	Matrix solver	Automatic
	Discretization Order	2nd Order
	Port solver	Automatic
Initial Mesh	Generation	Automatic
	Mesh Domain Optimization	Off
	Target Mesh Size	Automatic
	Conductor Edge Mesh Level	Off
	Minimum Mesh Size	Off
Adaptive Refinement	Delta Error	0.02
	Consecutive Passes of Delta Error	1
	Minimum Number of Adaptations	1
	Maximum Number of Adaptations	15
	Refinement Frequency	Maximum Frequency
Physical Model	Thick conductor model	Automatic
	Via conductor model	Automatic
Preprocessor	Healing snap distance	Automatic
	Simplify layout	On
	Ignore conductor shapes	Automatic
	Ignore conductor holes	Automatic

3.2.3 Evaluation of Simulation settings for MultiTech

Different simulation settings were tested for the MultiTech simulations in order to evaluate their impact on simulation time, memory usage, and S-parameter results compared with the initial settings in ADS RFPro. The investigated settings included various mesh configurations and adaptive refinement settings. To evaluate them, a test structure consisting of an octagonal inductor flip-chip mounted onto a GaAs material was simulated. This setup, together with its placement inside the SiP, can be seen in Figure 3.5. In Figure 3.5a, the solid green rectangle and the yellow frame represent the GND planes. The yellow frame is a solid metal plane but has been made transparent for visualization purposes. Ports 1 and 2 belong to the GaAs PDK, while the inductor belongs to the interposer. Together with the signal via connecting the signal path, these components are located between the two ground planes and therefore do not make contact with the GND planes. TML ports are used in the simulation. The GND vias include both the vias in the two different materials and the solder bumps connecting them.



(a) Simulation stackup for MultiTech simulations of inductors seen from above.



(b) Simulation interface shown in red for the SiP. D is the interposer, E is the RF-chiplet, F is the signal traces and H is the solder bumps.

Figure 3.5: Simulation structure and interface for evaluation of MultiTech simulation settings.

It was found that by choosing a minimum mesh size close to the thinnest layer of the simulated structure, a significant impact on both simulation time and memory usage was observed while only having a negligible impact on the simulated S-parameter results. Based on these observations, the modified mesh settings were used for the MultiTech simulations in this thesis. The S-parameter results obtained from this setup can be seen in Figure 3.6.

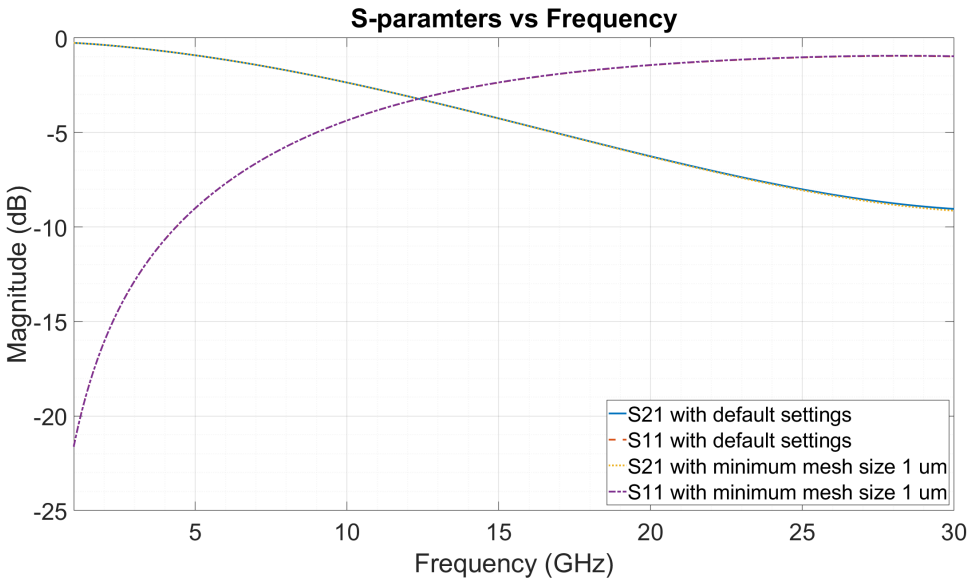


Figure 3.6: Comparison between initial settings and minimum mesh size of 1 μm for FEM simulation in RFPro.

From Figure 3.6, no differences in the S-parameters could be distinguished. A comparison between the default settings and using a minimum mesh size of 1 μm regarding key simulation metrics can be seen in Table 3.2. It can be seen that simulation time and memory usage decreased with a smaller minimum mesh size. The same can be seen for the number of mesh cells but the number of adaptive passes was increased. Hence, it is important to choose the right settings when using MultiTech in order to minimize the resources needed when performing simulations.

Table 3.2: Comparison of simulation performance with the initial simulation settings and with a minimum mesh size of 1 μm.

Metric	**Initial**	**Min mesh 1 μm**
Total Simulation Time [min]	308	44
Peak Memory Usage [GB]	85.5	53
Number of Adaptive Passes	5	6
Final ΔS	0.0194	0.0130
Number of Mesh Cells	1166568	855382

3.3 Modeling of SiP Transitions

As part of the toolbox developed in this work, the transitions between the different materials: PCB, mPCB, interposer and RF-chiplet, within the SiP were simulated in order to characterize the electromagnetic behavior of the transitions. This was done using MultiTech simulations in ADS.

3.3.1 Simulation of Transitions between Materials

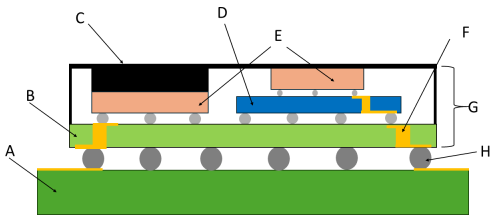


Figure 3.7: The SiP solution evaluated in this thesis. A is the PCB evaluation board, B is the mPCB, D is the interposer, E is the RF-chiplet and H is the solder bumps.

To simulate the transitions within the SiP, the substrate stackups for the materials of interest: PCB, micro-PCB, interposer, and RF-chiplet, were built in ADS. For the interposer and RF-chiplet, the given Process Design Kits (PDKs) had predefined material stacks. They only had to be modified to be compatible with MultiTech simulations. The stackups for the PCB and mPCB were built according to the data provided by the manufacturers. For the mPCB, the layout was already provided and had to be reconstructed in ADS from provided design files and documentation. As an example of a substrate stackup, the stackup for the evaluation board can be seen in Figure 3.8. The material stackup for the mPCB was implemented in a similar way as the PCB, but with a different substrate material, height, and four metal layers where the second layer was used as the signal layer. Solder bumps between the different materials were also implemented manually according to manufacturing data. This stackup can be seen in Figure 3.9.

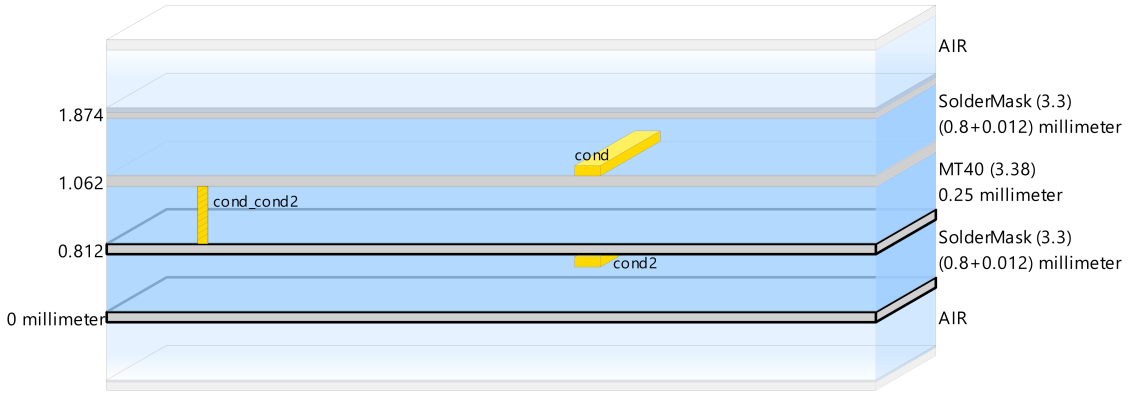


Figure 3.8: Material stackup for the evaluation board with two metal layers, cond and cond2, and one via connection, condcond2. The materials and solder mask together with their hight and relative permittivity can be seen in the stackup.

Figure 3.9: Material stackup for the mPCB board with four metal layers layers, Signaltop, SignalL2, SignalL3 and Signalbottom. Three via connections is also included ViatopL2, ViaL2L3 and ViaL3bottom. The materials and solder mask together with their hight and relative permittivity can be seen in the stackup.

3.3.2 Transmission Line Simulation

To build the simulation environment of the SiP from scratch, 50 Ω transmission lines for the PCB, mPCB, interposer, and GaN RF-chiplet were simulated with the aim of minimizing S_{11} and maximizing S_{21}. The simulation setup for the materials was designed to replicate real conditions when implemented within a SiP. The simulation interface for the different materials can be seen in Figure 3.10.

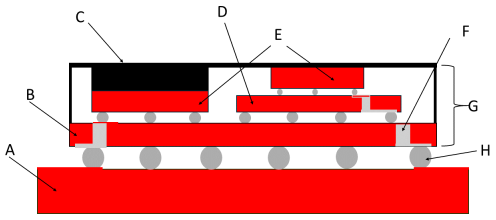


Figure 3.10: The SiP solution evaluated with the transmission line placement marked in red. A is the PCB evaluation board, B is the mPCB, D is the interposer and E is the RF-chiplet.

To replicate real conditions for transmission lines in the SiP a microstrip line on top of a GND plane was simulated for the PCB, interposer and chip with TML ports and the end of the line. Transmission lines on the micro-PCB instead had the characteristics of a CPWG with GND planes above and below the signal trace located at the SignalL2 layer. TML ports was also used for this simulation. The lines were simulated individually, and from this the S-parameters were obtained. In Figure 3.11, S_{11} for the different transmission lines can be observed.

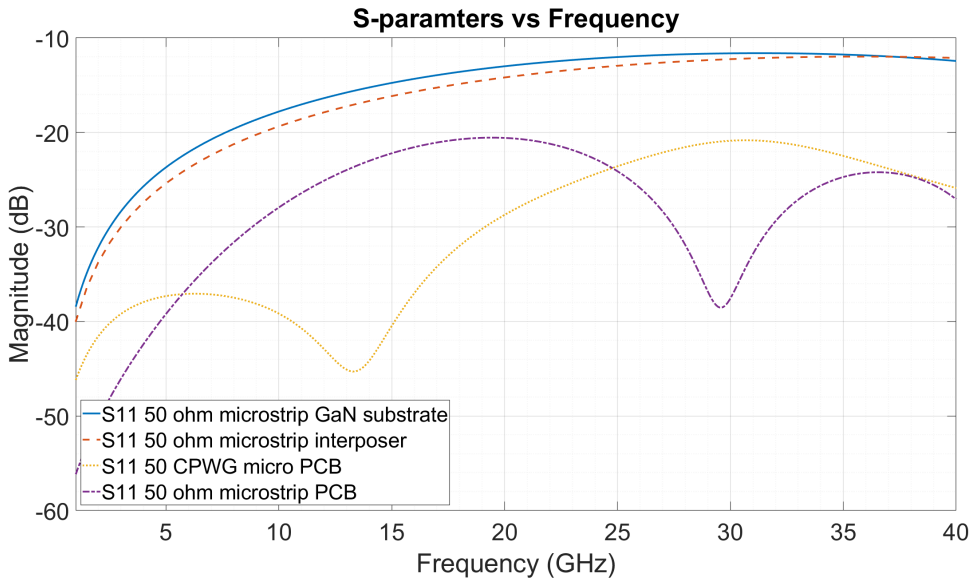


Figure 3.11: S_{11} for a 50 Ω line for the PCB, mPCB, interposer, and GaN RF-chiplet. All the simulated traces were equally long.

S_{21} for the transmission lines can be observed in Figure 3.12. From both figures, it can be seen that the transmission lines for the different material implementations show good impedance matching to an external 50 Ω system both in terms of reflection coefficient and transmission losses.

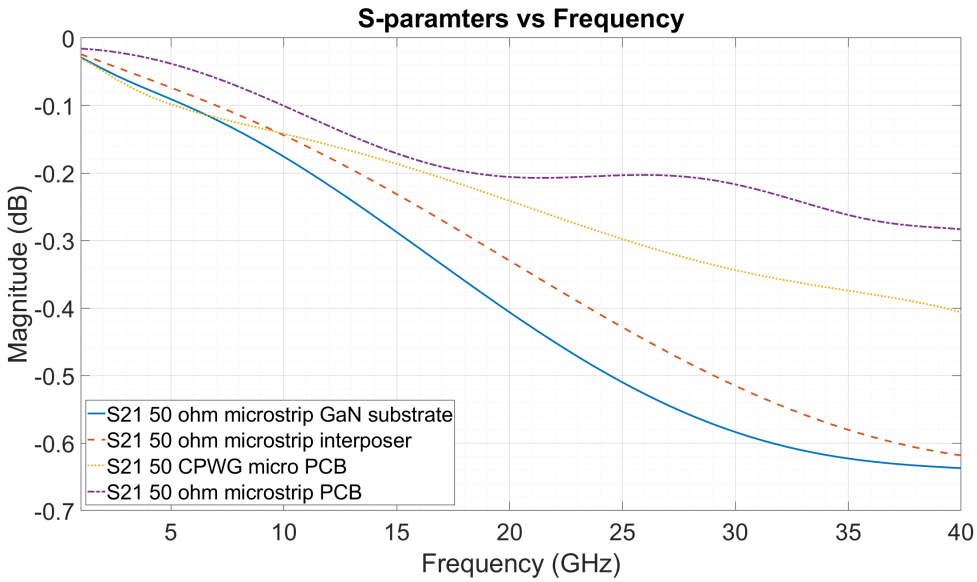
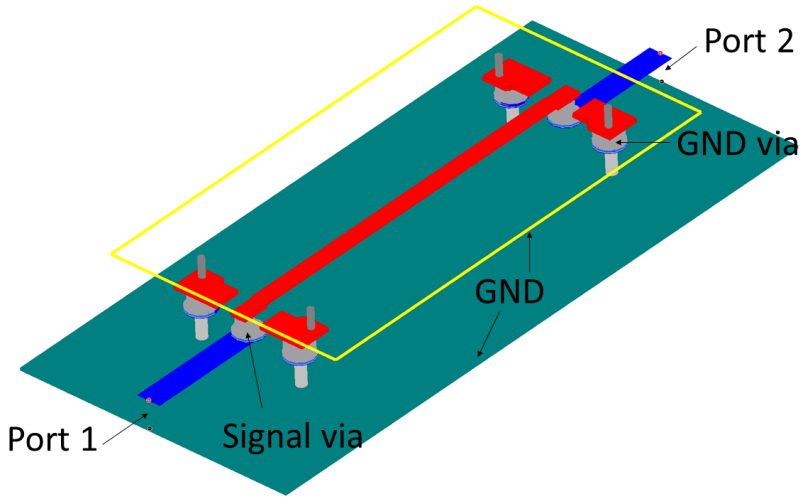


Figure 3.12: S_{21} for a 50 Ω line for the PCB, mPCB, interposer, and GaN RF-chiplet. All the simulated traces were equally long.

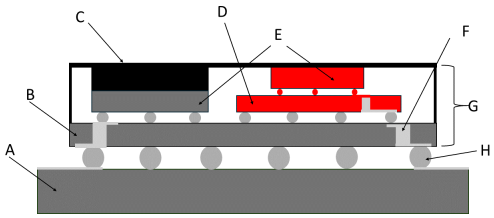
3.3.3 RF-chiplet to Interposer Transition

In order to characterize the SiP further, the transition between the interposer and the GaN RF-chiplet were simulated. A 50 Ω line was drawn in the GaN workspace

with added Ground-Signal-Ground (GSG) connections at each end of the line. A large solid metal plane was added under the microstrip as a GND plane together with grounding vias. Solder bumps with a height matching manufacturing conditions were then added to the layout. The designs were flip-chip mounted on transmission lines of the interposer workspace. This setup together with the simulation interface can be seen in Figure 3.13. The blue lines in Figure 3.13a is the microstrip line on the interposer and the red is placed on the RF-chiplet. Both the yellow frame and the green rectangel is GND planes connected with GND vias. Since the RF-chiplet is flip-chip mounted on the is the yellow frame placed above the red microstrip line.



(a) Simulation stackup for RF-chiplet to interposer in RFPro.



(b) Simulation interface shown in red inside the SiP. D is the interposer, E is the RF-chiplet and H is the solder bumps.

Figure 3.13: The simulated structure next to the simulation interface within a SiP, shown in red.

In order to simplify the MultiTech simulations and decrease the simulation time, simplified models for the solder bumps were used for the simulations carried out in MultiTech. Instead of spherical-shaped solder bumps, cylindrical bumps were used. The size of the simulated dielectric box was also decreased to reduce the area that needed to be meshed in order to perform the simulations. The structure was simulated, and S-parameters were extracted in RFPro to evaluate the transmission and reflection performance of the structure. The S-parameters of the transition

between the interposer and the GaN RF-chiplet can be seen in Figure 3.14. It can be seen that the transition provides good signal transmission with low reflection across the entire frequency range.

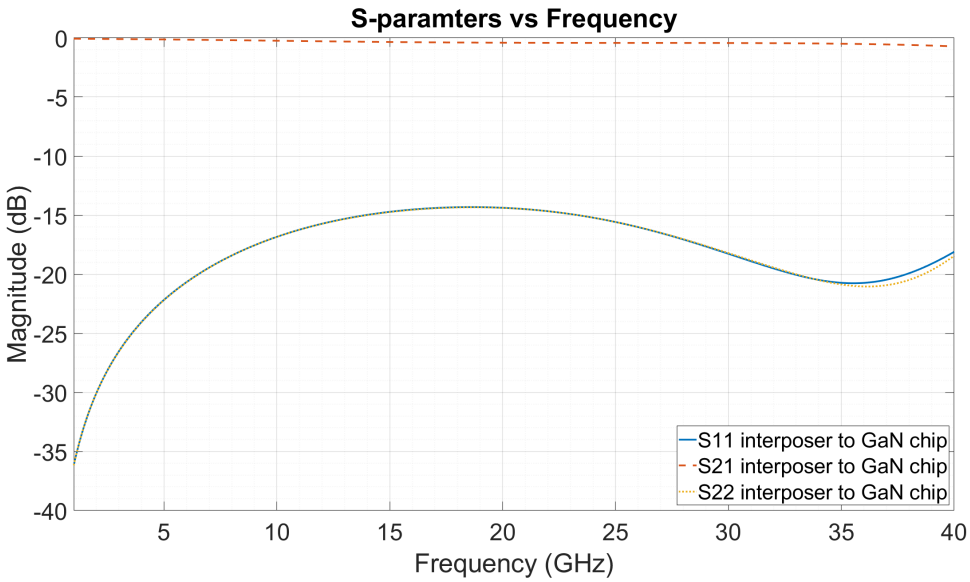
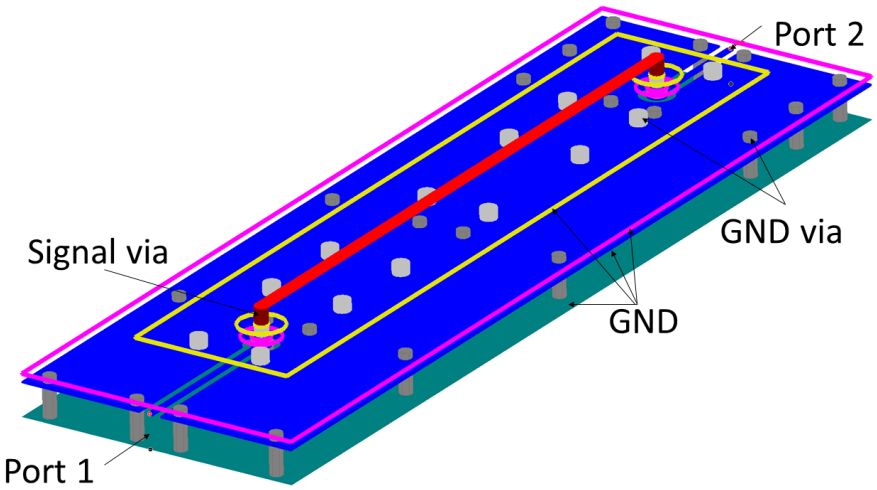


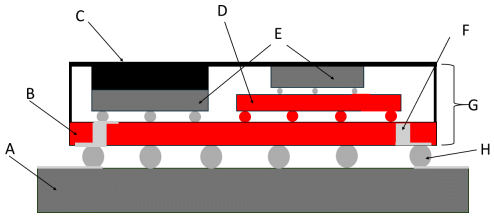
Figure 3.14: S-parameters of the signal path between the interposer and the GaN RF-chiplet.

3.3.4 Interposer to Micro-PCB Transition

The simulation of the transition between mPCB and interposer was carried out similarly to section 3.3.3. The difference was that the material stack up of the mPCB had to be arranged manually. A 50 Ω line for the interposer was placed in a layout for the mPCB together with solder bumps. In the new layout, vias and 50 Ω lines were placed in order to enable simulation of the transition. The complete setup can be seen in Figure 3.15. Four GND planes can be seen in the figure: the blue, pink, green, and yellow planes. The blue plane acts as the ground reference for the CPWG located on the mPCB. The yellow plane is the bottom ground plane of the interposer, meaning that it is connected to the mPCB through the light-grey GND vias. Two signal vias connecting the different materials can also be seen, as well as the simulation ports. This setup is a simplified version of the mPCB stackup shown in Figure 3.9, since the SignalBottom layer was found to have a negligible impact on the simulation results.



(a) Simulation stack up in RFPro for the simulation between the interposer and mPCB.



(b) Simulation interface shown in red inside the SiP. B is the mPCB, D is the interposer, F is vias and signal traces and H is the solder bumps.

Figure 3.15: The simulated structure next to the simulation interface within a SiP which is shown in red.

The simulations were carried out in RFPro using MultiTech. S-parameters were extracted from the simulations and the results can be seen in Figure 3.16. The results show that the transition provides good signal transmission with low reflection across the entire frequency range.

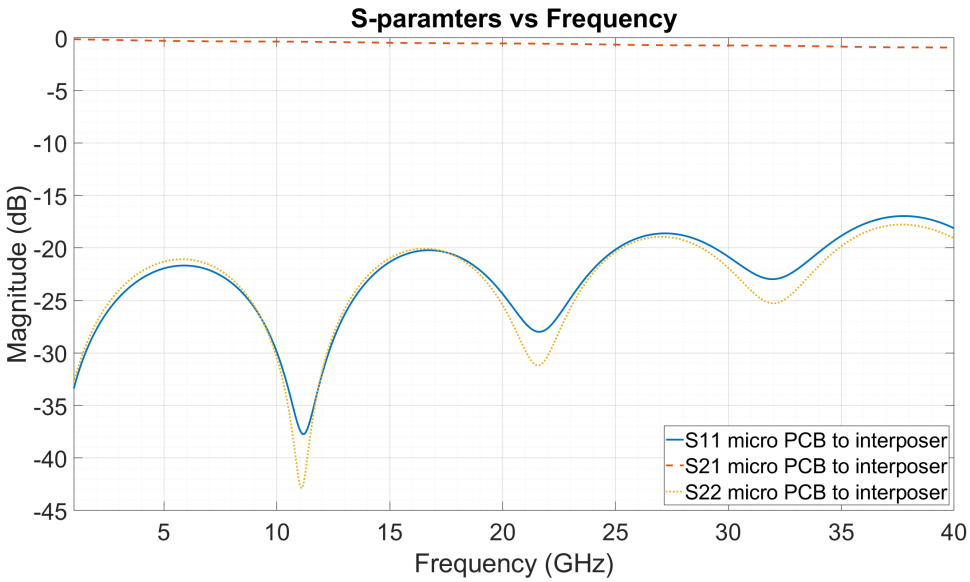
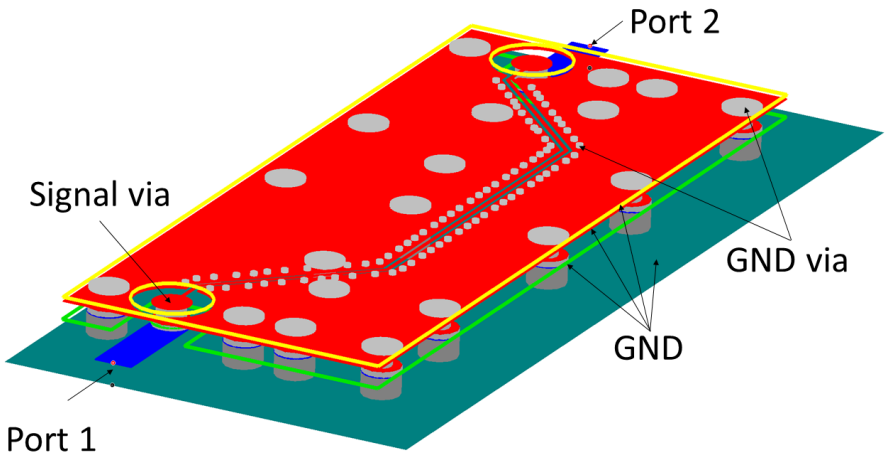


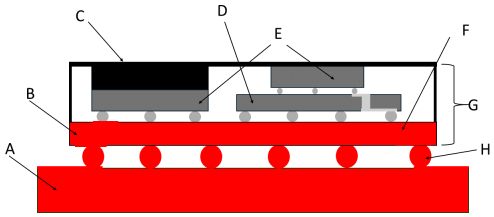
Figure 3.16: S-parameters of the signal path between the interposer and the mPCB.

3.3.5 Micro-PCB to PCB transition

To simulate the transition between the PCB and mPCB, the material stackup of the two-layer PCB was created in ADS according to the material parameters provided by the manufacturer. A 50 Ω line with connection pads at the end was placed in a layout in the workspace for the mPCB. It was connected using cylindrical solder bumps to 50 Ω lines in the PCB layout. Simulations were conducted in RFPro using MultiTech to extract S-parameters similarly as in section 3.3.3. The simulated structure together with the simulation interface can be seen in Figure 3.17. The blue microstrip lines are located on the PCB, and signal vias connect them to the CPWG on the mPCB. Four GND planes are present: the dark green, light green, red, and yellow planes. A clearance hole is present in the yellow GND plane above the signal via.



(a) Simulated structure in RFPro for simulation between mPCB and interposer.



(b) Simulation interface shown in red for the SiP. A is the PCB, B is the mPCB, F is the signal traces and H is the solder bumps.

Figure 3.17: The simulated structure next to the simulation interface within a SiP which is shown in red.

The S-parameters for the simulation can be seen in Figure 3.18. The results show that the transition provides good signal transmission with moderate reflection in the 1–20 GHz range. For the remaining frequency range the reflection and transmission losses increase.

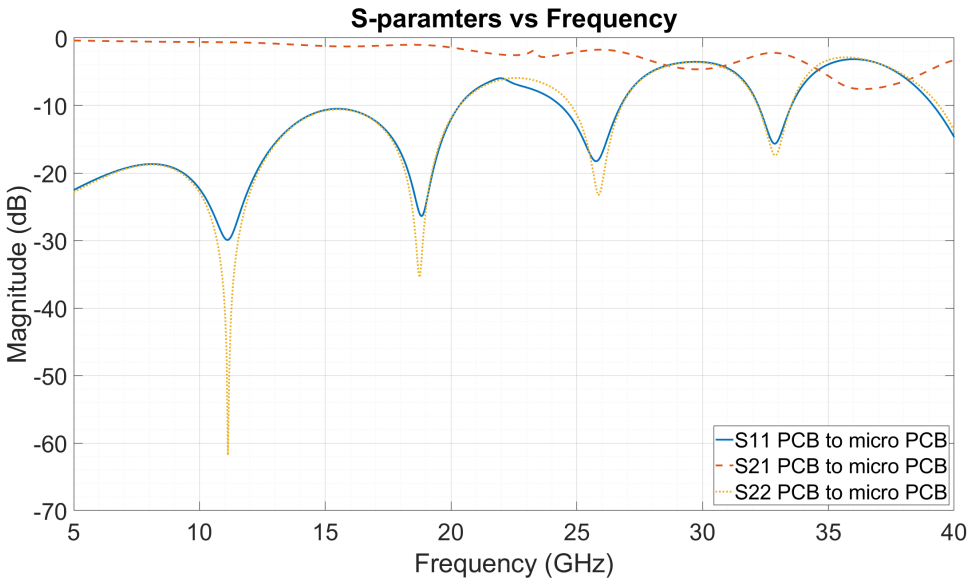
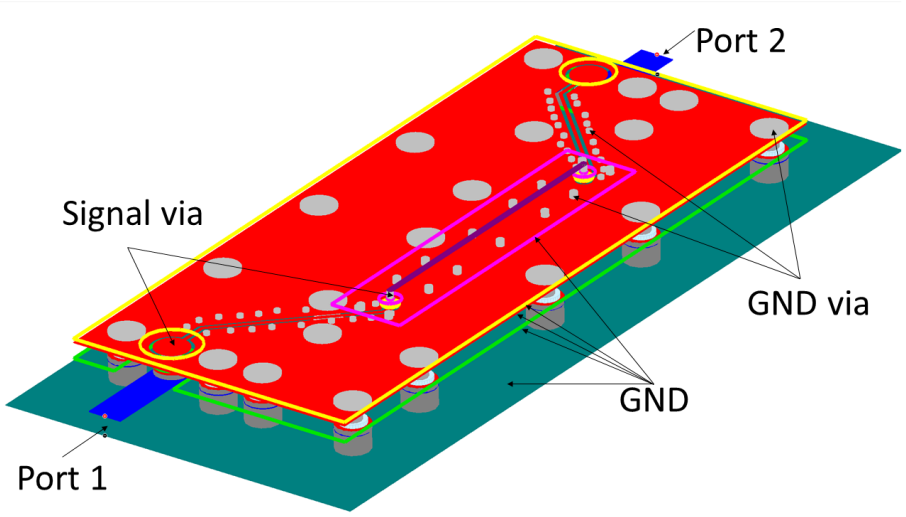


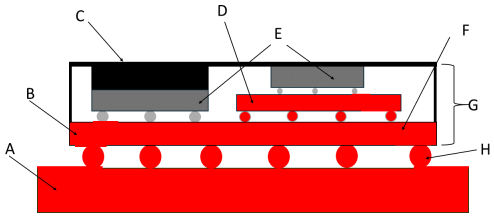
Figure 3.18: S-parameters for the transition between PCB and mPCB.

3.3.6 Interposer to PCB Transition

To simulate the transition between the PCB and the interposer the building blocks from the individual materials were put together in a new layout in the PCB workspace. The simulated structure together with the simulation interface can be seen in Figure 3.19. The PCB consists of the blue microstrip line and the dark green GND plane. The pink GND plane represents the bottom ground plane of the interposer, while the dark purple structure is the microstrip line located on it. The remaining GND planes belong to the mPCB. Signal vias connect the different conductors to each other.



(a) Simulated structure in RFPro for simulation between interposer and mPCB.



(b) Simulation interface shown in red for the SiP. A is the PCB, B is the mPCB, F is the signal traces and H is the solder bumps.

Figure 3.19: The simulated structure next to the simulation interface within a SiP which is shown in red.

The S-parameters for the setup were extracted in RFPro and the results can be seen in Figure 3.20. The results show that the transition provides acceptable signal transmission with moderate reflection in the 1–33 GHz range. For the remaining frequency range the reflection and transmission losses increase.

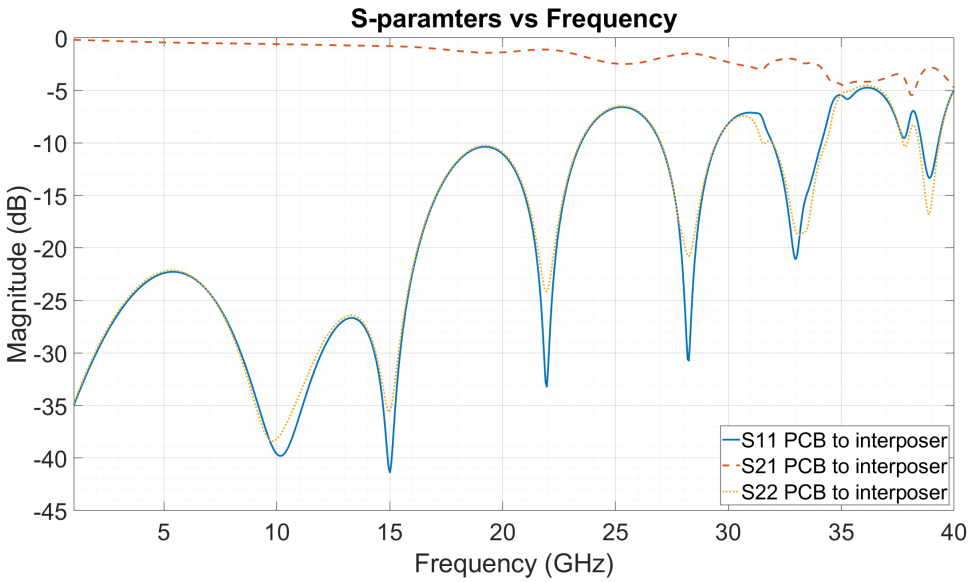
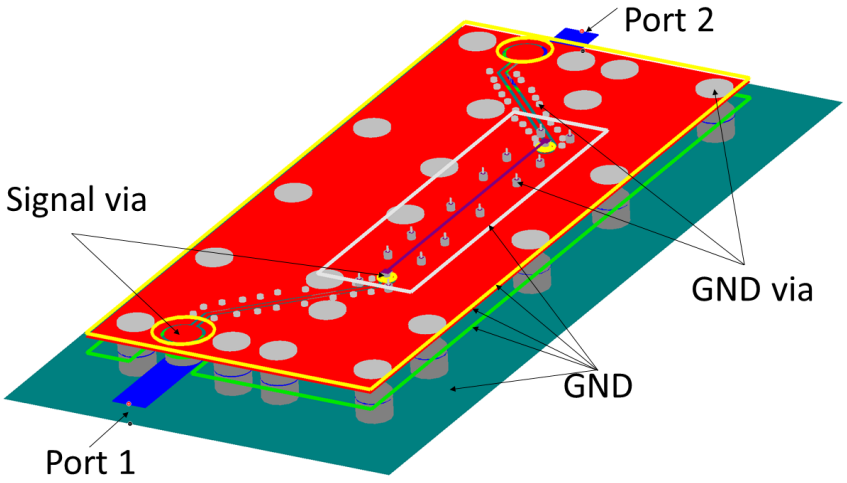


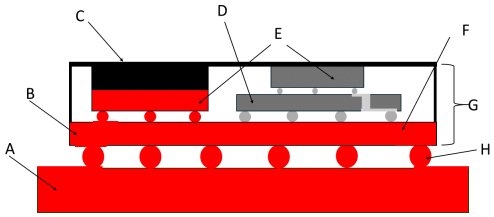
Figure 3.20: S-parameters for the signal path between PCB to interposer.

3.3.7 PCB to RF-chiplet Transition

To simulate the transition from the PCB to the GaN RF-chiplet, a 50 Ω line of the RF-chiplet was flip-chip mounted onto the mPCB layout. This structure was then placed on the PCB layout to enable the simulations. The simulated structure together with the simulation interface can be seen in Figure 3.21. The setup is similar to the one described in Section 3.3.6, but an RF chiplet is used instead of the interposer. The purple microstrip line represents the transmission line located on the RF chiplet. Since the RF chiplet is flip-chip mounted, the white GND plane is located above the microstrip line on the chiplet.



(a) Simulated structure in RFPro for simulation between mPCB and flip-chip mounted RF-chiplet.



(b) Simulation interface shown in red for the SiP. A is the PCB, B is the mPCB, F is the signal traces and H is the solder bumps.

Figure 3.21: Simulation setup for a flip-chip mounted component together with the simulation interface, shown in red. The component is placed beneath the white rectangle.

The simulations were carried out using MultiTech in RFPro. The extracted S-parameters are shown in Figure 3.22. Up to 18 GHz, the transmission is good and the reflection is low. Above this frequency, the transmission losses and reflections increase.

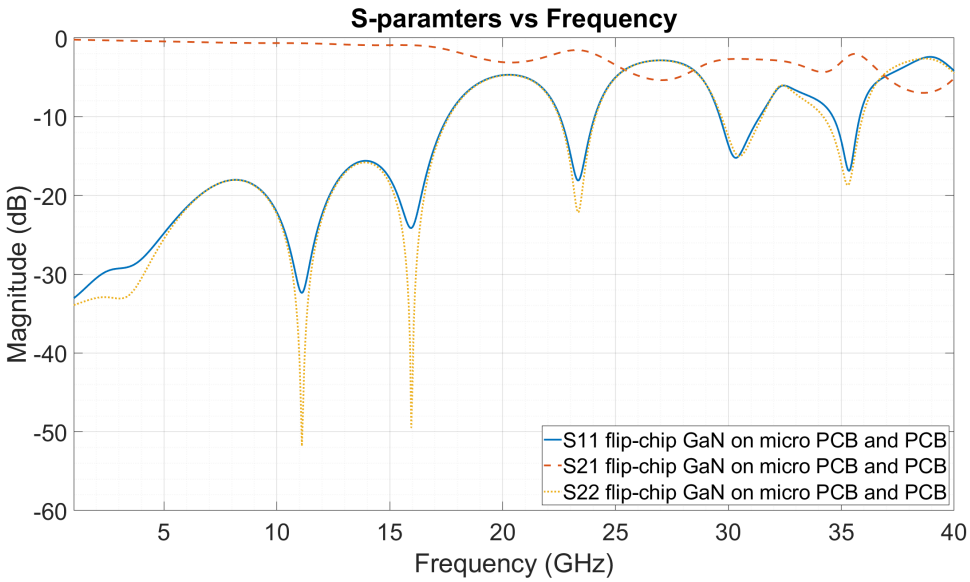
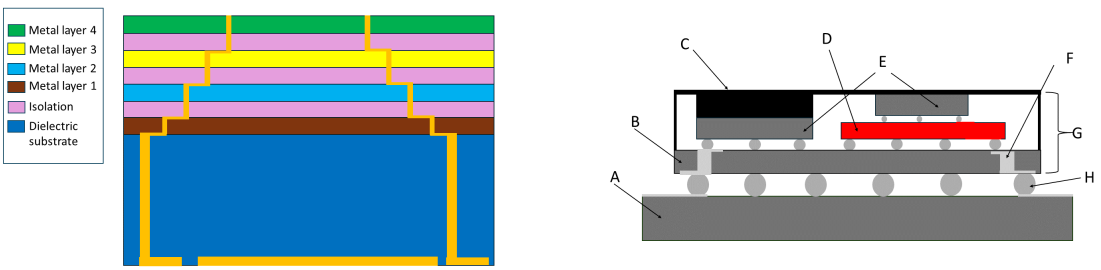


Figure 3.22: S-parameters for the signal path between PCB to flip-chip mounted GaN chip.

The results from Section 3.3 show that signal transmission through different materials in a SiP can be achieved using MultiTech simulations. It can also be seen that the results depend on which transitions are being simulated. Transitions containing PCB and mPCB show high transmission loss and reflection.

3.4 Interposer Evaluation

To evaluate the RF capabilities in terms of the properties of the different layers and capabilities for implementing passive components on the interposer for future SiP implementation, inductors and filters were designed and simulated on the interposer. These will be presented in this section. First a comparison between different inductor topologies is presented, followed by filter evaluation and simulation of existing RF components. The stackup and simulation interface for the interposer can be seen in Figure 3.23.



(a) Material stackup for the interposer

(b) Simulation interface shown in red for the SiP. D is the interposer.

Figure 3.23: Layer stackup together with the simulation interface for the interposer.

3.4.1 Simulation of Octagonal Inductors

To investigate the RF capabilities of the interposer, the two default inductor designs included in the PDK, one circular and one octagonal-shaped, were simulated. An example of an octagonal inductor can be seen in Figure 3.24.

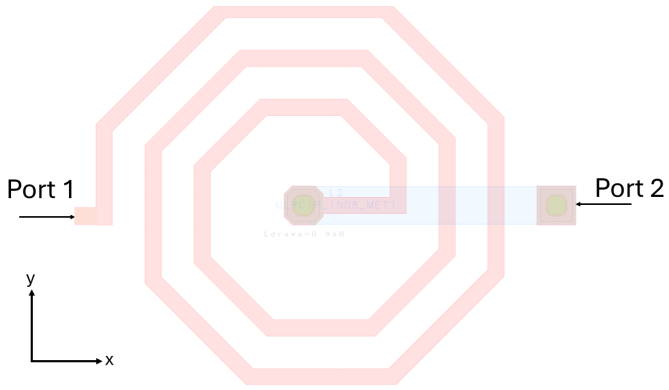


Figure 3.24: Octagonal inductor on met1 layer in red on the interposer. The blue air bridge on met3 layer can be seen in the figure. The TML ports 1 and 2 can also be seen.

The octagonal inductor was simulated for different trace widths and spacing between adjacent traces to evaluate the effects of the inductor parameters. The two metal layers, met1 and met3, were investigated to evaluate the effects of placing the inductor on different layers. For the simulations of the octagonal inductors in RFPro, MoM was used in order to reduce the simulation time and enable a more iterative design process. For this, default settings in ADS were used. As a GND reference for the simulation a GND cover placed under the inductor was used in ADS. The unloaded Q-value was evaluated since the simulations were done by exciting the inductor with 50 Ω ports directly at the inductor terminals. The Q-value and inductance were extracted for the different octagonal inductors.

3.4.2 Simulation of Circular Inductors

The circular inductor, also included in the PDK, was simulated using different trace widths and spacing values between adjacent traces. An example of the circular inductor can be seen in Figure 3.25.

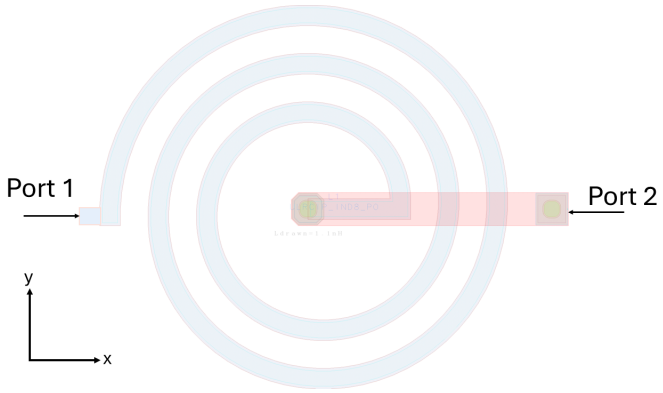


Figure 3.25: Circular inductor on met3 and met4 layers. The red air bridge on met1 layer can also be seen in the figure. The TML ports 1 and 2 are also marked out.

The circular inductor, also included in the PDK, was simulated using different trace widths and spacing values between adjacent traces. Compared with the octagonal inductor, the conductors of the circular inductor consisted of a combination of the met3 and met4 layers. Hence, only the width and distance between the traces could be varied and not the layer placement of the inductor. The simulations were also carried out using the RF MoM solver with the default settings in RFPro to speed up the simulation process. As a GND reference for the simulation a GND cover was used in ADS. Unloaded Q-values and inductance values from the different simulations were then extracted.

3.4.3 Design and Simulation of two layer Inductors

Since the interposer had multiple layers, it was possible to design two-layer inductors. Due to specifications in the manufacturing process of the interposer, only the combinations met1 and met3 or met1 together with met3 and met4 could be realized. The trace width of the design was selected to be as thin as possible while still satisfying the PDK requirements in order to maximize the inductance according to the inductance equations presented in Section 2.6. A circular two-layer inductor can be seen in Figure 3.26. Inductors with different numbers of turns were simulated using the FEM solver in RFPro. The GND reference was a cover placed under the inductor. Unloaded Q-values and inductance values were then extracted from the simulations.

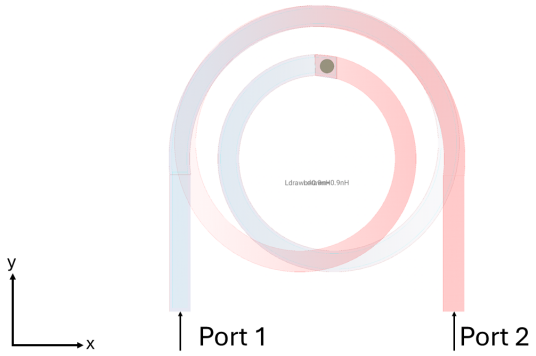


Figure 3.26: A arbitrary two layer inductor with met1 layer in red combined with met3 and met4 layer in blue. The TML ports 1 and 2 are marked out.

3.4.4 Design and Simulation of 3D-Inductor

Using the hot-via technology available in the interposer, a 3D inductor which can be seen in Figure 3.27 was designed.

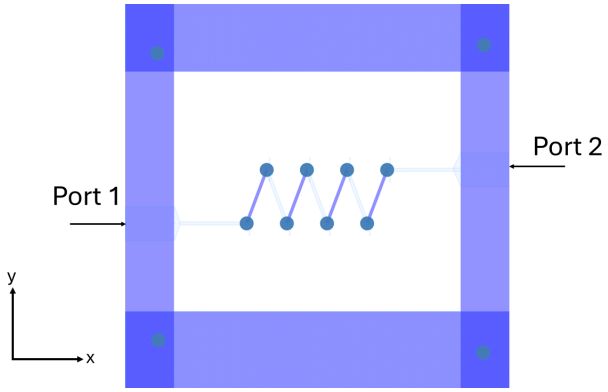


Figure 3.27: 3D inductor seen from above on the met3 and bottom layers of the interposer. The surrounding shield can be seen around the inductor. The dark blue lines drawn in the y-direction are the bottom-layer signal traces, and the light blue lines drawn in both x and y-direction are the met3 signal traces. The TML ports 1 and 2 are marked out and can be seen in the figure.

Hot vias were placed at the minimum distance allowed by the PDK in the x-direction from each other. In the y-direction, the distance between them was equal to the substrate thickness in order to maintain symmetry in the design. The shield around the inductor was placed at a distance of two-and-a-half substrate thicknesses from the closest signal via to keep the shield at a sufficient distance according to the theory of 3D inductors presented in Section 2.6.1. The structure was simulated using different metal layers, and the Q-value and inductance were extracted from the simulations. A FEM solver was used to obtain the S-parameters but since the design uses the bottom metal layer as a signal trace the surrounding shield had to be used as the GND referens.

3.4.5 Comparison between Inductors.

To compare the different types of inductors that were simulated, five different inductors with an inductance value of 1.6 nH were examined. These were two types of 3D inductors, one using the met1 layer and one using the met3 layer, one octagonal inductor, one circular inductor, and one two-layer inductor. The inductance and resonance frequency of the inductors can be seen in Figure 3.28. The Q-value of the inductors can be seen in Figure 3.29. Table 3.3 summarizes the different inductors in terms of inductance, resonance frequency, Q-value, and size.

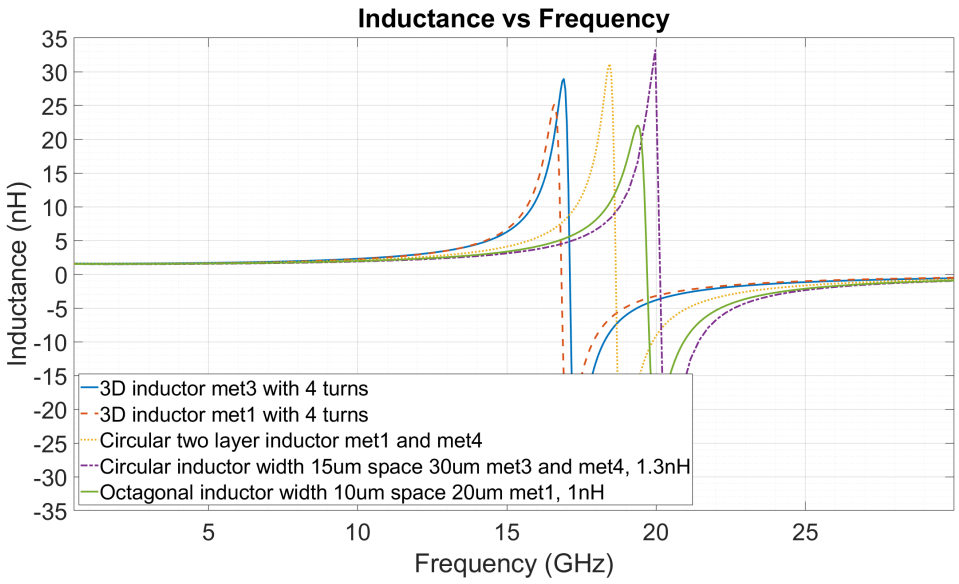


Figure 3.28: Resonance frequencies for different types of inductors with the same inductance value. For 3D inductors, the number of turns means the number of closed via loops, e.g. 4 turns correspond to 8 hot vias in total. The inductance value in the legend for the octagonal and circular inductors correspond to the nominal value from the PDK.

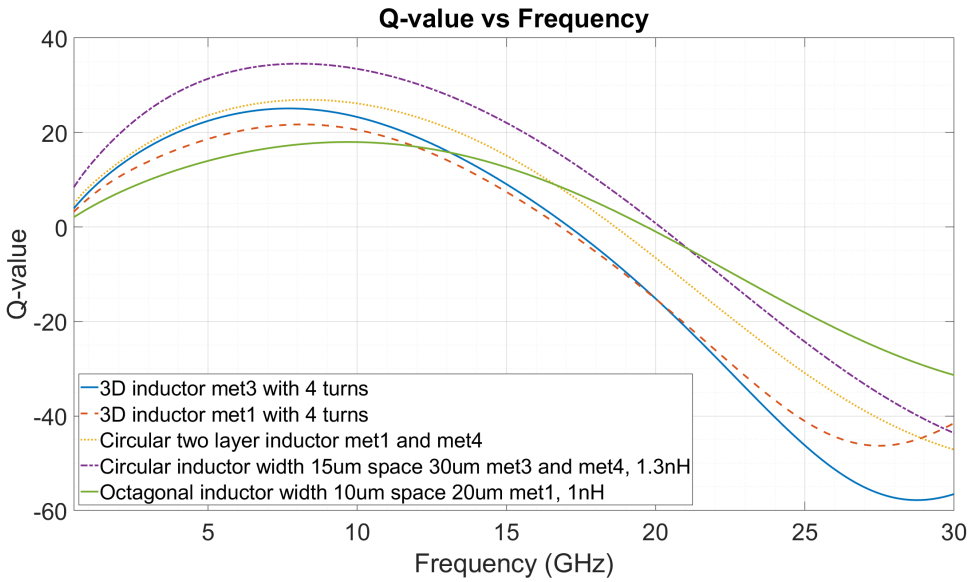


Figure 3.29: Q-value for different types of inductors. For 3D inductors, the number of turns means the number of closed via loops, e.g. 4 turns correspond to 8 hot vias in total. The inductance value in the legend for the octagonal and circular inductors correspond to the nominal value from the PDK.

Table 3.3: Comparison of five inductors in terms of inductance, maximum Q value, resonance frequency, and size.

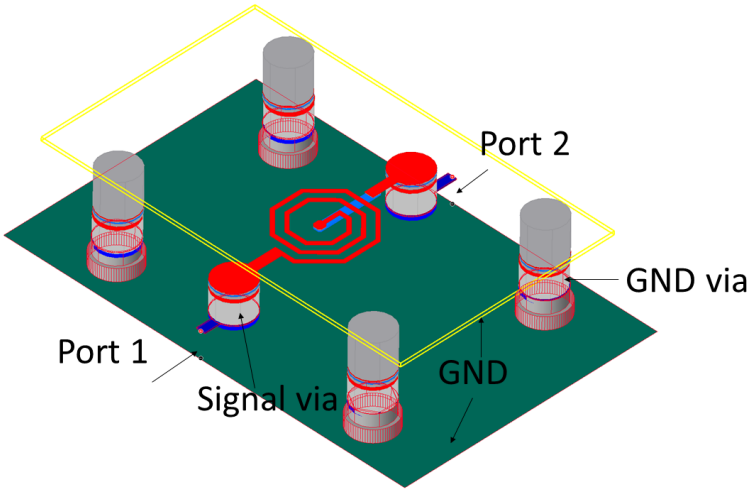
Inductor	**L (nH)**	**Max Q**	**Res. Freq. (GHz)**	**Size (μm)**
Two layer	1.6	28	18.5	215 × 230
Octagonal	1.6	19	19.8	300 × 235
Circular	1.6	35	20.2	240 × 280
3D met1	1.6	22	16.5	1150 × 1150 (190 × 450 inner)
3D met3	1.6	25	17	1150 × 1150 (190 × 450 inner)

From Table 3.3, it can be seen that the circular inductor has the highest Q-value and resonance frequency. The two layer inductor has the smallest size and the 3D inductor occupies the largest area. Depending on the application an inductor is used for, different designs are preferred. If, for example a narrow band filter should be constructed a circular inductor could be used because of its high Q-value. In a case where minimizing RF-chiplet area is of great importance a two-layer inductor is the best choice.

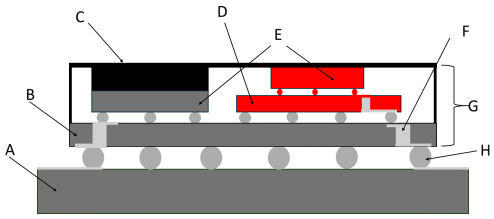
3.4.6 MultiTech Simulations of Inductors

The inductors were then simulated in MultiTech where they were flip-chip mounted on top of an RF-chiplet to evaluate the effect of the inductor parameters when the signal propagates between two different materials. These signal paths are of particular interest because they enable the possibility of creating an integrated design

between the interposer and the RF-chiplet. An example of this setup for an octagonal inductor together with the simulation interface of SiP can be seen in Figure 3.30. The set up is similair to the evaluation of MultiTech simulations. 3D-inducotrs is placed in a similar way but in that case the yellow GND plane has a hole in the middle where the traces of the 3D-inductor is drawn.



(a) Simulation stackup for MultiTech simulations of inductors.



(b) Simulation interface shown in red for the SiP. D is the interposer, E is the RF-chiplet, F is the signal traces and H is the solder bumps.

Figure 3.30: Simulation stackup for MultiTech simulations of inductors together with the simulation interface, shown in red within the SiP.

All inductors that were flip-chip mounted and simulated used the same simulation setup. For all simulations, the Q-value and inductance were obtained from the simulations. The results from an octagonal and a 3D inductor can be seen in Figures 3.31-3.34. It can be observed that the flip-chip mounting influences the inductor characteristics, both in terms of resonance frequency and Q-value but not the inductance value.

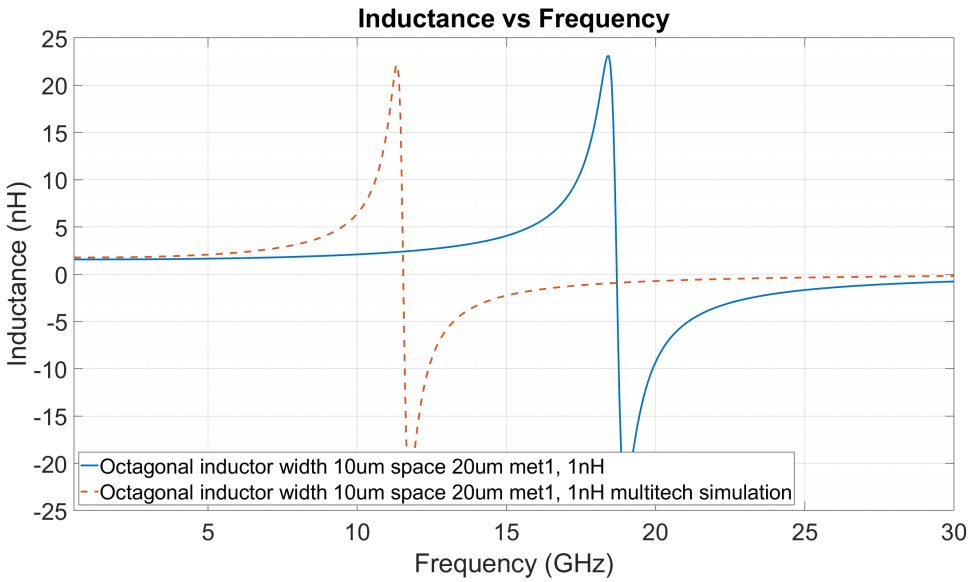


Figure 3.31: Inductance comparison between an octagonal inductor on the interposer and an octagonal inductor flip-chip mounted onto a GaAs RF-chiplet and simulated using MultiTech, including the resonance frequencies of the structures.

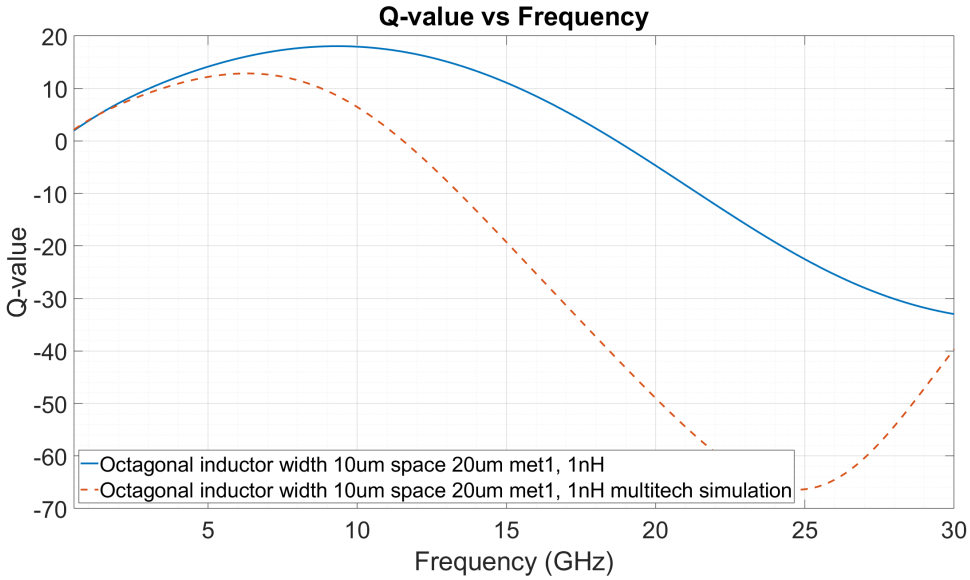


Figure 3.32: Q-value comparison between an octagonal inductor on the interposer and an octagonal inductor flip-chip mounted onto a GaAs RF-chiplet and simulated using MultiTech, including the resonance frequencies of the structures.

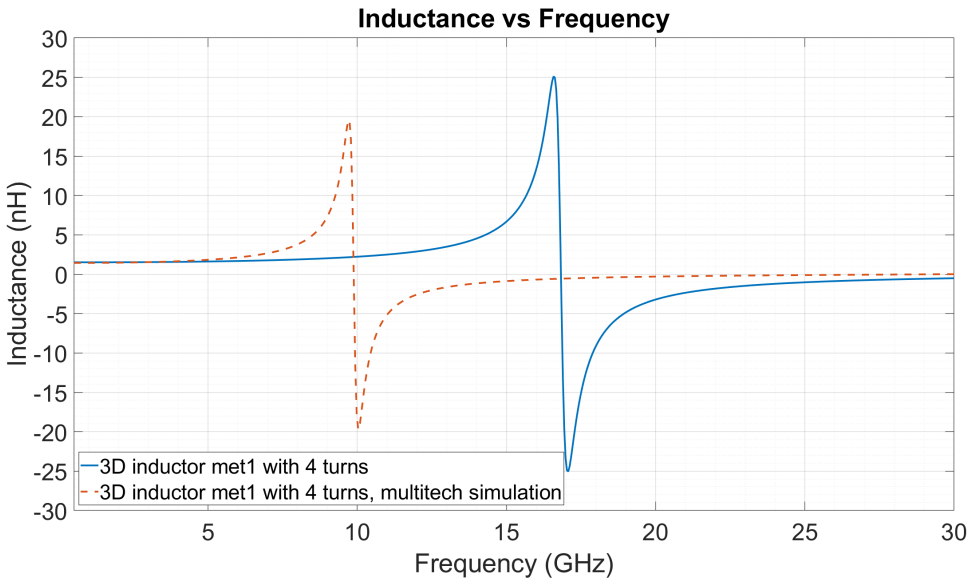


Figure 3.33: Inductance comparison between a 3D inductor on the interposer and a 3D inductor flip-chip mounted onto a GaAs RF-chiplet and simulated using MultiTech, including the resonance frequencies of the structures.

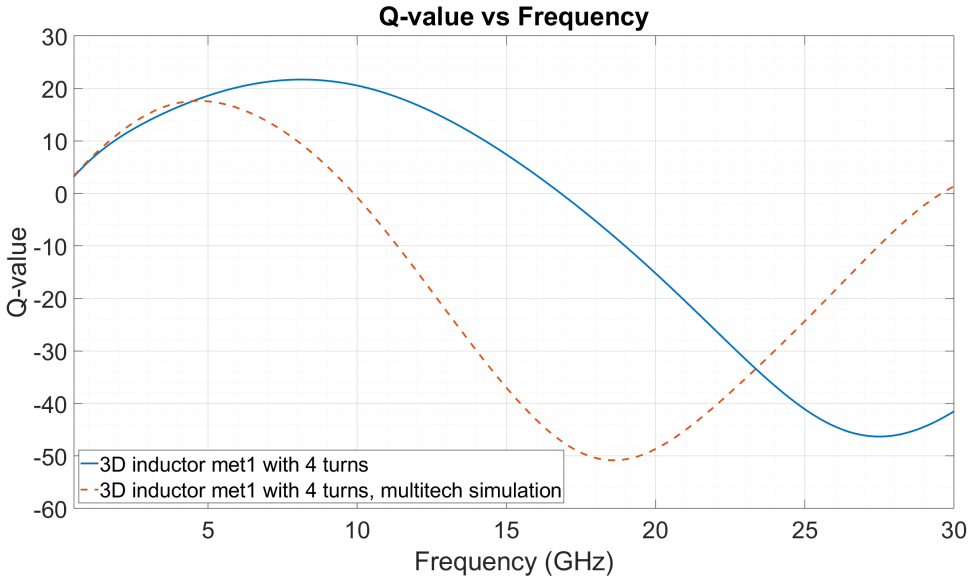


Figure 3.34: Inductance comparison between a 3D inductor on the interposer and a 3D inductor flip-chip mounted onto a GaAs RF-chiplet.

To evaluate the reason for the decreased performance caused by the flip-chip mounting, an octagonal planar inductor with the same size and parameter values as the one shown in Figure 3.30a was simulated. An extra length was added to both ports, equal to the additional length introduced by the signal via and microstrip line on the RF chiplet. The resulting inductor can be seen in Figure 3.35.

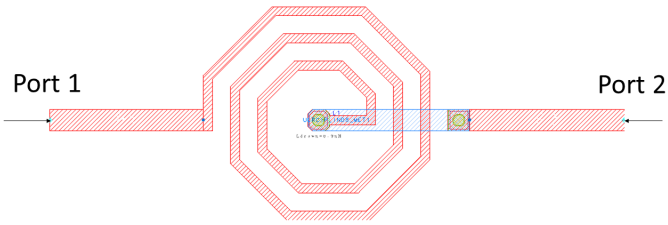


Figure 3.35: Octagonal inductor on met1 layer in red on the interposer. The blue air bridge on met3 layer can be seen in the figure. The TML ports 1 and 2 can also be seen. The extra length length added at the two ports is also present.

A comparison between the inductor with additional port length, the regular inductor, and the flip-chip mounted inductor was conducted. The results in terms of resonance frequency and Q-value are presented in Figures 3.36 and 3.37. It can be observed that both the resonance frequency and the Q-value decrease when additional length is added to the ports. However, the performance of the flip-chip mounted inductor is still worse. This indicates that the additional interconnect length contributes to the performance degradation, but cannot fully explain the observed behavior. The remaining degradation is therefore likely caused by dielectric loading and the close proximity of the ground plane, which introduce additional parasitic capacitances.

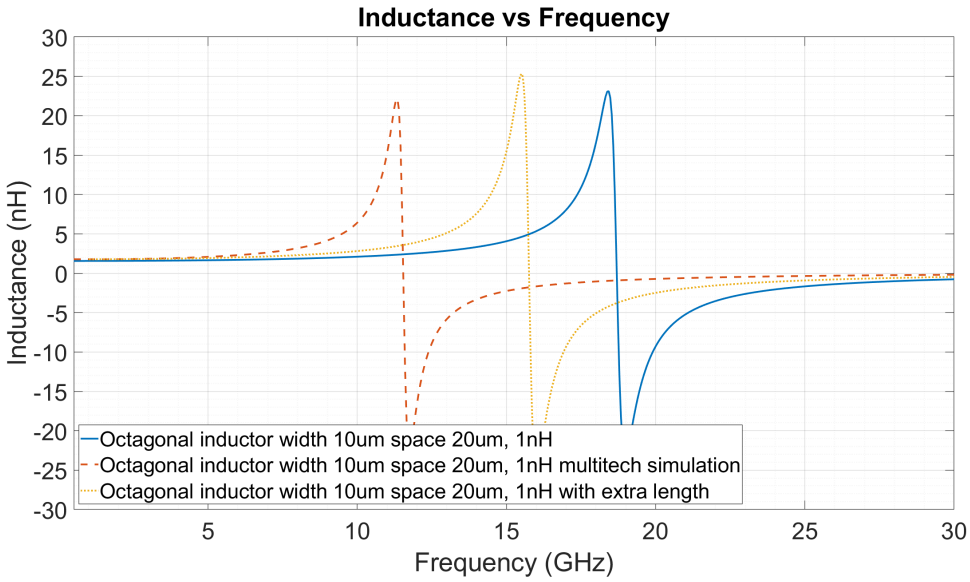


Figure 3.36: Inductance comparison between a regular octagonal inductor, an octagonal inductor with extra length, and a flip-chip mounted inductor on the interposer.

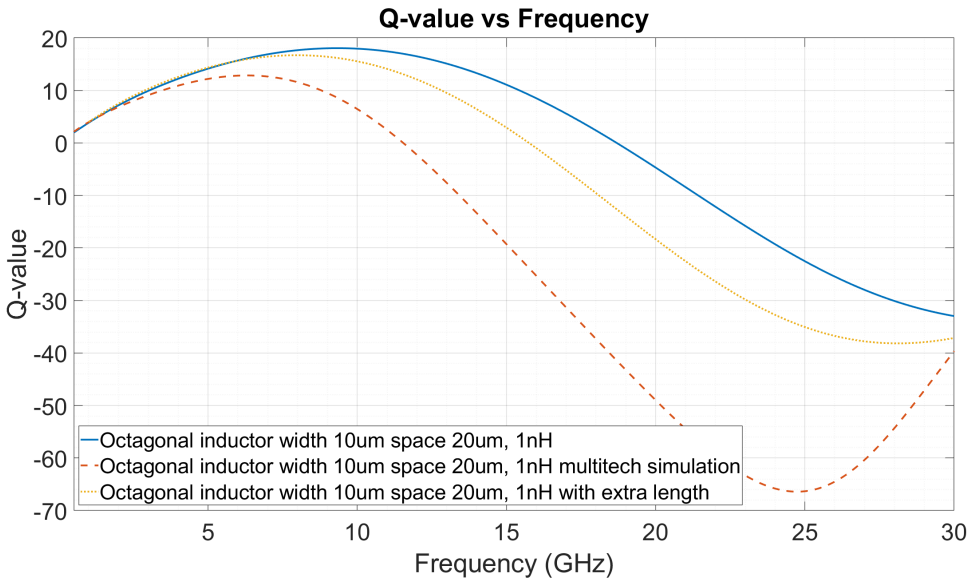
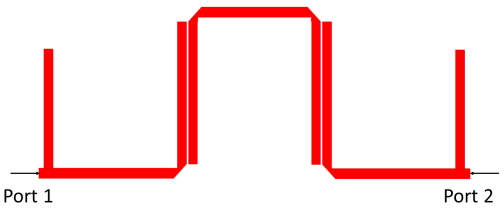


Figure 3.37: Q-value comparison between a regular octagonal inductor, an octagonal inductor with extra length, and a flip-chip mounted inductor on the interposer.

3.4.7 Filter Design and Simulation

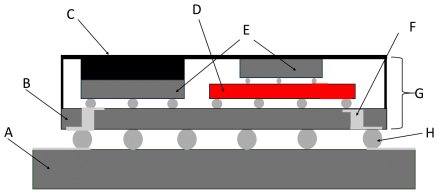
To further evaluate the interposer, two different Chebyshev filters were designed, simulated, and analyzed. One narrowband band-pass Chebyshev filter in X-band (8-12 GHz) using microstrip lines was designed in order to evaluate the impact of the different metal layers on filter design. One Chebyshev filter in Ku-band (12-18 GHz) using microstrip lines was additionally designed. Both filters were tried to be realized using lumped components. However, for the two frequency ranges of interest, they were difficult to realize since the inductor and capacitor values became too large for the interposer design rules.

The narrowband filter was designed to achieve the highest possible Q-value. The Ku-band filter was designed to have a bandwidth covering the whole Ku-band with an insertion loss (IL) below 3 dB. Different numbers of sections for the filters were evaluated to meet the requirements together with different topologies to minimize the filter size. This was done in an iterative process where filters were simulated and optimized for the requirements and then verified using EM simulations in ADS. For the final designs, S-parameters were extracted. The filters can be seen in Figure 3.38. These filters was simulated using MoM.



(a) Three section Chebyshev filter in Ku-band with large bandwidth.

(b) One section narrow band band-pass Chebyshev filter for X-band using microstrip line. The microstrip lines are placed on met1.



(c) Simulation interface for the filters in red.

Figure 3.38: Chebyshev microstrip filters and simulation interface.

The S-parameters for the X-band filters designed on different metal layers are presented in Figures 3.39-3.40. It can be seen that the narrowest filter bandwidth was achieved using one of the three metal-layer combinations: met1-met2-met3, met3-met4, or met1-met2-met3-met4. The results for these combinations in terms of bandwidth, IL, and RL can be seen in Table 3.4.

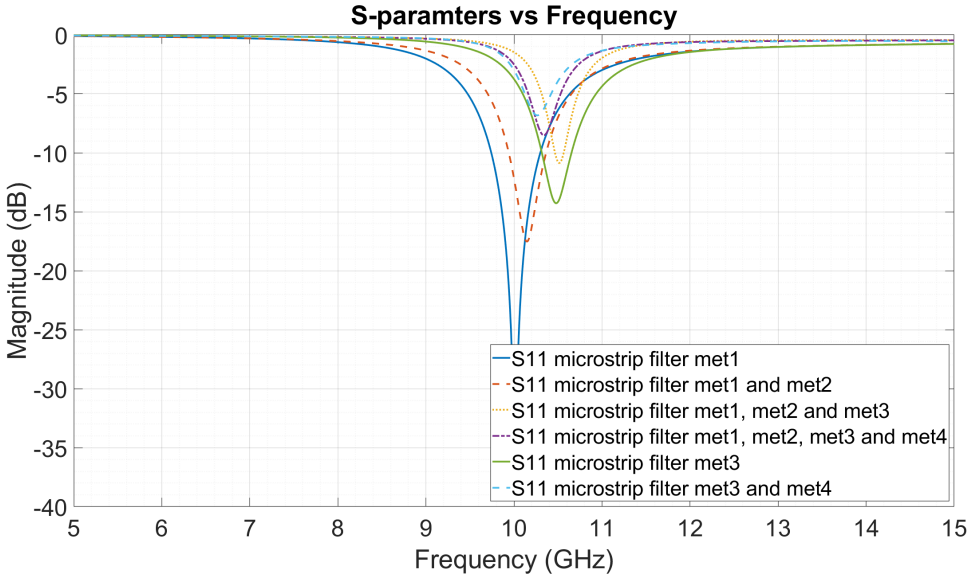


Figure 3.39: S_{11} for X-band filter on different metal layers on the interposer.

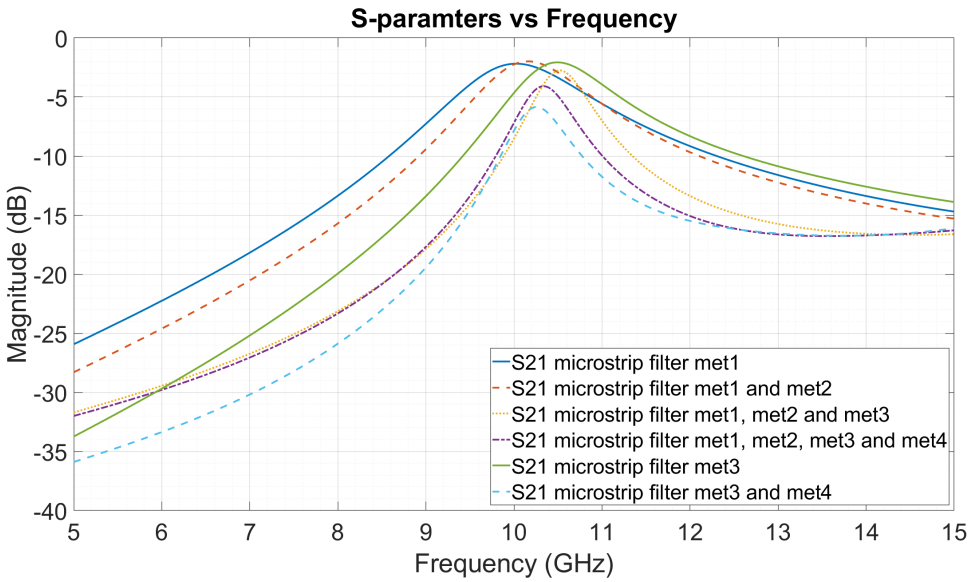


Figure 3.40: S_{21} for X-band filter on different metal layers on the interposer.

Table 3.4: Comparison of X-band filter performance for different metal layer combinations. IL and RL is for the center frequency.

Metal Layers	Bandwidth [GHz]	IL [dB]	RL [dB]
met1-met2-met3	0.7	-3	-11
met3-met4	0.7	-6	-7
met1-met2-met3-met4	0.7	-4	-8.5

For the Ku-band filter, the S-parameters are presented in Figure 3.41. It can be seen that a 5 GHz bandwidth with a center frequency of 15 GHz was achieved for a three-section Chebyshev filter with an IL below 3 dB across the entire passband.

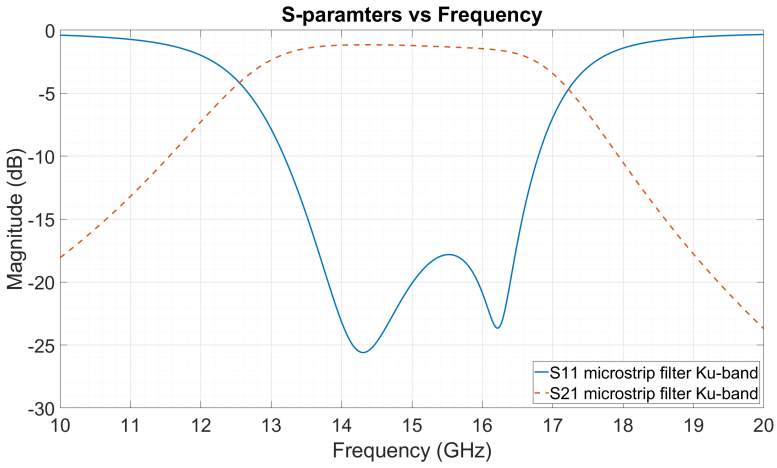
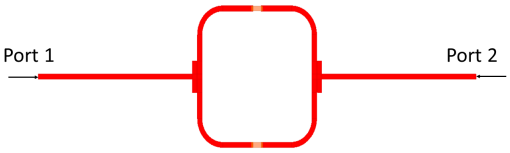


Figure 3.41: S-paramters for Ku-band filter on the interposer placed on met1 layer.

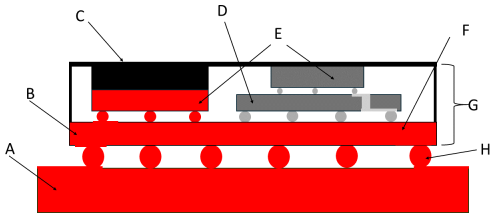
3.5 Evaluation of Flip-Chip Mounted Components on micro-PCB

In addition to the circuits and components designed within this thesis, a number of existing components relevant to a SiP solution were implemented and simulated. These consist of a ring resonator and one coupled-line filter in Ku-band. They are of specific interest for future SiP implementations since these simulations combine flip-chip-mounted components on the mPCB and PCB. The simulation setup is shown in Figure 3.21. The ring resonator can be seen together with the coupled-line filter and the simulation interface in Figure 3.42. The individual componets was simulated with MoM. For this the TML ports was placed on microstrip line on the PCB with the bottom layer as the GND for the structure. For the flip-chip mounting on the mPCB a similar structure as in Figure 3.21a but instead of a microstrip line the ring resonator and the coupeld line filter was placed in the structure.



(a) Topology of a ring resonator simulated in the scope of the thesis.

(b) Topology of a coupled line filter simulated in the scope of the thesis.



(c) Simulation interface for pre-designed components.

Figure 3.42: Microwave filter and resonator topologies together with simulation interface for pre-designed components.

A comparison of S-parameters between the MultiTech simulations and the individual simulations of the resonator and filter is presented in Figures 3.43-3.44. For the filter, it can be seen that the signal transmission degrades in the passband compared to the individual simulation. A ripple also appears in the simulations. The resonator also experiences ripple in the passband together with a downshift in the center frequency. The downshift in center frequency can clearly be seen in Figure 3.45.

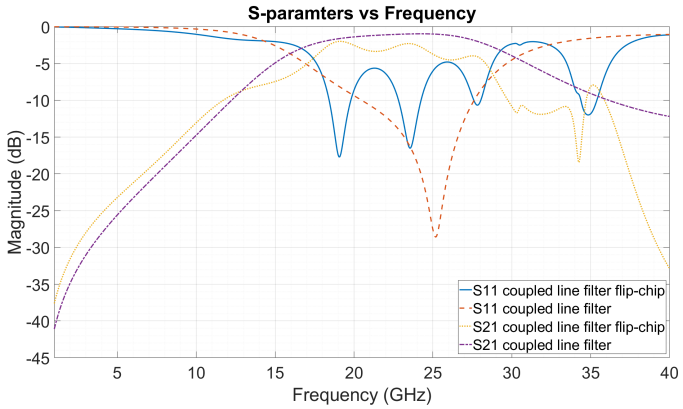


Figure 3.43: S-parameters for a coupled-line Ku-band filter implemented on the met1 layer on the interposer, simulated both with MultiTech and without MultiTech.

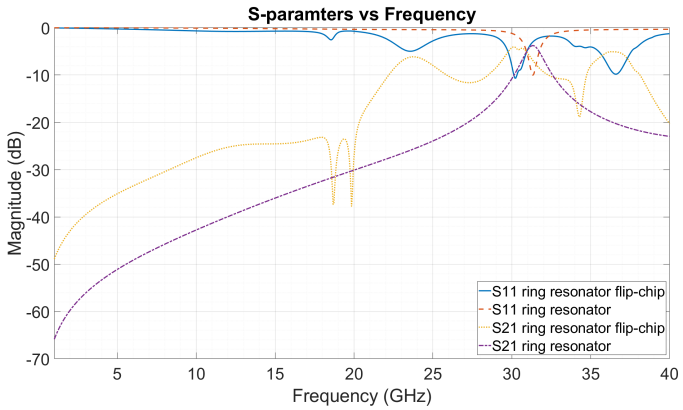


Figure 3.44: S-parameters for a ring resonator on the interposer implemented on the met1 layer, simulated both with MultiTech and without MultiTech.

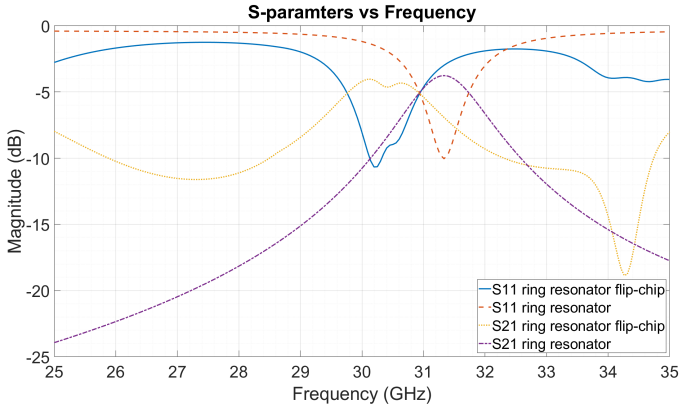
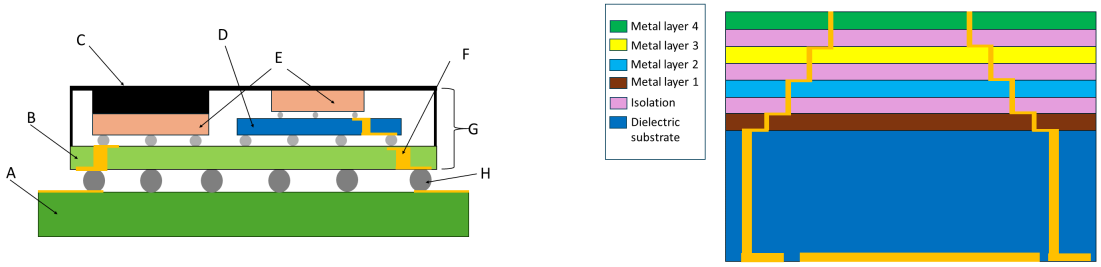


Figure 3.45: Zoomed-in S-parameters for a ring resonator on the interposer implemented on the met1 layer, simulated both with MultiTech and without MultiTech.

4

Discussion

Throughout this work, a toolbox for the development of future SiP solutions has been established. This has been achieved through the development of an evaluation board and simulation environments, characterization of the electromagnetic environment, and evaluation of the interposer. The stackup of the SiP solution and interposer used in this thesis can be seen in Figure 4.1.



(a) SiP stack up. **(b)** Interposer stackup.

Figure 4.1: Overview of the SiP and interposer stackup used in the report. A is PCB, B is mPCB, D is interposer, E is the RF-chiplet, F is the signal path and H are solder bumps.

4.1 MultiTech Simulation

It was shown that MultiTech simulations could be used to characterize a SiP solution. In order to do so, the correct settings in ADS were required in order to save simulation time and memory. Without adjusting any settings, the resources (time and memory) consumed to provide a result increased significantly, this can be clearly seen in Table 3.2. One could argue that even with adjusted settings, the simulations, which took 44 minutes, are time-consuming to finish a simulation. This is something that makes it hard to use MultiTech when designing a component in an iterative process where component values change frequently. These types of simulations probably work better to confirm a final design, for example to see if there is any frequency shift for a flip-chip mounted interposer filter placed in the mPCB. That said, almost all simulations carried out in this report can be considered wideband. Meaning that if a smaller frequency range had been simulated, both the simulation time and memory consumption could decrease. This depends on how the

simulations are set up. If a simulation is carried out for a lower frequency than the 40 GHz used in this thesis the tetrahedrons size for the FEM mesh could potentially be increased meaning that fewer solutions have to be calculated for a structure. This could reduce simulation time and memory usage. One way to combine wide band with narrow band simulations of a structure could be to use different numbers of simulation points depending on the frequency range of interest. If a small span is used more simulation points could be used to get a more accurate result. When a broadband solution is considered fewer simulation points could be used to confirm the behavior outside the frequency range of interest of the simulated band. This could potentially enable a more iterative workflow when considering a more limited frequency range. Numerous simulations have been conducted using different settings in order to speed up the simulation process. The results from these simulations were consistent, indicating that the results found in the report are independent of the selected simulation settings.

4.2 Simulation of Transitions

Transmission lines for the individual materials in the SiP solution show good electromagnetic performance characteristics in terms of both S_{21} and S_{11}. This can be seen in Figures 3.11 and 3.12. Good performance is also observed for the interposer-RF-chiplet and mPCB-interposer transitions, as shown in Figures 3.14 and 3.16. This indicates that these structures are well matched to a 50 Ω source. However, the simulation results for the PCB-mPCB, PCB-interposer, and PCB-RF-chiplet transitions, shown in Figures 3.18, 3.20 and 3.22, show increased transmission losses at higher frequencies. These losses may be related to dielectric losses and fringing effects, which become more significant at higher frequencies as described in section 2.2.2. Since the individual transmission lines show good performance over the simulated frequency range, the results indicate that the losses are mainly associated with the via transition rather than the individual materials themselves. In particular, the PCB-mPCB, PCB-interposer, and PCB-RF-chiplet transitions introduce losses that are not observed in the individual transmission lines or in the interposer-RF-chiplet and mPCB-interposer transitions The results indicate that transitions involving the PCB-mPCB interface are the main limiting factor for the high-frequency performance of the simulated SiP solution. One possible explanation is that the implemented mPCB stack-up, including the via implementation, does not accurately represent the physical structure since it was recreated in ADS based on the available design documentation. This can lead to small deviations in dimensions or via placement, which can significantly affect the performance at higher frequencies. This show the importance of having accurate models when simulating structures at high frequencies. Since it is unclear whether the observed losses originate from the transition itself or from inaccuracies in the simulation model, a simplified simulation setup consisting only of the PCB-mPCB transition could be realized. For example, a single stack-up could be built in ADS including all material layers from both the PCB and mPCB including the via solder bump connecting the two materials. The transition via could then be implemented using this stack-up to

replicate the transition. Instead of using the FEM solver, a MoM solver could be used to speed up the simualtion time in an iterative design process to identify which parameters have the largest impact on the transition performance, such as the via dimensions, the distance to the ground plane, or the placement of GND vias around the signal path. A more detailed investigation of this transition early in the design process would have helped to identify the source of the high-frequency losses. To confirm and validate the simulation setup, a manufactured SiP could be measured and used to validate the simulations.

4.3 Interposer

The interposer technology shows promising capabilities for inclusion of passive components in terms of the performance of the passive components designed and simulated. For the comparison between inductors in section 3.4.5, with the same inductance value, the circular inductor shows the best performance compared to the other inductors evaluated in this thesis, both in terms of high resonant frequency and Q-value. Since the Q-value is a metric of the losses of a resonating structure according to equation 2.27 this means that a circular inductor has the lowest loss. All inductors are placed on the same substrate, meaning that the substrate loss, i.e. the contribution from Q_d is identical for all structures. The differences in Q-value must therefore come from differences in conductor losses, radiation losses, or a combination of both. From the results it can be assumed that the layer combination met3-met4 are associated with low loss compared to, for example, the met1 layer where an octagonal inductor is placed. Contrary the geometry of the structures could have an effect on the losses as well. The hot vias of a 3D-inductor are embedded into the interposer substrate and this could change the properties of the total Q-value. However, from the simulations it is hard to distinguish between the different contributions to the total Q.

Better Q-value performance and increased inductance for the inductors could possibly be achieved by different designs. As an example, the 3D inductors constructed and simulated are restricted due to the interposer PDK. According to the governing equations for a 3D inductor in Section 2.6.1 the traces should be placed close to each other to maximize the inductance. This could possibly have an impact on the Q-value as well but it has to be examined.

In the case where an inductor on the interposer is flip-chip mounted on an RF-chiplet the performance in terms of Q-value and resonance frequency drops significantly. This is not so surprising since the flip-chip mounting technique introduces a new electromagnetic environment around the inductor that could affect the resonance frequency. The Q-value extracted could also be considered to be Q_l instead of Q_u for a single inductor. These effects need to be taken into account in a case where an RF-chiplet is being designed and some inductors are placed on the interposer. It might not be much to do about it, and in that case it might be better to place them directly on an RF-chiplet even if it occupies a large chiplet area. But this is something that needs to be examined in more detail to find areas of usage for

placing inductors on the interposer. The results in this thesis indicate that the additional signal path has an impact on the performance, but also that the new electromagnetic environment contributes to the degradation. Hence, future work could investigate the impact of, for example, GND-via placement to mitigate the decreased performance.

The X-band microstrip filter designed in this thesis showed a similar behavior as the inductor case when it comes to loss. Since a high Q-value corresponds to a sharp peak for a filter it can be seen in Figure 3.39 that multiple layers stacked together give a smaller bandwidth meaning that the losses are lower. For the X-band filter a smaller bandwidth than 0.7 GHz was hard to achieve with a Chebyshev filter structure. It could be that other topologies have different properties. This is something that could be examined in future studies. The Ku-band filter also shows promising characteristics for future implementation even if this specific design did not reach the design goal of covering the whole Ku-band. This could be affected by the number of filter elements or the losses occurring in the filter.

4.4 Flip-chip Mounted Components

The simulation results for the flip-chip mounted components, shown in Figures 3.43–3.45, appear reasonable given the uncertainties in the PCB and mPCB models used in the thesis. These simulations were made using the same model as for the simulations of transitions between materials, hence this assumption. For the flip-chip-mounted coupled-line filter it is hard to draw any conclusions since a ripple is introduced in the passband compared to the individual simulation. For the ring resonator, a ripple is introduced in the passband as well but it can clearly be seen that the center frequency is shifted down in frequency. This can be explained with equation 2.2 and the fact that the component is flip-chip mounted. The mounting style changes the effective permittivity of the resonator, hence the wavelength of the signal changes. According to the resonance criteria that states that a structure resonates when it is equal in length to either $\lambda_g/2$ or $\lambda_g/4$. So when λ_g changes so does the resonance frequency.

5
Conclusion

In this thesis a toolbox for future RF SiP implementations has been developed by examining simulation tools, a novel interposer technology, transitions between materials within a SiP and construction of an evaluation board for future SiP measurements. For simulations, the FEM MultiTech technique in ADS has been used in order to evaluate its capabilities and limitations for future RF-SiP design. The interposer has been evaluated through examination of different inductors including multilayer designs and filter topologies implemented on it. Different simulations were conducted to evaluate the effects on signal transmission between multiple materials. The results from the MultiTech simulations show that it is possible to evaluate a SiP using this technique. It was found that the settings used had a significant impact on simulation time and memory usage which highlights the importance of simulation settings when performing simulations. Even with reduced simulation time, it still takes a very long time to obtain results. This shows that MultiTech could be used to confirm a final design but it might be hard to implement it in an iterative design process.

Transitions between materials could be simulated, although with different results. Many transitions showed good performance in terms of transmission and reflection. The same applied to transmission on the individual materials. However, transitions between the two bottom layers included in the SiP stackup showed poor performance. This could possibly be explained by uncertainties in the models created in ADS or by the intrinsic material properties. Inductor designs implemented on the interposer show promising characteristics for future implementations where the designs presented in this thesis show similar performance to planar inductors implemented on the interposer. To really benefit from these designs more work needs to be conducted to optimize the designs, especially when it comes to optimizing future simulations. It is also of great importance to validate the simulation models of the mPCB and PCB in ADS by conducting physical measurements. Filters placed on the interposer show good performance for both broadband and narrowband applications even if it was found to be hard to make filters with a bandwidth < 0.7 GHz. The metal layer on which the transmission lines were placed was also found to impact the losses associated with passive components. Flip-chip mounting of passive components showed a significant impact on the simulated structure. The inductor Q-value decreased and a frequency shift could be observed in the resonating structures. The work presented in this thesis provides a foundation for continued development and optimization of future RF SiP technologies.

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A

Appendix 1

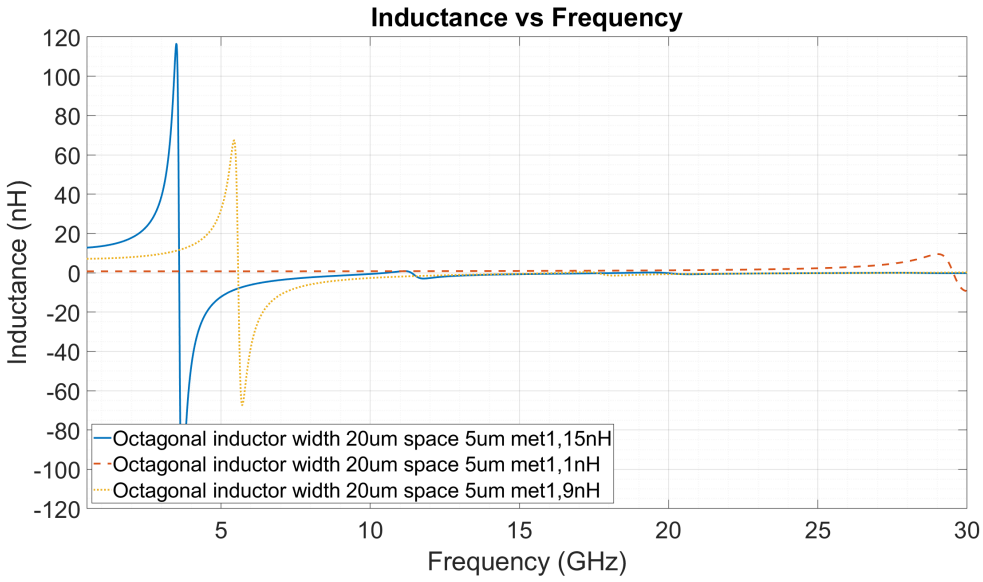

Figure A.1: Inductance for octagonal inductor.

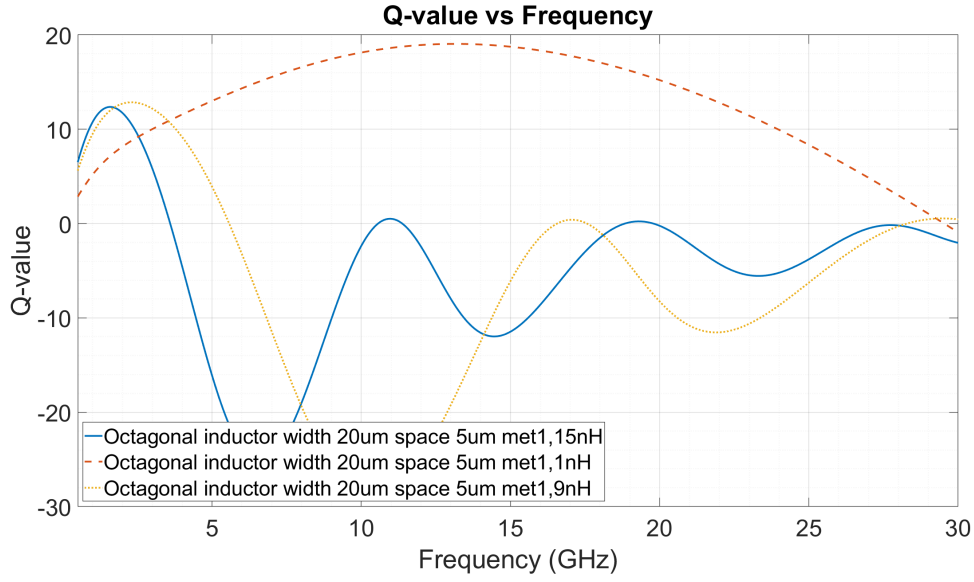

Figure A.2: Q-value for octagonal inductor.

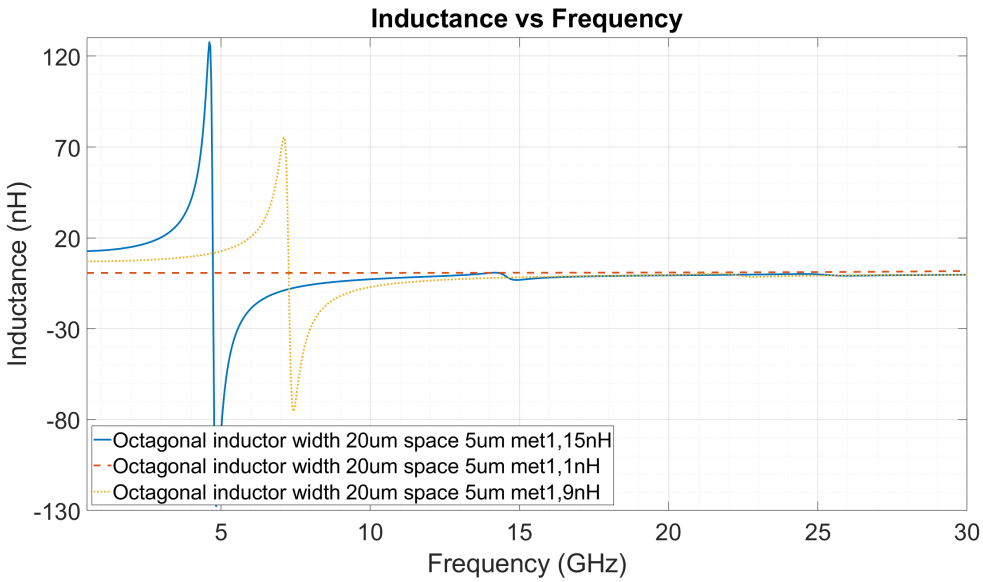

Figure A.3: Inductance for octagonal inductor on a interposer substrate made of glas.

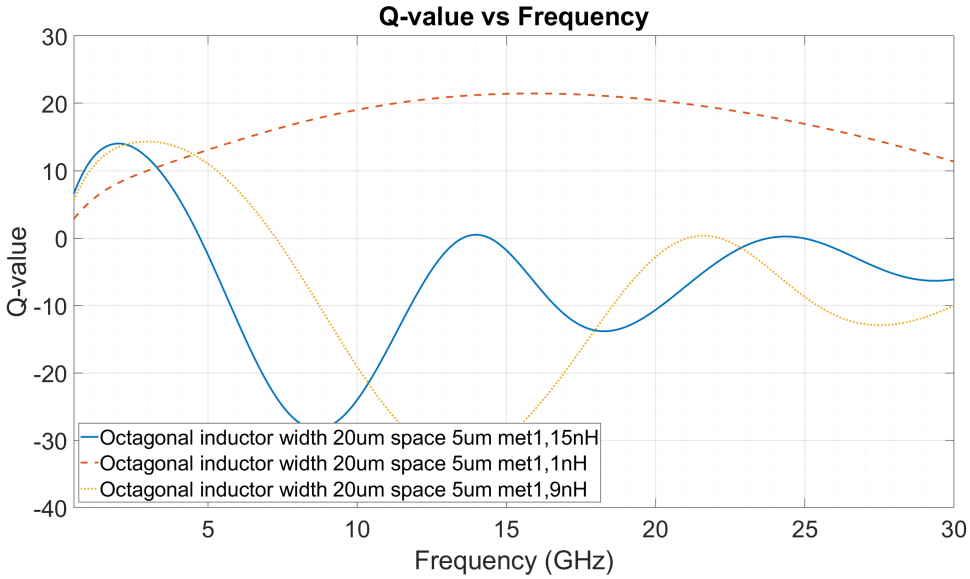

Figure A.4: Q-value for octagonal inductor on a interposer substrate made of glass.

B

Appendix 2

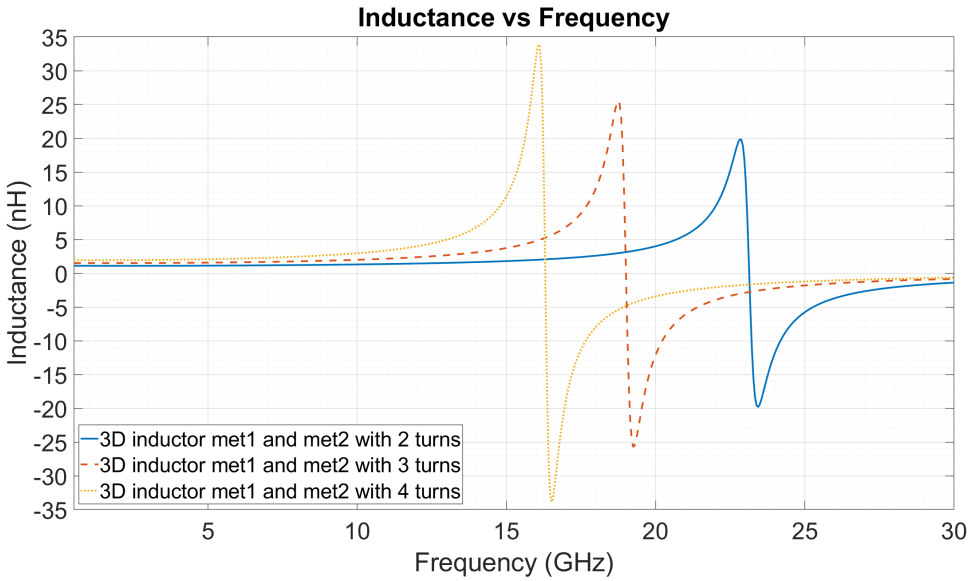

Figure B.1: Inductance for different sized 3D-inductors with met1 and met2 layer with vias tightly spaced.

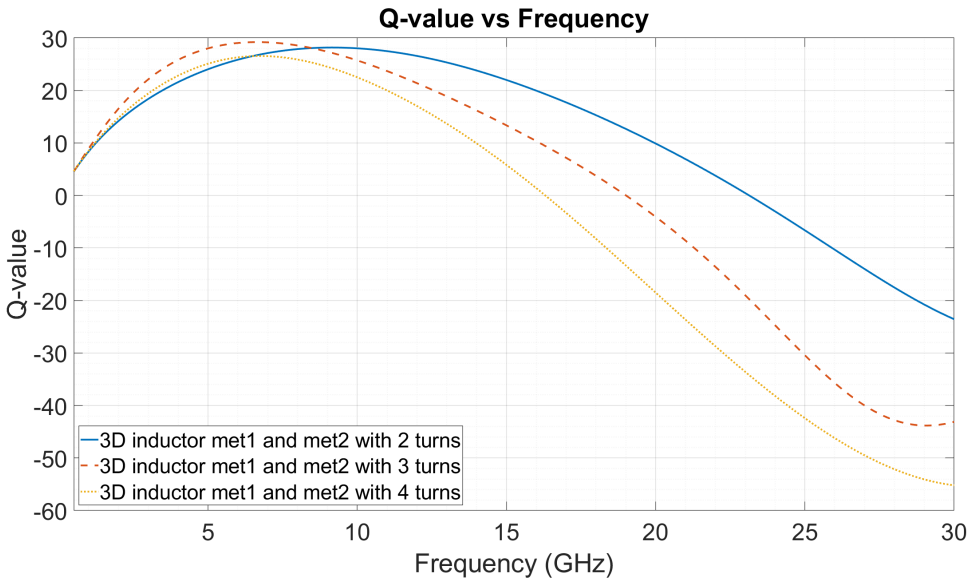

Figure B.2: Q-value for different sized 3D-inductors with met1 and met2 layer with vias tightly spaced.

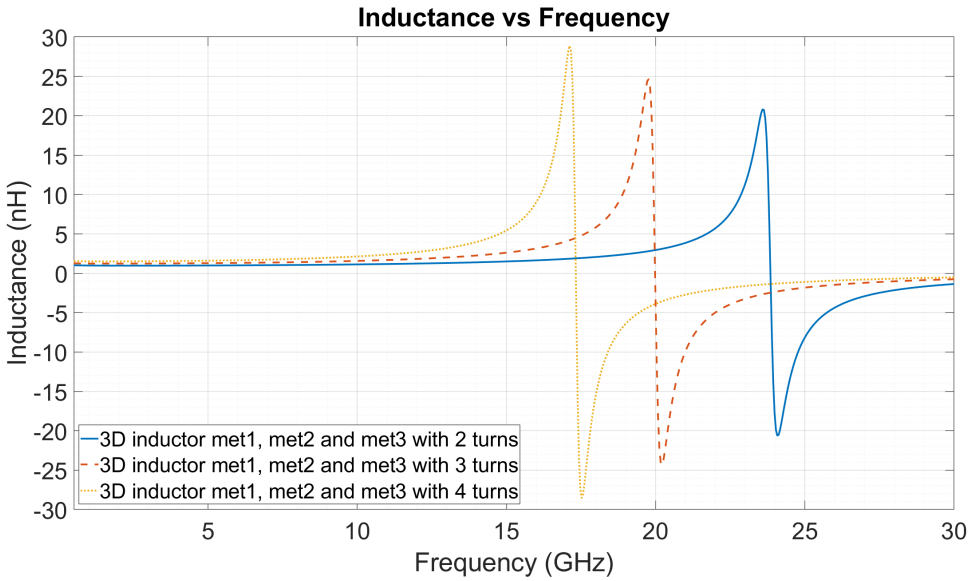

Figure B.3: Inductance for different sized 3D-inductors with met1, met2 and met3 layer.

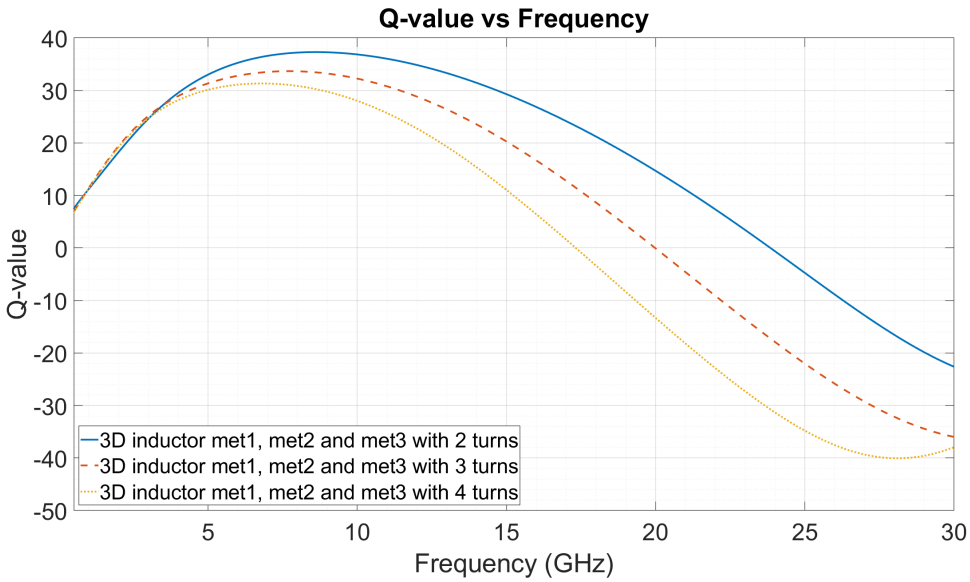

Figure B.4: Q-value for different sized 3D-inductors with met1, met2 and met3 layer.

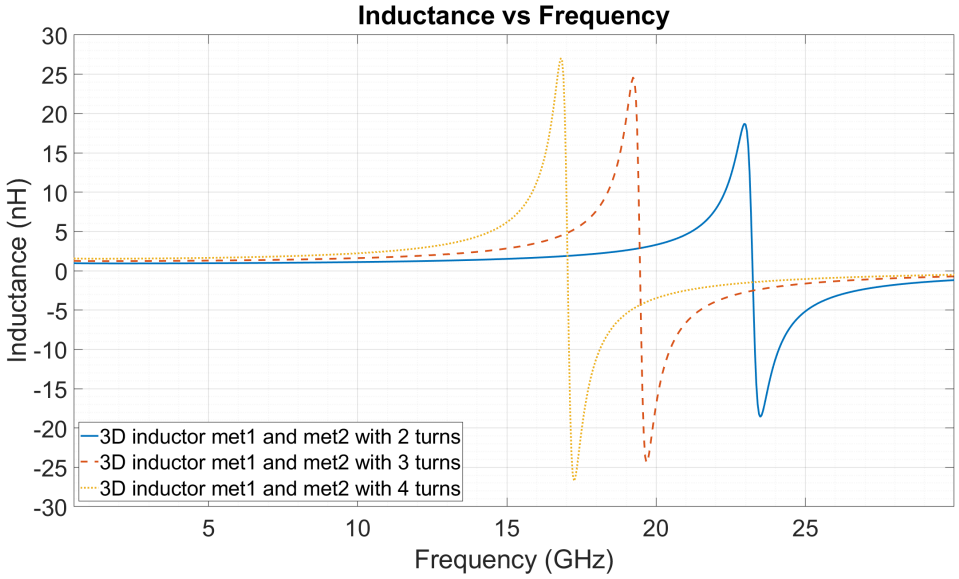

Figure B.5: Inductance for different sized 3D-inductors with met1 and met2 layer.

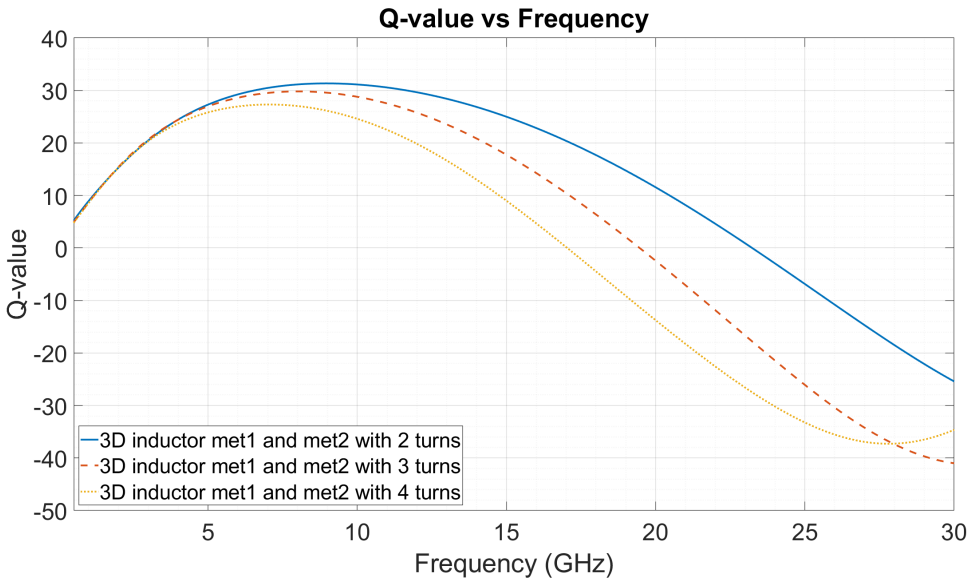

Figure B.6: Inductance for different sized 3D-inductors with met1 and met2 layer.

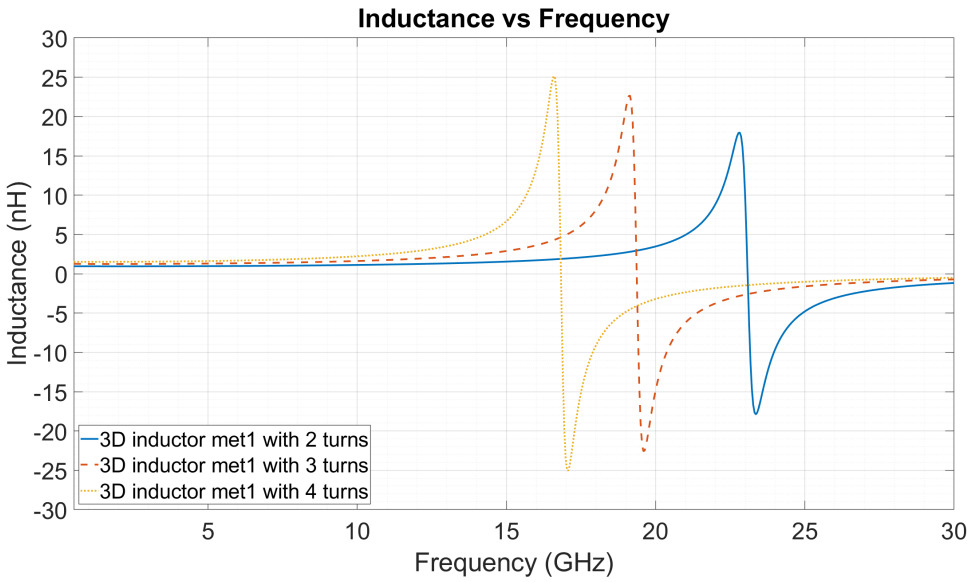

Figure B.7: Inductance for different sized 3D-inductors with met1 layer.

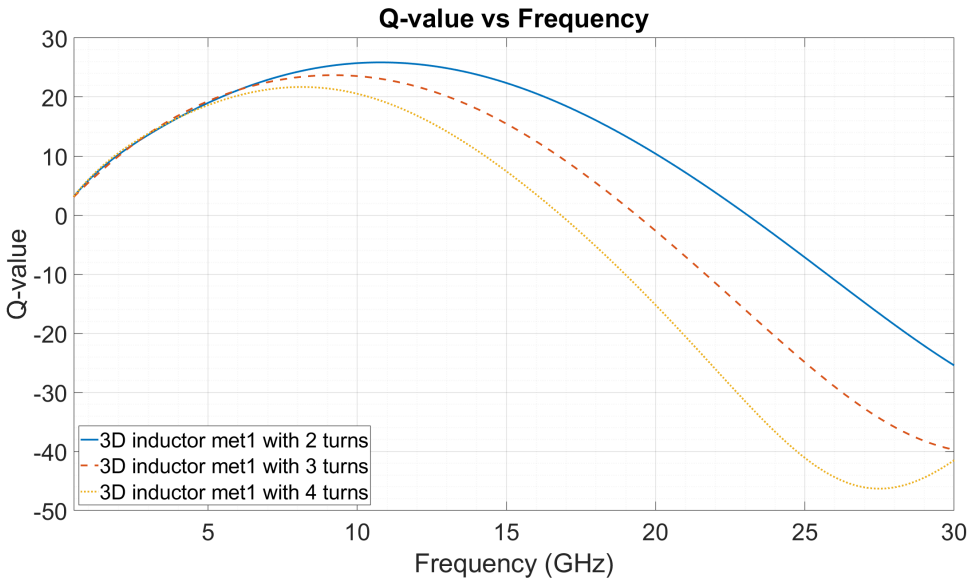

Figure B.8: Inductance for different sized 3D-inductors with met1 layer.

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