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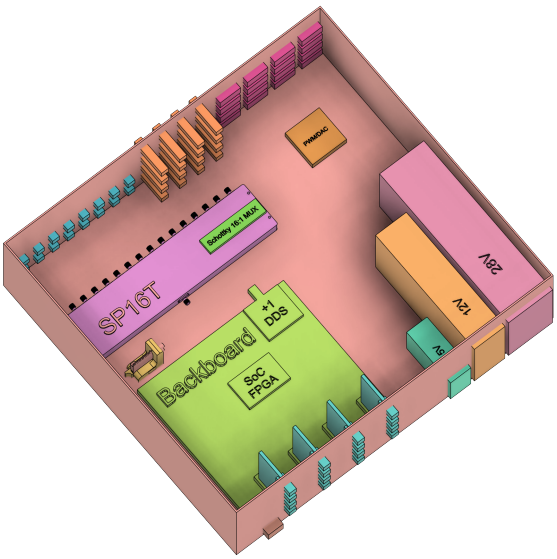

Signal-Generation Hardware for the Next Generation Chalmers Hyperthermia System

Design of a 16-channel Ultra Wideband Phased Array with deterministic Control and Calibration System

Masters project report in Biomedical Engineering

Viktor Olafsson & Gustav Rydner

DEPARTMENT OF SIGNAL PROCESSING AND BIOMEDICAL ENGINEERING

CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2025
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Degree project report 2025

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Cover: An illustrative 3D render of the CHS2 and the components used.

Acknowledgements, dedications, and similar personal statements in this thesis, reflect the author's own views.

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Abstract

Microwave hyperthermia is a promising complementary cancer treatment alongside conventional treatments such as chemotherapy and radiotherapy. By heating a target area to $40 - 44^{\circ}$ C using an antenna array, cytotoxic effects from traditional methods are enhanced in targeted cells. There are multiple versions of hyperthermia but the focus of this thesis is microwave hyperthermia, specifically the Chalmers Ultra Wideband Hyperthermia System. The purpose is to create a more compact version of the first hyperthermia system with frequency control per channel while also keeping correct documentation for future work and regulatory adherence. The project was divided into two phases. The first phase involved analyzing the legacy system to establish the requirements for its successor. This resulted in direct digital synthesis (DDS) being chosen as the new signal generation method and a overview for a 17 DDS-based system, alongside extra designed parts for control, calibration and amplification. A Quality Management System was also set up within the documentation for potential future work on the system. This newly developed system would be more compact, have a higher phase-shift resolution while incorporating frequency control per channel. The second part of the project consisted of validating and testing the DDS using a third party DDS Shield for Arduino Mega 2560. By comparing the DDS's frequency accuracy, stability, amplitude flatness and edge quality to the previous analog wave oscillator it was confirmed that the DDS would be a suitable replacement. Finally a Two-Channel Proof of Concept was implemented to prove that two DDS boards could be synchronized using a single reference clock. Although there was a random phase shift between the two boards, it was shown that synchronization was possible as they reliably were able to get in phase with each other. While the current DDS board could be used to replace the wave oscillator of the current system without further changes, there are many future developments available. The main one is to finish up the 17-DDS system hardware and testing it, introducing changes to the calibration system and following up on the regulatory pathway are all possible options.

Keywords: hyperthermia, direct digital synthesis, ultra-wideband, signal generation, phased array, RF, microwave, system design, regulations

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Gustav Rydner and Viktor Olafsson, Gothenburg, June 2025

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

AD	Analog Devices (Company)
ADC	Analog to Digital Converter
BoM	Bill of Materials
CAD	Computer Aided Design
CAPA	Corrective and Preventative Actions tickets
CMOS	Complementary Metal-Oxide-Semiconductor
CPA	Clear Phase Accumulator
CT	Computer Tomography
DAC	Digital to Analog Converter
DDS	Direct Digital Synthesis
ECAD	Electronics Computer Aided Design
EMC	ElectroMagnetic Compatability
FMEA	Failure Mode and Effects Analysis
FPGA	Field Programmable Gate Array
HT	Hyperthermia Therapy
LUT	Look Up Table
LVDS	Low-Voltage Differential Signaling
MDR	Medical Device Regulation
MRI	Magnetic Resonance Imaging
MW	Microwave
OCXO	Oven-Controlled Crystal Oscillator
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PoC	Proof of Concept
QMS	Quality Management System
RF	Radio Frequency
SDR	Software Defined Radio
SFDR	Spurious free Dynamic Range
SoC	System on Chip
SOP	Standard Operation Procedures
SPI	Serial Peripheral Interface
UWB	Ultra Wideband
VNA	Vector Network Analyzer

Nomenclature

Below is the nomenclature parameters that have been used throughout this thesis.

Parameters

f_{err}	Frequency error
σ_f	Standard deviation of frequency
V_{pp}	Peak to Peak Voltage
U	Server Rack Unit (44.45mm)

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Part I

Introduction

1
Introduction

In this chapter we will discuss relevant background, detailing fundamentals of microwave hyperthermia and existing technologies surrounding the field. This chapter will also outline the purpose, goal of this thesis and what limitations apply and the structure of the thesis.

1.1 Background

This section introduces the fundamentals of hyperthermia treatment and presents the existing microwave hyperthermia device developed at Chalmers University of Technology.

1.1.1 Introduction to Radio Frequency/Microwave Hyperthermia

Hyperthermia therapy (HT) in oncology is the medical practice of raising the temperature of cancerous tissues to approximately 40–44°C for 60 minutes to enhance the effectiveness of cancer treatments [1], [2]. At these elevated temperatures, cytotoxic effects from conventional therapies such as chemotherapy or radiotherapy are enhanced in targeted cells. [3], [4]. When combined with these conventional treatments, hyperthermia has been shown to significantly improve therapeutic efficacy. Among the various methods of hyperthermia, this thesis focuses specifically on radio frequency (RF) and microwave (MW) hyperthermia, which offers non-invasive, controllable energy delivery into deep seated targets.

1.1.2 Heating Enhances Cancer Treatment

Raising tumor temperature to 40–44°C for 60 minutes has 3 synergistic effects [2]:

- **Radiation sensitization** - Improved perfusion and oxygenation reduce radioresistance and inhibit the DNA's ability to repair.
- **Chemotherapy sensitization** - Blood perfusion and vascular permeability rises, increases local drug concentration.
- **Immune stimulation** - Recent studies suggest that hyperthermia can boost immune response by inducing an increased production of so called Heat Shock Proteins which carry tumor antigens [5].

Across multiple randomized trials these mechanisms translate into significantly higher complete response rates when combined with conventional treatments vs. when radiotherapy or chemotherapy is used alone[2].

1.1.3 Array-based Energy Delivery

Both RF and MW has an exponential loss in power deposition as depth increases and it is being frequency dependent [2]. There is an inverse relationship between frequency and penetration depth, lower frequencies reach deeper while higher energy deposition frequencies are shallower. To overcome this limitation and heat deep seated targets the use of multiple antennas in an array surrounding the target must be used. Steering the radiation from multiple antennas to facilitate constructive interference in the focal spot, this setup is called a *phased array system*. By adjusting each antenna's amplitude, phase and frequency the individual waves interfere constructively at the tumor center and destructively elsewhere, producing a spatially confined SAR "hot spot".

The technique utilizes RF/MW phased arrays to focus energy on tumors in a non-invasive manner. Typically, the patient is surrounded by a circular array of applicators that emit RF/MW signals. These signals are engineered to interfere constructively at a specific region, known as the focal spot, thereby delivering the highest energy concentration at the tumor site. This focused energy delivery results in a localized rise in temperature at the tumor, while minimizing heating of surrounding healthy tissues.

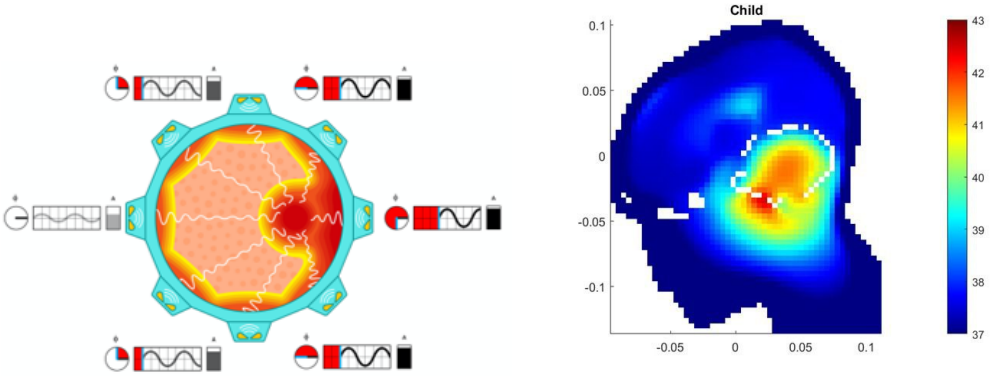


Figure 1.1: Left shows how a phased array of antenna can be used to induce a focal spot of concentrated energy used to heat up a tumor. Right is a simulation of a tumor outlined in white being heated inside the head of a child. Images courtesy of Dobsicek Trefna & Nilsson

Since tumors vary in size and location, it is imperative that the focal spot needs to be dynamically adjusted to effectively target different anatomical configurations. This is achieved by individually controlling the phase, amplitude, and frequency of the signal emitted by each antenna in the array as can be seen on the left in figure 1.1. By fine-tuning these parameters via treatment planning algorithms, tumors of

different sizes and locations can be effectively targeted while minimizing harm to surrounding healthy tissue.
Biological tissue behaves like a *lossy dielectric* [2]. When applying a oscillating EM field at RF/MV frequencies, typically ranging from 70 MHz to 915 MHz, to tissue it gets partially absorbed. Polar molecules under RF/MW frequencies rotate rapidly attempting to align with the field. This kinetic energy in turn causes friction from rotation and dissipates as heat effectively converting EM energy into heat.

The EM field generated by an array of antennas can be computed using Maxwell's equations [2]. These are often approximated for EM fields in biological tissue. Using this approximation of field strength can produce the quantified heat dissipation using the Specific Absorption Rate (SAR). SAR details the power absorbed per unit mass and depends on the constitution of the tissue being heated.

1.1.4 Treatment Planning and Optimization

Careful planning of the treatment is required for each treatment. It involves computer simulations to optimize and predict the treatment[2]. This usually involves patient specific CT/MRI models to and mapping out specific dielectric properties to different tissue to produce dielectric maps. These are then used in optimization routines to calculate parameters to maximize the tumor to focal spot SAR ratio. The treatment plan also needs to account for thermal diffusion and the cooling effect that blood flow can have on a tumor and using bio heat equations to account for that.

1.1.5 Legacy Microwave Hyperthermia System

Researchers at Chalmers University of Technology have developed a prototype microwave hyperthermia system, hereafter referred to as CHS1. Its a 16-channel ultra wideband (UWB) microwave hyperthermia device [6]. The device relies on a single wave oscillator whose output is divided into 16 separate paths. Each path is individually phase-shifted and amplified before it reaches the applicators, ensuring and limiting so that every channel operates at the oscillators fixed frequency. As it stands the device is currently at Chalmers University, but is planned to be moved to Sahlgrenska University Hospital for future clinical validation. A simplified schematic of the system is shown below in figure 1.2

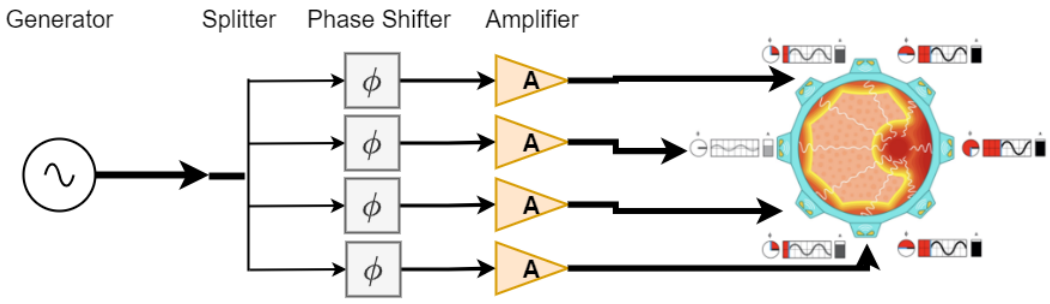


Figure 1.2: Simplified overview of 16-channel ultra wideband hyperthermia system. Figure courtesy of Nilsson.

Figure 1.3 below shows the current iteration of CHS1 in greater detail. It uses a manually operated analog wave generator (Agilent, HP8350B Sweep Oscillator Mainframe) which generates a RF-signal into 50Ω impedance co-axial cables (Harbour, SFL402-105FLEX). The signal is then split up into one main signal and one reference signal. The main signal is then amplified by a low noise amplifier (Minicircuits, ZFL-1000VH2+) before being split into 16 different signals (Pulsar Microwave, P16-05-456/1S). Each of these main signals then has its phase shifted by a phase shifter (SY89297U Evaluation board) before being amplified by two different amplifiers, one low power amplifier (EMPower RF Systems, 1043-BBM2C4AAJ) and one high power amplifier (Bruco Broadband High Power Amplifier). The signal gets coupled which means taking a sub-part of the main signal and sends it to the control part of the system before the main signal travels to the antennas. When the main signal reaches the antennas a reflected signal is created back into the system. This reaches the same coupler as before where it then travels into a zero bias Schottky detector (Eclipse, EZM0120A3) which detects amplitude convertes it into a voltage. This voltage is then sent to the control system which shuts down the system if the reflected signals amplitude reaches too high.

The control system is mainly centered around two parts, one Arduino Mega 2560 and 16 gain- and phase-detectors (Analog Devices, AD8302). AD8302 takes the forward signal and the reference signals as input and outputs the difference in phase and gain between the two as voltages. The reference signal first has its phase shifted by two 8-bit digital phase shifters (Pulsar Microvwave, DST-101-480/1S), which helps with calculating the phase difference which AD8302 outputs, before being split into 16 using the same splitter as the main signal. This is then input into AD8302 alongside the coupled forward signal with the output then being fed into the Arduino. The Arduino then measures the phase and gain difference and sends out control signals to the main signal phase shifter and low power amplifier.

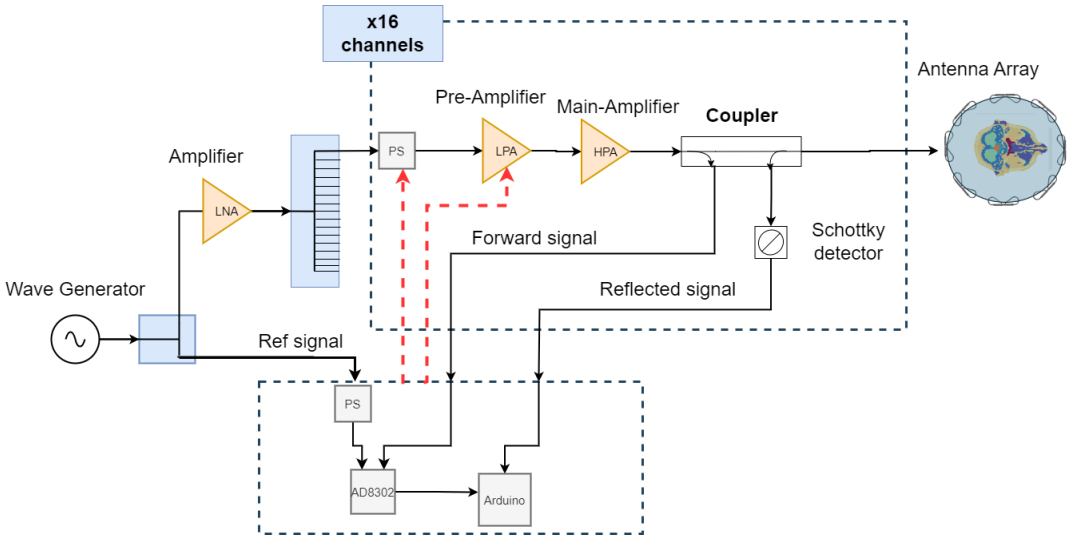


Figure 1.3: Old system layout before redesign

1.2 Purpose and Goals

This thesis aims to design a 16-channel UWB RF/MW phased array with independent channel control and embedded calibration functionality, hereafter referred to as CHS2. Its purpose is to be the next generation HT system to be used at Chalmers. The main goal of CHS2 is to achieve independent frequency per channel, alongside phase and amplitude control. A secondary goal is to improve upon the existing system by addressing previous limitations and more carefully planning the system as a whole from the outset. The final goal is to facilitate future work on CHS2 by designing the system with modularity in mind while also keeping proper documentation throughout its development. To these ends the goal is to keep detailed record keeping and documentation by applying developing a Quality Management System (QMS) in preparation for Medical Device Regulation (MDR) compliance, as full compliance is beyond the scope of this thesis.

1.3 Scope and Legacy-to-CHS2 Upgrade Map

This thesis focuses on the signal generation hardware for the Chalmers hyperthermia system. This encompasses everything seen in figure 1.3 except for the applicators. The main focus of the project will be the wave generator and the replacement of it to upgrade the systems capabilities. Other components may be subject to smaller changes and some sub systems will be reused in their entirety. The design of the applicators and treatment planning software will not be covered in this thesis. Table 1.1 summaries which CHS1 subsystems fall inside this thesis scope and their planned disposition in CHS2. Detailed architectural and validation results appear in Parts II–III; 1.1.

Table 1.1: CHS1 subsystem inventory and disposition in the CHS2 architecture.

Subsystem	**CHS1 Implementation**	**Status in CHS2**	**Rationale / Action**
Wave Generator	HP8350B	*Replaced*	Per-channel synthesis enables independent f, ϕ, A control.
Amplitude control	PWM to Amplifier	*Modified*	New controllers; same PA hardware.
Power amplifiers	53dB Ca. 200W	*Retained*	Meets power / bandwidth targets.
Applicators	16 antennas	*Retained*	Untouched.
Calibration detectors	Per-channel AD8302	*Modified*	Single AD8302 + switch reduces footprint.
Control logic	Arduino board	*Replaced*	Faster controller
Mechanical rack	19", Half a rack	*Modified*	Made more compact.

1.4 Limitations

The following restrictions are relevant to the project to keep it achievable whilst allowing to maintain focus on the core research and design goals.

- Technical Restrictions: The use of evaluation boards and of the shelf hardware vs custom solutions and Printed Circuit Boards (PCB).
- Safety and Regulatory Restrictions: Working within the safety constraints imposed by Chalmers and taking into considerations MDR compliance.
- Resource and Time Constraints: Working with available lab equipment and facilities as well as taking into considerations the time scope of the project, as it might limit the ability to iterate due to wait times of shipping.
- Scope and Complexity: Considerations must be made for the intended scope and complexity so that it falls within reasonable limitations for a masters thesis. Full MDR compliance is out of scope but QMS groundwork is laid.
- Budgetary Constraints: When developing the device, compromises have to be made to balance different options so cost and performance.

1.5 Layout of the Report

To help guide the reader through the multidisciplinary material, the thesis has been organized into *four separate parts*. From clinical motivation, through design, to practical validation/verification and finally critical reflection and summary. The structure can be seen in the table of content or briefly summarized in the list below:

Part I – Introduction **(Chs. 1)**
Establishes the clinical background of microwave hyperthermia, introduces the first-

generation CHS1 system, states the thesis goals and limitations.

Part II – System Architecture and Design (Chs. 2–4)
Presents the conceptual leap from a single-frequency CHS1 to the multi-frequency CHS2. Chapters 4–6 guide the reader from requirement derivation through block-level architecture to concrete PCB and mechanical layouts and covers out the regulatory context. Chapter 7 discusses expected benefits and trade-offs.

Part III – Hardware Validation and Testing (Chs. 5–7)
Documents the laboratory methods used to validate the chosen signal sources and details the use of a proof-of-concept, providing quantitative evidence for frequency accuracy, phase coherence, and power handling. Limitations observed here directly motivate several design choices in Part II.

Part IV – General Discussion and Conclusion (Chs. 8–9)
Synthesizes lessons learned, outlines how CHS2 can already enhance CHS1, and maps out the remaining work towards a clinical-grade system, including regulatory and quality-management road-maps.

Parts II and III serve to be self contained sections with their own respective introductions, backgrounds, theories, results and discussions. This serves to separate the thesis into two distinct narratives for clarity. Keeping the evidence focused to respective part and helps readers find material most relevant to them.

Part II

System Architecture and Design

2

CHS2

Building upon the knowledge and experience gained from CHS1, the proposed CHS2 introduces a significant architectural evolution aimed at enhancing treatment flexibility and potentially improving therapeutic outcomes. The main difference between the two versions is that the CHS1 generates only with one signal source split across all channels, constraining the system to only be able to operate at one frequency for all antennas at a time during treatment [6]. CHS2 is conceptualized with 16 independent signal generating channels. This fundamental change introduces another degree of freedom in treatment planning which allow for independent control of not only amplitude and phase but also frequency of the 16 channels.

Figure 2.1 shows a conceptual framework block diagram for a multi frequency system. Notably the system has 16 separate signal sources and an additional *+1* channel to be used as a reference signal for calibration and control purposes to close the feedback loop. Many parts of the original CHS1 will be reused in the CHS2 design, such as the amplifiers and applicators as the redesign of these components lie beyond the scope of this thesis.

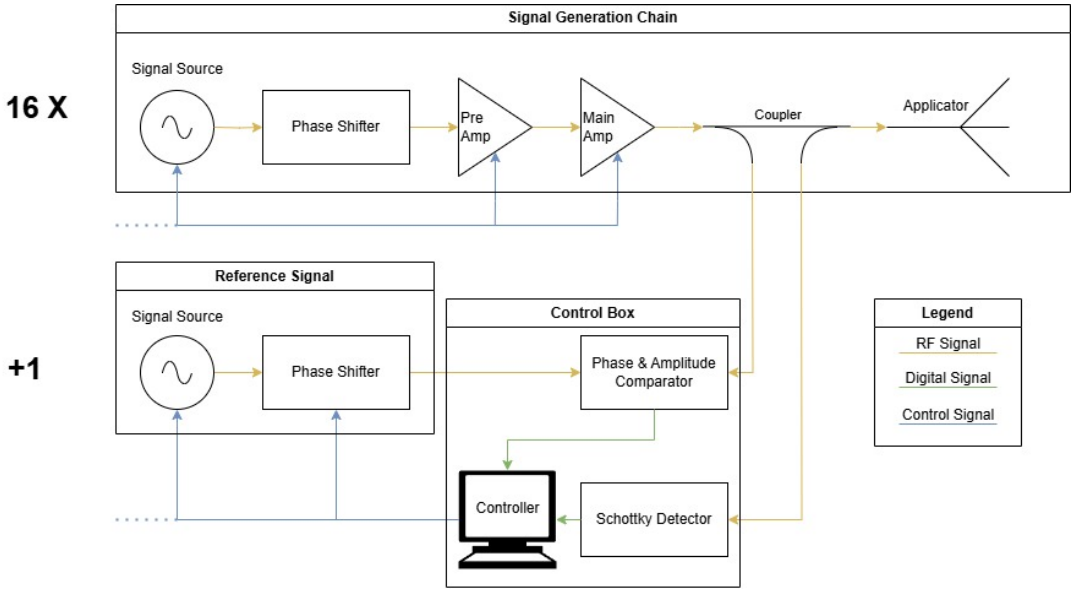


Figure 2.1: Illustrative block diagram of a system with independent signal sources for each channel

2.1 Independent Frequency Control

The theoretical motivation behind adopting independent frequency control per channel stems from the potential to overcome limitations inherent to single frequency phased array systems. By utilizing multiple frequencies CHS2's architecture will open up the door for more sophisticated treatment strategies. It can also allow for better focusing of the focal spot and better more advanced beamforming capabilities [6], [7]. It can also potentially allow for better performance on complicated treatment sites such as the head and brain [8], [9]. It has potential to help overcome penetration depth vs. resolution tradeoffs, as lower frequencies generally offer greater penetration depth, whilst higher frequencies provide better resolution but shallower penetration. The CHS2 could offer a middle ground between this to optimize for depth and focus simultaneously by using different frequencies on different antennas. Although this could incur serious development efforts to solve for complicated algorithms and optimization strategies to get the best treatment plan.

2.2 Signal Generation

The signal generating block is central to the system. It must provide each antenna with spectrally pure and phase predictable RF power. This was achieved using a single synthesizer in CHS1, whose output was subsequently split and each channel is amplified. However CHS1 cannot be converted into CHS2 by adding more independent signal oscillators. Transitioning to CHS2, a system where each channel has a corresponding synthesizer, means synchronization features and more focus on signal integrity are needed for precise waveform super positioning inside of tissue [2]. As a result, nanosecond scale timing errors can directly translate into errors in the dimension or position of the focal spot.

2.2.1 Phase Coherency

When independent RF oscillators are used, they free-run with arbitrary initial phases upon power-up. Even small frequency mismatches between oscillators lead to continuous relative phase drift over time. Since precise hyperthermia requires stable and deterministic phase alignment across all channels, this drift prevents reliable spatial control of the heating pattern.

2.2.2 Startup Determinism and Architectural Implications

What is then required of the CHS2 system is the ability to achieve deterministic phase sync, with a stable phase relationship between each channel. To these means each synthesizer must support deterministic phase reset. This ensures that programmed phase patterns are repeatable. To be able to add more signals sources three conditions must be met that each necessitates their own subsystem:

1. **Common Reference** - Each signal source will have to share a common reference delivered by a **distribution network** with sub picoseconds skew.

2. **Synchronization Logic** - To align phase accumulator resets.
3. **Firmware** - That helps monitor and compensate for errors to maintain a stable phase relationship.

When these three conditions are fulfilled do the possibilities for multi source, independent frequency and phase adjusting become safely exploitable. The remainder of this section will survey three candidate technologies that can deliver on the outlined conditions:

- **Analog Phase-Locked Loops (Analog PLL):** Using an input refrence signal an analog PLL is designed to generate an output signal whos pase is locked on to the refrence [10]. It accomplishes this by being a feedback controlled system, where you typically have a Voltage-Controlled Oscillator (VCO), a Phase Detector (PD), a Loop Filter (LF) and often frequency dividers. The PD compares the VCO output phase with the internal refrence, generating an error signal that usually gets filtered and then is used to tune the VCO. This enables the synthesis of stable frequency generation that is integer of fractional multiples of the refrence. Analog PLLs are excellent at generating low phase noise single frequency signals but lack flexibility in frequency synthesis and tuning range.

- **Discrete Digital-to-Analog Converter (DAC) + Field-Programmable Gate Array (FPGA):** This approach uses an FPGA, a flexible and reprogrammable digital chip to enable digital signal processing [11]. The FPGA computes and generates the desired waveform as a sequence of digital samples. This digital sample sequence is then sent to a DAC, preferably of high speed and resolution to be converted into an analog signal based on a precise clock. This method offers outstanding flexibility in regards to generating complex and arbitrary waveforms. This comes at a higher complexity cost in regards to hardware design and interfacing.

- **Direct Digital Synthesis (DDS):** DDS is a digital based technique for generating analog waveforms [10]. Using a stable clock it is primarily used to generate sine waves. A core component of the DDS is a phase accumulator, which increments its digital value based on a frequency tuning word at each clock cycle. The digital phase value then typically addresses a lookup table (LUT) to retrieve the corresponding waveform amplitude sample. Using a built in DAC, it then converts these digital samples into the final analog output. DDS technology provides extremely fine frequency and phase resolution. It is also suitable for very fast switching between frequencies and phases, making it suitable for applications requiring high agility.

These three technologies represent distinct methods for generating the required microwave signals, each with its own set of advantages and disadvantages relevant to the hyperthermia application. A detailed comparison outlining key performance aspects is presented in table 2.1.

Table 2.1: Comparison of Analog PLL, Discrete DAC+FPGA, and DDS for Wideband Microwave Hyperthermia Signal Generation

Aspect	**Analog PLL**	**Discrete DAC + FPGA**	**DDS**
Operating Principle	VCO locked to stable reference via fractional/integer division	Digital waveforms generated in FPGA, converted to analog by high-speed DAC	Phase accumulator, LUT, and on-board DAC generate precise waveforms from a reference clock
Frequency Range	Up to multiple GHz with appropriate PLL and VCO selection	Limited by DAC sampling rate and output bandwidth; can be extended via up-conversion	Typically hundreds of MHz to a few GHz, depending on the specific DDS IC and clock speed
Tuning Resolution	Determined by reference frequency and division ratios; fractional-N offers fine steps (Hz or sub-Hz)	Very high; determined by DAC resolution and digital precision within the FPGA (sub-Hz possible)	Extremely fine (sub-Hz); limited primarily by the number of bits in the phase accumulator
Tuning Speed	Moderate to fast (typically μs range settling time); lock time depends on loop bandwidth	Potentially very fast (ns to μs); limited by FPGA update rate, interface speed, and filter settling	Very fast frequency/phase hopping (typically ns range) once registers are updated
Phase Noise / Spurious	Generally good phase noise close to the carrier, potentially worse far out. Fractional-N can introduce spurs.	Highly dependent on reference clock quality, DAC performance (linearity, noise), and power supply purity. Careful filtering often required.	Generally good phase noise profile. Can exhibit discrete spurs due to DAC non-linearities and phase/amplitude quantization.
Complexity	Relatively lower hardware complexity, especially with integrated PLL modules. Loop filter design is critical.	Higher complexity involving high-speed digital design (FPGA), mixed-signal layout (DAC), clocking, and potentially complex software/firmware.	Moderate complexity; often available as integrated circuits requiring careful layout and clocking, but less flexible than FPGA approach.
Waveform Flexibility	Primarily generates single-tone (sine wave) signals. Limited modulation capabilities possible.	Extremely flexible: arbitrary waveforms, multi-tone signals, complex modulation (AM, FM, PM), real-time signal generation.	Primarily generates sine waves. Some DDS ICs offer limited modulation or basic waveform shapes (triangle, square). Excellent for fast frequency/phase switching.
Cost / Availability	Moderate cost for components. Wide variety of integrated circuits and modules available.	Higher cost due to expensive high-speed DACs, capable FPGAs, and increased development effort.	Moderate cost for DDS ICs. Availability depends on required performance specs.

2.3 Phase and Amplitude Measurements

While accurate per-channel knowledge of both RF phase and amplitude is essential for converting raw microwave power into a controllable thermal focal spot, several factors complicate this task. Even after phase alignment of the signal sources using the methods described in section 2.2.2, multiple components can alter both the phase and amplitude before the signal reaches the applicator. Every coaxial cable and splitter introduces a constant phase shift that can be corrected during calibration. In contrast, active components such as high-gain power amplifiers add frequency-dependent gain ripple and phase offsets that drift with temperature and supply voltage, making calibration more challenging. Unless these effects are continuously measured and compensated, the signals at the applicator array will deviate from the intended treatment plan in both phase and amplitude, preventing the formation of a precise focal spot. A closed-loop feedback system is therefore mandatory for both CHS1 and CHS2.

3
Design Process

This part the of the method will cover how the requirements for the CHS2 were derived and what they are based on. After that the chapter covers the tools and processes used for the creation of the design for CHS2.

3.1 Requirements Derivation

This chapter explains how the concrete requirements collected and presented in section 6.1 and 6.3 were produced. Rather than simply listing numbers, it focuses on the process that turned wishes of project supervisors, safety constraints and regulatory obligations into the measurable specifications that underpin every later design decision.

3.1.1 Guiding Philosophy and Applicable Standards

The derivation approach is risk based and evidence driven. There are three main pillars that guided every decision that can be seen in table 3.1:

Table 3.1: Guiding pillars used in the requirement-derivation process

Pillar	**Key references**	**Why it matters**
Clinical effectiveness & patient safety	Head/neck hyperthermia literature, historic CHS1 performance data	Requirements must ensure CHS2 can form a predictable focal spot without overheating healthy tissue.
Regulation & quality	EU MDR 2017/745, ISO 13485 QMS, IEC 60601-1 safety, IEC 62366 usability	We keep only requirements that we can later verify and justify to a notified body.
Feasibility & life-cycle cost	CHS1 maintenance logs, component availability and Sahlgrenska installation constraints	Ambitious targets are useless if they render the prototype unbuildable, unserviceable, or unaffordable.

3.1.2 Methodological Framework

The requirement derivation workflow was implemented as a 5-step loop. The table 3.2 summaries the inputs, core activities and outputs associated with every step.

Together this loop was used to derive the requirements for the CHS2.

Table 3.2: Five-step methodology used to derive hardware, software, and documentation requirements

Step	**Inputs**	**Activities**	**Principal outputs**
1. Project supervisor questioning	Interviews and meetings with Hana Dobsicek Trefna & Robin Nilsson, CHS1 documentation	Use-case scenarios, pain points, wish list	Functional needs list
2. Regulatory landscape scan	MDR and other relevant standards	Identification of relevant and applicable regulations and standards	Compliance framework
3. Functional decomposition	System block diagram, use-cases diagram	Partitioning into relevant subsystems	Subsystem boundaries
4. Benchmark & gap analysis	Literature, CHS1 measurements and other existing devices	Quantitative targets for phase, frequency etc.	Performance envelopes
5. Requirement formulation	Results of Steps 1–4	Translate to concrete requirements (e.g. *phase error* $\leq$ *5°*, *freq 100–1000 MHz*)	Draft requirement set

3.2 Design Methods

The design and development of the CHS2 system followed a structured and iterative design process, with the purpose and aim of systematically translating defined functional requirements into a well defined and implementable hardware solution. This multifaceted process leveraged a combination of visual planning tools, organizational structure, computer aided design (CAD) and electronics computer aided design (ECAD) techniques to manage complexity, facilitate informed decision making and ensure a robust final design. The tools used for conceptualizing the system architecture through block diagrams, 3D modeling and more and the methodologies employed for validation, organization and documentation will be detailed in the following subsections.

3.2.1 Block Diagram Design

Clear visual representations are crucial for effectively designing, communicating and documenting complex systems such as the CHS2. Block diagrams and conceptual figures were employed extensively throughout the design process, to visualize the system architecture, map component interactions and illustrate signal flow. To this extent the free web based diagramming tool Draw.io was utilized for the creating of visual aids because of its flexibility, collaborative functionality, accessibility and ease of use. Using Draw.io enables the design of comprehensive diagrams of various detail levels, such as high level system diagrams, subsystem block diagrams and signal and control flowcharts. It provides a mean to greater understanding of a complex multilayered system by allowing to easily break down and iterate on diagrams in a collaborative manor. It contributes to the clarity of the design process and quality of the resulting documentation.

3.2.2 3D Modeling for Hardware Layout and Prototyping using 3D printing

CAD allows for 3D modeling of various components and parts of the system. This enables visualization for better understanding and planning of the project. 3D modeling enables the feasibility to try out and plan the layout of components in an constrained environment such as a standard server rack to verify feasibility before committing to ordering anything. 3D modeling can be used in conjunction with 3D printing to enable rapid prototyping and production of custom design solutions to problems the might arise when working with integrating existing and custom designed components.

4

System Requirements and Architecture

This chapter introduces the system requirements and design considerations. This is then followed up by the proposed architecture for the CHS2 going over each major system-block before introducing block diagrams with the design.

4.1 Requirement, Specifications and Design Consideration

4.1.1 Frequency Range

The signal generating hardware must be able to operate within a frequency range of 100-1000 MHz. This constraint is dictated by existing components being compatible with it such as the amplifiers used as well as considering future improvements to the system hardware. This frequency range covers the applicable range of the current amplifiers and applicators while still increasing the potential bandwidth of the system for future applications. It also covers most conventional hyperthermia frequencies.

4.1.2 Output Power and Gain

The existing power amplifier stage is designed to amplify a 0 dBm input signal up to a maximum output power of 53 dBm. So the signal source should output at 0 dBm to ensure compatibility with existing hardware as the amplifier stage will be reused from CHS1. Operating at 0 dBm simplifies calculations and reliability with the rest of the system.

4.1.3 Channel Count and Control

Channel count is to remain the same as CHS1 at 16 for CHS2 while employing a flexible design allowing it to still work with a smaller amount of channels. A smaller scale platform of 8 channels is a preliminary target as it is a sufficient array of applicators to perform basic targeting of tissue to heat for aiding in prototyping and testing. The intent is to scale up the channel count to same number as CHS1 of 16 at a later date and considerations will be made as to the modularity. CHS2

should be able to control each channels frequency, phase and amplitude. Fulfilling this requirements serves multiple objectives:

- **Phase Coherence:** Establishing and maintaining a known phase relationship between channels ensures the ability to reliably create positive or negative interference patterns.
- **Amplitude Control:** High resolution amplitude adjustments on each channel allow to better selectively deposit power into a targeted focal spot.
- **Spatial and Frequency Control:** Independent channels and frequencies allow for precise shaping of electromagnetic fields within the patient's tissue for improved tumor targeting accuracy.

4.1.4 Accuracy and Performance metrics

To successfully operate a microwave hyperthermia system, particularly a phased array system like CHS2 it is critically dependent to have precise and accurately controlled signals for each channel. Accuracy in amplitude, phase and frequency directly impact the ability to form a focused thermal spot. Accuracy is also important for mitigating unintended heating of surrounding healthy tissue. Therefore stringent accuracy and performance metrics are essential requirements of the signal generating hardware.

The system should be able to meet specific accuracy targets to ensure therapeutic efficacy and safety. Based on recommendations, experience with the CHS1 and research in the field, the following constraints are considered:

- **Amplitude Accuracy**:
  The AMC-8 an existing RF 8 channel hyperthermia device has an absolute deviation of 10W for amplitude [12]. In relative terms for CHS2 since the final target amplitude is 53 dBm or approximately 200W a deviation of 10W is equivalent to 5% and will be the primary design goal. This adheres to existing guidelines that recommend a amplitude accuracy of 5% [2][13].
- **Phase Accuracy**:
  The aforementioned AMC-8 also has a phase accuracy of 3° for their 70 MHz system. With CHS2 operating at higher frequencies up to 1 GHz keeping the same level of accuracy can prove to be more challenging. Therefore the chosen design goal for the CHS2 will be 5° to account for UWB capabilities and to align with existing guidelines [2].

Meeting these accuracy and performance metrics necessitates careful component selection, robust calibrations procedures and monitoring and feedback mechanisms within the system design.

4.1.5 Calibration

Accurate phase stability and synchronization of the separate channels is crucial for achieving good performance of the system. This means that a calibration routine is needed for both the signal generator itself and the system as a whole.

For calibration of the system as a whole some sort of gain and phase comparer is needed, such as AD8302 used in CHS1. This is needed as multiple different components have different frequency dependent phase and amplitude shifts between multiple copies of themselves meaning each channel will need to be calibrated individually.

4.1.6 Physical Form Factor

The current CHS1 is situated inside of a standard 19 inch server rack. The new hardware should be compatible with a similar standard server rack interface and have a maximum height of 6U which equates to 26.7cm. This is to ensure compatibility with the rest of the system situated in the same server rack as well as to provide enough space to fit and cool all components. Adhering to this standard will also facilitate comparability with the Sahlgrenska shielded room infrastructure.

4.1.7 Modularity and Integration

Similarly to the server rack constraint on the physical form factor, considerations have to be made to ensure modularity and integration with the current system. The components used in the device have to be modular to facilitate maintenance, future upgrades and potential reconfigurations for different applicator arrays.

4.2 Design Considerations

4.2.1 Monitoring and Fail-safes

Attention must be paid towards ensuring proper safety measures towards both the safety of the device as well as the patient. Being able to monitor device activity in a efficient and responsive manner is instrumental in conducting safe operation. Factoring in metrics such as thermals and reflected signals from the applicator and having fail-safes to prevent substantial harm occurring.

4.3 System Architecture Decisions

Designing or redesigning a system requires thorough exploration and careful consideration of available technologies. Alternative approaches must be critically evaluated against defined system requirements and practical considerations. This to ensure that any adopted technology not only meets performance benchmarks but also integrates smoothly, is economically viable and supports future scalability and maintenance.

Based on the analysis of system requirements and design considerations detailed in sections 4.1 and 4.2 a summary of key specifications for essential for CHS2 has been compiled as can be seen in the following table 4.1.

Table 4.1: Key Specifications for the Signal Generation and Amplification Hardware

Specification	**Requirement**
Frequency Range	100–1000 MHz
Signal Source Output	0 dBm (for compatibility with 53 dBm PA stage)
Channel Count	16 channels with independent frequency, phase, and amplitude control
Phase Accuracy	5 degrees
Amplitude Accuracy	5%
Physical Form Factor	19-inch rack mount, maximum height 6 U
Modularity	Swappable components for future upgrades and maintenance
Calibration	Embedded system enabling per-channel phase and amplitude alignment
Monitoring	Thermal, reflected power, and system status monitoring
Fail-Safes	Automated shutdown upon detecting critical faults

4.4 CHS2 Architecture

4.4.1 Signal Generating Technology: DDS

The chosen signal generating technology was DDS. It was selected over a traditional analog PLL not only for its generally high phase and frequency accuracy, but also because it allows rapid adjustment of these parameters, which is essential when using a separate signal generator as a reference. Another advantage of DDS is that it has already been successfully implemented in hyperthermia systems, with promising results [12]–[14].

4.4.2 Amplification: DAC

For the amplification control, DACs were chosen. These were chosen over PWM as the system could be made more compact using them compared to PWM-DC converters by using higher channel DACs. An additional advantage is their ability to reach higher control resolutions than PWN-DC converters.

4.4.3 Feedback Loop

To effectively close the feedback loop and deliver real-time calibration data required by the CHS2 signal chain it has been decided to mostly reuse the hardware that made up the feedback subsystem that was successfully deployed in CHS1. The legacy design has already demonstrated adequate accuracy and stability in trial runs, therefore within the scope of this thesis, a full redesign was considered unnecessary. Instead, the existing hardware will be migrated into the new architecture with slight tweaks to better suit the CHS2 architecture but provide the same functionality.

4.4.4 Structural Improvements

Experience with the CHS1 showed that the SMA connectors on the used AD8302 module often fail under operational tension. A dedicated print in place bracket was therefore designed, see figure 4.1. It features:

- **Mechanical relief** - The SMA contacts are held in place by the bracket, so torsion is transferred to the bracket instead of the contacts.
- **Tool-less service** - A compliant snap-latch permits the detector to be swapped in seconds while also holding it securely in place.
- **Scalable geometry** - The bracket is tileable, an eight slot version of it can easily retrofit into the CHS1 in case of uppgrade.
- **Printability** - Rounded fillets and 45 degree overhangs allow 3D printing in one piece without support, eliminating the screws and three part assembly required by the first generation fixture while retaining structural rigidity.

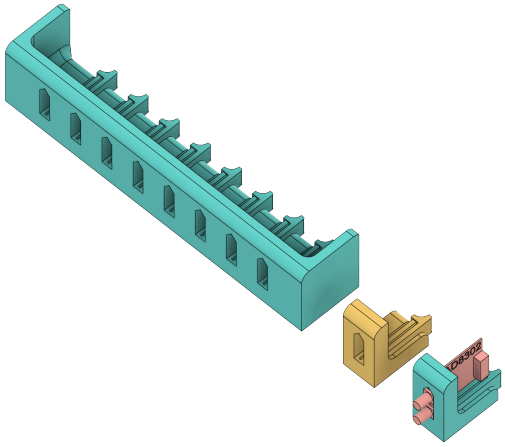


Figure 4.1: Render of a single AD8302 mounting bracket for CHS2 (and eight piece array for use in CHS1)

The complete results of this mounting bracket can be found in the appendix B.

4.5 Component Selection and System Assembly

Component selection is the bridge between the abstract architecture outlined previously and a build-able CHS2 prototype. Each component choice was carefully evaluated for its performance vs. outlined requirements. Parts were reused from CHS1 where they were already proven and new parts were introduced and presented within the scope of the rest of the system. The rest of the section examines the electrical, firmware and mechanical details that turn a parts list into a coherent, rack-mountable CHS2 signal generation device.

4.5.1 The CHS2 Architectural Overview

This chapter presents the complete 16-channel signal generation platform that will drive the CHS2. A top level block diagram is illustrated in figure 4.2, it features color coded arrow to distinguishes between connection types.

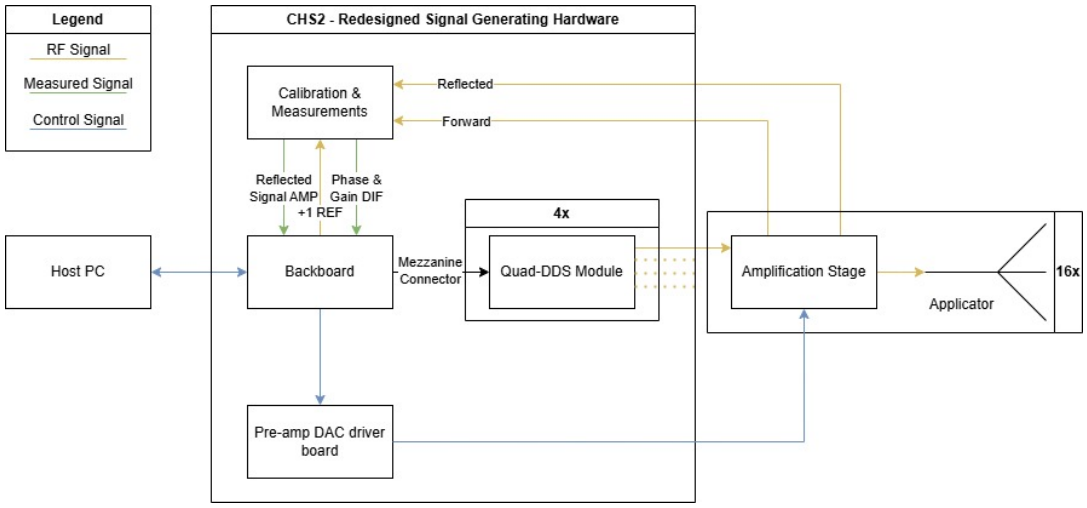


Figure 4.2: Top level block diagram of the proposed CHS2 signal generation platform

CHS2 retains the host PC, amplification stage and applicators from the first generation CHS1. All other features outlined in the figure are either a new design or redesigned. CHS2 was designed with the constraint of a 19 inch server rack enclosure. The new signal generating hardware is realized as four cooperating sub-assemblies:

- **The Backboard** - The backboard serves as the backbone of the system. It carries central processing, distribution of signals across components, generation of REF CLK, hosts the *+1* master DDS for calibration and provides the sole communication link to the host PC.
- **The Quad-DDS Module** - Connected to the backboard via hot swappable mezzanine connector, each containing four AD9915 DDS devices. Up to four quad-DDS modules can be installed, resulting in a maximum of 16 coherent RF outputs that feed the into the amplification stage
- **The Pre-amp DAC Driver Board** - Is a complimentary board used to help the backboard to issue commands to and control each pre-amp for all 16 channels in the amplification stage.
- **Calibration and Measurements** - Using an AD8302 to compare the amplified forwards signal with the +1 reference channel. Digitizing the reflected power via Schottky detector and feeds these values back to the backboard for closed-loop control.

4.5.1.1 Hybrid Backboard/Mezzanine Philosophy

Early design prototypes evaluated two extremes:

1. Using 17 independent DDS cards and connecting everything using wires.
2. An all in one motherboard that hosts every DDS and other components.

The first option offers excellent modularity but introduces risks to timing certainty and is prone to errors from excessive wiring. The second option maximizes electrical performance but sacrifices serviceability and is prone to single point failures necessitating costly board wide rework.

Therefore CHS2 adopts a hybrid approach to the system architecture by creating a system housed on a backboard where one can install separate DDS modules. The advantages of this are:

- Performance critical functions reside on the rigid backboard ensuring sub-degree phase determinism.
- Replicating and isolating separate functions via connectors and mezzanines. A faulty or upgraded quad-DDS module can be exchanged in minutes without disturbing the rest of the system.
- Clear separation of domains simplify iteration: the backboard can be swapped out or upgraded to a newer FPGA or faster reference source while the quad-DDS modules remain unchanged or vice versa.

The remainder of this section expands each block of the block diagram in figure 4.2 into greater detail.

4.5.1.2 Backboard

Accurate timing is paramount to successful operation of a multi channel DDS system. The backboard serves as the timing and control center of the CHS2, see figure 4.3. Every performance critical clock originates from the backboard, as well as every other signal needed for the DDS originates from here and passes through fan out buffers before connecting to the four quad-DDS mezzanines. The System-on-Chip Field-Programmable Gate Array (SoC FPGA) is responsible for all control, collection of measurements, safety feedback and communication with host PC.

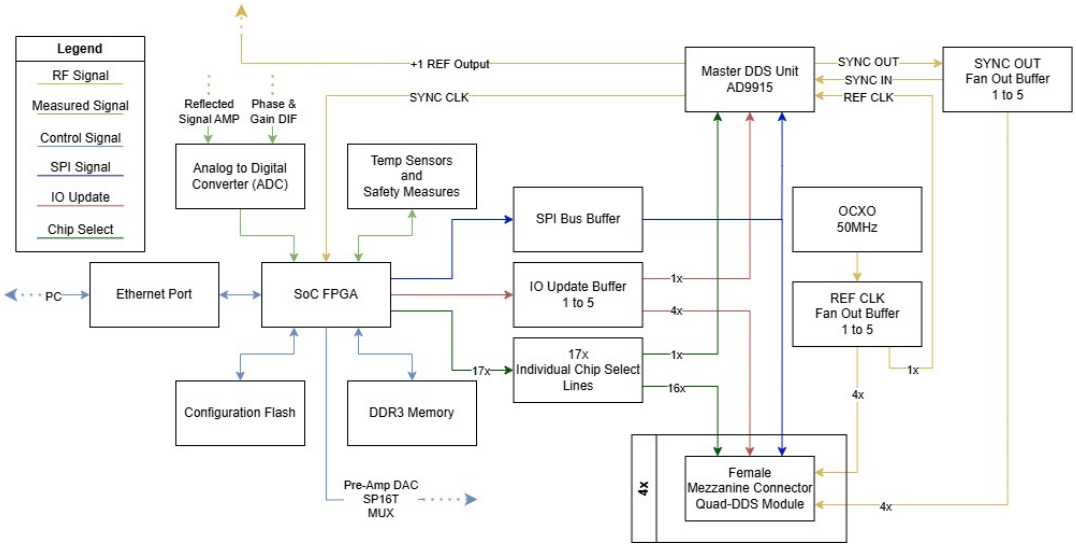


Figure 4.3: Detailed view of the CHS2 backboard

A Xilinx **Zynq-7020** (XC7Z020-2CLG400I) SoC FPGA is equiped with an SoC dual core arm chip allowing for high level control and interfacing with the host PC through peripheral ports such as Ethernet and the FPGA fabric allows for deterministic fast signal distribution and control. The FPGA is fast enough to operate withing strict time tolerances necessary to achieve synchronization. A 256MB or

more of 16-bit DDR3L memory bank delivers suficient bandwidth for waveform tables, detector logging or potential operating system. The configuration flash consisting of a 128MB QSPI flash serves the purpose of storing a potential boot loader, bit stream and Linux root file-system.
The backboard houses the master DDS that serves as the channel *+1* to the other main 16 channels. Its output does not go through any amplification or phase shifting and thus can serve as a base line reference channel for calibration of the other 16 channels. The master DDS outputs SYNC CLK to the SoC FPGA that uses it to time its coincidental IO updates for synchronization as detailed in section 4.3. It also outputs the SYNC OUT signal making it crucial for the synchronous operation of the system as a whole.

The system requires a stable and low-jitter reference clock to ensure deterministic synchronization across all DDS channels. For this purpose, a 50 MHz oven-controlled crystal oscillator (OCXO) was selected. Preliminary tests (see Part III, Section 5.3) demonstrated that using a 50 MHz external clock with the internal PLL achieved performance comparable to driving the system directly at 2.5 GHz. In addition, distributing a 50 MHz clock eases the design constraints on the backboard, since lower-frequency signals are less demanding to route than multi-gigahertz signals.
The quality of the OCXO is directly reflected in the overall system performance, as its output serves as the REF CLK input to each DDS. Consequently, the noise floor of the DDS is directly correlated with the OCXO's performance. To distribute the reference clock, the 50 MHz signal is buffered through a low-noise fan-out stage (1-to-5). Four of these outputs drive the quad-DDS mezzanines, while the fifth is routed to the master DDS.
There are three signals that must arrive at all DDS chips with sub-nanosecond skew:

- **SYNC OUT** - Generated by the master DDS it is buffered in a 1 to 5 fan out and one of the outputs goes back into the SYNC IN port of the master DDS while the other 4 drive the mezzanine connectors.
- **IO UPDATE** - Generated by the FPGA it is routed through a 1 to 5 fan out buffer: 1 goes to the master DDS the rest go to the mezzanine connectors.
- **REF CLK** - Generated by the OCXO, it is fed into a low noise fan out buffer (1 to 5). Four of the outputs drive the quad-DDS mezzanines, the fifth is routed to the master DDS.

Together these signals eliminate random ambiguity and allows for guaranteed deterministic power up phase alignment.
The Serial Peripheral Interface (SPI) bus consists of SDO, SDIO and SCLK, its fanned out to all DDS units through a buffer. All DDS's share the same SPI bus and receive the same broadcast commands through it. Chip select allows for individual DDS control, when the chip select is set to high a DDS is selected to programming. This necessitates that the chip select populates 17 individual pins on the FPGA one for each DDS for granular control capabilities.
Using an Analog to Digital Converter (ADC) to sample the incoming signals from calibration system, such as the differential phase and gain error as well as the amplitude of the reflected signal. The results are streamed to SoC FPGA to be broadcast back to the host PC or used in calibration. Along with the reflected signal am-

plitude the FPGA also receives readings from temperature sensors mounted around the board and system allowing the SoC FPGA to initiate a shutdown sequence when anomalous measurements are detected, such as high temperature or high reflection coefficient. The backboard also exposes pins that allow it to connect to external components to control them such as the pre-amp DAC driver board or the MUX or SP16T used for calibration.

Overall, the backboard implements every element that benefits from tight tolerances and accurate phase alignment. It allows for a convenient single point of maintenance or upgrade, while delegating replicated RF to easily replaceable mezzanine connected modules. This setup safeguards the serviceability without compromising the performance necessary to achieve the targets set in chapter 5.

4.5.1.3 Quad-DDS Module

Each Quad-DDS module takes five different signals as inputs, with three of them passing through fan out buffers before each DDS while two of them goes directly to the DDS. The first signal is the SPI Bus which goes to all four DDS units by splitting up the bus. The second signal is the chip select signal which is four separate signals, each one routed to one respective DDS. Finally the three last signals are the sync out, IO update and reference clock signals. These three all goes into a one to four fan out buffer before the DDS units. This is needed as both of the RF signals (sync out and the reference clock) needs to keep their frequency and phase as close to each other as possible whereas the IO update needs to go through a fan out buffer as to make sure each update signal reaches each DDS as simultaneously as possible. This all results in four synchronized DDS units which each outputs one RF signal to the amplifiers.

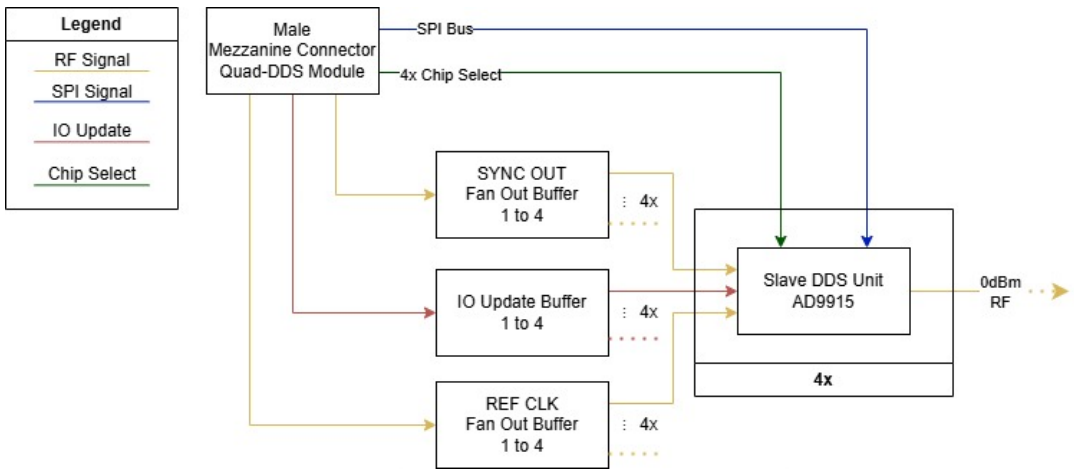


Figure 4.4: Top view block diagram of the proposed CHS2

4.5.1.4 Single Channel DDS Set Up

Figure 4.5 expands on one of the 17 AD9915 DDS's present found throughout the CHS2. Although the DDS chip itself performs the calculation and generation of

the waveform, several analogue peripherals are required to meed spectral purity and synchronization targets.

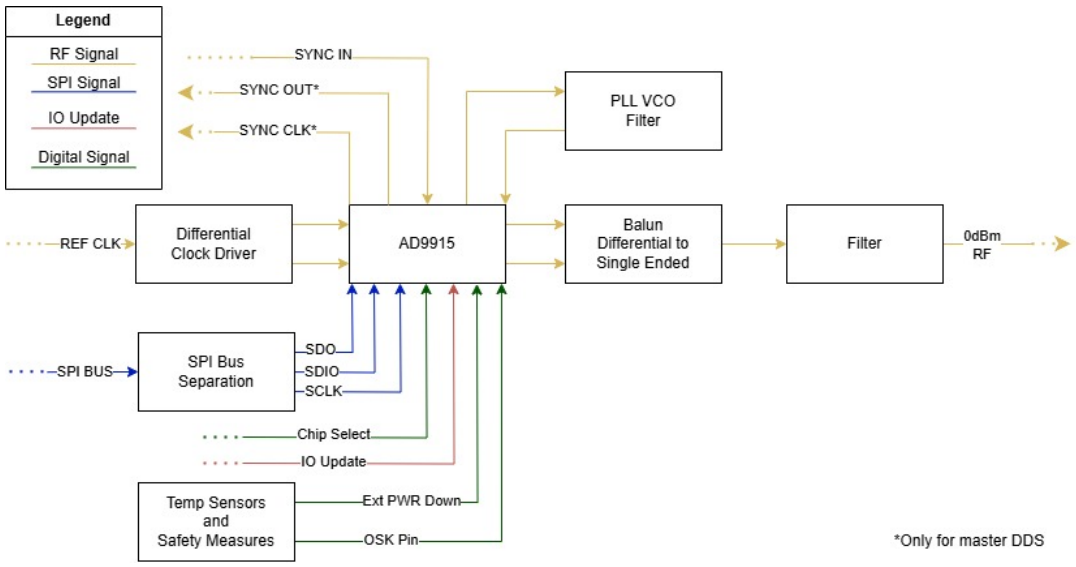


Figure 4.5: Functional peripherals surrounding a single AD9915.

Before entering the DDS, the single-ended 50 MHz REF CLK from the OCXO is converted to a differential signal using the ADCLK925, a low-noise differential clock driver. The driver presents a 100 differential REF CLK, which is terminated at the DDS. Since the AD9915's REF CLK pins are designed as LVDS (Low-Voltage Differential Signaling) receivers, they only meet their timing and noise specifications when driven differentially.
Using the ADCLK925 and differential routing reduces electromagnetic interference (EMI), as single-ended CMOS (Complementary Metal-Oxide-Semiconductor) signaling is more susceptible to crosstalk. Furthermore, the differential driver helps isolate the OCXO from digital noise that could otherwise couple back from the DDS into the oscillator.
When operating at lower REF CLK frequencies and using the internal PLL of the AD9915 to multiply it up to higher clock speeds an external PLL loop filter is required for optimal performance. The filter serves the purpose to enhance stability, faster operation and phase noise containment to keep the REF CLK jitter from being amplified. The filter design was copied from the evaluation board of the AD9915.
The DDS produces a differential RF output, using a 2 to 1 transmission line balun like the Mini-Circuits TC1-1-13M+ to convert it to a single ended 50Ω voltage. This gives us similar benefits as the differential clock driver and the REF CLK signal but for the output. This is followed by a seventh-order elliptic low-pass filter to suppress sampling process artifacts.
Proper synchronization of the AD9915 requires carefully routed and precisely timed SYNC IN and IO UPDATE signals. Only the master DDS generates SYNC OUT and SYNC CLK, while the slave DDS units do not. However, for troubleshooting and fine-tuning the delay registers, the SYNC CLK from a slave DDS can optionally be routed to a breakout pin. All DDS units receive the same control signals via the

SPI bus, but they only respond when their respective chip select line is set high. The AD9915 features two pins of interest that can enable safe operation of the unit. Namely the Ext PWR Down and the OSK pin. Both pins when set to high essentially have the same end result, the DDS ceases to output any signal. The OSK pin can be used to toggle the signal output on and off whilst keeping the rest of the DDS operational and ready for commands whilst the Ext PWR Down put initializes an entire shutdown sequence of the DDS. Propper use of these alongside diagnostic measures such as thermal sensors and measurements from the feedback system will help ensure safe operation of CHS2.

Together these peripherals and control signals allow the raw digital waveform generated inside the DDS core to exit the module as a spectrally clean, phase deterministic 0 dBm carrier, ready for further amplification in the amplification stage seen section 4.5.4, in a safe and effective manner.

4.5.2 Mechanical Layout and Rapid-Prototyping

To verify that the system designed in the preceding sections can be accommodated in a standards enclosure that fits the requirements outlined in chapter 5, a mechanical mock-up was built in Fusion 360. Commercial parts used, power supplies, various ports, SP16T, AD8302, 19 inch chassis and more were replicated and represented by simplified volume models made to taken measurements. The yet to be fabricated components (backboard, quad-DDS modules and pre-amp DAC driver board) were approximated in size and implemented as well. This exercise served two purposes:

- **Spatial feasibility** - The assembly shown in figure 4.6 confirms that all hardware fits in a aproximately 4U (180mm) height, standard 19 inch server rack while also respecting the service corridor demanded by the rack.
- **Front/rear I/O planning** - Power entry, Ethernet for the backboard and 16 0 dBm RF outputs are routed from the front panel for easy access after installation. The amplification stage connections and the forward/reflected break-out are situated on the rear side to minimize clutter. Leaving cables blank rather than modeling every cable avoids visual clutter at this stage, a clear wiring path was left for continued work.

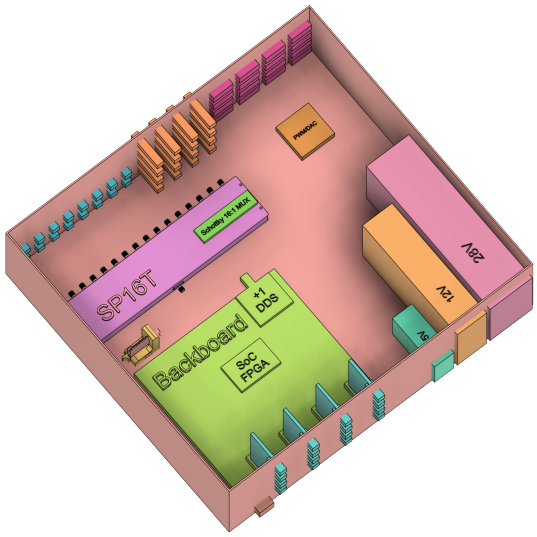


Figure 4.6: Preliminary component placement in a 4U, 19 inch rack enclosure.

These rapid prototyping steps provide early confidence that the CHS2 is feasible and the electronic and mechanical design can coexist within established constraints. This reduces the risk of radical redesign requirements in the later stages that would necessitate a enclosure rework.

4.5.3 AD9915

As for the specific DDS of choice, the AD9915 from Analog Devices became the final choice [15]. The AD9915 has 16-bit phase tuning resolution, 12-bit amplitude scaling, a 135pHz frequency tuning resolution and a maximum frequency output of 1 GHz. It also has built in support for multi-chip synchronization which was the main reason it was chosen. Alongside this it also has low phase noise (-128 dBc/Hz) and a low wideband Spurious Free Dynamic Range (SFDR) ($<$ -57 dBc) meaning that both its phase and frequency noise is low.

Another reason for choosing the AD9915 was the amount of additional resources that were available, both from official Analog Devices (AD) and from their forum EngineerZone where both AD and community members can answer any questions asked. Finally, the existence of an evaluation board and third party options added ease of prototyping as the DDS could be tested without having to design custom PCB's.

Initially the AD9915's higher spec version was chosen, since it has the same architecture as but provides a higher clock speed and maximum frequency output. Nevertheless the multi-chip synchronization limits clock speed and maximum frequency output to the same as AD9915 and therefore there was no reason to pick the more expensive AD9914.

4.5.4 Amplitude Control: AD5694 DAC

Amplification control of the system is implemented through the pre-amplifiers in the amplification stage, which are driven by 0–5 V DC and digital signals. This creates the need to convert digital control signals into analog voltages to regulate the pre-amplifiers. In CHS1, this was achieved using Pulse-Width Modulation (PWM) to DC converters, where the duty cycle of the digital PWM signal is translated into a corresponding analog voltage as shown in figure 4.7 below.

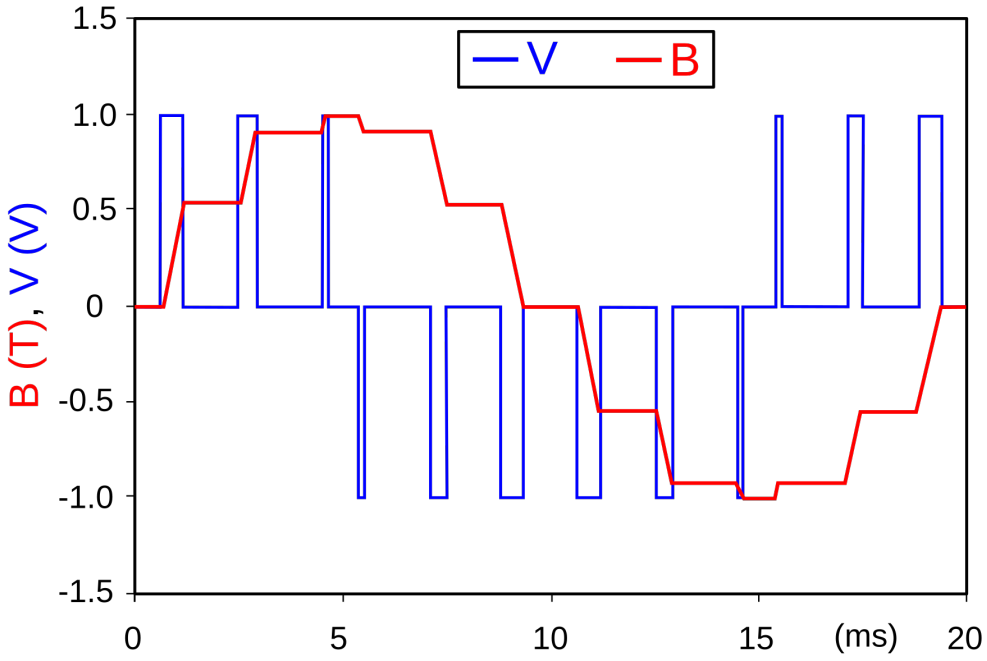


Figure 4.7: An example PWM signal where the blue line is the digital PWM signal while the red signal is the resulting in the DC voltage shown by the red line. By Zureks - Own work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=1835361 [16]

For CHS2, the AD5694 DAC was used to replace the original PWM-DC converters which reduces the amplification controls footprint. Figure 4.8 below shows the layout of a 8 channel pre-amplifier control board taking digital I^2C inputs and outputting 8 control signals, 8 shutdown signals while also routing the control signals through a multiplexer which adds a debug channel for reading the control signals.

The final PCB design shown in figure 4.9 was based on a previous version done developed by the projects supervisor Robin Nilsson which initially included a microcontroller for control. Later on in development the I/O expander and multiplexer debug output was added.

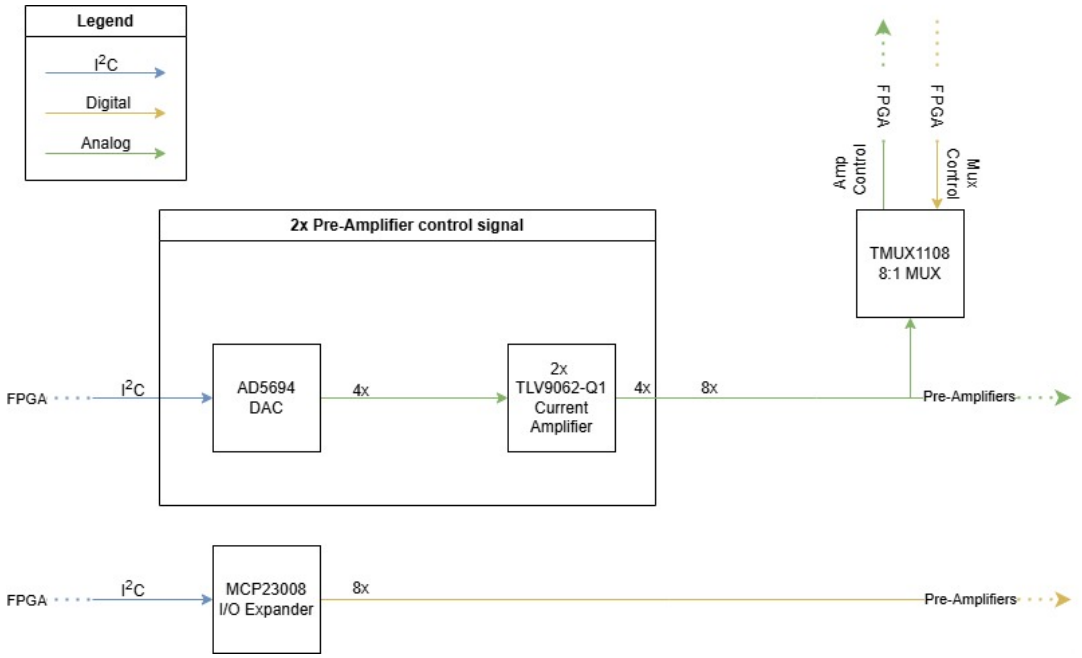


Figure 4.8: System overview of 8-channel pre-amplifier DAC driver PCB

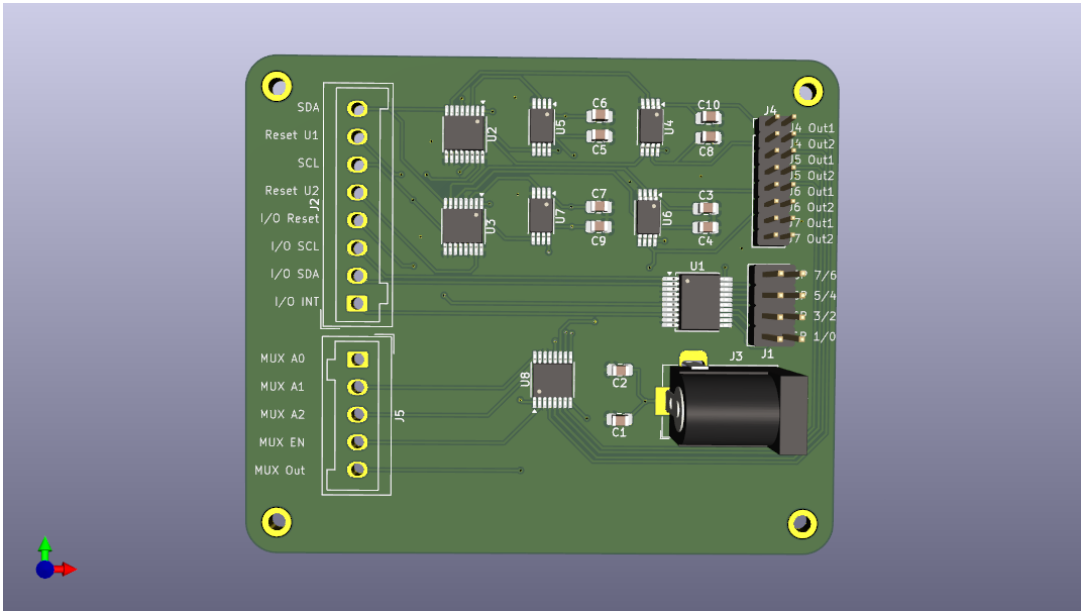


Figure 4.9: KiCAD 3D view of pre-amp DAC Driver PCB

The amplification stage is inherited unchanged from CHS1 and is therefore only briefly treated here. Each lane boosts the 0dBm source produced by the quad-DDS modules up to the 53dBm 200W used in the applicator array. Every channel incorporates a bidirectional coupler that exposes the forward and reflected signals on SMA ports. These ports are connected back via coaxial cables to the calibration and measurement sub-system discussed in section 4.5.5. The figure 4.10 displays one out of the 16 total channels used in the amplification stage.

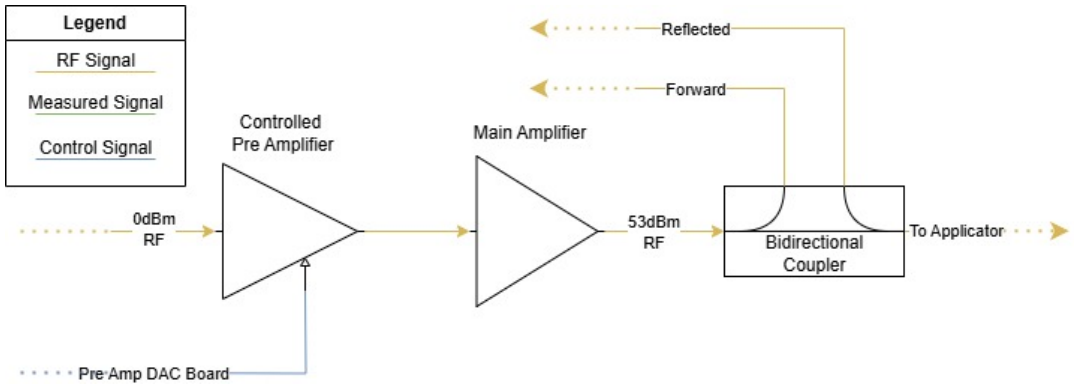


Figure 4.10: Block diagram of a single amplification stage channel out of a total 16

4.5.5 Feedback Loop: AD8302

The feedback loop chosen reuses most of the CHS1's system architecture with the difference being using only one AD8302 phase and gain comparator connected to a switch. CHS2's calibration and measurements sub-system closes the loop between generated and delivered RF power while simultaneously providing real time fault detection. As illustrated in figure 4.11 the sub-system is partitioned in to two distinct signal paths:

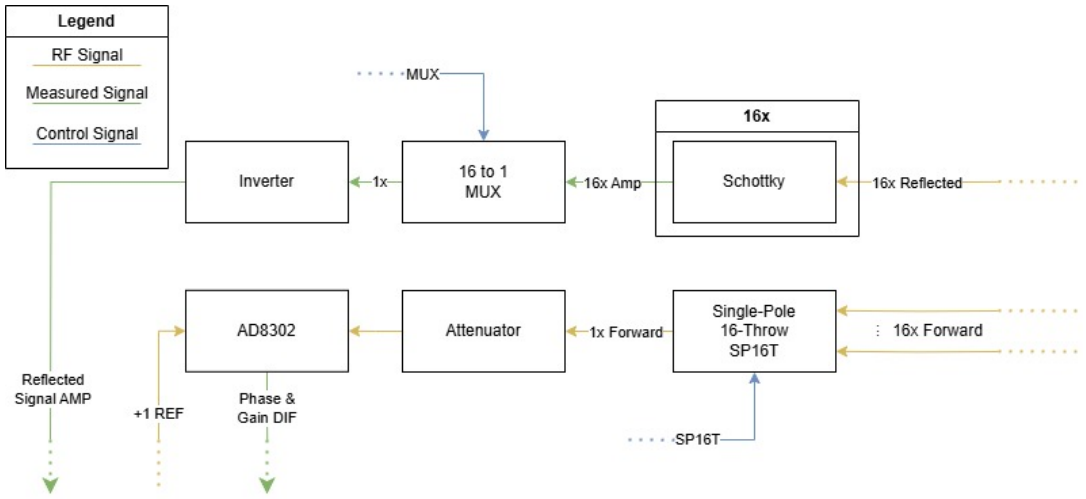


Figure 4.11: Block diagram view of the calibration and measurements subsystem of the proposed CHS2

4.5.5.1 Reflected Signal Path - Measurements and Safety Monitoring

The architecture mirrors that of the legacy CHS1 and re-uses the proven method employing the Schottky detectors. The signal generated here can be used to monitor the safety of the system while operating in firmware. Tripping a hardware shutdown sequence if too much reflected energy is detected.

4.5.5.2 Forward Signal Path - Calibration

The incoming forward signal from all 16 channels is multiplexed by a Single-Pole 16-Throw (SP16T) switch such as the Mini-Circuits USB-1SP16T-83H. This reduces the amount of necessary AD8302 detectors down to one from the 16 present in CHS1. When calibrating, the *+1* master DDS hops to the same frequency as the desired channel being calibrated and the SP16T puts it through to the AD8302. This comes with a trade-off where this design precludes simultaneous, real-time monitoring of all channels. Despite calibration becoming a sequential process it doesn't hinder the functionality of the CHS2 as it follows the same calibration philosophy of the CHS1 where the calibration is performed before the treatment. It being sequential instead of parallel then only increases the time by at most approximately 500ms it takes to perform calibration without affecting performance.

4.5.5.3 CHS2 Full-Power Calibration Routine

Changes in hardware necessitates a new calibration routine for the CHS2, this section outlines the basic steps of a full-power calibration routine. A key function used in this routine is the Clear Phase Accumulator (CPA) bit. When set to 1 it clears the phase accumulator on IO UPDATE, this allows us to avoid destructive phase steps ensuring the calibration is phase-safe.

Step 1: Initialize

- **Step 1:**1. Reset and follow the 8 step synchronization recipe outlined in the AN-1254.
- **Step 1:**2. Load desired therapy frequencies to channels 1-16, set the +1 reference DDS to an idle frequency, with CPA enabled issue global IO UPDATE.
- **Step 1:**3. After a period of time to let equipment warm up un-mute the amplification stage at full power.

Step 2: Measure each channel

- **Step 2:**1. Switch the SP16T to channel **i**.
- **Step 2:**2. Hop reference DDS to frequency of channel **i** with CPA enabled, then assert global IO UPDATE.
- **Step 2:**3. Wait and collect samples from AD8302.
  Repeat for all 16 channels.

Step 3: Update look-up table (LUT) - Using the samples collected update a look-up table stored in FPGA DDR3L to be used for treatment. It holds the correctional values.

Step 4: Start Therapy - From the LUT apply the new corrections and begin the treatment. Verify results if necessary.

This calibration routine must be completed before treatment begins and should not be performed mid-treatment. Running the procedure during therapy would disrupt the phase continuity of the reference DDS, leading to unintended phase steps and loss of synchronization across channels.

4.6 Documentation and QMS

As CHS2 is a medical device being developed and planned to operate inside the EU, it has to adhere to Medical Device Regulation [17]. Number of regulatory, technical and clinical aspects needs to be met. For this project the focus has been on developing a base for a future Quality Management System (QMS), by following the ISO-13485 and the ISO 9000 family of standards, while also following correct technical documentation procedures (Annex II and III of MDR) [18]. This documentation was saved on a private github repository whose structure is shown in appendix A with the intention of allowing clear communication to any future collaborators.

The first of the directory in the root directory is the design folder. This folder contains all the design files and is divided into Firmware, Hardware and System Architecture where firmware contains all the code for the project, hardware contains all the hardware design files such as PCB files and 3D print files while System Architecture contains Design notes and Visualizations such as 3D models.
The next directory in root is the Manufacturing directory. Here all the files needed for manufacturing are contained such as assembly drawings, Bill of Materials (BoM) and PCB manufacturing files (Gerber files).

The QMS directory contains the base of the QMS and contains the related files. The first directory is for storage of future audit records while the second one contains a template and folder for Corrective and Preventative Actions tickets (CAPA). A CAPA ticket is submitted if a problem occurs and contains background info, data and a root cause analysis of said problem, which is then used to correct the issue. The third QMS directory contains the Quality manual which describes how the QMS is laid out and what to standard to follow. The risk management directory contains files with hazard analysis and risk management plans. A Failure Mode and Effects Analysis (FMEA) table directory is also stored here where potential risks are assessed before and after corrective action. Finally, the QMS directory contains a folder with Standard Operation Procedures (SOP) for different parts of the documentation.

References is next in the root directory. In here all figures, datasheets, pictures, scientific papers and technical sources are stored for future use. Traceability directory map's requirements to corresponding design elements, verification and validation tests in a formal traceability matrix.

The final two directories of the root directory are Validation and Verification where respective simulation reports, test protocols and test reports/data are stored.

Finally, in the root directory lies a changelog file where every change and addition is added alongside the date of the change.

4.7 Summary

The system proposed in this part addresses the main goals outlined in Section 1.2, while also improving other aspects of the design. The primary objective of CHS2 was to achieve independent frequency, phase, and amplitude control per channel. This was realized by replacing the single analog oscillator with multiple DDS boards, which are more compact and scalable.
In addition to meeting the primary goal, CHS2 also fulfills secondary objectives by reducing the physical size and complexity of the system. This was accomplished through the introduction of a dedicated pre-amplifier DAC board, which consolidates all pre-amplifier control onto a single board, and by implementing the proposed SP16T switch design, which requires only one AD8302 comparator instead of sixteen. Finally, CHS2 improves the phase control resolution from 10-bit to 16-bit by using the DDS for both frequency and phase control. This adds two orders of magnitude in precision, further supporting modularity and future scalability. Collectively, these improvements align with the goals of advancing beyond the previous system and facilitating future development through a more modular and well-documented design.

Part III

Hardware Validation and Testing

5

Hardware Validation and Testing

The signal generation hardware designed in part II promises to deliver 100 MHz-1 GHz coverage with 5 degree phase and 5% amplitude accuracy at 0 dBm (table 5.1). Before fully commiting to a 16-channel full scale build, these requirements must be demonstrated on a smaller scale test bed. The test must demonstrate that it fulfills the tight synchronization requirements that hyperthermia systems demands. Part III is therefore sets out to answer a set of laboratory questions pertaining to the performance of the AD9915 DDS for use in the CHS2 system:

- **Single channel fidelity** - Does one DDS stay within the frequency phase and amplitude limits over the full band?
- **Multi channel determinism** - Can two or more DDS chips boot with a repeatable and stable phase relationship?
- **Optimal settings** - The AD9915 has several different operating modes, how do they (*PLL*, *ExtRef*, *ExtRefMult*) compare against the legacy HP8350B oscillator in terms of jitter, spurs and rise-time?

The remainder of part III is dedicated to answering these questions by selecting commercial evaluation hardware that serves as a stand in for the planned quad-DDS module, creating repeatable test protocols and comparing the results against the CHS2 requirements.

5.1 Background

The first generation CHS1 is driven by a single HP8350 wave generator that is split, phase shifted and amplified 16 ways. While electrically simpler than CHS2, that design bases every channel on one common frequency, takes up nearly 10U's combined and offers only 10-bit phase resolution. CHS2 replaces the bulky wave generator with sixteen AD9915 DDS sources, gaining per channel frequency control and 16-bit phase resolution in a 4U form factor. The architectural leap is nontrivial but so is the complexity that the CHS2 brings with it, requiring picoseconds timing tolerances to operate optimally.

5.1.1 Preliminary Evidence

AD's own data sheet features benchmarks showcasing the performance of the AD9914 /AD9915 clocked from a low jitter source and shows very promising results before it even arrived in the lab [15]. These results legitimized the purchasing of prototype equipment for further evaluation. Nevertheless data sheet for the DDS also outlined

the complexity to sync multiple units as well as a synchronization application note, AN-1254 outlining the steps necessary to achieve deterministic startup [19].

5.1.2 Hardware Evaluated

For rapid iteration the use of a commercial of the shelf solution from GRA & AFCH was used [20]. Two AD9914 IO shields, each mounted on a Arduino Mega-2560. Although limited to one DDS per shield compared to the planned quad-DDS module the shields have most of the same functionality available to them and featured in a self reliant package. With additional amenities such as active cooling from a fan and on board peripherals for convenient control and monitoring in the form of a OLED screen and rotary encoder. The chosen DDS shield can be seen in figure 5.1.

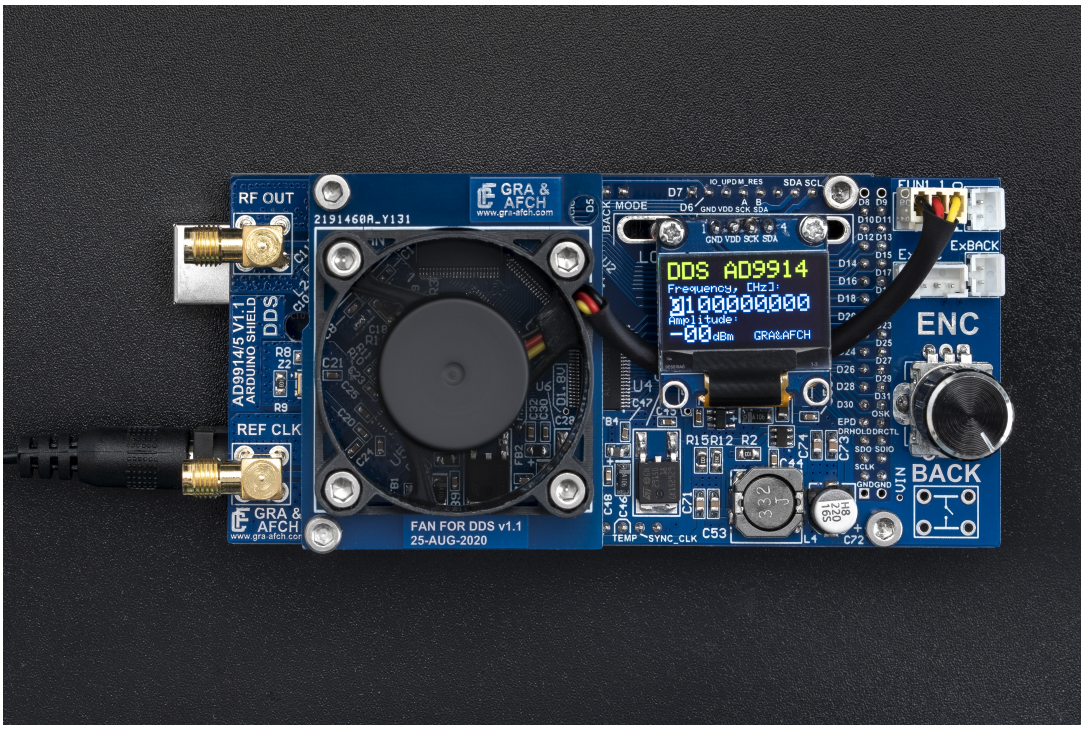


Figure 5.1: The GRA & AFCH AD9914 Arduino Shield

Using the DDS Arduino shield allows prototyping within days rather than months. On the choice between the AD9914 and AD9915, both are sister chips, with both the chip and IO shield are nearly identical, the differences lies in the clock speed that affects the upper bound of the frequency generation range. The AD9915 is an updated version of the AD9914 focusing on multi unit synchronization, as the AD9914 can synchronize between copies of itself only up to 2.5 GHz clock speed the functional max clock speed of the AD9915. The AD9915 is favored for fulfilling the requirements the CHS2 needs for a lower price.

Before implementing the new signal generator into the system, testing had to be performed to see if it conformed to the system requirements. The main experimental setups for this is using a Oscilloscope for visual and time domain analysis of the

signal. Some testing was tried on a Vector Network Analyzer (VNA) and a Software Defined Radio (SDR) to validate the performance claims made in the datasheet of the AD9914/AD9915 and by the vendor of the GRA & AFCH.

5.2 Experimental Setup

To validate the theory that a DDS source can replace the currently used legacy HP8350B Sweep Oscillator in CHS1, two AD9914 Arduino MEGA IO shields GRA & AFCH V3 were purchased and then characterized[1] [20].

5.2.1 Measurement Setup

The AD9914 has several modes of operation and all of them will be compared to the legacy wave generator from CHS1. The target clock speed used to drive the AD9914 was chosen to be 2.5 GHz as it is the same as the upper bound for the AD9915 and gives us the possible frequency range of up to 2.5 x 0.4 = 1 GHz according to the datasheet [15]. Below is the details for the measurement setup used to collect data.

- **Signal Sources**
  WaveGen: HP8350B Sweep Oscillator (Baseline)
  PLL: AD9914 shield using onboard PLL at 2.5 GHz
  ExtRef: AD9914 shield locked on to an external 2.5 GHz generated by HP8350B
  ExtRefMult: AD9914 shield locked on to an external 50 MHz generated by HP8350B with 50x multiplier
- **Instrumentation**
  HP Infinium Oscilloscope 1.5 GHz 8Gsa/s @ 50Ω for time domain capture. All cables were phase matched and 50Ω.
- **Procedure**
  Each source was stepped from 100 MHz to 1 GHz in 50 MHz increments. For every measurement 10 seconds worth of continuous cycles were sampled before measurement was noted into a CSV document.

5.3 Single-Channel DDS Performance

The four plots in figures 5.2 through 5.5 comparing the three different modes of operation for the DDS (*ExtRef*, *ExtRefMult* and *PLL*) and the legacy *WaveGen* across the entire 100-1000 MHz sweep. Table 5.1 provides a succinct overview of numerical averages and an overal figure of merit (FOM). A lower value is indicative of better behavior.

[1] Primarily chosen for their compact form factor 53.26 x 114mm, lower unit cost €700 compared with €1100 for the official Analog Digital evaluation board and access to the open source firmware library used to control it [21]

5.3.1 Frequency Accuracy and Stability

Figure 5.2 shows that a DDS using *ExtRef* tracks the programmed frequency within 0.38 MHz, compared to the legacy *WaveGen* it is on average, roughly a four fold improvement. This shows the static offset between the frequency programmed and the frequency the source actually delivers measured across the entire sweep. In phased arrays this can have a direct impact on phase accuracy and the accuracy of energy delivery. The data shows that the legacy wave generator and the internal PLL mode for the DDS both start to deteriorate beyond 900 MHz.

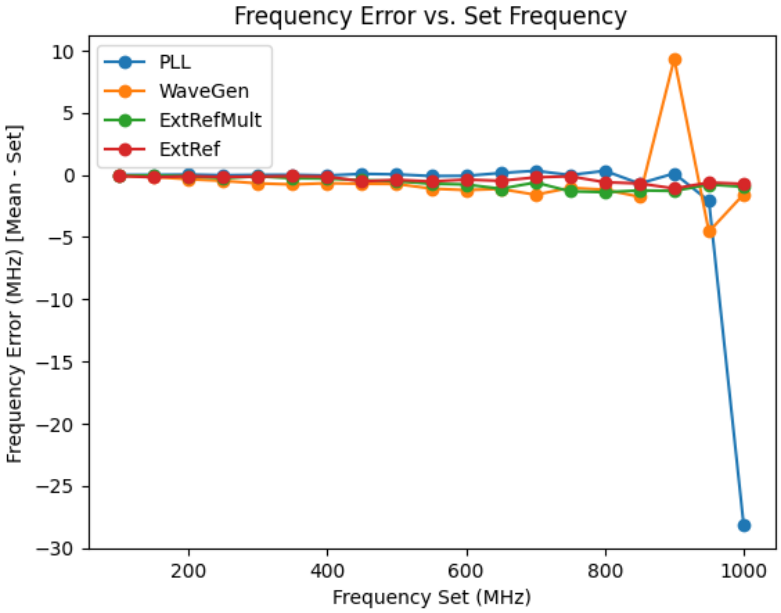


Figure 5.2: Frequency Error vs. Set Frequency: Illustrates the deviation between programmed and delivered frequencies, crucial for maintaining long-term phase alignment in applications like phased arrays.

When looking at the short term jitter, it follows a similar pattern: the standard deviation stays below 2.3kHz for both *ExtRef* and *ExtRefMult* see figure 5.3 and table 5.1, far outperforming the legacy *WaveGen* which notably struggles with some outliers towards the higher end of the measurement range. It represents the short-term statistical spread of the output frequency around its mean, plotted across the sweep. It captures the phase noise and indicates the spectral purity of a signal. Similarly to the previous metric the data shows that both the legacy wave generator and the PLLs performance worsens at 900 MHz and beyond.

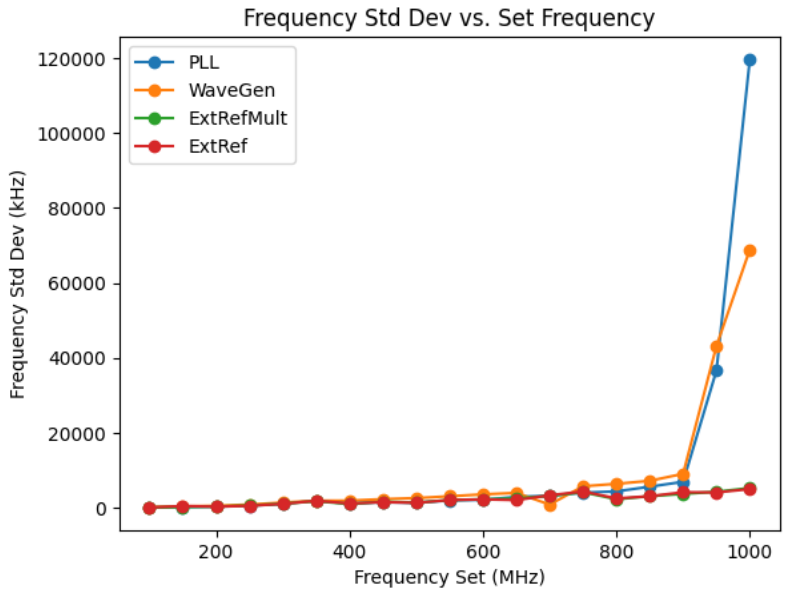


Figure 5.3: Frequency Standard Deviation vs. Set Frequency: Shows the short-term statistical spread of the output frequency, directly indicating signal spectral purity and short-term coherence.

5.3.2 Amplitude Flatness

All sources follow a similar pattern of a downwards trending slope for their peak to peak voltage as frequency increases. Notably the legacy *WaveGen* is superior in its linearity, whereas all the DDS's follow more of a wavy pattern with a local minima at 200 MHz and a local maxima at 450 MHz as shown in figure 5.4. This behavior is probably due to the intrinsic sin(x)/x rolloff inherent in the output as well as the characteristics of the output filter and balun but it is unlikely to affect performance as it is within the margins that the system can manage. Beyond that the DDS variants all hold an amplitude standard deviation below 0.01V see table 5.1, well inside the 5% budget specified in table 4.1 outlined in section 3.3. Notably the AD9914 shield has the ability to adjust for amplitude but for the purposes of this test it was left on the 0 dBm setting.

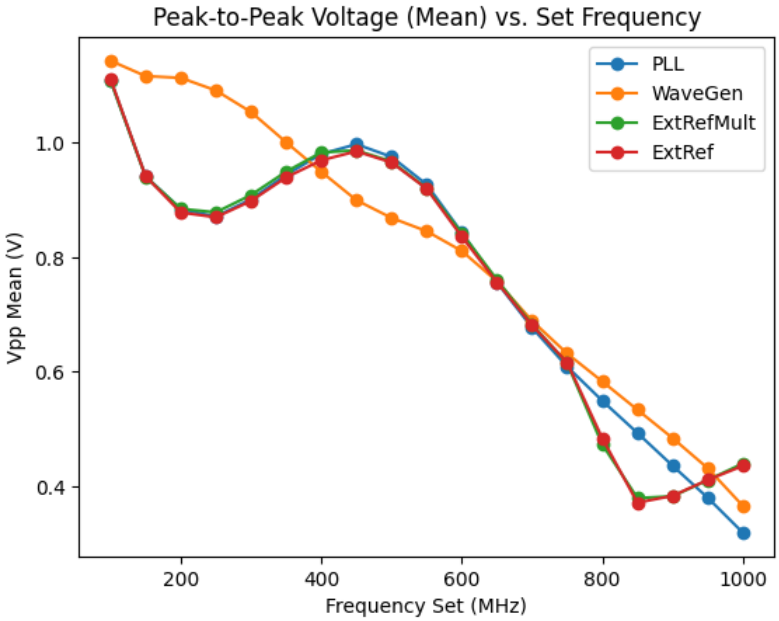


Figure 5.4: Peak-to-Peak Voltage (Mean) vs. Set Frequency: Displays the average peak-to-peak voltage across the frequency sweep, ensuring uniform power delivery for consistent system performance.

5.3.3 Edge Quality

The average rise time, see table 5.1, groups tightly between 0.827ns and 0.835ns. The sub nanosecond spread and nearly identical results for rise time as seen in figure 5.5 indicate that none of the sources will be a bottle neck or hindrance in future use. It effectively measures system bandwidth and edge fidelity indicating the performance for modulating or changing the frequency.

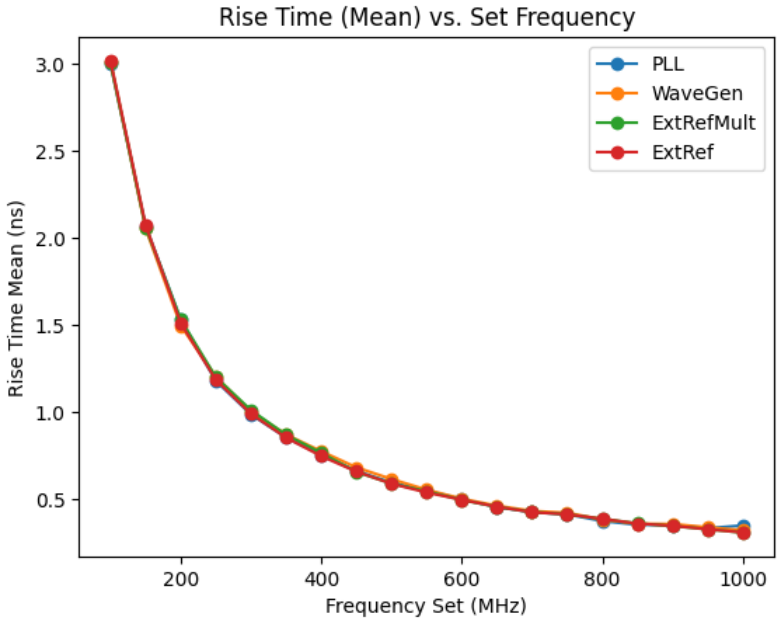


Figure 5.5: Rise Time (Mean) vs. Set Frequency: Illustrates the average signal rise time across the frequency range, indicating system bandwidth and edge fidelity for maintaining wide-band integrity during modulation.

Table 5.1: Mean performance metrics over the 100–1000 MHz sweep (lower FOM values are better).

Metric	**ExtRef**	**ExtRefMult**	**WaveGen**	**PLL**
Frequency accuracy				
Avg. $\lvert f_{\text{err}} \rvert$ (MHz)	0.382	0.648	1.533	1.700
Frequency stability				
Avg. σ_f (kHz)	2 214.9	2 199.4	8 676.3	10 336.3
Amplitude stability				
Avg. V_{pp} Std. (V)	0.0078	0.0066	0.0097	0.0096
Edge quality				
Avg. rise time (ns)	0.827	0.831	0.835	0.829
Aggregate metric				
Figure of Merit†	1.279	1.315	1.876	1.991

† Defined as the root-sum-square of the normalised four metrics above; lower values indicate better overall performance.

5.3.4 Overall Assessment

The aggregate FOM in table 5.1 is synthesized by combining the four normalized metrics via a root-sum-square calculation. *ExtRef* and *ExtRefMult* emerge as clear

winners with the lowest FOM scores of roughly 1.3, outperforming the legacy *WaveGen* by approximately 30%. The data then confirms that a AD9914 DDS IO shield using a low-noise external reference is a drop in replacement for the HP8350B. Meeting or exceeding every accuracy, stability and timing requirement across the full hyperthermia band.

This puts the DDS well withing the performance targets outlined in section 3.3 table 4.1. These results justify proceeding with the two channel synchronization tests described in section 4.3

5.4 Operating Multiple DDS

Without any synchronization, two AD9914 using the onboard PLL as a reference signal and set to the same amplitude and frequency settings will not be phase locked.. Connecting them to an oscilloscope gave the result shown in figure .

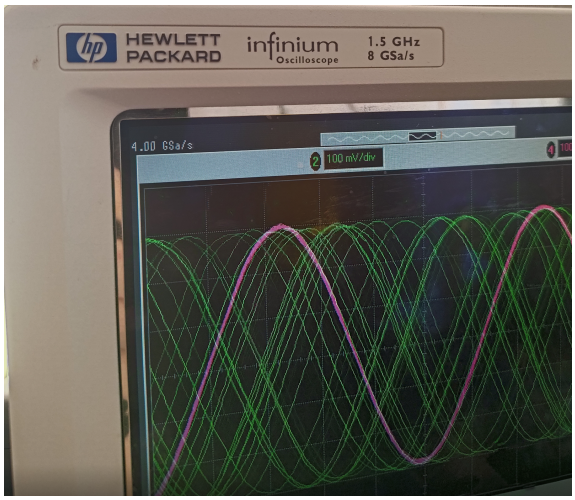


Figure 5.6: Image of the oscilloscope with it being able only to lock onto one signal at a time, in this case pink, and green is left drifting, despite both signals sharing the same amplitude and frequency settings.

Supplying a common external reference signal does not improve coherence, confirming the need for extra measures to be taken to achieve a proper phase locked system.

Deterministic phase coherent operation demands:

1. A common shared external reference such as *ExtRef* and *ExtRefMult* being fed into each DDS.
2. Correct use of the AD9914 deterministic sync pins **SYNC OUT, SYNC IN** and **SYNC CLK**
3. Proper firmware implementation of a synchronization routine using **IO UPDATE**, resetting and DAC calibration

In the next section 5.5, the necessary hardware wiring and firmware modifications necessary will be employed to construct a proof of concept.

5.5 Two-Channel Proof of Concept (PoC)

Having confirmed the viability of a single DDS shield can serve as a stable microwave source, the next step was to verify whether two such generators can be driven in deterministic phase coherence, a prerequisite for the viability of the multi channel CHS2. This proof of concept emulates a smaller scale version of the CHS2 architecture by synchronizing two AD9914 DDS shields.

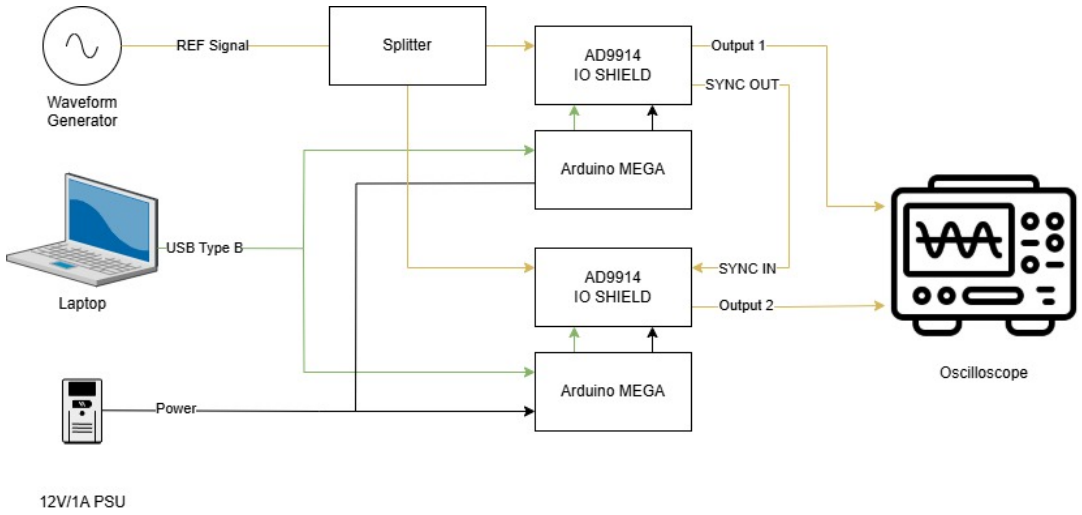


Figure 5.7: Diagram of the Two-Channel PoC

The PoC hardware setup can be seen in figure 5.7, it consists of two GRA & AFCH AD9914 IO shield mounted on an Arduino Mega 2560 each. The Arduino is connected to separate power supplies receiving 12V/1A. Using the legacy *WaveGen* to generate the 2.5 GHz or 50 MHz reference signal that is fed into a 2 way splitter. The output from the splitter is delivered through equal length, 50Ω, phase matched coaxial cables to the **REF CLK** input of both shields, providing the common timing reference *ExtRef* or *ExtRefMult*.

5.5.1 DDS Shield Limitations

The shield came with unpopulated pads for **SYNC OUT, SYNC IN** and ground. Pins were added to **SYNC OUT** and **SYNC IN** of both the shields. One DDS is configured as master, the other as a slave. The master's SYNC OUT is linked to the slave's SYNC IN via a short jumper cable.

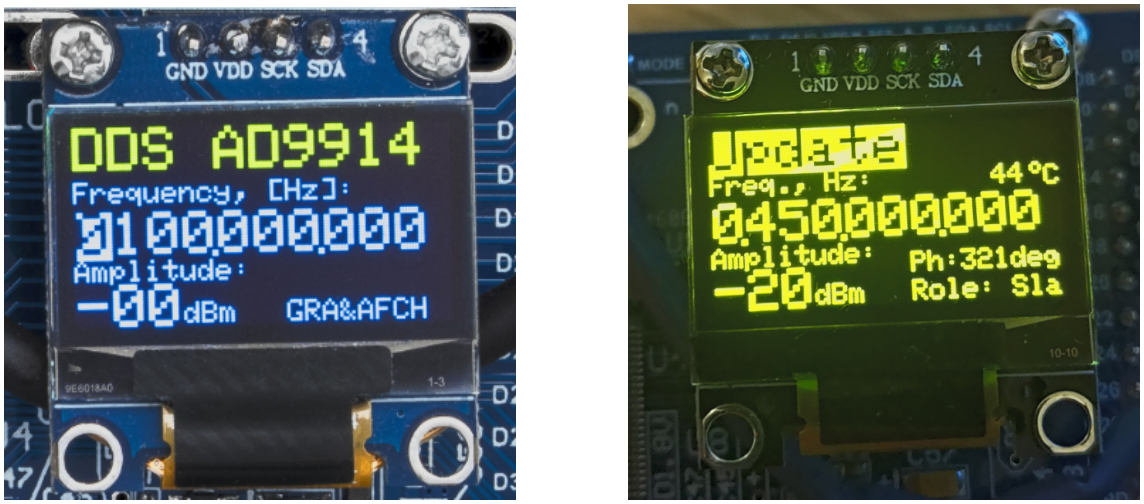
The design of the IO shield limits access to any of the IO ports on the Arduino and provides no easy access to the **SYNC CLK**. Only available port for communication is the USB D port on the Arduino. Each Arduino communicates with the host PC over USB for programming and control. The RF outputs of the two DDS shields are routed via impedance and phase matched coaxial cables to separate oscilloscope channels for measurements. .

5.5.2 Two-Channel Firmware

GRA & AFCH provide an open source C++ library for the AD9914 shield hosted on their GitHub [21]. It offered basic control over the AD9914, providing reference source selection (*ExtRef*, *ExtRefMult* or on chip *PLL*), frequency setting, amplitude adjustment (0 to -68 dBm) and RF output toggle. The firmware also has implementation to be controlled via on board rotary encoder and OLED interface and via USB serial commands. For deterministic multi device operation, four capabilities were implemented:

1. **Master/Slave role selection** - An internal function that toggles settings for either state:
   Master: **SYNC CLK** and **SYNC OUT** enabled.
   Slave: **SYNC CLK** and **SYNC OUT** disabled, **SYNC IN** always active.
2. **Deterministic IO UPDATE** - Automatic IO updates after every parameter change were removed. IO update was made to be manually called from either a dedicated menu item or a serial command from PC. This allows for multiple settings to be staged before being applied simultaneously upon IO update.
3. **Phase offset functionality** - A new function to write a 16-bit Phase Offset Word POW to the 32-bit phase accumulator, allowing for full 360 degree phase adjustment. The function is exposed in the on device OLED menu and as a serial command.
4. **Persistent settings** - All new parameters mentioned above are saved to EEPROM and restored on power on.

Additionally the hardware **RESET** pulse was made available to be called via USB to aid in debugging and testing. The visible changes made can be seen in figure 5.8b.



(a) Original firmware and picture from GRA & AFCH [20], [21]

(b) Modified firmware for synchronization

Figure 5.8: Before and after modification of the DDS shield monitor

The initialization routine for the DDS shield was rewritten to better mirror the eight

step synchronization process outlined in AD's application notes AN-1254 [19]. To summarise from the AN-1254 these are the steps necessary to synchronize: Power up device and apply REF CLK → master reset → DAC calibration with IO update → enable SYNC OUT for master → DAC calibration with IO update → adjust SYNC OUT delay → repeat step 3 → issue common IO UPDATE.

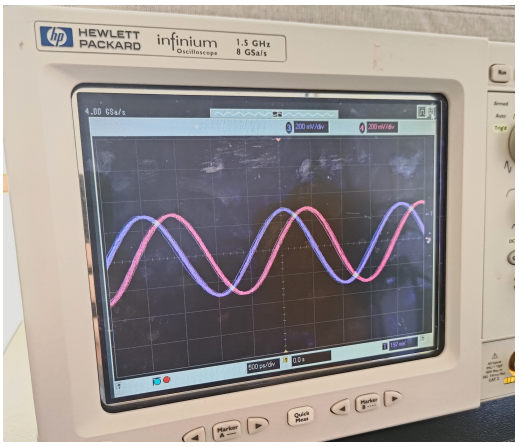
A lightweight Python script was written and used to connect to both Arduinos via USB and can broadcast serial commands. It reinitializes each DDS and during that process identifies each boards role. Most critically it is used to perform the final step of the eight step synchronization recipe, it drives simultaneous IO UPDATE pulses to both devices, an essential part in the process to achieve deterministic phase alignment. The limitations of this approach will be discussed in section chapter 11.

5.5.3 Two-Channel Results

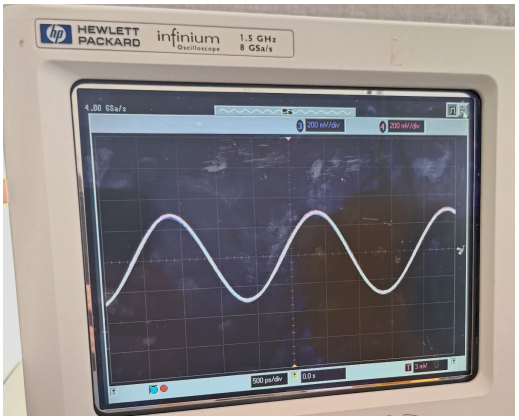
After configuring the wiring to be as seen in figure 5.7 and loading the custom firmware onto both Arduinos, the host PC launches the Python script. After establishing a connection, identifying each DDS and the DDS has gone through steps 1 through 7 of the AN-1254 both DDS shields await the coincident IO update [19]. A minor firmware bug occasionally prevents the chosen reference source from being correctly restored from EEPROM. Until resolved a work around is to manually save the REF CLK setting to guarantee repeatability.

5.5.3.1 Initial Synchronization

After using the Python script to issue the simultaneous IO update, both shields will now generate the desired preprogramed signal. The waveforms exhibited a stable, non-zero, phase offset, confirming phase coherence as can be seen on the oscilloscope see figure 5.9a. This residual phase error proves that the two shields share the common reference REF CLK but their internal **SYNC CLK** are not aligned.



(a) Oscilloscope output after doing the final step 8 IO update, notably in stable phase relationship but not in perfect sync

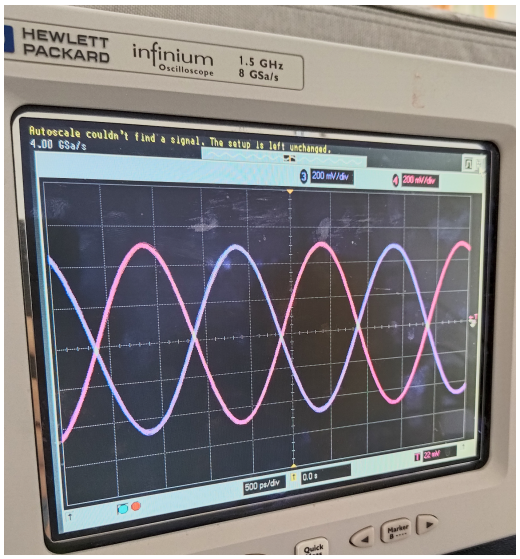


(b) Output after manual calibration to match the phase of the slave to the master DDS

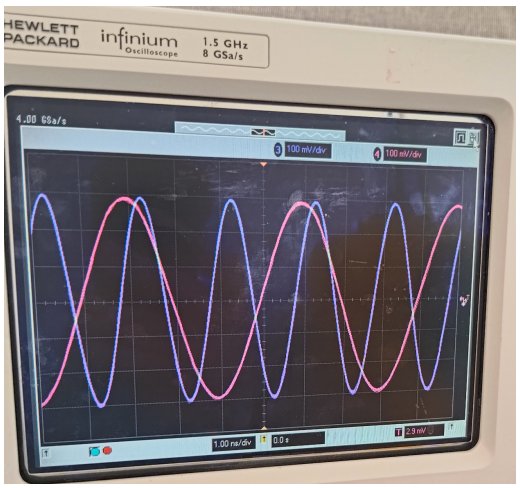
Figure 5.9: Oscilloscope output after synchronization with a) being before manual calibration and b) being after.

5.5.3.2 Manual Phase and Frequency Adjustment

By adjusting the slave's 16-bit POW we can eliminate the gap and achieve overlapping waveforms as seen in figure 5.9b effectively manually calibrating for the error. This exercise also confirms full post synchronization control: any desired relative phase see figure 5.10a or even channel independent frequencies see figure 5.10b can be programmed and staged, then with an IO update can be asserted.



(a) Two signals with one adjusted to be 180 degrees phase shifted against the other



(b) Two signals where purples frequency is twice as large compared to pink

Figure 5.10: Comparison between the on screen menu of the original firmware and the modified version

5.5.3.3 Stability

The stability of the setup was tested by synchronizing the setup to a state similar to as seen in figure 5.9b and leaving it running for 2 hours. After the time elapsed no observable change in phase amplitude or frequency had occurred and the temperature remained the same hovering at about 80 degrees C.

5.6 Observed Limitations of Multiple DDS system

Random boot offset Each power cycle or reset yields a different random initial phase. This is caused by the USB based IO update arriving asynchronously to **SYNC CLK**. It is detailed in the AN-1254 that a requirement of the IO update signal is that it has a 2ns setup and 0ns hold, requirements far tighter than the USB can deliver with a latency of around 1ms.

Hidden SYNC CLK The DDS shield does not break out the pin displaying the SYNC CLK, so its timing can not be verified. To illustrate the issue at hand the AN-1254 details the behavior of SYNC CLK in our case see figure 5.11 causing the random boot offset and in the desired case see figure 5.12.

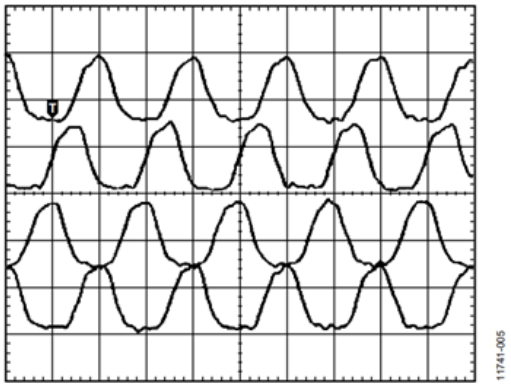


Figure 5.11: The state of the SYNC CLK even after performing synchronization [19]

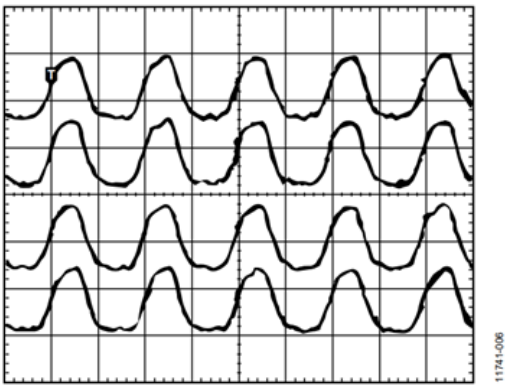


Figure 5.12: The correct desired state of SYNC CLK when calibration goes well before issuing the final coincident IO update [19]

Lack of SYNC OUT fan out buffer As it stands the master SYNC OUT pin is directly connected to SYNC IN of the slave. This is an incomplete solution and prohibits the SYNC OUT SYNC IN mechanism from operating properly resulting in the aforementioned random boot offset. A proper setup would have used a fan out buffer with length matched wiring to provide a coincident SYNC OUT signal from the master to **both** the slave and the masters own SYNC IN as mentioned in the AN-1254.

Measurement Bias The legacy wave generator was used in this test as a reference clock source to the AD9914, this presents an inherent bias to all measurements made. The AD9914 noise floor is inherently based on REF CLK and any impurities or noise in the REF CLK directly reflect in the final output. Essentially the REF CLK sets a hard limit on the noise floor and a better measurement of the AD9914 performance would have been to use a OCXO or other cleaner form of signal to see the full extent of the potential of the AD9914.

Testing with amplification stage As it stands the tests were performed with the signal generators only. Future work includes performing similar tests on the DDS shields while they are connected to the amplification system and feedback system. The initial tests still suggest that the DDS is a suitable drop in upgrade in place of the legacy wave gen.

Frequency adjusting = phase step When adjusting the frequency of a DDS shield and then returning it to the previous frequency there will be an unavoidable phase discontinuity equal to the to the phase accumulator advance during the detour. This is if its issued using a simple IO update or no reset is made.

These shortcomings and observations helped motivate design decisions for the CHS2 design in part II.

Part IV

General Discussion and Conclusion

6
Future Work

This project aimed to design a 16-channel UWB RF phased array for use in Deep Hyperthermia Treatment resulting in the design of a Quad DDS module and Backboard system.

6.1 Adaption of Current Work

By replacing the analog wave oscillator in CHS1 to the DDS Shield yields advantages. The DDS shield is much smaller than the wave oscillator and could therefore be incorporated into one of the server rack boxes. By using the SPI connection the frequency can be controlled through a computer alongside the phase shifters and amplifiers, instead of manually changing the frequency on the wave oscillator. This would effectively make for a wideband hyperthermia system with the main thing missing compared to CHS2 being the channel independent frequency control and the 16-bit phase control compared to CHS1 10-bit control.

Furthermore, the 3D printed drop holder for AD8302 improves the availability of replacing and repairing the system in the case of mechanical failure while also fitting in the current AD8302 rail system.

6.2 Future Development

The present thesis establishes the designa and architectural blueprint for CHS2. The next phase is to translate that blueprint into working hardware and verification results. The task can be grouped into parts: electronics implementation and embedded software development.

The hybrid architecture facilitates an incremental build up strategy: fabricate the backboard and one quad-DDS module, verify deterministic phase and signal performance, then populate the remaining three slots once the design is proven to work.

6.2.1 Hardware - Electronics Implementation

The block diagrams in chapter 4 for backboard and quad-DDS module define signal flow and timing, but lack the component level detail required for fabrication. Future work therefore beings with a complete schematic capture:

- Select power-tree components and regulators that meet the SoC FPGA start up requirements and the noise limits of the AD9915.
- Finalize clock-distribution parts selecting appropriate Low-Voltage Positive Emitter-Coupled Logic fan out buffers.
- Complete an BOM cost vs performance analysis, comparing alternatives against each other for the best choice.

Once the schematic is complete, a multi-layer RF PCB must be routed. Key tasks include:

1. Impedance controlled and length matched routes for REF CLK, SYNC and IO UPDATE.
2. Power plane stack, separation of analog and digital power, proper grounding. Partitioning to suppress digital to analogue crosstalk.
3. Electromagnetic, phase integrity and signal integrity simulations to validate the DDS input and outputs.

6.2.2 Firmware - Embedded Software Development

The development of the FPGA firmware can be broken up into the 3 following stages:

Bare essential hardware test-suite

Minimal C/C++ and VHDL code that allow to toggle each DDS via SPI, measure SYNC CLK and exercise a fast shutdown fault line. This suite should establish the essentials for testing if the system itself works before data can be gathered.

Real time FPGA control

This includes HDL code for deterministic IO UPDATE timing, the code to control peripherals suchg as the SP16T switch and to be able to gather measurement data.

Application Layer

Finally the last stages of the FPGA firmware will introduce PC communication, a calibration algorithm and standard compliant safety protocols.

6.2.3 Testing

Once hardware development and a base control software is implemented, testing of the full system is needed. Signal integrity needs to be tested at the part where the applicators would be connected. These tests would included frequency stability/jitter, phase stability and amplitude tests.

The second factor which needs to be tested is how well the DDS units remain synchronized, as stable inter-channel phase relationships are essential for forming and maintaining a precise thermal focal spot. Any loss of synchronization would result in phase errors between channels, degrading the constructive interference pattern

required.

Testing of a DAC reconstruction filter is also required because the planned 7th order elliptic lowpass filter introduces ripple in both its passband and stopband (equiripple). This ripple could translate into periodic frequency shifts, wich may distort the output spectrum and reduce heating precision. Quantifiyng this effect ensures that the filter does not compromise treatment accuracy.

6.2.4 Additional Directions for Future Work

The road map detailed above covers the core deliverables that take CHS2 from block diagram to realized hardware. There exists several complementary lines of developments, either omitted or only touched on in this thesis, that deserve explicit mentioning before closing.

6.2.4.1 Alternative Controller Platforms

An alternative to developing an embedded custom FPGA PCB to control the system, is using an FPGA evaluation kit as a bridge solution. Using commercially available SoC FPGA evaluation board kits and then have it be separate from the backboard would further improve the modularity and the benefits that the hybrid approach brings. Allow some degree of certainty operational viability and allow for development efforts before backboard is even fabricated. The evalboard would connect and provide the signals needed to the backboard through potentially another mezzanine connector.

Another alternative is using another established micro controller like the STM32H7 that is easier to develop firmware for but using additional peripherals such as an Complex Programmable Logic Device or a FPGA co-processor to allow it to perform at the same level as an standalone SoC FPGA.

6.2.4.2 Alternatives and Improvements to Calibration

The AD8302 is a phase and amplitude comparator widely used in RF systems due to its compact design and ability to directly measure both parameters in real time. In CHS2 it is employed for calibration of the signal paths. However, despite its usefulness, the AD8302 occupies a niche with few true drop-in alternatives. It also has several limitations: the device wraps phase measurements every 180°, introducing ambiguity; it is relatively fragile and prone to mechanical stress; and even with mitigation, such as the use of a 3D-printed bracket, these issues warrant consideration of alternative solutions.

A suggested replacement technology for the AD8302 is using an IQ demodulator and a high resolution ADC. This alternative would deliver potentially higher accuracy for both phase and amplitude without any phase ambiguity. This comes at the cost of some higher development cost and power draw. Future work should prototype a version of this to benchmark it versus the AD8302 over a period of time to measure

its performance and drift tendencies.

With this another improvement would be to introduce a continuous calibration routine. The present routine necessitates stopping of the device and cant be performed mid treatment and only at the start. A rolling calibration routine would be able to measure mid treatment to account for any potential thermal drifting or other imperfections. This would necessitate the reworking the calibration logic to keep a continuous phase on the +1 master DDS without CPA by issuing phase offset commands to match the the phase offset when frequency hopping.

6.2.4.3 Regulatory Pathway (MDR)

With the growing importance placed on the MDR by the EU more work could be done in regards to it. The basics have been covered in the thesis but more work can be done in regards to the usability engineering for a medical device with regards to IEC 62366. It touches upon operator interfacing with GUI and failure tests such as deliberately incorrect cable connections or a disconnected thermal sensor.

Electrical safety and Electromagnetic Compatibility (EMC) tests and compliance with in regards to to EN 60601-1-2 is another future working point. Identifying and accounting for emission sources present in the system.

7
Conclusion

This thesis addressed the primary limitation of the existing CHS1 with its single-frequency operation, by presenting a theoretical complete design and validation of the core signal generation technology for CHS2, a next-generation, multi-channel UWB hyperthermia platform with independent per-channel frequency control. There were three driving objectives behind this thesis, mainly creating a more compact system with frequency per channel while keeping proper documentation for future research and development.

7.1 What Has Been Achieved

The following results and achievements have become apparent as a product of this thesis:

- **Compiled requirement specifications** - A risk and evidence based process that converted clinical, regulatory and practical constrains and yielded concrete quantitative targets.
- **Defined architecture** - Through comparative analysis of different signal generation technologies the DDS was chosen as the solution that simultaneously offers fine frequency and phase tuning resolution, fast switching speeds and deterministic multi chip synchronization. A modular hybrid based approach was developed utilizing a backboard and mezzanine coupled quad-DDS modules. Complimented by a re-engineered feedback system and DAC based pre-amp board.
- **Component selection & mechanical design** - The AD9915 DDS and AD5694 were chosen for the CHS2 design. A new mounting bracket was designed for the AD8302 and 3D printed. 3D models verifying the preliminary component layout inside a 4U enclosure were produced and tested.
- **Prototype validation** - A single and two channel PoC were used for testing to produce results that showed that the chosen DDS was an significant improvements over the legacy HP8350B and demonstrating the viability of the DDS for multi channel operation.
- **Quality management groundwork** - All design artefacts were version-controlled and traced in line with ISO 13485, creating a maintainable baseline for eventual MDR conformity.

The results demonstrate the theoretical viability of the CHS2 and give confidence that the it can deliver on the requirements necessary for next generation performance. This without sacrificing compatibility with existing supporting infrastruc-

ture.

Table 7.1 outlines the quantitative differences between the CHS1, the proposed CHS2 architecture and the developed 2-Channel PoC. The data indicates a clear trend in increased performance between the CHS1 and CHS2. With the CHS2 boasting greater spectral agility, fidelity and phase precision. The PoC is lacking in feature completeness of the proposed CHS2 but has shown promising performance results to justify its existence.

Table 7.1: Key performance comparison between CHS1 (legacy) and CHS2 (proposed) with CHS2 being divided into its initial requirements (CHS2 Req) and the performance of the Proof of Concept system (CHS2 PoC).

Parameter	**CHS1**	**CHS2 Req.**	**CHS2 PoC**
Frequency range [MHz]	100–1000	100–1000	100–1000
Frequency accuracy [σ_f]	1.5 MHz	$\leq$ 0.50 MHz	$\leq$ 0.65 MHz
Phase resolution [bits]	10 (0.35°)	$\geq$ 16 (0.006°)	16
Phase determinism on reboot	Single f	Yes	No
Channels	16 (single f)	16 (indep. f)	2 (PoC)
Output power [dBm]	53	53	0
Rack height [U]	$\geq$ 10	$\leq$ 6	n/a (Benchtop PoC)

7.2 Significance for HT Research at Chalmers

The CHS2 promises exciting possibilities for future HT research at Chalmers. It improves upon accuracy and performance over CHS1 and it also introduces a new degree of freedom in the form of per channel frequency control. This will potentially allow for further research and testing to be done for new treatment strategies that utilize this new feature has the to improve focal spot formation and increase treatment quality.

7.3 Limitations

The thesis remains an engineering prototype. At present only a two channel DDS PoC was produced. Where two modules were synchronized and notably not deterministically, due to limitations in hardware. Theoretical steps and requirements for deterministic synchronization were outlined. The 2 channel PoC was also not implemented with the existing CHS1 amplification stage to gain a better assessment of performance under load, still the results indicate promising viability.

Notably some of the deliverables from this thesis can already be used and retrofitted to improve upon the CHS1 without major reworking of its design required.

7.4 Future Work

With the design of the CHS2 and the framework that this thesis has outlined there is great potential for future work. There are multiple approaches for future work:

- **Complete design of electronics PCB and enclosure assembly** - Completing the design of schematic and PCB to be able to order and assemble all components outlined in CHS2.
- **Develop firmware for synchronization, operation and safety** - Programming the SoC FPGA.
- **Improvements to calibration sub system** - The potential for new and better technologies needs evaluating and for new advanced calibration routines.
- **Integration with treatment planning software** - Further development with interfacing with high level treatment planning software.
- **Extensive testing** - Following results from hardware production testing for EMC and safety to EN 60601-1-2 standard.
- **Advance MDR compliance** - Further work on the regulatory aspects behind development of a medical device and further work on QMS and other applicable standards.

7.5 Closing Remarks

The thesis has systematically translated clinical requirements into a validated technical blueprint. CHS2 is a decisive step towards a truly agile next generation hyperthermia platform. Once fully realised, CHS2 will serve as a valuable research asset for Chalmers and serve to further and contribute to more effective cancer therapy for patients all over the world.

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A

GitHub Directory Tree

```
/
├── Design
│   ├── Firmware
│   │   └── DDS Code ...
│   ├── Hardware
│   │   ├── KiCAD Files ...
│   │   └── Mechanical
│   │       └── 3D Printed Parts ...
│   └── System Architecture
│       ├── Design Notes ...
│       └── Visualizations ...
├── Manufacturing
│   ├── Bill of Materials
│   ├── Gerber Files
│   └── Assembly Drawings
├── Quality Management System
│   ├── Audit Records
│   ├── Corrective and Preventative Actions (CAPA)
│   ├── Quality Manual
│   ├── Risk Management ...
│   │   └── FMEA
│   └── Standard Operation Procedures (SOPs) ...
├── References
│   ├── Datasheets ...
│   ├── Pictures ...
│   ├── Project Planning ...
│   ├── Scientific Papers ...
│   └── Technical Sources ...
├── Requirements ...
├── Traceability ...
├── Validation
├── Verification
│   ├── Simulation Results
│   ├── Test Protocols ...
│   │   └── Test Reports
│   │       └── Test Data ...
└── Changelog.md
```

B

3D Prints

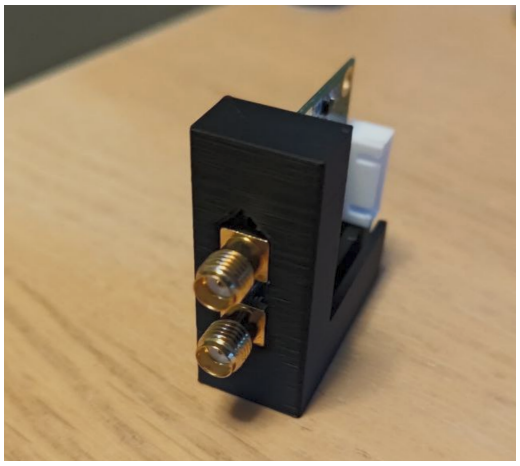

Figure B.1: Single AD8302 bracket viewed from the front

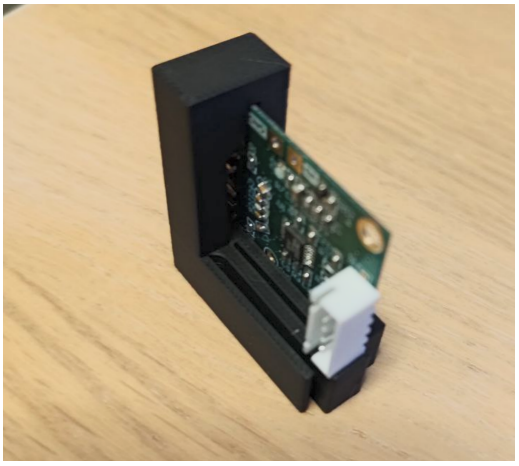

Figure B.2: Single AD8302 bracket viewed from the back

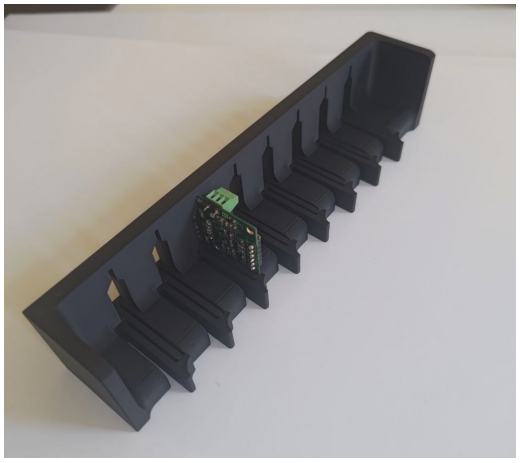

Figure B.3: Row of 8 AD8302 bracket

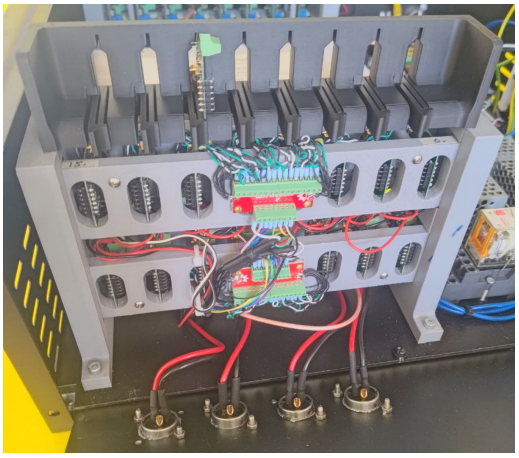

Figure B.4: Same, but placed next to the previous design and to highlight that it fits.

Figure B.5: Figures displaying the results for the 3D prints

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