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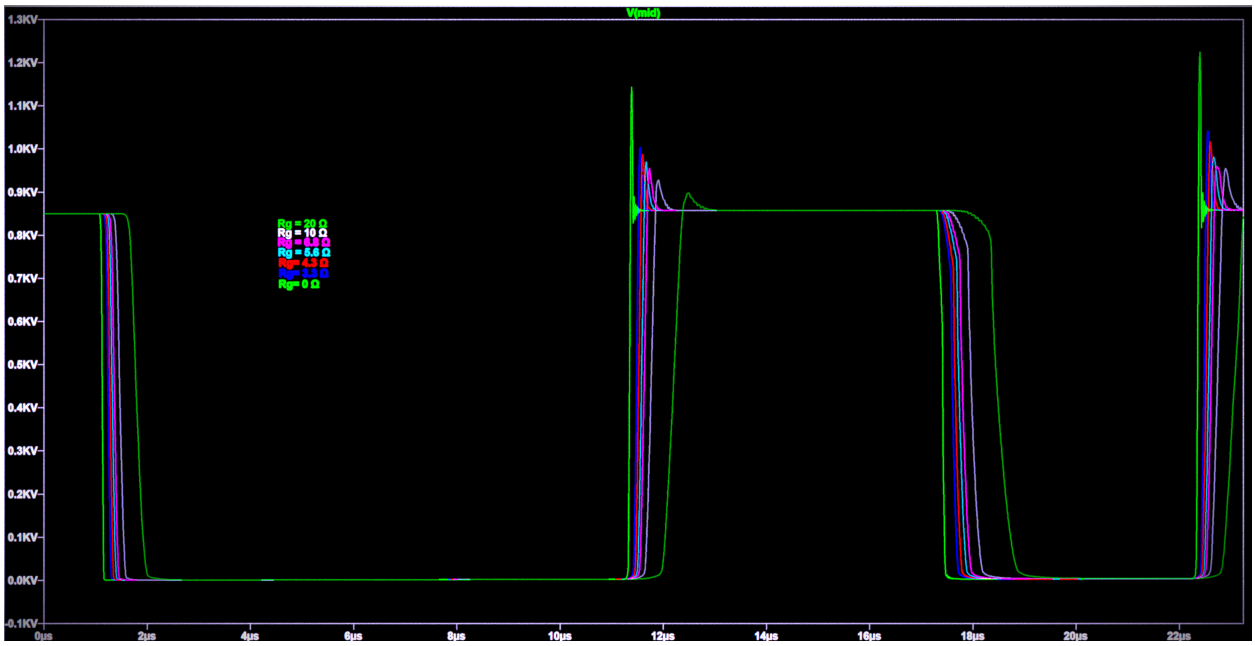

Impact of Dynamic Gate Drive on System-Level Efficiency of SiC-Based Electric Drive Units

Improving the efficiency and overall performance of EDU by implementing DGD for optimization of switching losses and voltage overshoot

Master's thesis in Sustainable Electric Power Engineering and Electromobility

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Cover:
Voltage waveform with varying external gate resistance in LTspice.

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Abstract

The Electric Drive Unit (EDU) is a critical subsystem in Battery Electric Vehicles (BEVs), responsible for converting electrical energy from the battery into mechanical power for propulsion. A central element of the EDU is the inverter, which converts DC power into AC to drive the electric motor. Silicon Carbide (SiC) inverters are increasingly employed in BEVs due to their high efficiency and thermal performance. However, their fast switching characteristics introduce challenges such as voltage overshoots, current spikes, and Electromagnetic Interference (EMI), potentially affecting system reliability and efficiency.

This thesis investigates a Dynamic Gate Drive (DGD) strategy, in which the external gate resistance is adjusted for the turn-off transition of SiC MOSFETs to balance switching losses and voltage overshoot. Circuit-level simulations were performed using a Double Pulse Test (DPT) setup in LTspice to evaluate switching behaviour, while conduction losses were estimated based on the relationship between device voltage rating and on-state resistance R_{DS}. Motor performance under different operating conditions was assessed in Motor-CAD, and system-level losses was analysed under a Worldwide Harmonized Light Vehicle Test Procedure (WLTP) drive cycle.

The results indicate that the DGD approach can reduce inverter losses, particularly under low initial state-of-charge (SOC) conditions, and provide marginal improvements in overall EDU efficiency. However, the impact of DGD on the efficiency of the electric machine was not straightforward, and no clear trend could be established. Nevertheless, reduced voltage overshoot allows for a modest increase in DC link voltage utilization, contributing to higher base speed, increased torque output, and improved peak power performance in the constant power region. While the improvements at the system level are limited, the findings highlight that, in principle, DGD is a method to enhance inverter performance and enable more effective utilization of existing powertrain components in electric vehicle applications.

Keywords: EDU, SiC, switching losses, voltage overshoot, Dynamic Gate Drive, DPT.

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Sara Murnieks Andersson, Göteborg, June 2025

List of Acronyms

Below is a list of acronyms used throughout this thesis, presented in alphabetical order:

AC	Alternating Current
BEV	Battery Electric Vehicle
DC	Direct Current
DGD	Dynamic Gate Drive
DPT	Double Pulse Test
DUT	Device Under Test
EDU	Electric Drive Unit
EM	Electrical Machine
EMI	Electromagnetic Interference
EV	Electrical Vehicle
FOC	Field Oriented Control
FWC	Field Weakening Control
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTPA	Maximum Torque Per Ampere
PMSM	Permanent Magnet Synchronous Machine
PWM	Pulse Width Modulation
SiC	Silicon Carbine
SOC	State Of Charge
WLTP	Worldwide Harmonized Light Vehicle Test Procedure

Contents

1
Introduction

Battery Electric Vehicles (BEVs) are becoming increasingly important in the transition towards more sustainable and environmentally friendly transportation systems[1]. Unlike conventional internal combustion engine vehicles, BEVs run entirely on electricity stored in batteries. An Electric Drive Unit (EDU) plays a crucial role in the propulsion system of the BEVs, converting the electrical energy from the battery into mechanical energy to drive the vehicle's wheels. An Electric Drive Unit (EDU) consists of an inverter, the Electric Machine (EM), and the transmission system. The inverter is a key component converting DC power from the battery into AC power for the electric motor in the Electrical Vehicle (EV). In addition, improving the efficiency of the inverter can greatly enhance the overall performance of the drive system, accelerating the development of electrical vehicles.

1.1 Background

Silicon-based IGBTs and MOSFETs has been widely used in the Electrical Vehicle (EV) industry due to their reliable performance, cost-effectiveness and efficiency in handling power conversion applications. Recently the potential of Silicon-Carbine (SiC) MOSFETs has emerged, in comparison to traditional silicon devices, SiC-based MOSFETs offer further improvements in EV applications due to their superior switching performance and reduced switching losses [2][3][4]. However, the fast switching speeds of SiC MOSFETs introduces issues such as voltage overshoots, current spikes, and electromagnetic interference (EMI), which can negatively affect inverter efficiency and system performance [5].

To address these challenges, there has been significant and ongoing research in this area investigating different techniques. One promising approach to reduce these issues while maintaining the benefits of SiC MOSFETs is adjusting the gate resistance [6].

The power modules in inverters used for EVs are designed for a specific dc-link voltage level. However, a 1200V-rated power module is not designed to continuously operate at 1200V instead, it is rated for a maximum voltage. During fast switching, voltage overshoots occur due to parasitic inductances and diode recovery causing the spikes to exceed the steady-state DC bus voltage [1]. A 1200V battery may push the actual voltage across the MOSFET to 1250–1400V during transients which is

enough to damage or destroy a 1200V module, hence a 1200V power module cannot be used together with a 1200V DC link voltage battery. For safe and reliable operation a margin is therefore necessary, depending on the magnitude of the voltage overshoot. Moreover, the magnitude of the overshoot depends on the gate driver which controls the switching speed. Increasing the battery voltage and with that decrease the margin in a safe way, limiting the voltage overshoot, may improve performance, efficiency and cost.

The principle of a Dynamic Gate Drive (DGD) is based on the potential of implementing external gate resistances. To achieve slower switching and thus less EMI, a higher external gate resistance is used, while a lower resistance results in faster switching speeds and lower switching losses. The choice of the number of gate resistance should depend on the added complexity, cost of components, and the impact on performance and efficiency. Studies have shown the potential of implementing an external gate resistance on minimizing ringing and power losses in specific operating conditions. However, studies have not yet fully covered the impact of variable gate resistances on a EDU system level and from a performance perspective. In this study, the impact of different external gate resistances on both the inverter efficiency and the system efficiency as well as the impact on the electric machine will be explored through simulations.

To fully comprehend and optimize the performance and efficiency of the electric drive unit at a system level, it is beneficial to examine the impacts of DGD on the electric motor.

1.2 Previous Work

To achieve optimal performance, various gate driving techniques has been examined for power transistors can minimize power losses for example. These techniques can be classified into dynamic schemes that can be adjusted each cycle, and passive circuits, that do not monitor operating conditions [7].
Passive control methods, such as adding external gate resistors, may manage switching transients [8]. For passive control, the system remains fixed for all operating conditions and active control of the switching transient refers to either an open-loop or a closed-loop system [9]. However, since these solutions are optimized for specific operating conditions, they may lead to reduced efficiency when conditions change [10][11].

One of the main three control categories is dynamic gate resistance, where the resistance is adjusted in real-time to alter the driving strength and simulate varying gate resistance patterns [12]. By building multiple output transistors into the gate driver, acting as variable gate resistors, the gate of the transistor can be controlled during various operating conditions. One approach incorporates a fixed gate resistance during each switching cycle. In unoptimized conditions, the gate resistance can be adjusted between switching cycles to optimize performance. This is used to modify the resistance during higher current conditions, helping to reduce noise and provide

better damping during switching [11]. Another approach is based on a patterned RG profile that further enhances efficiency by gradually increasing resistance during the transient, improving overall performance and minimizing power losses [12].

Studies have been made on optimization methods indicating that the gate resistance has a significant impact on both switching losses and voltage overshoots. There has been several studies on the parasitic effects in SiC based MOSFETs, [13] showed that increasing gate resistance significantly reduced both current and voltage overshoots and that it indicated a consistent influence on the total time duration. Furthermore, it showed an increase in switching losses with increasing gate resistance. Through simulation and experimental tests study [14] verified that an adjustable gate driver can reduce both voltage overshoot as well as current overshoot compared to a conventional gate driver.

Study [15] proposed an active gate drive technique, dynamically modulating the gate resistance in four stages in order to control the gate current. The voltage and current overshoot are reduced by controlling the dv/dt and di/dt independently as well as decreasing switching loss by reducing switching time. One main approach to determine the optimal timing to change the different gate resistance segments is based on trial and error methods. This leaves rooms for improvement, study [7] introduces the application of a RC filter to monitor gate voltage and identify the optimal dynamic driving pattern for a SiC power MOSFET, showing potential in optimizing the gate resistance pattern.

1.3 Purpose

The aim of this study is to evaluate the effectiveness of a DGD strategy in improving the efficiency of a power electronic converter, particularly in electric vehicle applications. This dynamic adjustment seeks to optimize the trade-off between switching losses and voltage overshoots, which are typically influenced by fixed gate resistance in conventional designs. By adapting the gate resistance in real time, the goal is to minimize overall energy loss during a drive cycle while also considering the effect on MOSFET selection, conduction losses, and motor behaviour.

1.4 Delimitation

This thesis is limited to evaluating the impact of a DGD strategy on switching losses and voltage overshoots in a three-phase inverter system. Other factors such as electromagnetic interference (EMI) will not however be examined within the scope of this study. Alternative optimization strategies will not be explored in this study. The focus will be on investigating system-level benefits from dynamic gate control, in addition to improvements observed at the component level.

The analysis will be conducted primarily through theoretical methods and circuit-level simulations using LTSpice and MotorCAD. Due to time and resource constraints, no physical prototyping or in-vehicle testing will be carried out. As such, the practical integration challenges and system-level validation of DGD in real-world applications remain outside the scope of this work. Furthermore, this study evaluates the influence of adjusting the gate resistance with a focus on the turn-off transition. The same gate resistance value will be applied for turn-on while the gate resistance for the turn-off will be varied. As such, the effect of changing the turn-on resistances is not considered.

The concept of adjusting gate resistance is explored with the aim of reducing switching losses and mitigating voltage overshoot. While experimental validation could be conducted using discrete gate resistors manually switched between operating points, such a method would not be practical for commercial implementation. Real-world systems would require programmable or software-controlled gate drivers to achieve automated dynamic behaviour. Although the thesis does not include hardware realization, similar principles are currently being explored in commercial solutions that dynamically modify gate drive characteristics. Therefore, this work is expected to contribute conceptually to ongoing development in this area, despite not addressing implementation or validation in physical systems.

2
Theory

In this chapter the fundamental concepts related to SiC MOSFET switching, and Permanent Magnet (PM) machine basics are introduced.

2.1 Inverter Construction and Design

A MOSFET is a semiconductor device with three terminals consisting of a gate, drain, and source, illustrated in Figure 2.1. It works as a voltage controlled switch, where the gate voltage determines the current flow between the drain and source. When a positive voltage is applied between the gate and source, exceeding the threshold level, current flows from the drain to the source. When the gate voltage is reduced below a specific threshold level the device turns off and the MOSFET blocks current flow, acting as an open circuit. An intrinsic component of the power MOSFET's structure is the body diode, showed in Figure 2.1.

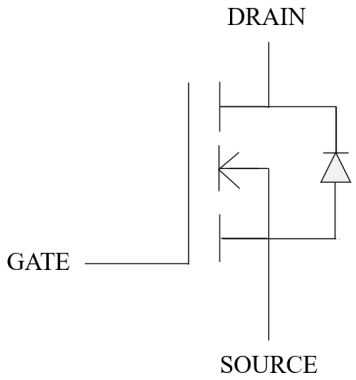


Figure 2.1: MOSFET terminals with the intrinsic body diode between drain and source.

In an ideal scenario, the voltage and current waveforms would show an abrupt drop zero when the device turns on or off, with no overlap. This would mean zero switching losses and perfectly efficient operation. However, due to parasitic inductances, capacitances, and the intrinsic properties of the MOSFET the transitions are not instantaneous. This leads to a period during which both voltage and current are present simultaneously. Figure 2.2 presents the typical switching and conduction loss, where E_{on} and E_{off} represents the switching loss during turn-on and turn-off events and E_{cond} the conduction loss.

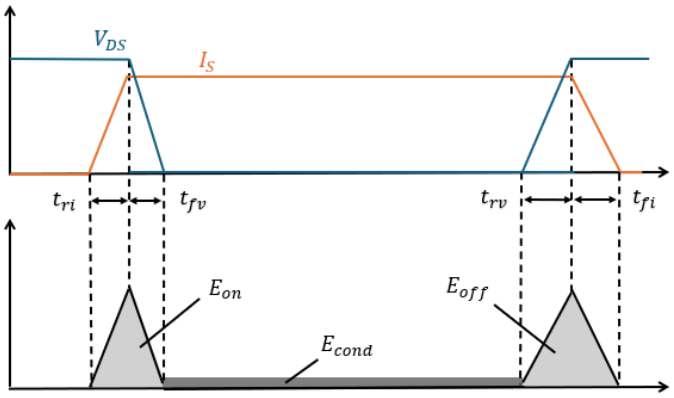


Figure 2.2: Switching loss and conduction loss during the transition between on and off states, including current and voltage rise time and fall time; t_{ri}, t_{fv}, t_{rv} and t_{fi}.

Figure 2.3 illustrates the overlap during the turn-off transient when V_{DS} is rising while i_{DS} is still falling which causes switching losses.

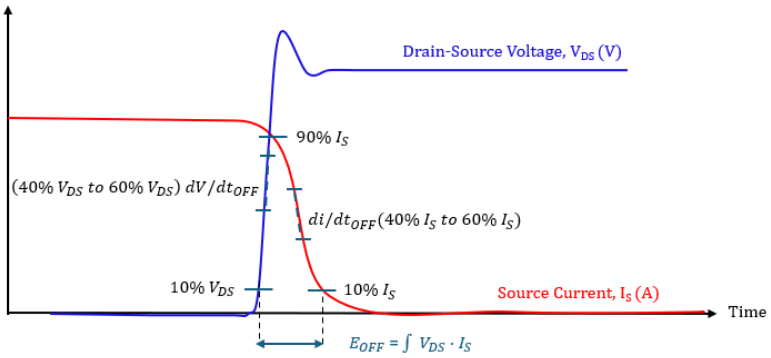


Figure 2.3: Turn-off Transient definitions, inspired by [16]

In Figure 2.3, the slew rate is defined as the slope of the voltage transition from 40% to 60% of V_{DS} [16]. Similarly, the current slew rate is determined by the slope of the current decline from 60% to 40% of the drain current (Ids). Slew rate refers to the rate of change in voltage or current over time during a switching event. These rates are critical for understanding switching dynamics, as they directly influence switching losses, voltage overshoot, and overall system efficiency during transitions.

A high slew rate typically reduces switching losses but can lead to increased electromagnetic interference and voltage stress on components. A controlled, lower slew rate can reduce EMI and improve reliability, though it may increase switching losses. Understanding the switching behaviour of MOSFETs is critical in designing efficient converters and motor drive systems.

2.1.1 Switching Losses

Switching losses in a power MOSFET occur during the transitions between the on-state and off-state, when both the drain current i_{DS} and the drain-to-source voltage V_{DS} are non-zero at the same time. This causes power dissipation inside the MOSFET and the switching energy can be calculated using the expression

$$E_{sw} = \int V_{DS}(t)\ i_{DS}(t)\ dt \tag{2.1}$$

which is a simplified way of calculating the switching losses. Using (2.4) the switching energy can be presented using measured value of V_{DS} and i_{DS}.

The switching losses are typically characterized by the energy dissipated per switching event and the switching frequency, P_{on} can be calculated using the equation

$$P_{on} = \frac{1}{2}\ V_{DS}\ I_{DS}\ (t_{ri} + t_{fv})\ f_{sw} \tag{2.2}$$

where P_{on} is the switching loss during the turn-on event, per cycle in watts, V_{DS} is the drain-to-source voltage in volts, and I_{D} is the drain current in amperes during the switching event. Additionally, t_{ri} is the rise time of the current waveform in seconds, and t_{fv} is the fall time of the voltage waveform in seconds. Finally, f_{sw} represents the switching frequency in hertz. Moreover, P_{off} can be calculated using the eqaution

$$P_{off} = \frac{1}{2} V_{DS}\, I_{DS}\, (t_{rv} + t_{fi})\, f_{sw} \tag{2.3}$$

The switching loss for a IGBT and MOSFET can also be derived from the expression

$$P_{sw} = f_{sw}\ E_{sw} \left(\frac{1}{\pi}\ \frac{I_{out}}{I_{ref}}\right)^{K_I} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \tag{2.4}$$

where E_{sw} is the switching loss obtained from a reference voltage and current, V_{ref} an I_{ref}

2.1.2 Conduction Losses

Conduction losses in a power MOSFET refer to the energy dissipated as heat when the device is on and conducting current. Unlike switching losses, which occur during the brief transitions between on and off states, conduction losses happen during the entire period that the MOSFET remains in the on-state. The conduction losses can be calculated as

$$P_{cond} = I_{D,RMS}^2\ R_{DS(on)} \tag{2.5}$$

where I_{DS} is the drain current during conduction and $R_{DS(on)}$ is the drain-to-source on-resistance of the MOSFET.

The selection of a MOSFET's voltage rating has a direct impact on its conduction losses, primarily through its influence on the $R_{DS(on)}$ [17]. As the rated drain-source

voltage increases, the internal structure of the MOSFET must be adapted—specifically, by increasing the thickness and reducing the doping of the drift region—to withstand higher voltages. This structural change leads to a significant increase in $R_{DS(on)}$, which in turn raises conduction losses, especially under high current conditions.

For a given device footprint or packaging constraint, a 10% increase in voltage rating can result in more than a 25% increase in on-resistance [17]. While higher voltage ratings improve robustness against transient overvoltages, they also degrade efficiency due to elevated conduction losses.

2.1.3 Voltage Overshoot

When the transistor is switched off, the current flowing through the inductor or load has to find another part, which will be through the body diode off the opposite transistor, and the stored energy causes a sudden voltage spike, illustrated in Figure 2.4.

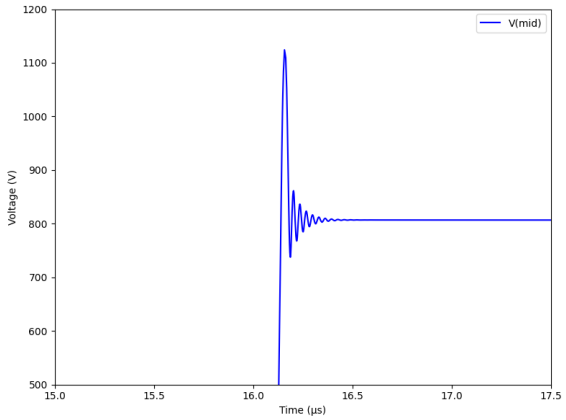


Figure 2.4: Voltage overshoot observed across the drain-source terminals during turn-off.

The magnitude of this overshoot is directly related to the stray inductance and the rate of current change. Stray inductance, also referred to as parasitic inductance, is the inherent inductance present in a circuit due to the layout and configuration of the components and their connections. Figure 2.5 presents the circuit module with stray inductances. Paracitic inductances comes from the bond wires connecting the gate driver and the SiC MOSFET. The higher the current at the moment of switching, the worse the overshoot.

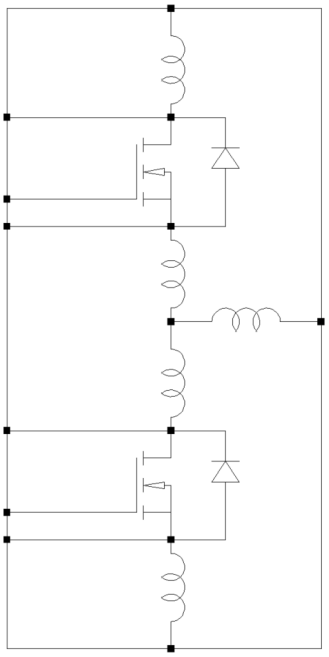


Figure 2.5: SiC module with stray inductance illustrated.

The magnitude of the voltage overshoot increases as the stray inductance and the rate of current change increase. This can be derived from the relation

$$\Delta V = -L_{STRAY} \frac{di}{dt} \tag{2.6}$$

where L_{stray} represents the stray inductance of the circuit, and $\frac{di}{dt}$ is the rate at which current changes during the turn-off process.

The effects of voltage overshoot due to stray inductance can be detrimental. First, the overshoot can cause device stress by exceeding the voltage rating of the device, which may lead to permanent damage or degradation. Additionally, the high voltage spikes generated during switching can result in Electromagnetic interference (EMI), which can disrupt the operation of nearby electronics and compromise system performance. Another concern is the impact on insulation breakdown, where the high voltage stresses the insulation materials in the device or surrounding components, potentially causing partial discharge and eventual failure.

2.1.4 Diode Reverse Recovery

The reverse recovery current shown in Figure 2.6 indicates the behaviour of the diode when it transitions from a conducting state, during forward bias to a non-conducting state, with reverse bias. When the diode switches from conducting to blocking, the stored charge within the diode must be removed. During this process, the current flows in the opposite direction, causing it to go below zero.

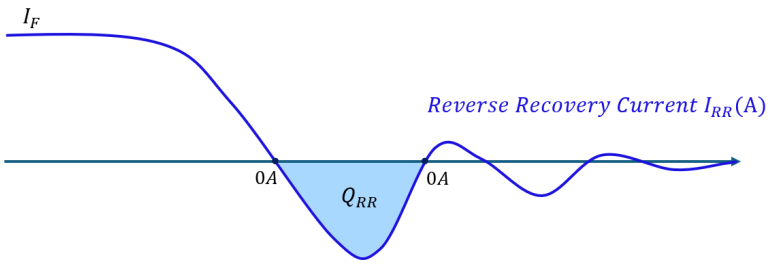


Figure 2.6: Diode Reverse Recovery.

This reverse recovery current introduces additional switching losses and can lead to increased power dissipation in the circuit. In MOSFET-based circuits, this reverse recovery effect can degrade performance, generate electromagnetic interference (EMI), and shorten the lifespan of the components.

2.1.5 External Gate Resistance

The value of gate resistance significantly impacts the switching speed of a transistor, such as a MOSFET. Gate resistance controls the current flowing into or out of the gate, thus affecting both the rise and fall times during switching. When designing a gate driver, several factors must be considered, including transient overshoots, current and voltage spikes, Electromagnetic Compatibility (EMC), and the *di/dt* of the power MOSFET.

A higher gate resistance increases the time required to charge and discharge the gate capacitance, resulting in slower switching (weak gate drive condition), presented in Figure 2.7. It also helps to damp oscillations caused by parasitic inductance and capacitance in the circuit. This creates a trade-off between achieving fast switching speeds (with lower switching losses) and ensuring stability and controlled switching. While low gate resistance can lead to drain-source voltage overshoots, excessively high resistance can increase switching losses making it essential to select the appropriate gate resistance value [18].

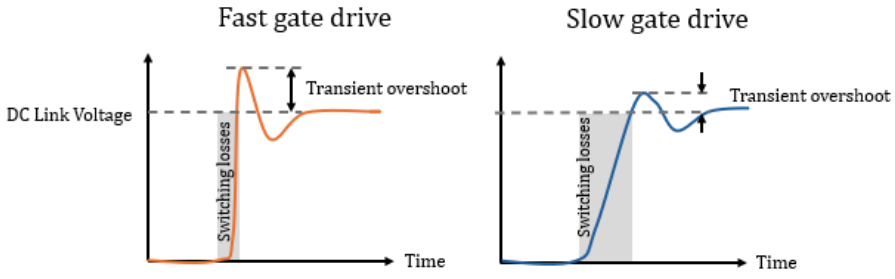


Figure 2.7: Trade-off between slow and fast gate drive.

The choice of gate resistance is limited by the ripple during drive performance, from a drive ability point of view [18]. The element of the gate resistance of the design of the gate drive is important in the trade off between the fast fall and rise times and the oscillations [18].

2.2 DPT

During the operation of a power MOSFET in a typical switching converter circuit, the voltage and current waveforms across various terminals change over time as the MOSFET switches between its on and off states. These transitions can be understood by dividing the switching cycle into four key time intervals, illustrated in Figure 2.8. At time t_1, the gate voltage rises to V_g, turning the MOSFET on. This causes the drain-to-source voltage V_{DS} to drop from V_{dc} to nearly zero, allowing current to flow through the device. The inductor current i_L begins to increase due to a positive inductor voltage V_L. V_{DS} remains low, and i_L continues rising toward the value I_{M1} as the inductor stores energy. At t_2, the gate voltage drops to zero, turning the MOSFET off. V_{DS} rises back to V_{dc}, and the current through the MOSFET, i_{DS}, falls to zero. However, i_L continues flowing through the body diode. At t_3, the gate voltage is high again, turning the MOSFET on for a second time. As the device begins to conduct, V_{DS} drops rapidly to near zero. Between t_3 and t_4, V_{DS} remains low, and i_L begins to rise once more due to a positive V_L, indicating that the inductor is storing energy again. At t_4, the gate voltage goes low, turning the MOSFET off once again and V_{DS} rises toward the supply voltage.

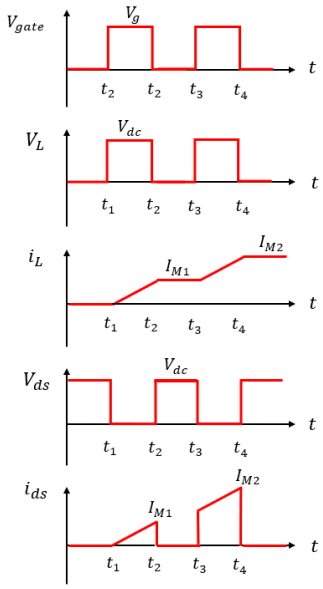


Figure 2.8: Ideal waveforms for a SiC Power MOSFET during a Double Pulse Test.

The low-side MOSFET acts as the Device Under Test (DUT), with the high-side MOSFET remaining inactive during the test, where the DUT is exposed to the double pulse switching. Even though the high-side MOSFET is unactive during the test, it completes the circuit path and allows freewheeling during the off period.

Under the DPT, the device is turned on for a specified duration, during which it charges the load inductor. This phase is referred to as the charge pulse. The current will gradually increase until it reaches the desired load current. The time required

to achieve this value is influenced by the size of the inductance, with a larger inductance resulting in a slower rate of current increase. At the end of the first pulse, the Device Under Test (DUT) is switched off, enabling the measurement of its off-state characteristics. The turn-off process is initiated by disabling the low-side device once the desired load current is reached. The current freewheels through the high side diode and the load inductor. The low side device is then turned on again. The current through the high-side body diode decreases to zero, while the low side device is conducting the current from the inductor. However, the current will drop bellow zero causing a reverse recovery event due to the non-ideal behaviour of the diode. The DPT is completed by turning off the low side device for a second time.

2.3 PM Machine Basics

The demand for high efficiency electric machines constantly increases, with this the need of PMSM for EV applications also increases in spite of high costs due to their superior efficiency [19]. This is due to high power density, high operation efficiency and wide constant power operating region [20].

There are two electrical limits for a PMSM drive the voltage limit, from the inverter restrictions such as the maximum available DC bus voltage and the current limit imposed by the motor, with the rated current.

Equations for the voltage in the d and q axis of a synchronous PM machine at steady state can be expressed as

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} R_s & -w_e L_q \\ w_e L_d & R_s \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \lambda_m w_e \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{2.7}$$

where v_d and v_q are the d- and q-axis components of stator terminal voltage, i_d and i_q are the d- and q-axis components of stator current. λ_m is the flux linkage of the PM, and ω_e is the rotor (electrical) angular velocity. R_s is the resistance of phase winding, L_d and L_q are the d- and q-axis components of armature winding self-inductance. [20].

For surface mounted PM machines, the electromagnetic torque of the PMSM can be found from the relation

$$T_e = \frac{3}{2}\frac{P}{2}\lambda_m i_q \tag{2.8}$$

where P is the pole number. Since the flux linkage of the permanent magnets is constant, the electromagnetic torque is proportional to the q- axis current.

2.4 Control Techniques

To achieve reliable and high-performance motor drive systems in EV applications control techniques play a crucial part. The choice of control strategy will depend on the specific requirements of the application. Some of the control strategies will be presented in the following sections.

2.4.1 FWC

Field weakening control is used in a PMSM to allow operation above base speed at the expense of reduced maximum available torque. As the stator terminal voltage approaches the limit of the inverter output, the speed of the PMSM is limited. To exceed this speed, the field weakening technique reduces the magnetic field strength, allowing higher speed at a lower voltage. This can be done by reducing the d-axis current of the motor's rotor flux, weakening the magnetic field and allowing the motor to run faster without exceeding the voltage limit of the inverter, but at the cost of reduced maximum available torque.

At low speeds, the back EMF (Electromotive Force) is low, allowing high torque production, and at high speeds, the back EMF increases, limiting the voltage available for further speed increase. To extend speed range, flux weakening reduces the magnetic flux by injecting negative d-axis current, reducing the influence of the permanent magnets. This enables the motor to operate at constant power while staying within voltage and current constraints. The advantages of this method are, extending the speed range beyond the base speed, enabling constant power operation at high speeds.

2.4.2 FOC

FOC necessitates the conversion of stator currents from the stationary reference frame into the rotor flux reference frame, commonly referred to as the d-q reference frame. Field Oriented Control(FOC) allows for decoupling the torque and flux control, enabling precise control of the torque, and thus also of the speed. The stator current is divided into the two components q-axis and d-axis, responsible for generating torque and flux respectively.

When using the FOC algorithm to operate a motor at rated flux, the maximum speed is constrained by factors such as stator voltages, rated current, and back EMF, defining the base speed. Above this speed, motor operation becomes more complex due to the back EMF exceeding the supply voltage. However, by setting the d-axis stator current (Id) to a negative value, the rotor flux linkage decreases, enabling the motor to exceed the base speed.

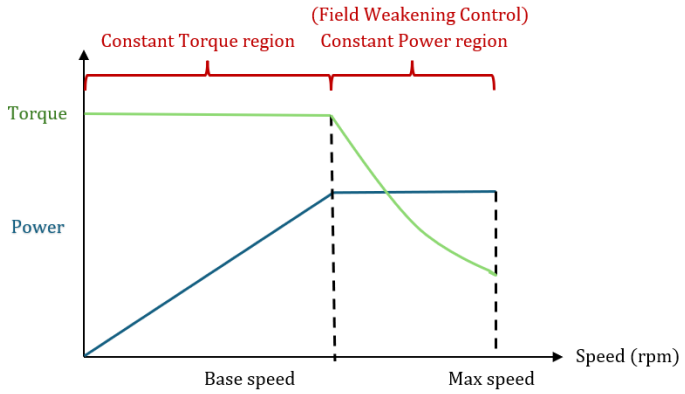


Figure 2.9: Torque and power curves as functions of motor speed, highlighting constant torque region and constant power region.

2.4.3 Current Control

When the PM machine is in the constant torque region, below base speed, the voltage required is lower than the maximum available voltage allowing the d-axis current and q-axis current to be controlled smoothly and independently. However, as the speed rises above base speed and enters the field weakening region, there are some challenges with the control of PM machines [20]. One of these is the limitation of available DC bus voltage which can cause instabilities of the current and torque in the deep field weakening operation region [20].

When the commanded voltage is greater than the maximum voltage available, the currents of the d- and q-axis are coupled and is no longer be separately controlled [20]. Furthermore, PM machine's operating point can smoothly make a transition between motoring and generating modes.

2.4.4 MTPA

One method of controlling high-efficiency motors is MTPA control, which allows full usage of the motor torque [21]. Furthermore, MTPA control evaluates both PM and reluctance torque providing maximum resulting torque. The selection of the exact approach to implement MTPA algorithms strongly depends on both the specific motor drive as well as design targets [21].

The MTPA can be characterised from the relationship between the current components i_d and i_q

$$i_d = \frac{\lambda_m}{2(L_q - L_d)} - \sqrt{\frac{\lambda_m^2}{4(L_q - L_d)^2} + i_q^2} \tag{2.9}$$

if L_d, L_q & λ_m are independent of i_d & i_q. [22]. Where L_d and L_q are the inductances along the d-axis and q-axis, respectively.

The MTPA control, which is used to generate the highest possible torque, is suitable below the base speed [23]. The principle is to control the operating point of the motor in order to achieve the maximum torque for the least current. This is done by adjusting the voltage vector such that the motor operates on a trajectory that provides maximum torque per unit of current. MTPA requires real-time knowledge of the operating conditions of the motor, e.g speed, current and voltage.

2.4.5 Conduction Losses

Conduction losses occur primarily in the stator windings due to their electrical resistance, of the current-carrying components. As current flows through the stator, electrical energy is dissipated as heat, which reduces the overall efficiency of the machine.

These losses are influenced by several factors, including the load on the machine, operating temperature, and the material properties of the stator windings. Additionally, as temperature rises, the resistance of the winding conductors increases, further amplifying these losses. Using materials with low resistivity, such as copper, helps minimize conduction losses.

2.4.6 Winding Insulation

The winding insulation system in electric machines ensures electrical isolation between conductive elements within the stator and rotor. Its primary role is to prevent short circuits between turns, phases, and between the windings and the core (ground), thereby safeguarding the machine's functionality and operational reliability [24]. Winding insulation is especially critical in machines driven by voltage-source pulse-width modulation (PWM) inverters, where the fast voltage rise times (high dv/dt) and high-frequency switching of wide-bandgap (WBG) semiconductors lead to increased electrical stress.

One of the most critical failure mechanisms for insulation is partial discharge, a localized dielectric breakdown that occurs in micro-voids or defects within the insulation material when the electric field exceeds the local dielectric strength—often triggered by PWM-induced surges [24]. Partial Discharge (PD) activity can lead to progressive degradation such as delamination, erosion, or cracking of the insulation, ultimately resulting in electrical failure.

Insulation systems are classified in the IEC 60034-18 standard into Type I and Type II [25]. Type I systems (typically used in low-voltage, random-wound motors) are based on organic insulation and are not expected to experience PD under normal operation. Type II systems (often used in form-wound, high-voltage machines) are designed to tolerate PD activity over extended periods, provided that its magnitude remains within acceptable limits.

The insulation thickness and design must therefore be adequate to withstand not

only thermal and mechanical stresses but also these newly dominant electrical stresses. Common stress types are grouped under the TEAM framework: Thermal, Electrical, Ambient, and Mechanical [24]. While thermal and mechanical degradation have historically been the main ageing factors, modern drive systems require careful consideration of electrical stress due to increased switching frequencies. Proper insulation design, material selection, and condition monitoring (e.g., PD detection) are essential to ensure long-term reliability, particularly as insulation remains one of the most failure-prone components in electric drives.

2.5 Battery

The state of charge (SOC) refers to the remaining capacity of a battery cell as a percentage of its total capacity and is a crucial parameter that indicates the battery's performance [1]. Since the battery stores energy chemically and cannot be directly accessed internally, the SOC cannot be measured directly [26]. Instead, it is estimated using measurable battery variables, such as voltage and current. Figure 2.10 presents the usable SOC range is indicated in the middle portion of the curve, avoiding the regions near full charge and deep discharge.

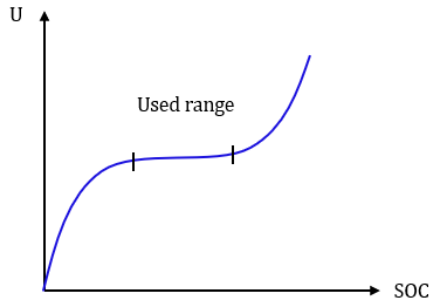


Figure 2.10: Battery terminal voltage as a function of state of charge (SOC).

The initial SOC refers to the estimated or assumed SOC value of a battery at the start of a simulation, experiment, or operation cycle. It serves as the baseline for tracking the battery's charge or energy content over time.

2.6 WLTP

The Worldwide Harmonized Light Vehicle Test Procedure (WLTP) is a standardized method developed at the United Nations level through UNECE, used to assess vehicle performance under realistic driving conditions [27] [28].

The WLTP includes a series of predefined test cycles that simulate a variety of driving scenarios . One of these cycles represents low-speed urban driving, mimicking city traffic with frequent stops and low speeds. Another cycle simulates suburban and highway driving, which involves steady, higher-speed driving on suburban roads and highways. Additionally, the WLTP incorporates a cycle for acceleration and

deceleration, representing aggressive driving behaviors with rapid changes in speed. These test cycles together provide a comprehensive and realistic evaluation of vehicle performance in different real-world conditions.

3

Case Set-up

This chapter presents the Case Set-up used in the study. It describes the simulation setup of switching behaviour through DPT simulations in LTspice and the electric machine set-up in Motor-cad.

3.1 DPT Set-up

In Figure 3.1 the Double Pulse Test setup in LTspice is illustrated, which is used for the analysis of the switching behaviour, in form of switching losses and voltage overshoot of the SiC MOSFET under specific conditions. The setup is a half-bridge configuration consisting of two MOSFETS.

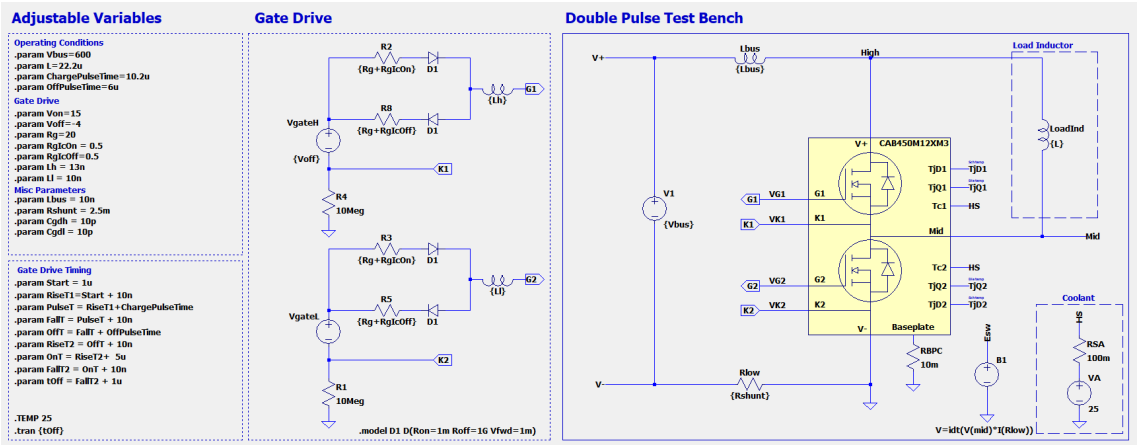


Figure 3.1: Double Pulse Test Setup in LTspice

The SiC MOSFET module used for this study was chosen from Wolfspeed, and the parameters were set according to the data sheet for the MOSFET model CAB450M12XM3 [16].

The design of the DPT allows for variable key parameters such as DC bus voltage, load inductance, and external gate resistances in the adjustable variables section. The gate drive section enables modification of the gate drive process, while the test bench illustrates the basic circuit used to determine the transient behaviour of the SiC MOSFET under specific conditions. With DPT the device is only switched four times to extract the transient characteristics, and the total time of the duration is

kept very short, i.e tenths of microseconds. The two pulses is illustrated in Figure 3.2

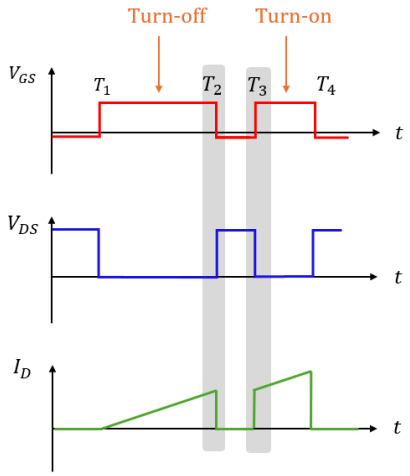


Figure 3.2: Double Pulse Test waveforms illustrating the switching behaviour of the device under test.

The switching losses during turn-on and turn-off events were initially observed to be very similar when using the same gate resistance for both transitions, as presented in Figure 3.3. In this study, to address the challenge of voltage overshoot that occurs during the turn-off event, the gate resistance is adjusted for turn-off $R_{g,\text{off}}$, while maintaining a fixed value for turn-on resistance $R_{g,\text{on}}$.

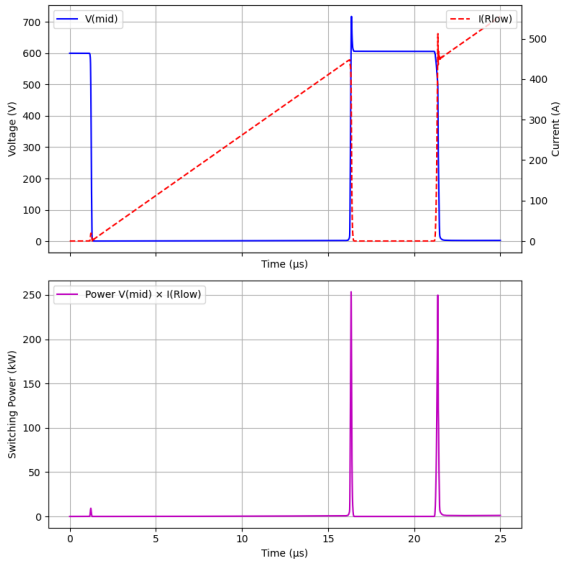


Figure 3.3: The voltage overshoot and the switching losses for turn-on and turn-off events when both $R_{g,\text{on}}$ and $R_{g,\text{off}}$ is 4Ω.

3.2 Electromagnetic Model Setup

An electromagnetic model is used to define the winding configuration and geometric layout of the electrical machine under study. The model is implemented in Motor-CAD, where the machine type and topology are selected, showed in Figure 3.4 and Figure 3.5.

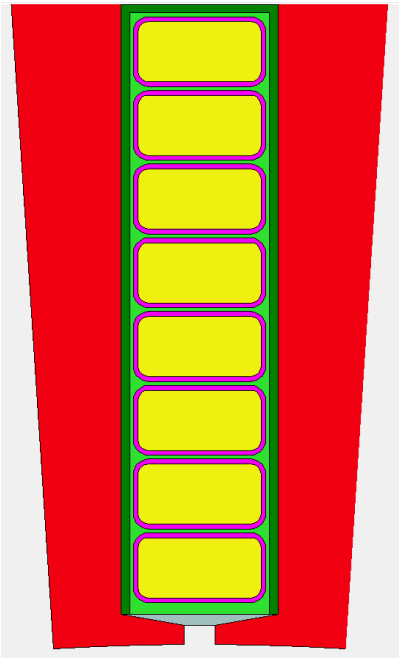


Figure 3.4: Winding layout

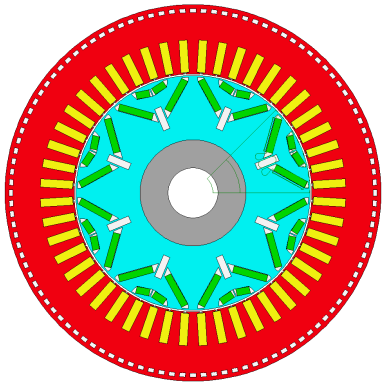


Figure 3.5: Geometry layout

The maximum modulation index is consistently set to 0.93. In order to analyse the impact of the DGD on system behaviour, the DC bus voltage is varied between $400V$, $600V$, $800V$ and $840V$. The corresponding simulation results, including measured data and generated curves, are analysed to evaluate the effect of varying DC voltage on the behaviour and performance of the motor. The power factor distribution is presented in Figure 3.6

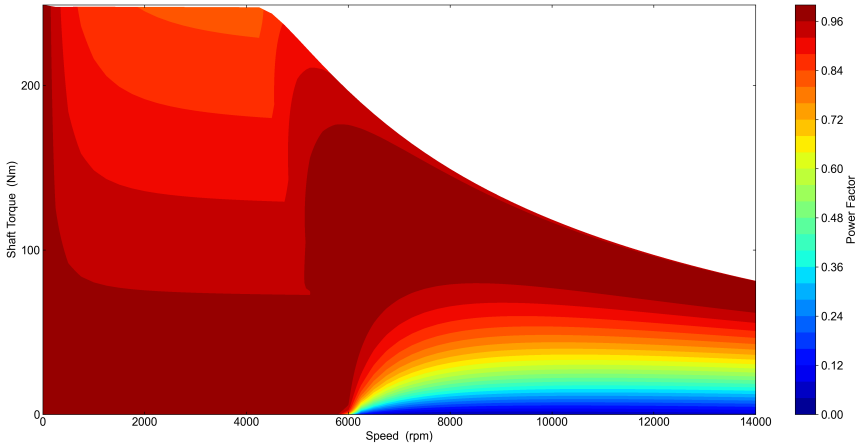


Figure 3.6: Power factor as a function of motor speed, illustrating the variation across the operating range.

3.3 System Set-up

To evaluate the impact of dynamic gate resistance on inverter losses over a driving cycle, a simulation model was implemented using a complete power-train setup. The model illustrated in Figure 3.7 includes the inverters, the electric motor and the vehicle speed profile based on the Worldwide Harmonized Light Vehicles Test Procedure (WLTP).

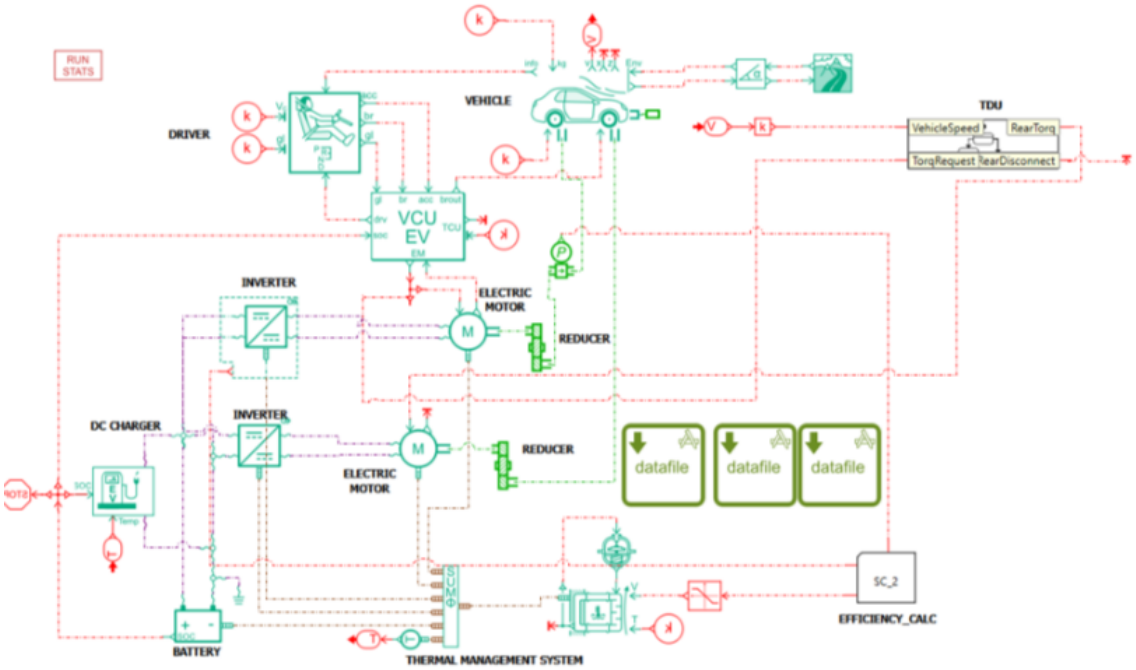


Figure 3.7: System simulation set-up, obtained with Simcenter Amesim and MATLAB.

4

Methodology

This chapter presents the methodology used in the project. It describes the procedure based on the analysation of switching losses and voltage overshoot obtained through DPT simulations, which are used to generate data for further evaluation in Motorcad.

4.1 Validation of Simulation Setup

To validate the case setup, switching losses were calculated through simulation under the conditions stated in the Wolfspeed datasheet of the component, which is marked in the red box in Figure 4.1.

MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_{DS} = 132 mA	
			2.0			V_{DS} = V_{GS}, I_{DS} = 132 mA, T_{VJ} = 175°C	
Zero Gate Voltage Drain Current	I_{DSS}		5	200	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
Gate-Source Leakage Current	I_{GSS}		50	1300	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (MOSFET Only)	$R_{DS(on)}$		2.6	3.4	mΩ	V_{GS} = 15 V, I_D = 450 A	Fig. 2 Fig. 3
			4.7			V_{GS} = 15 V, I_D = 450 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		348		S	V_{DS} = 20 V, I_D = 450 A	Fig. 4
			333			V_{DS} = 20 V, I_D = 450 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{On}		25.4 24.0 24.4		mJ	V_{DD} = 600 V, I_D = 450 A, V_{GS} = -4 V/15 V, $R_{G\text{-}ON(ext)}$ = 4.0 Ω, $R_{G\text{-}OFF(ext)}$ = 0.0 Ω, L_σ = 10.2 nH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{Off}		7.51 8.10 8.35				
Internal Gate Resistance	$R_{G(int)}$		2.5		Ω	f = 100 kHz	
Input Capacitance	C_{iss}		38.0		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		1.5				
Reverse Transfer Capacitance	C_{rss}		35		pF		
Gate to Source Charge	Q_{GS}		385		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V, I_D = 450 A, Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		475				
Total Gate Charge	Q_G		1300				
FET Thermal Resistance, Junction to Case	$R_{th\,JC}$		0.094		°C/W		Fig. 17

Figure 4.1: Wolfspeed, power module datasheet for the MOSFET CAB450M12XM3 [16].

With the same parameters in the datasheet, the DPT resulted in the switching energy 25.6 mJ during turn-off and 7.74 mJ during turn-on. The results of E_{on} and

E_{off} aligned well with the switching energies specified in the datasheet, as illustrated in Figure 4.1.

The waveforms obtained from the DPT simulation were carefully analysed to explore the switching characteristics of the device. The switching losses were then calculated by measuring the energy dissipated during turn-on and turn-off events, based on the voltage and current waveforms captured during the simulation. This analysis helped quantify the impact of gate resistance on the switching performance of the SiC MOSFET.

In the DC bus voltage and the load conditions were also modified during the simulations. These adjustments enabled the exploration of the device's behaviour under different voltage and current levels, providing a comprehensive understanding of the influence of gate resistance under varying operational conditions.

4.2 Analysation of DC Link Voltage and Current Level

The simulations were performed at multiple DC-link voltage levels, ranging from 600 V to 850 V, to assess the sensitivity of overshoot and energy loss to operating voltage. For each gate resistance value, voltage and current waveforms were recorded during both turn-on and turn-off events. The switching losses were calculated by integrating the product of drain-source voltage and drain current over the switching intervals. This approach allowed for a quantification of energy dissipated per switching event as a function of gate resistance and voltage level.

In addition, the influence of load current was studied by simulating switching events at current level 300 A and 450 A. These current levels were chosen to examine how parasitic inductance and switching energy scale with increasing load conditions.

4.3 External Gate Resistance

The main objective is to limit voltage overshoot during the turn-off transient without significantly increasing switching losses. By varying only $R_{g,\text{off}}$, the methodology aims to find a balance between overshoot suppression and overall efficiency, ensuring that switching losses remain minimal while improving voltage transient behaviour during device turn-off.

The gate resistance during turn-on R_{gon} was remained fixed at 4 Ω throughout the test, while the gate resistance during turn-off R_{goff} was varied across five different values: 3.3 Ω, 5.6, Ω, 6.8 Ω, 9.1 Ω, 10 Ω, 12 Ω, 15 Ω, and 20 Ω. These specific values were chosen based on a table of nominal gate resistances commonly used in power electronics applications, shown in Figure 4.2. The chosen gate resistance values allow

for an assessment of the impact of switching speed on the device's performance at varying operating points.

E24	Nominal values of resistances							
1.0	0.01 Ω	0.1 Ω	1 Ω	10 Ω	100 Ω	1 kΩ	10 kΩ	100 kΩ
1.1	0.011 Ω	0.11 Ω	1.1 Ω	11 Ω	110 Ω	1.1 kΩ	11 kΩ	
1.2	0.012 Ω	0.12 Ω	1.2 Ω	12 Ω	120 Ω	1.2 kΩ	12 kΩ	
1.3	0.013 Ω	0.13 Ω	1.3 Ω	13 Ω	130 Ω	1.3 kΩ	13 kΩ	
1.5	0.015 Ω	0.15 Ω	1.5 Ω	15 Ω	150 Ω	1.5 kΩ	15 kΩ	
1.6	0.016 Ω	0.16 Ω	1.6 Ω	16 Ω	160 Ω	1.6 kΩ	16 kΩ	
1.8	0.018 Ω	0.18 Ω	1.8 Ω	18 Ω	180 Ω	1.8 kΩ	18 kΩ	
2.0	0.02 Ω	0.2 Ω	2.0 Ω	20 Ω	200 Ω	2.0 kΩ	20 kΩ	
2.2	0.022 Ω	0.22 Ω	2.2 Ω	22 Ω	220 Ω	2.2 kΩ	22 kΩ	
2.4	0.024 Ω	0.24 Ω	2.4 Ω	24 Ω	240 Ω	2.4 kΩ	24 kΩ	
2.7	0.027 Ω	0.27 Ω	2.7 Ω	27 Ω	270 Ω	2.7 kΩ	27 kΩ	
3.0	0.03 Ω	0.3 Ω	3.0 Ω	30 Ω	300 Ω	3.0 kΩ	30 kΩ	
3.3	0.033 Ω	0.33 Ω	3.3 Ω	33 Ω	330 Ω	3.3 kΩ	33 kΩ	
3.6	0.036 Ω	0.36 Ω	3.6 Ω	36 Ω	360 Ω	3.6 kΩ	36 kΩ	
3.9	0.039 Ω	0.39 Ω	3.9 Ω	39 Ω	390 Ω	3.9 kΩ	39 kΩ	
4.3	0.043 Ω	0.43 Ω	4.3 Ω	43 Ω	430 Ω	4.3 kΩ	43 kΩ	
4.7	0.047 Ω	0.47 Ω	4.7 Ω	47 Ω	470 Ω	4.7 kΩ	47 kΩ	
5.1	0.051 Ω	0.51 Ω	5.1 Ω	51 Ω	510 Ω	5.1 kΩ	51 kΩ	
5.6	0.056 Ω	0.56 Ω	5.6 Ω	56 Ω	560 Ω	5.6 kΩ	56 kΩ	
6.2	0.062 Ω	0.62 Ω	6.2 Ω	62 Ω	620 Ω	6.2 kΩ	62 kΩ	
6.8	0.068 Ω	0.68 Ω	6.8 Ω	68 Ω	680 Ω	6.8 kΩ	68 kΩ	
7.5	0.075 Ω	0.75 Ω	7.5 Ω	75 Ω	750 Ω	7.5 kΩ	75 kΩ	
8.2	0.082 Ω	0.82 Ω	8.2 Ω	82 Ω	820 Ω	8.2 kΩ	82 kΩ	
9.1	0.091 Ω	0.91 Ω	9.1 Ω	91 Ω	910 Ω	9.1 kΩ	91 kΩ	

Figure 4.2: Nominal values of gate resistances [29].

4.4 Conduction Losses

To investigate the connection between voltage overshoot reduction, based on the impact of external gate resistance, and conduction losses, the following assumption was used. By reducing the voltage overshoot, and decreasing the maximum voltage, it becomes possible to safely employ a MOSFET with a lower voltage rating, which impacts the selection of the $R_{DS(on)}$. The relationship considered was

$$R_{DS(on)} = \left(\frac{V_{max}}{V_{nom}}\right)^2 R_{DS,nom} \tag{4.1}$$

where $V_{max} = 1200\ V$ and $R_{DS,nom} = 2.6\ m\Omega$ at $R_{g,off} = 0\ \Omega$ were picked from the Datasheet [16]. Although the design of real-world devices involves additional complexities, this illustrates how effective control of voltage overshoot can facilitate the use of more efficient components.

With a DC link at 800 V, the voltage overshoot was obtained and the marginal between the maximum voltage and the nominal voltage for $R_{g,off} = 0\ \Omega$ was then used in the calculations for $R_{DS(on)}$ for the other gate resistances.

4.5 WLTP Test Procedure

A WLTP test was performed to examine the impact of DGD on inverter and EDU system losses. Operating points were extracted from the WLTP cycle, presented in Figure 4.3. A total of six operating points were selected based on the largest

circles in the energy density plot, which typically represent the most commonly encountered driving conditions during vehicle operation. For each of these points, the corresponding torque and speed values were identified. These values were then used to retrieve the associated differences in switching losses and conduction losses through simulations conducted in LTspice. The losses from these simulations were incorporated into the WLTP model to assess their impact on overall system efficiency.

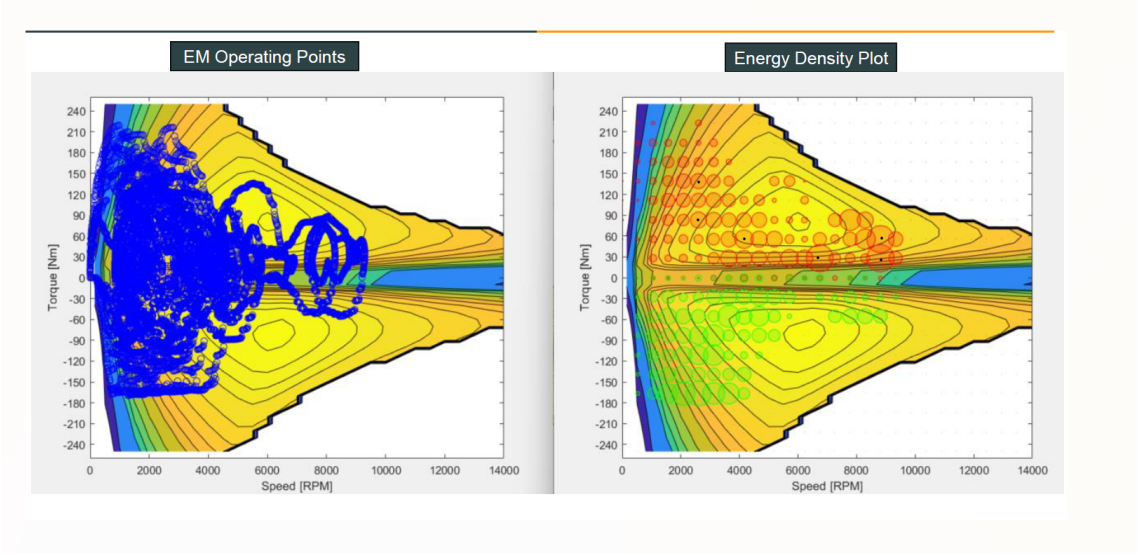


Figure 4.3: Energy density distribution over the motor operating map, indicating regions where the vehicle most frequently operates. The six black markers highlight the selected operating points used for further analysis, chosen based on their high occurrence in the energy density profile.

The approach with DGD is compared to a drive with a fixed external gate resistance. One base case scenario is set, with a fixed gate resistance of 10 Ω. The base case was compared to a gate resistance of 5.6 Ω and 3.3 Ω for both low initial SOC of 30% and at nominal initial SOC of approximately 50%.

4.6 Performance

To evaluate the impact of dynamic gate resistance adjustment on motor drive performance, a comparative simulation study was conducted using two distinct gate resistance values: $R_{g,off} = 10\ \Omega$ (base case) and $R_{g,off} = 20\ \Omega$. Initially, the switching behaviour for each case was simulated to observe the resulting voltage overshoot during turn-off events. The reduction in overshoot observed when the gate resistance was increased from $R_{g,off} = 10\ \Omega$ to $R_{g,off} = 20\ \Omega$. Based on this observation, the DC-link voltage was increased by the same amount of to investigate how the reduced overshoot margin could enable the use of a higher DC bus voltage, i.e. a larger battery, with the same components without exceeding safe device limits.

The adjusted voltage levels were then used as input parameters in drive cycle simulations, where the torque-speed characteristics of the system were evaluated. The simulations examined both the constant torque and constant power regions to identify any performance shifts caused by the increased DC-link voltage. Subsequently, efficiency maps were generated for each configuration to visualize changes in system efficiency across the operating range. These maps were obtained to provide insights into how the improved voltage margin and corresponding increase in DC bus voltage influence overall drive efficiency, particularly in the field-weakening region.

5

Results and Analysis

This chapter presents the analysis of voltage overshoot and switching losses obtained from Double Pulse Test (DPT) simulations conducted in LTspice. Following this, the study assesses switching and conduction losses are under a WLTP drive cycle to determine the loss distribution across different operating conditions. Inverter and cumulative system losses are quantified to evaluate overall efficiency improvements. Furthermore, the impact of the DGD approach on the electric machine's performance is examined to provide a holistic understanding of its effects on the propulsion system.

5.1 Current and DC Link effect

Figure 5.1 illustrates the impact of different gate resistances on voltage overshoot during turn-off. At each voltage level, a higher gate resistances result in reduced overshoot magnitudes. Notably, even moderate increases in $R_{g,\text{off}}$ lead to reductions in overshoot, indicating a damping response. The most significant damping occurs between 0 Ω and 3.3 Ω, where the overshoot drops sharply across all bus voltage levels. Furthermore, the impact of increasing DC-link voltage is most pronounced when $R_{g,\text{off}} = 0$ Ω, showing the largest variation in overshoot magnitude across the tested voltages. For gate resistances above 10 Ω, the influence of DC-link voltage on overshoot becomes much less significant.

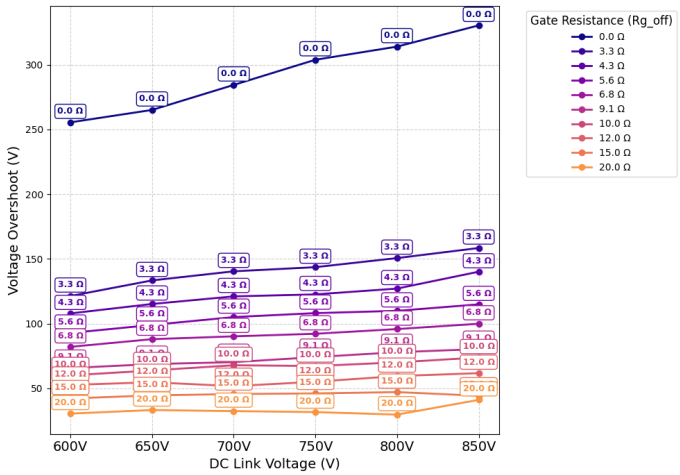


Figure 5.1: The voltage overshoot plotted across a range of gate resistances $R_{g,\text{off}}$ as the DC-link voltage increases from 600 V to 850 V.

The trend observed in Figure 5.2, is that the switching energy increases with higher DC-link voltage for all gate resistances. The lowest energy losses are recorded at $R_{g,\text{off}} = 0\ \Omega$, while the highest occur at 20 Ω, reflecting the slower switching transitions and increased switching duration introduced by higher resistances.

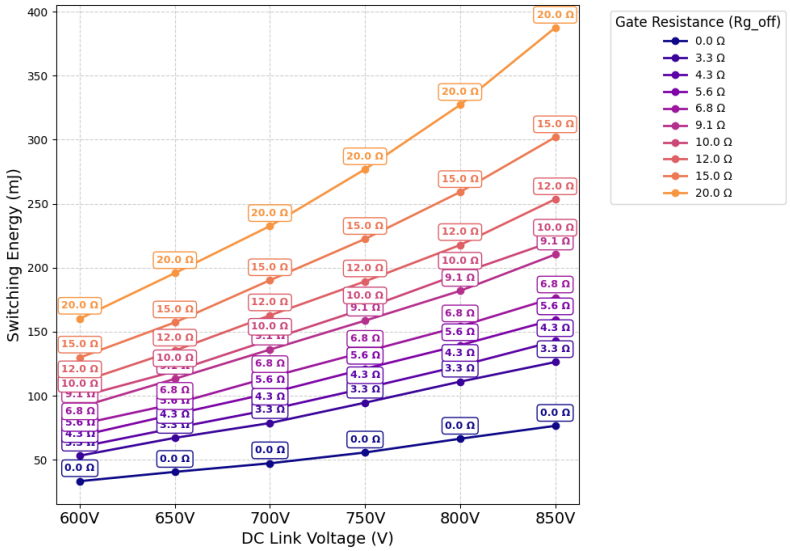
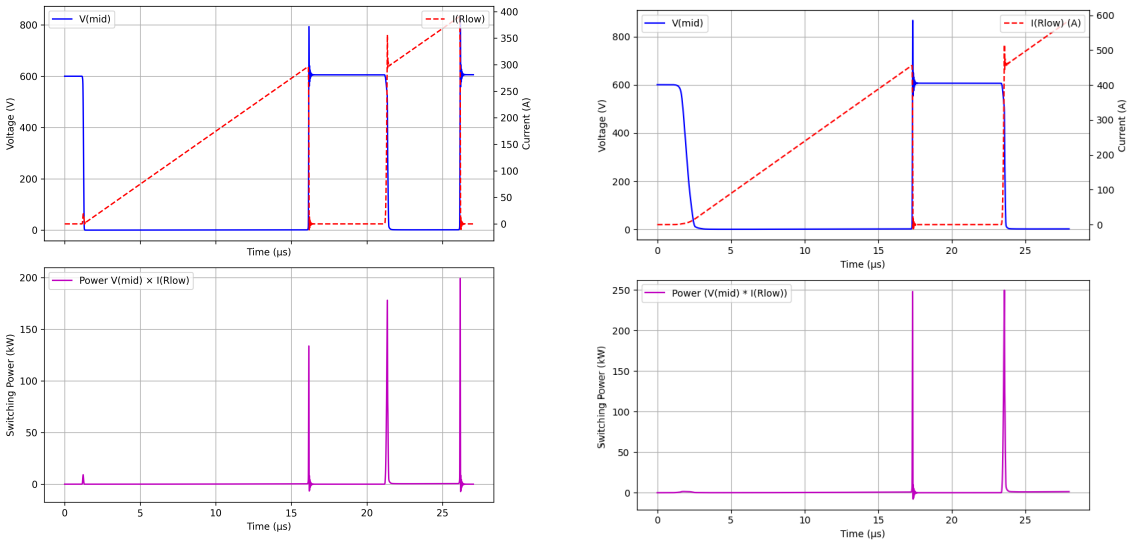


Figure 5.2: Total switching loss for a range of gate resistances $R_{g,\text{off}}$ as the DC-link voltage varies from 600 V to 850 V.

As expected, Figure 5.1 and Figure 5.2 highlights the trade-off between switching speed and loss.

As shown in Figure 5.3, the voltage overshoot increases progressively with higher current levels. Figure 5.3a shows a voltage overshoot of 200 V, when the current reaches a level of 300 A. As the current approaches 450 A in Figure 5.3b, the overshoot magnitude is increased to 250 V. This behaviour highlights the growing impact of parasitic inductance associated with higher load currents. Additionally, the switching losses, indicated by the purple spikes in the waveform, also increase with current. The switching loss is significantly increased during the turn-off event due to the simultaneous presence of high voltage and current, further demonstrating the advantage of reducing the voltage overshoot.



(a) Current reaching 300 A.

(b) Current reaching 450 A.

Figure 5.3: Current and voltage waveforms, along with the corresponding switching energy, measured at load currents of 300 A and 450 A.

5.2 Voltage Overshoot

The voltage overshoot decreases consistently with increasing gate resistance, as observed when varying the external gate resistance from $3.3\,\Omega$ to $20\,\Omega$ in Figure 5.4. With a gate resistance of $0\,\Omega$ the voltage spike is considerably higher, approximately $250\,V$, in relation to the DC Bus voltage, significantly limiting the available voltage level. At $20\,\Omega$, the voltage overshoot is reduced to approximately 30 V, representing the most effective suppression among the tested values.

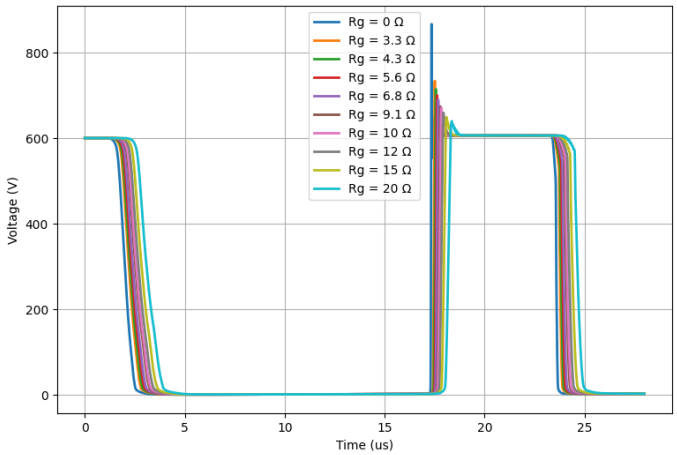


Figure 5.4: Voltage waveforms for varying gate resistance over time illustrating the voltage overshoot, for a DC-link of 600 V.

5.3 Switching Losses

The switching losses for turn-on, turn-off, and the total switching loss with $R_{g,\text{off}} = 0\ \Omega$ and $R_{g,\text{on}} = 4\ \Omega$ are illustrated in Figure 5.5. As observed, the total switching loss increases with rising current, consistent with the behaviour reported in the device data-sheet provided by WOLFSPEED [16]. Turn-on losses exhibit a sharper increase compared to turn-off losses, contributing more significantly to the total switching loss at higher current levels. The trend confirms the dynamic characteristics of the transistor, validating the device's switching performance under increasing load conditions.

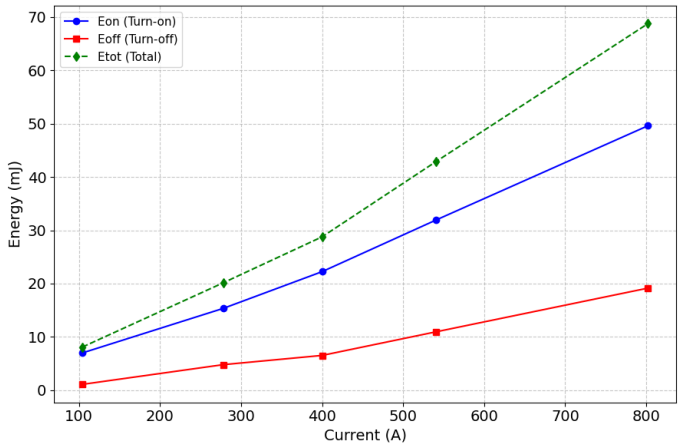


Figure 5.5: Switching energy over drain current.

Figure 5.6 illustrates the switching power loss as a function of current for various gate resistance values. The switching loss increases approximately linearly with current across all tested gate resistances. In addition, the difference in switching loss between the different gate resistances also increases with higher current levels.

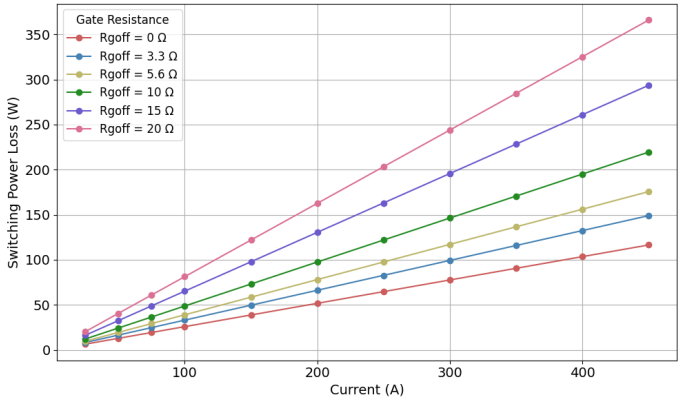


Figure 5.6: Total switching power for the different gate resistances at a DC link voltage of 800 V

5.4 Conduction Losses

By effectively limiting voltage overshoots relative to the DC-link voltage, it becomes possible to use transistors with lower voltage ratings. Increasing the gate resistance $R_{g,\text{off}}$, reduces the voltage overshoot and therefore the maximum voltage. Furthermore, if the maximum voltage can be reduced the value of the $R_{DS(on)}$ can be decreased according to the assumption made, the results are presented in Table 5.1.

Table 5.1: Calculated values for $R_{DS(on)}$ with a range of gate resistances for a DC-link of 800 V, using (4.1).

$R_{g,off}[\Omega]$	$V_{max}[V]$	$R_{DS(on)}[\text{m}\Omega]$
0	1114	2.6
3,3	1037	1.94
4,3	1013	1.85
5,6	996	1.79
6,8	982	1.74
9,1	964	1.68
10	956	1.65
12	946	1.61
15	933	1.57
20	916	1.51

The conduction loss decreases consistently with increasing gate resistance, as observed when varying the external gate resistance from 3.3 Ω to 20 Ω in Figure 5.7. As expected, the conduction loss increases non-linearly with rising current due to the quadratic relationship between current and conduction power dissipation. The conduction loss is significantly high with a gate resistance of 0 V compared to the other values. The lowest conduction loss curve is observed with 20 Ω. The lowest conduction loss curve from the tested values was observed when using an external gate resistance $R_{g,off} = 20\ \Omega$ with $R_{DS(on)} = 1,51\ m\Omega$.

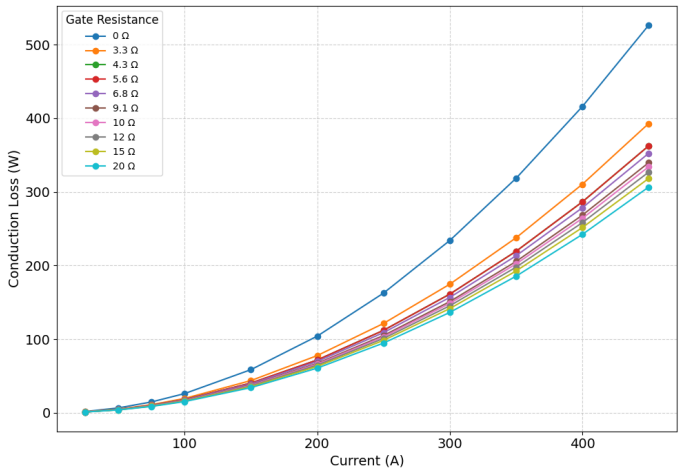


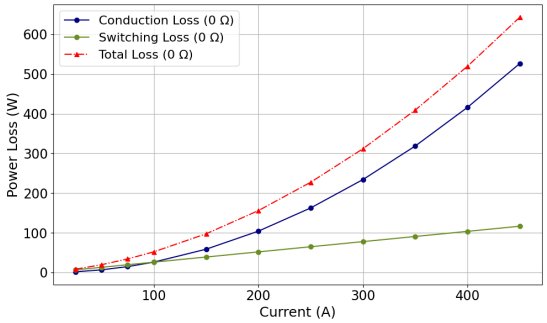
Figure 5.7: Calculated conduction losses using the calculated $R_{DS(on)}$ values with a range of gate resistances for a DC-link of 800 V.

5.5 Inverter Losses

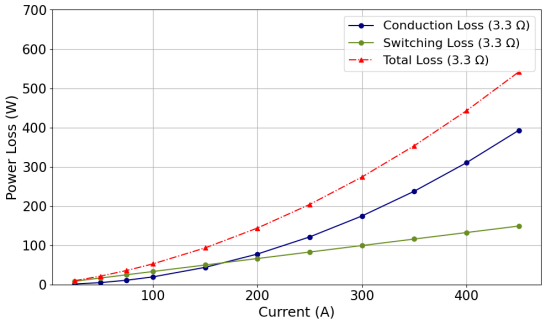
The impact of the selection of $R_{DS(on)}$ leads to two scenarios regarding conduction losses. In the first case, a fixed gate resistance is considered, meaning the chosen $R_{DS(on)}$ must correspond to the specific gate resistance used in the system. In the second case, a variable gate resistance is considered. A higher gate resistance will be applied during voltage overshoot sensitive points. Furthermore, the choice of the $R_{DS(on)}$ can be based on the higher gate resistance used in the system, minimizing conduction losses.

5.5.1 Fixed Gate Resistance

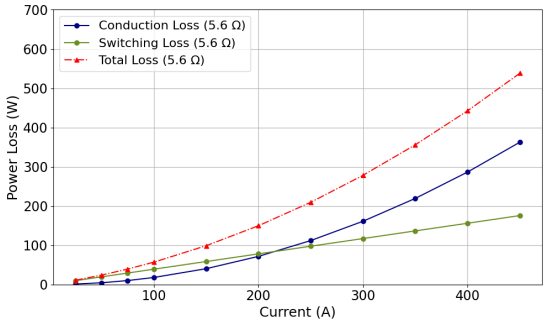
With a fixed gate resistance the total power losses, referring to the switching losses together with the conduction losses, both changes depending on the external gate resistance used, as shown in Figure 5.8.



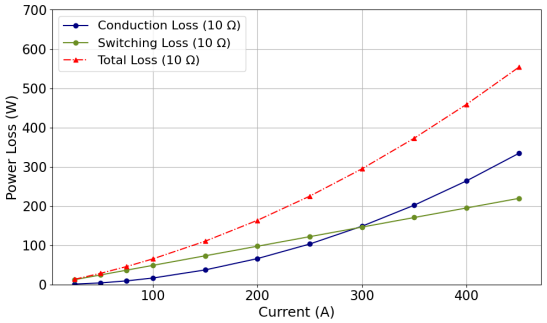
(a) External Gate Resistance 0 Ω



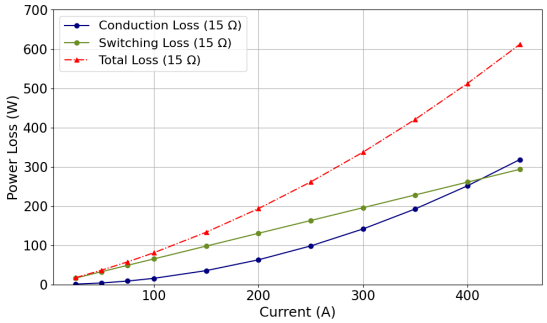
(b) External Gate Resistance 3.3 Ω



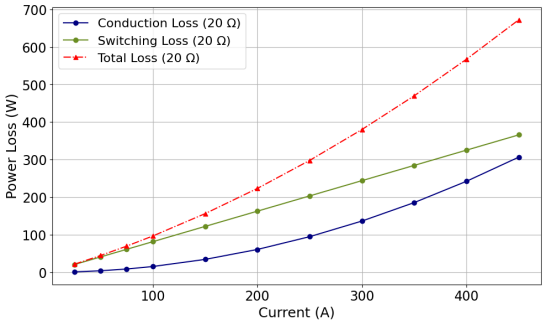
(c) External Gate Resistance 5.6 Ω



(d) External Gate Resistance 10 Ω



(e) External Gate Resistance 15 Ω



(f) External Gate Resistance 20 Ω

Figure 5.8: Total losses at different external gate resistances from 0 Ω to 20 Ω across various current levels.

As can be observed in Figure 5.8, the curve of the total loss varies for the different external gate resistances. Figure 5.9 compares the total power loss curves and their shapes obtained with the different external gate resistances. Moreover, the external gate resistance that gives the lowest total power loss varies with the different current values.

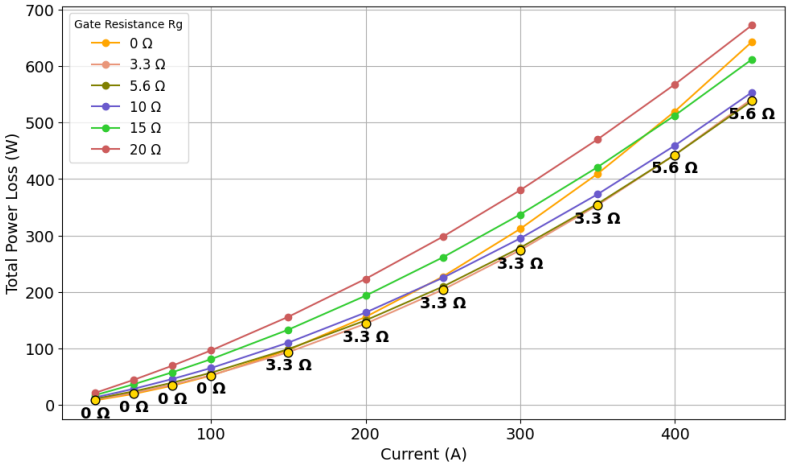
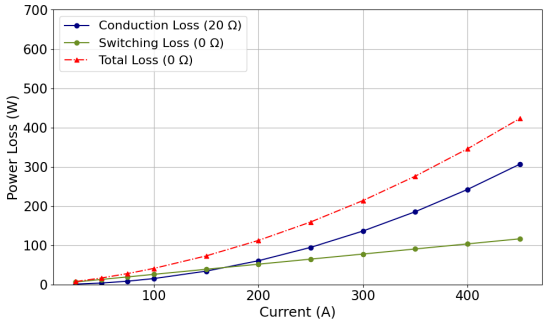


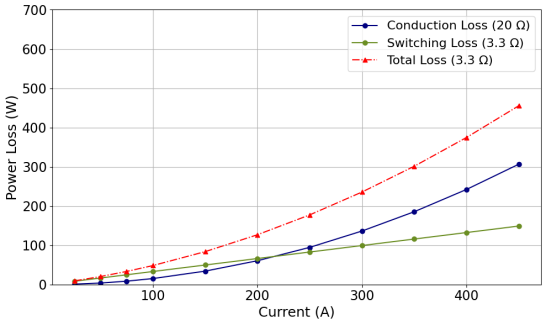
Figure 5.9: Total power loss obtained with various gate resistances, with fixed external gate resistance.

5.5.2 Variable Gate Resistance

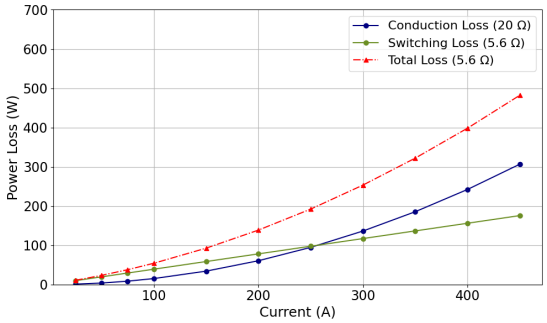
With a variable gate resistance, a higher gate resistance can be used during voltage overshoot sensitive points, allowing a lower value of $R_{DS,on}$ for the transistor. As a result, only the switching losses vary with gate resistance, while the conduction losses remain minimized. The total power losses obtained with the different external gate resistances, when minimizing the conduction losses, are presented in Figure 5.12.



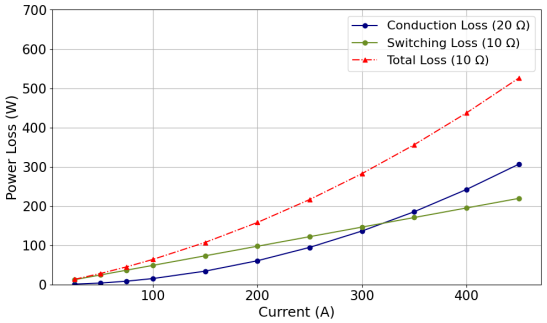
(a) External Gate Resistance 0 Ω



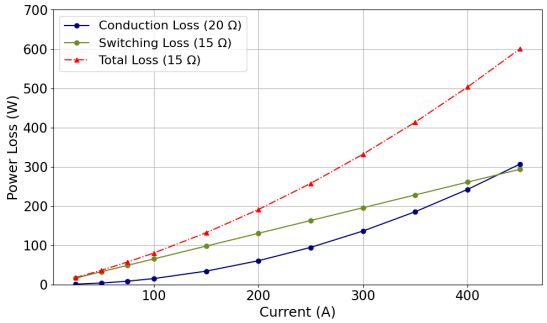
(b) External Gate Resistance 3.3 Ω



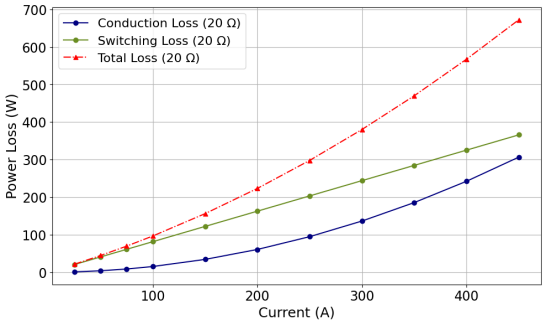
(c) External Gate Resistance 5.6 Ω



(d) External Gate Resistance 10 Ω



(e) External Gate Resistance 15 Ω



(f) External Gate Resistance 20 Ω

Figure 5.10: Total losses at different gate resistances between 0 Ω to 20 Ω across various current levels.

The ability to select a transistor with the lowest $R_{DS,on}$ contributes to minimizing the total power loss across all current levels, as shown in Figure 5.11.

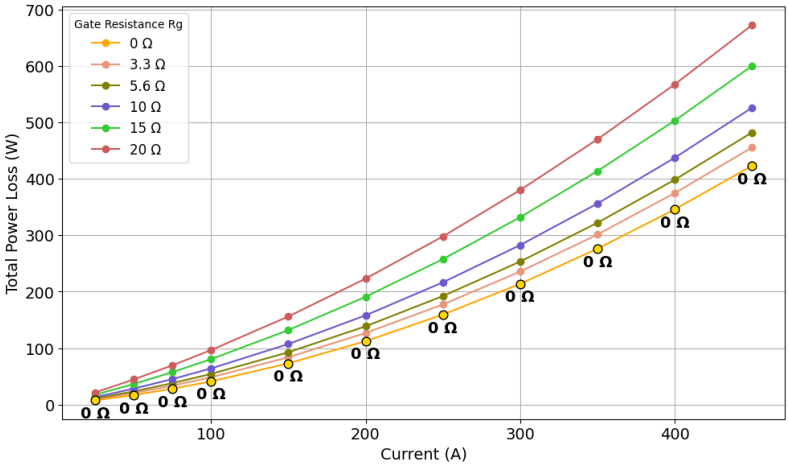
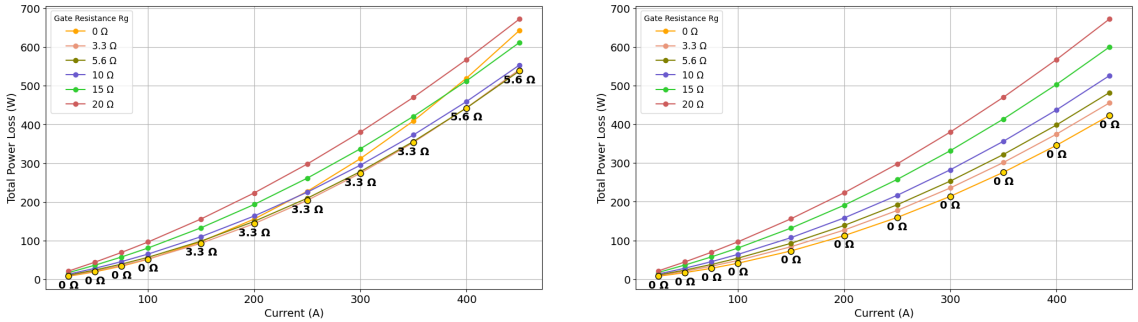


Figure 5.11: Total power loss obtained with various gate resistances, with variable external gate resistance.

Comparing the two conduction loss scenarios, total power losses during current levels between approximately 100 A and 300 A can be reduced when using a variable external gate resistance. At lower current levels, the difference is smaller, and at higher current levels, when the higher gate resistance will be applied, the losses remain the same, as presented in Figure 5.12.



(a) Fixed External Gate Resistance. **(b)** Variable External Gate Resistance

Figure 5.12: Total power losses for the different external gate resistances across current.

Notably, the lowest external gate resistance does not significantly reduce the total losses due to the conduction losses at higher current levels, as shown in Figure 5.12a. The optimal external gate resistance, from a power loss perspective, varies depending on the current level, for a fixed system. The use of a variable external gate resistance, on the other hand, minimises the impact of conduction losses, resulting in minimised total power loss from using a lower external gate resistance across all current levels, shown in Figure 5.12b.

5.6 WLTP cycle

Figure 5.13 presents the inverter losses over a WLTP cycle at low initial SOC of 30% and at nominal initial SOC of approximately 50%. With a reference gate resistance of 10 Ω at low initial SOC, the inverter losses can be reduced with 18.3% and for the gate resistance $R_{g,off} = 3.3\,\Omega$ and 11.7% with the gate resistance $R_{g,off} = 5.6\,\Omega$.

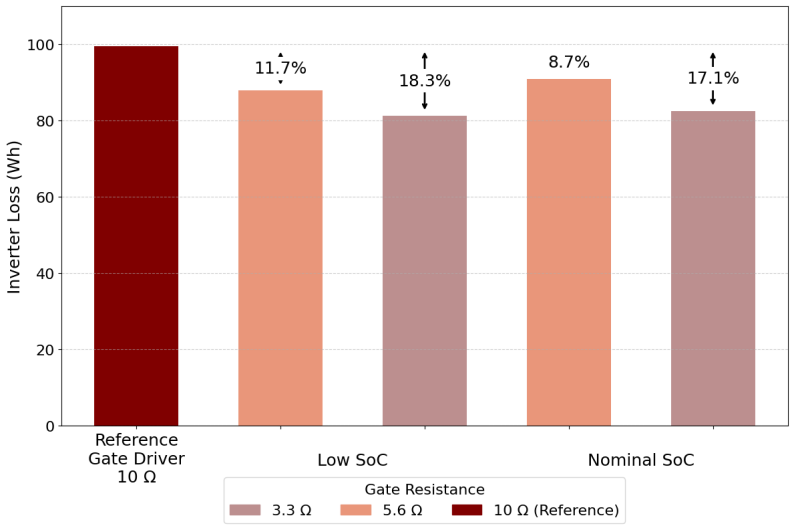


Figure 5.13: Inverter losses over a WLTP cycle at initial SOC levels of 30% and 50%, using a reference gate resistance of 10 Ω at nominal SOC.

The results, shown in Figure 5.14, demonstrate the reduction in cumulative losses, with inverter, EM and transmission losses, relative to the 10 Ω baseline. The loss reduction was 2.8% at low initial SOC and reached up to 2.6% at nominal SOC for the lowest external gate resistances.

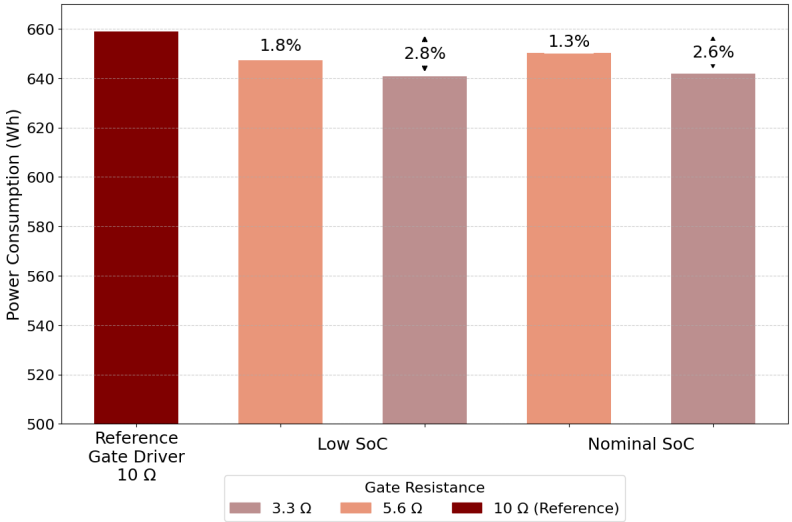


Figure 5.14: Cumulative losses over a WLTP cycle at initial SOC levels of 30% and 50%, using a reference gate resistance of 10 Ω.

5.7 Electric Motor Level

Subsection 4.2.2 demonstrated that gate resistance impacts the voltage overshoot. To examine the impact of the DGD on the electric motor, this is used. The DC Bus voltage is increased with the same amount of voltage that is decreased in the overshoot by using a larger gate resistance.

5.7.1 Performance

Figure 4.6 presents the torque-speed curves for the base case with a fixed gate resistance of 10 Ω versus a higher gate resistance of 20 Ω. When the gate resistance is increased to 20 Ω the voltage overshoot decreases from 70 V to 30 V and the DC Bus voltage is therefore increased with 40 V in order to simulate the possible impact of the DGD on the torque characteristics.

During the constant torque region the impact of the increased DC Bus voltage is negligible, as can be seen in Figure 5.15. However, with a DC Bus voltage of 840 V the base speed is increased from 8750 RPM to 9100 RPM. The increase of base speed results in a difference of approximately 10 Nm between the two curves as the torque decreases in the constant power region.

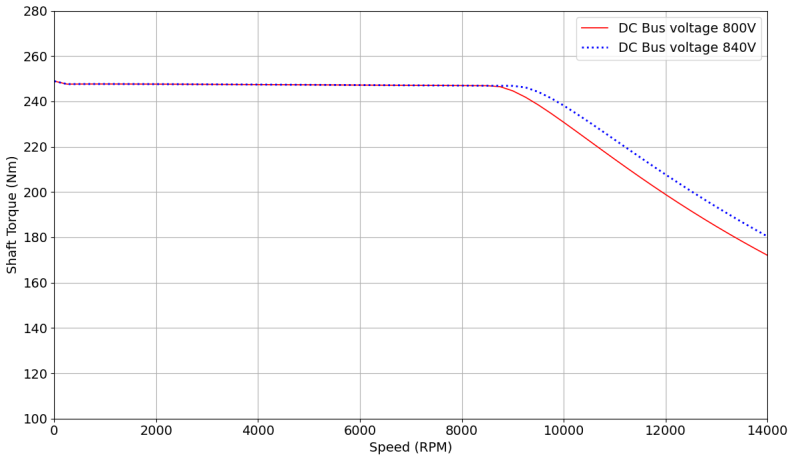


Figure 5.15: The shaft torque with a DC Bus voltage of 800 V, representing $R_{g,off}$ =10 Ω and 850 V, representing $R_{g,off}$ = 20 Ω.

Figure 5.16 shows the impact of the increased torque on the power-speed characteristics in the field-weakening region. DC Bus voltage of 840 V provide about 4.84% more peak power at top speed compared to DC Bus voltage of 800 V, as a result of increasing the torque. In addition, the acceleration time from 80 to 160 km/h is improved by 0.2 seconds when using 840 V with a DGD, compared to 800 V with a conventional gate driver.

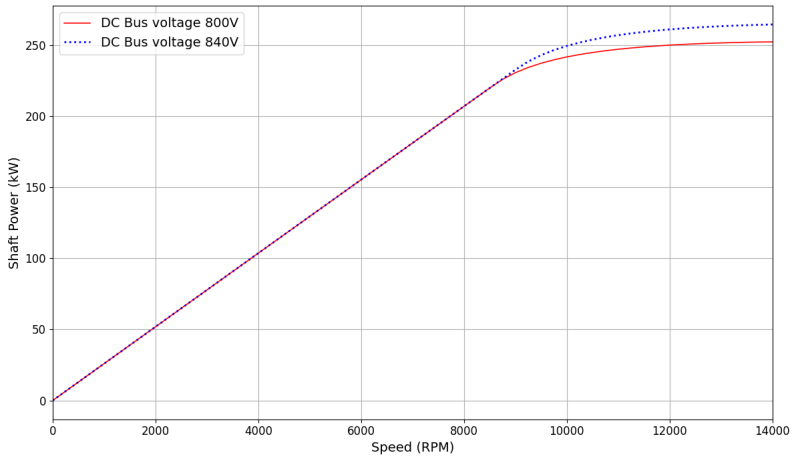
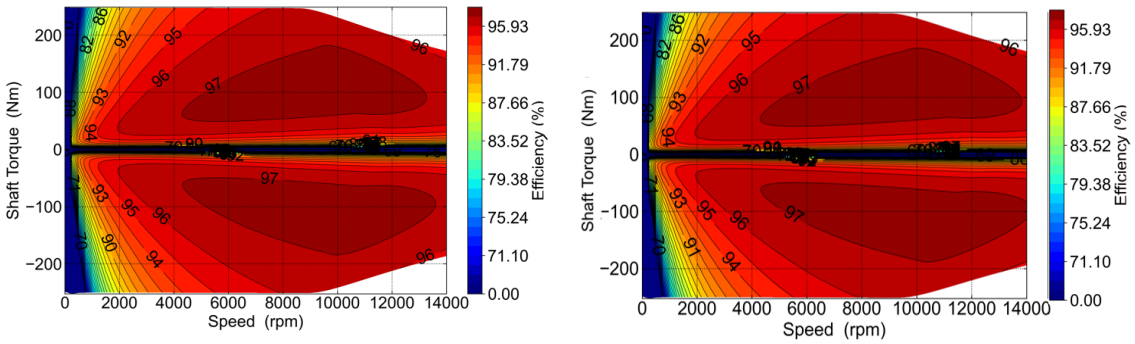


Figure 5.16: The shaft power with a DC Bus voltage of 800 V, representing $R_g = 10\,\Omega$ and 850 V, representing $R_g = 20\,\Omega$.

The resulting efficiency maps are shown in Figure 5.17. The efficiency for the two cases are the same until the field weakening region, with a DC Bus voltage of 840 V, the peak efficiency level expand over a larger operating area.



(a) DC Bus voltage of 800 V **(b)** DC Bus voltage of 840 V

Figure 5.17: The efficiency over the shaft torque characteristics.

Although the WLTP cycle indicates that the vehicle predominantly operates at lower speeds, where the improvement has limited effect, the enhancement remains of interest from a system design perspective. From a broader perspective, the relation between DGD and the electric motor is not straight forward. While lower voltage overshoot could, in theory, enable the use of a higher system voltage, thereby reducing current and associated winding losses, this is not easily realized in practice. The system voltage is typically fixed due to design constraints and safety margins, and increasing it may necessitate de-rating under fully charged conditions, making such adjustments unlikely without significant system-level changes. Furthermore, although improved transient control could potentially allow for reduced insulation thickness, such implications remain speculative and would require a detailed evaluation of insulation standards and long-term reliability considerations.

6
Discussion

In terms of switching performance, a lower gate resistance is generally considered beneficial, as it tends to enable faster switching by reducing the time required to charge and discharge the gate capacitance, which may help reduce switching losses. However, conduction losses also play a significant role in determining overall inverter efficiency. This study considers two scenarios: one with a fixed external gate resistance, where the $R_{DS(on)}$ is selected to accommodate higher current levels, and another with a dynamic gate driver, allowing variation in gate resistance during operation. In the latter case, it may be possible to take advantage of an assumed relationship between voltage rating and $R_{DS(on)}$.

While switching losses are typically reduced with lower external gate resistance during turn-off, conduction losses decrease with higher gate resistance, due to reduced voltage overshoot and a corresponding decrease in required voltage rating and $R_{DS(on)}$. Additionally, higher DC-link voltages can reduce the required current, which could further lower conduction losses and partially counteract increased switching losses. By dynamically adjusting gate resistance, it may be possible to minimize both switching and conduction losses, while also improving the effective utilization of the DC-link voltage with the same components. However, the precise impact of selecting a specific $R_{DS(on)}$ value on overall efficiency and system behaviour remains uncertain and would require further investigation. In the WLTP cycle analysis of the inverter and system simulations conducted in this study, conduction losses were assumed to be constant, using $R_{DS(on)} = 2.6\,\mathrm{m\Omega}$ from the datasheet, for all gate resistance values. As a result, the efficiency impact of varying gate resistance may be underestimated, and the potential for further improvement remains.

To optimize gate driver performance, it may be beneficial to implement three distinct gate resistance values: one for non-critical operating points, one for intermediate voltage and current levels, and one for critical operating conditions, where the primary goal is to limit voltage overshoot and protect the power semiconductor devices. Such an approach can enhance system reliability and efficiency, particularly in applications with dynamic load profiles or stringent transient requirements. The lowest gate resistance should be used when the DC Link voltage is relatively low to minimize switching losses for the majority of the operating points. However, it is not feasible to reduce the gate resistance to zero, as this can introduce high-frequency oscillations caused by parasitic inductances and capacitances in the gate drive loop. These limitations should be explored further in order to determine the optimal values for the DGD.

While efficiency improvements at the inverter level can be significant, their impact on the EDU system level tends to be more limited. The inverter typically operates with high efficiency, and further improvements contribute positively at the component level. However, when viewed in the context of the entire system, which includes multiple subsystems with varying losses, the resulting gain in total efficiency is relatively small. Nonetheless, incremental improvements across all components remain important, as they collectively contribute to enhanced overall system performance. One potential advantage of implementing DGD technology is that it may require minimal hardware modifications to existing inverter designs.

The impact of external gate resistance on the electric machine is complex and not immediately apparent. Its influence on the overall efficiency of the electric machine may be marginal and highly dependent on system conditions. Although this study explores potential effects and considerations related to dynamic gate drive control and its implications for the electric machine's performance and reliability. The available system voltage for the electric machine must typically accommodate voltage overshoots. Theoretically, by reducing transient voltage overshoot during peak battery voltage, the system voltage set point could potentially be increased. According to Ohm's law, an increase in voltage would allow for a proportional decrease in current at the same power level. Since ohmic losses in the motor windings are proportional to the square of the current, a reduction in current may lead to improved motor efficiency. However, in practical system design, it is often not feasible to alter voltage levels dynamically, as this would require de-rating under fully charged conditions.

Alternatively, the effect of dynamic gate drive (DGD) on the winding insulation could be considered. By potentially reducing voltage overshoot, electrical stress on the windings and their insulation may be minimized, thereby lowering the risk of partial discharges. Reduced overshoot could enable the use of less robust insulation systems or thinner insulation layers, which might further decrease ohmic losses in the windings. Nevertheless, thinner insulation may increase the risk of overheating and premature failure, which could have severe consequences. Insulation systems are typically designed with substantial safety margins. Therefore, these margins are intentionally conservative to ensure reliability. Investigating whether gate drive optimization through variable gate resistance can justify reducing insulation thickness would require detailed study, including thorough analysis of insulation standards and long-term reliability implications.

7
Conclusions

7.1 Presented Work

This thesis investigated the potential of a DGD strategy to improve inverter efficiency and reduce voltage overshoot in a SiC-based inverter for battery electric vehicle (BEV) applications. The evaluation was conducted using circuit-level simulations and focused primarily on the impact of varying the external gate resistance during the turn-off transition.

Simulation results demonstrate that switching losses increase with higher gate resistance, while voltage overshoot decreases. The trade-off between these two effects forms the basis for considering a variable gate resistance approach. Under a WLTP drive cycle, the inverter loss reduction reached up to 18.3% when compared to a fixed gate resistance of $10\,\Omega$, particularly at low SOC conditions. At EDU level the reduction in cumulative losses was found to be 2.8%. This indicates that applying a higher gate resistance during critical operating points could reduce voltage stress on the device while maintaining efficient operation in less critical regions with a lower resistance.

Although the inverter-level efficiency improvements are notable, the overall impact on EDU efficiency is limited. This is mainly due to the high baseline efficiency of modern inverters and the relatively small contribution of inverter losses to total drivetrain losses. Nevertheless, the results highlight that incremental improvements at the component level are still meaningful for the complete system.

Due to the reduced voltage overshoot enabled by the higher gate resistance, the DC Bus voltage could be increased by approximately 40 V in the simulations, which represents the effect of using a larger battery while keeping the same inverter components. This increase led to an extension of the base speed from 8750 RPM to 9100 RPM and enabled a higher torque output in the constant power region. As a result, the peak power of the electric machine increased by around 4.84%, suggesting that dynamic gate drive control may offer marginal performance improvements by enabling better utilization of the available DC voltage. Regarding the efficiency of the electric machine, the impact of reduced voltage overshoot is less direct. In theory, lower overshoot may allow a slightly higher system voltage set point, which could reduce the required phase current and subsequently ohmic losses in the windings. However, in practice, the system voltage is typically fixed based on insulation limits

and safety margins, making such adjustments unlikely without broader system-level changes. In addition, the potential to reduce insulation thickness based on improved transient behaviour was considered, but this remains speculative and would require thorough investigation into insulation standards and long-term reliability.

Overall, dynamic gate resistance adjustment offers a promising method for balancing switching performance and system reliability in SiC-based inverters. While its impact on EDU-level efficiency is modest, it can contribute to reduced voltage stress, improved component utilization, and lower energy losses during high-demand operation.

7.2 Future Work

While this study has demonstrated the potential benefits of DGD control in simulation environments, several important aspects remain to be addressed in future work to fully evaluate its practical viability and performance in real-world applications. A key area for further investigation is experimental validation. While simulation results indicate a clear trade-off between switching losses, conduction losses, and voltage overshoots, practical implementation may reveal additional complexities such as parasitic effects, thermal behaviour, and measurement uncertainty.

Additionally, this study focused exclusively on the turn-off transition, holding the turn-on resistance constant. Future research could evaluate the combined impact of adjustable gate resistance during both turn-on and turn-off phases to identify optimal switching strategies. Another promising avenue is to explore the long-term reliability implications of DGD control. This includes analyzing the effects of dynamically varying gate resistance on component aging, thermal cycling, and the insulation system of the electric machine. One speculative benefit identified in this study is the potential to reduce the required insulation thickness due to lower voltage overshoots, which could contribute to improved motor efficiency and material savings. However, any such design changes would require thorough investigation of insulation standards, safety margins, and partial discharge risks, which are critical to ensuring system robustness and compliance with automotive regulations.

Furthermore, future work should aim to determine the optimal number and values of discrete gate resistance levels needed for effective DGD implementation. This would involve system-level analysis to strike a balance between performance gains, circuit complexity, and control effort. In particular, it may be beneficial to evaluate adaptive algorithms capable of selecting gate resistance values based on real-time operating conditions such as current, voltage, or temperature.

Lastly, it is worth exploring the feasibility of software-based DGD implementation, where gate drive strength could be adjusted dynamically using existing voltage and current sensors in conjunction with configurable gate driver ICs. This approach may offer a practical and scalable path toward integration in commercial electric vehicle powertrains, with minimal hardware modifications.

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