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Analysis of Multi-level Inverters for Electric Vehicle Application

Master's thesis in Electric Power Engineering

MANOJ KRISHNA SESHADRI, VISHAL KANIPAKAM

DEPARTMENT OF ENERGY AND ENVIRONMENT

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Manoj Krishna Seshadri, Vishal Kanipakam

Supervisor: Kooros Moabber
Examiner: Torbjön Thiringer

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Department of Energy and Environment
Division of Electrical Engineering
Electric Power Engineering MPEPO
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

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Manoj Krishna Seshadri, Vishal Kanipakam
Department of Energy and Environment
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Abstract

Traditional two-level inverters are used for electric vehicles on the market today. But, in recent years there is a growing interest in multi-level inverters to be used as the propulsion inverter in electric vehicles. So, this thesis work analyzes the performance of a multi-level inverter of different topologies as a traction inverter and a comparison is made with a traditional two-level inverter. Using a multi-level inverter, multiple levels of the output voltage can be obtained which helps in the reduction of losses and also THD. The implementation and analysis of this work are mostly carried out in PLECS software where different topologies of the multi-level inverter are modeled, simulated and the comparison between the different topologies is made in various aspects such as losses, THD, and also the DC link ripple from the capacitors. The thermal analysis is also done as the inverter models are designed considering the thermal properties of the power module. Finally, a comparison of the different topologies is made using two different switches. One uses the SiC switch and the other uses the GaN switch.

In this thesis, a two-level inverter and a multi-level inverter of three levels are investigated. In a multi-level inverter, four different topologies (i.e., Neutral point clamped inverter, T-type neutral point clamped inverter, Flying capacitor inverter, and Cascaded H-bridge inverter) are modeled, simulated, and analyzed. Two different switching strategies (i.e., Sine wave PWM and Space vector PWM) are implemented for the inverter models. But for the multi-level inverter models, phase-shifted sine wave PWM is used. As the number of levels increases, the complexity of the modulation technique, cost, and size of the inverter increases. So, when it comes to selecting an inverter, it is a trade-off between all the above parameters.

Keywords: Electric vehicles, Traction inverter, PLECS, Thermal model, DC link voltage, Electrical losses.

Acknowledgements

We would like to express our gratitude to our supervisors Kooros Moabber and Lars Johansson, for their support and motivation throughout this thesis work. Additionally, we would like to thank our examiner Prof. Torbjörn Thiringer for his for excellent supervision and guidance that kept us on track throughout this thesis work.

Manoj Krishna Seshadri, Vishal Kanipakam, Gothenburg, October 2022

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

CHMI	Cascaded H-bridge MLI
EMI	Electro-Magnetic Interference
EV	Electric Vehicle
FCMI	Flying Capacitor MLI
GaN	Gallium Nitride
IEEE	Institute of Electrical and Electronics Engineer
LSPWM	Level Shifted PWM
MLI	Multi-level inverter
MOSFET	Metal oxide semiconductor field effect transistor
NCMI	Neutral Point Clamped MLI
PSPWM	Phase Shifted PWM
PWM	Pulse width modulation
SiC	Silicon Carbide
SVPWM	Space Vector PWM
SWPWM	Sine Wave PWM
TNCMI	T-type Neutral Point Clamped MLI

Contents

1
Introduction

Internal combustion engines ruled the personal transportation sector for almost a century and for the past few years there is a rapid growth and also demand for the Electric Vehicles (EV) in the transportation sector and vehicle market all over the world [1]. There could be a significant change in the society with the broad-scale growth of electric vehicles in the field of not only technology that is used in personal transportation but also the economy will be moved away from petroleum and this helps in reducing the environmental footprint of transportation.

1.1 Background

In recent times, the multilevel inverters are gaining more attention in the industry as one of the preferred devices for power electronic conversion in high power applications [2]. Currently, the two level inverters are far most used power electronic converter for the electric vehicle applications [3]. But with the continuous increase in the voltage and power levels, there are studies and research on Multi-Level Inverters (MLI) which proves to be a cost effective solution with increase in power quality within the acceptable standards [4]. By addition of few extra components, the voltage level of the output can be increased in steps which is why it is called a MLI. The basic topologies that are mostly discussed about are: Neutral Point Clamped MLI (NCMI), T-type Neutral Point Clamped MLI (TNCMI), Flying Capacitor MLI (FCMI), and Cascaded H-bridge MLI (CHMI).

The recent studies and research shows that all the MLI's have a significant reduction in the total harmonic distortion and also the switching losses but with the increase in the number of components leads to higher costs and power loss. In case of FCMI, larger capacitors are used as the number of levels increase which also increases the complexity of control [5].In case of CHMI, there is a need for isolated dc sources for individual phase leg which makes its application limited in the electric vehicle industry. Hence this thesis work will study different MLI topologies and compare them with Two-Level Inverter (TLI) and also each other on various parameters such as losses, THD, temperature in the semiconductor devices, etc.

1.2 Aim

Modelling and simulation of different topologies for MLI and TLI with suitable modulation technique. The comparison of all the topologies will be done and to see

which inverter performs well for an EV application.

1.3 Scope

The thesis will focus on the comparison between the TLI and MLI topologies that will be simulated using software and not look into to hardware implementation. The topologies will be modelled in terms of selected parameters and the Sine wave PWM and Space Vector PWM (SVPWM) modulation techniques will only be implemented. With this in consideration, only three level MLIs have been considered for this thesis. The losses for the inverters have been considered from the switches, DC link capacitors, DC cable and AC cable have only. Only these parameters will be implemented along with the final circuit diagram of each topology. Due to more number of simulations that needs to be performed the results have been obtained with a open loop model of the inverter for all topologies to avoid longer simulation times.

2

Theoretical Background

This chapter discusses about the theory of TLI and MLI. The different topologies of MLI that will be analysed in this thesis will be discussed based on their circuit design and number of components used. Afterwards, different types of modulation techniques that will be applied for these topologies will be seen. Then the power electronic device used for switching in the MLIs will be seen and the losses created by them and also due to other elements in the inverter. Finally the thermal aspect that will be implemented while modelling the inverter will also be discussed.

2.1 Two level inverter

A three phase, TLI is the most common and simplest inverter topology that is used in electric vehicle applications. This device uses a DC voltage source as its input and converts it to AC voltage which is supplied to the load, an electric machine. This topology consists of six semi-conductor switches and each switch has an anti-parallel diode for the current to flow in the reverse direction. Two levels of output voltage, $+V_{dc}$ and $-V_{dc}$ can be obtained from this inverter in its phase to ground voltage. The circuit diagram of a three phase two level inverter can be seen in Figure 2.1.

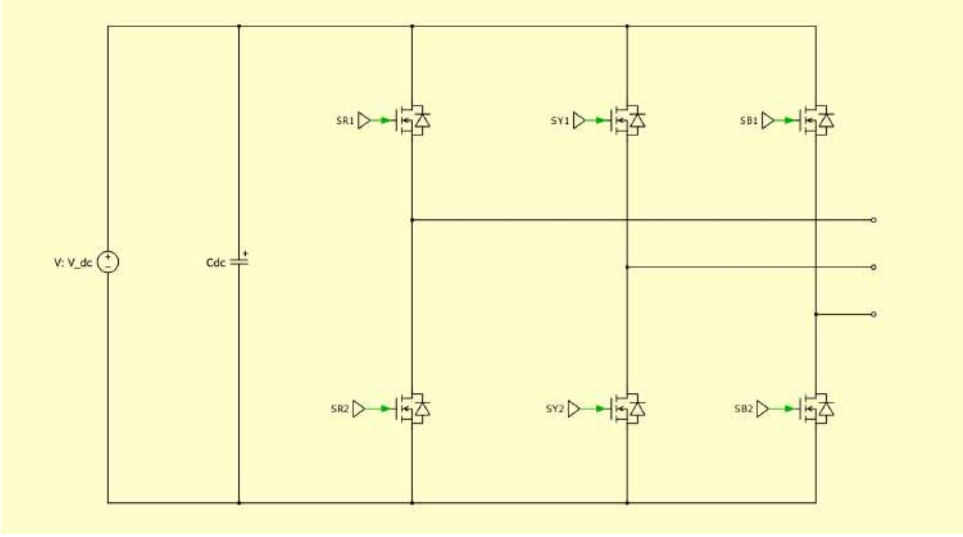


Figure 2.1: Circuit diagram of two level inverter

2.2 Multi-level inverter

The concept of MLI has been around since 1975 [6]. It is a power electronic device which provides a solution to achieve higher power by making use of more switching devices to produce an output phase to ground voltage with more than two levels. A n level MLI will be able to produce n number of voltage levels in its phase to ground output voltage waveform. It has several advantages when compared to the TLI. As the number of levels are increased, a more sinusoidal voltage waveform can be realised at a lower switching frequency when compared to the TLI. This helps in reducing the THD. As the number of levels increases, the voltage across each switch also goes down. This reduces the switching losses and Electro-Magnetic Interference (EMI) in the MLI [3]. Hence it is able to deliver an improved power quality and higher voltage capability.

2.2.1 Neutral Point Clamped Multi-level Inverter

The Neutral point Clamped Multi-level Inverter (NCMI), also called as diode clamped multi-level inverter, uses clamping diodes which enable to achieve the additional voltage levels at the output in its phase to ground voltage. The circuit diagram of a three phase three level NCMI can be seen in Figure 2.2.

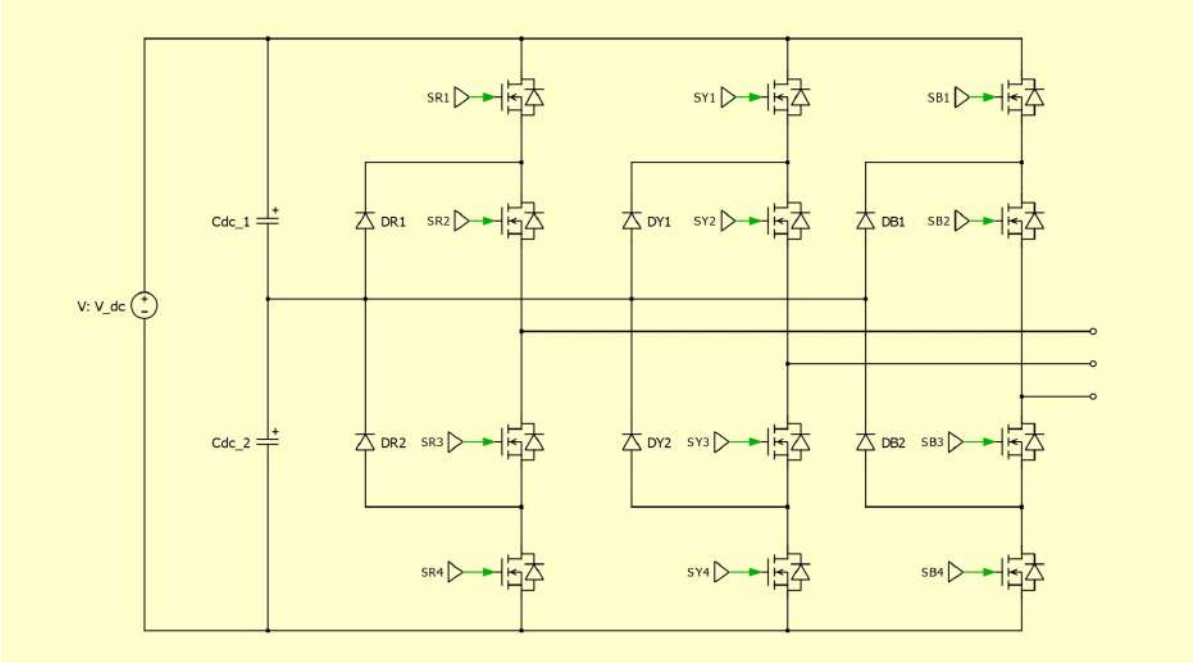


Figure 2.2: Circuit diagram of three level, three phase NCMI

For an n level NCMI, $(n-1)(n-2)$ clamping diodes are used across each phase leg. It consists of $(n-1)$ capacitors on the DC bus, also called as DC link capacitors. As the DC link capacitors are charged to their respective voltage levels, they provide the additional voltage levels by performing the correct switching strategy.

For a three level NCMI, the additional zero level is achieved by making use of clamping diodes. The circuit diagram for the NCMI for a single phase leg has been shown in Figure 2.3.

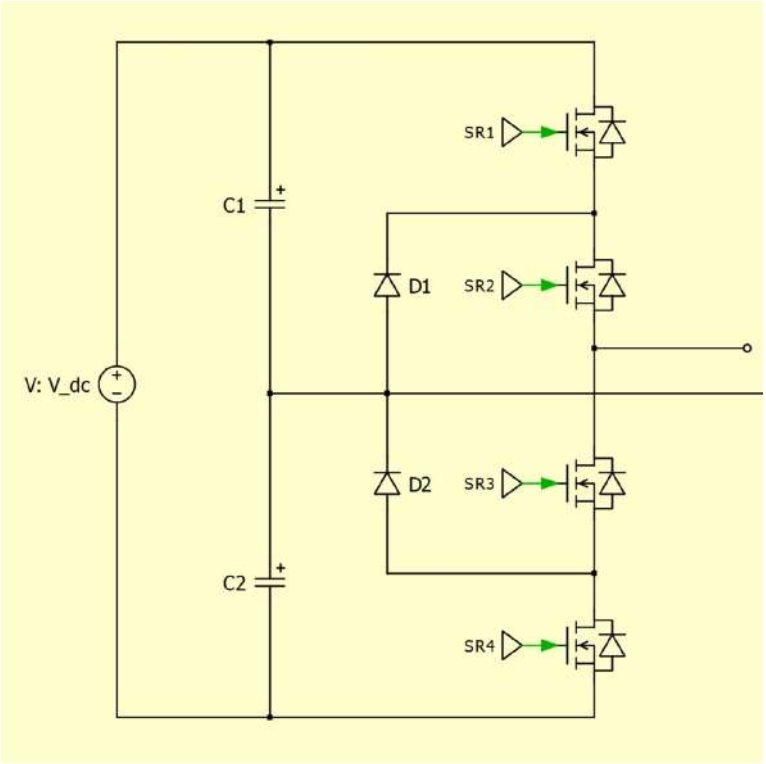
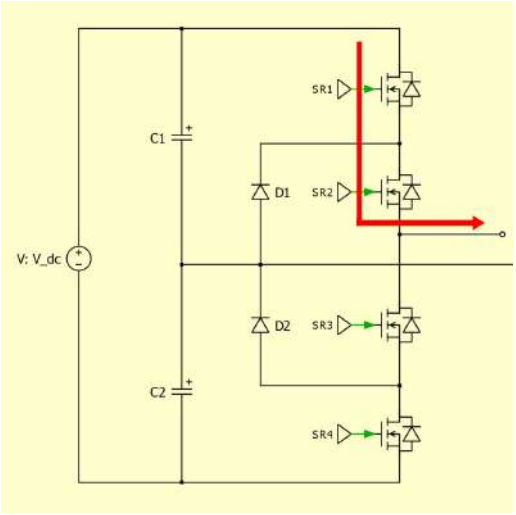
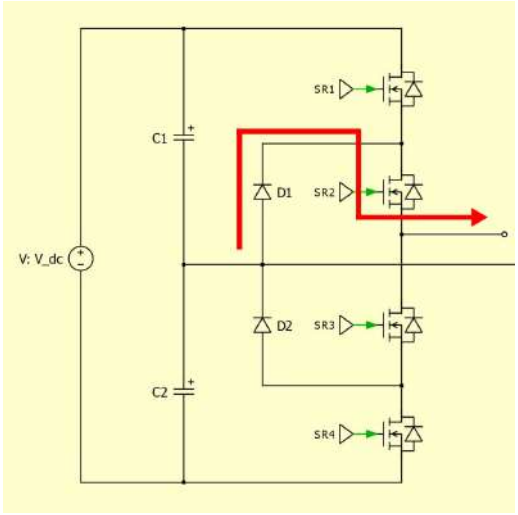


Figure 2.3: Single phase leg of the NCMI

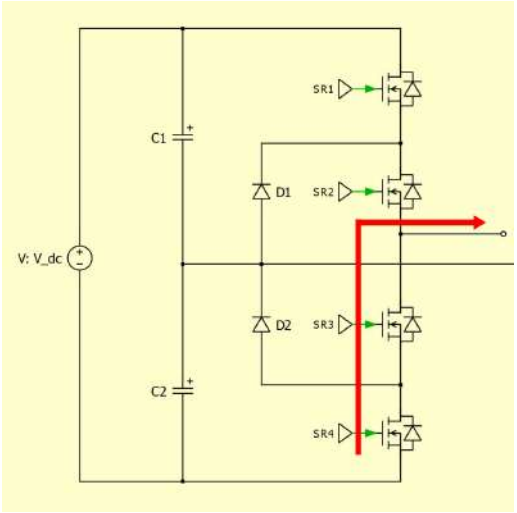
For a positive current output, all the switching states for the NCMI can be seen in Fig 2.4 and in Table 2.1. The DC voltage is split into two by the DC link capacitors, which is $V_{dc}/2$. In case 1, switches SR1 and SR2 are on to produce the positive voltage. Case 2 shows the two zero level switching states. Here either the switch SR2 or SR3 conducts depending on the current direction. For a positive current, the switch SR2 conducts and for a negative current, the switch SR3 conducts. In case 3, switches SR3 and SR4 are on to produce the negative voltage. For all the cases, based on the current direction, either the switch conducts or the anti-parallel diodes conduct. For example, for a positive current in case 1 switches SR1 and SR2 conducts but for negative current the anti-parallel diodes conduct. The voltage across all switches shall now be only $V_{dc}/2$.



(a) Case 1



(b) Case 2



(c) Case 3

Figure 2.4: Switching states for the three phase three level NCMI

Table 2.1: NCMI - Switching states

Switching State	Phase Voltage	**S1**	**S2**	**S3**	**S4**
Case 1	$V_{dc}/2$	On	On	Off	Off
Case 2	0	Off	On	On	Off
Case 3	$-V_{dc}/2$	Off	Off	On	On

2.2.2 T-type Neutral Point Clamped Multi-level Inverter

The T-type Neutral point Clamped Multi-level Inverter (TNCMI) is similar to the traditional NCMI where two switches are used in the place of clamping diodes in each phase leg which helps in reducing the conduction loss [7]. The circuit diagram of a three phase three level TNCMI can be seen in Figure 2.5.

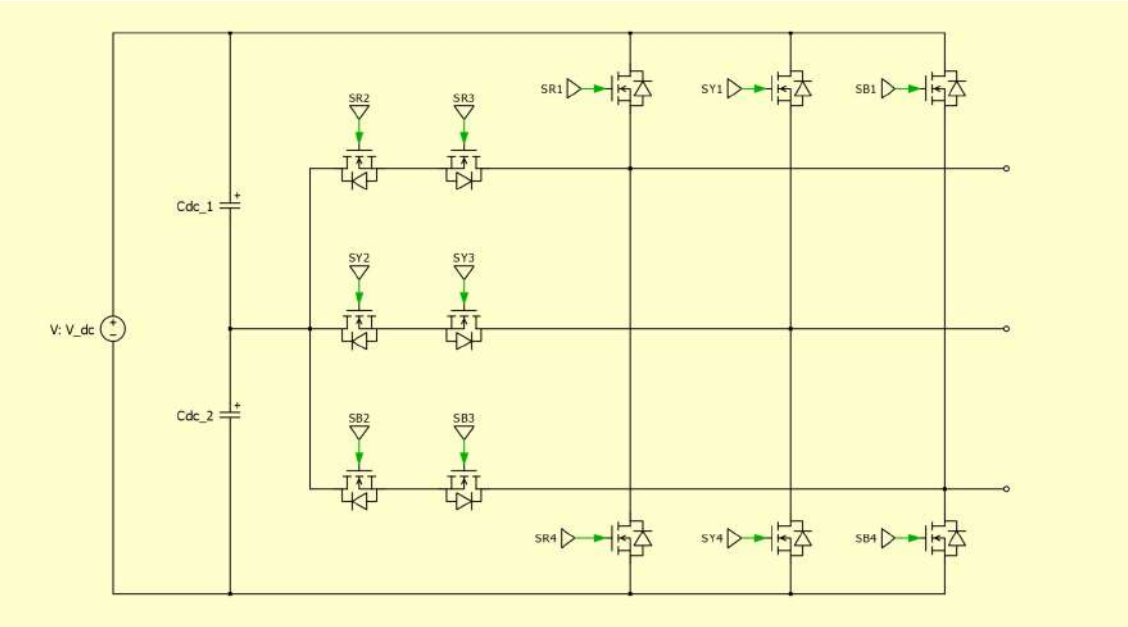


Figure 2.5: Circuit diagram of three level, three phase TNCMI

Similar to NCMI, the TNCMI also has $(n-1)$ DC link capacitors. As the DC link capacitors are charged to their respective voltage levels, they provide the additional voltage levels by performing the correct switching strategy.

For a three level TNCMI, the additional zero level is achieved by the way how the switches are connected in each of its phase leg. The circuit diagram for the TNCMI for a single phase leg has been shown in Figure 2.6.

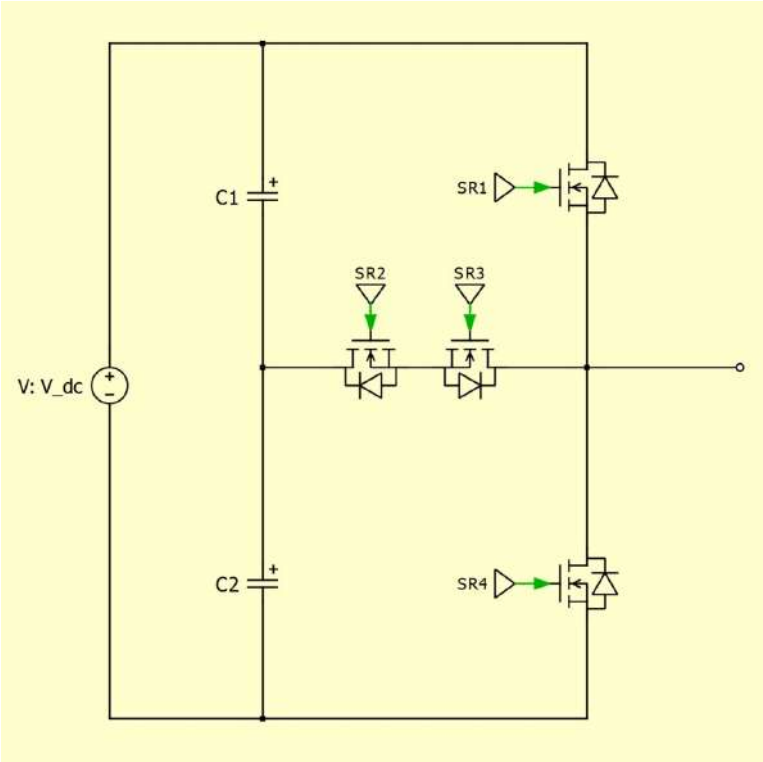
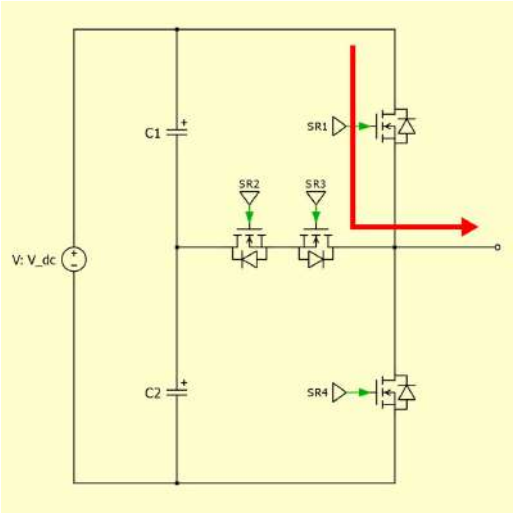
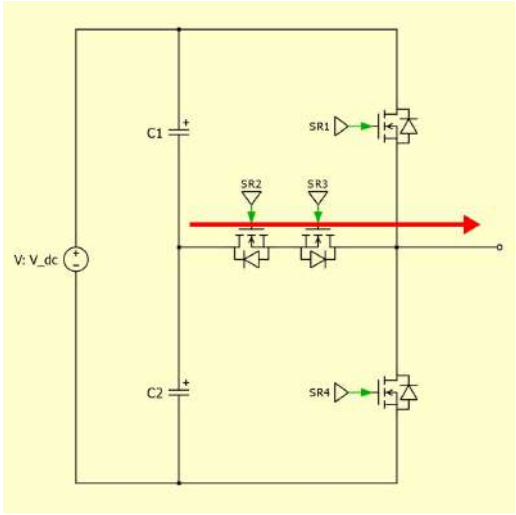


Figure 2.6: Single phase leg of the TNCMI

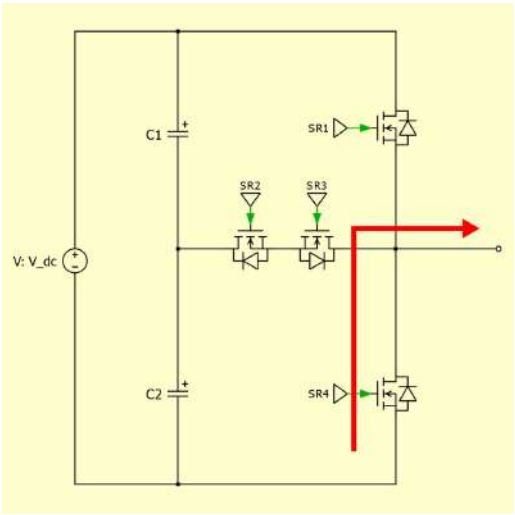
For a positive current output, all the switching states for the TNCMI can be seen in Fig 2.7 and in Table 2.2. The DC voltage is split into two by the DC link capacitors, which is $V_{dc}/2$ similar to the NCMI topology. In case 1, switches SR1 and SR2 (or just SR1) are on to produce the positive voltage. Case 2 shows the two zero level switching states. Here either the switch SR2 or SR3 conducts depending on the current direction. For a positive current, the switch SR2 and the anti-parallel diode of SR3 conducts and for a negative current, the switch SR3 and the anti-parallel diode of SR2 conducts. In case 3, switches SR3 and SR4 (or just SR4) are on to produce the negative voltage. The voltage across switches SR2 and SR3 are $V_{dc}/2$ but the voltage across SR1 and SR2 can go up to V_{dc}.



(a) Case 1



(b) Case 2



(c) Case 3

Figure 2.7: Switching states for the three phase three level TNCMI

Table 2.2: TNCMI - Switching states

Switching State	Phase Voltage	**S1**	**S2**	**S3**	**S4**
Case 1	$V_{dc}/2$	On	On	Off	Off
Case 2	0	Off	On	On	Off
Case 3	$-V_{dc}/2$	Off	Off	On	On

2.2.3 Flying Capacitor Multi-level Inverter

The Flying Capacitor Multi-level Inverter (FCMI) has capacitors attached in parallel to each phase leg. These capacitors are termed as flying capacitors. They enable to achieve the additional voltage levels at the output in its phase to ground voltage. The FCMI has very similar operation in comparison to the NCMI. The circuit diagram of a three phase three level FCMI can be seen in Figure 2.8.

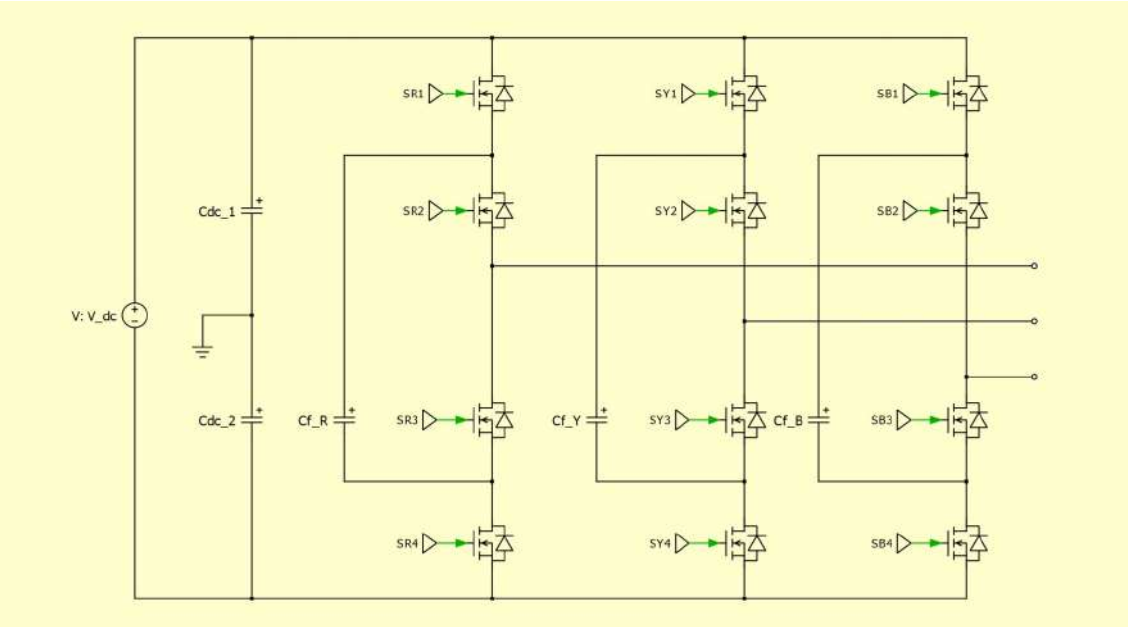


Figure 2.8: Circuit diagram of three level, three phase FCMI

For an n level FCMI, $(n-1)(n-2)/2$ flying capacitors are used across each phase leg and the voltage across each capacitor is $(V_{dc})/(n-1)$ [8] [9]. As the flying capacitors are charged to their respective voltage levels, they provide the additional voltage levels by performing the correct switching strategy. Hence, as the number of levels increases, the number of capacitors will also significantly increase which could make the device bulky. It is important to also consider the size of flying capacitors to have lower voltage ripple for the flying capacitors as well.

For a three level FCMI, the additional zero level is achieved by making use of flying capacitors. The circuit diagram for the FCMI for a single phase leg has been shown in Figure 2.9. This topology has two different switching states to produce the zero-voltage level. Hence it is necessary that both these switching states are equally used to ensure that the corresponding switches are evenly stressed.

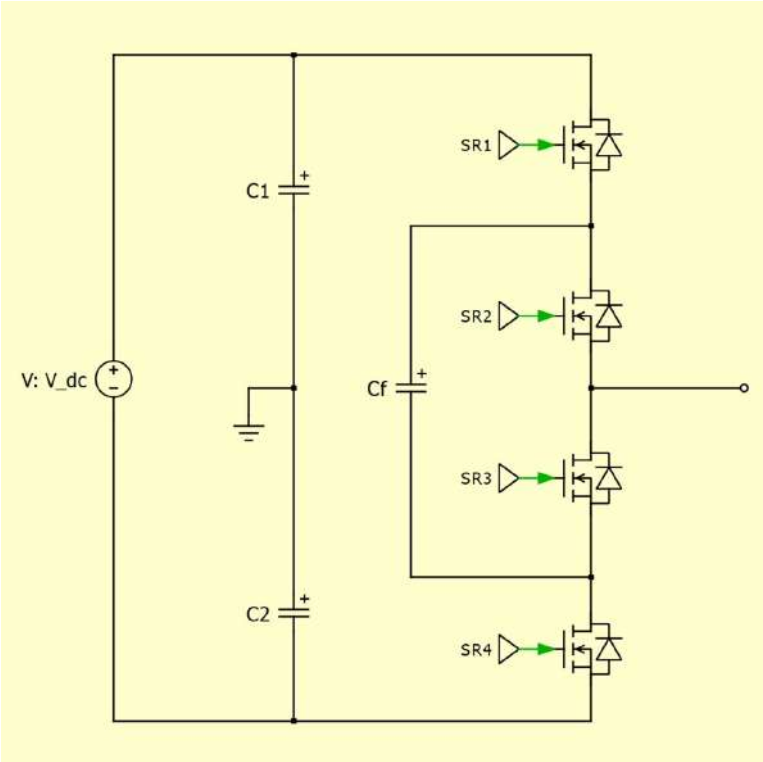
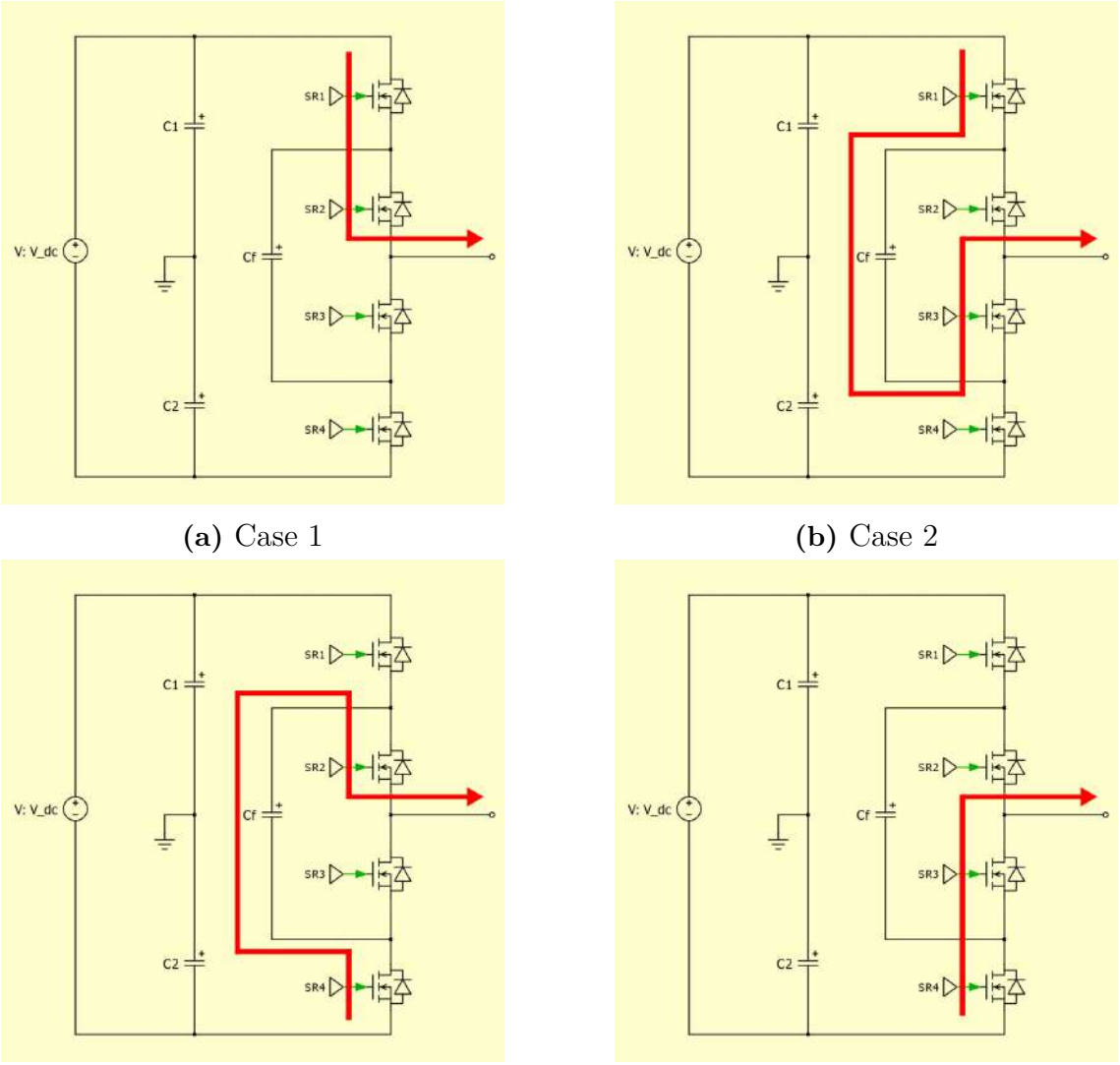


Figure 2.9: Single phase leg of the FCMI

For a positive current output, all the switching states for the FCMI can be seen in Fig 2.10 and in Table 2.3. The similarity regarding to the operation of the NCMI topology can be seen here for for producing the positive and negative voltages. The DC voltage is split into two by the DC link capacitors, which is $V_{dc/2}$. The flying capacitors shall also have a voltage of $V_{dc/2}$. In case 1, switches SR1 and SR2 are on to produce the positive voltage. Cases 2 and 3 show the two zero level switching states. For the FCMI, these two switching states need to happen alternatively. This automatically provides voltage balancing for the flying capacitors present in each phase leg. In case 2, the voltage produced due to C1 is opposed by Cf and the capacitor goes into a charging state. In case 3, the voltage produced due to C2 is opposed by Cf and the capacitor goes into a dis-charging state. In case 4, switches SR3 and SR4 are on to produce the negative voltage. The voltage across all switches shall now be only $V_{dc/2}$.



(a) Case 1 **(b)** Case 2

(c) Case 3 **(d)** Case 4

Figure 2.10: Switching states for three phase three level FCMI

Table 2.3: FCMI - Switching states

Switching State	Phase Voltage	**S1**	**S2**	**S3**	**S4**
Case 1	$V_{dc}/2$	On	On	Off	Off
Case 2	0	On	Off	On	Off
Case 3	0	Off	On	Off	On
Case 4	$-V_{dc}/2$	Off	Off	On	On

2.2.4 Cascaded H-bridge Multi-level Inverter

The Cascaded H-bridge Multi-level Inverter (CHMI) has an H-bridge inverter as a sub-module with individual DC sources for each phase leg. This enables to achieve the three different voltage levels in its phase to ground voltage. The circuit diagram of a three phase three level CHMI can be seen in Figure 2.11.

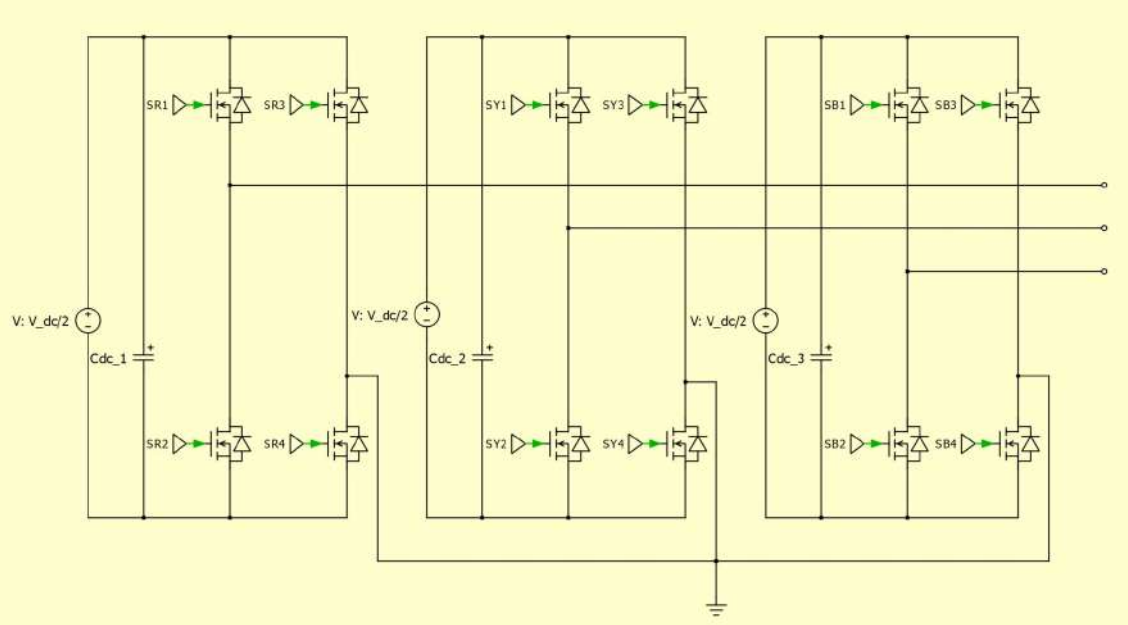


Figure 2.11: Circuit diagram of three level, three phase CHMI

To get an n level CHMI, n sub-modules will need to be used in series for each phase and $2(n-1)$ switches will be required for each phase. The voltage stress across each switch depends on the DC source of the sub-module. It can be extended to higher levels easily due to its modular structure. This topology requires individual DC sources for each sub-module. It does not need additional components such as diodes or capacitors used in the previous topologies.

For a three level CHMI, the additional zero level is achieved by making use of individual DC sources to in each of its phase leg to produce the three different voltage levels. The individual DC sources have an voltage of $V_{DC/2}$ which is half in value when compared with the DC sources in other topologies. The circuit diagram for the CHMI for a single phase leg has been shown in Figure 2.12. Like the FCMI topology, this topology also has two different switching states to produce the zero-voltage level and that both these switching states are equally used.

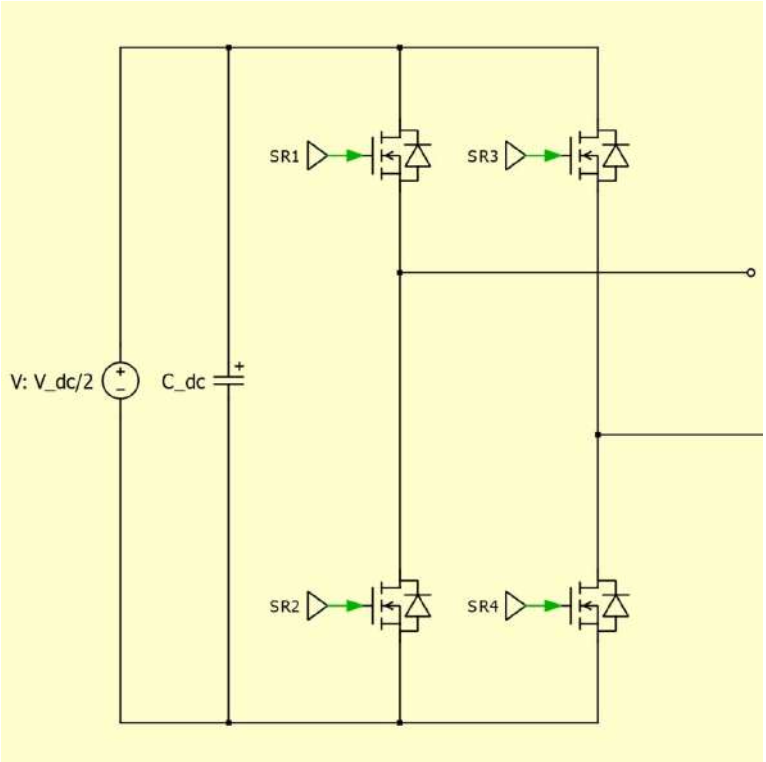
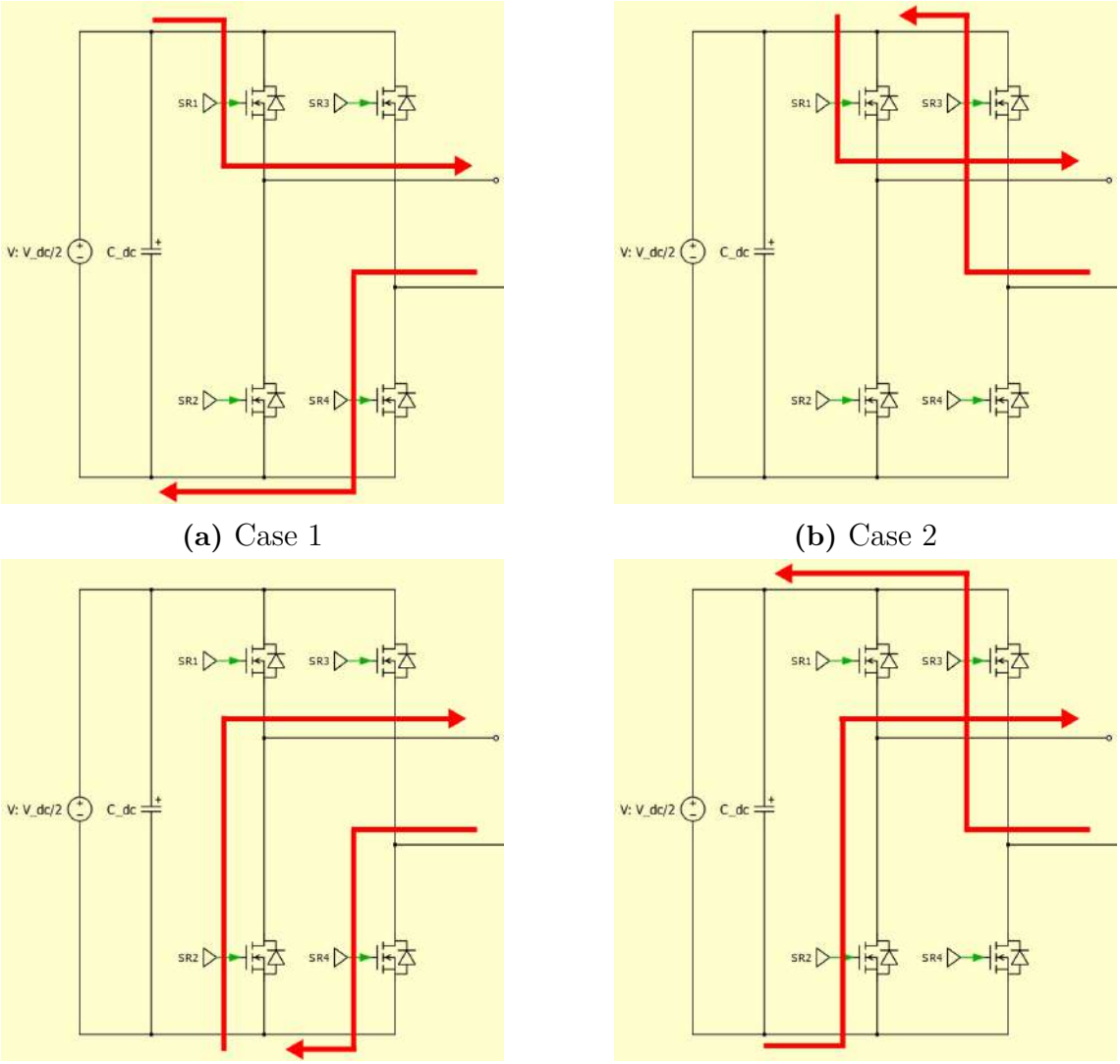


Figure 2.12: Single phase leg of the CHMI

For a positive current output, all the switching states for the CHMI can be seen in Fig 2.13 and in Table 2.4. The DC source present in each phase leg will also have DC link capacitors as well. In case 1, switches SR1 and SR4 are on to produce the positive voltage. The output is in parallel connection to the DC link capacitor. Cases 2 and 3 show the two zero level switching states. For this either the top two switches or the bottom two switches can be closed, which makes the output to be in short circuit condition to produce the zero voltage level. In case 4, switches SR2 and SR3 are on to produce the negative voltage level. The output is connected in parallel but with reversed polarities. The voltage across all switches shall now be only $V_{dc/2}$.



(a) Case 1

(b) Case 2

(c) Case 3

(d) Case 4

Figure 2.13: Switching states for the three phase three level CHMI

Table 2.4: CHMI - Switching states

Switching State	Phase Voltage	**S1**	**S2**	**S3**	**S4**
Case 1	$V_{dc}/2$	On	Off	Off	On
Case 2	0	On	Off	On	Off
Case 3	0	Off	On	Off	On
Case 4	$-V_{dc}/2$	Off	On	On	Off

2.3 Pulse width modulation techniques

Pulse width modulation (PWM) techniques are used to achieve the desired reference voltage waveform with lower total harmonic distortion. The harmonics created also

gets pushed from the fundamental frequency to the carrier frequency and multiples of carrier frequency. The drawback of using PWM is the increase in switching losses.

2.3.1 Sine Wave PWM

Sine Wave PWM (SWPWM) uses the reference and carrier waveforms, which are compared against each other to achieve the desired switching, therefore producing the desired output voltage waveform. As the number of levels increases, there are more number of switches present for each phase leg. Hence more number of carrier wave-forms are required to achieve the desired voltage waveform. For an n level MLI, there will be $(n-1)$ carrier waves required. The references for the three phases are per

$$V_a^*(t) = m_a V_{dc} \sin \omega t \tag{2.1}$$

$$V_b^*(t) = m_a V_{dc} \sin(\omega t - \frac{2\pi}{3}) \tag{2.2}$$

$$V_c^*(t) = m_a V_{dc} \sin(\omega t + \frac{2\pi}{3}) \tag{2.3}$$

where V_a^*, V_b^* and V_c^* are the reference voltages for three phases, V_{dc} is the DC link voltage, m_a is modulation index

There are two major types SWPWM techniques, Phase Shifted PWM and Level shifted PWM.

2.3.1.1 Phase shifted multi-carrier PWM

In Phase shifted multi-carrier PWM (PSPWM), the carrier signals will be phase shifted by $360/(n-1)$ [9]. The same reference signal will be used to compare with all the carrier signals. The amplitude of the carrier and reference signal are the same. Figure 2.14 shows the reference and carrier waveform for a three level MLI.

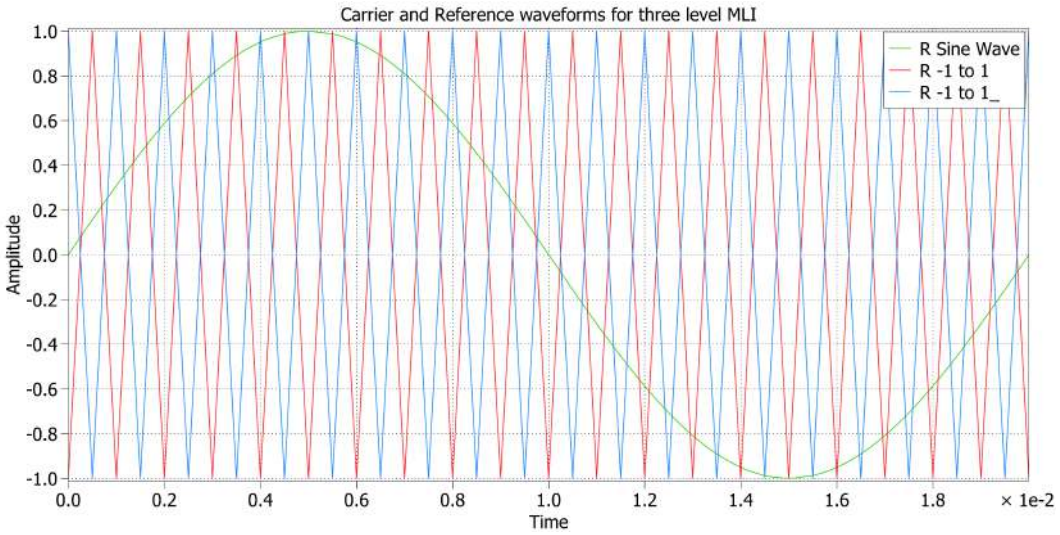


Figure 2.14: Phase shifted multi-carrier PWM for a three level MLI

2.3.1.2 Level shifted multi-carrier PWM

In Level shifted multi-carrier PWM (LSPWM), the carrier signals be level shifted completely. The same reference signal will be used to compare with all the carrier signals[10]. The sum of the amplitude of all the carrier signals is equal to amplitude of the reference signal. Figure 2.15 shows the reference and carrier waveform for a three level MLI.

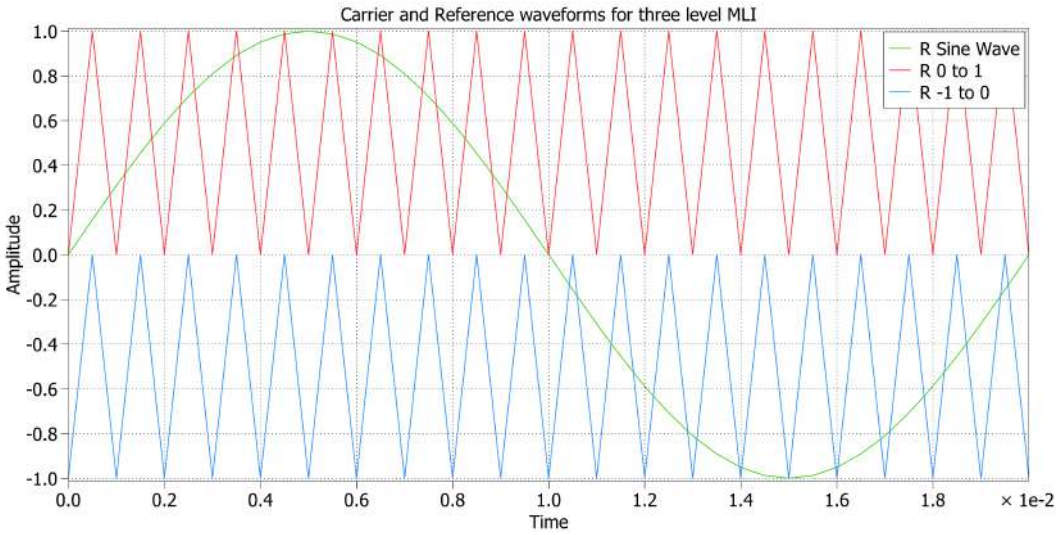


Figure 2.15: Level shifted multi-carrier PWM for a three level MLI

For all the topologies, the PSPWM was chosen. For each phase leg, a single reference waveform was compared with two other carrier waveforms. All the switching sequences for the MLIs for the three levels of output voltages are known. A comparison is made between the reference and carrier waveforms to produce the correct switching output in each phase leg.

2.3.2 Space vector PWM

Space vector PWM (SVPWM) is another modulation technique which uses mathematical transformation and calculation to estimate the on time for respective switches to achieve the desired output voltage waveform [11]. It makes use of the Clarke transformation to transform the three phase system to a two phase system ($\alpha\beta$ - frame). Depending upon the location of $\vec{V_{ref}}$ in the $\alpha\beta$ frame, the duty cycles for the switches are calculated. The reference waveforms in the $\alpha\beta$ frame are as per

$$V_{\alpha}^{*} = \frac{2}{3}(V_{a}^{*} - \frac{1}{2}V_{b}^{*} - \frac{1}{2}V_{c}^{*}) \tag{2.4}$$

$$V_{\beta}^{*} = \frac{2}{3}(\frac{\sqrt{3}}{2}V_{b}^{*} - \frac{\sqrt{3}}{2}V_{c}^{*}) \tag{2.5}$$

$$V_{ref} = V_{\alpha}^{*} + jV_{\beta}^{*} \tag{2.6}$$

where V_{α}^{*} and V_{β}^{*} are the alpha and beta component of the reference voltage in the $\alpha\beta$ frame, V_{ref} is the reference voltage

The switching is made to ensure lower losses and lower THD. SVPWM has higher voltage capability when compared to SWPWM technique by a range of 15.5% [11].

2.3.2.1 Two level SVPWM

The space vector diagram for a two level inverter is as per Figure (2.16). It has two voltage levels in its phase to ground voltage, positive voltage $'P'$ and negative voltage $'N'$. The same can be seen in Figure 2.16 for all corresponding switching states. It has seven voltage vector positions from $\vec{V_0}$ to $\vec{V_6}$. $\vec{V_0}$ is a zero state vector and has two switching states.

The whole area is divided into six sectors where each sector is 60 degrees. The first step is to identify in which sector $\vec{V_{ref}}$ is present. As θ is known by making Clarke transformation, the sector where the $\vec{V_{ref}}$ lies can be found.

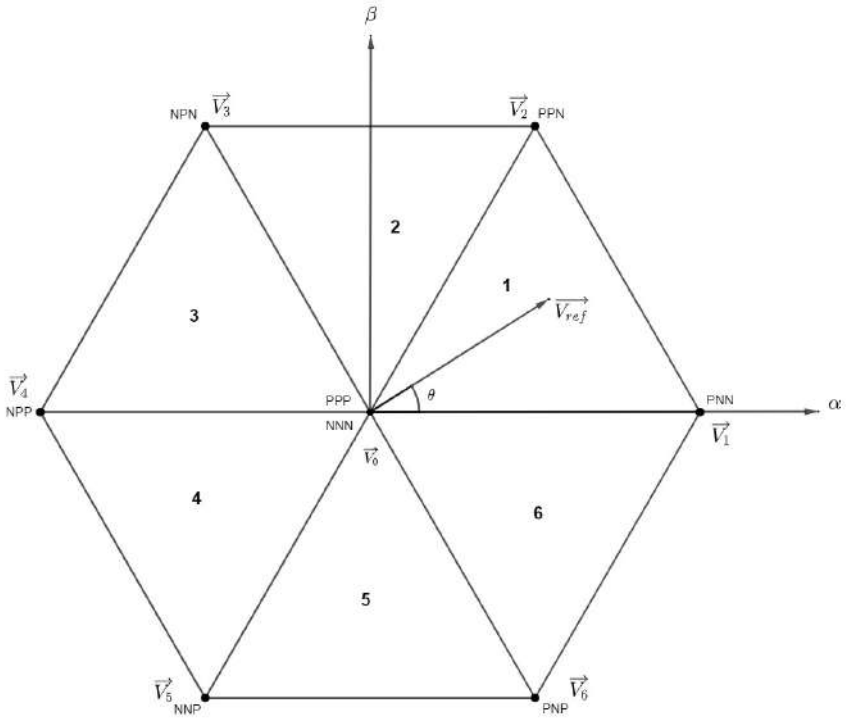


Figure 2.16: Space vector diagram for two level inverter

2.3.2.2 Three level SVPWM

The space vector diagram for a three level inverter is shown in Figure 2.17. It has three voltage levels in its phase to ground voltage, postive voltage $'P'$, negative voltage $'N'$ and zero voltage $'O'$. The same can be seen in Figure 2.17 for all corresponding switching states. It has eighteen voltage vector positions and 27 switching states[11].

- Zero vector ($\vec{V_0}$): The magnitude of the voltage vector $\vec{V_0}$ is zero. It has three switching states, PPP, NNN and OOO.
- Small vectors ($\vec{V_1}$ to $\vec{V_6}$): The magnitude of the voltage vectors $\vec{V_1}$ to $\vec{V_6}$ is $V_{dc}/3$. Each vector has two switching states.
- Medium vector ($\vec{V_7}$ to $\vec{V_{12}}$): The magnitude of the voltage vectors $\vec{V_7}$ to $\vec{V_{12}}$ is $V_{dc}/\sqrt{3}$. Each vector has only one switching state.
- Large vector ($\vec{V_{13}}$ to $\vec{V_{18}}$): The magnitude of the voltage vectors $\vec{V_{13}}$ to $\vec{V_{18}}$ is $2V_{dc}/3$. Each vector has only one switching state.

The whole area is divided into six sectors in the same way as for a two level inverter. Each sector is further divided into four regions. For the three level inverter, first the sector is identified in the same manner as for the two level inverter. As the modulation index for $\vec{V_{ref}}$ is also known, the corresponding region can also be found.

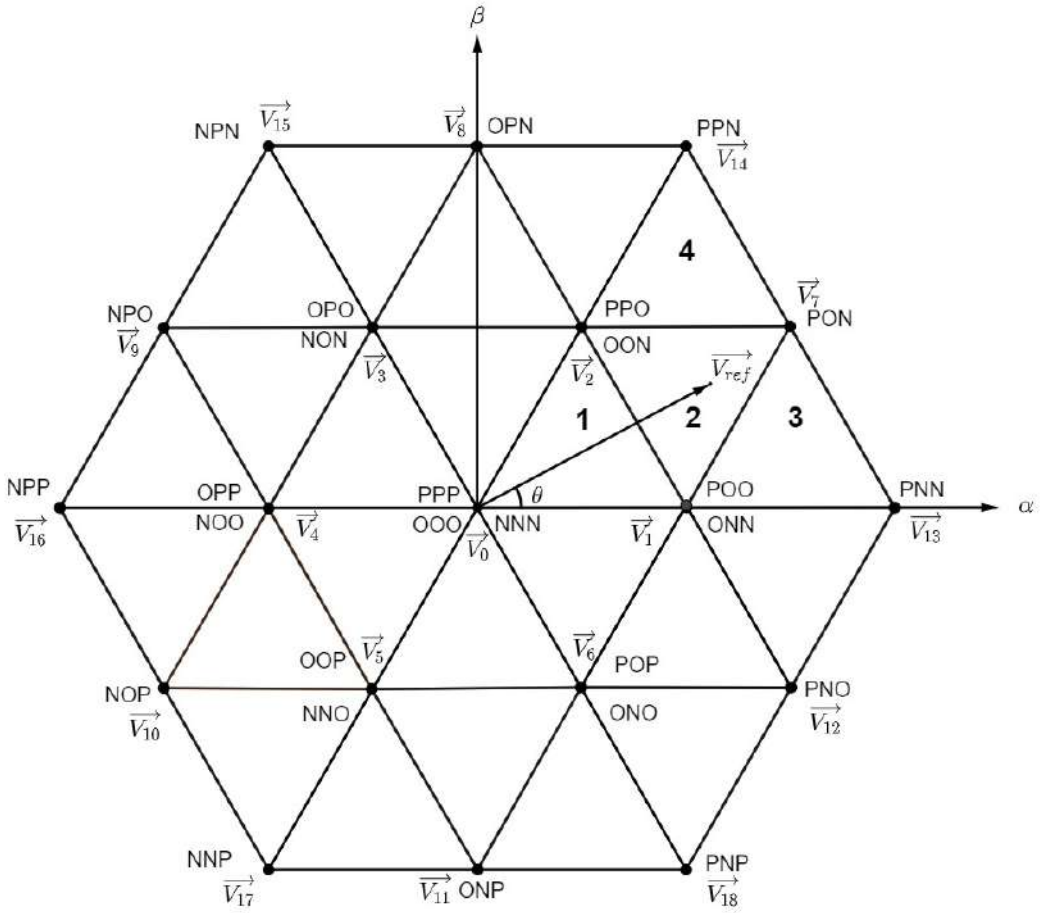


Figure 2.17: Space vector diagram for three level inverter

2.3.2.3 Dwell time

After $\vec{V_{ref}}$ is located, the closest three vector positions are known, for any n level MLI, it makes use of an algorithm based on Volt-second balancing principle to determine the dwell time for the respective switches. This principle implies the product of the reference voltage vector $\vec{V_{ref}}$ and the sampling period T_s is equal to the sum of the nearest three voltage vectors multiplied by the time interval of the corresponding vectors[11].

Figure 2.17 shows that $\vec{V_{ref}}$ is in region 2 of sector 1. The nearest three voltage vectors are $\vec{V_1}$, $\vec{V_2}$ and $\vec{V_7}$. Using the volt-second balancing principle the dwell times are calculated using

$$\vec{V_{ref}} T_s = \vec{V_1} T_a + \vec{V_7} T_b + \vec{V_2} T_c \tag{2.7}$$

$$T_s = T_a + T_b + T_c \tag{2.8}$$

where T_s is the sampling time for one period, T_a, T_b and T_c are the dwell times at voltage vectors $\vec{V_1}$, $\vec{V_7}$ and $\vec{V_2}$.

Once the dwell times for all the voltage vectors are calculated, based on the region the reference voltage vector is located, the switching sequence needs to be generated. The dwell times for the voltage vectors in each region for sector 1 is shown in table 2.5. Schematic representation of sector 1 is shown in figure 2.18 and the voltage vectors corresponding to each region is also presented.

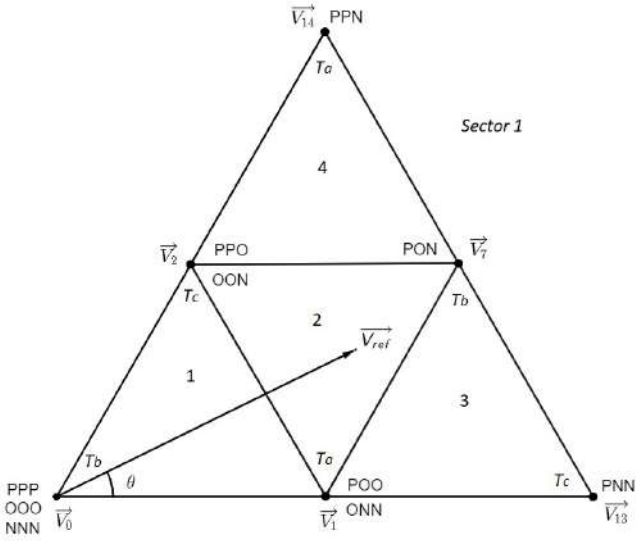


Figure 2.18: Sector 1 of the 3 level space vector diagram

Table 2.5: Timing expressions for three level SVPWM

Region	Vector	T_a	Vector	T_b	Vector	T_c
1	V_1	$T_s[2m_a \sin(\frac{\pi}{3} - \theta)]$	V_0	$T_s[1\text{-}2m_a \sin(\frac{\pi}{3} + \theta)]$	V_2	$T_s[2m_a \sin(\theta)]$
2	V_1	$T_s[1\text{-}2m_a \sin(\theta)]$	V_7	$T_s[2m_a \sin(\theta)\text{-}1]$	V_2	$T_s[1\text{-}2m_a \sin(\frac{\pi}{3} - \theta)]$
3	V_1	$T_s[2\text{-}2m_a \sin(\frac{\pi}{3} + \theta)]$	V_7	$T_s[2m_a \sin(\theta)]$	V_{13}	$T_s[2m_a \sin(\frac{\pi}{3} - \theta) - 1]$
4	V_{14}	$T_s[2m_a \sin(\theta) - 1]$	V_7	$T_s[2m_a \sin(\frac{\pi}{3} - \theta)]$	V_2	$T_s[2\text{-}2m_a \sin(\frac{\pi}{3} + \theta)]$

Now based on the region and the switching states, the switching sequence is generated and this can be done in several ways since there are multiple redundant states for each inverter topology. The switching sequence is determined in such a way that the switching loss and the THD are minimized. The requirements to achieve this strategy is to have

- only two switches in the same inverter phase leg involve in the transition from one switching state to the next state i.e; one being switched on and the other being switched off.
- minimum number of switching (zero if possible) when the reference voltage vector moves from one sector (or region) to the next.
- minimal neutral point voltage deviation depending on the inverter topology.

Taking these considerations into account, the switching sequence is determined for all the regions. Figure 2.19 represents the switching sequence for region 2 of sector 1 along with the calculated dwell times. This sequence fulfills the requirements mentioned above for lower switching losses and THD.

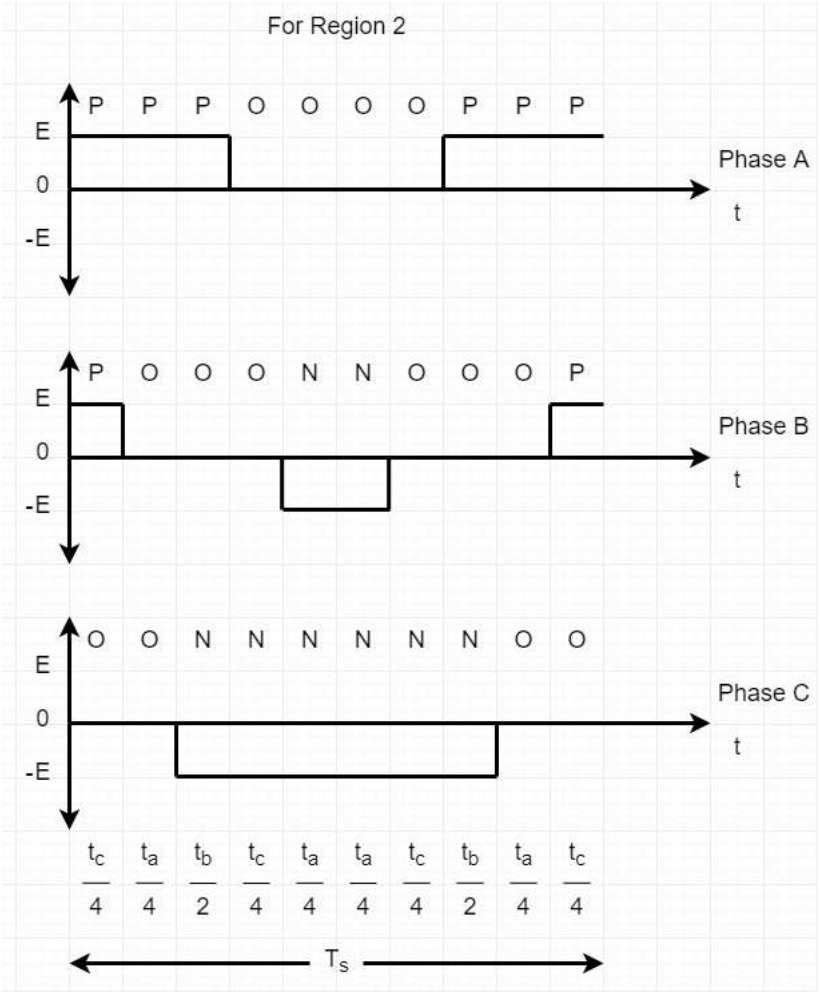


Figure 2.19: Switching sequence for 3 level MLI when V_{ref} is region 2

2.4 Switching device

There are many types of switching devices used in an inverter such as the Metal oxide semiconductor field effect transistor (MOSFET), Insulated gate bipolar transistor, Bipolar junction transistor. The inverters to be designed are for lower application. With the availability of wide band gap power electronic devices, the MOSFET is chosen as the switching device for this thesis.

2.4.1 Metal Oxide Semiconductor Field Effect Transistors

MOSFET is a voltage-controlled device which has three terminals with gate, drain, and source. It is a type of semiconductor device with the capability to have high

frequency switching and is used in low and medium voltage applications. MOSFET is turned on by providing a positive voltage at the gate terminal and turned off when zero voltage is provided to the gate terminal. The silicon (Si) MOSFET is one of the most common MOSFETs being used. It has a band gap energy of of 1.1eV.

2.4.1.1 Silicon Carbide MOSFET

A Silicon Carbide (SiC) MOSFET is a wide band gap semiconductor device. It has a band gap energy of of 3.3eV. The operating voltage for SiC MOSFETs is from 650V and above. When compared to the Si MOSFET, SiC MOSFET it has a

- higher switching speed which allows it to have lower switching losses.
- much less body diode recovery.
- higher stability for the $R_{DS,on}$ over temperature variation [12].
- higher gate voltage swing but lower gate charge stored.
- higher break down voltage margin.

2.4.1.2 Gallium Nitride MOSFET

A Gallium Nitride (GaN) MOSFET is a wide band gap semiconductor device. It has a band gap energy of of 3.4eV. The operating voltage for SiC MOSFETs is below 650V. When compared to the SiC MOSFET, GaN MOSFET has

- higher electron mobility
- higher switching speed which allows it to have lower switching losses.
- zero reverse recovery as there is no presence of a PN junction in the lateral structure for a GaN MOSFET. Hence there is no body diode and associated reverse recovery losses.
- lower stability for $R_{DS,on}$ over temperature variation. It is important to check the $R_{DS,on}$ values at the operating temperature and then calculate the efficiencies.
- similar gate voltage swing but lower gate charge stored.

2.5 Losses in a three phase inverter

There are different factors that contribute to losses in a three phase inverter. The majority of the losses is due to the power semiconductor device, the MOSFET. There are two types of losses which happen in the MOSFET and can be represented as

$$P_{tot} = P_{sw} + P_{cond} \tag{2.9}$$

where P_{tot} is the total power loss, P_{sw} is the switching loss and P_{cond} is the conduction loss happening in the MOSFET. As there are other components present in the inverter, they will have equivalent resistances and contribute towards losses in the inverter. This is called as ohmic losses and is represented by

$$P_{ohmic} = I_{rms}^2 R \tag{2.10}$$

where P_{ohmic} is the ohmic losses, I_{rms} is the rms value of current flowing through the component during conduction and R is value of resistance of the corresponding components.

2.5.1 Switching losses

Switching loss occurs when the MOSFET is turned on or turned off as this cannot happen instantaneously. There is always a turn on and turn off time for the switches which causes power dissipation. During turn off, the switch has a voltage which is equal to the source voltage and during turn on, the voltage becomes zero and at the same time the current also start flowing through the switch. Since there is both voltage and current at this time, there will also be power loss which is called as switching loss which can be estimated with

$$P_{sw} = f_{sw} E_{sw} \left(\frac{1}{\pi} \frac{\hat{I_{out}}}{I_{ref}} \right)^{K_i} \left(\frac{V_{DS}}{V_{ref}} \right)^{K_v} \tag{2.11}$$

where P_{sw} is the total switching loss, f_{sw} is the carrier frequency used for pulse width modulation, E_{sw} represents either the turn on and turn off losses for one time period in a MOSFET or the reverse recovery losses in a diode, $\hat{I_{out}}$ is the peak value of current flowing through the switch, I_{ref} and V_{ref} are the values taken from the test condition of corresponding E_{sw}, V_{DS} is the voltage applied across the switch, K_i and K_V are constants for current and voltage depending on the E_{sw}. The switching losses are also dependent on MOSFET's junction temperature.

2.5.2 Conduction losses

Conduction losses happen due to the presence of internal resistances and forward voltage drops present in a power semiconductor device. The conduction losses for any device can be represented using

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_{cond}(V_{pn} + R_{cond} i_{cond})\, dt \tag{2.12}$$

$$P_{cond} = \frac{V_{pn}}{T_{sw}} \int_0^{T_{sw}} i_{cond}\, dt + \frac{R_{cond}}{T_{sw}} \int_0^{T_{sw}} i_{cond}^2\, dt \tag{2.13}$$

$$P_{cond} = V_{pn} I_{cond(AVG)} + R_{cond} I_{cond(RMS)}^2 \tag{2.14}$$

where P_{cond} is the conduction loss, T_{sw} is the time period for one switching cycle, i_{cond} is the instantaneous current flowing through the device, V_{pn} is the forward voltage drop in the device, R_{cond} is the resistance of the device during conduction, $I_{cond(AVG)}$ is average conduction current flowing through the device, $I_{cond(RMS)}$ is the rms value of current flowing the device.

The MOSFET being a unipolar device, there is no constant voltage drop ($V_{pn} = 0$). Hence the conduction losses for a MOSFET can be written as

$$P_{MOSFET} = R_{DS,on} I_{FET(RMS)}^2 \tag{2.15}$$

where P_{MOSFET} is the conduction losses in a MOSFET, $R_{DS,on}$ is the resistance of MOSFET, $I_{FET(RMS)}$ is the rms value of current flowing through the MOSFET.

As the diode has both the internal resistance and forward voltage drop, the conduction losses for the diode shall be as per (2.14).

2.6 Thermal Implementation

The advancement in the field of power electronics is leading to a significant reduction in the size of the devices which in turn is causing a higher heat flux in the semiconductors [13]. The provided junction temperature of the semiconductor device should be kept in mind for the reliable performance of the inverter. The temperature rise in these components is proportional to the thermal loss where joule heating is a major reason for the thermal loss. Hence, the electrical and thermal implementation of the model is important for a proper functioning of the device.

To estimate the junction temperature of these components, the simulation softwares like PLECS use the RC-type network. Commonly in semiconductor devices the heat propagation is done by conduction and from [14] a simplified heat conduction equation can be proposed in an equivalent electrical equation. The equivalent variables in thermal and electrical equations are shown in table 2.6 and the thermal circuit equivalent to the electrical circuit consisting of only RC components is shown in figure 2.20.

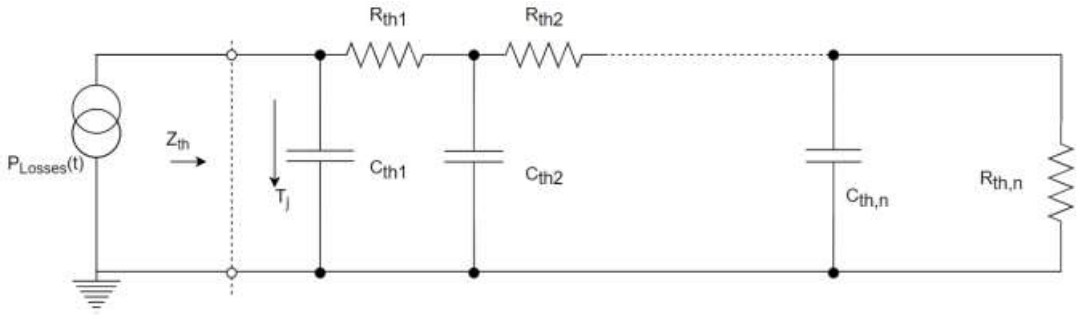


Figure 2.20: Thermal circuit equivalent to the electrical circuit

Table 2.6: The equivalent variables in thermal and electrical equations

Thermal		Electrical	
Temperature	T in K	Voltage	U in V
Heat flow	P in W	Current	I in A
Thermal resistance	R_{th} in K/W	Resistance	R in V/A
Thermal capacitance	C_{th} in Ws/K	Capacitance	C in As/V

where K is Kelvin, V is Volt, A is Ampere, W is Watt, and s is seconds.

3

Modelling and Simulation

This section discusses the modelling of the MLIs that have been implemented. All the topologies that have been implemented are for a three level MLI. For the phase to ground voltage potential, the two level inverter has a positive and negative voltage as output. The three level inverter has an additional zero level voltage. This section also discusses how the models have been implemented by making use of the PLECS software.

3.1 Inverter modelling in PLECS

PLECS is the software chosen to analyse efficiency and THD present in all the topologies. The loss model for switches can be obtained from the PLECS models available from the MOSFET manufacturers. Software also helps to analyse the THD easily. The thermal model of the system can also built and the thermal aspects of the switch can be analysed as well.

3.1.1 Additional components

The ideal circuit diagram of all the topologies have been seen. In reality, there are additional components present in the circuit that needs to be modelled for a more realistic simulation. The values for these models was already available.

3.1.1.1 Battery model

A battery is a non-linear system whose impedance keeps changing based on the frequency. In this case, the battery has been modelled with two resistors and a capacitor as shown in Fig 3.1. The values for the components are shown in Table 3.1

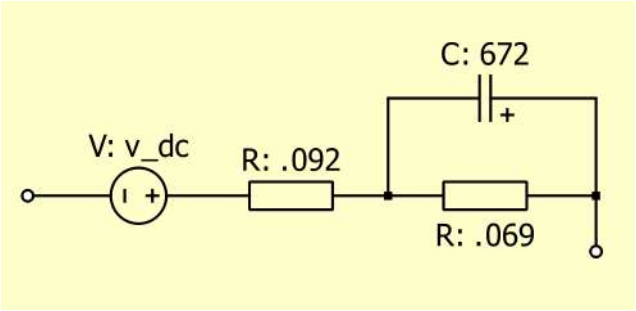


Figure 3.1: Battery model representation

Table 3.1: Battery model

Parameters	Values	Units
R0	0.092	Ω
R1	0.069	Ω
C1	672	F

3.1.1.2 DC cable model

The cables used to connect the battery and inverter will also need to be modelled. This is represented as a resistor in series with inductor. The values for these are 0.7 Ω and 10 μH and is shown in Fig 3.2

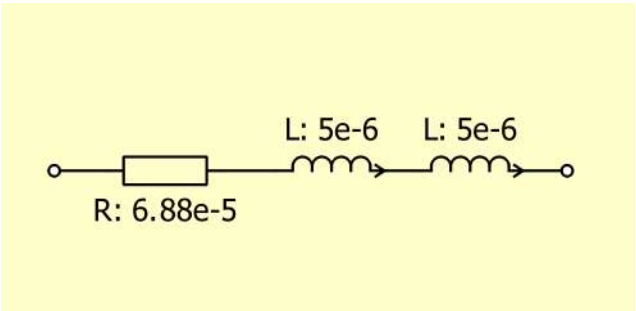


Figure 3.2: DC cable model representation

3.1.1.3 AC bus bar model

The AC bus bars will be used to connect the output of the inverter and the electric machine load. The resistive part of this on the output of the inverter side and input of the load side are 0.7 Ω and 0.3 Ω and is shown in Fig 3.3

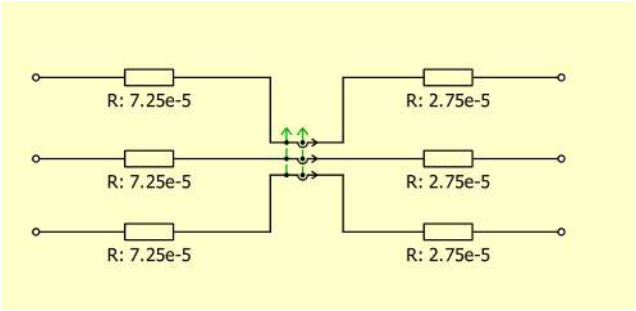


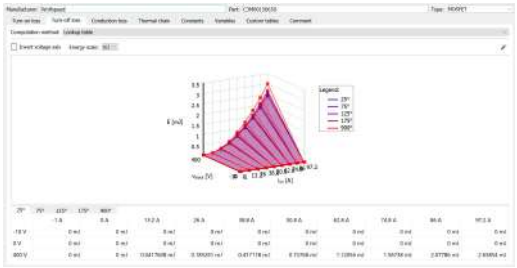
Figure 3.3: AC bus bar model representation

For all these components, the resistive elements have been considered to compute the total losses of the inverter.

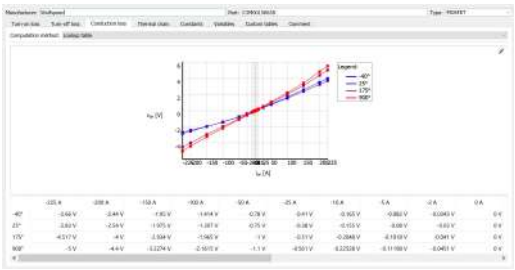
3.1.2 Switch model

As PLECS is the software used, there are switch models available to be used from various MOSFET manufacturers. The switch model has various representations. The model consists look up tables and formulas to calculate the losses in each switch. Each manufacturer makes use of separate formulas. For this thesis, the data provided in the table alone is considered for calculating the losses to have similar accuracy in all simulations. There are separate tables to compute the switching losses and conduction losses and the values has been calculated at various operating temperatures and can be seen in Fig 3.4. The software uses interpolation to calculate the loss values.

(a) Turn on losses



(b) Turn off losses



(c) Conduction losses

Figure 3.4: Look up tables for losses in a MOSFET in PLECS

3.1.3 Thermal model

The thermal model of the inverter has been modelled using three individual heat sinks. These heat sinks would simulate the coolant temperature flowing through them. The worst case temperature has been considered for this and they are 65 °C, 65+3 °C and 65+8 °C for phase A, phase B and phase C respectively. The variation in temperature in each phase leg is due to the gradual rise in coolant temperature as it moves from phase A to phase C and can be seen in Fig 3.5. The MOSFETs are also initialized with these initial temperatures during startup.

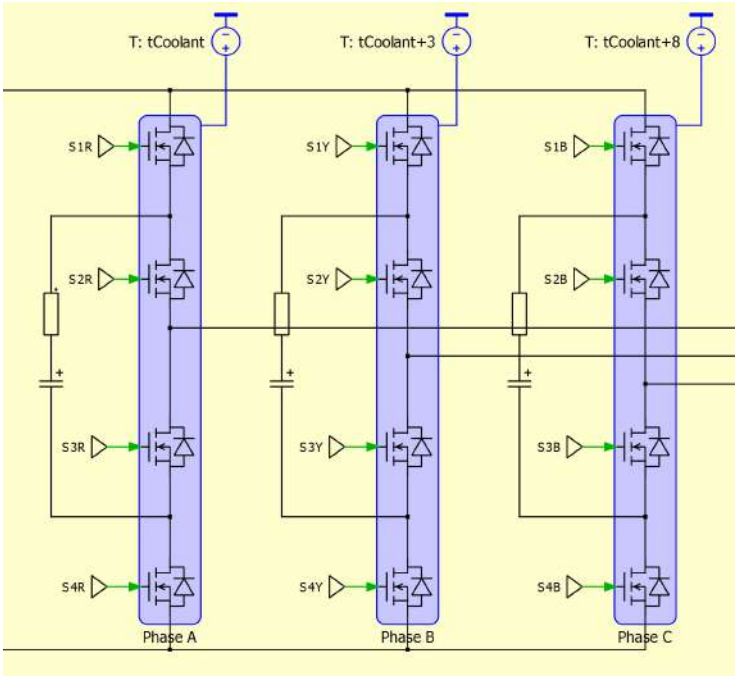


Figure 3.5: Heat sinks initialized coolant temperatures

The MOSFETs also have their own thermal model with its thermal resistance and thermal capacitance provided by the manufacturer and can be seen in Fig 3.6. The losses due to rise in temperatures based on the amount of current flowing throuhg the MOSFET's will also be captured.

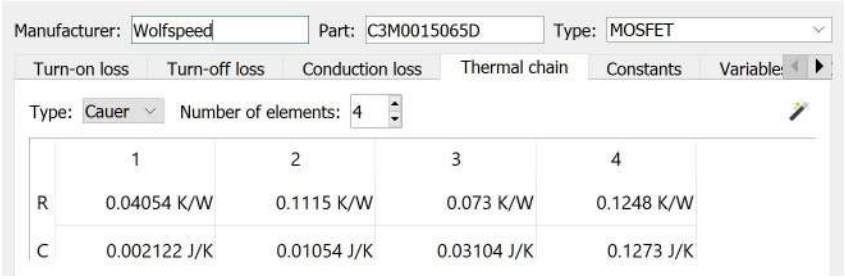


Figure 3.6: Thermal network representation for MOSFETs in PLECS model

3.1.4 Load model

The data for current flowing in the load, the input I_d and I_q currents, the line to line voltage magnitude at the output, current angle, voltage angle and power factor were given for corresponding torque and speed inputs. The modulation index was calculated by taking the ratio of phase to ground voltage and DC link voltage applied. These results were obtained by doing an FEM simulation for all speed and torque values for an electric machine. With these inputs, an open loop simulation was done.

3.1.4.1 Load as a current source

This model has been used to obtain all results except for finding THD of the phase currents. With current source as a load along with an equivalent resistance of the load, there will be same currents flowing in load for simulations in all topologies. This helps to have a better comparison in finding out which topology performs more efficiently. The load represented as current source can be seen in Fig 3.7.

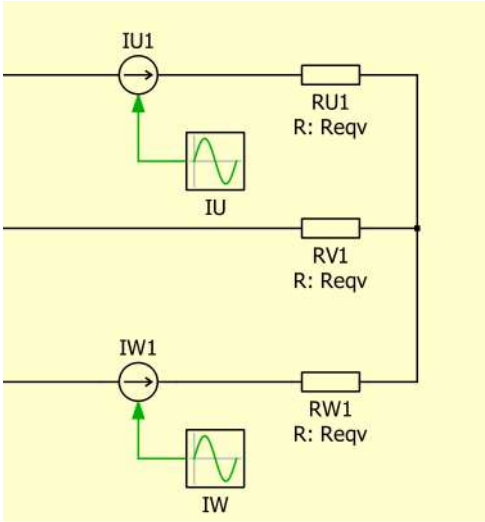


Figure 3.7: Load as a current source

3.1.4.2 Load as a RL

This model is only used to see the presence of harmonics present in the output of phase currents. It cannot be seen in the previous model as ideal sinusoidal waveforms will be generated for the phase currents due to the current source. From the electric machine data, the magnitude of load resistance was calculated from phase to ground voltage and current magnitude. The values of resistor and inductor were then calculated by multiplying magnitude of load resistance with cosine and sine of angle between voltage and current. The load represented as RL can be seen in Fig 3.8.

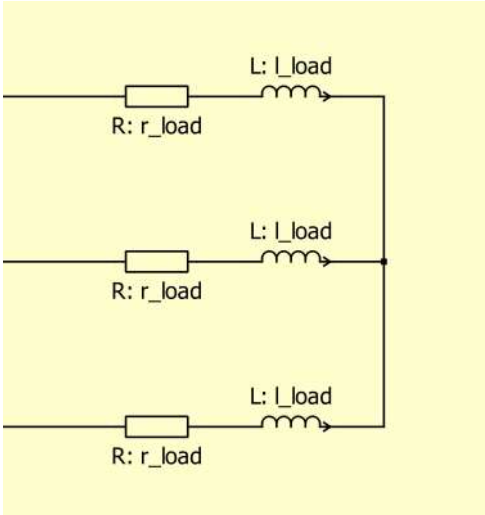


Figure 3.8: Load modelled as an RL

3.2 Case 1: Peak current analysis

The operating point chosen here is at base speed of the electric machine with the highest rated current allowed to flow in the output. As the peak current is 778A, a SiC power module is used comprising of MOSFETs connected in parallel to handle the high current rating as a single switch for TLI. The switch model used for MLIs have a blocking voltage of 700V and the TLIs instead of have a blocking voltage of 1200V. The PLECS model for TLI with 1200V blocking voltage was already available and not for the 700V blocking voltage. The datasheet for the SiC module with the blocking voltage of 700V was available. The SiC power module was modelled from the same 1200V power module PLECS model by changing the loss values according to the datasheet. The simulation was run till the temperature reaches a steady state and the time for this was found to be three seconds. The losses begin to become constant and more accurate simulation results were taken. This is the only case where the thermal parameters of the coolant have been considered along with the switch model. The parameters used for case 1 can be seen in Table 3.2.

Table 3.2: Parameters for Case 1

Parameters	Values	Units
V_{DC}	850	V
Fundamental frequency	360	Hz
Carrier frequency	10000	Hz
Modulation index	0.92	-
Current source (pk)	778	A

3.3 Case 2: Different current level analysis

The results for case 1 was seen and it was important to verify if all the topologies performed similarly different current levels. Three operating points chosen here for varying current levels. The speed has been set as a constant and the operating points were chosen for different torque levels of the electric machine. The currents chosen for case 2 can be seen in Table 3.3. The PLECS models of power module were not readily available. Hence a MOSFET was chosen with highest current rating available. The MOSFET chosen here for MLIs is C3M0015065D from Wolfspeed which is rated for a current of 150A and a blocking voltage of 650V. Six MOSFETs were decided to be considered to operate in parallel giving a total current carrying capability of 900A to simulate an equivalent power module, which will representing a single switch shown in circuit diagrams earlier. The loss and thermal network parameters of the switch were modified according as the six MOSFETs have been connected in parallel. For the TLI, the switch chosen is C3M0016120D from Wolfspeed which is rated for 115A and a blocking voltage of 1200V. Here eight MOSFETs have been considered in parallel giving a current carrying capability of 920A to simulate an equivalent power module. Eight MOSFETs were considered so that TLI and MLIs have switches with almost the same current carrying capability. The thermal parameters of the coolant have not been considered for the switch model. The temperature begins to reach its steady state more quickly. The simulation time has been considered for 0.4 seconds. Although it is not completely accurate in simulating results when compared to case 1, the same conditions are applied to all topologies. A fair comparison is still made to see which topology performs well.

Table 3.3: Parameters for Case 2

Parameters	I1	I2	I3	Units
V_{DC}	710	710	710	V
Fundamental frequency	600	600	600	Hz
Carrier frequency	10000	10000	10000	Hz
Modulation index	0.94	0.75	0.77	-
Current source (pk)	144	343	778	A
Power factor	0.74	0.99	0.77	-

3.4 Case 3: Implementation of GaN

The voltage across each switch for TLIs is V_{dc} where as for three level MLIs is $V_{dc}/2$. The battery voltage is at 800V which will be voltage across the switches for TLIs. Hence for a TLI, switches with a blocking voltage of 1200V needs to be used and for MLIs a blocking voltage of 600V needs to be used. GaN MOSFETs with a blocking voltage of 650V is widely used and has been chosen as the MOSFET for MLIs in the analysis of this case. The MOSFET selected for this comparison is GS-065-150 from GaN Systems, which has current rating of 150A and a blocking voltage of 650V. Six MOSFETs have been considered in parallel to simulate a single switch as power module with a current carrying capability of 900A. For TLIs, the same MOSFET

used in case 2 with a blocking voltage of 1200V is used. The advantage of GaN is now available to three level MLIs and investigation shall be done to see how it performs.

Table 3.4: Parameters for Case 3

Parameters	Values	Units
V_{DC}	710	V
Fundamental frequency	600	Hz
Carrier frequency	10000	Hz
Modulation index	0.62	-
Current source (pk)	78	A

4

Results

This chapter discusses about results that were obtained when for the topologies were modelled in PLECS. After that the results that were obtained in the above three case setups have been tabled. The topologies have been compared against various parameters such as efficiency, THD V_{pp} and temperature. In the end, the loss maps for certain topologies have been plotted for a wide range of operating points to have better understanding of how each topology performs.

4.1 LSPWM vs PSPWM

Topologies were simulated using LSPWM and PSPWM. The output waveforms for the FCMI topology using LSPWM and PSPWM have been shown in Fig 4.1 and Fig 4.2 respectively.

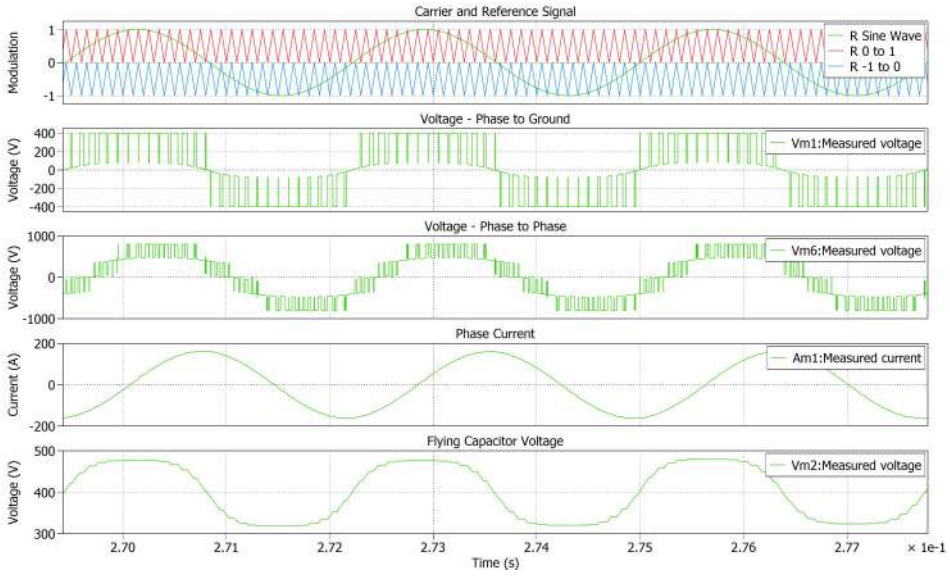


Figure 4.1: FCMI operating with LSPWM

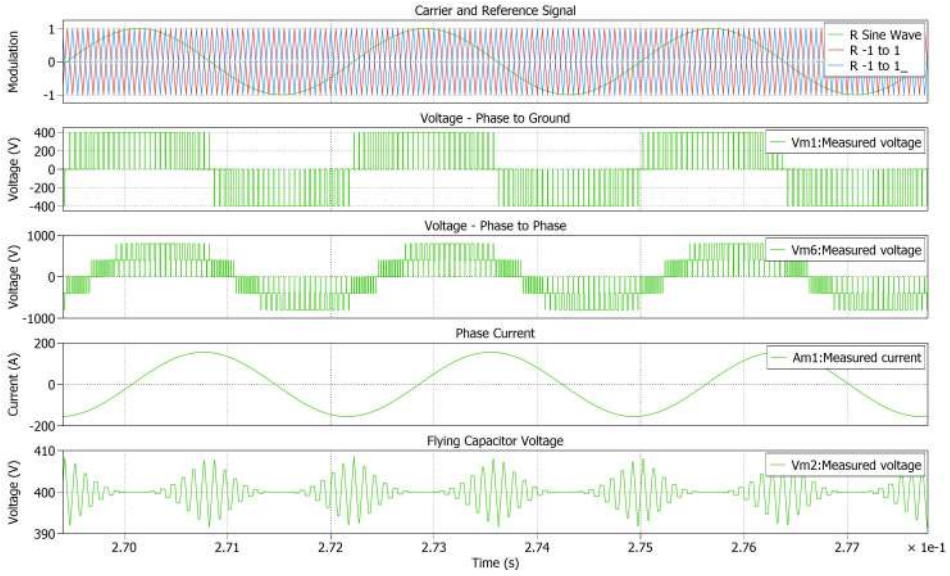


Figure 4.2: FCMI operating with PSPWM

4.2 Output waveforms for all topologies

The waveforms obtained for all topologies with the parameters mentioned in Case 1 have been shown in this section.

4.2.1 TLI

Waveforms obtained for TLI operating with SVPWM has been show in Fig 4.3

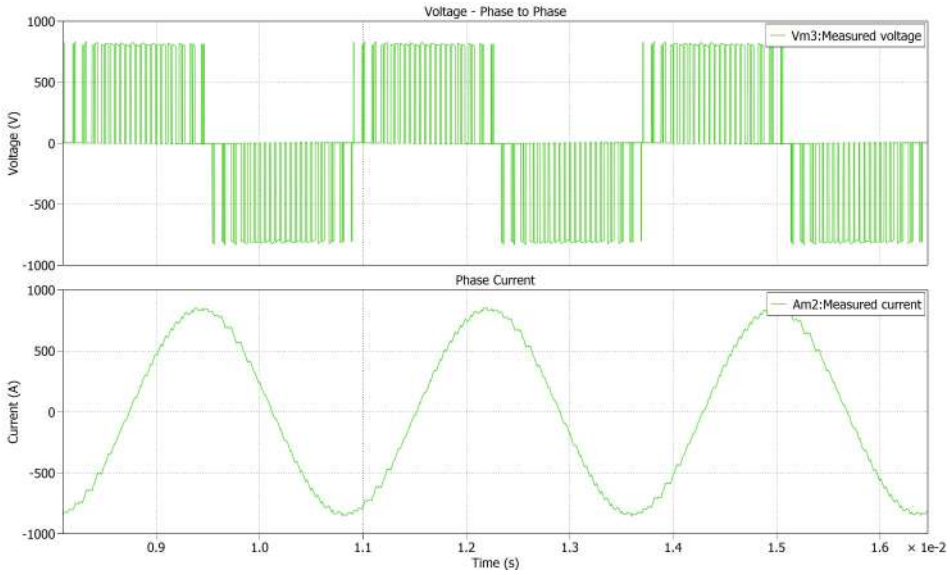


Figure 4.3: TLI output operating with SVPWM

4.2.2 NCMI

Waveforms obtained for NCMI topology operating with PSPWM and SVPWM has been show in Fig 4.4 and Fig 4.5

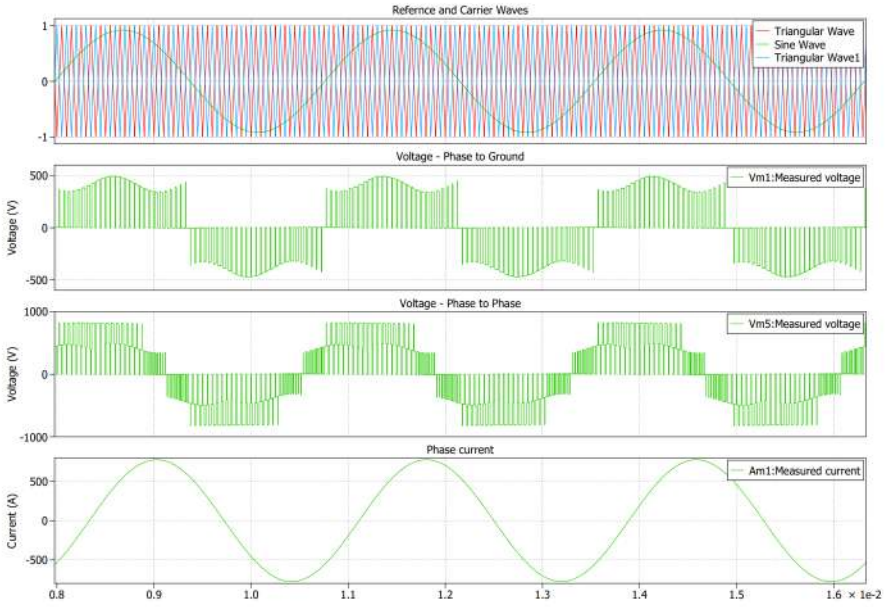


Figure 4.4: NCMI output operating with PSPWM

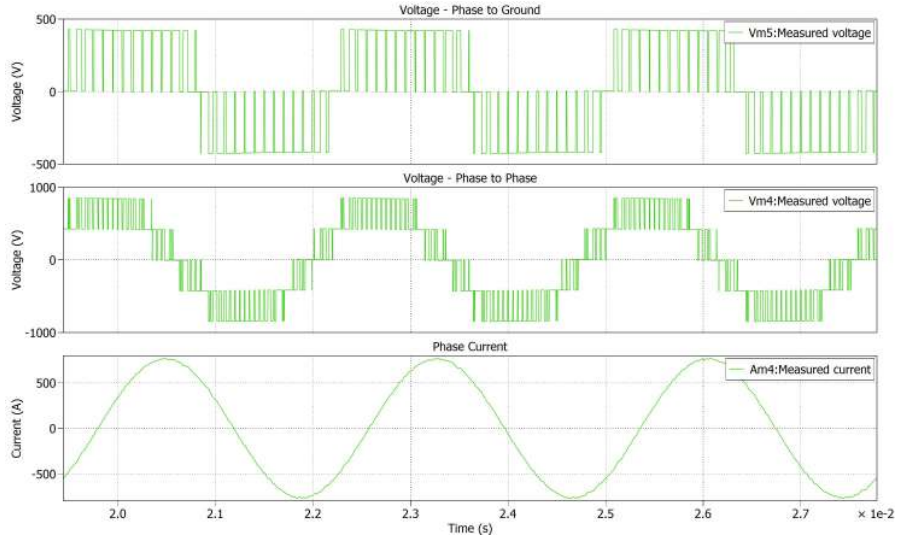


Figure 4.5: NCMI output operating with SVPWM

4.2.3 TNCMI

Waveforms obtained for TNCMI topology operating with PSPWM and SVPWM has been show in Fig 4.6 and Fig 4.7

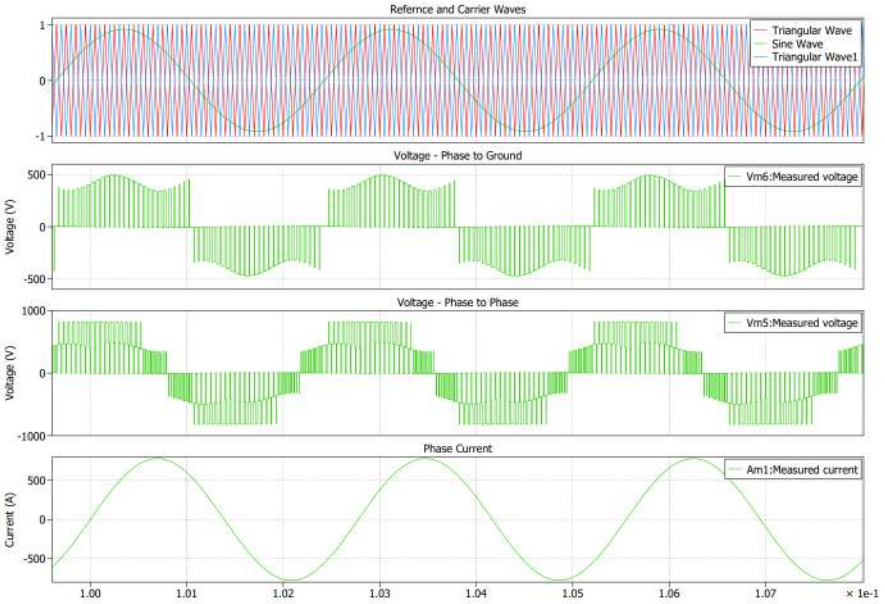


Figure 4.6: TNCMI output operating with PSPWM

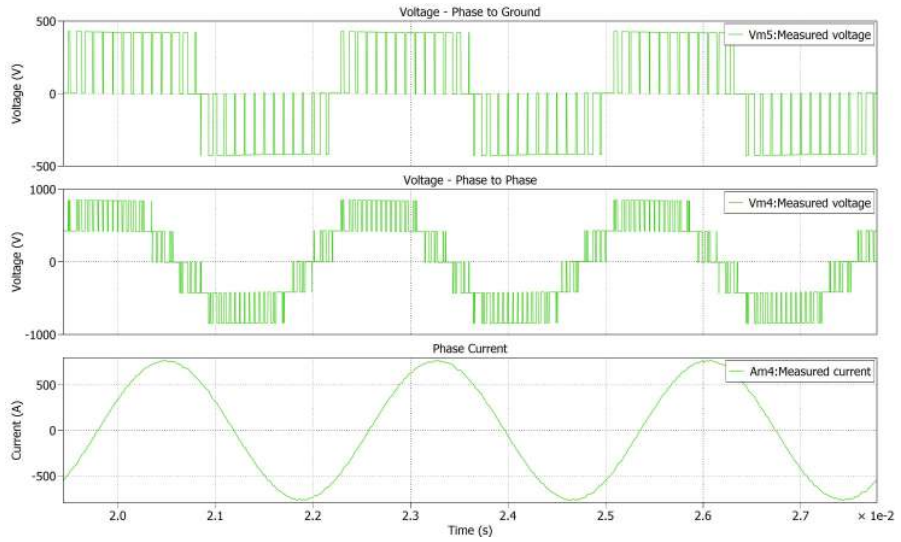


Figure 4.7: TNCMI output operating with SVPWM

4.2.4 FCMI

Waveforms obtained for FCMI topology operating with PSPWM and zero sequence injection with PSPWM has been show in Fig 4.8 and Fig 4.9

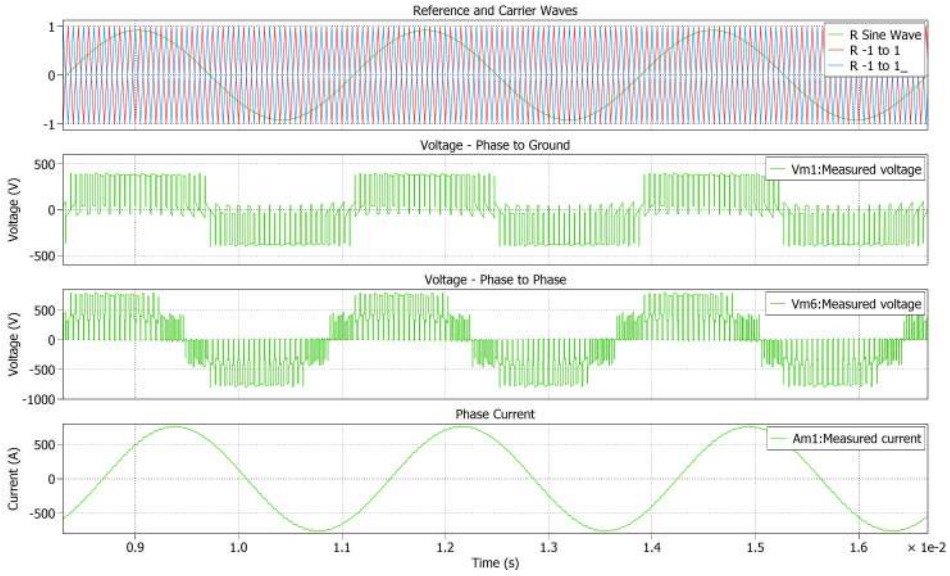


Figure 4.8: FCMI output operating with PSPWM

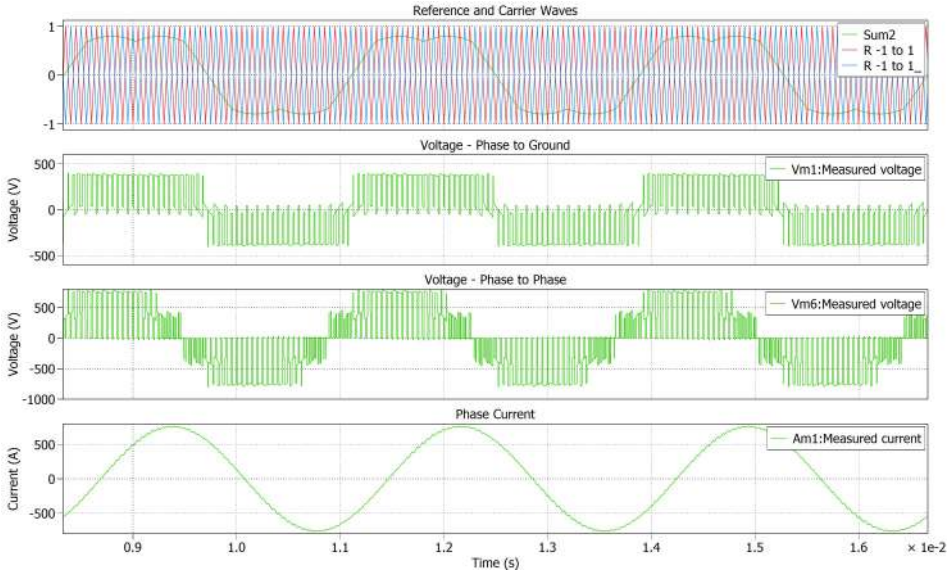


Figure 4.9: FCMI output operating with PSPWM with zero sequence injection

4.2.5 CHMI

Waveforms obtained for CHMI topology operating with PSPWM and SVPWM has been show in Fig 4.10 and Fig 4.11

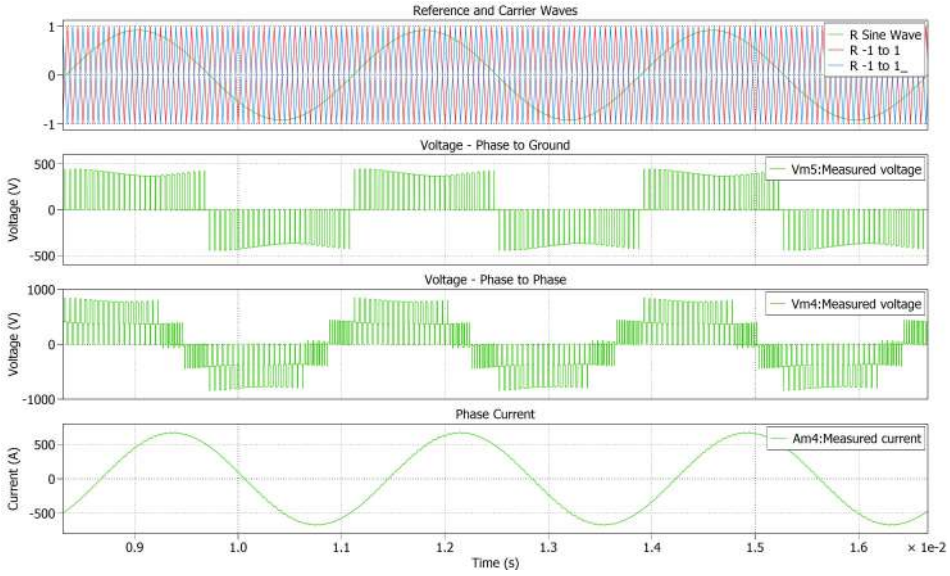


Figure 4.10: CHMI output operating with PSPWM

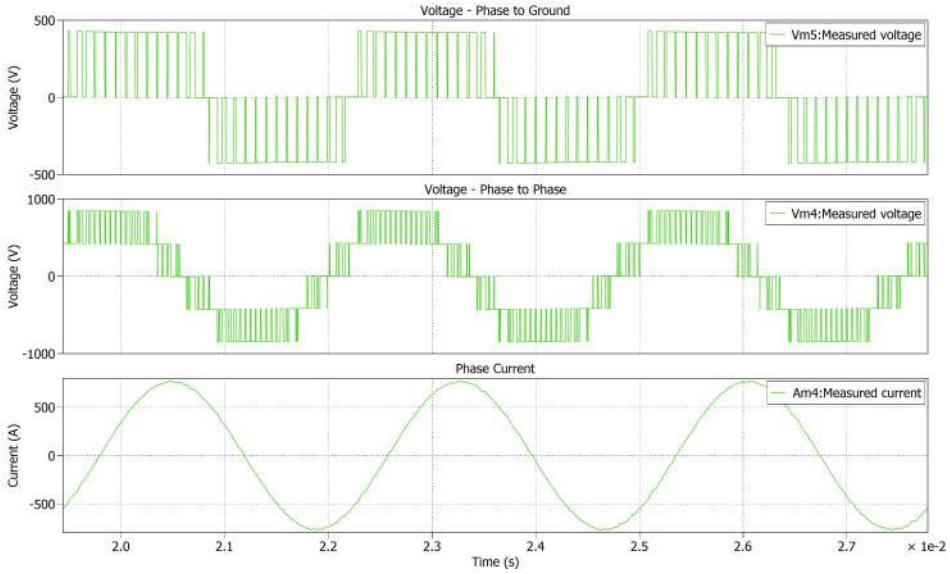


Figure 4.11: CHMI output operating with SVPWM

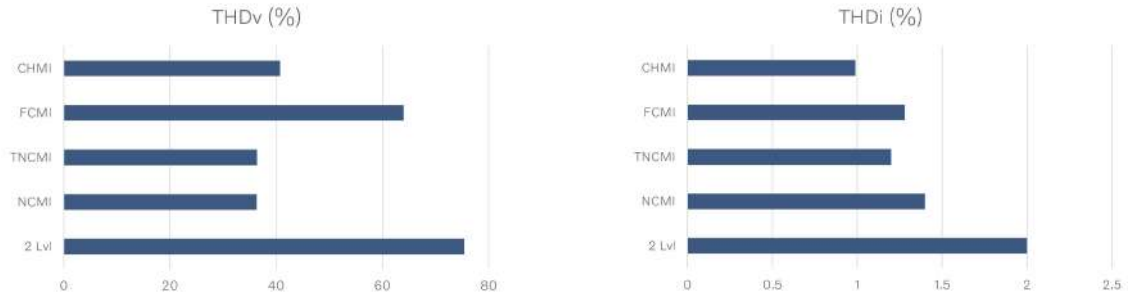
4.3 Case 1: Peak current analysis

The simulation results for Case 1 can be seen in Table 4.1. The results have been taken after the temperature in the switches have reached a steady state. This simulation also takes into consideration the thermal effect of cooling in the thermal network.

Table 4.1: Results for Case 1

Parameters	Units	2 Level	NCMI		TNCMI		FCMI		CHMI	
		SVPWM	SWPWM	SVPWM	SWPWM	SVPWM	SWPWM	Zero-sq	SWPWM	SVPWM
Efficiency	%	98.33	98.39	98.53	98.43	98.64	98.2	98.28	97.98	98.15
Output Power	kW	311.42	304.95	317.22	305.83	316.91	296.26	299.06	280.27	285.81
Losses	kW	5.3	5	4.72	3.95	3.4	5.41	5.24	5.77	5.38
THD V_{LL}	%	75.42	51.64	36.3	51.4	36.4	54.78	63.97	56.93	40.76
THD i	%	2	1.3	1.4	1.34	1.2	1.11	1.28	1.01	0.99
Temperature	°C	166.9	111.85	111.3	107.15	102	117.4	116.6	143.44	127.7
Temp. variation	°C	14	7	6.8	3	1.9	5.5	6	5.3	5.45
Volt. ripple on DC link	V	30	160	160	160	153	35	33	87	120

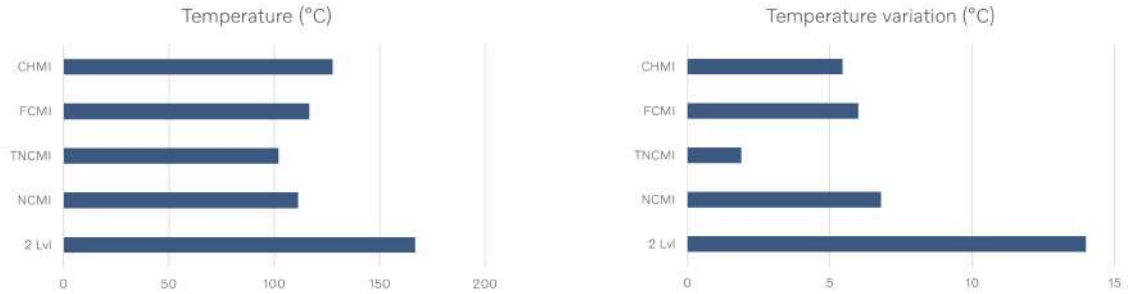
The THD comparison for all the topologies can be seen in Fig 4.12a and 4.12b



(a) THDv **(b)** THDi

Figure 4.12: THD comparison done for SVPWM switching

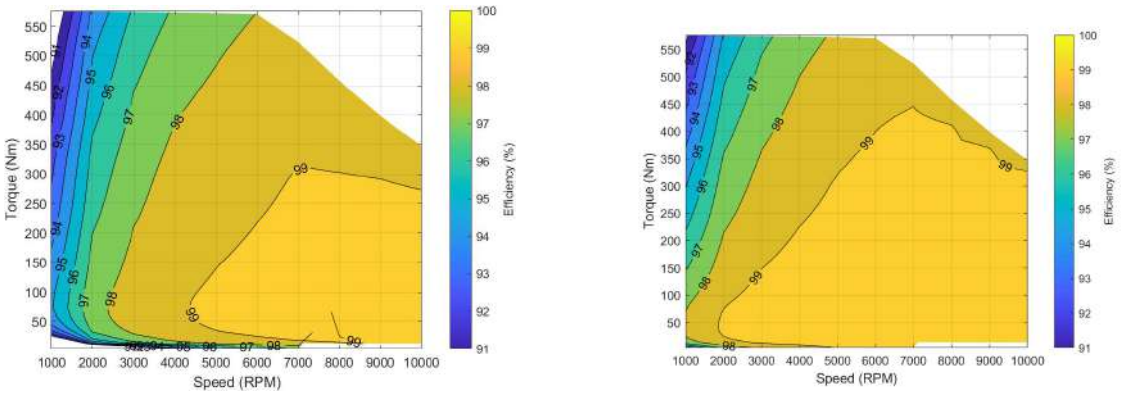
The temperature and temperature variation comparison for all the topologies can be seen in Fig 4.13a and 4.13b



(a) Temperature **(b)** Temperature variation

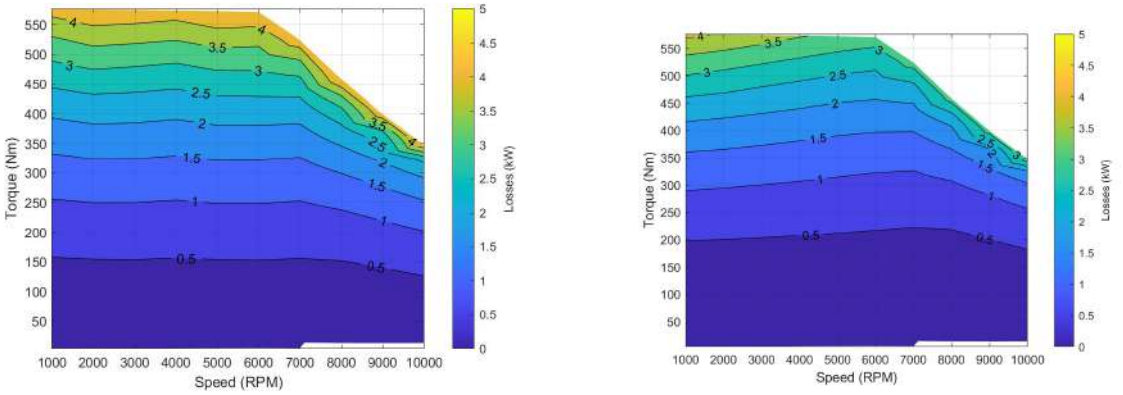
Figure 4.13: Temperature and temperature variation comparison done for SVPWM switching

The performance maps for the TLI and TNCMI operating with SVPWM can be seen in Fig 4.14, 4.15 and 4.16



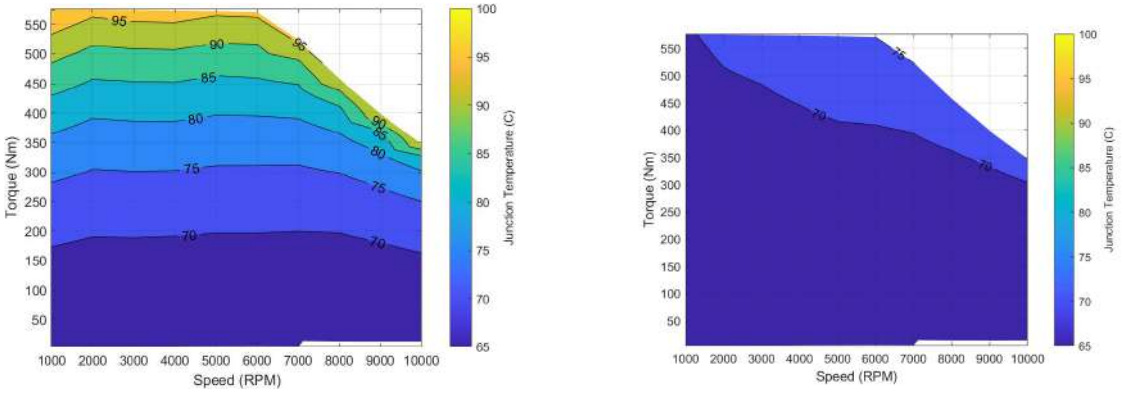
(a) TLI **(b)** TNCMI

Figure 4.14: Comparison of efficiency maps between TLI and TNCMI with SVPWM



(a) TLI **(b)** TNCMI

Figure 4.15: Comparison of loss maps between TLI and TNCMI with SVPWM



(a) TLI **(b)** TNCMI

Figure 4.16: Comparison of junction temperature maps between TLI and TNCMI with SVPWM

4.4 Case 2: Different current level analysis

The simulation results for Case 2 can be seen in Table 4.2, 4.3 and 4.4. The results have been taken after the temperature in the switches have reached a steady state. The simulations only takes into consideration the thermal effect of switches between junction to case in the thermal network.

Table 4.2: Results for Case 2 when current is I1

Parameters	Units	2 Level	NCMI		TNCMI		FCMI		CHMI	
		SVPWM	SWPWM	SVPWM	SWPWM	SVPWM	SWPWM	Zero-sq	SWPWM	SVPWM
Efficiency	%	99.43	99.46	99.54	99.6	99.7	99.52	99.52	99.47	99.6
Output Power	kW	52.34	52.1	51.81	51.9	51.69	51.68	51.69	50.87	51.45
Losses	kW	0.3	0.29	0.24	0.21	0.16	0.25	0.25	0.27	0.21
THD V_{LL}	%	76.89	50.3	37.6	50.3	38.6	50.84	60.91	50.92	37.53
THDi	%	3.81	1.77	1.86	1.63	1.72	1.78	2.21	1.79	1.8
Temperature	°C	70	67.4	66.84	67.4	66.85	67.4	67.4	68.1	67.1
Temp. variation	°C	0.53	0.14	0.14	0.1	0.1	0.16	0.16	0.16	0.1
Volt. ripple on DC link	V	5.1	19	18	19	17	6.8	6	21	25

Table 4.3: Results for Case 2 when current is I2

Parameters	Units	2 Level	NCMI		TNCMI		FCMI		CHMI	
		SVPWM	SWPWM	SVPWM	SWPWM	SVPWM	SWPWM	Zero-sq	SWPWM	SVPWM
Efficiency	%	99.16	99.1	99.2	99.33	99.42	99.13	99.13	99.04	99.19
Output Power	kW	129.38	125	126.1	125.32	126.1	124.79	124.8	120.44	123.72
Losses	kW	1.09	1.14	1.03	0.85	0.73	1.1	1.1	1.17	1
THD V_{LL}	%	99.59	78.3	43.6	78	44.3	79.12	88.89	79.28	44.46
THDi	%	18.2	13.3	6.3	13.36	6.34	13.31	14.84	13.41	6.67
Temperature	°C	81.2	72.2	71.2	72.2	70.9	73.2	73.2	77.4	73.8
Temp. variation	°C	1.8	0.8	0.8	0.32	0.32	0.75	0.6	0.75	0.61
Volt. ripple on DC link	V	10.2	34	23	34	23	14.4	10	42	46

Table 4.4: Results for Case 2 when current is I3

Parameters	Units	2 Level	NCMI		TNCMI		FCMI		CHMI	
		SVPWM	SWPWM	SVPWM	SWPWM	SVPWM	SWPWM	Zero-sq	SWPWM	SVPWM
Efficiency	%	97.98	97.86	97.9	98.24	98.38	97.65	97.67	97.35	97.54
Output Power	kW	228.03	219.7	217.2	220.35	217.2	215.79	215.81	200.7	205.978
Losses	kW	4.71	4.8	4.6	3.95	3.57	5.19	5.15	5.47	5.19
THD V_{LL}	%	97	76.8	45.1	77.6	44	79.52	87.8	81.64	48.77
THDi	%	4.58	3.33	2.05	2.28	1.78	3.35	3.71	3.39	2.36
Temperature	°C	132.4	96.72	96.7	98.6	94.7	100.8	100.9	122.2	111.8
Temp. variation	°C	7	0.5	4.1	1.7	1.4	3.3	3.2	3.46	3.6
Volt. ripple on DC link	V	24	85	68	90	68	31	26	95	115

The THD comparison for all the topologies can be seen in Fig 4.17a and 4.17b

(a) THDv **(b)** THDi

Figure 4.17: THD comparison done for all topologies

The temperature and temperature variation comparison for all the topologies can be seen in Fig 4.13a and 4.13b

(a) Temperature **(b)** Temperature variation

Figure 4.18: Temperature and temperature variation comparison done for all topologies

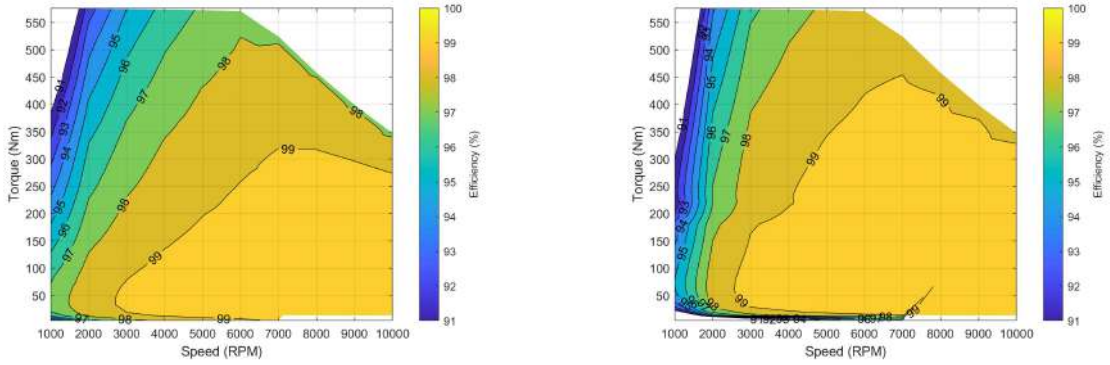
4.5 Case 3: Implementation of GaN

The simulation results for Case 3 can be seen in Table 4.5. The results have been taken after the temperature in the switches have reached a steady state. The simulations only takes into consideration the thermal effect of switches between junction to case in the thermal network.

Table 4.5: Results for Case 3

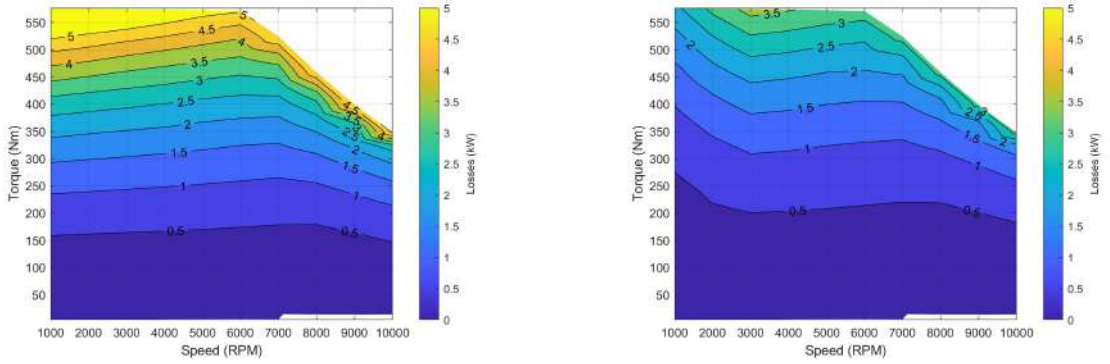
Parameters	Units	2 Level	NCMI		TNCMI		FCMI		CHMI	
		SVPWM	SWPWM	SVPWM	SWPWM	SVPWM	SWPWM	Zero-sq	SWPWM	SVPWM
Efficiency	%	98.54	98.98	99.01	99.08	99.16	98.83	98.83	98.84	99.02
Output Power	kW	24.1	23.85	24.03	23.9	24.02	23.83	23.83	23.69	24
Losses	kW	0.36	0.25	0.24	0.22	0.2	0.28	0.28	0.28	0.24
THD V_{LL}	%	125.8	97.8	49.8	97.8	49.8	97.91	112.12	97.24	50.43
Temperature	°C	94.2	76.2	76.6	76.2	76.1	76.2	76.1	76.2	76.43
Temp. variation	°C	8	2.7	2.8	7.7	1.9	2.2	2.2	2.2	1.82
Volt. ripple on DC link	V	2.2	7.5	4	7.4	3.8	2.8	2.2	7	8.5

The performance maps for the TNCMI topology with SiC and GaN switches operating with SVPWM can be seen in Fig 4.19, 4.20 and 4.21



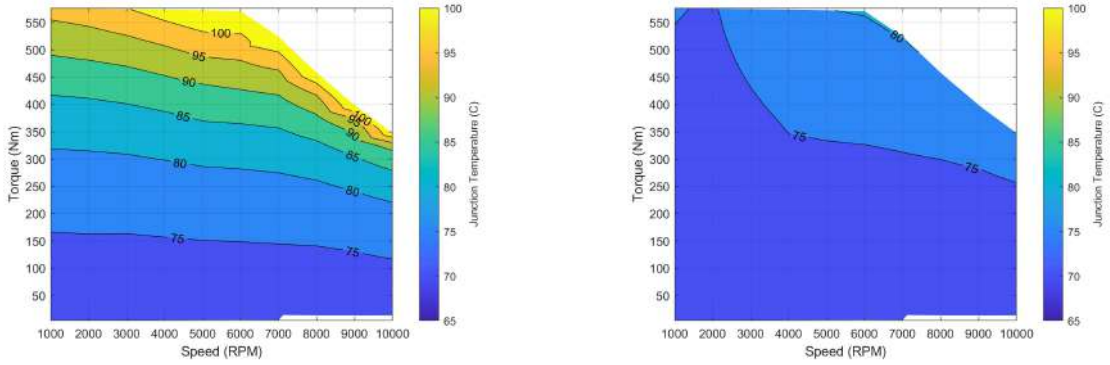
(a) TNCMI with SiC **(b)** TNCMI with GaN

Figure 4.19: Comparison of efficiency maps between TNCMI topology with SiC and GaN switches with SVPWM



(a) TNCMI with SiC **(b)** TNCMI with GaN

Figure 4.20: Comparison of loss maps between TNCMI topology with SiC and GaN switches with SVPWM



(a) TNCMI with SiC **(b)** TNCMI with GaN

Figure 4.21: Comparison of junction temperature maps between TNCMI topology with SiC and GaN switches with SVPWM

5
Discussion

5.1 Analysis of number of components in MLIs

Table 5.1 presents the number of components being used in the topologies that have been implemented. The MLI topologies are using twice the number of switches when compared to the TLI. The switches in the TLI will have an operating voltage of 800V but the MLIs will only have an operating voltage of 400V except for the TNCMI topology. For the TNCMI, six switches will have an operating voltage of 800V and 400V for the other six switches. The MLIs can now have switches with reduced blocking voltages. This leads to lower switching losses and $R_{ds(on)}$ compared to the switches used in the TLI. The CHMI topology needs three DC link capacitors, one for each phase leg. The other MLI topologies make use of two DC link capacitors which makes it possible to split the DC source voltage in half.

There are additional components present in other topologies which enable their operation. The NCMI has six clamping diodes, the FCMI has three flying capacitors and the CHMI has three DC sources instead of one. Even though the MLIs switches have their blocking voltage halved, they have more components present. The conduction losses due to these components will also need to be considered.

Table 5.1: Number of components present in MLIs

Components	TLI	NCMI	TNCMI	FCMI	CHMI
Switches (650kV BV)	0	12	6	12	12
Switches (1200kV BV)	6	0	6	0	0
DC link capacitors	1	2	2	2	3
Clamping diodes	0	6	0	0	0
Flying capacitors	0	0	0	3	0
DC source	1	1	1	1	3

5.2 LSPWM vs PSPWM

The LSPWM and PSPWM had their own advantages when they were implemented. From Fig 4.1 and Fig 4.2 it is observed that the LSPWM strategy has less THD in the phase-to-phase voltage. This strategy can be chosen if the THD in voltage needs to be reduced. When PSPWM strategy was used, all four switches in a single phase leg were in operation when the reference carrier wave ranged between 0 and

1. But for the LSPWM strategy, only the top two switches were in operation and the bottom two switches were in operation when the reference carrier wave ranged between -1 and 0. For this thesis, the PSPWM was chosen so that all four switches in a single phase leg were more evenly used. For the FCMI topology, the PSPWM strategy is more beneficial. It helps to naturally balance the voltages at the flying capacitors. The voltage ripple when using LSPWM was 180V whereas it was only 20V when the PSPWM strategy was used for the same value of flying capacitors.

5.3 SVPWM vs Zero sequence injection

The reference waveforms for the SVPWM and the zero sequence injection in the PSPWM modulation techniques look similar. But from the theory, it is known that their method of working is completely different. The difference in results can be inferred from Fig 4.9 Fig 4.11. The THD in phase-to-phase voltage is better in the SVPWM strategy. Also in all the case simulation setups for the FCMI topology, the measured efficiency almost remains the same for the PSPWM strategy and the zero sequence injection strategy. When a comparison is made between the PSPWM strategy and the SVPWM strategy in other topologies, improvements in efficiencies were always seen. The main reason for this is that in the zero sequence injection strategy, only the reference signal is changed but the switching method is the same as the PSPWM strategy. The only difference between the PSPWM strategy and the zero sequence injection strategy is that the zero sequence injection strategy can now have a modulation index up to 1.15. The SVPWM strategy is more efficient because it has a more efficient switching method. As explained earlier theory, it makes sure the losses are reduced by changing the switching level in only one of the three phases as the reference voltage moves from one region to another. The output phase-to-phase voltage also has a reduced THD when compared to the PSPWM modulation implemented with PSPWM.

5.4 Case study analysis

In this section each case will be analyzed and discussed individually.

5.4.1 Case 1

In case 1, all the inverter models were analysed for the peak current operating point. The simulation results are presented in Table 4.1. The NCMI and the TNCMI have better efficiency than the TLI with the SVPWM modulation technique. Apart from the efficiency, the THDv, THDi, temperature and temperature variation of the switches were also analyzed and comparisons have been made in Fig 4.12 and 4.13. From these results, it is inferred that the MLIs perform better when compared to the TLI. The NCMI and the TNCMI have the lowest THDv but in the case of THDi, CHMI has the lowest value. The TNCMI has a 52% less THDv and a 40% less THDi when compared to the TLI. In the case of the temperature rise and the temperature variation of the switches, the TNCMI performs the best. In comparison

to the TLI, the TNCMI has a 39% less rise in temperature rise and a 86% less rise in temperature variation in the switches with 700V blocking voltage. Since the TNCMI performed better in most of the cases, performance maps were plotted for the TLI and the TNCMI operating with the SVPWM modulation technique for efficiency, total loss and junction temperature which can be seen in Fig 4.14, 4.15 and 4.16. In the efficiency map, the TNCMI has a bigger operating area for 99% efficiency when compared with the TLI. This is also reflected in the loss maps as well. The TLI has losses of more than 4kW for higher torque values whereas the TNCMI mostly has losses of less than 4kW. The operating temperature of the switches also contributes to losses. For high torque operating points, the temperature of the switches has risen to more than 95C in the TLI whereas it has risen to only 75C in the TNCMI.

5.4.2 Case 2

In case 2, all the inverter models were analysed for three different current levels. The simulation results are presented in Table 4.2, 4.3 and 4.4. The results obtained were similar to case 1 for different values of current as well. From these results, it is inferred that the TNCMI has better efficiency than the other topologies for all the three current levels. The THDv and THDi for the TNCMI, NCMI and CHMI operating with the SVPWM modulation technique have significantly less when compared to the TLI and can be seen in Fig 4.17. In the temperature rise and the temperature variation of the switches, the TNCMI performs better operating with the SVPWM modulation technique and the NCMI operating with the PSPWM has better performance in temperature variation of the switches which are shown in Fig 4.18. The main reason for this test was to see the effect of THDv and THDi for lower current levels.

5.4.3 Case 3

In case 3, the GaN switches are implemented in place of the SiC switches to analyse how the inverter models performed. The simulation results are presented in Table 4.5. The results were similar to case 1. Even with a GaN switch, the TNCMI operating with the SVPWM modulation technique is still the most efficient topology. The TNCMI topology showed the best performance in terms of THDv, temperature rise and temperature variation as well. Since the TNCMI has the best performance with both GaN and SiC switches, a comparison was made with GaN and SiC switches and performance maps were plotted for efficiency, total loss and junction temperature and the same can be seen in Fig 4.19, 4.20 and 4.21. In the efficiency map, the TNCMI with GaN switches has a bigger operating area for 99% efficiency when compared with SiC switches. This is also reflected in the loss maps as well. The TNCMI with SiC switches has losses of more than 5kW for higher torque values whereas the TNCMI with GaN switches mostly has losses of less than 3.5kW. For high torque operating points, the temperature of the switches has risen to more than 95C in the TNCMI with SiC switches whereas it has risen to only 80C in the TNCMI with GaN switches.

5.5 Short coming from simulations

For the purposes of making comparisons fair, the same input parameters have been given in all cases. But it is also important to mention what considerations could be included to get even more accurate results.

5.5.1 Efficiency maps

The efficiency maps have been plotted with a much shorter simulation time. This was done due to the long simulation time it takes for one operating point where the temperature measured at the MOSFETs reaches a steady state. Although every operating point is run for the same simulation time in all topologies, more accurate results can be obtained if the measured parameters are taken after the temperature reaches a steady value. The results when compared are expected to have similar inferences from the results that have been already obtained from case 2 at different current levels.

5.5.2 Loss estimation

The MOSFET models used in PLECS have been used by different manufacturers. In PLECS there are separate tabulations to calculate the turn-on losses, the turn-off losses and the conduction losses. Along with the look-up tables provided, formulas with additional parameters have been given to estimate the losses. These formulas and parameters vary depending on the manufacturer. In this thesis, only the look tables for considered. To get more accurate results for losses, a better understanding of the parameters and formulas given by the manufacturers needs to be considered. Communication with the manufacturer will aid in understanding this but was not done due to time limitations. But since the same switches were used for making comparisons in the test cases, all the topologies will have the same level of accuracy.

5.5.3 Compatibility between PLECS and Simulink

In this thesis, the simulations were done in Matlab / Simulink and PLECS software. All the inverter topologies were modelled in PLECS since the switch models of various MOSFET manufacturers were available online for implementation in PLECS and also the thermal model of the inverter has been modelled using three individual heat sinks. But in the case of modelling the SVPWM strategy for inverter switching, Matlab / Simulink was used. The Matlab function block was used to develop the logic of a three-level SVPWM as the implementation strategy varies depending upon the topology used. Due to this, the solver from Simulink was used for simulation in the SVPWM strategy instead of the PLECS solver. The time taken to run a simulation for even 3 seconds was higher for the SVPWM technique when compared to the PSPWM technique as the PSPWM did not require developing a logic using the Matlab function block and just the logical function blocks in the PLECS software were sufficient. So, if the SVPWM technique is also developed using the PLECS software, the simulation run time might be reduced.

5.6 Sustainable aspects

When it comes to the automobile industry, the greenhouse gas emissions and the CO_2 emissions are one of the most concerning areas for the environmental aspects since they play a significant role in air pollution, resulting in climate change. For instance, about one-quarter of the total greenhouse gases in the EU are produced by the transport sector. Hence, there have been high requirements set by the EU commission for these CO_2 emissions produced by vehicles with IC engines [15]. One of the alternatives for the automobile industry is to replace IC engine vehicles with EVs as they have the potential to reduce greenhouse gas emission and thus the rapid growth of interest in electrification of passenger vehicles over the last decade. Also, the electricity needed for charging the EVs should come from renewable energy sources since there will be CO_2 emissions if non-renewable energy sources are used which will be a conflict of interest in this case [16]. It has been concluded that the usage of EVs in the EU has reduced CO_2 emissions by 80% compared to IC engines as they do not emit noxious chemicals, which can be very dangerous to the environment. Hence, analyzing and studying the performance of the inverter, which is a significant part of the EV, helps improve the efficiency and the power losses in the device. This in turn helps in the reduction of input power required for the EVs and achieve the goal set by the EU commission [17].

5.7 Ethical aspects

While working on this thesis, the authors followed the Institute of Electrical and Electronics Engineers (IEEE) Code of Ethics [18] to avoid any ethical misconduct. Below are a few points from the code of ethics that was followed during this thesis work.

Considering the fifth point in the code which says, "*to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, to be honest and realistic in stating claims or estimates based on available data, and to credit properly the contributions of others;*" As the thesis work is solely based on simulations, there could be risk of manipulation in the data to require the desired results. This was avoided by having weekly meetings with supervisors and the results were presented and discussed. Also, for each test case, the same switches and operating parameters were given to all topologies.

Considering the seventh point in the code which says, "*to treat all persons fairly and with respect, and to not engage in discrimination based on characteristics such as race, religion, gender, disability, age, national origin, sexual orientation, gender identity, or gender expression;*" To avoid this, it was made sure to have open and clear conversations within the group. Also attending meetings on time also helped establish a good understanding among the group members. Even during some disagreements during the meetings, the technical points were presented in multiple ways to explain the problem and solutions or agreement within the group was reached.

6
Conclusion

In this thesis work, different inverter topologies of the MLIs and the TLI were modelled and simulated to investigate and analyse the performance of the inverter models. A comparison was also made between all the topologies on various aspects such as efficiency, power loss, THD for both current and voltage and also temperature for three different test cases.

So to conclude, the MLIs performed better in many aspects and in particular, the TNCMI had better performance in most aspects. This was expected since the MLIs have lower switching loss and conduction loss compared to a TLI. This is mainly due to the reduced operating voltage in which the switches to almost half in value when compared with the TLI switches, which in turn helps in improving efficiency. Selecting the switching technique also made a significant improvement in the performance of the inverters. With the use of the SVPWM technique, there was a significant reduction THDv and also the efficiency was improved when compared with the PSPWM technique. Along with the switching technique, the type of switch that is used is also important. In this thesis work, the GaN switches performed better than the SiC switches for all MLIs. But there is a trade-off with the size and cost of the device as when the number of levels increases, the number of components will also increase which in turn increases the size of the inverter. So all these aspects need to be considered when selecting a topology as to which topology suits the application best.

6.1 Future work

As the MLI is a vast topic, further studies can be done based on the existing results from this thesis.

- Implementation of a closed loop system and make dynamic analysis based on the speed and torque of the motor for all the MLIs.
- Design a control strategy to reduce the voltage ripple on the DC link capacitors.
- Analyze the effect of Electromagnetic interference (EMI) in all the MLI topologies.
- This project focuses only on three-level inverter topologies, but further analysis can be done by increasing the number of levels and comparing the results with the existing three-level models.
- Modelling the SVPWM strategy in PLECS instead of Matlab as the compat-

ibility issues can be avoided between the two softwares and the time to run a simulation will be significantly low.

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A

Appendix 1 - Simulation models

A.1 TLI

Complete circuit diagram and implementation for the TLI topology

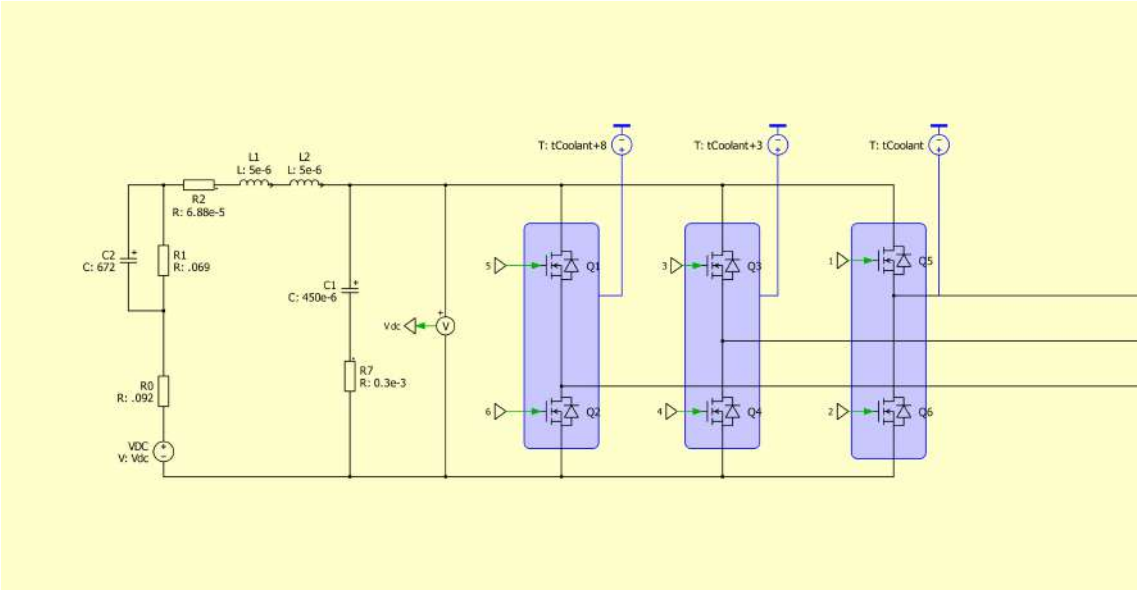


Figure A.1: Circuit diagram for the TLI with SVPWM

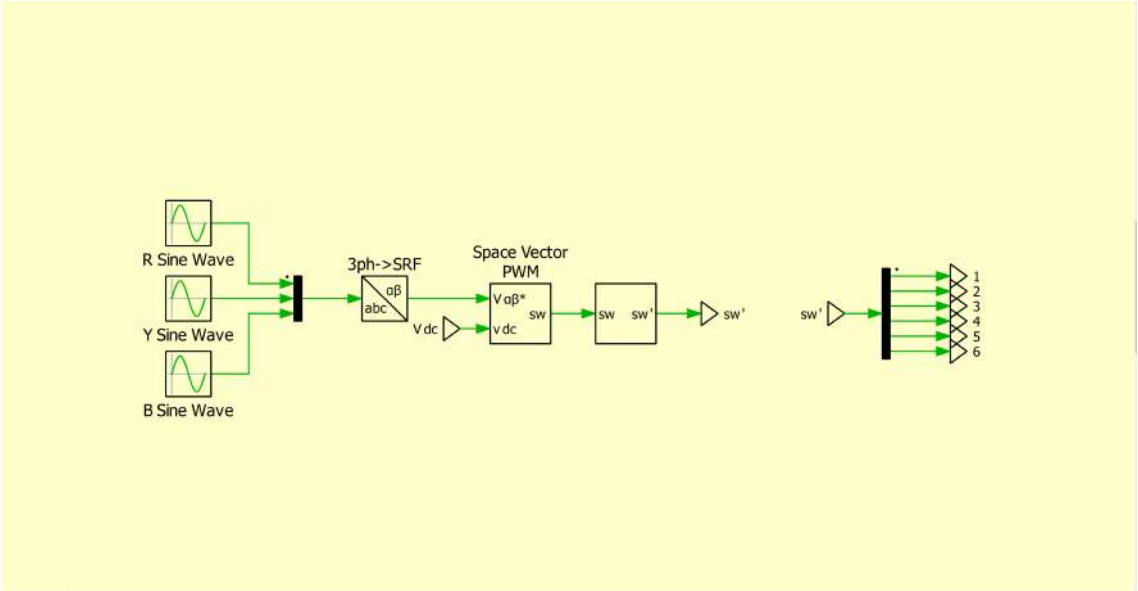


Figure A.2: Logical operation for the TLI with SVPWM

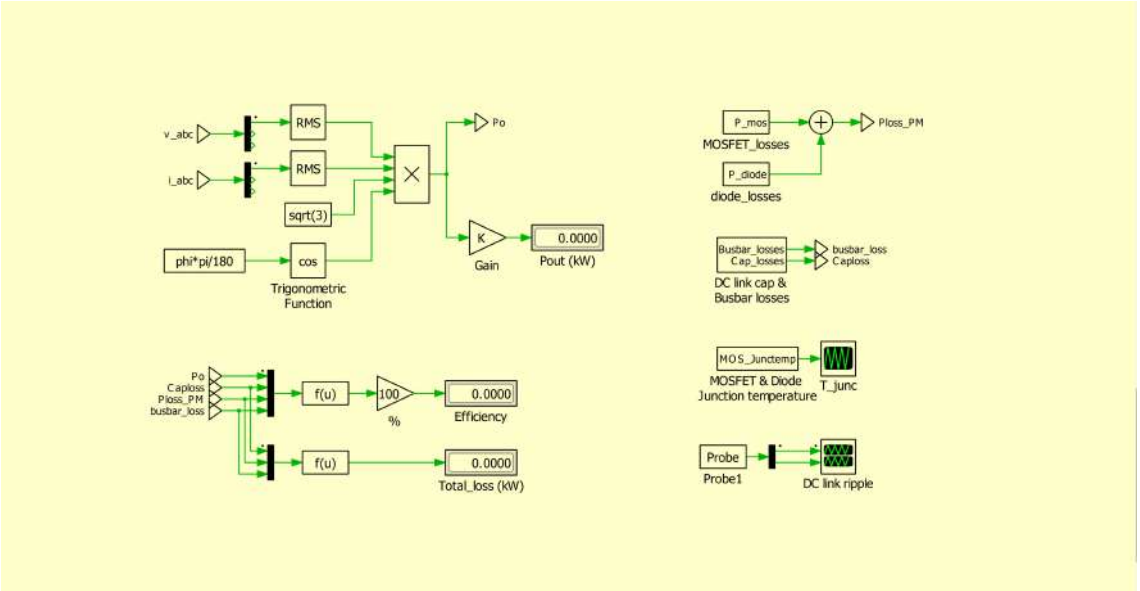


Figure A.3: Loss and efficiency calculation for the TLI with SVPWM

A.2 NCMI

Complete circuit diagram and implementation for the NCMI topology

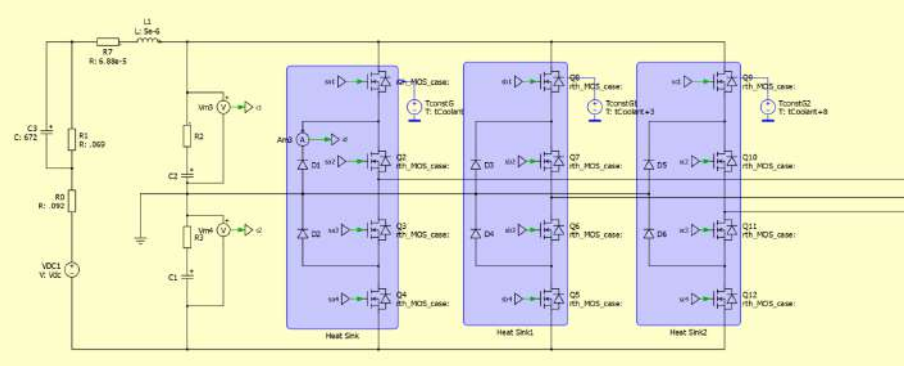


Figure A.4: Circuit diagram for the NCMI with PSPWM

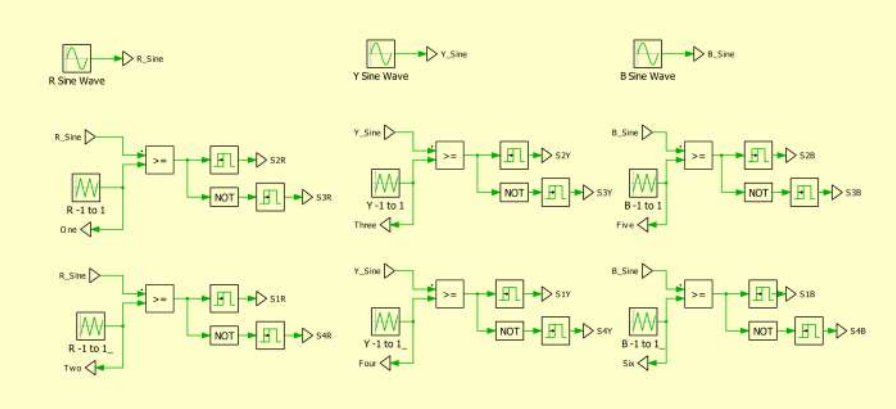


Figure A.5: Logical operation for the NCMI with PSPWM

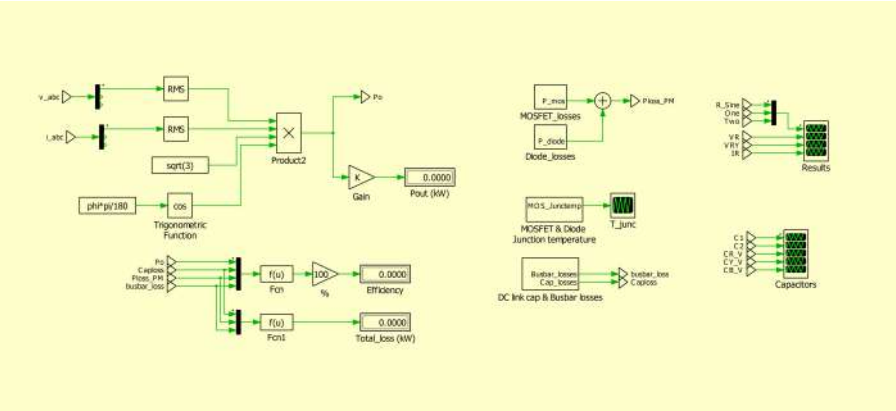


Figure A.6: Loss and efficiency calculation for the NCMI with PSPWM

A.3 TNCMI

Complete circuit diagram and implementation for the TNCMI topology

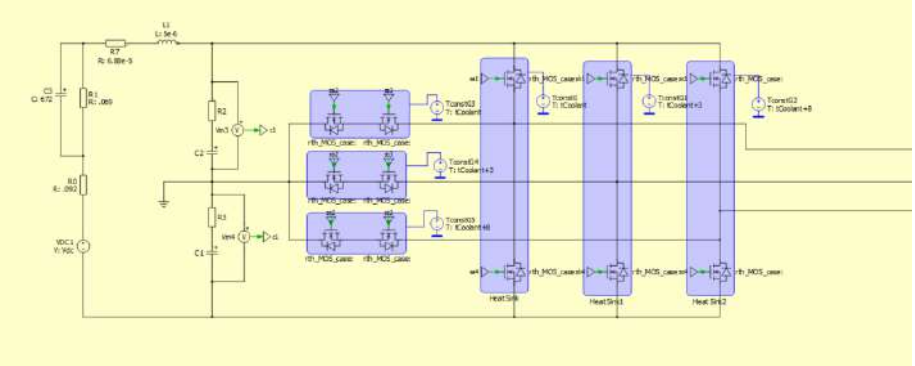


Figure A.7: Circuit diagram for the TNCMI with PSPWM

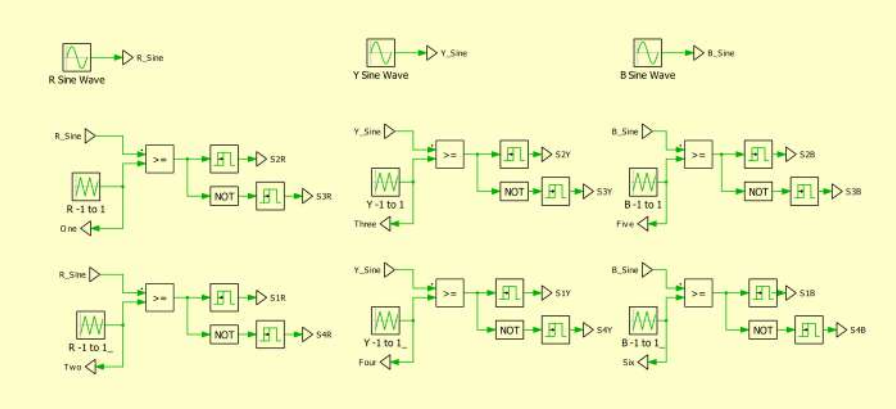


Figure A.8: Logical operation for the TNCMI with PSPWM

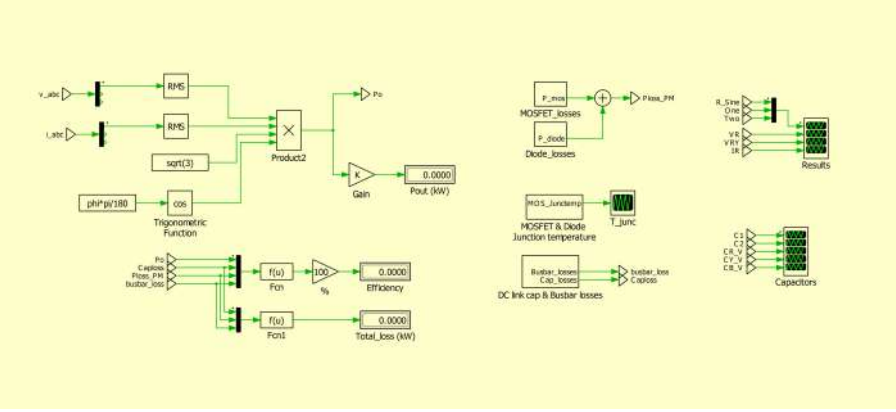


Figure A.9: Loss and efficiency calculation for the TNCMI with PSPWM

A.4 FCMI

Complete circuit diagram and implementation for the FCMI topology

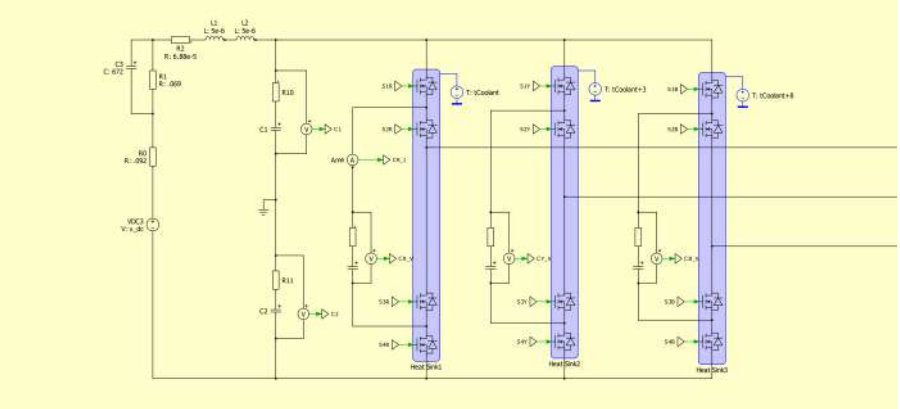


Figure A.10: Circuit diagram for the FCMI with PSPWM

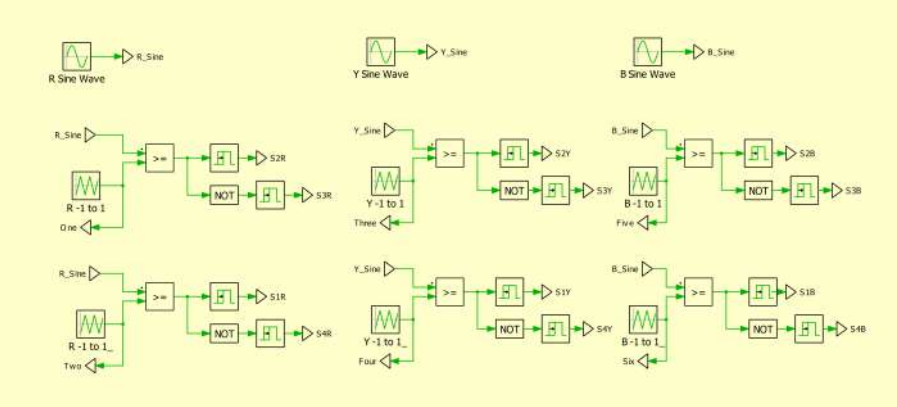


Figure A.11: Logical operation for the FCMI with PSPWM

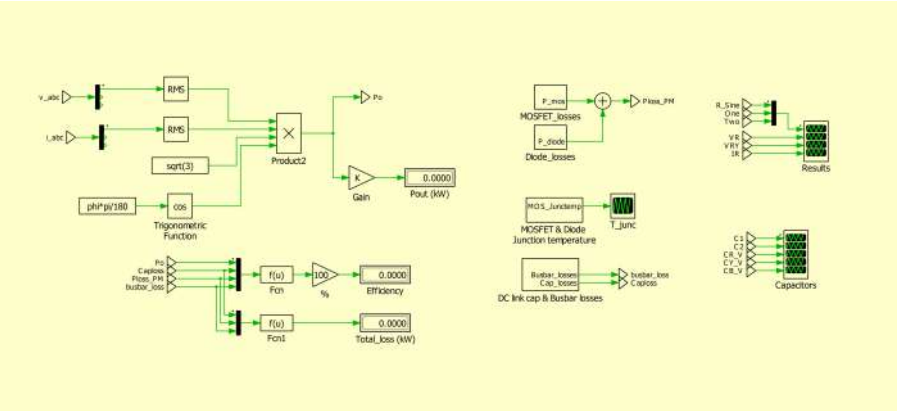


Figure A.12: Loss and efficiency calculation for the FCMI with PSPWM

A.5 CHMI

Complete circuit diagram and implementation for the CHMI topology

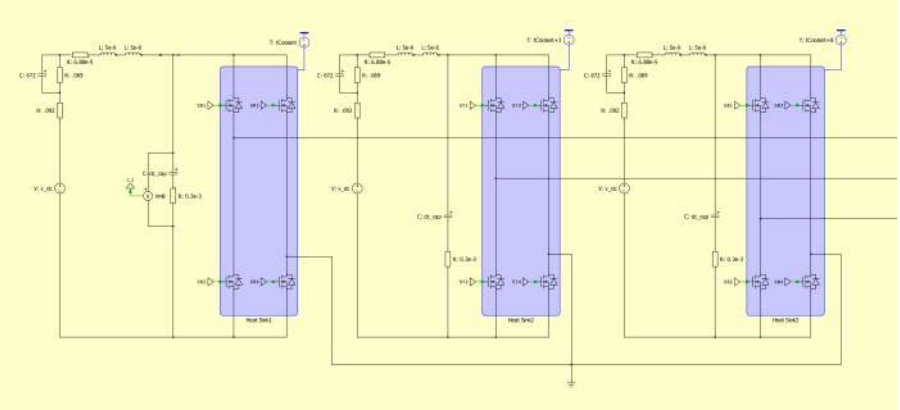


Figure A.13: Circuit diagram for the CHMI with PSPWM

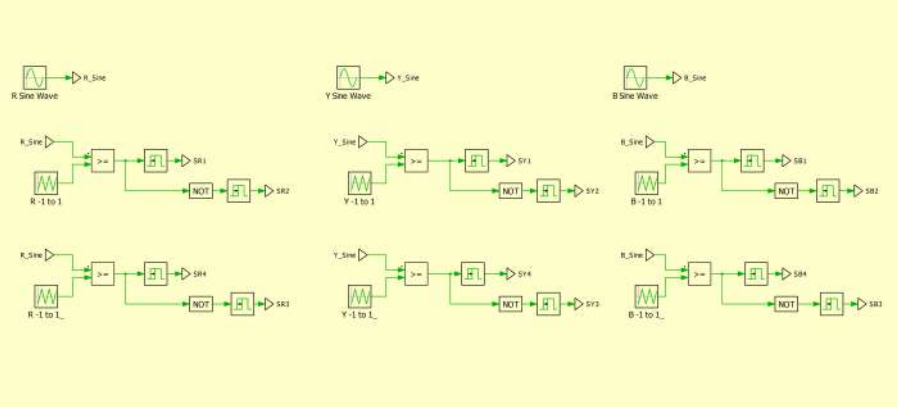


Figure A.14: Logical operation of the CHMI with PSPWM

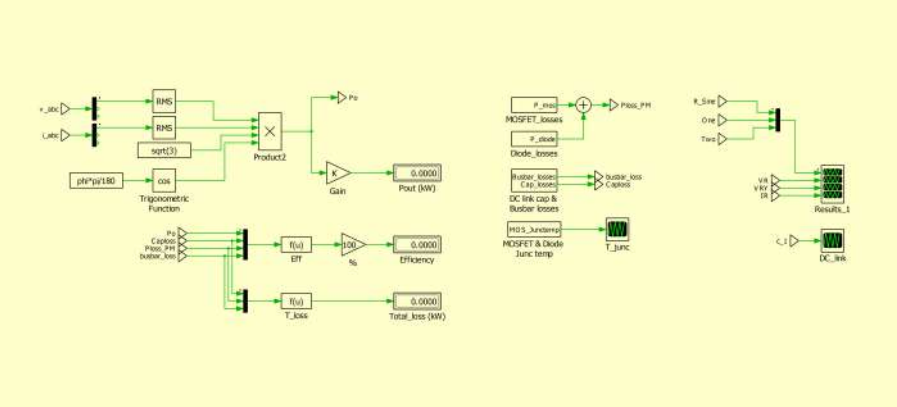
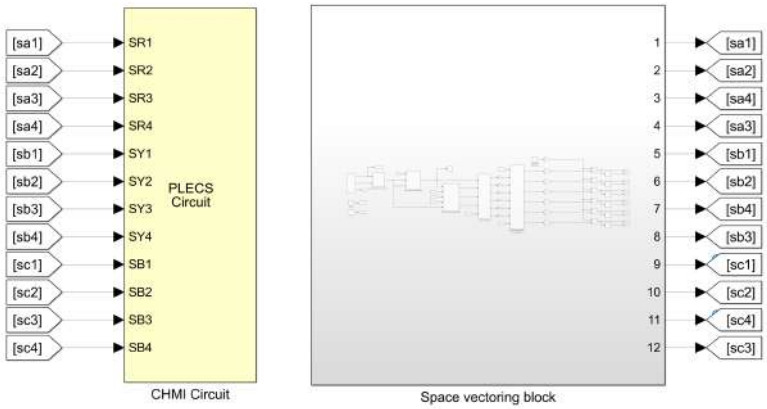
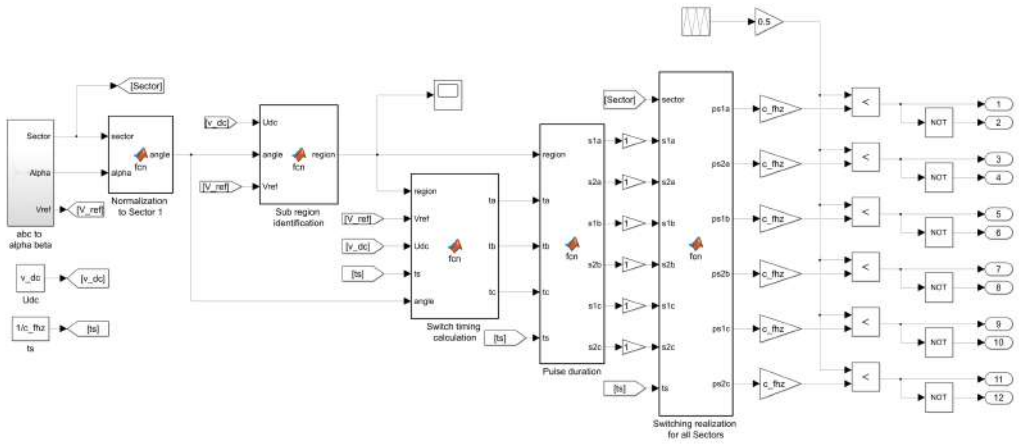


Figure A.15: Loss and efficiency calculation for the CHMI with PSPWM

A.6 SVPWM implementation



(a) Communication between the PLECS and Simulink software



(b) Block diagram for SVPWM implementation in Simulink

Figure A.16: Implementation for the SVPWM technique in the Simulink software

B

Appendix 2 - MATLAB scripts

These are the MATLAB scripts present inside the respective function blocks shown in Figure A.16

B.1 Normalization to Sector 1

MATLAB script used to normalize the voltage vector as it moves in all sectors to Sector 1.

```
function angle = fcn(sector,alpha)
angle = 0;
if (sector == 1)
angle = alpha;
end
if (sector == 2)
angle = alpha-pi/3;
end
if (sector == 3)
angle = alpha-2*pi/3;
end
if (sector == 4)
angle = alpha+pi;
end
if (sector == 5)
angle = 2*pi/3+alpha;
end
if (sector == 6)
angle = pi/3+alpha;
end
```

B.2 Sub region identification

MATLAB script used to identify in which sub-region the voltage vector is present in Sector 1.

```
function region = fcn(Udc, angle, Vref)
region = 0;
ma = sqrt(3)*(Vref/Udc);
m1 = ma*(cos(angle)-(sin(angle)/sqrt(3)));
m2 = (2/sqrt(3))*ma*sin(angle);
if (m1<0.5) && (m2<0.5) && (m1+m2<0.5)
    region = 1;
end
if (m1<0.5) && (m2<0.5) && (m1+m2>0.5)
    region = 2;
end
if (m2>0.5)
    region = 3;
end
if (m1>0.5)
    region = 4;
end
```

B.3 Switching timing calculation

MATLAB script used to for the calculation of the switching time for the CHMI topology.

```
function [ta, tb, tc] = fcn(region, Vref, Udc, ts, angle)
ta = 0;
tb = 0;
tc = 0;

ma = sqrt(3)*(Vref/Udc);
if (region == 1)
    ta = 2*ts*ma*sin((pi/3)-angle);
    tb = ts*(1-2*ma*sin((pi/3)+angle));
    tc = 2*ts*ma*sin(angle);
end
if (region == 2)
    ta = ts*(1-2*ma*sin(angle));
    tb = ts*(2*ma*sin((pi/3)+angle)-1);
    tc = ts*(1-2*ma*sin((pi/3)-angle));
end
if (region == 3)
    ta = ts*(2*ma*sin(angle)-1);
    tb = 2*ts*ma*sin((pi/3)-angle);
    tc = ts*(2-2*ma*sin((pi/3)+angle));
end
if (region == 4)
    ta = ts*(2-2*ma*sin((pi/3)+angle));
    tb = 2*ts*ma*sin(angle);
    tc = ts*(2*ma*sin((pi/3)-angle)-1);
end
```

B.4 Pulse duration

MATLAB script used for giving the right instant to give pulses for the three phases.

```
function [s1a, s2a, s1b, s2b, s1c, s2c] = fcn(region, ta, tb
    , tc, ts)
s1a = 0;
s2a = 0;
s1b = 0;
s2b = 0;
s1c = 0;
s2c = 0;
if (region == 1)
     s1a = tc/4+ta/4;
     s2a = ts/2;
     s1b = tc/4;
     s2b = ts/2-ta/4;
     s1c = 0;
     s2c= ts/2-ta/4-tc/4;
end
if (region == 2)
     s1a = tc/4+ta/4+tb/2;
     s2a = ts/2;
     s1b = tc/4;
     s2b = ts/2-ta/4;
     s1c = 0;
     s2c= tc/4+ta/4;
end
if (region == 3)
     s1a = ts/2-tc/4;
     s2a = ts/2;
     s1b = tc/4+ta/2;
     s2b = ts/2;
     s1c = 0;
     s2c= tc/4;
end
if (region == 4)
     s1a = ts/2-ta/4;
     s2a = ts/2;
     s1b = 0;
     s2b = ta/4+tb/2;
     s1c = 0;
     s2c= ta/4;
end
```

B.5 Switching realization to all sectors

MATLAB script used to for sending the signals back to its own vectors

```
function [ps1a, ps2a, ps1b, ps2b, ps1c, ps2c] = fcn(sector,
    s1a, s2a, s1b, s2b, s1c, s2c, ts)
ps1a = 0;
ps2a = 0;
ps1b = 0;
ps2b = 0;
ps1c = 0;
ps2c = 0;

if (sector == 1)
    ps1a = s1a;
    ps2a = s2a;
    ps1b = s1b;
    ps2b = s2b;
    ps1c = s1c;
    ps2c = s2c;
end
if (sector == 2)
    ps1a = ts/2-s2b;
    ps2a = ts/2-s1b;
    ps1b = ts/2-s2c;
    ps2b = ts/2-s1c;
    ps1c = ts/2-s2a;
    ps2c = ts/2-s1a;
end
if (sector == 3)
    ps1a = s1c;
    ps2a = s2c;
    ps1b = s1a;
    ps2b = s2a;
    ps1c = s1b;
    ps2c = s2b;
end
if (sector == 4)
    ps1a = ts/2-s2a;
    ps2a = ts/2-s1a;
    ps1b = ts/2-s2b;
    ps2b = ts/2-s1b;
    ps1c = ts/2-s2c;
    ps2c = ts/2-s1c;
end
if (sector == 5)
    ps1a = s1b;
```

```
43      ps2a = s2b;
44      ps1b = s1c;
45      ps2b = s2c;
46      ps1c = s1a;
47      ps2c = s2a;
48  end
49  if (sector == 6)
50      ps1a = ts/2-s2c;
51      ps2a = ts/2-s1c;
52      ps1b = ts/2-s2a;
53      ps2b = ts/2-s1a;
54      ps1c = ts/2-s2b;
55      ps2c = ts/2-s1b;
56  end
```

C

Appendix 3 - Switch models

C.1 C3M0015065D

The MOSFET datasheet considered from the Wolfspeed - C3M0015065D MOSFET and modified to operate as an equivalent power module which has been used in Case 2 has been shown below

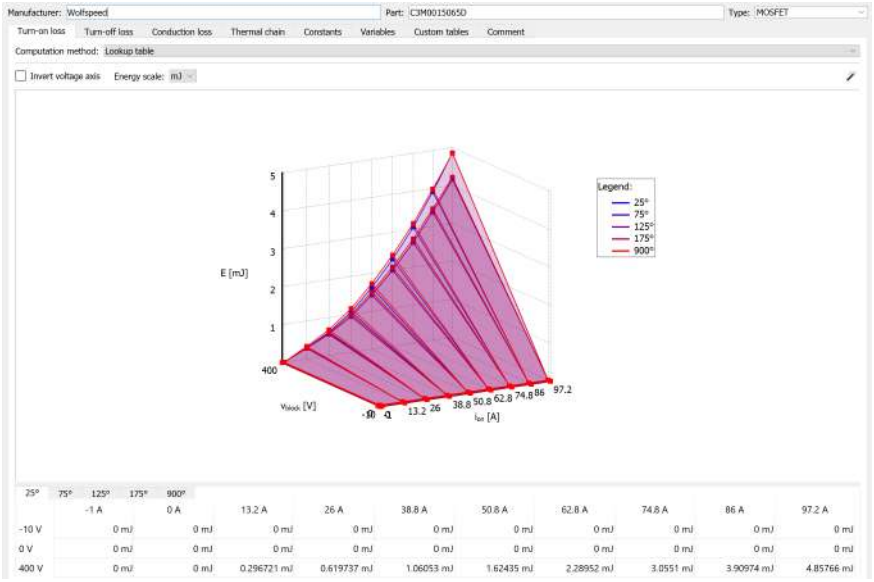


Figure C.1: Turn on losses for the modified switch used in Case 2

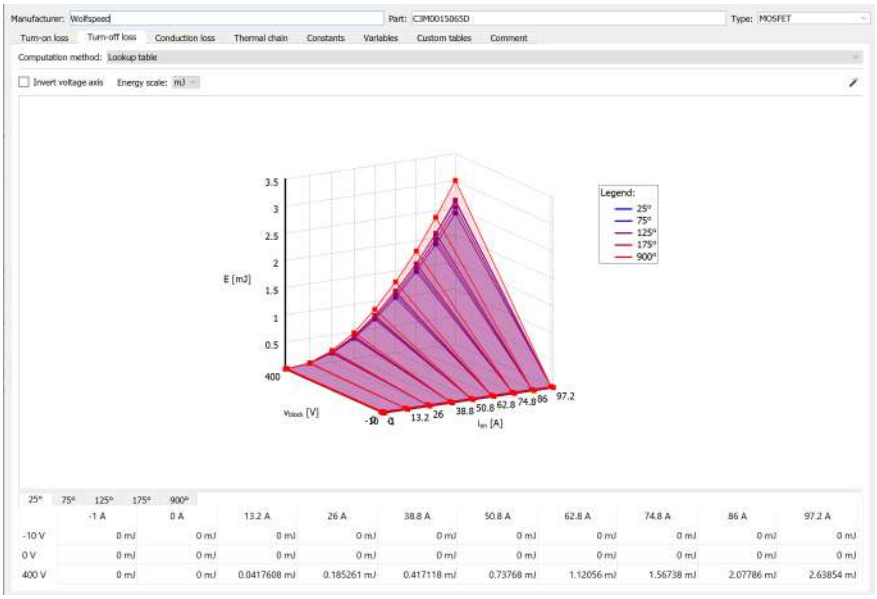


Figure C.2: Turn off losses for the modified switch used in Case 2

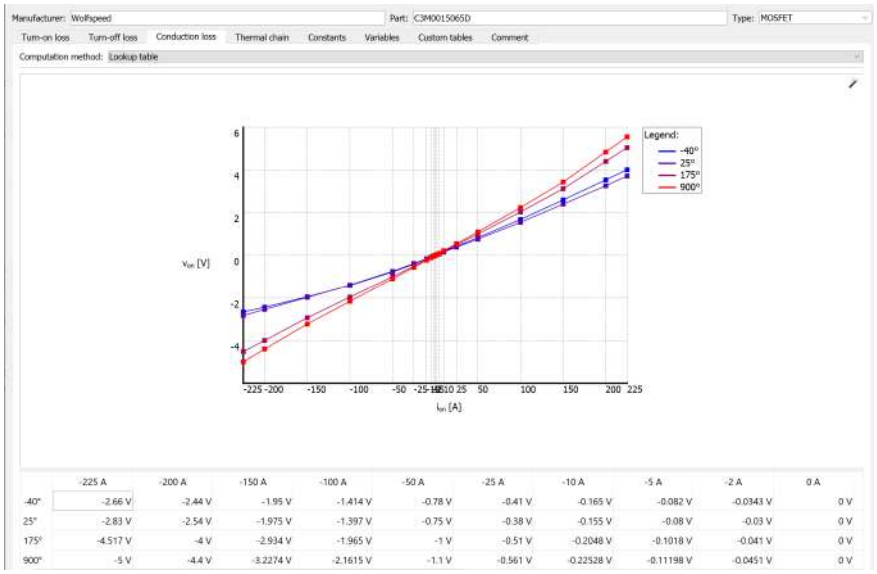


Figure C.3: Conduction losses for the modified switch used in Case 2

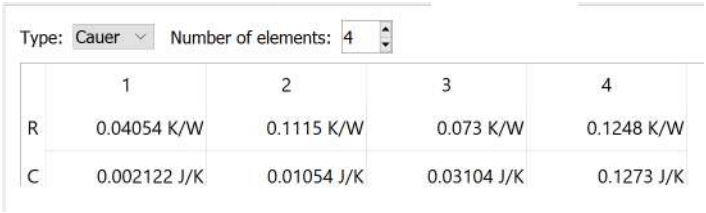


Figure C.4: Thermal network for the modified switch used in Case 2

C.2 GS-065-150

The MOSFET datasheet considered from the GaN Systems - GS-065-150 MOSFET and modified to operate as an equivalent power module which has been used in Case 3 has been shown below

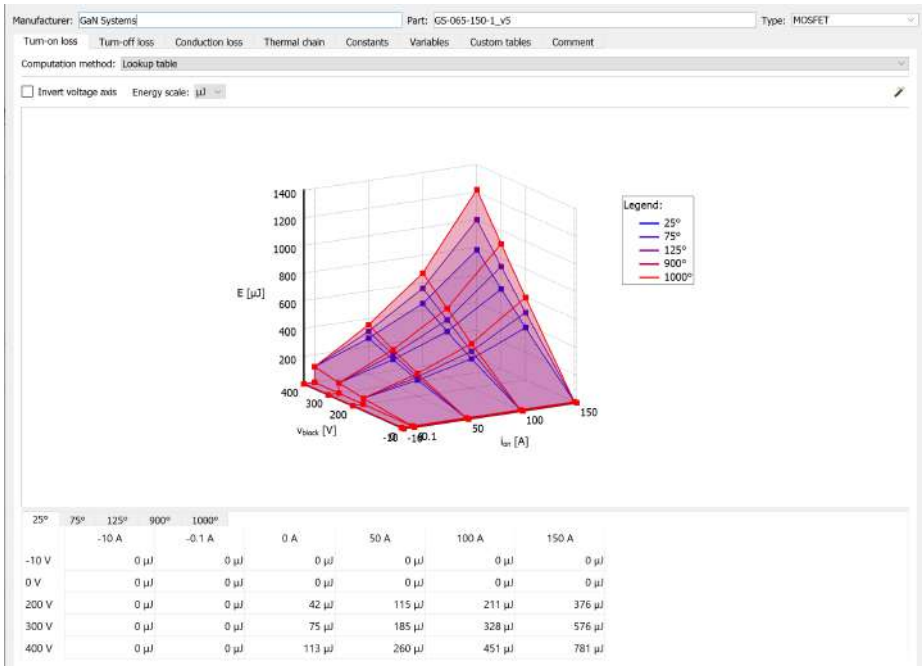


Figure C.5: Turn on losses for the modified switch used in Case 3

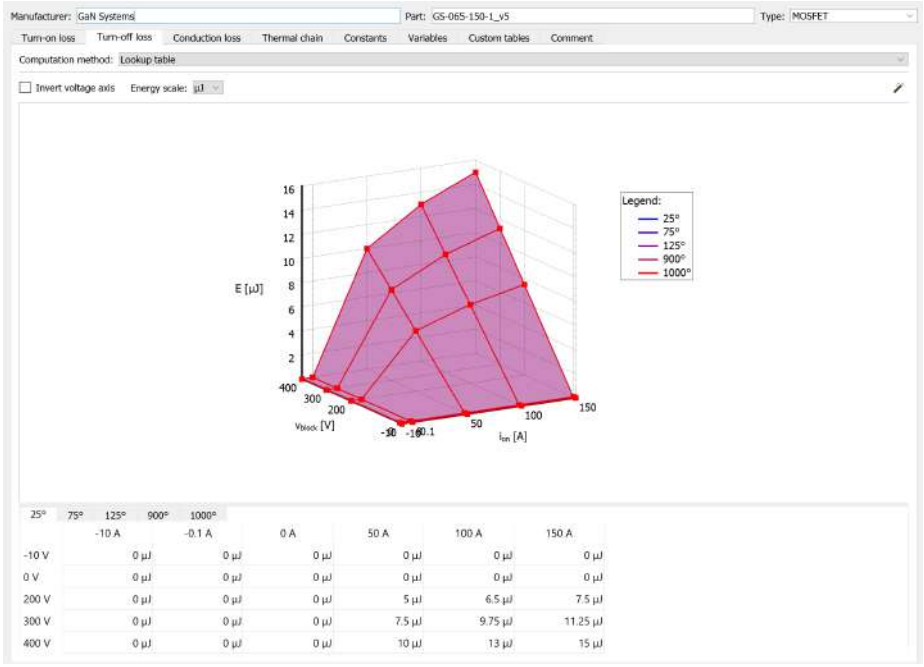
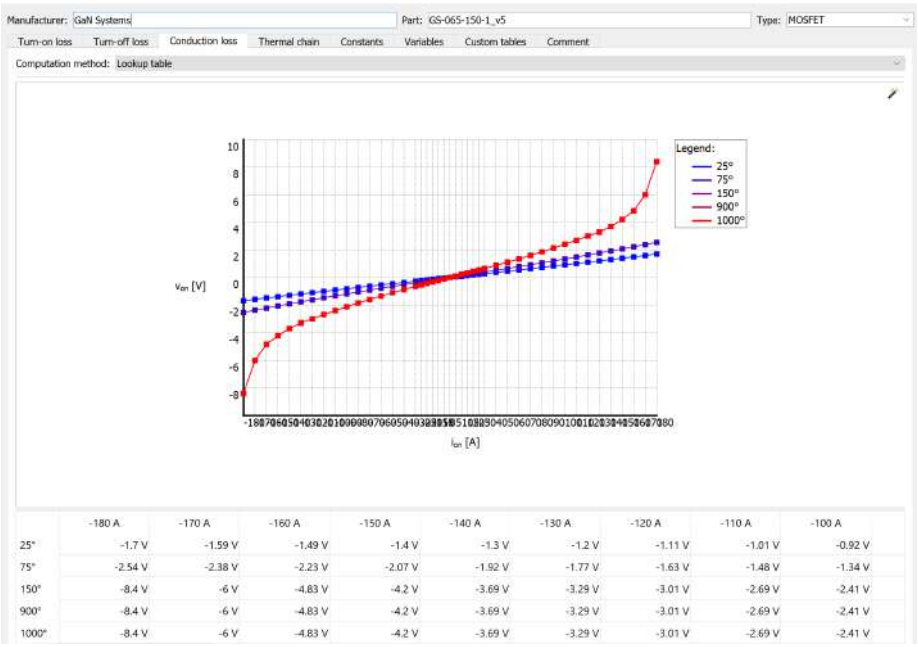


Figure C.6: Turn off losses for the modified switch used in Case 3



	-180 A	-170 A	-160 A	-150 A	-140 A	-130 A	-120 A	-110 A	-100 A
25°	-1.7 V	-1.59 V	-1.49 V	-1.4 V	-1.3 V	-1.2 V	-1.11 V	-1.01 V	-0.92 V
75°	-2.54 V	-2.38 V	-2.23 V	-2.07 V	-1.92 V	-1.77 V	-1.63 V	-1.48 V	-1.34 V
150°	-8.4 V	-6 V	-4.83 V	-4.2 V	-3.69 V	-3.29 V	-3.01 V	-2.69 V	-2.41 V
900°	-8.4 V	-6 V	-4.83 V	-4.2 V	-3.69 V	-3.29 V	-3.01 V	-2.69 V	-2.41 V
1000°	-8.4 V	-6 V	-4.83 V	-4.2 V	-3.69 V	-3.29 V	-3.01 V	-2.69 V	-2.41 V

Figure C.7: Conduction losses for the modified switch used in Case 3

Type: Cauer Number of elements: 3

	1	2	3
R	0.004 K/W	0.023 K/W	0.043 K/W
C	0.0005 J/K	0.003 J/K	0.0095 J/K

Figure C.8: Thermal network for the modified switch used in Case 3

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CHALMERS UNIVERSITY OF TECHNOLOGY
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