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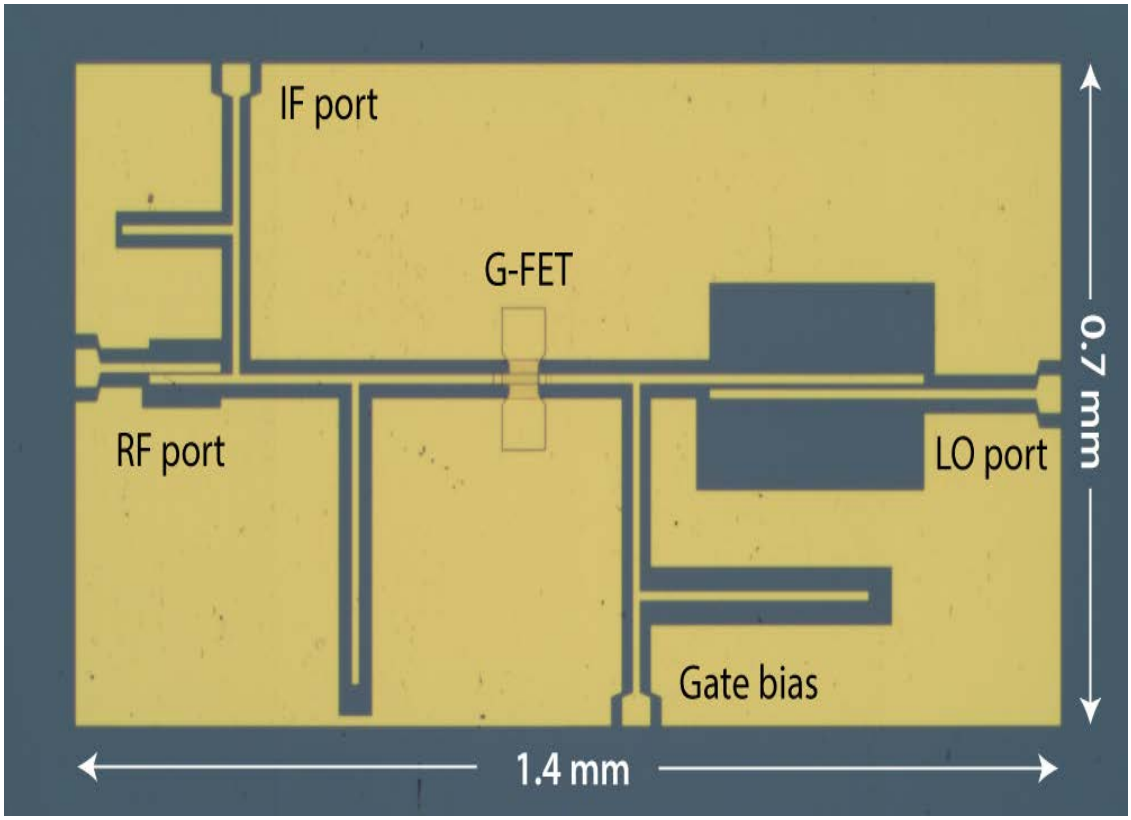

A 200 GHz Subharmonic Resistive Mixer and an IF Amplifier Based on GFETs

Master's thesis in Microtechnology and nanoscience

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Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2016

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Abstract

In recent years, graphene, a two-dimensional monolayer of carbon atoms, has rapidly attracted great attention in high-speed electronics. The promising property such as the high intrinsic carrier mobility as well as high carrier saturation velocity make graphene a potential candidate for high-speed transistors operating in the millimetre wave and the terahertz frequency ranges.

In this thesis, a 200 GHz subharmonic resistive mixer and a microwave amplifier based on graphene FET (GFET) are presented. The mixer is designed to down convert 200 GHz to 1 GHz with LO frequency of 100.5 GHz, and the amplifier is operating at 1 GHz. A large-signal GFET model is set up in a standard circuit simulator for the mixer and amplifier device optimisation as well as circuit-device integrative simulation. The device of the amplifier has a gate length 1 μm and a width $2 \cdot 120\ \mu m$, and the mixer GFET is designed as $L_g \cdot W_g = 0.5 \cdot 80\ \mu m^2$. An array of bow-tie structured graphene nanoconstructions is applied in the mixer GFET channel to obtain simultaneously a right impedance level as well as a higher current on-off ratio. Chemical vapor deposition (CVD) method is utilised for graphene preparation, and the mixer and amplifier circuit are realised in coplanar waveguide (CPW) technology on a 100 μm thick high resistive silicon substrate. A planar inductor is applied in the amplifier design for the purpose of input matching as well as circuit's integration. Metal air-bridges are added in final layout for reducing circuit discontinuities and parasitic mode propagation at the circuit T junction. Full-wave EM simulations are used for the passive circuits design. The first version of integrated receiver circuit including the designed mixer and amplifier is also fabricated.

The conversion loss (CL) of the mixer over the RF frequencies from 190 to 210 GHz is measured to be 34 dB $\pm$ 3 dB, with the minimum CL of 31.5 dB at 190 GHz and 10 dBm LO pump power. The amplifier power gain is measured to be 6 dB at 1 GHz.

Keywords: Graphene, GFETs, subharmonic resistive mixers, small-signal amplifiers, CPW technology, integrated circuits (ICs).

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Yaxin Zhang
Gothenburg, June 2016

Contents

List of Abbreviations

CH_4	Methane
CL	Conversion Loss
CNT	Carbon Nanutube
CPW	Coplanar Waveguide
DWL	Direct Laser Writer
E-beam	Electron Beam
EM	Electromagnetic
FET	Field Effect Transistor
GFET	Graphene Field Effect Transistor
HEMT	High Electron Mobility Transistor
HFET	Heterojuction FET
LNA	Low Noise Amplifiers
MESFET	Metal-semiconductor Field Effect Transistor
MISFET	Metal-insulator-semiconductor FET
MOSFET	Metal-oxide Semiconductor FET
PET	Polyethylene Terephthalate
PMMA	Poly Methyl Methacrylate A4 Resist

List of Notations

α	Lattice Constant
V_{gs}	Gate Voltage
I_{ds}	Drain-source Current
V_{ds}	Drain Voltage
g_m	Transconductance
g_d	Output Conductance
L_g	Gate Length
W_g	Gate Width
f_T	Cutoff Frequency
f_{max}	Maximum Frequency of Oscillation
C_{gs}, C_{gd}	Top Gate Capacitance
R_{ds}	Drain-source Resistance
R_{pg}, R_{pd}	Substrate Leakage Resistances
L_g, L_d, L_s	Gate, Drain, Source Inductance
R_s, R_d, R_g	Gate, Drain, Source Resistance
C_{pd}, C_{pg}	Parasitic Capacitance
n(x)	Carrier Density
v_{drift}(x)	Carrier Velocity
v_{sat}	Saturation Carrier Velocity
μ_e, μ_h	Electron and Hole Carrier Mobility
ρ_g	Resistivity of The Gate Material
$R_{contact}$	Contact Resistance
$R_{channel}$	Graphene Channel Resistance
Γ	Reflection Coefficient
Z_0	System Impedance
G_T	Transducer Gain
f_{RF}	Radio Frequency
f_{LO}	Local Oscillator Pumping Frequency
f_{IF}	Intermediate Frequency
$L_{channel}$, $W_{channel}$	Graphene Channel Length and Width

1
Introduction

In recent years, the carbon-based technology [1], has been considered as a extension of the existing silicon based technology due to it offering plenty of promising materials such as diamond, Carbon NanuTube (CNT) and two-dimensional carbon atoms sheet (graphene). Diamond, as it was commonly regarded as precious jewelries, currently is nominated as a potential candidate for high-power devices [2] for its wide band gap feature and excellent thermal conductivity [3]. CNT as well as graphene also attract great attention with their ultra-high carrier mobilities [4]. The 2D planar material, i.e., graphene, is easier to implement in the standard device process, and low contact resistance makes graphene based devices possible to connect with standard circuits. This thesis project is focusing on studying and developing of graphene based circuit utilisation in millimetre wave range.

1.1 Microwave FETs

Microwave technology have profoundly influenced our modern life. From daily wireless communication, to high-speed Internet connection, it makes our life much more convenient. Microwave Field Effect Transistor (FET) is a key component which promotes the microwave evolution tremendously. The FET principle dates back to the year of 1952 by W. Shockley [5]. However, the first version of a microwave FET was presented much later in 1967 using epitaxial GaAs Metal-Semiconductor Field Effect Transistor (MESFET) with the maximum frequency of oscillation, f_{max}, of 3 GHz [6]. After that, continuous research which was trying hard to achieve higher operating frequency and to improve the RF performance by down-scaling the transistor channel length. Nevertheless, the operating frequency of GaAs MESFETs was still limited to $f < 50$ GHz. As a consequence, applying new channel materials with high carrier mobilities and saturation velocities is required. Particularly, a great breakthrough was made by the introduction of the new type of FET named GaAs High Electron Mobility Transistor (GaAs HEMT) in 1980 [7]. This type of FETs implement 2DEG channel to separate the carriers from the impurity dopants, which enabled transistor technology towards terahertz frequency range. In the last 20 years, the InP based FET played an important role since the the InP substrate allows higher mobility channels in FET, which push the operating frequency to even higher range. Till recently, the highest report for the state-of-the-art InP HEMT gives a $f_{max} = 1.5$ THz [8] and the reported cut-off frequency (f_T) is 688 GHz [9] for In$Ga_{1-x}As_x$ mHEMTs. Nonetheless, it is difficult to make further improvement

for InP HEMTs due to the limitation of channel dimensions and channel carrier mobility. Besides, InP HEMT technology is a quite expensive and comparatively low-yield technology so that industrial mass production can not become true nowadays. Inevitably, new structures and materials need to be researched and explored.

1.2 Graphene

Previously, 2D planar low-dimensional materials were considered to be unstable for thermodynamical reason, where this concept was updated when the first graphene micromechanical cleavage from graphite was reported in 2004 [10]. For the reason of this excellent work, Andre Geim and Konstantin Noveoselov were awarded the Noble Prize in physics in 2010 jointly. After that, this two-dimensional monolayer of carbon atoms has rapidly drawn great attention and open up a continuous research both theoretically and experimentally. The exquisite electrical and mechanical characterisations such as high current density (up to 10^8 A/cm^2 [11]), high carrier mobility (top reported 2×10^5 cm^2/V·s at low temperature [12]), as well as high thermal conductivity (reported $5{\times}10^3$ W/mK [13]) make graphene a promising material for numerous applications. Currently, graphene has been researched to improve the performance of wireless high-speed communication links [14], security imaging [15], photonics and optoelectronics [16] as well as sensing [17, 18]. Moreover, graphene also expand to the new applications such as plasmonics [19, 20, 21].

1.3 Motivation

Due to the increasing requirements of high-speed wireless communication and THz sensing, improving the operation frequency and the performance of such applications have became a vital goal in today's research [22]. As mentioned in section 1.1, III-V elements based devices and circuits present superior performance compared with other type of devices and circuits. But the drawbacks of low-yield as well as high-cost limit the large scale application of such technology.
Graphene shows a plenty of outstanding characteristics, as mentioned in section 1.2. These excellent properties make graphene based devices, i.e., graphene field effect transistor (GFET) a potential solution in high-speed electronics. Apart from that, the transfer process of graphene on the silicon carrier is potentially capable to be adapted with flexible substrates, of which the GFET based applications are promise for flexible electronics. Till recently, numerous work and effort have been done for the sake of optimising the GFET performance. As a result, the highest intrinsic f_T is reported to be 427 GHz [23], but it is limited by the low carrier mobility in GFET devices. Additionally, the highest intrinsic and extrinsic f_{max} were reported only 70 GHz and 40 GHz [24], respectively. thesis value are much lower than the f_T due to lacking current saturation in GFET channel. Besides, several GFET based circuits in microwave range are also reported. With the exception of graphene based application in millimetre wave range [25, 26] and in terahertz range

(i.e., power detectors) [27, 28], graphene integrated circuits are required. Nevertheless, the operating frequency of graphene based circuit still limit below 30 GHz, as demonstrated in [29, 30]. To date, fruitful work have been done for GFET based microwave devices [31, 24] and circuits: a fundamental single-ended [32] and a double balanced [33] resistive mixer achieved with Conversion Loss (CL) of 14 dB at 2 GHz and 33 dB at 3.6 GHz respectively, but they did not utilise the inherent symmetry of GFET channel conductance. Therefore, two subharmonic resistive GFET mixers have been presented with 22 dB and 19 dB CL at 2-5 GHz and 24-31 GHz [30, 34], respectively. As shown above, the operating frequency is far away from the anticipated values. Hence, enhancing the operating frequency and performance of the GFETs based circuits towards integrated circuits are vital for realisation of potentiality of graphene.

In this thesis, GFETs based applications including a 200 GHz subharmonic resistive mixer and a 1 GHz small-signal amplifier are presented. This mixer is aiming at down converting signal from 200 GHz band to 1 GHz and the amplifier is designed to operate at 1 GHz. Device modelling, amplifier and mixer relevant circuit design as well as device and circuit fabrication are included in this work. The first version of integrated receiver including the designed mixer and amplifier are also fabricated.

1.4 Thesis outline

To begin with, this thesis introduces the background knowledge including graphene properties and GFET modelling in chapter 2. GFET based circuit design, i.e., a subharmonic resistive mixer and a small- signal amplifier, is described in chapter 3. Additionally, the fabrication techniques is presented in chapter 4. Furthermore, the circuit characterisation as well as discussion is exhibited in chapter 5. Finally, the conclusion and future work discussion are shown in chapter 6.

2

Theory of graphene and GFET

In this chapter, graphene and GFETs based theory are introduced. To start with, the graphene properties is presented. Then, the GFET characterisation, which consists of DC and microwave performance is described. Finally, the GFET structure and modelling including general layout of GFET, small and large signal modelling are demonstrated.

2.1 Graphene properties

2.1.1 Graphene band structure

Graphene is a single 2D layer of carbon atoms of which the thickness d is $\simeq 0.3$ nm only. Each carbon atom owns three neighbours, by which they are bonding with each other utilising very strong covalent. These bounding generates a dense hexagonal honeycomb lattice with lattice constant, $\alpha = 1.42$ Å, as shown in Fig 2.1a. Graphene full band structure is demonstrated in Fig.2.1b [35], which can be found by solving the Dirac equation. As can be seen, the conduction and the valence band meet each other at on single point with the charge neutrality, which we call Dirac points in the Brillouin zone. Because of this unique property, graphene becomes a zero bandgap semiconductor (semi-metal) and consequently, no mass of carriers at the position nearby Dirac point.

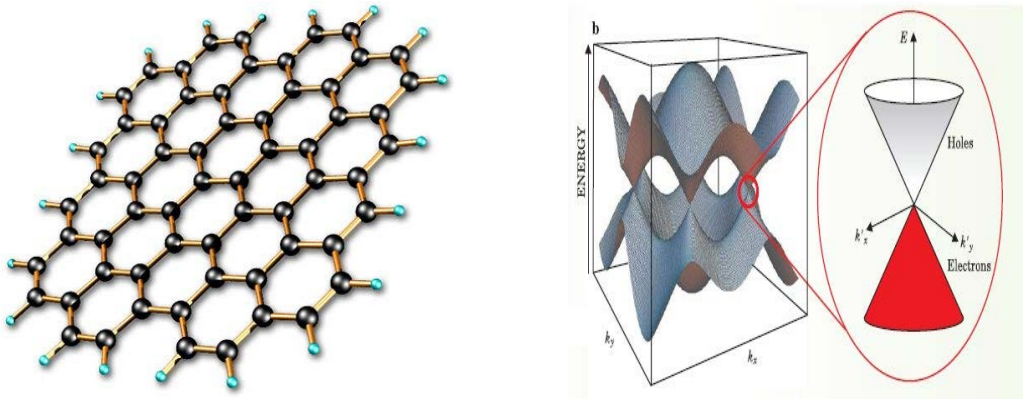

Figure 2.1: a) Graphene lattice structure b) Graphene full-band structure [35].

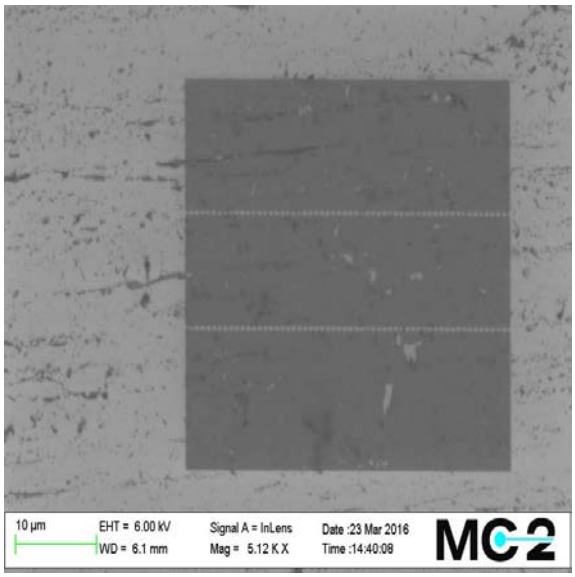

Figure 2.2: The SEM photo of nanoconstriction graphene channel.

2.1.2 Nanoconstrictions

Aiming at applying GFET based devices in high frequency range, setting up a bandgap in graphene channel is desirable. There are three main methods towards opening graphene bandgap nowadays. One is done by lateral confinement of graphene width in nanoribbon [36], then by implementing nano-constrictions into graphene channel [37], and the third one is by applying perpendicular electric field in bilayer graphene [38]. Compared with the other two mathods, the bilayer technology gives the best result in opening graphene bandgap (up to 0.25 eV at room temperature) [39]. Nevertheless, due to the instability of bilayer graphene in fabrication, the ratio of monolayer, bilayer even three layer within graphene sheet is quite hard to control. Hence, although the bilayer graphene technology enables tunable graphene bandgap, it still far away from materials level to the device level. As for rest of two methods, we prefer nanoconstriction in stead of nanoribbon because nanoconstriction builds up bandgap more efficiently. For the 20 nm nanoconstriction, 130 meV bandgap is achieved, where only about half value can be obtained by the same dimension nanoribbon [36, 37]. Apart from that, a high on-off ratio can be obeained by creating nanoconstrictions within graphene channel. This is beneficial also to subharmonic resistive mixer property. A SEM photo for nanoconstrictions in graphene channel is shown in Fig.2.2, and more details will be discussed in the next chapter.

2.2 GFET characteristics

2.2.1 Field effect transistors

FETs, as an active and nonlinear device, plays a significant role in the field of electronics. The principle of the FETs is to generate a capacitance between two

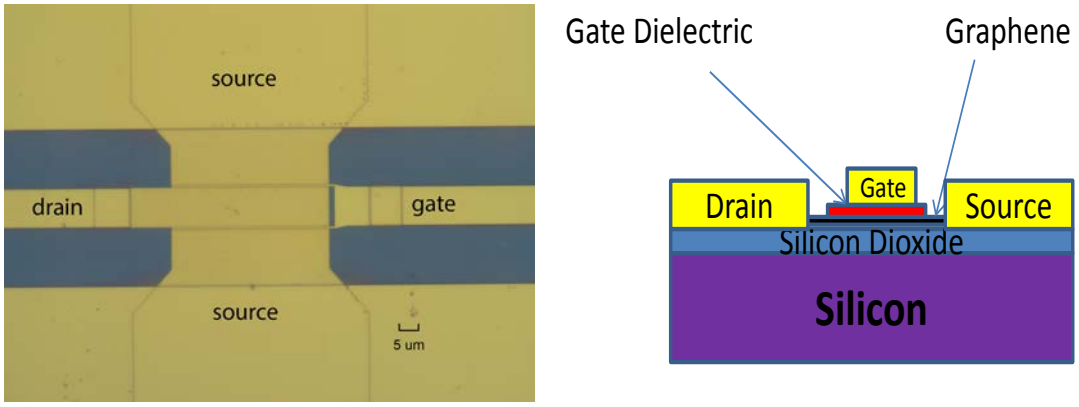

Figure 2.3: a) A three terminals GFET image b) the structure of GFET on silicon substrate.

electrodes (i.e., drain and source). By applying an electric field, the carrier density of the cross section area of the channel is controlled [5]. According to the different gate capacitor structures, we can separate FETs into three groups. One way is to from gate capacitor by insulating gate, which can be achieved either by injecting a dielectric layer in a Metal-Oxide Semiconductor FET (MOSFET) and Metal-Insulator-Semiconductor FET (MISFET), or by a large bandgap semiconductor layer in a Heterojuction FET (HFET) [7]. The second way is utilising a Schottky barrier, for instance, Metal Semiconductor FET (MESFET), and the remaining one is done by depletion layer of a p-n junction, i.e., junction FET. Principally, there are two different types of carrier drifting in FET channel, namely electron and hole, by which we named the channel "n-type channel" or "p-type channel". For high frequency applications, n-type channel FETs are more compact because electron mobility usually superior than that of hole. The GFET is a kind of MOSFETs, and it can be regarded as either n-type or p-type FET which depend on the gate bias voltage because of the electron-hole duality in graphene. Fig 2.3a shows an 3 terminals GFET image, and the cross sectional structure layout is demonstrated in Fig 2.3b.

2.2.2 DC characteristics

Understanding the GFET DC characteristics is the first step to indicate GFET high frequency performance. The DC characteristics of a GFET is consist of two figure-of-merits. One is the drain current I_{ds} versus gate voltage V_{gs}, which is called the transfer characteristic. The other is the drain current I_{ds} versus drain voltage V_{ds}, which we name it output characteristic respectively. There are two significant parameters that can be deduced from DC characteristics, one is the transconductance g_m, and the other is output conductance g_d. The g_m represents the channel current

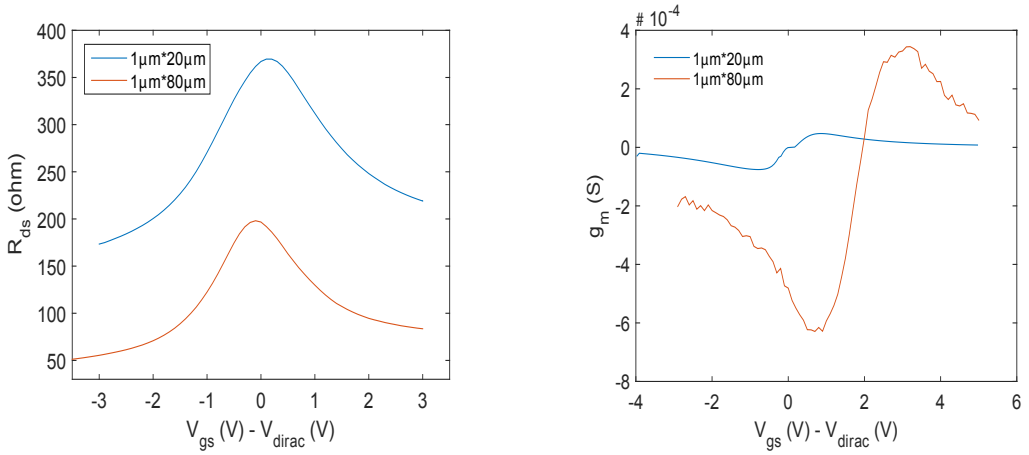

Figure 2.4: measured a) R_{ds} vs V_{gs}, b) g_m vs V_{gs} at $V_{ds} = 0.1$ V for devices with $L_g \times W_g = 1\times\ 20\ \mu m^2$ and $1\times\ 80\ \mu m^2$.

controlling capability of the gate voltage, which is shown as,

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}|_{V_{ds=const}}. \tag{2.1}$$

The g_d describes the differential of the output resistance of the transistor, of which the expression is,

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}}|_{V_{gs=const}}. \tag{2.2}$$

Here, both g_m and g_d are the extrinsic value and the parasitic effect is contained. In high frequency applications, a high transconductance of GFET is required. Generally, GFETs present high contact and access resistances because of the contact effect between graphene and other metals. Therefore considerable difference make it necessary to distinguish the intrinsic and extrinsic g_m and g_d. The extraction method of $g_{m,in}$ and $g_{d,in}$ is obtained in [40] using extrinsic values,

$$g_{m,in} = \frac{g_{m,ex}}{1 - R_s g_{m,ex}((R_s + R_d)g_{d,ex}) - (R_s + R_d)g_{d,ex}} \tag{2.3a}$$

$$g_{d,in} = \frac{g_{d,ex}}{1 - R_s g_{d,ex}((R_s + R_d)g_{m,ex}) - (R_s + R_d)g_{m,ex}}. \tag{2.3b}$$

2.2.3 Microwave characteristics

After analysing DC characteristics of GFETs, we are now focusing on GFET microwave characteristics. Cutoff frequency, f_T, as well as maximum frequency of oscillation, f_{max}, are two important figures-of-merits which demonstrate the high frequency performance and the upper frequency limitation of FETs. The f_T is defined as the frequency that the transistor's current gain drops to unity. An analytical expression for f_T is described as,

$$f_T = \frac{g_{m,in}}{2\pi((C_{gs} + C_{gd})(1 + g_{d,in}(R_d + R_s)) + C_{gd}g_{m,in}(R_d + R_s) + C_{pg})}. \tag{2.4}$$

The f_{max} is the maximum frequency when the power gain of the device reduce to 1. The relation between f_{max} and f_T is shown as,

$$f_{max} = \frac{f_T}{2\sqrt{g_{d,in}(R_g + R_s + R_i) + 2\pi R_g C_{gd} f_T}}. \tag{2.5}$$

As the equation shown above, we can easily deduce that enlarging the g_m as well as reducing the gate capacitance C_g are two main ways to improve the device high frequency performance. The g_m can be increased by down scaling the drain-source resistance R_{ds}. The R_{ds} consists of a channel resistance, which mainly determined by mobility, and a contact resistance respectively. The mobility, however, is influenced only by the material type and the preparation method, which can not be improved much by optimising device dimension. Hence, achieving lower contact resistance is another option for higher g_m. Measured results of R_{ds} versus V_{gs} and g_m versus V_{gs} at $V_{ds} = 0.1$ V for GFET devices with $L_g \times W_g = 1 \times 20\ \mu m^2$ and $1\times 80\ \mu m^2$ are shown in Fig 2.4a and Fig 2.4b respectively. As can be seen, the wider device with $L_g \times W_g = 1\times 20\ \mu m^2$ shows a g_m of 0.6 mS, where the narrower device with $L_g \times W_g = 1\times 80\ \mu m^2$ only offers 1/10 of the first value. This is mainly due to the difference of contact area. On the other hand, parasitic capacitance effect as well as gate capacitance increase dramatically when extending the device dimension, which generate a trade-off in high frequency device analysis. Therefore, the optimisation of device dimension by setting up a accurate device model is necessary.

2.3 GFET modelling

2.3.1 Small-signal GFET model

Despite that the device model is normally valid under certain assumptions and limitations, an accurate device modelling enables better device optimisation, circuit design and performance estimation. Physical modelling and empirical modelling are two main ways to model a device. The physical modelling is to define devices by physical geometry and semiconductor properties, which is often used in optimising devices and understanding of the device behaviors. Several physical models for GFET have been demonstrated [41, 42, 43, 44], yet they are too complicated to use in circuits design. The empirical modelling, however, is built up by extracting parameters and algebraic relations from electrical measurements. Due to the limited physical knowledge required, empirical modelling is usually implement in circuit simulations. Besides, acceptable accuracy and fast calculation speed make empirical model easier to apply in standard circuit simulator tools, for example Agilent ADS, etc. In our case, a reliable empirical GFET model need to be applied both for amplifier and mixer circuit design.

Small-signal GFET model is the first step towards the entire GFET modelling. This type of model is valid when the low RF power can not modulate the quiescent point, especially in the case of Low Noise Amplifiers (LNA) and small-signal amplifiers.

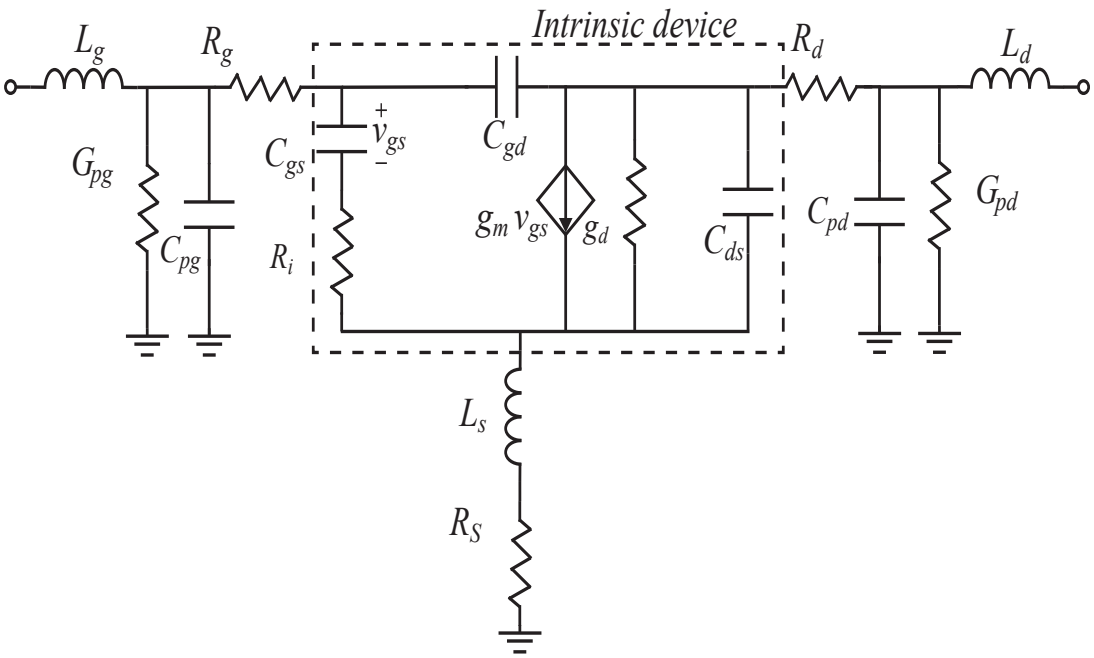

Figure 2.5: Small-signal GFET equivalent circuit.

Fig 2.5 demonstrates the equivalent circuit of a small-signal GFET. As shown above, the equivalent circuit is quite similar to the standard FET small-signal equivalent circuit. However, the substrate leakage conductances G_{pg} and G_{pd} through gate and drain pads, which are generally neglected in GaAs and InP technologies but could appear when the silicon substrate insulation is insufficient. We can separate the equivalent circuit in two parts, namely the intrinsic and extrinsic circuit. The intrinsic circuit, which is marked by a dashed block, includes g_m, g_d, top gate capacitance C_{gs} and C_{gd}, drain source capacitance C_{ds}, channel resistance R_i, and τ. Where the extrinsic part, which is independent of the biasing conditions, consist of inductance L_g, L_d, L_s and resistance R_s, R_d, R_g of gate drain and source terminals, and parasitic capacitance C_{pd}, C_{pg} respectively.

The core part of the intrinsic circuit is the voltage-controlled current source current $g_m \cdot V_{gs}$, which can be defined in current linearisation around the bias,

$$I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{Ggs,DC}, V_{gs,DC}) + \frac{\partial I_{ds}}{\partial V_{gs}} \triangle V_{gs} + \frac{\partial I_{ds}}{\partial V_{ds}} \triangle V_{ds} \tag{2.6}$$

where the differential of drain to source current and gate to source voltage $\frac{\partial I_{ds}}{\partial V_{gs}}$ represent g_m and the differential of drain to source current and drain to source voltage is the g_d. According to the theory [45, 46], the Y matrix of the intrinsic circuit can be easily characterised because the intrinsic device exhibits a PI topology,

which are,

$$y_{11} = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega(\frac{C_{gs}}{D} + C_{gd}) \tag{2.7a}$$

$$y_{12} = -j\omega C_{gd} \tag{2.7b}$$

$$y_{21} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} \tag{2.7c}$$

$$y_{22} = \frac{1}{R_{ds}} + j\omega(C_{ds} + C_{gd}) \tag{2.7d}$$

$$D = 1 + \omega^2 C_{gs}^2 R_i^2. \tag{2.7e}$$

After understanding the Y-matrix of the intrinsic circuit, the following work is to extract each intrinsic element form the Y matrix, through Berroth's work [47],

$$C_{gd} = \frac{-Im(Y_{12})}{\omega}, \tag{2.8a}$$

$$C_{gs} = \frac{Im(Y_{11}) - \omega C_{gd}}{\omega}(1 + \frac{Re(Y_{11})^2}{(Im(Y_{11}) - \omega C_{gd})^2}) \tag{2.8b}$$

$$R_i = \frac{Re(Y_{11})}{(Im(Y_{11}) - \omega C_{gd})^2 + Re(Y_{11})^2} \tag{2.8c}$$

$$g_m = \sqrt{((Re(Y_{11}))^2 + (Im(Y_{21}) + \omega C_{gd})^2)(1 + \omega^2 C_{gs}^2 R_i^2)} \tag{2.8d}$$

$$\tau = \frac{1}{\omega} arcsin(\frac{-\omega C_{gd} - Im(Y_{21}) - \omega C_{gs} R_i Re(Y_{21})}{g_m}) \tag{2.8e}$$

$$C_{ds} = \frac{Im(Y_{22}) - \omega C_{gd}}{\omega} \tag{2.8f}$$

$$g_d = Re(Y_{22}) = \frac{1}{R_{ds}}. \tag{2.8g}$$

Here, C_{gs} and C_{gd} above is influenced by parasitic effect, i.e., C_{pg} and C_{pd}. In order to extract this two parasitic parameters, an method based on pinch-off measurement will be introduced later in section 2.3.3.

2.3.2 Large-signal GFET model

As discussed before, the small-signal GFET model will be no longer valid if the RF power is large enough to influence the quiescent point. In many applications, such as mixers and power amplifiers, a large input RF power is required to pump the device so that the quiscent point will be modulated in a large operating range. Therefore, a GFET large-signal model should be built up for GFET based mixer design. Traditional empirical FET models was tried to represent GFETs, such as [48, 49]. However, because of the zero bandgap property and electron-hole duality performance, it could not realised. Till recently, many works were presented to develop an large-signal GFET model. By utilising the semi-empirical square-root charge-voltage relation, some models are reported in [50, 51], by which the I-V curve characterisation of GFET can be estimated. The latest work which done by Habibpour et al.[52] improved GFET modelling by implementing different carrier

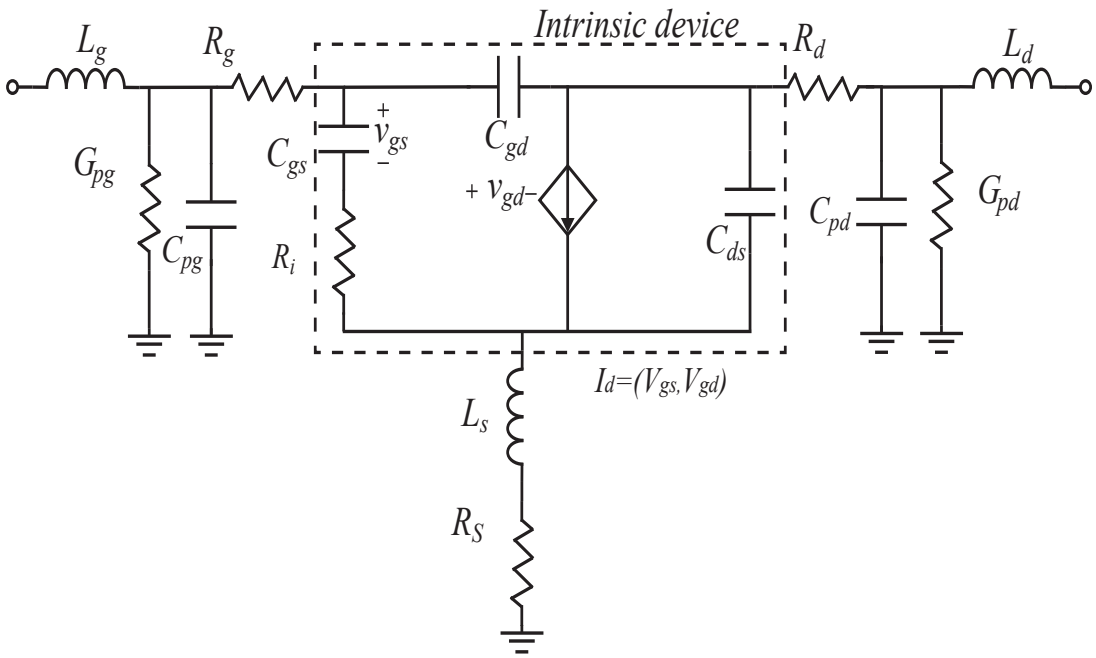

Figure 2.6: Large-signal GFET equivalent circuit.

mobilities for electrons and holes in current function and taking channel carrier type dependance for contact resistance into consideration [53]. For these achievements, the electron-hole duality of GFETs [54] can be accurately estimated. Our large signal GFET modelling work are follows Habibpour's method.

Fig 2.6 describes the equivalent circuit of large-signal GFET. Instead of using an a first-order voltage controlled current source, an drain current expression, I_{ds} as a function of the two bias voltages V_{gs} and V_{gd}, was implemented to show bias dependence in a large sweeping range. Besides, carrier type can also be determined by V_{gs} and V_{gd}. The extrinsic part remains the same due to its independence of the operation point.

According to [52], the current within the channel can be described by,

$$I_{ds} = q\frac{W}{L} \int_0^L n(x) v_{drift}(x) dx \tag{2.9}$$

of which the n(x) is the carrier density , v_{drift}(x) is the carrier velocity, L and W represent the channel length and width respectively. Then the carrier density n(x) can be expressed as,

$$n(x) = \sqrt{n_0^2 + \left(\frac{C \times V(x)}{q}\right)^2} \tag{2.10}$$

where the C is the top gate capacitance per area calculated by C = $(C_{gs} + C_{gd})$/LW, and n_0 is the residual carrier density. Furthermore, velocity saturation model [55]

shows the carrier drift velocity v_{drift} as,

$$v_{drift}(x) = \frac{\mu E(x)}{\sqrt[m]{1 + (\frac{\mu|E(x)|}{v_{sat}})^m}} \tag{2.11a}$$

$$v_{sat} = v_F\beta/\sqrt{n}. \tag{2.11b}$$

Here, v_{sat} is saturation carrier velocity, m is fitting parameter (usually 1), $v_F = 10^8$ cm/s, $\beta = 4 \times 10^5\ cm^{-1}$ for graphene on SiO_2 and μ is carrier mobility of which we assumed as a constant for electrons μ_e and holes μ_h respectively.

As discussed above, graphene have electrons-hole duality performance, therefore the drain-source current I_{ds} can be separated into four quadrant of $V_{gs} - V_{gd}$ plane according to different charge types, as shown below [52]: For the first quadrant ($V_{gs} > 0$, $V_{gd} > 0$), both carriers are electrons,

$$I_{ds1} = \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + (\frac{\mu_e|V_{gs}-V_{gd}|}{L\overline{v}_{sat}})}} \frac{W}{L} \overline{f}(\overline{V}_{gs}, \overline{V}_{gd}). \tag{2.12}$$

of which,

$$Q_0 = q \times n_0 \tag{2.13a}$$

$$V_0 = Q_0/C \tag{2.13b}$$

$$\overline{V}_{gs} = V_{gs}/V_0 \tag{2.13c}$$

$$\overline{V}_{ds} = V_{gd}/V_0 \tag{2.13d}$$

$$\overline{v}_{sat} = v_F\beta/\sqrt[4]{n_0^2 + (C(V_{gs} + V_{gd})/2q)^2}. \tag{2.13e}$$

Besides,

$$f(x,y) = \frac{1}{2}(x\sqrt{1+x^2} - y\sqrt{1+y^2}) + \frac{1}{2}(ln(x + \sqrt{1+x^2})) - ln(y + \sqrt{1+y^2}). \tag{2.14}$$

Similarly, for the second quadrant ($V_{gs} > 0$, $V_{gd} < 0$), electrons dominates near source but holes dominates the drain,

$$\begin{aligned} I_{ds2} =& \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + (\frac{\mu_e|V_{gs}-V_{gd}|}{L\overline{v}_{sat}})}} \frac{W}{L} \overline{f}(\overline{V}_{gs}, 0) \\ &+ \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + (\frac{\mu_h|V_{gs}-V_{gd}|}{L\overline{v}_{sat}})}} \frac{W}{L} \overline{f}(0, \overline{V}_{gd}) \end{aligned} \tag{2.15}$$

For the third quadrant ($V_{gs} < 0$, $V_{gd} > 0$), same procedure as before but holes dominates near source and electrons dominates the drain,

$$\begin{aligned} I_{ds3} =& \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + (\frac{\mu_h|V_{gs}-V_{gd}|}{L\overline{v}_{sat}})}} \frac{W}{L} \overline{f}(\overline{V}_{gs}, 0) \\ &+ \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + (\frac{\mu_e|V_{gs}-V_{gd}|}{L\overline{v}_{sat}})}} \frac{W}{L} \overline{f}(0, \overline{V}_{gd}) \end{aligned} \tag{2.16}$$

Finally comes to the last quadrant ($V_{gs} < 0$, $V_{gd} > 0$), where the holes becomes the major carrier at both source and drain part,

$$I_{ds4} = \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + (\frac{\mu_h |V_{gs} - V_{gd}|}{L \overline{v}_{sat}})}} \frac{W}{L} \overline{f}(\overline{V}_{gs}, \overline{V}_{gd}) \tag{2.17}$$

By combining these equations using steps function, all different bias situations are included so that large signal modelling is generated.

Furthermore, due to the p-n barrier difference caused by deposited metal effect [56], the DC characteristic of GFET is not perfectly symmetrical. In order to take this phenomena into account , an extra resistance is necessary to be added into the large signal GFET model [52],

$$\begin{aligned} R_{ext}(V_{gs}, V_{gd}) = & \frac{1 + tanh(V_{gs}/V_2)}{2} \\ & \frac{1 + tanh(V_{gd}/V_2)}{2} \times R_{exto}. \end{aligned} \tag{2.18}$$

Here, V_2 is the fitting factor. When electrons become the majority carriers in GFET channel, an extra resistance R_{exto} affect in the drain to source resistance R_{ds}. After adding this extra resistance, the imperfect property in drain-source resistance measurement is will fitted.

2.3.3 Parameter extraction and de-embedding

After setting up a device model, each element in the equivalent circuit need to be extracted and all parameters can be extracted from DC and S-parameters measurements respectively. To begin with, forward biased (short) and pinch-off (open) method are applied for parasitic elements extraction of $L_s, L_g, L_s, R_{pg}, R_{pd}, C_{pg}$, and C_{pd} [45, 57]. Because of the zero bandgap property, graphene channel within GFET can not be turn on /off completely. Therefore the S-parameter measurement data for open and short structure devices with identical layout are utilised instead. Fig 2.7a and b describe the open and short structure of GFET equivalent circuits. Parasitic inductances can be obtained according to the method proposed by Tayrani et al.[57], after S-parameter transferring to Z matrix,

$$L_s = Im(Z_{12,short})/\omega \tag{2.19a}$$

$$L_d = Im(Z_{22,short})/\omega - L_s \tag{2.19b}$$

$$L_g = \frac{\omega_x Im(Z_{11,short,x}) - \omega_y Im(Z_{11,short,y}) - (\omega_x^2 - \omega_y^2) L_s}{\omega_x^2 - \omega_y^2}. \tag{2.19c}$$

The x and y represent two different frequency points. Consequently, parasitic capacitances can be extracted from pinch-off measurements. At low frequency range, parasitic resistances and inductances are neglected. Expressions of each element of

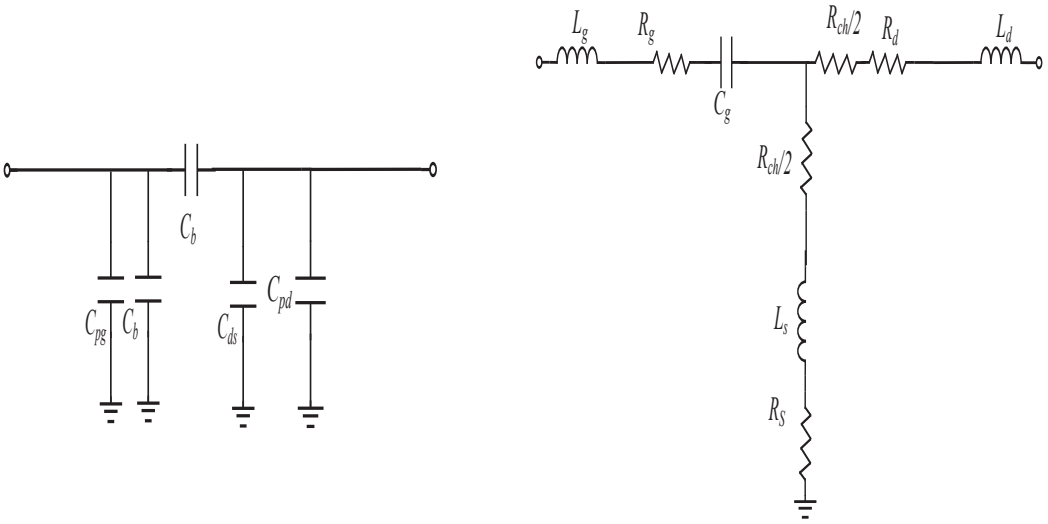

Figure 2.7: (a) Open and (b) short structure of GFET equivalent circuit.

Y parameters are shown below,

$$Y_{11} = j\omega(C_{pg} + 2C_b) \tag{2.20a}$$

$$Y_{12} = -j\omega C_b = Y_{21} \tag{2.20b}$$

$$Y_{22} = j\omega(C_{ds} + C_b + C_{pd}). \tag{2.20c}$$

Here, we can assume the value of C_{pg} is equal to C_{pd} because of the symmetric layout of GFET pads. Simultaneously, parasitic resistances can be taken from the real part of Y parameters,

$$R_{pg} = \frac{1}{Re(Y_{11}, open)} \tag{2.21a}$$

$$R_{pd} = \frac{1}{Re(Y_{22}, open)}. \tag{2.21b}$$

Generally, the gate is designed as a rectangular gate, and the gate ohmic resistance can be calculated by standard rectangular resistance formula,

$$R_g = \rho_g \frac{W}{3Lh}. \tag{2.22}$$

The h, W, L and ρ_g are the height, width, length, and the resistivity of the gate material respectively. The equation is divided by the factor of 3 because of the current distribution phenomena in multi-finger gate of the GFET.
The following step is the extraction of R_d and R_s. Here, we utilise an drain-source resistance R_{ds} model which introduced by Seyoung et al. [58],

$$R_{ds} = R_{contact} + R_{channel}, \tag{2.23a}$$

$$R_{channel} = \frac{N_{sq}}{n_{tot} e\mu} = \frac{N_{sq}}{\sqrt{n_0^2 + n[V_{gs}^*]^2} e\mu}, \tag{2.23b}$$

$$V_{gs}^* = V_{gs} - V_{gs,Dirac} = \frac{e}{C_{ox}} n + \frac{h v_F \sqrt{\pi n}}{e}, \tag{2.23c}$$

where N_{sq} represents the number of squares of the top gate area, $R_{contact}$ is the contact resistance and $R_{channel}$ is the graphene channel resistance covered by top gate electrode. By fitting R_{ds} model with the measured data, relevant elements, n_0, carrier mobility μ_e, μ_h, and $R_{contact}$ can be extracted. Now, all extrinsic elements are able to be extracted. Finally, by de-embedding the extrinsic elements, the intrinsic Y matrix can be obtained and the intrinsic element can be extracted by Eq. 2.8. After all extrinsic as well as intrinsic parameters extraction, this large signal model are available to implement in EDA tools for GFET circuits design.

3

Design of GFET based circuits

In this chapter, GFET based circuits design including a small-signal IF amplifier and a 200 GHz subharmonic resistive mixer are demonstrated.

3.1 Small-signal amplifiers

Small-signal amplifiers is a key part in microwave receivers. This type of component enables energy amplification from input to output signal by utilising current control effect of transistors. Generally, the signal becomes weak after received from antenna and down converted by mixer. Hence, amplifiers are usually implemented after down converting mixer in a receiver to strengthen the signal. Therefore, the realisation of GFET amplifier is a prerequisite in order to achieve an receiver.

3.1.1 Device design

Fig 3.1 shows a block diagram of an amplifier. A complete amplifier network consist of three parts, namely input matching circuit, transistor, and output matching circuit. Γ is the reflection coefficient and Z_0 is the system impedance which is usually set as 50 Ohm. Generally, transducer gain G_T is used to describe amplification capability, which expressed as,

$$G_T = \frac{P_{Load}}{P_{av}} = \frac{(1-|\Gamma_S|^2)}{|1-\Gamma_{IN}\Gamma_S|^2}|S_{21}|^2\frac{(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2}. \tag{3.1}$$

In common cases, S_{12} is small so that we can simplify the gain expression by assuming $S_{12} = 0$. In this case, $\Gamma_{IN} = S_{11}$, $\Gamma_{OUT} = S_{22}$, and the transducer gain can be simplified as,

$$G_{TU} = \frac{(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2}. \tag{3.2}$$

As shown in the equation, both good matching network design and device optimisation are essential in order to achieve better amplification. To begin with, let's concentrate on device optimisation. S_{21} determines the amplification ability of a devices, which rolls of with frequency as,

$$S_{21} = \frac{2Z_0 g_{m,ex}}{1+Z_0 g_{d,ex}} \times \frac{1}{1+j\omega C_{gs} Z_0}. \tag{3.3}$$

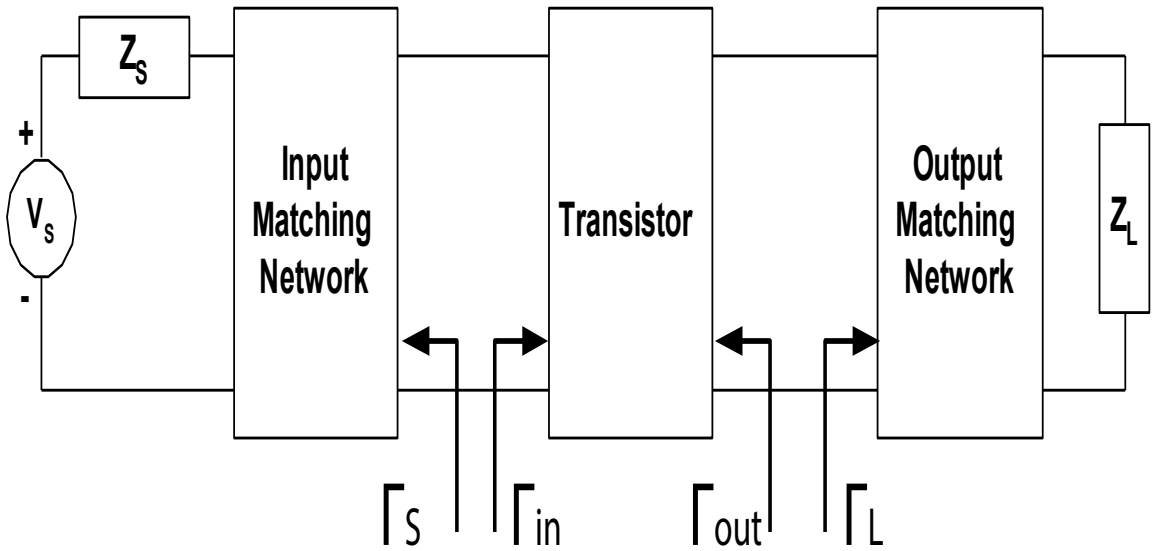

Figure 3.1: Transistor amplifier diagram.

For 1 GHz case, $\omega \cdot C_{gs}$ still keeps in a low value, and the expression of S_{21} can be simplified by assuming $\omega \cdot C_{gs} \approx 0$,

$$|S_{21}| = \frac{2Z_0 g_m}{1 + Z_0 g_d}. \tag{3.4}$$

When $|S_{21}|^2 > 1$, the device itself will present a power gain without any matching networking cascaded ($\Gamma_L = \Gamma_s = 0$). Undeniably, the higher S_{21} we achieve, the larger power gain we will be obtained. Till recently, long gate length GFETs presents a higher $g_{m,ex}$ than that of short gate length devices [59]. Reducing the contact resistance and access resistance are also benefit to scaling up g_m [60]. Besides, the high quality graphene ensures the high carrier mobility and a higher g_m also can be achieved. By implementing the device model described in chapter 2 into EDA tools and do comparison with measurement results of groups of devices, the relationship between dimensions and device performances can be well estimated.

Fig 3.2a demonstrates the measured R_{ds} as well as g_m versus gate width sweeping from 60 μm to 240 μm, and Fig 3.2b exhibits $|S_{21}|$ versus gate width. As can be seen, wider devices give a higher g_m and higher $|S_{21}|$, which ensures a better self-amplification capability of the GFET. Hence, choosing device with a large dimension is beneficial in GFET amplifier design.

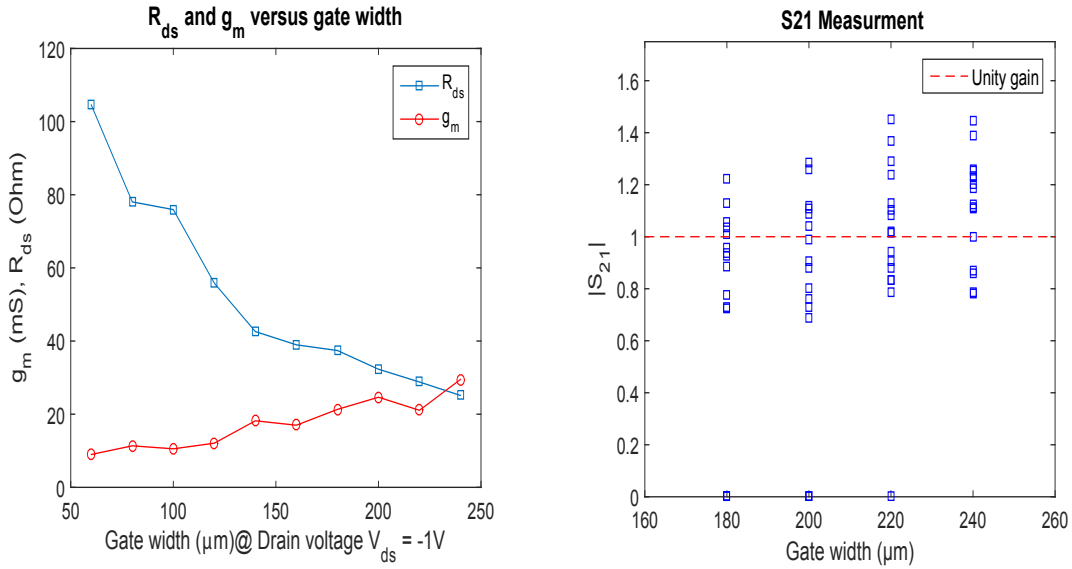

Figure 3.2: a) R_{ds} and g_m versus gate width, b) $|S_{21}|$ versus gate width @ $L_g = 1$ μm.

3.1.2 Circuit design

The measured S-parameter matrix of the GFET device with V_{gs} = -1.5 V and v_{ds} = - 1 V at 1 GHz is:

$$\begin{pmatrix} 0.966\angle -29.96^\circ & 0.01\angle 70.7^\circ \\ 1.446\angle 159.2^\circ & 0.299\angle -169.4^\circ \end{pmatrix}$$

Generally, the standard small-signal amplifier circuit design steps are shown as follows:

• Unilateral or bilateral case checking.

The unilateral or bilateral case of the amplifiers is determined by the transmit S-parameter S_{12}. As can be seen the S_{12} is a small value but not equal to 0, therefore the error U due to the unilateral approximation need to be confirmed, using

$$U = \frac{|S_{11}||S_{12}||S_{21}||S_{22}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)}. \tag{3.5}$$

The calculated U is 0.05, which translate to 0.45 dB Gain error. Thus, the unilateral approximation is acceptable.

• Stability checking.

In order to check the stability of the amplifiers, K factor as well as $|\Delta|$ are required, of which the expressions are:

$$|\Delta| = |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}| \tag{3.6a}$$

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12} \cdot S_{21}|}. \tag{3.6b}$$

the calculate K and $|\Delta|$ are 2.12 and 0.21, respectively. This means the amplifier is unconditional stable.

• Matching network design.
As shown in Eq 3.2. In order to obtain better amplification performance, input as well as output matching network design are necessary, i.e., $\Gamma_S = \Gamma_{in} = S_{11}^*$ and $\Gamma_L = \Gamma_{out} = S_{22}^*$, respectively. Ideally, for the unilateral amplifier, the maximum power gain contributed from the device itself, input as well as output matching networks are shown below:

$$G_{S,max} = \frac{1}{1 - |S_{11}|^2} \tag{3.7a}$$

$$G_0 = |S_{21}|^2 \tag{3.7b}$$

$$G_{L,max} = \frac{1}{1 - |S_{22}|^2}. \tag{3.7c}$$

If perfectly matched at both input and output port, maximum of 8.6 dB and 0.2 dB power gain can be achieved. Generally, S_{11} of GFET is located in bottom half region and closed to the open point of the smith chart at 1 GHz, as shown in Fig 3.3a (red point). Therefore, a large value of series inductor, i.e. L > 20 nH, is required in order to achieve good conjugate input matching, resulting > 5 dB improvement. As for output matching part, the S_{22} of GFET is close to 50 Ohm, only 0.2 dB gain can be achieve by output matching. Therefore, setting $\Gamma_L = 0$, i.e., connecting directly with 50 Ω transmission line is acceptable to save chip area.
For input matching, the inductance can be realised by either Lumped or distributed elements. The lumped elements, such as wired inductor, are usually used at low frequency. However, the distributed elements, which were realised by transmission line and print structure, are much more popular in high frequency range due to its smaller parasitic effects. However, the wavelength at 1 GHz is around 30 cm, which is too large to be matched by traditional distributed transmission in an IC design. Previously, wired inductor was used in [62] and a L = 36 nH at 1 GHz was realised, achieving a 7-dB improvement from input matching network. However, it sacrifices the circuit's integration level. In our work, a planar inductor was designed in order to obtain simultaneously good input match and maintain the circuit's integration.

An equivalent circuit of the planar inductor is exhibited in Fig 3.3b, where L is the inductor, R is the sheet resistance, C_{pb} is the parasitic capacitance between two series resistance lines and C_p is the parasitic capacitance between signal and the ground. In order to improve the design accuracy, full -wave simulation (CST microwave studio, FDTD) was implemented and the drawn layout is demonstrated in Fig 3.4a. As shown, several metal air-bridges are required, and more details will be discussed in Chapter 4. In this design, both probe GSG separation and system impedance should be taken in to consideration, and the metal as well as substrate parameters keep the same as we used in the circuit design of the mixer. Fig 3.4b presents the results comparison of ideal inductor, inductor model as well as CST simulation for a 7-turn inductor at frequency from 0.5 GHz to 2 GHz. Pure inductance presents track that perfectly fit the unity circle in smith chart, where the parasitic capacitance effect and metal resistance make the S_{11} track of the planar inductor fall inside the unity circle. By fitting model measurement result with inductor model, each element can be extracted (shown in chapter 5). The circuitry of the amplifier structure are demonstrated in Fig 3.5.

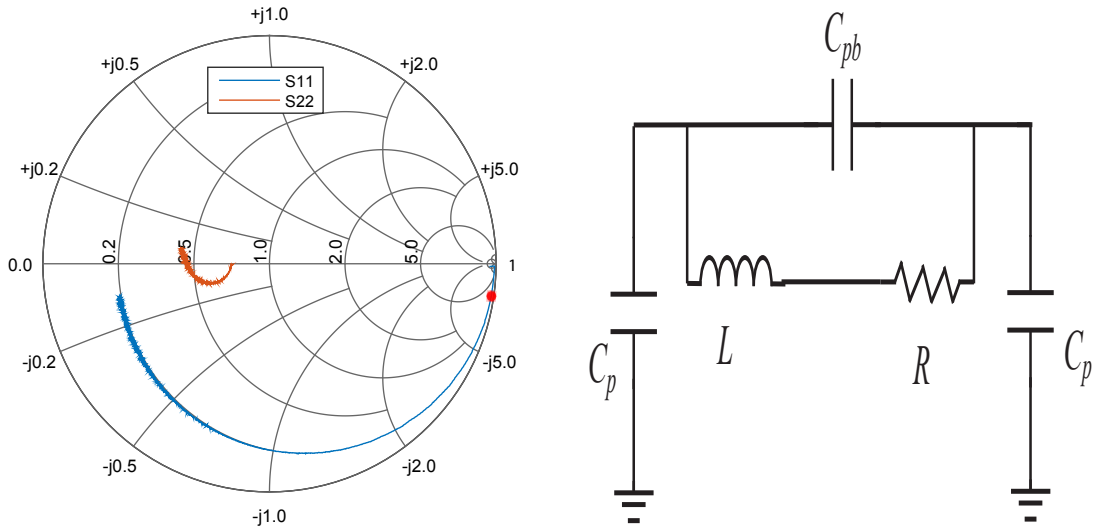

Figure 3.3: a) Measured S_{11} and S_{22} of a GFET with $L \times W = 1\times$ 160 μm^2 from 0.02 GHz to 20 GHz, b) planar inductor equivalent circuit.

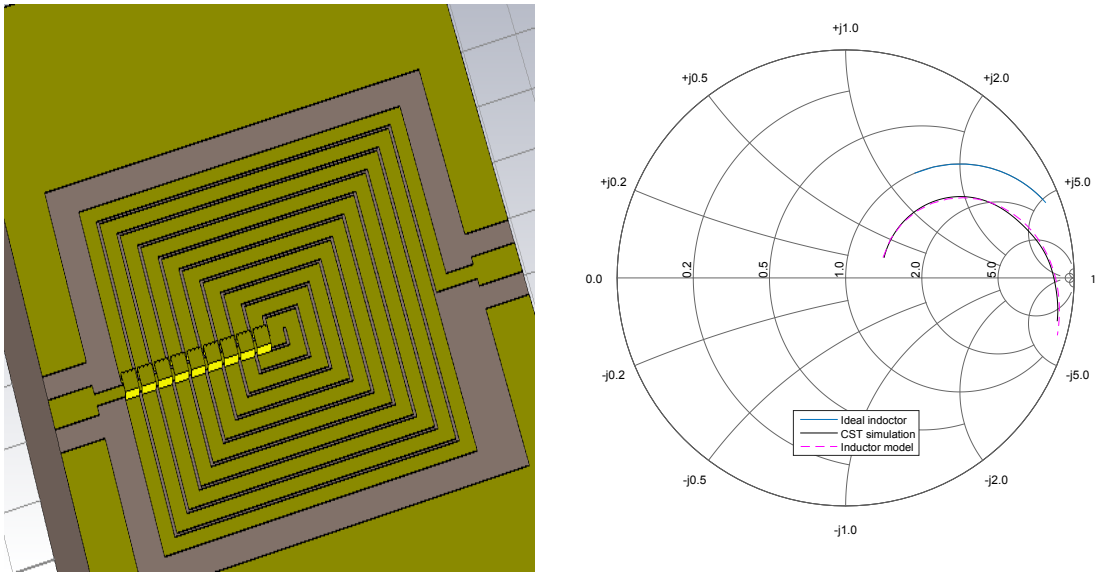

Figure 3.4: a) A test 9-turn rotated inductor CST simulation layout, b) results comparison of ideal L = 20 nH, inductor model and CST simulation for a 7-turn inductor from 0.5 GHz to 2 GHz.

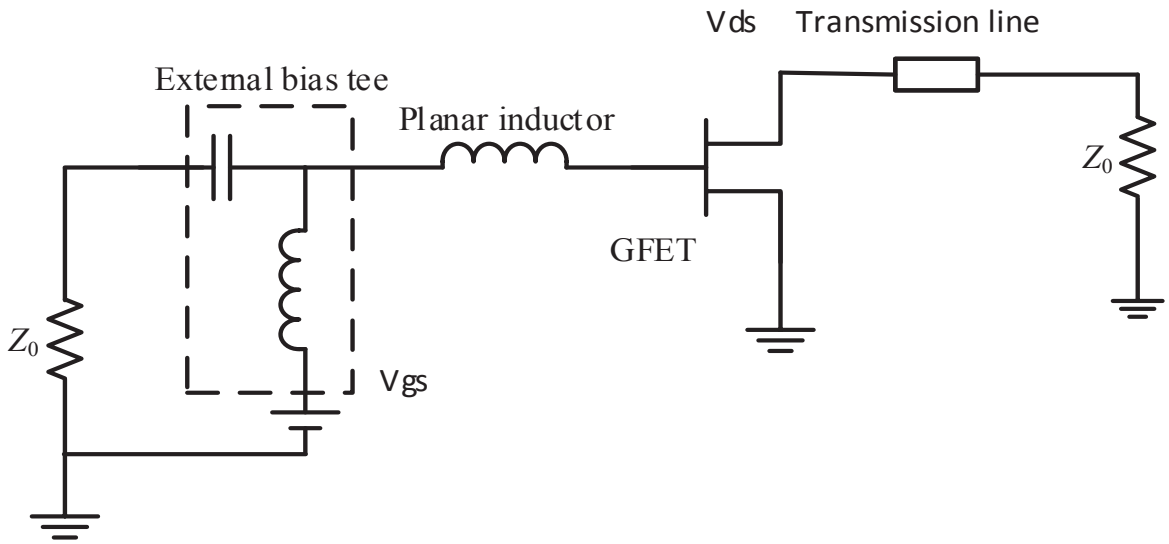

Figure 3.5: Amplifier circuitry.

3.2 Subharmonic resistive mixers

A mixer plays an important role in wireless communication system which enables signal frequency up-convertsion or down-conversion and maintain the information simultaneously [63]. Up-converting mixer is used in transmitters, where down-converting mixers are implemented in receivers. Mixers can be separated into two different groups according to different types of mixing method. One is the passive mixer(resistive), of which the CL can be expressed as CL = P_{IF} / P_{RF}. Another is named the active mixer(transconductance), which may offer conversion gain, CG = 1/ CL. Generally, down-converting mixers contain three ports. Two input port, the radio frequency f_{RF} as well as the local oscillator pumping frequency f_{LO}, and one output port at the intermediate frequency f_{IF}. By analysing the product of two cosinusoids, the mixing principle can be expressed as the sum and difference frequencies,

$$cos(\omega_{RF}t) \times cos(\omega_{LO}t) = \frac{1}{2}[cos(\omega_{RF} + \omega_{LO})t + cos(\omega_{RF} - \omega_{LO})t]. \tag{3.8}$$

Apart from the fundamental mixing method mentioned above, there is another type of mixer for which the RF frequency mix with a harmonic component of the LO frequency, $f_{IF} = f_{RF} \pm n \times f_{LO}$. For our subharmonic mixer case, the harmonic factor n = 2. Due to the lack of high power local oscillator source in the high frequency range, subharmonic mixers are promising with only half frequency LO source required. Besides, the electron-hole duality of GFETs makes single device subharmonic resistive mixing possible.

3.2.1 GFET design

GFETs characterisation and optimisation is the key step to in the mixer design. In a subharmonic resistive mixer, the drain-source channel resistance is swept by an LO source at the gate as a time-varying resistor, $R_{ds}(t)$, which contains different harmonic frequency components. According to [64], the conversion loss is quantified as,

$$CL = \frac{\pi^2}{(\Gamma_{max} - \Gamma_{min})^2}, \tag{3.9}$$

where, a time-varying reflection coefficient is defined by,

$$\Gamma(t) = \frac{R_{ds}(t) - Z_0}{R_{ds}(t) + Z_0}. \tag{3.10}$$

Aiming to achieve a lower CL, higher Γ_{max} as well as lower Γ_{min} are required, which translates to $R_{max} \gg Z_0$ and $R_{min} \ll Z_0$. This requires GFET components with high current on-off ratio and preferably with an impedance level $Z_0 = \sqrt{R_{max}R_{min}} \approx 50\ \Omega$. The drain-source resistance of GFETs is shown as,

$$R_{ds} = R_{channel} + R_c, \tag{3.11}$$

Here, the $R_{channel}$ presents the gate variable GFET channel resistance, and it is essentially determined by $L_{channel}/W_{channel}$, and the R_c describes the contact resistance, which determined by the contact area [60]. For the sake of getting a lower R_{min}, a wider device is beneficial. One the other hand, a wider device simultaneously reduces R_{max} due to no off-state in GFETs. Furthermore, the RF performance of the device is strongly dependent with the gate C_{gs} and C_{gd}, which is determined by channel area, i.e. $L_{channel} \times W_{channel}$. Generally, this trade-off in the device dimension limit the degrees of freedom for a normal GFET channel structure because of $L_{channel} = L_{gate}$ and $W_{channel} = W_{gate}$. As described in chapter 2, an arrays of nanoconstrictions [65], i.e., bow-tie structured GFET channels which offers $W_{gate} > W_{channel}$, are implemented to realise simultaneously a higher current on-off ratio and a proper impedance level. The best device dimension value can be obtained by applying the Large-signal GFET model described in Chapter 2 into EDA tools. Fig 3.6a demonstrates the final dimension of the GFET channel, and Fig 3.6b shows a GFET device micrograph. After optimisation, the best CL point is given with $W_g = 12\ \mu$m, of which around 120 nanoconstructions and 100 nm for each are designed.

3.2.2 Circuit design

Transmission line technology is the foundation of the high frequency circuit design. As the operation frequency increases, the wavelength reduces to a similar level compared with transmission line dimension. Thus, the distributed transmission line technology becomes popular for the purpose of transferring signal information through different components in a designed impedance level. Several transmission technologies can be implemented to satisfy different applications. For instance, the

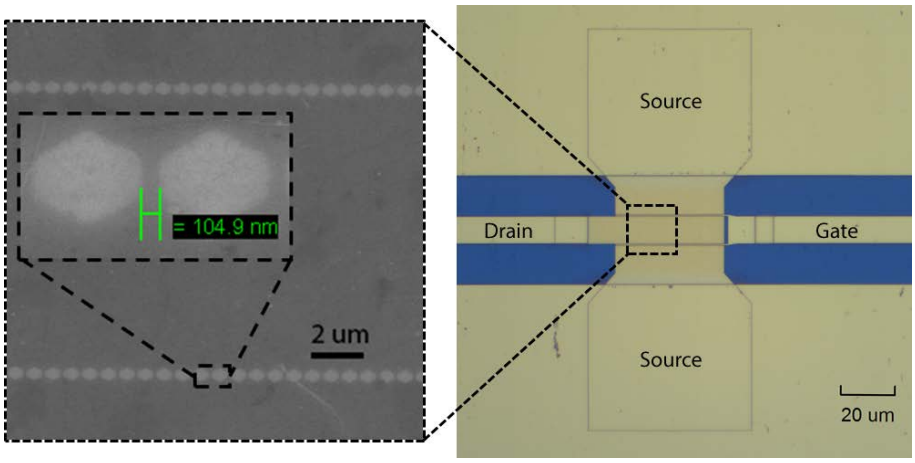

Figure 3.6: a) SEM image of patterned graphene channels b)a close-up image of the two-finger G-FET.

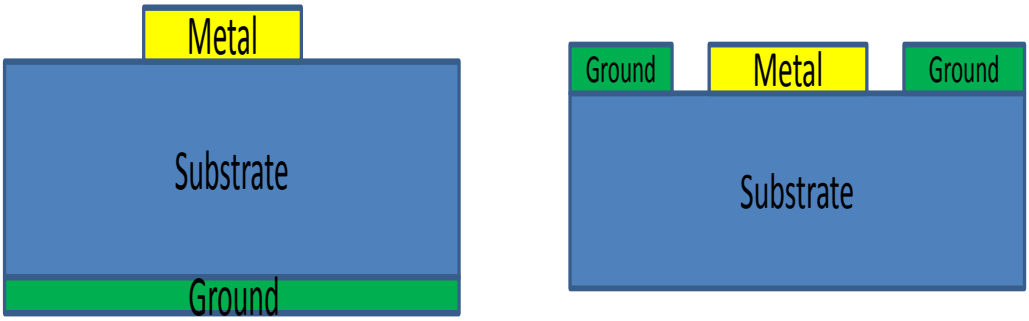

Figure 3.7: Diagram of a) microstrip and b) coplanar waveguide.

coaxial transmission line is perfectly protected and can be either planar or banded, which makes flexible electronics possible. While the coplanar stripline enables simple feeds for printed dipole antennas. Most commonly, there are two most popular transmission line technologies in modern microwave circuits, namely microstrip, shown in Fig 3.7a, and Coplanar Waveguide (CPW) described in Fig 3.7b.

Microstrip technology is competitive in microwave frequency due to its simple structure and sufficient infrastructure for both EDA and electromagnetic (EM) simulation. Nevertheless, some drawbacks limit the microstrip utilisation in sub-millimetre and even higher frequency range. For the reason that the ground plane is on the other side of metal plane, a via through substrate is required to contact with ground. As the operating frequency increasing, the parasitic inductance access effect becomes critical which decreases RF performance dramatically [66]. In addition, energy will easily radiate and couple to adjacent structures when electrical length and substrate thickness are in same level. Conversely, CPW technology overcomes this limitations and becomes more compact in higher frequency IC designs. In view of same plane

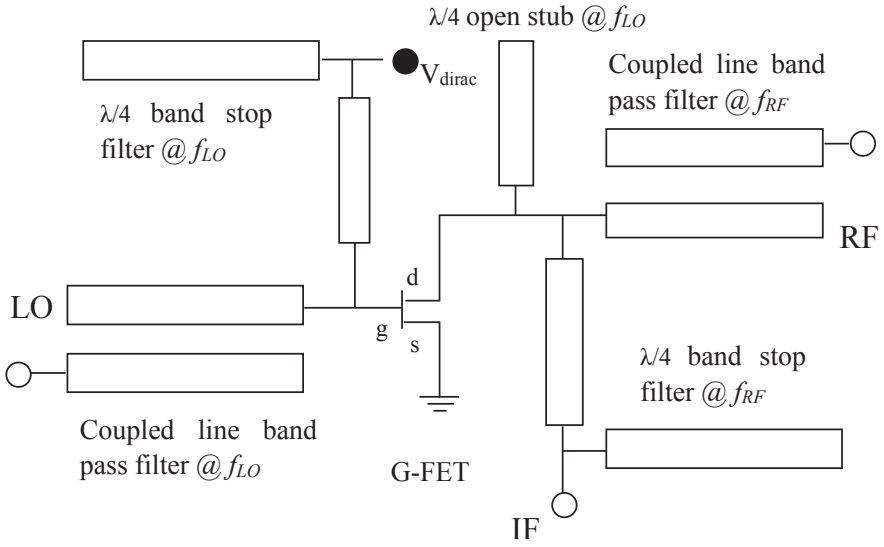

Figure 3.8: The mixer topology.

between signal and ground, parasitic inductance access effect mentioned above can be significantly reduced. Wider separation between metal line and ground plane make conductor loss minimum also. Moreover, much lower dispersion than microstrip techniques offers CPW more degree of freedom in broadband applications [67]. Hence, our circuit is realised in CPW techniques with relatively lower risk of parasitic mode propagation as well as lower dispersion [68] obtained after properly designed.

The dimension of the CPW line and the thickness of the silicon substrate are two main things that need to be taken into consideration in our circuit. Generally, microwave applications are applied in 50 Ohm level, therefore, a 50 Ohm CPW transmission line is required. In addition, the silicon substrate thickness need to be thinned down due to the multi-mode propagation and the radiation loss at high frequency. In practice, thinned silicon substrate (especially under 100 μm) is not robust, of which a break may happen when doing the lapping process. In order to design a CPW line with a proper dimension and to ensure the suppression of such effects and for layout dimensional optimization, full wave EM simulations (CST, FDTD) is applied. To achieve 50 Ω line impedance and fit the device dimension, the center line of the CPW is designed to be 10 μm, together with 15 μm gaps at both sides. The center metal and the metal-ground spacing are designed to be 10 μm and 15 μm respectively. The silicon substrate thickness is designed to be 100 μm to keep the low radiation loss and chip robust simultaneously. wide ports are designed for the purpose of matching the pitch of the GSG probe (75 μm) during the measurement as can be seen in Fig 3.9.
For the purpose of designing a good mixer related circuit, subharmonic resistive mixer topology need to be studied, which is presented in Fig 3.8. The RF frequency, IF frequency and LO frequency are designed to be 200 GHz, 1 GHz, and 100.5 GHz respectively. As shown in the topology, IF port as well as RF port meet at drain side,

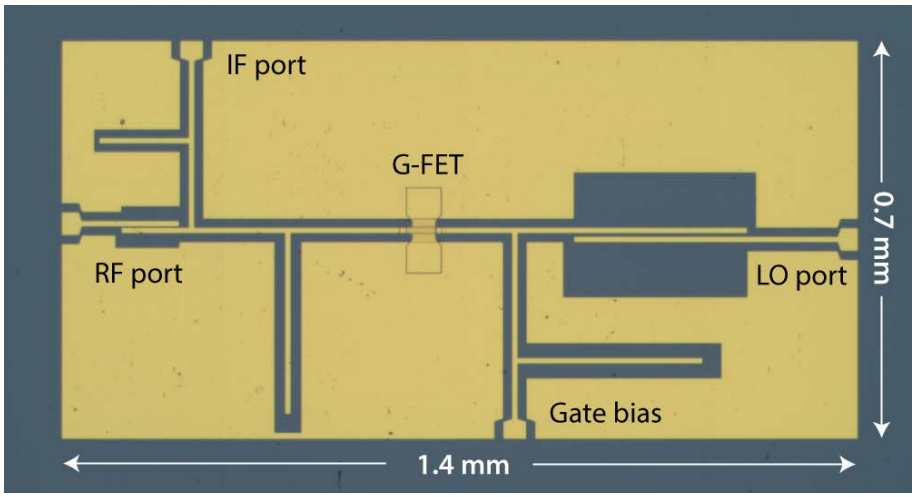

Figure 3.9: Micrograph of the fabricated circuit.

hence, a good block should be implemented to realise RF-IF isolation. Generally, the bandpass filter usually presents periodical property, wherefore it is difficult to design a bandpass RF and IF filter due to the large frequency gap from 1 GHz to 200 GHz. Moreover, multi-stage is necessary when designing a narrow band bandpass, which makes the circuit roomy and complex. Therefore, we realise the filter by a simple stub bandstop filter as well as couple line filter. This two types of simple filter are preferable because of the requirement of circuit simplification and area limitation. As for LO signal, however, neither the IF- nor the RF-filters are able to attenuate LO signal. Hence, an additional bandstop filter at the LO frequency is required. Similarly as the DC feed, we use a simple stub bandstop filter operating at LO frequency to achieve the LO rejection. By locating one stub filter at drain trunk, both LO-RF and LO-IF isolation are well achieved. The mixer layout is exhibited in Fig 3.9.

3.2.3 Circuit optimisation

Circuit optimisation is the next step going from theory towards practice. One prior thing is the metal air-bridge, which is commonly applied in high-frequency IC design. Generally, in order to connect different structures and perform specific circuit performance, T-connection is inevitable, as can be seen in mixer layout, Fig 3.9. However, in sub-millimetre and even higher frequency range, much shorter wavelength give rise to discontinuity at T-structure of the circuit. Additionally, large ground plane takes electric potential difference between two sides of the transmission line, by which extra energy loss is caused. Hence, signal propagation loss caused by energy leakage should be reduced. Metal air-bridge is a popular way in many IC designs [66] to make current flow from one side of ground plane to another as well as reduce circuit discontinuities. Practically, two main reasons make it difficult to set up a parameterised model. One is the large amount of variables included, the other is the configuration must be taken into account [66]. Therefore, full-wave simulation (CST studio) is implemented for air-bridge design and performance estimation.

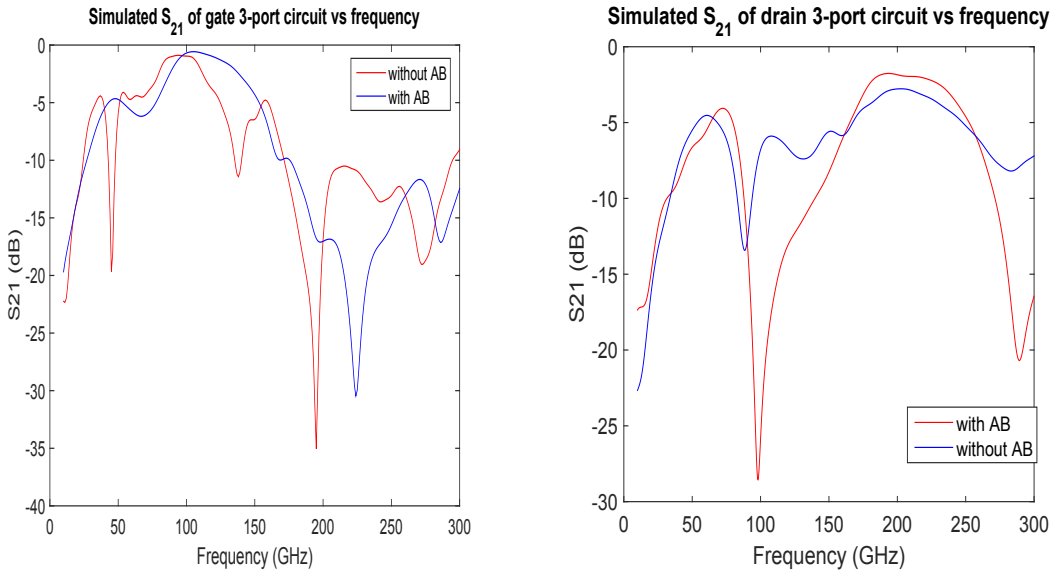

Figure 3.10: CST simulation result comparison between with and without air-bridges of the 3-port a) gate b) drain 3-port circuits.

Fig 3.10a and 3.10b demonstrate the CST simulation result comparison between the circuit with and without air-bridges of the grain and gate 3-port circuits. As shown clearly, the metal air-bridges enhance the circuit performance by 0.6 dB at 100 GHz LO passband and by 2.3 dB at 200 GHz RF passband respectively. Furthermore, the height of the air-bridges should also be taken care due to the parasitic capacitance between the air-bridge and the transmission line, especially in sub-millimetre wave or even higher range. More than 1.5 μm height is necessary to reduce the parasitic effect mentioned above, according to the simulation result.

3.2.4 Circuit integration

The first version of the integrated receiver circuit including the mixer and amplifier is also designed. The block diagram of the integrated receiver circuit is demonstrated in Fig 3.11. As can be seen, a intermediate capacitor is required due to the different bias condition of the amplifier and the mixer. The most common way in MMIC designs is to insert a metal-isolation-metal (MIM) capacitor which enables the circuit integration and DC isolation simultaneously. The MIM capacitor is a parallel plate capacitor, of which the capacitance can be calculated approximately as,

$$C = \frac{\epsilon A}{d}, \tag{3.12}$$

where A is the area of parallel plate capacitor, ϵ is the dielectric constant, and d is the distance between the two parallel metal plates. In our receiver system, this MIM capacitor should be implemented between IF port of mixer and the small signal amplifier. The IF frequency at 1 GHz should pass through the capacitor as well. According to Eq 3.12, a MIM capacitor with 200 μm^2 metal area with 30 nm Al_2O_3 thickness is necessary, with which less than 1 dB loss can be obtained by the MIM

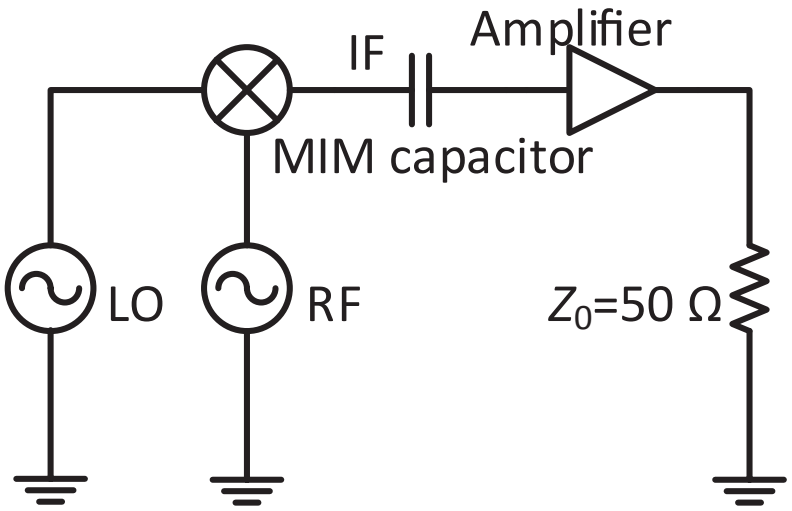

Figure 3.11: Diagram of the integrated receiver circuit.

capacitor at 1 GHz.

4

Circuit fabrication techniques

In this chapter, the circuit fabrication techniques in details are introduced.

4.1 Graphene preparation

Till date, two main graphene fabrication procedures are most commonly used, exfoliated and chemical vapour deposition (CVD) [69]. Graphene prepared by exfoliation presents the highest mobility and lowest defect density, whereas CVD techniques shows a lower mobility but a large scale fabrication possibility. The lower mobility of CVD method is mainly caused by the water molecules at the graphene-substrate interface by which strong p-type films generated [70]. In this thesis, the graphene sample are prepared by the CVD technique. The main advantage of CVD graphene is the potential flexibility. In principle, the CVD graphene can be transferred from catalyst to an arbitrary flexible substrate, plastics for example, by which the graphene based electronics becomes a potential candidate for flexible electronics [71]. In this process, graphene was grown on 50 μm thick Cu foil (99.9995% purity). The process flow can be described as follows: to begin with, acetone and isopropanol are utilised in order to remove organic residual and clean the foils. Secondly, 5 min copper annealing in 20 sccm H_2 and 1000 sccr Ar at 1000°C. Furthermore, etching procedure is implemented for the purpose of etching away remaining oxide and improving graphene quality. Last but not the least, 30 sccm methane (CH_4) carbon precursor gas was diluted to 5 % in Ar. Final step is to cool down the graphene sample to room temperature.

After growing graphene on Cu foil, transferring procedure should be applied to transfer graphene from Cu to high resistive silicon substrate [69]. Firstly, Poly Methyl Methacrylate A4 resist (PMMA) was spun on Cu foil and working as supporting polymer. Subsequently, electrolysis method was used and graphene can be separate from Cu foil by H_2 bubbling. During this step, an polyethylene terephthalate (PET) thermal releasing tape was glued on the PMMA to reduce the possibility of break and wrinkles. After separation, the frame was placed on the high resistive Si substrate and wait for graphene sample until it becomes dry. Finally, the PMMA can be washed away by acetone.

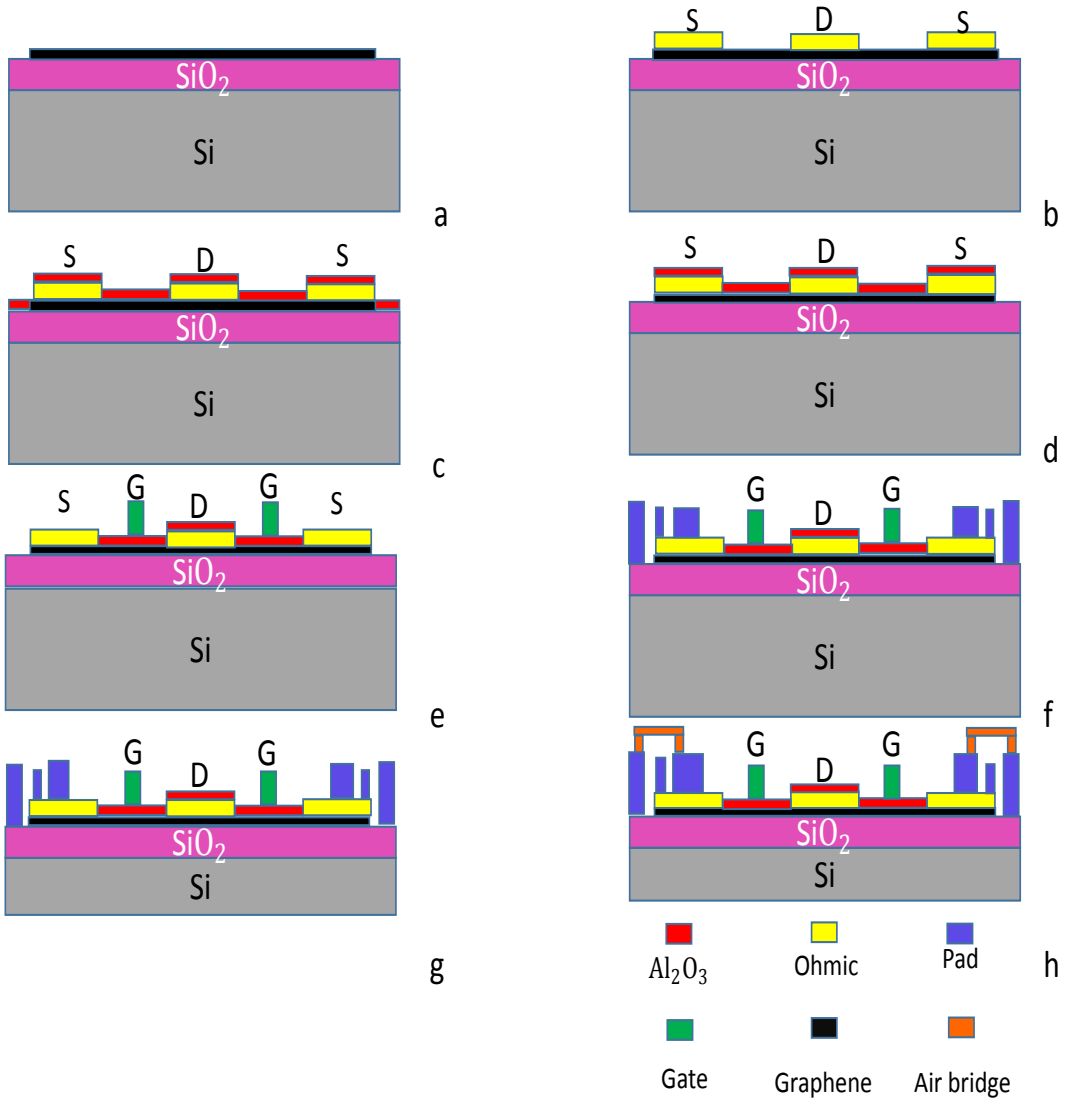

Figure 4.1: IC fabrication flow.

4.2 IC fabrication flow

An electron beam (e-beam) as well as Direct Laser Writer (DWL) based procedures are utilised for the sake of fabricating ICs. E-beam lithography is a slow process but achieves high accuracy (10 nm) compared with photo lithography (>1 μm). After transferring graphene on 280 μm high resistive silicon substrate (10 kΩcm bulk resistivity), the following step by step fabrication procedures are illustrated in Fig 4.1 and descriptions for each step are described as follows.

• Mesa layer is patterned in the beginning step. Negative resist (ma-N 2401) is spun on the chip. After the e-beam and developing processes, a plasma etching (50 W) chain including 5 s - 250 mTorr, 6 s - 50 mTorr, and 3 s - 250 mTorr to remove resist, etch graphene and clean burned resist respectively. The SEM image for patterned

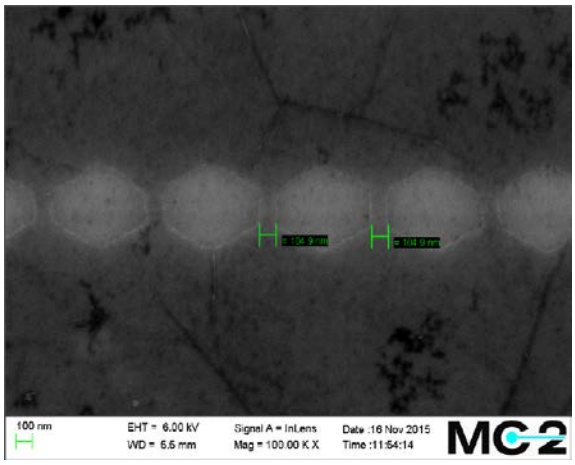

Figure 4.2: A SEM image for patterned graphene channel.

graphene channel is shown in Fig 4.2, and the distance between two nanoconstructions is measured to be $\sim$ 105 nm, which is within $\pm$ 5 nm of the designed value.
• As can be seen in Fig 4.1b, the second step is to pattern the Ohmic contacts layer which consist of 1 nm Ti, 15 nm Pd, and 100 nm Au. The Ti layer is operating as adhesion layer, which the Pd layer is used to determine the contact property. A bilayer resist stack which includes ZEP 520A and MMA EL10 was spun before the second e-beam lithography, and metalisation by e-gun evaporation and lift-off steps follows the e-beam process. Afterwards, an annealing process in Ar gas at T = 230° C enables graphene cleaning of resist residue [72] and decreasing contact resistance [73].
• Additionally, 4 times the flow of 1 nm Al evaporation + 160° C baking together with a 176-cycle 15 nm Al_2O_3 atomic layer deposition were used to generate 15 + 4 $\times$ 1.5 nm Al_2O_3 dielectric layer. Then, the same e-beam and evaporation procedure continues for 10 nm Ti + 250 nm Al + 50 nm Au gate fingers, as shown in Fig 4.1d and e. Besides, an additional 176 cycles atomic layer deposition process was processed to grow the extra 15 nm thick MIM capacitor dielectrics (30 nm in total).
• After atomic layer deposition, Al_2O_3 covers everywhere on the chip. Hence, an extra etch layer should be patterned at the contact area between device and circuit pad in order to etch down dielectrics and make a perfect contact. Due to less accuracy required, DWL process, uses S1813 positive resist and BOE etching of oxide, is applied to simplify the fabrication processes.
• Circuit pad layer is the most time-consuming step all over the fabrication flow. Utilising similar procedure as Ohmic layer (e-beam + evaporation), 10 nm Ti + 500 nm Au circuit metal layer was made, see Fig 4.1f.
• Then, the silicon substrate was thinned down from 280 μm to 100 μm by a lapping process (Fig 4.1g).
• Finally, for the air-bridge fabrication, two layer steps is required. One is the support layer, including HMDS and PMGI, of which the HMDS is used to make resist stay at SiO_2, and PMGI layer is used to support the air-bridge before lift-off. Fig 4.3a exhibits the micrograph of support layer after S1813 resist removal (DWL test). Another layer is for metal evaporation of the air-bridges, using PMMA A11 resist

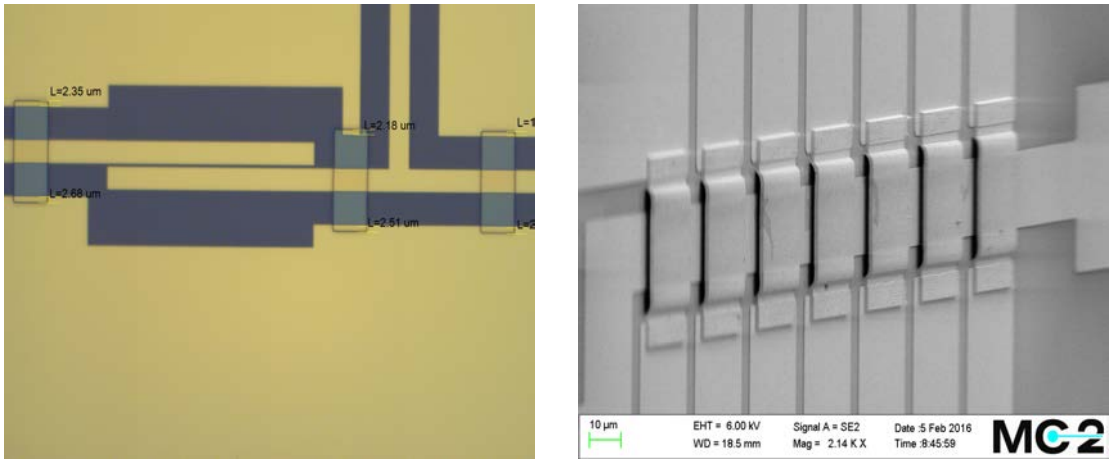

Figure 4.3: a) Micrograph of support layer of air-bridges, b) SEM image for metal air-bridges.

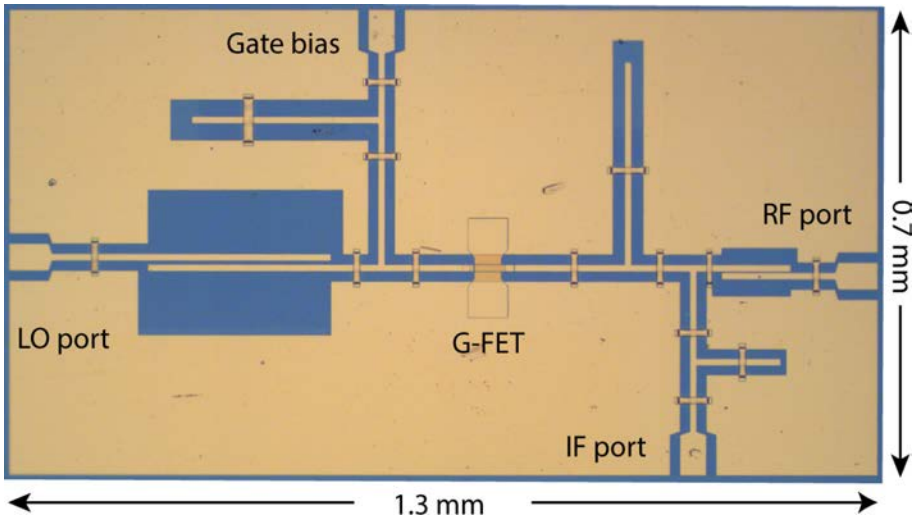

Figure 4.4: Micrograph of second version mixer.

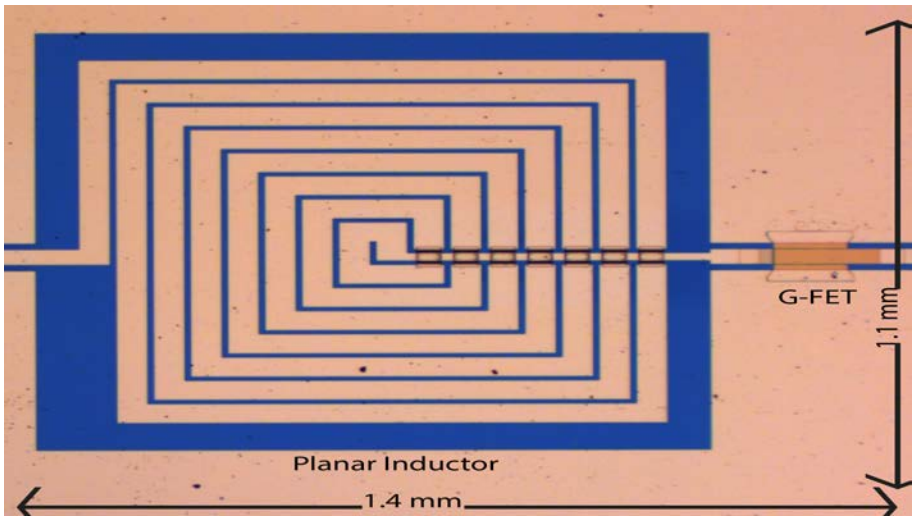

Figure 4.5: Micrograph of amplifier layout.

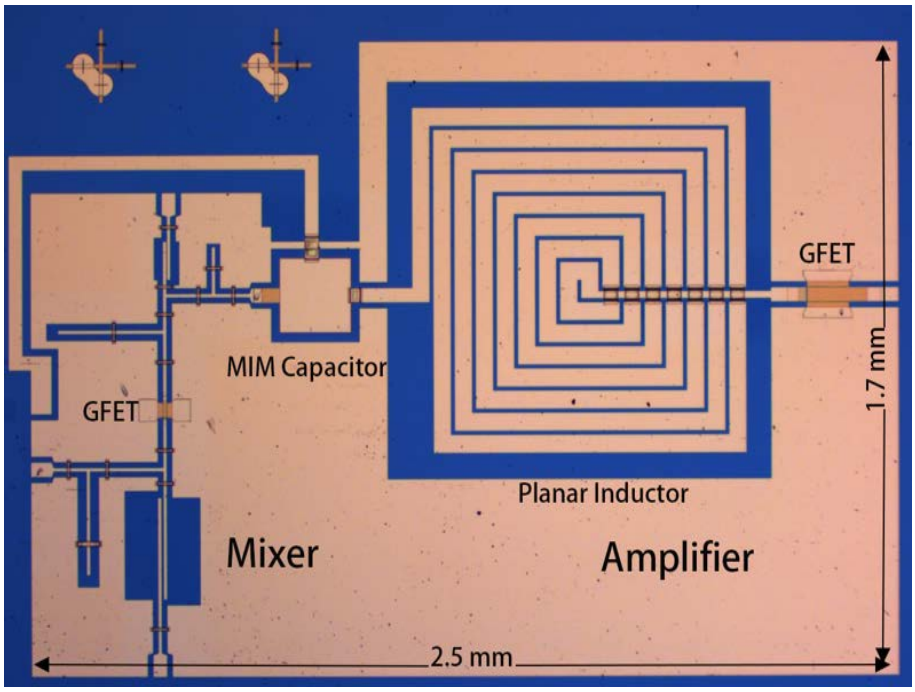

Figure 4.6: Micrograph of integrated receiver layout.

(Fig 4.1g). After e-beam, evaporation and PMGI removal, air-bridge with a height of 1.5 μm is achieved, Fig 4.1h. The SEM image of metal air-bridge can be seen in Fig 4.3b.
During the process we did substrate lapping in front of air-bridge fabrication for the sake of reducing the possibility of the air-bridge broken, where several problems are caused by this fabrication sequence. The air-bridge dimension is in μm level so that DWL is preferable for saving time. However due to the $\pm$ 3 μm margin of the lapping process, the undersurface of the silicon substrate after thinning down is not perfectly flat and the whole sample becomes concave. This makes the chip difficult to stabilise on the DWL by the vacuum hole. Therefore, time-consuming e-beam have to be used instead. In addition, thinned chip was hard to handle by tweezers during the air-bridge fabrication step. Actually, the fabricated air-bridge can be protected by thick resist when thinning down the substrate. Therefore, doing lapping step at last could be better.

Fig 4.4 and Fig 4.5 shows the micrograph of final layout of the amplifier and mixer circuit. The dimension of the mixer and amplifier circuit are measured to be 0.7 mm $\times$ 1.4 mm and 1.1 mm $\times$ 1.4 mm, respectively. Fig 4.6 is the image of the fabricated integrated receiver circuit.

5

Circuit characterisation and discussions

In this chapter, the measurement setup is described at first. Then the measurement characterisation including modelling parameter extraction, amplifier as well as mixer measurement results are presented and discussed.

5.1 Measurement setup

The measurement setup consists of three part. For DC characterization of GFETs in mixer and amplifier, Keithley 4200 semiconductor characterisation system is used. Using four-probe measurement, the I-V curves as well as drain-source resistance can be measured. Besides, the amplifier S-parameter from 0.5 - 20 GHz are measured by Agilent N5230A network analyser. Finally, the mixer is characterized on-wafer using waveguide interfaced multi-pin GSG microprobes. The LO chain consists of an OML ×6 multiplied source connected by a W-band power amplifier. The RF power level can be swept electronically and provided by a standard VDI-AMC-S120 ×18 multiplier module. An Agilent E4419B power metre together with a W8486A power sensor and an Erickson PM4 power metre are applied for the LO and RF powers calibration, respectively. The FSU26 spectrum analyzer is used for monitoring the IF signal power. The block diagram and the photo of the measurement chain for the circuit characterisation is sketched and demonstrated in Fig 5.1 and Fig 5.2 respectively.

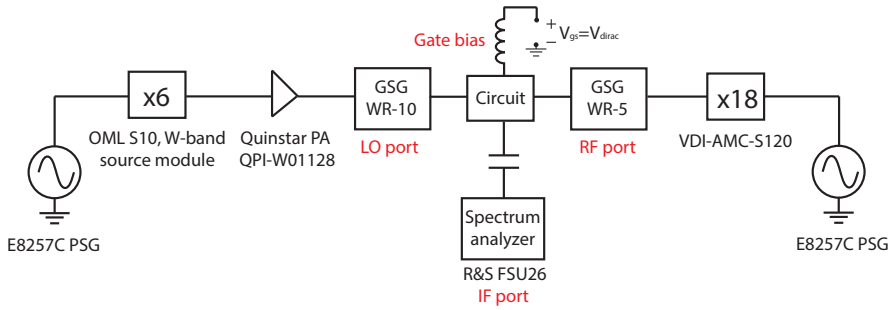

Figure 5.1: Schematic block diagram of the circuit measurement setup.

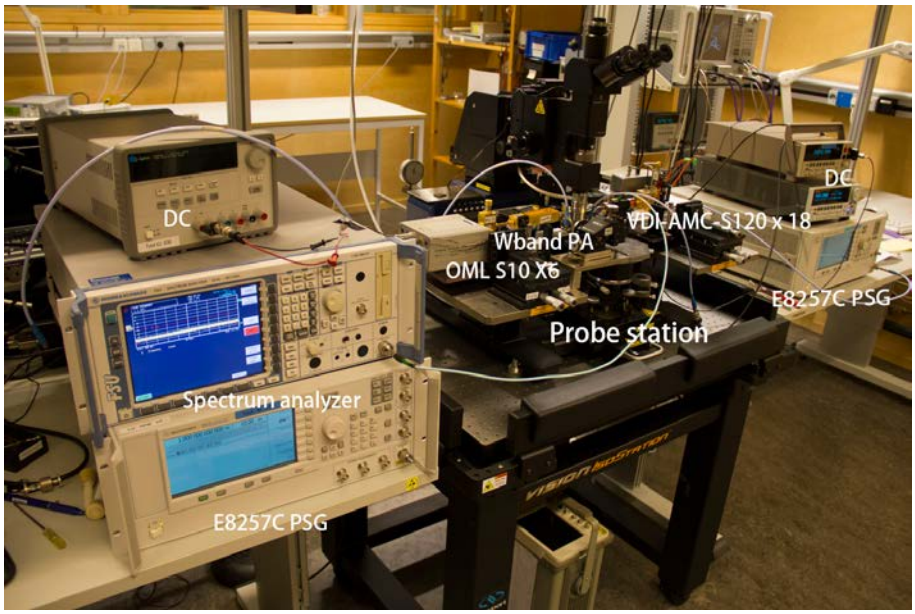

Figure 5.2: Photo of the the circuit measurement setup.

Table 5.1: Parameters extracted from DC characteristics for mixer and amplifier devices

	mixer	amplifier
R_{ext}(Ohm)	16	10
$n_0(cm^{-2})$	$10 \cdot 10^{11}$	$14 \cdot 10^{11}$
$\mu_e(cm^2/Vs)$	1900	880
$\mu_h(cm^2/Vs)$	1850	810
V_{dirac}(V)	-1	-1.2
$C_{gate}(nF/cm^2)$	440	440
R_g(Ohm)	1	1.4
R_c(ohm)	11.2	1.6

5.2 Circuit characterisation

5.2.1 Model parameter extraction for GFET

Fig 5.3a and b demonstrate the simulation as well as measurement result of drain resistance R_{ds} versus gate bias voltage V_{gs} at V_{ds} = 0.1 V for mixer and amplifier devices respectively. As can be seen, for mixer device, a current on-off ratio $\sim$ 5 is achieved and the average impedance level is close to 50 Ohm with the device dimension $L_g \times W_g$ = 0.5 $\mu m\times$ 80 μm, where for amplifier device, relative high transconductance g_m (3 mS) is realised with the device dimension $L_g \times W_g = 1\mu m\times$ 240 μm. According to the large-signal modelling discussed in Chapter 2, model parameters can be extracted by fitting R_{ds} curves, and the value are presented in Table 1.

S-parameter fitting as well as the parameters extraction of previous devices are beneficial to estimate the level of the model parameters of our amplifier and mixer

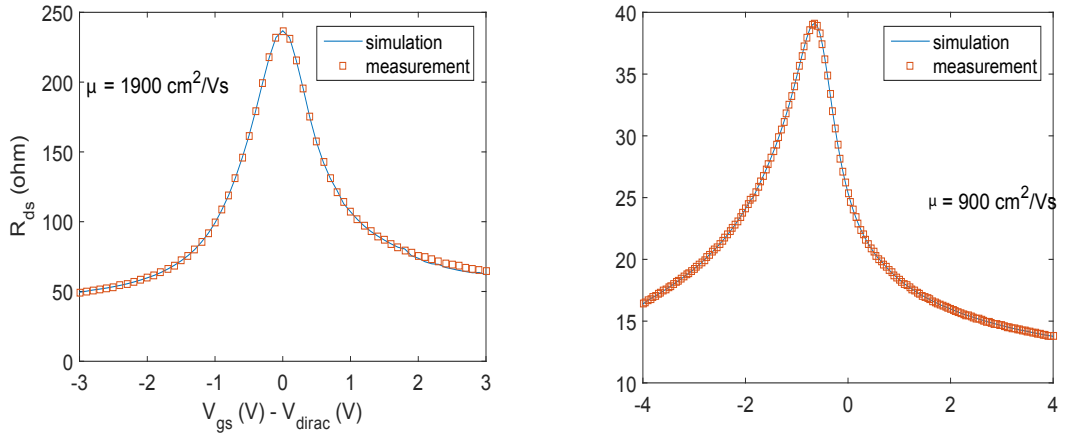

Figure 5.3: The simulation and measurement of drain resistance R_{ds} versus gate bias voltage V_{gs} of a) mixer b) amplifier, at $V_{ds} = 0.1$ V.

Table 5.2: Parameters extracted from S-parameter fitting for different devices

	0.5 μm	1 μm	2 μm
R_i(Ohm)	60	46	40
L_g(pH)	64	46	41.9
L_d(pH)	19	26	18
L_s(pH)	6.5	5	5.5
C_{pg}(fF)	4	7	8
C_{pd}(fF)	5	6	8
C_{ds}(fF)	7	3	6
R_{pg}(ohm)	7000	8200	7000
R_{pd}(ohm)	6500	7300	6100

devices. Fig 5.4, Fig 5.5, Fig 5.6 demonstrates the S-parameter measurement versus model simulation for GFETs with the gate width of 20 μm and the gate length of 0.5 μm, 1 μm, and 2 μm respectively. By using the method mentioned in chapter 2, the model parameters can be extracted in Table 2. The parasitic inductance is depend on pad structure of the device and usually at 5-30 pH level, and the parasitic resistance R_{pg} and R_{pd} generally keep in kOhm range. The parasitic capacitance usually stay in several fF region. Apart from that, some parameter-dimension relationships can also be described according to the study on previous devices,

$$R_{ch} \sim \frac{L_g}{W_g} \tag{5.1a}$$

$$R_c \sim \frac{1}{W_g}(800Ohm \cdot \mu m) \tag{5.1b}$$

$$C_{gs} \simeq C_{gd} = L_g \times W_g \cdot C_{ox}/2, \tag{5.1c}$$

where C_{ox} is the oxide gate capacitance which can be estimated by standard planar metal capacitance equation, i.e., Eq 4.1, and these scaling rules were used in the device optimisation described in chapter 3.

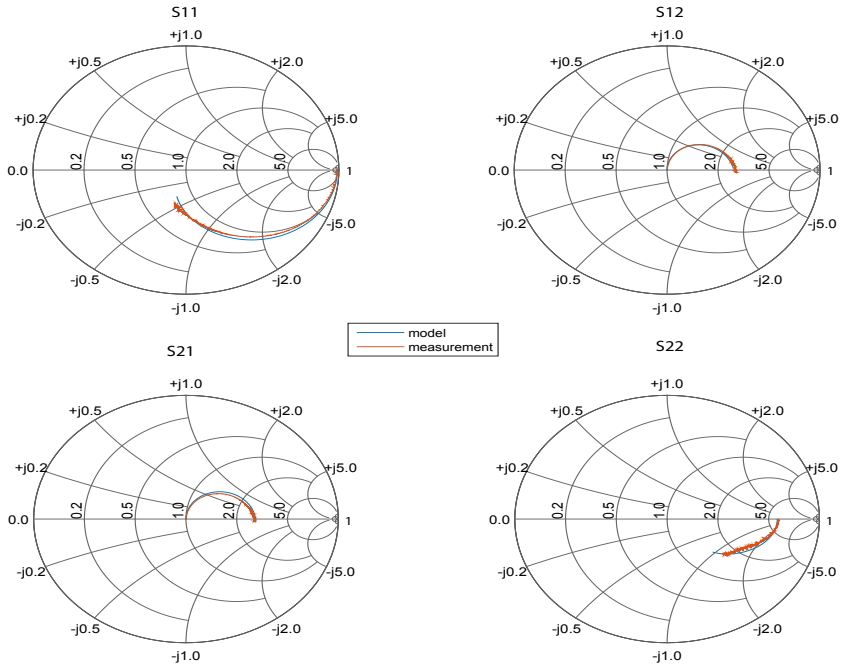

Figure 5.4: S-parameter measurement versus model for GFET with 0.5 μm $\times$ 20 μm, 0.1 - 60 GHz.

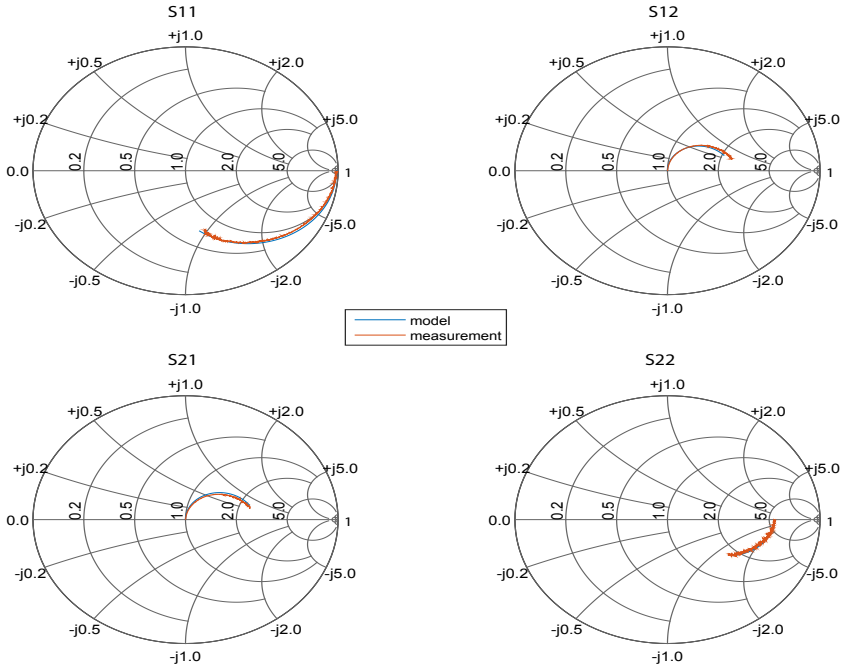

Figure 5.5: S-parameter measurement versus model for GFET with 1 μm $\times$ 20 μm, 0.1 - 60 GHz.

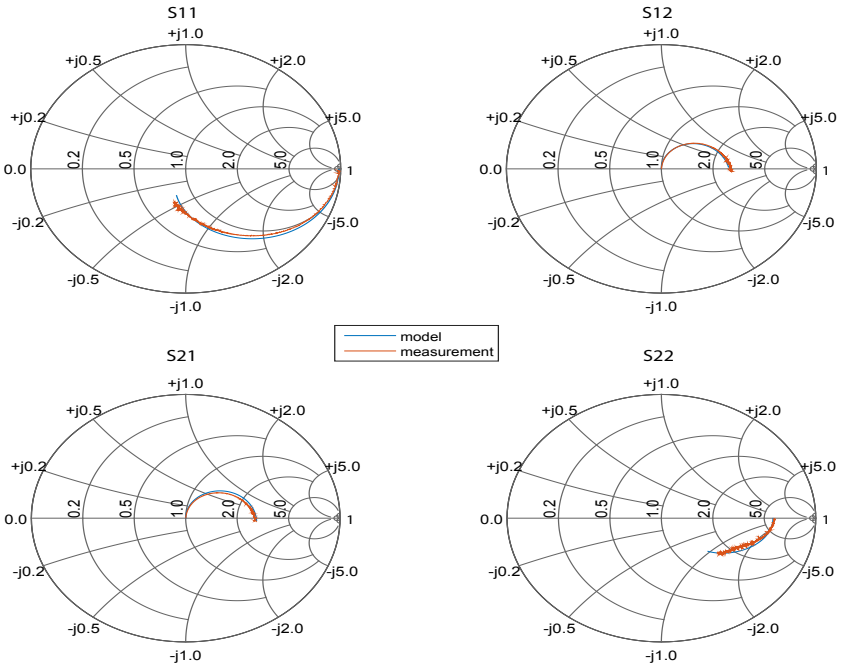

Figure 5.6: S-parameter measurement versus model for GFET with 2 μm $\times$ 20 μm, 0.1 - 60 GHz.

Table 5.3: Inductor model parameters extracted from measurement result

	R(Ω)	L(nH)	C_{pb}(fF)	C_p(fF)	Q
6-turn	21	16	3	133	4.8
7-turn	24	21	5	145	5.5
8-turn	29	25	7	177	5.4
9-turn	35	29	9	190	5.2

5.2.2 Amplifier measurement

Fig 5.7 presents the measurement result of S_{11} of 6-, 7-, 8-, and 9-turn planar inductor. By fitting the S_{11} of the inductor model with the measurement result, shown in chapter 2, the parameter value also can be extracted for 6-turn, 7-turn, 8-turn and 9-turn planar inductor respectively. Extracted values and the calculated Q value of the inductor are shown in Table 3. Despite a higher inductance value presented, a higher parasitic capacitance as well as resistance which created by the higher order printed inductor simultaneously will kill the matching performance dramatically. Besides, the higher turn planar inductor also occupies much larger area than that of a smaller turn inductor. As a consequence, we decide to utilise 7-turn planar inductor.

The measured S_{11} and the power gain in dB of the amplifier are demonstrated in Fig 5.8a and 5.8b respectively. As shown in Fig 5.8a, the S_{11} presents a value of 15 dB at 1.1 GHz, which indicates a good matching achieved, and around 0.1 GHz frequency drift compared with simulation. That is to say, the fabricated planar

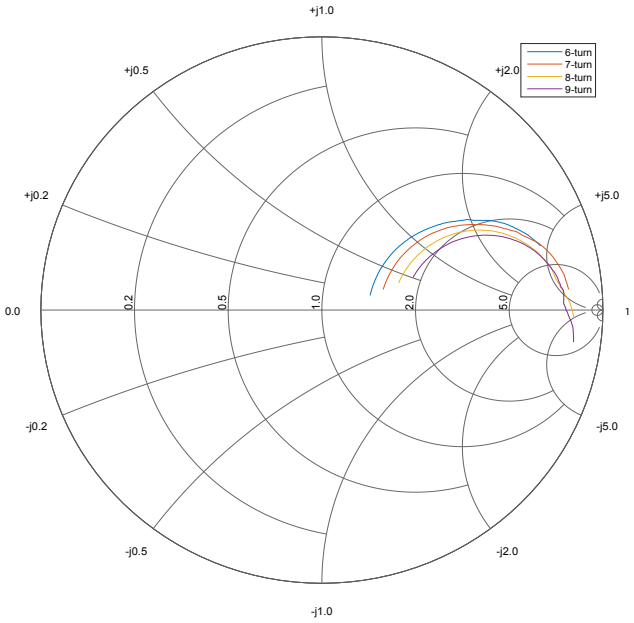

Figure 5.7: Measured S_{11} of 6-, 7-, 8-, and 9-turn planar inductor, from 0.01 - 3 GHz.

Table 5.4: Comparison of graphene-based resistive mixers

	[32]	[33]	[34]	[30]	[74]	[75]
RF frequency (GHz)	2	3.6	5	27	330	190
Conversion Loss (dB)	14	33	20	18	65	31.5
Subharmonic Order	1	1	2	2	6	2

inductor shows good but narrow-band matching performance. Fig 5.8b describes the power gain from 0.2 GHz to 2 GHz at V_{gs} = -1.6 V and V_{ds} = -3.5 V. As can be seen, close to 6 dB power gain is realised by the small signal amplifier.

5.2.3 Mixer measurement

The initial version of the subharmonic mixer (without metal air-bridges) was measured when V_{gs} was biased at the Dirac point $V_{gs} = V_{dirac}$. The measured CL is 34 ± 3 dB at 190 - 210 GHz to 210 GHz frequency range with 10 dBm LO pumping power and the overall minimum CL is 31.5 dB at 190 GHz, as shown in Fig 5.9. The center frequency appears shifted to lower frequency, and this possibly because of tolerances in the circuit dimensions and substrate thickness. The measured IF output power for different RF input powers presented in Fig. 5.10 confirms the linear operation regime of the mixer at f_{RF} = 190 GHz.

Fig. 5.11 demonstrates the normalized conversion loss versus gate bias voltage at 200 GHz RF frequency. As can be seen, the mixer performance is strongly dependent on DC gate bias point and the CL increases 6 dB when deviating ±1 V

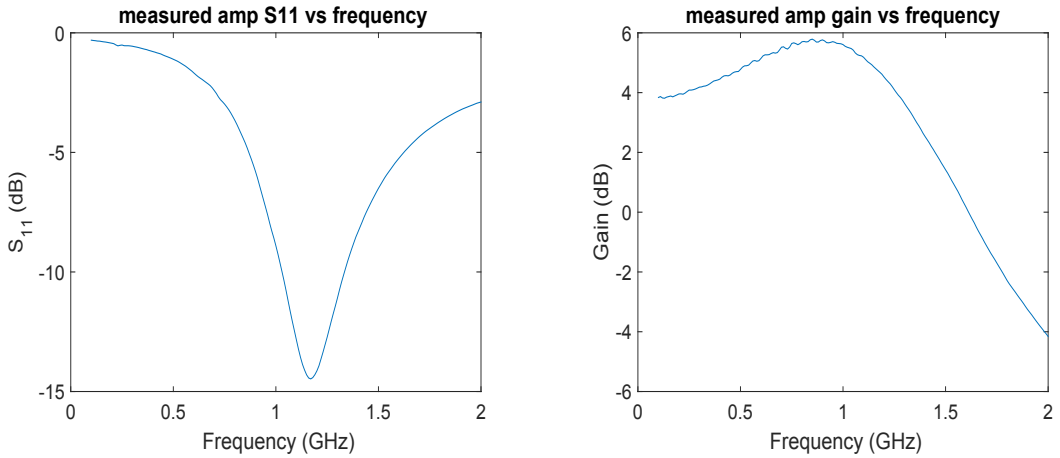

Figure 5.8: Measured a) S_{11} and b) power gain for the small signal amplifier.

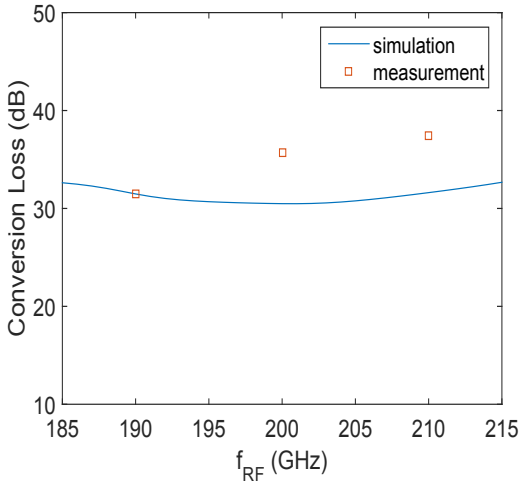

Figure 5.9: Mixer Conversion loss vs. f_{RF} at $P_{LO} = 10$ dBm, $f_{IF} = 1$ GHz.

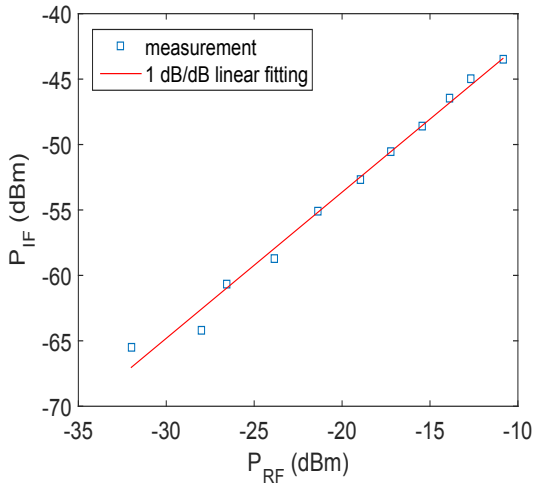

Figure 5.10: P_{IF} vs. P_{RF} at $f_{RF} = 190$ GHz, $V_{gs} = V_{dirac}$ and $P_{LO} = 10$ dBm.

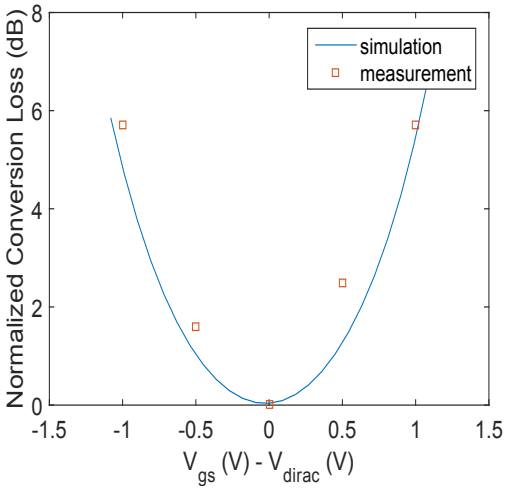

Figure 5.11: Conversion loss vs. V_{gs} at P_{LO} = 10 dBm and f_{RF} = 200 GHz.

Table 5.5: Comparison of G-FET subharmonic Mixer with Other Resistive Mixer

	[76]	[77]	[78]	[79]	[75]
RF (GHz)	180 - 220	130 -180	200 - 230	240	190
Technology	CMOS (bulk)	CMOS (SOI)	G_aA_s mHEMT	Schottky diode	G-FET
Order	1	1	2	2	2
CL (dB)	22 - 25	12 - 13	9 - 11	9	31.5
P_{LO} (dBm)	-2.8	3	1.5	5.5	10

from V_{dirac}. Reason behind is the utilisation of symmetrical transfer characteristic of G-FET. Besides, ± 2 dB uncertainty could appears due to the unstability of G-FET and the V_{dirac} might drift ± 0.4 V during measurements. The mixer performance comparison among this work and previous graphene-based implementations are presented in Table 5.4. As shown in the table, the previous graphene based mixer work are either operating below 30 GHz or present a relative bad mixing performance. A breakthrough of 7-fold improvement in operating frequency and a significant (>30 dB) performance improvement [74] is achieved in our mixer work, with which the potentiality of graphene based THz mixer is demonstrated.

The comparison among the GFET based mixer and other resistive mixer are demonstrated in Table 5.5. Despite the performance of our mixer is inferior compared with CMOS [76] and III-V technology [79], the CVD transfer method make graphene based technology promising for flexible electronics.

5.2.4 Receiver circuit measurement

The measured CL of the integrated receiver circuits is higher than 60 dB, which is far away from the receiver CL estimation calculated from the break-out mixer and amplifier results, i.e., 34 ± 3 dB - 6 dB = 28 ± 3 dB.

Based on the DC measurements of the individual devices and the air-bridges, the DC-current flows properly throughout the receiver circuit. Therefore the MIM capacitor is not shorted, and the poor performance of the receiver is probably due to the mixer and/or amplifier. In order to get a lower CL of the receiver circuit, both the mixer and the amplifier devices should operate properly. Separate amplifiers, mixers were fabricated and measured, respectively. The number of separate amplifiers with high power gain also follows the DC measurement results, i.e., devices with high transconductance exhibited high power gain. Only the number of low CL mixer are much lower than that of the mixer GFETs with good DC characteristics. Hence, it was hard to find a pair of well-operating mixer and amplifier in one receiver circuit, and the most probable reason for the measured poor receiver CL is the low-yield of the mixer.
According to the break-out mixers measurement results, a GFET with poor DC characteristics gives more than 50 dB CL. Besides, a poor amplifier will not amplify but attenuate the signal which degrades the receiver conversion loss by 10 dB. Moreover, as discussed above, both the mixer and the amplifier are strongly dependent on the DC bias condition, which is quite difficult to control when measuring the receiver circuit due to the dirac point possible shifting of both GFETs.
Of course, in order to verify the cause of the problem, further investigation need to be done and more separate measurements of the different parts of the integrated receiver circuit are necessary.

6
Conclusions and future work

6.1 Conclusions

A 200 GHz subharmonic resistive mixer and a microwave amplifier based on GFETs are presented in this thesis. This resistive mixer is designed to convert 200 GHz to 1 GHz with LO frequency of 100.5 GHz, and the small-signal amplifier is operating at 1 GHz. A large-signal GFET model is studied and implemented in mixer and amplifier design and performance estimation. An array of bow-tie structured graphene is applied in the G-FET channel of the mixer device in order to obtain simultaneously a more suitable impedance level as well as a higher current on-off ratio. All GFETs in the circuit are fabricated by CVD graphene, and the IC is realised in CPW technology on a 100 μm high resistive silicon substrate with several metal air-bridges. The first version of integrated receiver circuit is also fabricated. The amplifier power gain is measured to be 6 dB at 1GHz, and the CL over the RF frequencies from 190 to 210 GHz is measured to be 34 dB $\pm$ 3 dB and overall minimum CL is 31.5 dB at 190 GHz and 10 dBm LO power. A breakthrough of 7-fold frequency improvement as well as a significant (>30 dB) performance improvement is present compared to previously reported graphene based mixers.

6.2 Future work

Further improvement of the GFET based mixer is required firstly. Besides, due to the poor performance of the first version of the fabricated integrated receiver circuit, following investigation should be continues. Furthermore, due to the potentiality of CVD graphene based flexible electronics, graphene based flexible electronics also attracts great attention and it's worth to be focused on in the future.

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Paper A

A 200 GHz CVD Graphene FET Based Resistive Subharmonic Mixer

Y. Zhang, M. A. Andersson, and J. Stake

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