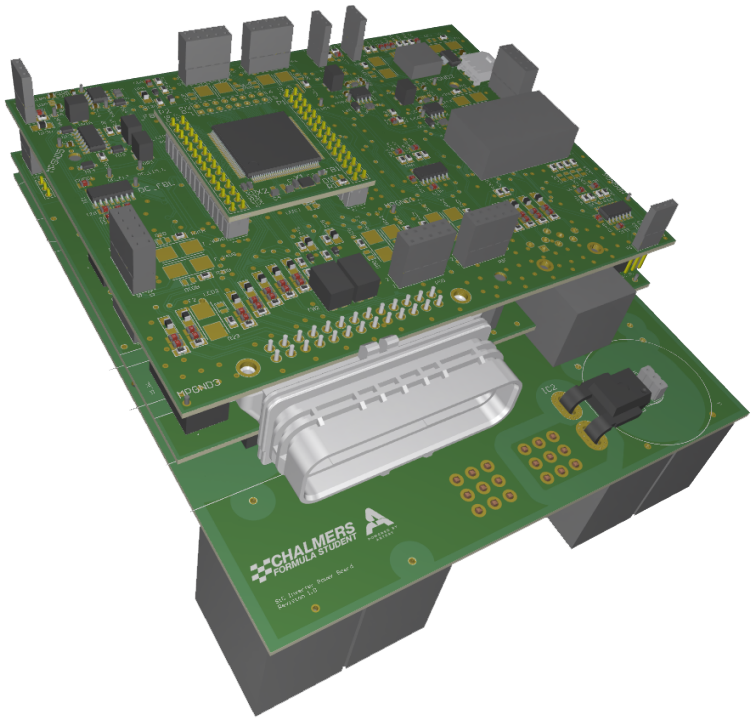
CHALMERS
UNIVERSITY OF TECHNOLOGY



Design and verification of a SiC voltage source inverter for Chalmers Formula Student

Master's thesis in Electric Power Engineering & Systems, Control and Mechatronics

Alexander Andersson
Marcus Kaveh Vencel

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2020

Master's thesis

Design and verification of a SiC voltage source inverter for Chalmers Formula Student

Alexander Andersson
Marcus Kaveh Vencel

CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
Gothenburg, Sweden 2020

Design and verification of a SiC voltage source inverter
for Chalmers Formula Student
Alexander Andersson
Marcus Kaveh Vencel

Supervisor: Axel Andalen & Anton Johansson, ABTERY AB
Examiner: Stefan Lundberg, Electrical Engineering

Master's Thesis Department of Electrical Engineering
Division of Electrical Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Typeset in LaTeX

Design and verification of a SiC voltage source inverter for Chalmers Formula Student

Alexander Andersson
Marcus Kaveh Vencel
Department of Electrical Engineering
Chalmers University of Technology

Abstract

In this report a 34 kW silicon carbide voltage source inverter for a traction motor is designed, built and verified. The intended application is for usage in a Formula Student car to drive a motor with severe high frequency harmonics. Thus, the two main design goals for this project were to increase the switching frequency and reduce the volume (and by extension also the mass) compared to a reference solution used by Chalmers Formula Student.

The design considerations that will be discussed in this report include switch selection, DC-link capacitor selection, gate driver selection as well as phase current sensor selection. Additionally, to remove the need for any high voltage, high current fuses a novel overcurrent protection circuit will be discussed and analysed. This is important since it contributes to a lower volume, whilst remaining compliant with the Formula Student ruleset.

The resulting prototype inverter ended up being 77 % smaller in volume resulting in a power density of 22 kW/l. With some simple modifications to the design, further improvements could result in a total volume reduction of almost 90 % and a power density of 49 kW/l.

The data collected during testing shows that the predicted case temperature matches the measured case temperature to withing ± 2.7 °C. This indicates that the thermal modelling techniques used are accurate.

Keywords: SiC, silicon carbide, power density, harmonics, inverter, VSI.

Acknowledgements

We would like to thank René Lause and Erik Lund in our sister group that worked on their master's thesis in parallel to us. Being able to discuss ideas and problems with more people was very helpful. Working towards a common goal also gave the thesis a higher purpose which improved working morale.

We would also like to thank our supervisor Stefan Lundberg at Chalmers for his dedication, support, great knowledge and highly detailed reports. Without his help, this thesis would most likely not have been successful.

Additionally, we would like to thank Vincotech and Morten Rabæk Kjær for supplying us with two SiC power modules for testing.

Last but not least, we would like to thank ABTERY AB for believing in us and giving us the opportunity to work on this thesis with their support. In particular, Axel Andalen and Anton Johansson at ABTERY have been very helpful by agilely supporting us when we needed it.

Alexander Andersson and Marcus Kaveh Vencel, Gothenburg, June 2020

Contents

List of Figures

List of Tables

Acronyms

AC	Alternating Current. 1
CFS	Chalmers Formula Student. 1–3, 26, 27, 58
CSI	Current Source Inverter. 3
DC	Direct Current. 1
ESD	Electro-static discharge. 61
EV	Electric Vehicle. 1
FSG	Formula Student Germany. 37, 54
IC	Integrated Circuit. 37, 38, 40, 41, 61
IGBT	Insulated-Gate Bipolar Transistor. 1–3, 11–14, 19, 21, 26, 27, 30, 31, 34, 67
MOSFET	Metal Oxide Semiconductor Field Effect Transistor. 1–3, 7, 8, 10–14, 19, 21, 23, 24, 26, 28, 36–39, 41, 42, 55, 58, 61, 68
MPF	Metallized Polypropylene Film. 46, 47, 62, 64
PCB	Printed Circuit Board. 25, 55, 59–62
PMSM	Permanent Magnet Synchronous Motor. 1, 27
PWM	Pulse Width Modulation. 3–5, 41, 66
RMS	Root Mean Square. 10, 15, 26, 29
Si	Silicon. 1, 2, 19, 26
SiC	Silicon Carbide. 1, 2, 19, 21, 26, 31, 34, 67
SPWM	Sinusoidal Pulse Width Modulation. 3, 4, 6, 7, 11, 14
SVPWM	Space Vector Modulation. 3, 7

THD	Total Harmonic Distortion. 15, 16, 27, 66, 67
THI-PWM	Third Harmonic Injection Pulse Width Modulation. 3, 6, 7, 14
VSI	Voltage Source Inverter. 2–4, 11, 14, 15, 21, 58

Symbols

Symbol	Description	Unit
$A_{\mathbf{m}}$	Amplitude of the injected third harmonic when using THIPWM.	-
$A_{\mathbf{sw,off}}$	MOSFET turn-off switching losses fitting constant.	-
$A_{\mathbf{sw,on}}$	MOSFET turn-on switching losses fitting constant.	-
$B_{\mathbf{sw,off}}$	MOSFET turn-off switching losses fitting constant.	-
$B_{\mathbf{sw,on}}$	MOSFET turn-on switching losses fitting constant.	-
$C_{\mathbf{GD}}$	MOSFET gate-drain capacitance.	F
$C_{\mathbf{GS}}$	MOSFET gate-source capacitance.	F
$E_{\mathbf{rr}}$	Reverse recovery energy.	J
$I_{\mathbf{D}}$	Drain current	A
$R_{\mathbf{Gext}}$	External gate resistance	Ω
$R_{\mathbf{G}}$	Total gate resistance	Ω
$R_{\mathbf{on}}$	MOSFET on resistance	Ω
$V_{\mathbf{DSon}}$	MOSFET on state voltage drop	V
$V_{\mathbf{GG}}$	Gate driver voltage	V
$V_{\mathbf{GS}}$	MOSFET gate-source voltage	V
$V_{\mathbf{th}}$	MOSFET threshold voltage	V
$f_{\mathbf{1}}$	Fundamental frequency	Hz
$f_{\mathbf{sw}}$	Switching frequency	Hz
$r_{\mathbf{G}}$	Internal gate resistance	Ω

1

Introduction

In the project Chalmers Formula Student (CFS), students from different backgrounds at Chalmers work together to design, manufacture and test a formula type car every year. The results of the efforts made by CFS 2019 can be seen in Figure 1.1. Since 2015 when CFS made their first Electric Vehicle (EV) the Permanent Magnet Synchronous Motor (PMSM) as well as the power electronics converting the Direct Current (DC) from the battery to Alternating Current (AC) powering them has been sponsored by Aros Electronics AB. However, due to unwanted harmonics in the PMSM, the current power electronics cannot switch quick enough to ensure full control of the currents at all times.

Figure 1.1: Chalmers Formula Student 2019 race car in action.

Over the last few years, Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have started to see more use to replace the traditional Silicon (Si) Insulated-Gate Bipolar Transistors (IGBTs). SiC MOSFETs enable higher switching frequencies and higher efficiencies with smaller size due to their properties [3]. All of these properties are highly desired in racing applications, and thus they provide a solid foundation to make a new inverter for CFS that is both lighter and smaller, and possibly more efficient.

1.1 Aim

The aim of this thesis is to design and verify a SiC MOSFET based Voltage Source Inverter (VSI) to be used with the CFS motors. The inverter should be smaller and lighter than the previous solution, as well as be capable of a switching frequency of at least 50 kHz.

1.2 Scope

In this project all the electrical hardware needed for the VSI will be designed. However, not all of the hardware will be covered in this thesis due to the limited academic value of some aspects of the design. Also, the control system software will not be derived as part of this thesis. Instead the control system software will be developed in a different thesis [4].

The VSI will be water-cooled but the cooling plate will not be designed as part of this thesis. To further limit the scope, a SiC MOSFET module will be used instead of discrete components to reduce the risk of introducing additional stray inductance in the design.

The designed inverter will be compared to what CFS is currently using, the Aros Electronics HPC-HTDFS.

1.3 SiC MOSFETs and sustainability

Given that SiC MOSFETs has lower switching losses there is potential for a reduction in energy consumption in many applications that are predominately using Si IGBT based solutions today. This would have a positive impact on both economic and environmental sustainability, at least in a scenario where all other parameters are kept constant. Efficiency gains in electric vehicles will lead to a lower energy use while operating the vehicle, but could also have other positive knock-on effects. For instance, the battery size could be reduced while maintaining the same range which means that less minerals are needed for production. Or if the battery size is kept the same then an increase in range can instead help with acceptance and adoption of electric vehicles as a replacement for internal combustion engine vehicles.

One other potential advantage with SiC MOSFETs is that the switching frequency can for some applications be pushed above the human audible limit to remove noise and whine, which could help with acceptance in emerging technologies such as electrified vehicles. This could have a small positive impact on sustainability in general as one small piece of a much larger puzzle in a world that moves away from fossil fuels.

2

Voltage source inverter

As the name suggests, a VSI is an inverter that uses a voltage source as an input. An alternative is the Current Source Inverter (CSI) which instead uses a current source as an input [5]. Since the CFS car uses a battery as its power source, a VSI will be used in this thesis. The overview of a VSI is shown in Figure 2.1. The control system is derived from a model of the motor and can be implemented in a variety of ways discussed in [4]. This control system then sends a voltage request to the microcontroller. The microcontroller then sends the corresponding Pulse Width Modulation (PWM) signal to the gate driver circuit, whose main function is to boost the PWM signal from the microcontroller since it is not powerful enough to drive the gates directly. A gate driver circuit can also contain additional circuits as will be described later, such as overcurrent protection. The PWM signal then controls the switches such that a controlled request voltage is output. To close the loop, the output current is then measured and fed back into the control system where a new voltage request is prepared.

The following section of the report contains the most important theoretical knowledge required to make an inverter. Many of the equations presented are related to predicting the temperature of various components, which are used in an attempt to choose the smallest possible components whilst still being able to guarantee that those components will always operate under safe conditions. The switch selection has a particular big impact on the size of the inverter, and thus that is an area of focus. Choosing the optimal switch is made complicated by the fact that MOSFETs and IGBTs can endure different amounts of stress depending on what type of load they are exposed to, and how well they are cooled. Thus, the manufacturer's specified current rating is not enough to make an optimal decision. This is explored in the coming section, along with DC-link capacitor theory and overcurrent protection.

2.1 Switching patterns

For a VSI, several different patterns for turning the switches on and off can be used to generate the desired voltage. The most common methods are Sinusoidal Pulse Width Modulation (SPWM), Third Harmonic Injection Pulse Width Modulation (THI-PWM) and Space Vector Modulation (SVPWM), which will be described in

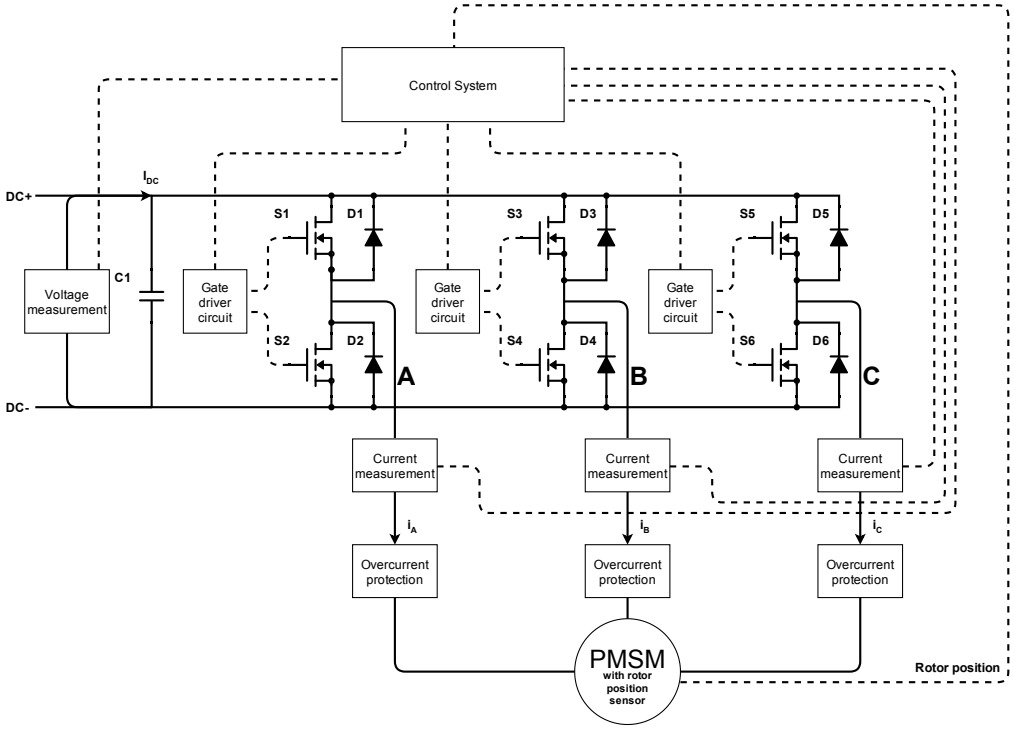


Figure 2.1: Overview of all parts in an inverter together with a PMSM.

the coming sections.

2.1.1 Sine Pulse Width Modulation

One way to control the VSI switches is by use of SPWM. The PWM signal is generated by comparing a triangular wave with the requested voltage, a reference sine wave, where the triangle wave has the frequency as the switching frequency f_{sw} and the reference sine wave has the same frequency as the fundamental of the desired output of the inverter, f_1. As is shown in [6] the references for the three phases can then be described as

$$\begin{aligned} U_{\text{ref,a}}(t) &= M\sin(\omega t) \\ U_{\text{ref,b}}(t) &= M\sin(\omega t - 120\ ^\circ) \\ U_{\text{ref,c}}(t) &= M\sin(\omega t + 120\ ^\circ) \end{aligned} \tag{2.1}$$

where:

$U_{\text{ref,x}}$	is the reference for each of the phase voltages,
M	is the modulation index,
ω	is the angular frequency [rad/s],
t	is the time [s].

If the maximum phase voltage occurs when the reference is 1, and by letting the reference vary between 0 and 1, the modulation index can be described as

$$M = \frac{\sqrt{2}U_{\mathrm{s}}}{U_{\mathrm{DC}}} \text{ for } U_{\mathrm{s}} \leq \frac{U_{\mathrm{DC}}}{\sqrt{2}} \tag{2.2}$$

where:

U_{s}	is the desired RMS phase to neutral voltage,
U_{DC}	is the input DC voltage.

The result of a PWM signal is shown in Figure 2.2. For illustration purposes f_{sw} has been set very low. The signal is then sent to the gates of the switches to turn them on and off. When the signal is 1 the upper switch in the phase leg is turned on, and when the signal is 0 the lower switch is on.

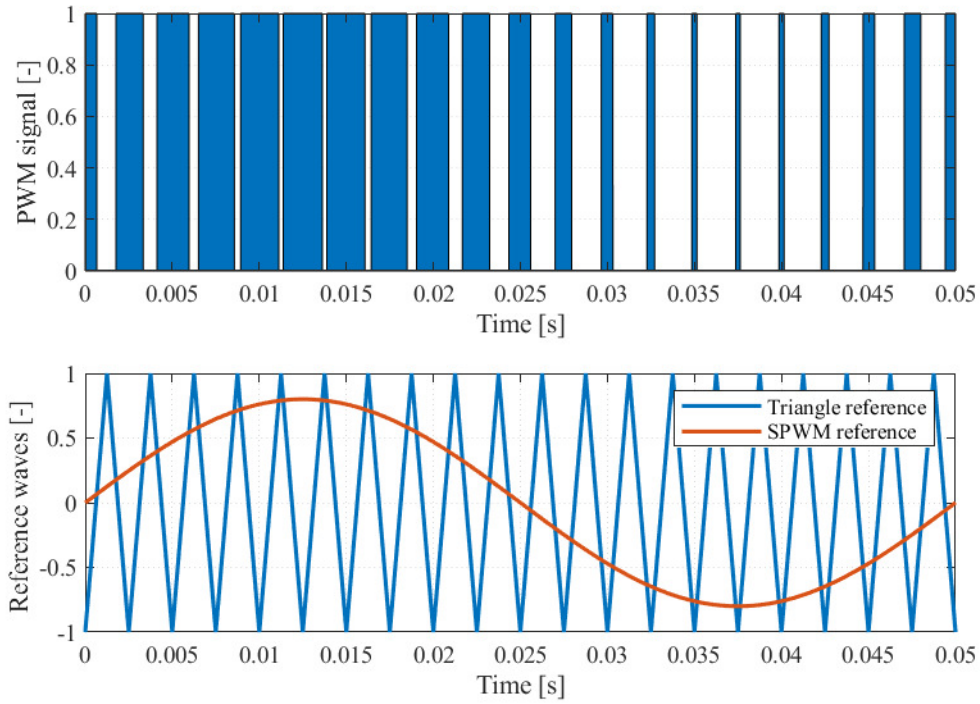


Figure 2.2: The top plot shows the SPWM-signal that is generated by comparing the two signals in the lower plot.

An advantage with this method is that it is simple to implement and realise on a microcontroller.

2.1.2 Third Harmonic Injection Pulse Width Modulation

Another modulation technique that is commonly used is THI-PWM. This technique is the same as SPWM, but has a sinusoidal with a injected third harmonic with the amplitude A_{m} superimposed onto it. Then the references can be described as

$$\begin{aligned} U_{\mathrm{ref,a}}(t) &= M\Big(\sin(\omega t) + A_{\mathrm{m}}\sin(3wt)\Big) \\ U_{\mathrm{ref,b}}(t) &= M\Big(\sin(\omega t - 120\ ^\circ) + A_{\mathrm{m}}\sin(3\omega t)\Big) \\ U_{\mathrm{ref,c}}(t) &= M\Big(\sin(\omega t + 120\ ^\circ) + A_{\mathrm{m}}\sin(3\omega t)\Big). \end{aligned} \tag{2.3}$$

If the load does not have a neutral point connected (i.e. the neutral point is floating), the third harmonic component disappears in the load without distorting the current [6]. This also means that A_{m} can be chosen freely. However, to limit torque ripple in electrical machines, $A_{\mathrm{m}} = \frac{1}{4}$ is commonly used [6][7].

An example switching signal is shown in Figure 2.3. The third harmonic can be seen in the reference signal and when compared to Figure 2.2 a slight increase in on-time of the switches can be noticed.

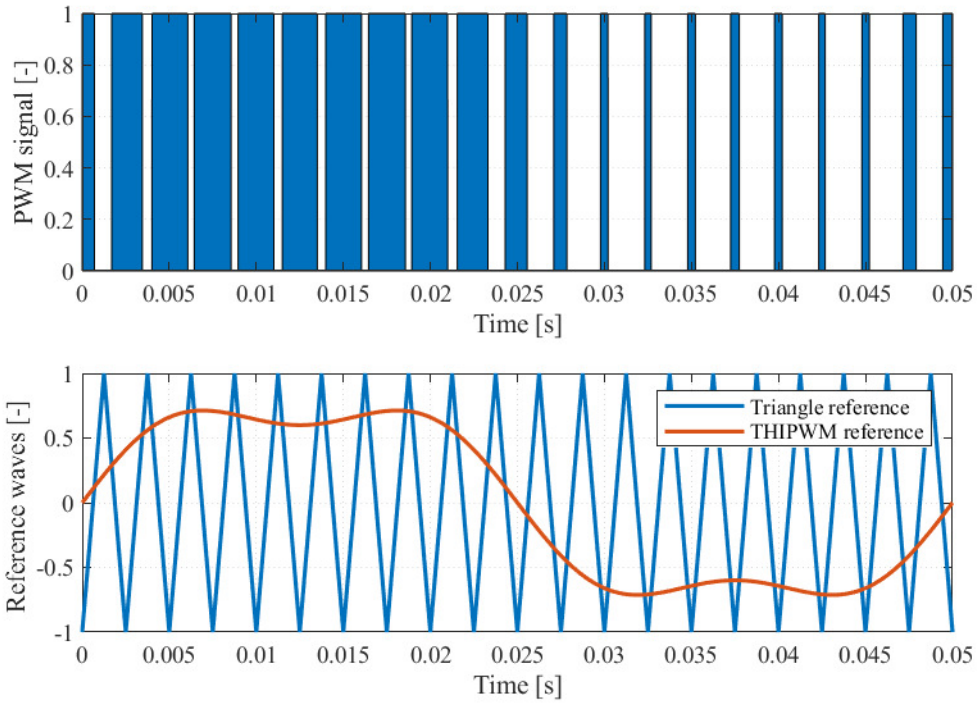


Figure 2.3: The upper plot shows the resulting THI-PWM signal output when comparing the two reference signals in the lower plot.

When using THI-PWM, the maximum modulation index can be described as in [6] to be

$$M_{\max} = \frac{1}{8A_{\mathrm{m}}} \left(\frac{12A_{\mathrm{m}}}{1+3A_{\mathrm{m}}} \right)^{\frac{3}{2}}. \tag{2.4}$$

If $A_{\mathrm{m}} = \frac{1}{4}$ is used, this leads to that the maximum phase voltage can be described as

$$U_{\mathrm{p,max,3}} = 1.12\frac{U_{\mathrm{DC}}}{\sqrt{2}}. \tag{2.5}$$

Similar to SPWM, this method is also easy to implement on a microcontroller, but has the additional benefit of being able to output a higher voltage.

2.1.3 Space vector modulation

According to [8] SVPWM and THI-PWM have very similar properties. SVPWM is however more difficult to implement on a microcontroller and will therefore not be investigated further.

2.1.4 Sampling of the phase currents

The sampling of the phase currents ties in closely with the switching frequency. It is recommended to sample at the peaks of the triangular reference signal that is shown in figures 2.2 and 2.3. Therefore the measurement will be done after any noise caused by turn-on and turn-off has stopped. This means that the sampling can be performed twice every switching period, which would result in a sampling frequency that is two times the switching frequency.

Furthermore, there is relationship between the bandwidth of the current controller and the sampling frequency to ensure that the steps controller is not too rough. This means that the sampling frequency should be at least 20 times the bandwidth, which in turns means that the switching frequency should be at least 10 times the bandwidth [9].

2.2 MOSFET turn-on and turn-off

To explain the turn-on and turn-off of the MOSFET, a more detailed model is required. The MOSFET model includes additional parasitic capacitance between the different pins as can be seen in Figure 2.4 together with the internal gate reistance r_{G}. The MOSFET is also modelled with a dependant current source, I_{D}, where I_{D} depends on V_{GS}. Any stray capacitance and inductance caused by the packaging of the MOSFET has been excluded. In Figure 2.4 the external gate resistance R_{Gext} and the voltage source V_{GG} representing the gate driver circuit are also shown. The gate driver is used to turn the MOSFET on and off and boost the signals from the microprocessor.

During turn-on and turn-off, there are four different stages that the MOSFET goes through. An example plot of this can be seen in Figure 2.5. Assuming there is

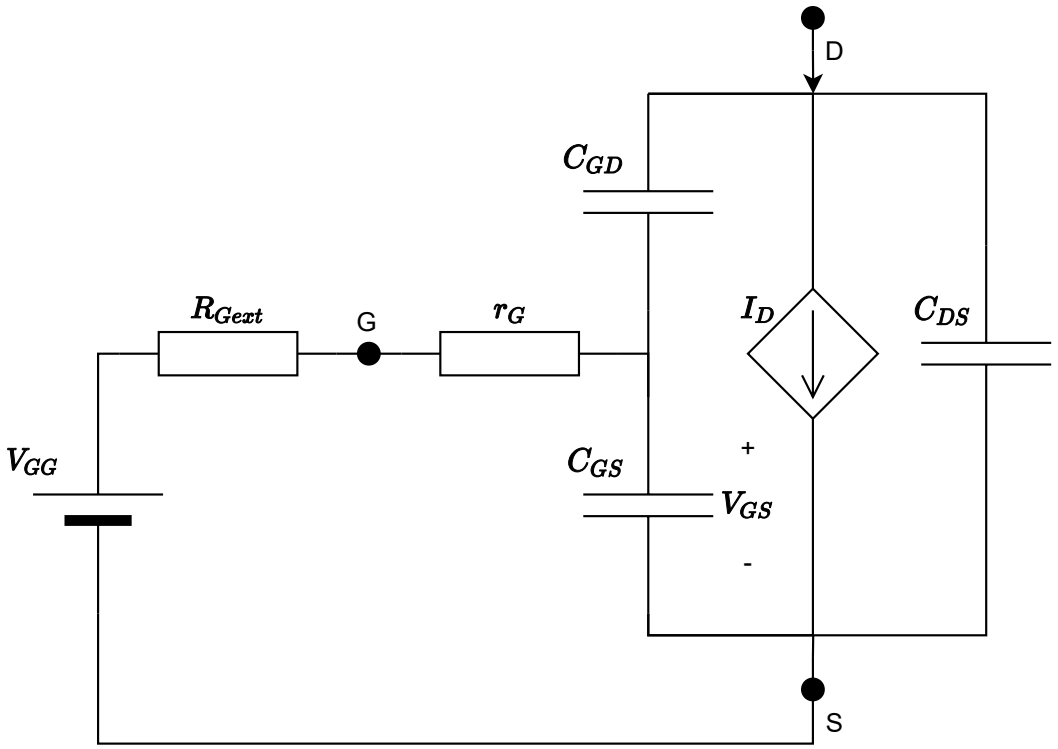


Figure 2.4: A more detailed model of a MOSFET including the three parasitic capacitors C_{GS}, C_{GD} and C_{DS} as well as the internal gate resistance r_{g}, external gate resistance R_{Gext} and the gate driver voltage V_{GG}.

already a current flowing in the system through the anti-parallel diode of the other switch in the same phase leg, I_0, during the first stage, T_1, the gate voltage V_{GS} rises to the threshold voltage V_{th} during what is called the turn-on delay time. During the second part, T_2 V_{GS} has reached V_{th} and the MOSFET is in the active region of operation. Now the drain current I_{D} will start increasing according to

$$I_{\mathrm{D}} = g_{\mathrm{m}}(V_{\mathrm{GS}} - V_{\mathrm{th}}) \tag{2.6}$$

until it reaches I_0. The transconductance g_{m} is used to describe the relationship between I_{D} and V_{GS}. It is described as

$$g_{\mathrm{m}} = \frac{\Delta I_{\mathrm{D}}}{\Delta V_{\mathrm{GS}}}. \tag{2.7}$$

When the MOSFET carries the entire current and V_{GS} has reached the so called Miller Plateau where

$$V_{\mathrm{GS,Miller}} = V_{\mathrm{th}} + \frac{I_{\mathrm{D}}}{g_{\mathrm{m}}}. \tag{2.8}$$

Up until this point V_{GS} has increased according to

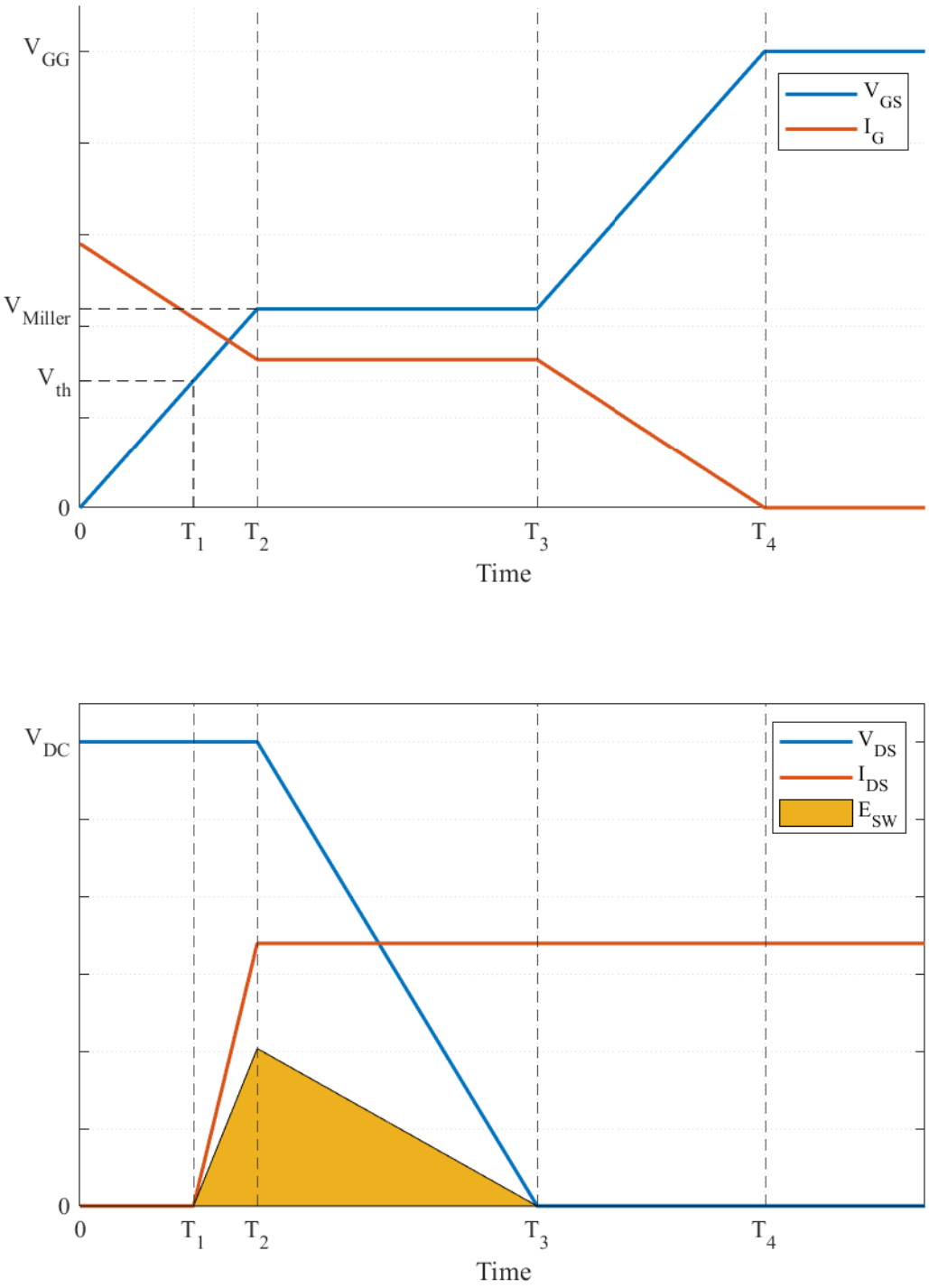


Figure 2.5: Typical idealised turn-on characteristic for MOSFETs divided into 4 distinct periods. A linear representation of the slopes are used since the difference is minimal. The area highlighted in yellow represents the switch loss energy during one turn-on cycle.

$$V_{\mathrm{GS}} = V_{\mathrm{GG}}(1 - e^{-t/\tau_1}) \tag{2.9}$$

exponentially as C_{GD} and C_{GS} has been charged through the total gate resistance $R_{\mathrm{G}} = R_{\mathrm{Gext}} + r_{\mathrm{G}}$ with the time constant $\tau_1 = R_{\mathrm{G}}(C_{\mathrm{gs}}+C_{\mathrm{gd}})$ [5]. After the MOSFET is fully turned on, the voltage over it will start dropping to V_{DSon}. This time period can be calculated as

$$T_3 = R_{\mathrm{G}} C_{\mathrm{GD}} \frac{V_{\mathrm{DC}} - I_{\mathrm{D}} R_{\mathrm{On}}}{V_{\mathrm{GG}} - V_{\mathrm{GS}}}. \tag{2.10}$$

After the voltage has dropped to V_{DSon} the switch is properly turned on and the gate voltage will keep increasing until it reaches the driver voltage after a time, T_4. When the MOSFET is later turned off, a similar switching pattern is seen and thus it can be described in the same way as the turn-on but reversed. However, it is possible to utilize a different external gate resistance, R_{Gext} and through that change the timings [10].

2.3 Power losses in IGBTs and MOSFETs

The biggest losses in the inverter will be those in the switches and therefore they need to be calculated, both to know the efficiency of the inverter, but also to dimension the switches used so that they do not overheat. This knowledge can also be used to determine which maximum switching frequency the inverter can operate at as well.

As shown in [5], the losses in an IGBT can be divided into two major parts: switching losses and conduction losses. The switching losses can be calculated as

$$P_{\mathrm{sw}} = f_{\mathrm{sw}}(E_{\mathrm{on}} + E_{\mathrm{off}}) \tag{2.11}$$

where

E_{on} & E_{off}	is the energy during gate turn-on and turn-off,
f_{sw}	is the frequency at which the gates switch.

The conduction losses can be calculated from the Root Mean Square (RMS) current and the on-state resistance of the MOSFET:

$$P_{\mathrm{con}} = R_{\mathrm{On}} I_{\mathrm{rms}}^2 \tag{2.12}$$

where

R_{On} is the on-state drain to source resistance of the MOSFET,
I_{RMS} is the RMS current trough the MOSFET.

The on-state conduction losses for an IGBT can be further described as

$$P_{\mathrm{con,IGBT}} = v_{\mathrm{T}} I_{\mathrm{ce,AVG}} + R_{\mathrm{T}} I_{\mathrm{ce,RMS}}^2 \tag{2.13}$$

where

v_{T} is the on-state voltage drop of the IGBT,
R_{T} is the on-state resistance of the IGBT,
$I_{\mathrm{ce,AVG}}$ is the average collector emitter current,
$I_{\mathrm{ce,RMS}}$ is the RMS collector emitter current.

However, when SPWM is used the power loss is different since the switches in the phase legs share the load. In [6] it is shown how the losses in an IGBT can be calculated. Because IGBTs do not conduct in reverse, the losses are shared between the transistors and the anti-parallel diodes.

Thus the conduction losses in an IGBT can be written as

$$P_{\mathrm{con}} = P_{\mathrm{con,IGBT}} + P_{\mathrm{con,DIODE}} \tag{2.14}$$

$$P_{\mathrm{con,IGBT}} = \frac{v_{0\mathrm{T}}\hat{I}}{2\pi}[1 + \frac{\pi}{4} M \cos(\phi)] + \frac{r_{\mathrm{T}}\hat{I}^2}{2\pi}[\frac{\pi}{4} + \frac{2}{3} M \cos(\phi)] \tag{2.15}$$

$$P_{\mathrm{con,DIODE}} = \frac{v_{0\mathrm{D}}\hat{I}}{2\pi}[1 - \frac{\pi}{4} M \cos(\phi)] + \frac{r_{\mathrm{D}}\hat{I}^2}{2\pi}[\frac{\pi}{4} - \frac{2}{3} M \cos(\phi)] \tag{2.16}$$

where

v_{T} is the on-state voltage drop of the IGBT,
v_{D} is the on-state voltage drop of the anti-parallel diode,
R_{T} is the on-state resistance of the IGBT,
R_{D} is the on-state resistance of the anti-parallel diode,
ϕ is the phase shift of the current,
M is the modulation index,
$\hat{I}$ is the amplitude of the collector emitter current.

Because the current flow can be described in a similar way for a MOSFET based VSI. If the blanking time is neglected and because of the MOSFETs ability to conduct in reverse, the conduction loss for a MOSFET can be calculated in a similar way

to (2.14) with $R_{\mathrm{T}} = R_{\mathrm{D}} = R_{\mathrm{On}}$. However, since MOSFETs do not have a constant voltage drop ($V_{0\mathrm{T}} = V_{0\mathrm{D}} = 0$) the losses can be simplified to

$$P_{\mathrm{con,MOSFET}} = \frac{r_{\mathrm{DS,on}} I_{\mathrm{RMS}}^2}{2}. \tag{2.17}$$

According to [6] the switching losses for IGBTs can be described as

$$\begin{aligned} P_{\mathrm{sw,IGBT}} = &\frac{f_1 \hat{I} U_{\mathrm{DC}} A_{\mathrm{sw,on}}}{2} \left(\frac{1}{\theta} - \frac{M\pi}{4} [\theta \cos(\phi) + \sin(\phi)] \right) \\ &+ \frac{f_1 \hat{I} U_{\mathrm{DC}} A_{\mathrm{sw,off}}}{2} \left(\frac{1}{\theta} - \frac{M\pi}{4} [\theta \cos(\phi) - \sin(\phi)] \right) \end{aligned} \tag{2.18}$$

This can also be applied to MOSFETs because the same amount of switching is done. Therefore, the switching losses for the MOSFET can be described as

$$\begin{aligned} P_{\mathrm{sw,MOSFET}} = &\frac{f_1 \hat{I} U_{\mathrm{DC}} A_{\mathrm{sw,on}}}{2} \left(\frac{1}{\theta} - \frac{M\pi}{4} [\theta \cos(\phi) + \sin(\phi)] \right) \\ &+ \frac{f_1 \hat{I} U_{\mathrm{DC}} A_{\mathrm{sw,off}}}{2} \left(\frac{1}{\theta} - \frac{M\pi}{4} [\theta \cos(\phi) - \sin(\phi)] \right) \end{aligned} \tag{2.19}$$

$$\theta = \frac{\pi f_1}{2 f_{\mathrm{c}}} \tag{2.20}$$

where

$\hat{I}$	is the peak current trough the MOSFET,
U_{DC}	is the DC voltage,
M	is the modulation index,
f_1	is the fundamental frequency,
f_{c}	is the frequency of the carrier wave,
ϕ	is the phase shift of the current,
$A_{\mathrm{sw,on}}$&$A_{\mathrm{sw,off}}$	are the fitting constants.

The fitting constants $A_{\mathrm{sw,on}}$ and $A_{\mathrm{sw,off}}$ are used to give a good approximation of the switching losses through a curve fitting as described in [6] such that

$$E_{\mathrm{sw}} = A_{\mathrm{sw,on}} u_{\mathrm{DS}}(t) i^{B_{\mathrm{SW,on}}}(t) + A_{\mathrm{sw,off}} u_{\mathrm{DS}}(t) i^{B_{\mathrm{SW,off}}}(t). \tag{2.21}$$

If $B_{\mathrm{sw,on}}$ and $B_{\mathrm{sw,off}}$ are assumed to be 1 (which is shown to be a good approximation in [6]) then (2.21) simplifies to

$$A_{\mathrm{sw,on}} = \frac{E_{\mathrm{sw,on}}}{u_{\mathrm{DS}}(t) i_{\mathrm{D}}(t)}$$
$$A_{\mathrm{sw,off}} = \frac{E_{\mathrm{sw,off}}}{u_{\mathrm{DS}}(t) i_{\mathrm{D}}(t)}. \tag{2.22}$$

With third harmonic injection and by using the same logic as above, the losses in an IGBT can be described as

$$P_{\mathrm{con,IGBT,THI}} = \frac{v_{0\mathrm{T}}\hat{I}}{2\pi}\left(1 + \frac{\pi}{4}M\cos(\phi)\right) + \frac{r_{0\mathrm{T}}\hat{I}^2}{2\pi}\left(\frac{\pi}{4} + \frac{2}{3}M\cos(\phi) - \frac{2MA_{\mathrm{m}}}{15}\cos(3\phi)\right) \tag{2.23}$$

$$\begin{aligned} P_{\mathrm{sw,IGBT,THI}} = {} & \frac{f_1\hat{I}U_{\mathrm{DC}}A_{\mathrm{sw,on}}}{2}\left(\frac{1}{\theta} - \frac{M\pi}{4}[\theta\cos(\phi) + \sin(\phi)] + \frac{M^2A_{\mathrm{m}}\theta}{6}[\cos(2\phi) - \frac{\cos(4\phi)}{5}]\right) \\ & + \frac{f_1\hat{I}U_{\mathrm{DC}}A_{\mathrm{sw,off}}}{2}\left(\frac{1}{\theta} - \frac{M\pi}{4}[\theta\cos(\phi) - \sin(\phi)] + \frac{M^2A_{\mathrm{m}}\theta}{6}[\cos(2\phi) - \frac{\cos(4\phi)}{5}]\right) \end{aligned} \tag{2.24}$$

while the losses in a MOSFET can be described as

$$P_{\mathrm{con,MOSFET,THI}} = \frac{R_{\mathrm{On}}I_{\mathrm{RMS}}^2}{2} \tag{2.25}$$

$$\begin{aligned} P_{\mathrm{sw,MOSFET,THI}} = {} & \frac{f_1\hat{I}U_{\mathrm{DC}}A_{\mathrm{sw,on}}}{2}\left(\frac{1}{\theta} - \frac{M\pi}{4}[\theta\cos(\phi) + \sin(\phi)] + \frac{M^2A_{\mathrm{m}}\theta}{6}[\cos(2\phi) - \frac{\cos(4\phi)}{5}]\right) \\ & + \frac{f_1\hat{I}U_{\mathrm{DC}}A_{\mathrm{sw,off}}}{2}\left(\frac{1}{\theta} - \frac{M\pi}{4}[\theta\cos(\phi) - \sin(\phi)] + \frac{M^2A_{\mathrm{m}}\theta}{6}[\cos(2\phi) - \frac{\cos(4\phi)}{5}]\right) \end{aligned} \tag{2.26}$$

where

R_{On}	is the on-state resistance of the MOSFET,
$\hat{I}$	is the peak current trough the MOSFET,
U_{DC}	is the DC voltage,
M	is the modulation index,
f_1	is the fundamental frequency,
θ	is the electrical rotor angle,
ϕ	is the phase shift of the current,
A_{m}	is the third harmonic injection amplitude,
$A_{\mathrm{sw,on}}$&$A_{\mathrm{sw,off}}$	are the fitting constants.

2.3.1 Losses in anti parallel diodes

Additionally, when used, the losses in the anti-parallel diodes are significant. In an IGBT based VSI, when the voltage and current are discordant the anti-parallel diodes will conduct in reverse since the IGBT cannot conduct in reverse. However, the switching losses in a diode are very low, and thus only the reverse recovery losses are worth noting. Thus the losses using SPWM can be written as in [6]:

$$P_{\text{con,Diode}} = \frac{v_{0\text{D}}\hat{I}}{2\pi}\left[1 - \frac{\pi}{4}M\cos(\Phi)\right] + \frac{r_{0\text{D}}\hat{I}^2}{2\pi}\left[\frac{\pi}{4} - \frac{2}{3}M\cos(\Phi)\right], \tag{2.27}$$

$$P_{\text{sw,Diode}} = f_1\hat{I}U_{\text{DC}}A_{\text{rr}}\left(\frac{1}{\theta} - \frac{M\pi}{4}[\theta\cos(\phi) + \sin(\phi)]\right) \tag{2.28}$$

where A_{rr} is the fitting constant for the reverse recovery energy E_{rr}:

$$A_{\text{rr}} = \frac{E_{\text{rr}}}{u_{\text{DS}}(t)i_{\text{D}}(t)}. \tag{2.29}$$

When THI-PWM is used the losses are instead

$$P_{\text{con,Diode,THI}} = \frac{v_{0\text{D}}\hat{I}}{2\pi}\left(1 + \frac{\pi}{4}M\cos(\phi)\right) + \frac{r_{0\text{D}}\hat{I}^2}{2\pi}\left(\frac{\pi}{4} + \frac{2}{3}M\cos(\phi) - \frac{2MA_{\text{m}}}{15}\cos(3\phi)\right) \tag{2.30}$$

$$P_{\text{sw,Diode,THI}} = f_1\hat{I}U_{\text{DC}}A_{\text{rr}}\left(\frac{1}{\theta} - \frac{M\pi}{4}[\theta\cos(\phi) - \sin(\phi)] + \frac{M^2A_{\text{m}}\theta}{6}\left[\cos(2\phi) - \frac{\cos(4\phi)}{5}\right]\right) \tag{2.31}$$

2.3.2 Thermal network modelling

The losses in the MOSFETs need to be handled by means of cooling. This is done to make sure that the MOSFETs remain within rated temperatures. The thermal network model used in this project can be seen in Figure 2.6. With this model, the case temperature T_{c} can be predicted according to

$$T_{\text{c}} = 6P(R_{\text{ch}} + R_{\text{hw}}) \tag{2.32}$$

where

T_{c}	is the case temperature,
R_{ch}	is the case-to-heatsink thermal resistance,
R_{hw}	is the heatsink-to-water thermal resistance,
P	is the total steady-state power loss in one MOSFET,
T_{w}	is the coolant water temperature.

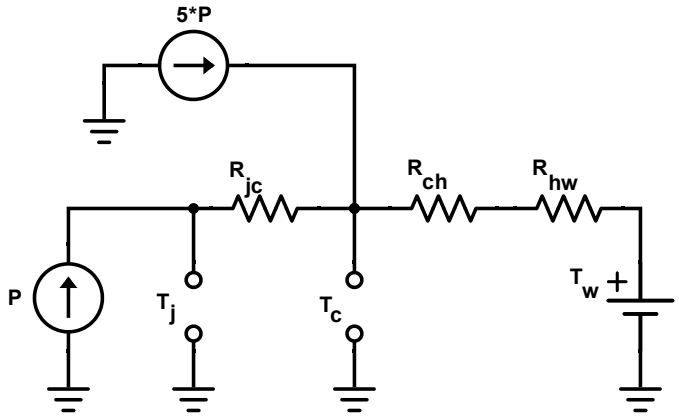


Figure 2.6: Thermal network of six MOSFETs at steady state with water cooling.

This is useful since for most power modules this is the only temperature that can be measured with the integrated temperature sensor (if there is one). One can also make predictions about the junction temperature T_j according to

$$T_\mathrm{j} = T_\mathrm{c} + P \cdot R_\mathrm{jc} = 6P(R_\mathrm{ch} + R_\mathrm{hw}) + P \cdot R_\mathrm{jc} \tag{2.33}$$

where

T_j is the junction temperature,
R_ch is the case-to-heatsink thermal resistance.

2.4 Total Harmonic Distortion and switching frequency selection

A useful tool for measuring the purity of the output of a VSI is to calculate the Total Harmonic Distortion (THD) of the currents. There exists two different versions of THD, one based on the fundamental of the signal, $\mathrm{THD_F}$ and another based on the RMS of the signal, $\mathrm{THD_R}$. In this thesis, $\mathrm{THD_F}$ will be used since $\mathrm{THD_R}$ can result in very large errors [11]. $\mathrm{THD_F}$ of the current I can be described as

$$\mathrm{THD_F} = \frac{\sqrt{\sum_{\mathrm{k}=2}^{\infty} I_\mathrm{k}^2}}{I_1} \tag{2.34}$$

where I_k could be either the RMS or the peak value of the harmonics of the current.

As has been shown, the switching losses of the VSI are proportional to the switching frequency, and for that reason it is desirable to have as low switching frequency as

possible to reduce the losses. However, it can also be shown that the switching frequency has an impact on the harmonics in the output currents of the inverter. As the switching frequency increases the harmonics become possible to control. Therefore, it is desirable to have a switching frequency of at least 20 times the fundamental frequency [12][6]. In the end, the choice of switching frequency becomes a trade-off between switching losses and lowering the THD.

2.5 Current and voltage ripple in DC-link capacitors

In order to dimension the capacitors in the DC-link some knowledge about the behavior of the currents and voltages in the inverter is required. The capacitors in the DC-link needs to handle the heat caused by any current flowing in and out of capacitor. In [13] the current ripple caused by the inductance L at a duty cycle d in a VSI is calculated as

$$\Delta I = \frac{d(1-d)U_{\mathrm{DC}}}{f_{\mathrm{sw}}L}. \tag{2.35}$$

Here it can be seen that the maximum ΔI is when the duty cycle is 0.5. This gives

$$\Delta I_{0.5\mathrm{t}} = \frac{U_{\mathrm{DC}}}{4f_{\mathrm{sw}}L}. \tag{2.36}$$

Furthermore the DC-link needs to protect the DC-supply from any harmful voltage ripple since this can cause over-voltage in it. In [13] this is shown to be calculated as

$$\Delta U_{0.5\mathrm{t}} = \frac{U_{\mathrm{DC}}}{32LCf_{\mathrm{sw}}^2} \tag{2.37}$$

which can be rewritten as

$$C = \frac{U_{\mathrm{DC}}}{32L\Delta U_{0.5\mathrm{t}}f_{\mathrm{sw}}^2}. \tag{2.38}$$

This shows that the higher the switching frequency, the lower capacitance is needed to keep the voltage ripple low.

Finally, in [14] it is shown that the RMS current stress of the capacitors can be estimated as

$$I_{\mathrm{C,RMS}} \approx \frac{I_{1,\mathrm{RMS}}}{\sqrt{2}}. \tag{2.39}$$

where:

$I_{\mathrm{C,RMS}}$ is the RMS current in the DC-link,
$I_{\mathrm{1,RMS}}$ is the RMS phase current.

2.6 Current measurement

For a functioning inverter it is for multiple reasons necessary to know the currents in the motor phases. One reason for this is that the control system uses that information for calculating the voltage reference. Another reason is that the information can be used to detect overcurrent events which in turn can be used to shut down the inverter to protect it and/or the motor from damage.

2.6.1 Topologies

For a VSI, a few different current sensing topologies can be implemented. Perhaps the most obvious one is to place a current sensor on at least two of the phase legs' outputs, which is sufficient given that $I_{\mathrm{a}} + I_{\mathrm{b}} + I_{\mathrm{c}} = 0$. Another possibility is to measure the bridge current in at least two of the half bridges. A third option is to measure the DC current going in to the inverter with a single sensor.

The first option is always possible to implement, but requires an isolated sensor solution because the common-mode voltage in the phases is equal to the DC-bus voltage. An advantage with this solution is that it is simple in the sense that no special care has to be taken to know the state of the currents (unlike the other two solutions).

The second option is not always possible to implement since some power modules only expose the DC-bus and the phase connections, meaning that the bridge current is kept internal to the power module. Another problem with this topology is that the current has to be sampled at specific time slots that depend on the current state of the switches [15]. The advantage with this solution is that the current can be measured with a constant reference to DC-, which is ideal for the shunt resistor option (see Section 2.6.2).

The third solution requires only one sensor, but does not provide all information about the current state of the phase currents on its own. To know the current state of the phase currents, the state of the switches needs to be taken into account. This increases complexity. An advantage with this solution is that similar to the bridge current topology the current can be measured with reference to DC-.

2.6.2 Current sensor options

Measuring current can be done in three fundamentally different ways.

- Ohm's law.

- Magnetic field around the conductor.
- The Faraday effect.

Out of these three, only the first two will be considered simply because no sensor utilising the Faraday effect for use in automotive applications was found.

Ohm's law can be used to calculate the current running through a resistor (which can be a shunt resistor, or a well known resistance of a PCB trace) according to

$$I = \frac{U}{R} \tag{2.40}$$

where

I is the sensed current,
U is the measured voltage drop across the resistor,
R is the resistance of the resistor.

A problem with this solution is that there is a balance between accuracy and power dissipation. If the resistance is very low, the resulting voltage signal will be very small and thus prone to disturbances. If the resistance is high then the voltage signal will be higher which makes it easier to measure it accurately, but the resistance is more likely to be affected by the additional heat dissipated in the resistor. Another property of this sensor type is that it is not naturally galvanically isolated, which means that design effort and additional components has to be put in if isolation is required.

For sensors utilising the magnetic field around a conductor there are two main types: hall effect sensors and current transformers. Hall effect sensors directly sense the magnetic field around a conductor and use that information to determine the current in the conductor. Current transformers work by having a coil wound around the conductor where a secondary current is induced according to Faraday's law. This means that current transformers cannot be used to measure DC current. It also means that current transducers are mainly current source devices, whereas hall effect sensors are voltage source devices. In practice a current transformer sensor is easily turned into a voltage source by letting the induced current create a voltage drop across a known resistor. Unlike the resistive type of sensors, magnetic field type of sensors are naturally galvanically isolated.

2.7 Overcurrent protection

Almost all electrical components have a maximum current carrying capability, where exceeding this limit will result in device failure and possibly damage to property and person. Therefore it is necessary to implement some form overcurrent protection for electrical devices. An overcurrent event is not necessarily as easy as defining a maximum current that can be sustained indefinitely. For example, the motor used

by CFS is designed with the intention of overloading it for short moments during heavy use (see Figure 2.7). The motor can do this because it has enough thermal mass that the temperature rise during an acceleration burst is kept within safe limits. This is typically not the case for semiconductor devices, which sometimes have such a low thermal mass that the maximum instantaneous current capability is similar to the maximum continuous current capability. For instance, in [16] it was found that some SiC MOSFET power modules fail after only as little as 3 µs of short circuit, whereas Si IGBT counterparts may handle a similar situation for up to 10 µs.

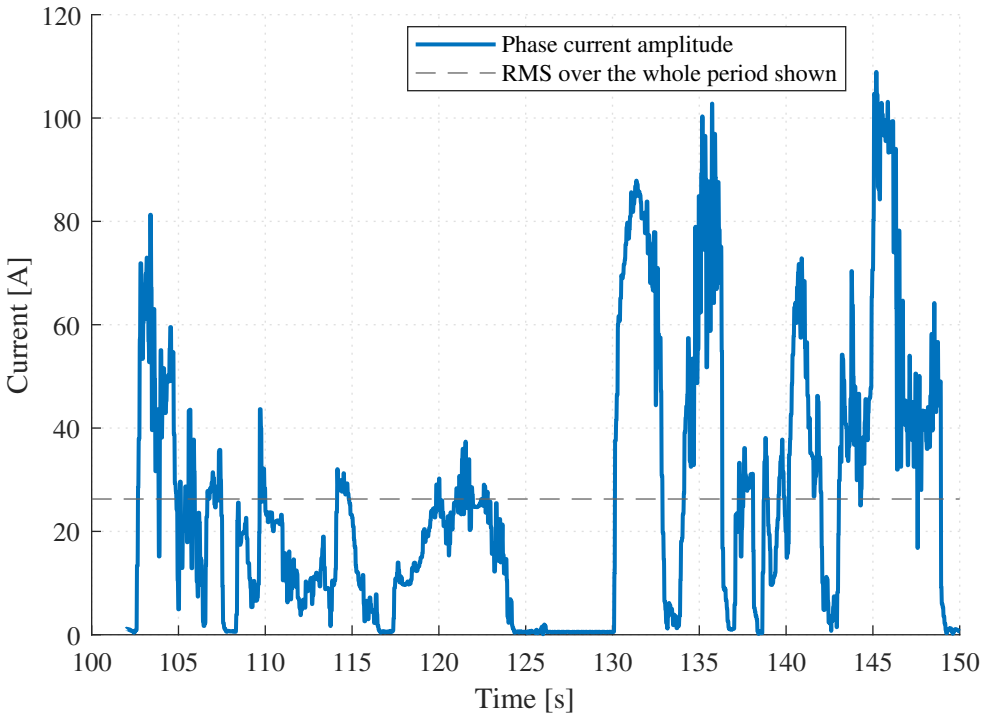


Figure 2.7: Current magnitude as well as RMS current in one phase over the whole period shown during an auto cross run by CFS in Aachen. Notice how the peaks are significantly higher than both the calculated RMS value, as well as the rated current of 48 A RMS [A.1].

Perhaps the most obvious danger in this project is an overcurrent event in the high current path (comprised by the DC-bus current, the bridge currents and the phase currents) since that is where most of the electrical power is exchanged. Some possible failure modes include:

- Shoot-through, which happens if both MOSFETs in a half bridge are turned on at the same time leading to a short-circuit. This can happen because of a signal fault to the gate driver or if one or more of the switches have failed short.

- Short circuit between the phases or to ground, for example due to mechanical failure of separation.

- Incorrect switching due to software faults, such as if the controller locks up in a state where at least two MOSFETs are turned on resulting in a high, uncontrolled DC-current.

- Excessive overload [1].

With a current sensor it would be possible to turn off the inverter through software in case of a detected over current event. This would be a lightweight and cheap solution since no additional components are needed (inclusion of a current sensing solution is already necessitated by the control system). Unfortunately this is not compliant with the Formula Student Germany rule set (see rule *EV 3.2.5* in [17]), and it is also harder to guarantee that the software will always react fast enough. Therefore, a hardware solution of some kind is necessary.

Two conventional hardware solutions for overcurrent protection are melt fuses and motor protection devices. A melt fuse is a type of device where the conductor melts or burns off in the event of overcurrent, thus stopping the flow of current through the device. This type of device is not desirable for a small and light inverter since it adds bulk. Another reason why fuses are not desirable is because they are single use (once they are broken, they cannot be reset but rather need to be replaced which is bad in terms of labour as well as sustainability [2]). If such a fuse breaks in a Formula Student car it would be rather difficult to change it since the housing for the inverter will be sealed during competitions. Motor protection devices solve this problem since they are resettable, typically through a mechanical push button. The problem with this type of device is that most commercially available products are meant for stationary industry applications and are designed to be mounted on a DIN-rail and not on PCBs. Motor protection devices typically include not only the over current detection, but also a circuit breaker which is triggered in case of a detected overcurrent event (which is not needed for this project since it is sufficient to drive the gates low to turn off the inverter). This makes them big and bulky, and thus not ideal for use in an automotive inverter. An advantage with both of these solutions is that they are proven and reliable.

Another possibility is to build an analog circuit that makes use of the pre-existing current sensing solution to detect an overcurrent event. Such a circuit would be ideal, since it would be easy to reset by power cycling the system (rather than replacing a physical component), and it could potentially be made to act faster than a fuse in short circuit events.

[1] While the motor Chalmers Formula Student uses is only rated for a continuous power of 13.5 kW, it can be overloaded at up to 32 kW for short periods of time. This is taken advantage of to allow the motor to be smaller and lighter. Therefore, excessive overload needs to be considered.

[2] As an example, it would be at best inconvenient and at worst dangerous if a car would stop on a highway due to a blown fuse without the possibility to reset any such faults. Therefore, it is the right choice to spend some time working on alternatives, both from an economic perspective as well as from an ethical perspective.

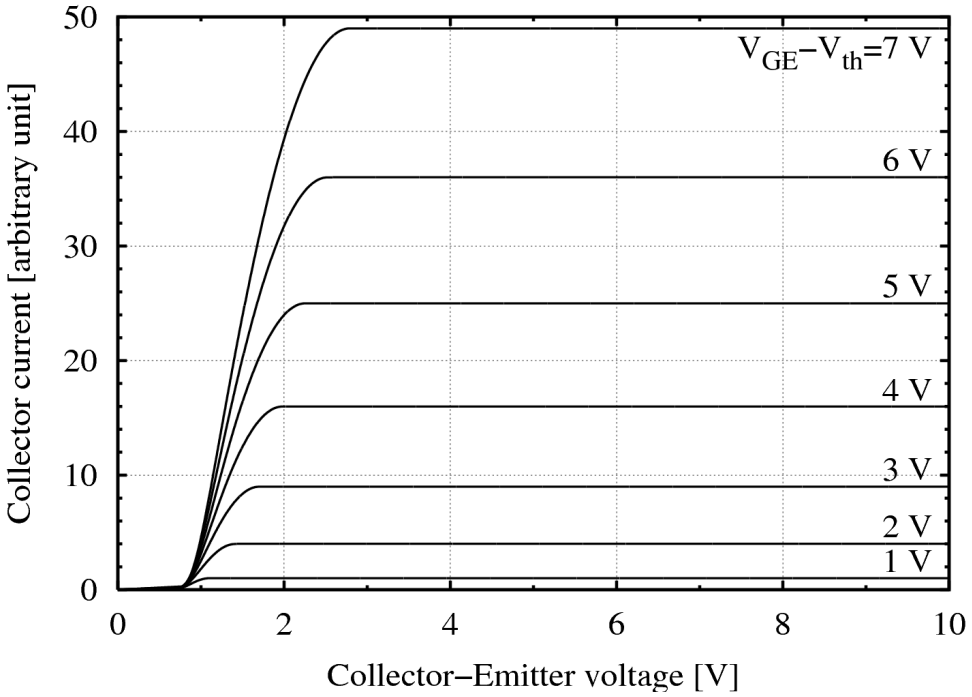


Figure 2.8: Static characteristic of a imaginary Insulated Gate Bipolar Transistor (IGBT). From [18]. CC.

2.7.1 Desaturation circuits

One way to protect from overcurrent is by observing the voltage drop over the switch. One advantage with this method is that it possible to implement it regardless of the switches used since it does not rely on any extra sensing outputs from the power modules. Moreover, it can detect the first three sources of overcurrent presented above, which are the most severe ones. This has been a very common protection circuits in IGBT based VSIs. The protection circuit exploits the fact that when a high current flows through an IGBT, the voltage drop across it will increase dramatically since it will exit the saturation region and enter the active region as seen in Figure 2.8.

Because the quick increase in V_{CE} in the active region, this protection scheme works very well since it gives a very well defined voltage threshold to trigger at. However, since SiC MOSFETs enters the saturation region much later than an IGBT as can be seen in Figure 2.9, this type of protection becomes harder to implement for SiC. Although it is still possible, this does create a circuit more sensitive to noise since it will have a lower detection threshold.

In Figure 2.10 the schematic for a desaturation circuit for MOSFETs is shown [1]. The on-state voltage drop of the MOSFET is represented by the voltage source $R_{\mathrm{On}}I_{\mathrm{D}}$. V_{DD} is the voltage connected to the gate drivers' high voltage side. When the MOSFET is turned on, the voltage V_1 in the circuit will be

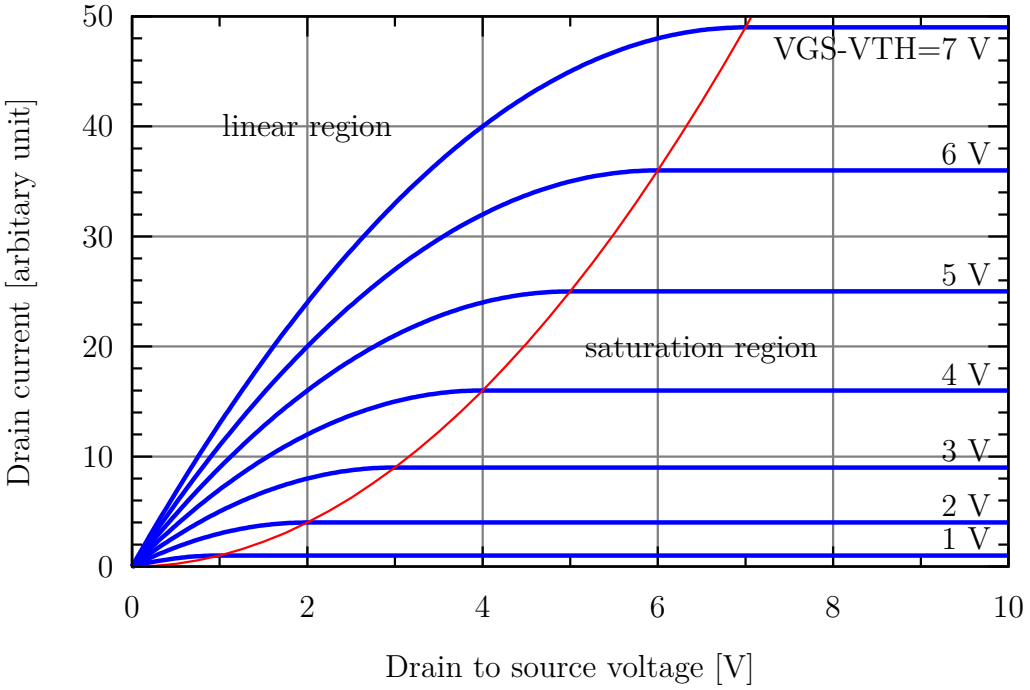


Figure 2.9: Drain current as a function of the drain-to-source voltage and the gate-to-source bias over the threshold voltage. From: [19]. CC.

$$V_1 = V_F + R_{On} I_D \tag{2.41}$$

where V_F is the forward voltage drop of the diode in the desaturation circuit. The voltage V_{OC} is then monitored by the gate driver and when it reaches the specified trigger voltage level, $V_{OC,trig}$ the gate driver turns off the switch.

By knowing V_{OC} and the voltage level of V_1 it is possible to derive the relationship between R_2 and R_3 as

$$V_{OC,trig} = \frac{R_3}{R_2 + R_3}(V_1, fault). \tag{2.42}$$

The relation between R_2 and R_3 should be such that the voltage V_1 at the highest drain current under normal operation gives a voltage V_{OC} with a margin below $V_{OC,trig}$, to not trigger an overcurrent at normal currents. It should also be selected so that the voltage V_1 at a too high drain current gives a voltage V_{OC} well above the $V_{OC,trig}$, level, to trigger an overcurrent fault. When an overcurrent is detected this will lead to an immediate turn off of the switch and the switch will be kept off.

It should be noted that when the switch is turned off, for example by the PWM signal, the voltage across the switch, $R_{On} I_D$, is V_{DC} and the diode in Figure 2.10 will be blocking. This means that the voltage V_{OC} will be $V_{DD} \frac{R3}{R1+R2+R3}$ which would then trigger the overcurrent protection since it will be higher than $V_{OC,trig}$. To prevent this from happening, it is common to disable the detection circuit when the gate

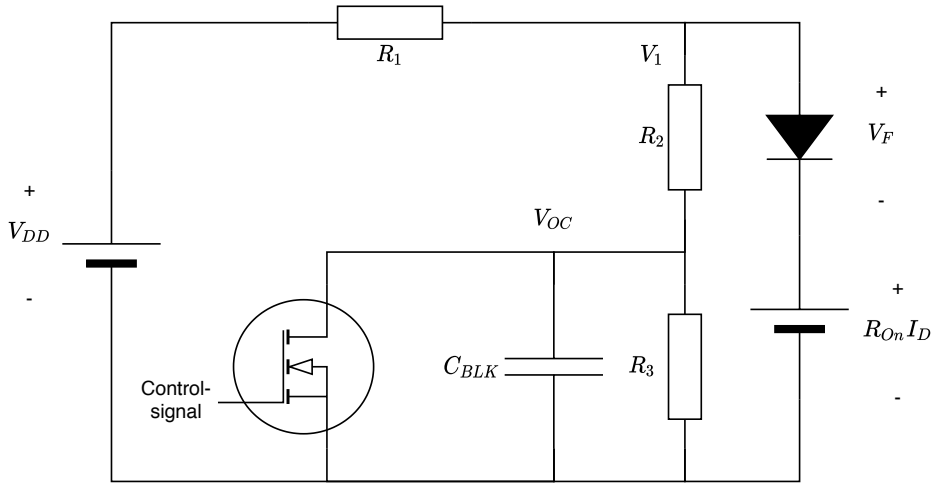


Figure 2.10: Schematic showing a desaturation circuit for SiC MOSFETs.

is turned off by using the NMOS connected in parallel with C_{BLK} in Figure 2.10. When the switch is turned off the NMOS is turned on which shorts the voltage V_{OC} and the capacitor to ground and thereby disables the detection circuit.

To make the detection circuit resistant to noise and preventing it from reacting to switching transients the capacitor C_{BLK} is connected in parallel with the voltage V_{OC}. This is done to prevent the gate driver from wrongly turning off the switch at disturbances. To pick the blanking capacitance C_{BLK} it is necessary to study the blanking time of the circuit, which is defined as the time it takes for the capacitor to charge up to the voltage where it detects a fault, $V_{\mathrm{OC,trig}}$. The time it takes for a capacitor to reach the voltage V with an applied voltage of V_0 in an RC circuit is given by

$$t = -RCln(1 - \frac{V}{V_0}). \tag{2.43}$$

The circuit is however not represented by an RC circuit in its original state and thus it needs to be converted into one by use of Thévenin's Theorem [20].

Depending on the severity of the fault two different cases can be obtained. The first case is for a "low" fault current so that $V_1 < V_{\mathrm{DD}}$ and in this case the voltage across R_2 and R_3 will be clamped at V_1 and this will determine the charging of the capacitor C_{BLK}. The other case is for a "high" fault current leading to that the voltage $R_{\mathrm{On}}I_{\mathrm{D}}{>}V_{\mathrm{DD}}\frac{R2+R3}{R1+R2+R3}$ and the diode will block. For this case the voltage across R_1, R_2 and R_3 will be clamped at V_{DD} and this will determine the charging of the capacitor C_{BLK}. Thévenin's Theorem can be used to calculate the equivalent resistance and charging voltage of these circuits seen from where the capacitor is connected. Starting with the first case, by replacing the diode and the MOSFET voltage drop with a voltage source and shorting it to ground, an equivalent resistance can be calculated as $R_{\mathrm{TH1}} = \frac{R_2R_3}{R_2+R_3}$. Furthermore, the voltage over R_3 is given by

$$V_{\mathrm{R_3}} = \frac{R_3}{R_2 + R_3} V_1. \tag{2.44}$$

Thus, the time it takes to charge C_{BLK} to the trigger voltage $V_{\mathrm{OC,trig}}$ is given for the two cases by

$$t_{\mathrm{BLK1}} = -\frac{R_2 R_3}{R_2 + R_3} C_{\mathrm{BLK}} \ln\left(1 - \frac{V_{\mathrm{OC,trig}}}{V_1} \frac{R_2 + R_3}{R_3}\right) \tag{2.45}$$

$$t_{\mathrm{BLK2}} = -\frac{(R_1 + R_2) R_3}{R_1 + R_2 + R_3} C_{\mathrm{BLK}} \ln\left(1 - \frac{V_{\mathrm{OC,trig}}}{V_{\mathrm{DD}}} \frac{R_1 + R_2 + R_3}{R_3}\right). \tag{2.46}$$

The blanking times, t_{BLK1} and t_{BLK2} should then be selected such that in the event of an overcurrent, the turn-off happens fast enough that no damage is done to the system while also being as resistant to noise as possible. It is also important to consider the entire turn-off event including gate driver and MOSFET turn-off delay to ensure that the entire sequence from detection to turn-off is fast enough.

3

Method

In the following section the methods used to design and evaluate the inverter are described.

3.1 Function realisation through PCB design

To realise the functionality described in Figure 2.1, four different Printed Circuit Boards (PCBs) were designed. The functionality of each is briefly described below.

The power board is a mainly high voltage and high current PCB since it accommodates the switches. To limit the voltage ripple, a DC-link will be located here as well. The power board will also contain parts for measuring the DC-link voltage, which is required for the control system. Finally it will contain the circuits used for measuring the phase currents which is needed for the control system.

Mounted on top of the power board are the gate drivers. While it would be preferable to have the gate drivers mounted on the same board as the power board for the sake of compactness and proximity, they will be mounted on a separate PCB to ease manufacturing. The gate driver board will also contain the desaturation circuits intended to protect the switches from high overcurrent.

The communications board houses all low voltage auxiliary signal circuits required to operate the inverter, such as communication and debugging circuits. It also provides an interface between the processor board and the gate drivers. Additionally, this PCB also provides some of the overcurrent protection by utilising the current sensor signals.

The processor board houses the microcontroller used to run the control software which determines the switch states. The microcontroller was placed on this separate board to allow for easy replacement in case of device failure.

3.2 Maximum current

To properly design the powerboard, the maximum phase current that will happen at operation needs to be identified. While the motors draw around 48 A RMS at rated operation, they can operate at a much high output power which is utilised by CFS to produce peaks of 32 kW instead of the rated 13.5 kW. Therefore it is required to know how high current is drawn at 24 Nm and 12000 RPM. Furthermore, because of the low thermal mass in a MOSFET it can be assumed that it needs to be able to carry the maximum current continuously and therefore no study into duration is needed.

3.3 MOSFET selection

To decide which MOSFET was the most suitable to use, a list of options was compiled out of options from different suppliers. However, only power modules were studied and no discrete options were considered. Both half-bridge power modules and six-pack modules were considered.

After the list was compiled, the increase in temperature at expected maximum load and up to 100 kHz switching frequency was calculated to verify that the MOSFETs would remain withing the rated temperature during operation. To calculate the thermal losses in the MOSFETs, the equations in 2.3 were used. These losses need to be removed by means of cooling. For that, a thermal network calculation was made using the same methods as in [21], but adapted for MOSFETs as opposed to IGBTs (except for calculations for the reference IGBT inverter solution). After that, the modules were compared based on size and price to pick one option. Efficiency was not considered since it not the aim of this thesis to build the most efficient inverter, but rather the smallest and lightest.

3.4 Si IGBT and SiC MOSFET comparison

After the SiC module was decided, a comparison was made between the module and the Si IGBT used in the HPC-HTDFS. The losses for both IGBT and diodes were calculated for the inverter Aros HPC-HTDFS while no external anti-parallel diodes were used for the SiC module. The operating point where the calculations were done was picked as the maximum operating current needed to produce 24 Nm while the switching frequency was swept up to 100 kHz and the temperatures compared.

3.5 Current measurement

In the automotive industry there are many current sensors to choose from. To narrow down the quantity to choose from, a list of requirements that each sensor needs to meet was constructed. From that list of requirements, a list of viable options was made and a sensor was picked based on size, cost and ease of implementation.

3.6 Overcurrent protection

To handle all different over-current modes described in Section 2.7, three different types of circuits were designed.

3.6.1 Desaturation circuit

An overcurrent protection circuit based on the desaturation of the IGBT was designed and implemented. This covered the most severe overcurrent faults of the inverter, but not the overload of the motor.

3.6.2 Current sensor based solution

A second overcurrent method was implemented as a supplement to the desaturation circuit. This circuit is intended to detect instantaneous overcurrent events by observing the signal from the current sensors and comparing that with a preset reference. If a fault is detected, the circuit must put the inverter into a safe state. The reaction time of such a circuit is potentially low since the current sensors introduce additional propagation delay as compared with the desaturation circuit. This will be discussed further is the Section 4.5.

3.6.3 Motor protection circuit

An attempt to design an analog motor protection circuit was made. To evaluate short circuit performance, a traditional melt fuse (IFÖ Highcap Eco gG 50A [22]) was used as a reference. In addition to that, drive cycle data from previous competitions that CFS has participated in was used to make sure that the overcurrent protection circuit can handle a drive cycle type of load. The circuit was designed and tested in Simulink, and after a satisfactory result was found it was also implemented in Altium.

The signal from the current sensor was fed into a low pass filter which is intended to emulate a slow heat up of a motor during overload. The output of the low pass filter was then used to determine if an overcurrent event has occurred. The combination of this signal and the signal out from the circuit described in Section 3.6.2 can then be used to drive the gates low, and thus completely turning off the power supplied to the motors.

3.7 Total Harmonic Distortion

To validate the inverter the THD of the current was measured and calculated. The currents were measured with different bandwidths of the current controller and the same switching frequency and operation point was used. A FFT was then done in MATLAB using the fft function. This gave an indication of how the increased switching frequency affected the total THD of the full system including the PMSM.

3.8 Dead-time

To prevent accidental shoot-through, a dead-time was inserted based on the turn-off delay given in the datasheet of the power module. An additional safety-margin was also added. The lowest possible dead-time was found by running the inverter at 50 % duty cycle (i.e. no load) while lowering the dead-time in small steps until cross conduction occurred and a very small increase in DC-current consumption was seen, upon which the dead-time was increased again to add safety margin. This was done for various different supply voltages up to 600 V DC.

Next, the actual dead-time was measured with an oscilloscope. The voltage from one phase output to DC- was measured as was the lower gate voltage for that phase and the current flowing in that phase. Then by studying the phase voltage when the current was flowing out of the phase leg, the dead time was identified. After that, the dead-time was lowered and fine tuned.

The current was measured with a LeCroy AP011 with a bandwidth of 120 kHz that was degaussed before testing. The gate voltage was measured on the pins of the MOSFET with a Testec TT-SI9101, that has a bandwidth of 100 MHz and which was set to an attenuation of 1:100. The phase voltage was measured with a Testec TT-SI9010 with a bandwidth of 100 MHz and also set to 1:100 attenuation. Phase-C was selected because of the accessibility to the gate.

4

Results and discussions

In the following section results from calculations, simulations as well as real world testing will be presented. The results will discussed and interpreted.

Figure 4.1 shows the measured RMS current at 24 Nm and 12000 RPM to be around 114 A RMS. This is an operation point that causes the maximum current. The data comes from a run in the test bench done by CFS 2018. For the rest of the report, 120 A RMS will be considered as the maximum current that the inverter will need to be able to handle.

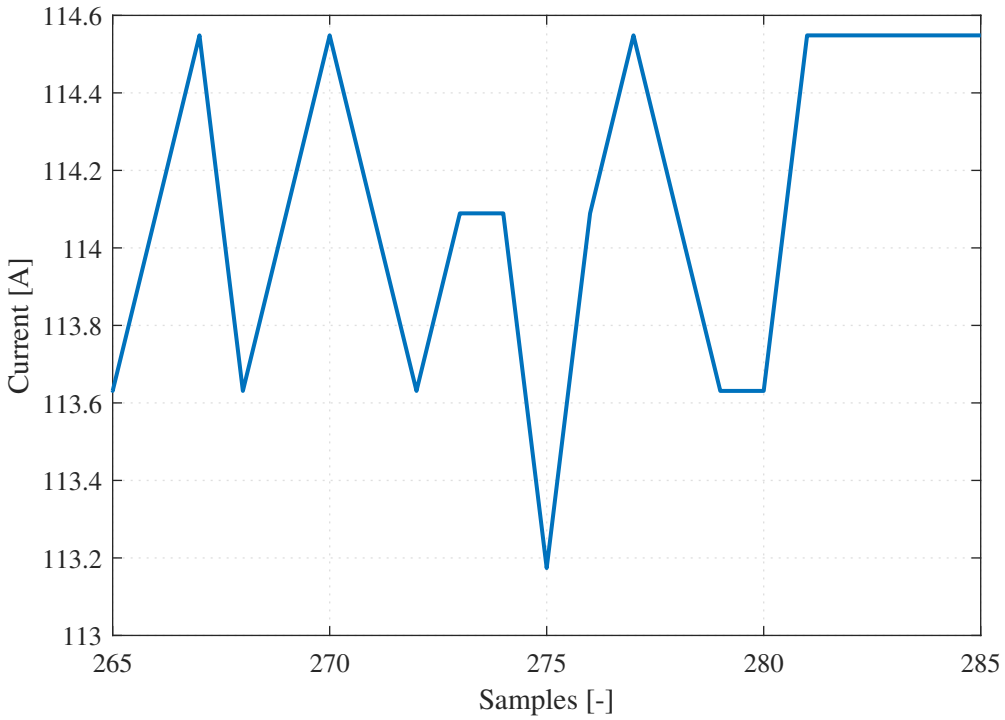


Figure 4.1: Maximum current at 12000 RPM and 24 Nm as measured during the motor testing done by CFS 2018.

4.1 Switch evaluation, selection and testing

Various SiC power modules were evaluated based on the parameters specified by the manufacturers' datasheets as well as with calculations. Based on the results from these theoretical methods, one power module was selected. Testing results from this module are also be presented.

4.1.1 Calculation results

In Table 4.1 some of the power module options are shown, together with the some of their properties compiled from the datasheets. These switches are the ones that are feasible, i.e. do not overheat at maximum operation of 120 A RMS phase current and a switching frequency of 50 kHz. For reference the IGBT module that is in the reference inverter from Aros is also included.

Table 4.1: List of feasible power modules with nominal datasheet specified properties and cost. The area and price is per module.

Model number	V_{DS} [V]	I_D [A]	R_{on} [mΩ]	$E_{sw,on}$ [mJ]	$E_{sw,off}$ [mJ]	Area [mm^2]	Price [SEK]
Triple half bridge: Microsemi APTMC120TAM12CTPAG [23]	1200	220	16.8	3.3	1.8	5184	18000 [1]
Triple half bridge: Vincotech 10-PH126PA010MR-L820F86T [24]	1200	134	14	4	2.4	3067	3800
Single half bridge: Infineon FF8MR12W2M1 _B11 [25]	1200	150	9.83	2.1	0.77	2409	1800
Single half bridge: Cree CAB400M12XM3 [26]	1200	395	4	5	4.2	4240	7800
Single half bridge: Microsemi APTGT200A120G (IGBT) [27]	1200	200	-	20	20	6480	1700

The data presented in Table 4.1 is not useful directly since the equations presented in Section 2.3 require $A_{sw,on}$ and $A_{sw,off}$. Also, the on-state resistance R_{on} is not always specified at the same operation point. Therefore, some pre-calculation has to be done, and the results of which is presented in Table 4.2. $A_{sw,on}$ and $A_{sw,off}$ were calculated using (2.22). R_{on} was adjusted for operation at 125 °C according to the datasheets of each module.

In Figures 4.2 and 4.3 three of the modules presented above were compared to the IGBT module used in the HPC-HTDFS with a constant current of 120 A RMS and with a varying switching frequency. The water temperature was set to 40 °C, and the heat sink thermal resistance was set to 0.01 K/W according to the commercially available heatsink in [28]. This thermal resistance was then scaled based on the surface area of each module.

[1] While this module is considered viable in terms of performance it is far too expensive to actually be a viable option overall.

[2] Corrected for $I_d = 120$ A and $T_j = 125$°C.

Table 4.2: List of feasible power modules' properties adapted for conduction loss and switch loss equations. Also note that for the half bridge modules the the area and price has been multiplied by three since three such modules would be needed for a three phase VSI.

Model number	$R_{on}{}^2$ [mΩ]	R_{jc} [m/K]	$A_{sw,on}$ $\left[\frac{nJ}{VA}\right]$	$A_{sw,off}$ $\left[\frac{nJ}{VA}\right]$	Area [mm^2]	Price [SEK]
APTGT200A120G [27]	-	0.25	167	167	19440	5100
10-PH126PA010MR-L820F86T [24]	14	0.33	66.7	50	3067	3800
CAB400M12XM3 [26]	5.6	0.15	37.5	25	12720	23400
FF8MR12W2M1_B11 [25]	9.83	0.35	20	13	7227	5400

It can be seen that at low switching frequencies, around 10 kHz, the temperatures of all modules, including the IGBT are all reasonable, and the IGBT is colder than the Vincotech module despite almost double the losses. This is because three half-bridge modules are used in comparison with one six-pack module which results in less than a third of the cooling area when comparing the modules. A similar behaviour is of course noticed when comparing the different SiC modules since the two other SiC modules are also half-bridges. The IGBT approaches 150 °C at 30 kHz and the Vincotech module reaches 175 °C at 85 kHz switching frequency while the other two modules remain within acceptable temperatures all the way up to 100 kHz.

However, even though the reference IGBT can switch at up to 30 kHz, it is infeasible when studying the efficiency of the inverter since it would have close to 3.3 kW losses as compared to the 990 W losses in the Vincotech module. From a racing perspective, this is more than 2 kW that can be output into the motor for extra performance and from a sustainability perspective it is of course better to not have to lose that power.

In Figures 4.4 and 4.5 all the SiC modules are compared with a constant switching frequency of 50 kHz and 40 °C water temperature. It can be notice that the junction temperatures all stay below 140 °C. The Vincotech module is however getting hotter than the other two modules and it has slightly higher losses and therefore a worse efficiency. It should however be noted that it has an efficiency of 97.7 % at rated operation and at 50 kHz.

In the end, the power module chosen was the one from Vincotech. While it is not the module with the lowest losses and highest efficiency, it makes up for this in size. It takes up less than half the surface area compared to the Infineon modules and will therefore make for a smaller inverter overall. The Vincotech module is also cheaper than either of the Infineon solutions. Keeping the cost down enabled the use of more expensive capacitors which in turn made for an even smaller design.

4.1.1.1 Efficiency at low switching frequencies

In figures 4.4 and 4.5 only high switching frequencies are considered. This is because of the goal of this thesis. However, if it was not a focus to reduce harmonics (i.e. by

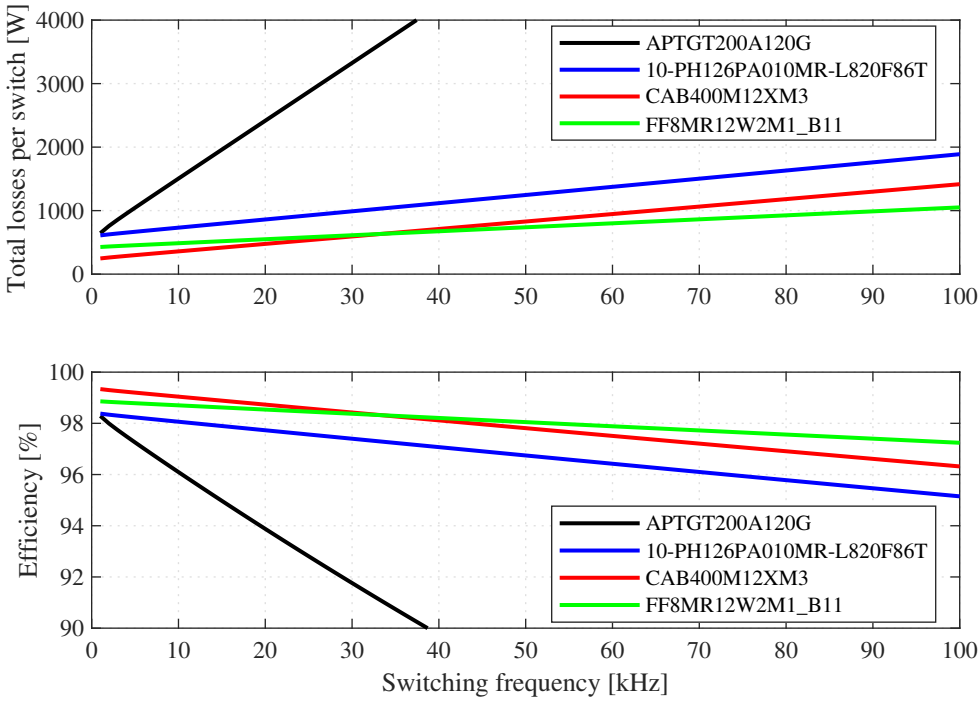


Figure 4.2: Losses and efficiency of three SiC modules and one IGBT module over different switching frequencies with 120 A RMS current.

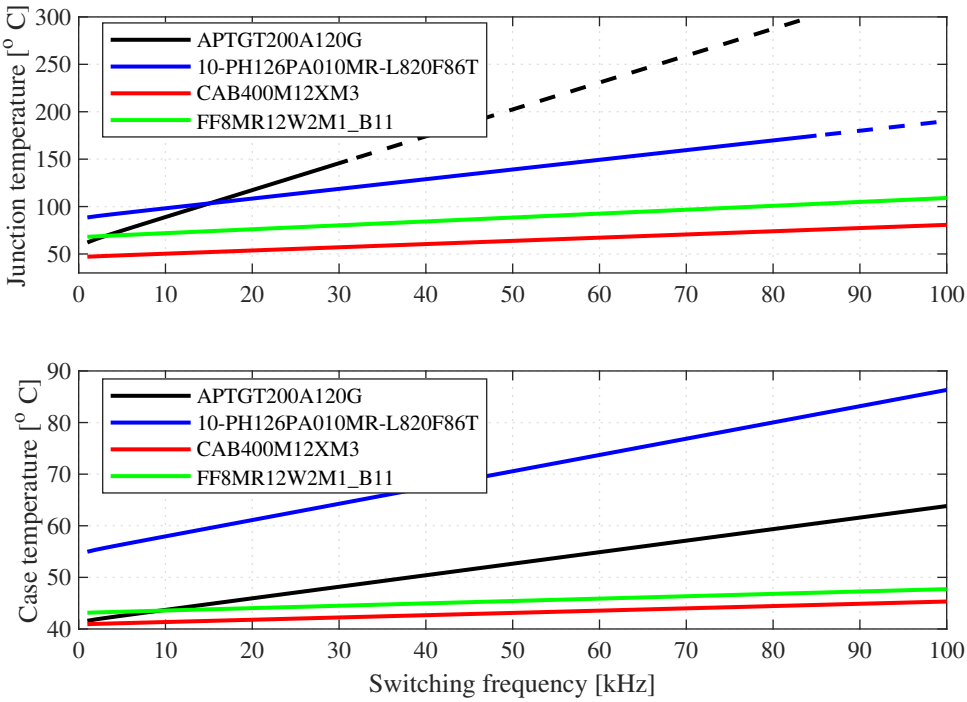


Figure 4.3: Steady state temperatures of three SiC modules and one IGBT module over different switching frequencies with 120 A RMS current and 40 °C water temperature. Dashed lines indicate exceeded maximum junction temperatures.

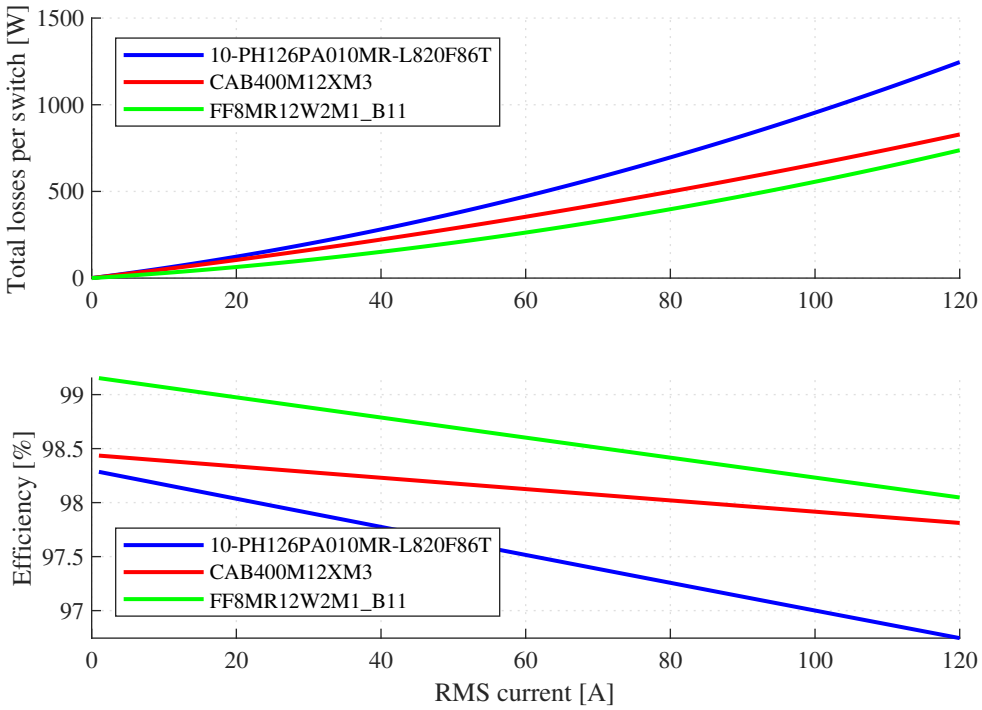


Figure 4.4: Losses and efficiency of three SiC modules over different load currents with a fix switching frequency of 50 kHz and a water temperature of 40 °C.

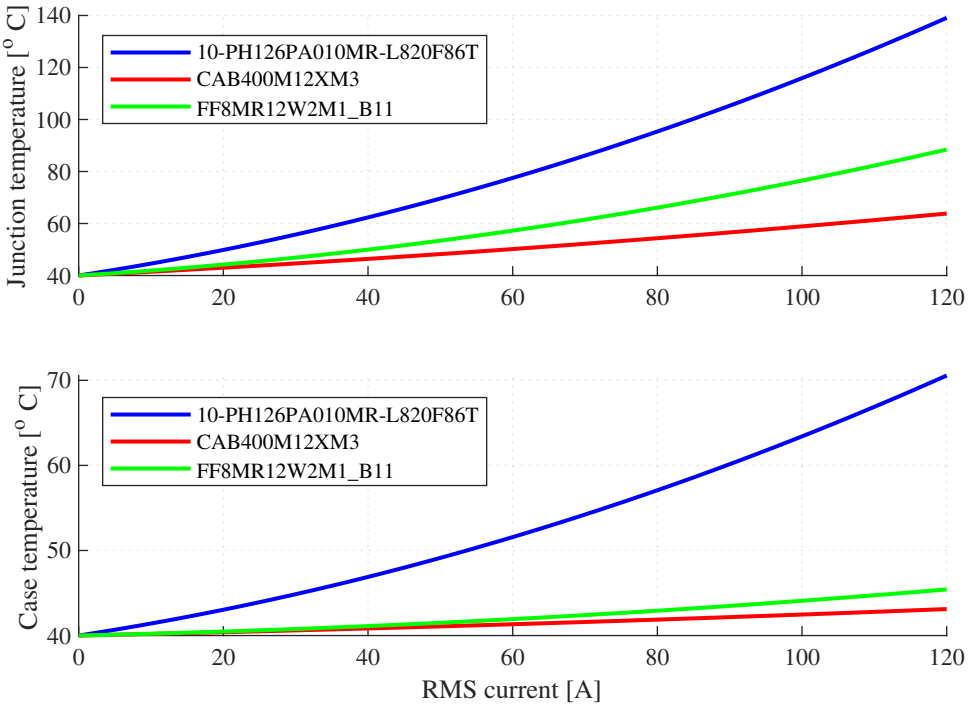


Figure 4.5: Steady state temperatures of three SiC modules over different load currents with a fix switching frequency of 50 kHz and a water temperature of 40 °C.

considering a motor without significant harmonics) a high switching frequency might not be needed. Instead, the inverter could run at the same switching frequency as the IGBT based reference solution and reap the benefits of having lower switching losses. In Figure 4.6 such a scenario is shown.

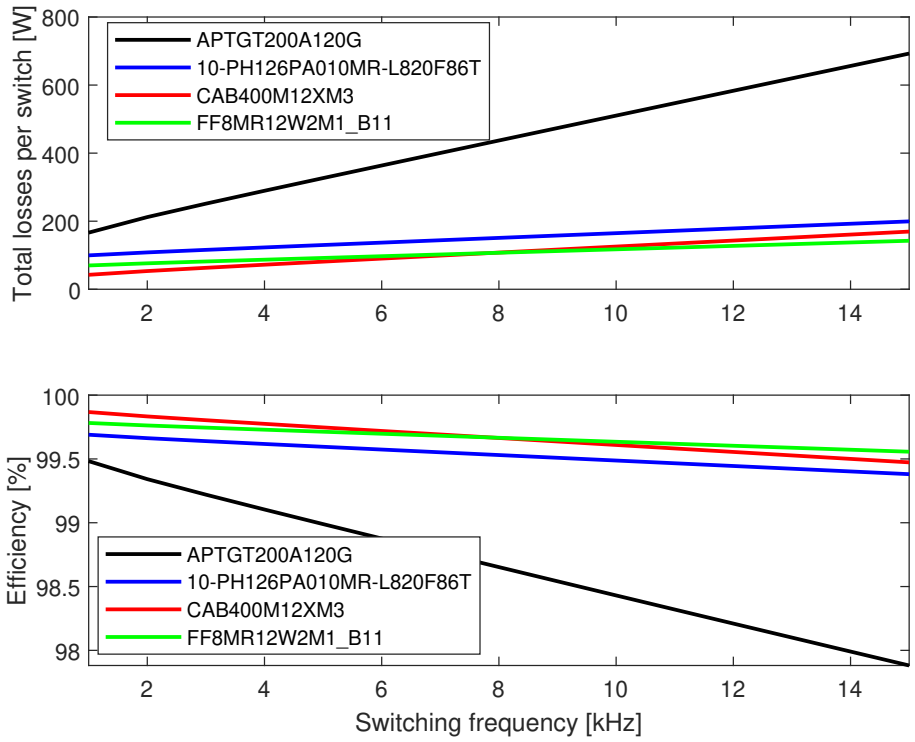


Figure 4.6: Switch losses and efficiency at lower switching frequencies and 48 A RMS using an external gate resistor of 4.8 Ω.

As can be seen in Figure 4.6, at maximum continuous rated motor current the inverter losses at 10 kHz can be reduced by around 75 % by going from an IGBT based inverter to a SiC based inverter. This might be a better approach in terms of sustainability and total energy use than raising the switching frequency to deal with the motor harmonics. It is hard to say conclusively though, and might depend on the drive cycle. Perhaps the ideal scenario would be to run the inverter with a variable switching frequency to be able to optimise for switch losses as well as losses caused by harmonics. This is something that could be investigated in future work.

4.1.2 Experimental results

To test the real world capability of the selected module a three-phase sinusoidal current was injected into three external inductors in a Y-connection. The current was gradually increased while measurements were taken with an oscilloscope as well as with the microcontroller. Many test runs were performed with various levels of success. One of the problems that occurred was that the currents measurements

were too noisy while running at a switching frequency $f_{sw} = 60$ kHz leading to spurious software overcurrent events despite raising the limits. For this reason all test data presented in this section was acquired at a switching frequency $f_{sw} = 30$ kHz.

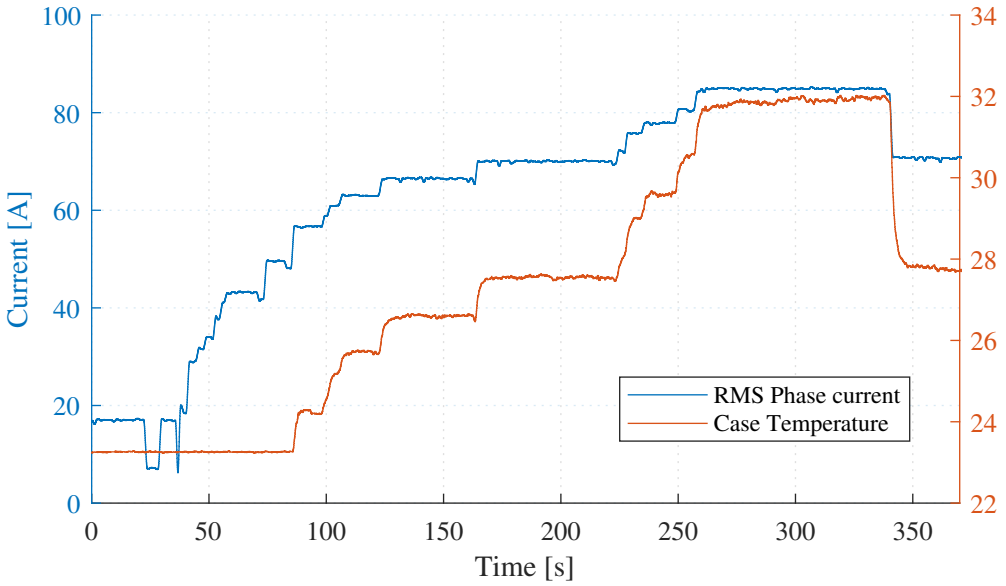


Figure 4.7: Log data from a test session where the inverter was connected to external inductors. The switching frequency was set to 30 kHz.

In Figure 4.7 current and temperature is plotted over time from one test session where up to 85 A RMS was achieved. A few data points from this data during steady state was compiled in Table 4.3, along with predicted values from Figure B.1. Since the tests were performed with much colder coolant than the 40 °C that was assumed during module selection, the predicted data has been adjusted accordingly.

Table 4.3: A selection of of data points from Figure 4.7 compared with predicted values from Figure B.1. Coolant temperature during the test was 15 °C, and thus the predicted values have been adjusted for that coolant temperature.

Current (RMS)[A]	Case temperature [°C]			Junction temperature [°C]
	Predicted	Measured	Error	Predicted
66.7	28.9	26.6	2.3	59.5
70.3	29.8	27.6	2.2	62.1
77.9	32.0	29.6	2.4	69.6
85.0	34.2	31.9	2.3	76.4
92.0 [3]	36.4	39.1	-2.7	83.6

In Figure 4.8 an attempt at reaching the design target of 120 A RMS is shown. Up to 92 A the inverter was operating as expected, but when the current was increased to

[3]This data point is from the test run depicted in Figure 4.8, and might therefore be inconsistent with the rest of the data points because of potential change of coolant flow rate.

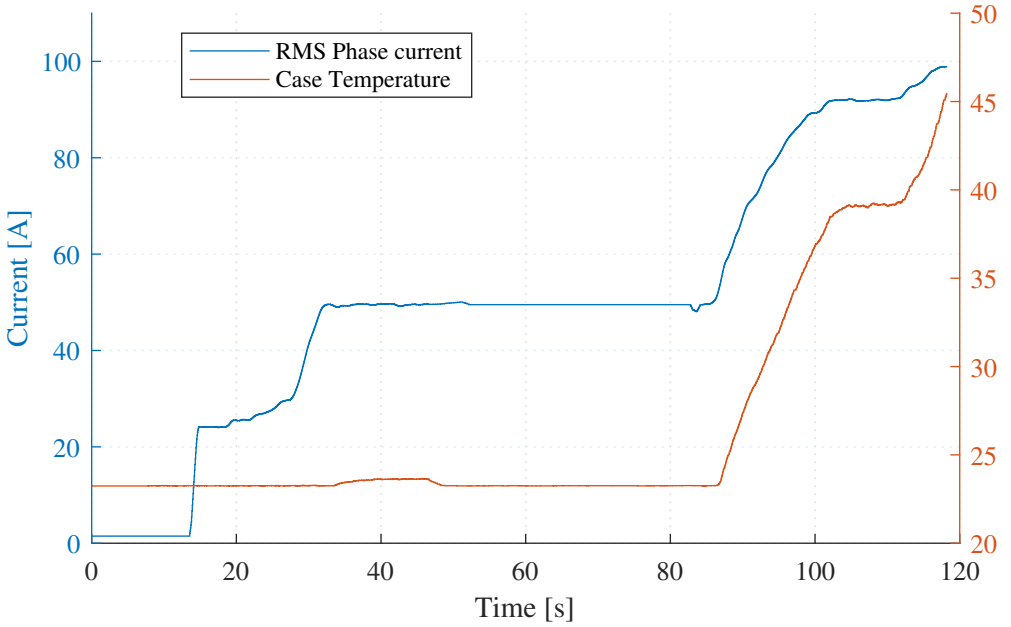


Figure 4.8: Data log from an attempt at reaching 120 A RMS with external inductors, leading to premature device failure at 99 A. Switching frequency was set to 30 kHz.

99 A one of the MOSFETs failed along with most of the components in the associated gate driver circuit. The root cause for this failure will likely never be known with full certainty, but one theory that could explain the failure is uneven cooling. Upon inspection it was found that the water cooling plate was not completely flat, and in particular there was a low spot (which would lead to poor cooling) in the area of the MOSFET that failed, which can be seen in Figure 4.9. It seems that the area where the thermistor is located within the module had a very good contact with the cooling plate, which would explain why the predicted case temperatures match rather well with the measured case temperatures. Thus, it cannot be concluded that the thermal modelling is wrong. Quite the opposite, all test results apart from the MOSFET failure points towards that the thermal modelling is correct. It must be said, however, that since not all test cases were performed (i.e. no switching frequency sweep, and device failure before 120 A was reached) there is still more work that has to be done before the proposed models can be fully trusted.

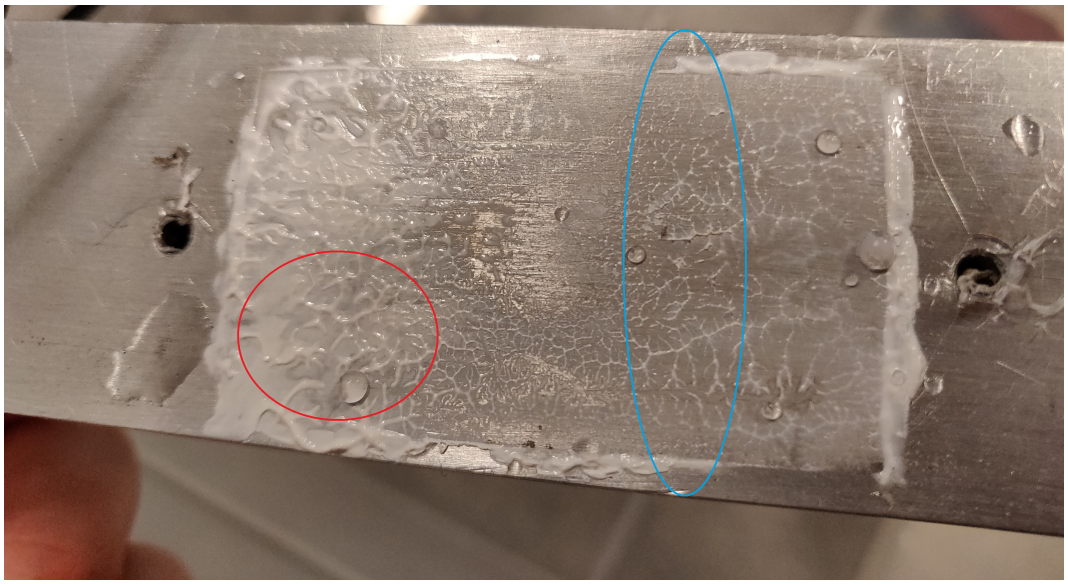


Figure 4.9: Uneven distribution of thermal interface material, indicating uneven cooling. The red ellipse indicates the position where the failed MOSFET was located, and the blue ellipse is the approximate position of the thermistor.

4.2 Gate driver

With the MOSFET selected, an appropriate gate driver was also required that met the requirements of the MOSFET. There are three different main options available when deciding how to design the gate driver circuit. Either use an existing solution that is designed for the module used and that includes overcurrent protection, isolation and everything else that is needed for the gate driver to work. However, this requires that the manufacturer has designed a gate driver that fits with their module. This is not available from Vincotech and therefore it was not an option. The other two options involve the complete design of the PCB. This can be done in two different ways: one using a ready made Integrated Circuit (IC) for boosting the signal from the processor and the other using discrete components to achieve the same function as the IC. Not using an IC would however introduce risks with timing and propagation delay and other design mistakes. Therefore to minimise risk and keep the design simpler, an IC solution was used.

The MOSFET can handle from -4 V to 22 V on the gate [24]. It has an internal gate resistance of 1.7 Ω. To minimise the risk of ground bouncing, a negative voltage was used which means that the gate driver would need to handle negative voltages. Furthermore, the gate driver would need to include galvanic isolation withstanding up to 1800 V DC as per the Formula Student Germany (FSG) ruleset (see rule *EV 1.2.1* in [17]), since the maximum DC voltage would be 600 V. To prevent thermal runaway caused by a too low V_{GS}, under-voltage lockout (UVLO) would also be required. To make the design easier, an overcurrent detection function should be included such that the gate driver turns itself off when it detects an overcurrent.

The Texas Instruments UCC21710 IC was selected as it includes multiple required features and the most important can be summarised as:

- ± 10 A maximum gate current enabling fast switching.
- 33 V maximum output voltage (VDD to VEE).
- High and low output enabling the use of different resistors on turn-on and turn-off if needed.
- Miller clamp function bypassing the resistors from the gate to VEE when turned off, minimising the risk of bouncing.
- 270 ns delay from overcurrent fault to gate low.
- 90 ns propagation delay on gate turn-on and turn-off.
- 150 V/ns common mode transient immunity.
- OC input that can be used with a desaturation circuit to turn off the gate in case of overcurrent.
- Isolated voltage sensing to be used for sensing module temperature and DC-link voltage. This is output on the low voltage side as a PWM signal.
- 5700 V galvanic isolation.

A positive gate voltage of 20 V ensures that the gate can be driven high fast and be held at a stable conducting state, resulting in an as high gate current as possible. 22 V is not chosen to leave room for eventual noise on the DCDC without going over the 22 V limit. As a safety, the ICs internal UVLO circuit triggers at 10.8 V, turning the gate off and preventing a thermal runaway. Furthermore, a negative voltage of -3 V is applied to ensure that the gate is held low and not being accidentally triggered by noise, leaving a margin to the minimum voltage allowed on the gate as well. The IC also includes an internal Miller clamp. This function pulls the gate to VEE, -3 V, bypassing the external resistors. This minimizes the risk of accidental turn-on by noise. Furthermore it also includes an isolated voltage measurement which provides a safe and easy measurement of the module temperature as well as the DC-link voltage. However, only the three lower ICs can be used for this as only the lower gates are connected to common. The current requirement of the DC-DC converter is calculated through the gate charge of the MOSFETs to be 43 mA at a switching frequency of 100 kHz. Furthermore, through (2.10), we get an estimate that the voltage over the MOSFETs will change between V_{DC} and V_{DSon} in 47 ns at $I_{\mathrm{D}} =$ 120 A RMS. This results in a change of 47 kV/µs. To meet these requirements the RECOM R24P22005D[29] DC-DC converter was selected. It is isolated at 6.4 kV DC, has an input of 24 V, and output of 20 V and -5 V with both outputs capable of outputting 80 mA. Furthermore it can handle voltage transients up to 65 kV/µs. Finally a linear regulator was used to bring the negative voltage up to -3 V.

The gate resistors were initially chosen as $R_{\mathrm{G,ext}} = 1\ \Omega$ which results in a peak gate current of 6.8 A. The $R_{\mathrm{G,ext}} = 4.8\ \Omega$ resistors were implemented when high frequency ringing was noticed during testing. By increasing the gate resistance, the MOSFETs will turn on slower and therefore the frequency of the noise will be lower. Theoretical turn-on switch behaviours at $I_{\mathrm{D,RMS}} = 120$ A for these two different gate resistors can be seen in Figure 4.10. There is a noticeable increase in turn-on time and it takes more than double the time for the MOSFET to turn-on due to the lower gate current used. The majority of the time comes from the time it takes for V_{DS} to drop to $V_{\mathrm{DS,on}}$. As is seen in (2.10), by increasing the total gate resistance, R_{G}, the time it takes for the voltage to drop decreases. This is due to the decrease in gate current. For the turn-off, the same calculations are applicable but the order of events are swapped.

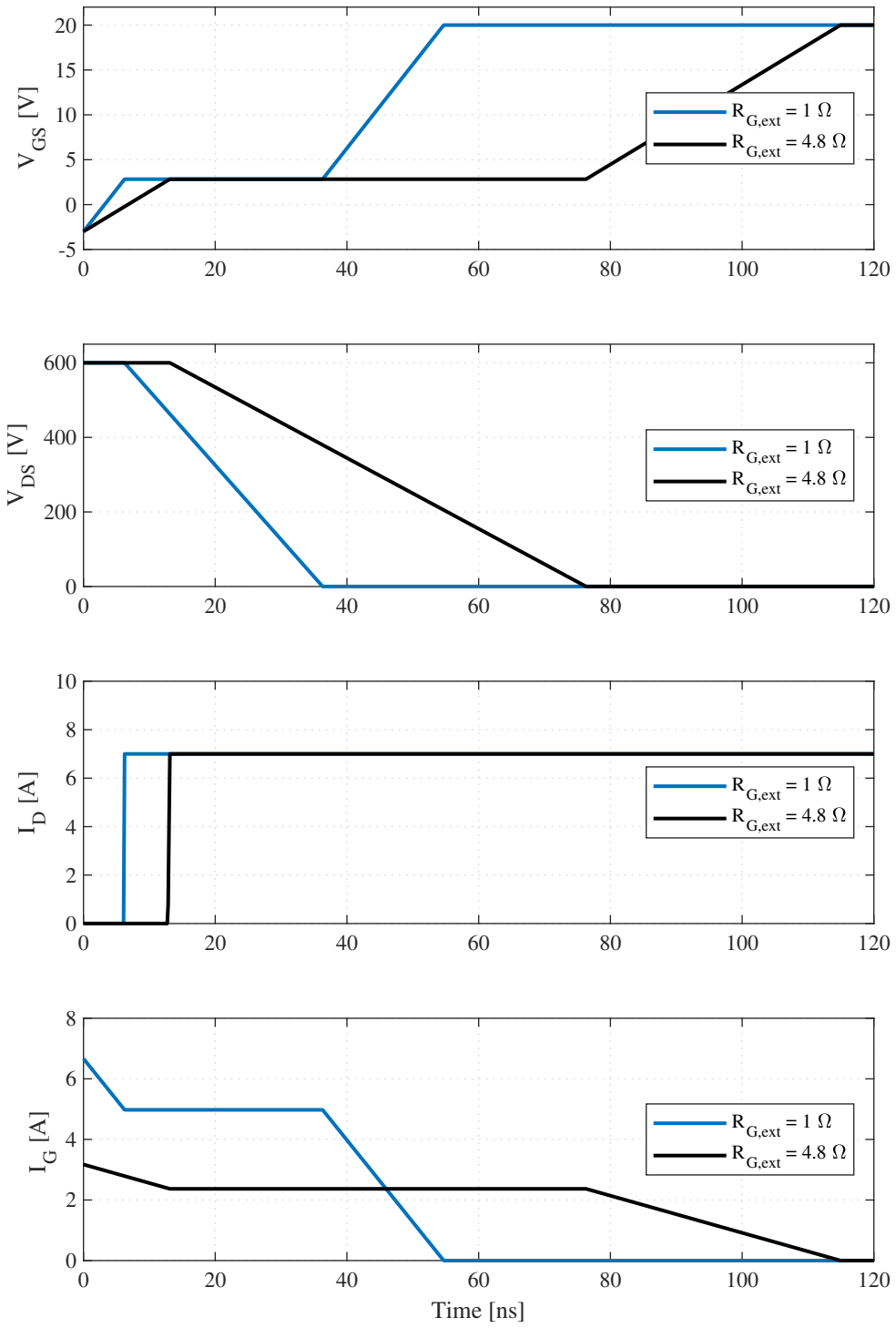


Figure 4.10: Calculated turn-on behaviour with $R_{\mathrm{G,ext}} = 1\ \Omega$ and $R_{\mathrm{G,ext}} = 4.8\ \Omega$ at $I_{\mathrm{D,RMS}} = 120$ A. $R_{\mathrm{G,ext}} = 4.8\ \Omega$ was implemented to reduce the high frequency (MHz) noise caused by the fast turn-on.

An additional safety feature in the gate driver IC is the PWM interlock preventing that both high and low switches are turned on at the same time. This is done by

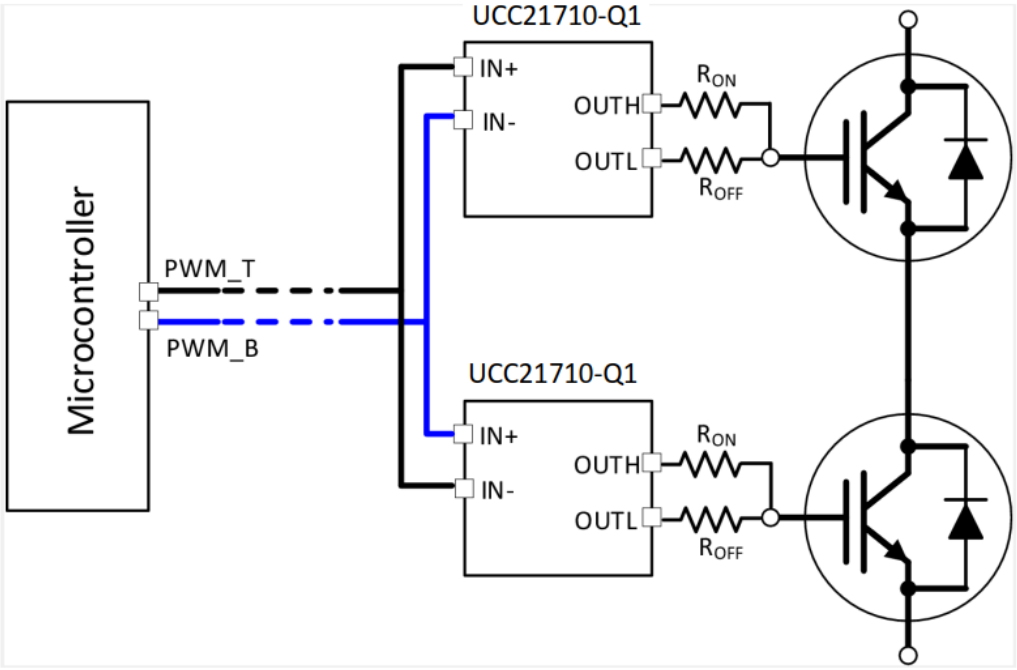


Figure 4.11: Interlock function of the UCC 21710-Q1 and how it is connected. Figure from [1].

connecting both the PWM signal and the complementary PWM signal to both gate driver ICs as shown in Figure 4.11.

Finally a desaturation circuit was implemented on each gate driver according to the schematic in Figure 2.10 and the the theory in Chapter 2.7.1. However, since the UCC21710-Q1 has a built in function that pulls the OC pin low whenever the gate signal is deactivated, there is no need for the NMOS. Therefore there is no risk off accidental triggering when the MOSFETs are turned off.

4.2.1 Dead-time

To verify the inserted dead-time both the module data was used and then the switching behaviour of one MOSFET was studied trough an oscilloscope. This was possible since the gate driver has the same propagation delay for both turn-on and turn-off.

The phase current as seen in the upper plots of Figures 4.12 and 4.13 is included to show the direction of the current where negative current means that the current is flowing into the leg which has an impact on the switching behaviour. However, a ripple with a frequency of around 1.7 MHz can be noted during switching in the measured current. Since the current probe is only rated for 120 kHz it is not clear why this was picked up the the oscilloscope, one possibility is that the measurements also include noise caused by EMI.

According to the datasheet [24], the module has a turn-off delay of 399.84 ns at

150 °C. This was used as a basis for the initial dead-time and 1 µs was used with an added safety margin. The first dead-time tests were done according to the first paragraph in Section 3.8, and at $V_{DC} = 600$ V a current increase could be seen at a dead-time of 275 ns. After that a safety margin of a factor 2 was added to account for dynamic changes in the behaviour caused by for example higher temperatures and currents.

The switching behaviour of the lower C phase MOSFET, measured from drain to source at a current of 8 A can be seen in Figure 4.12 where positive current is defined as flowing out of the phase leg [4]. It should be noted that a light moving average filter of 5 samples (sample time is 0.5 ns) has been applied on all measurements in Figures 4.12 to 4.14 to even out the measurements. This does not impact the results.

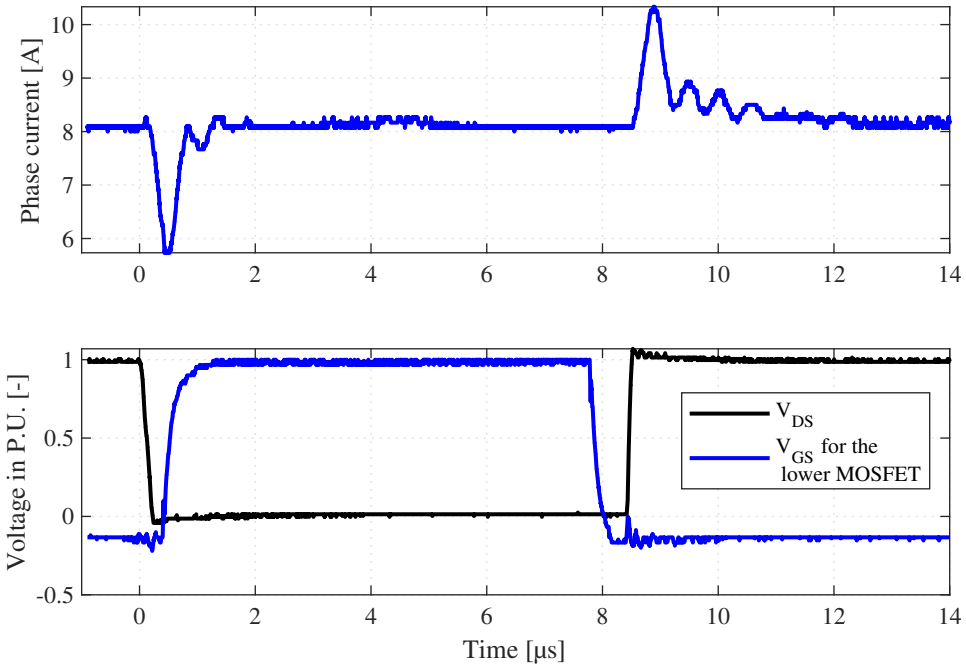


Figure 4.12: Measured C-phase and lower gate voltage (lower plot) as well as phase current (upper plot). Notice how the voltage over the switch drops before the switch is turned on since the body diode is already carrying the current, and thus the dead-time can be seen. The voltages are shown in p.u. where $V_{DS,base} = 600$ V and $V_{GS,base} = 20$ V

Compared to Figure 4.13 where the current is negative it can be noticed that in Figure 4.12 the phase voltage drops before the gate turns on. This can be explained through the direction of the current and by considering the state of the upper MOSFET as well. When the current is positive and the upper MOSFET turns off, the current will keep flowing but use the lower MOSFETs body diode to carry the current instead. Therefore the voltage drop over the lower MOSFET will decrease

[4] See Figure 2.1 for a schematic definition of positive phase current.

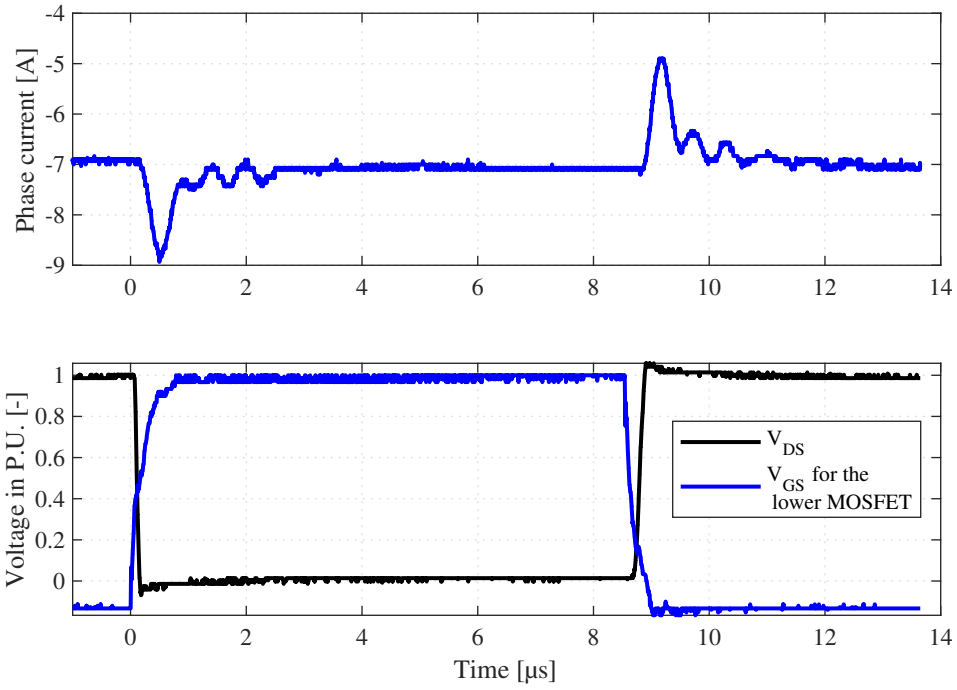


Figure 4.13: Measured C-phase and lower gate voltage (lower plot) as well as current (upper plot). The current is negative and therefore the voltage drops as the switch turns on. The voltages are shown in p.u. where $V_{\mathrm{DS,base}} = 600$ V and $V_{\mathrm{GS,base}} = 20$ V.

before it is turned on. The voltages in Figures 4.12 to 4.14 are shown in p.u. where $V_{\text{C,base}} = 600$ V and $V_{\text{GS,base}} = 20$ V.

In Figure 4.12 the time between the voltage over the switch starting to fall and the gate voltage starting to rise is around 355 ns, however since the inserted dead-time was supposed to be 500 ns, this was not enough. This could be explained by further studying the switch turn-off.

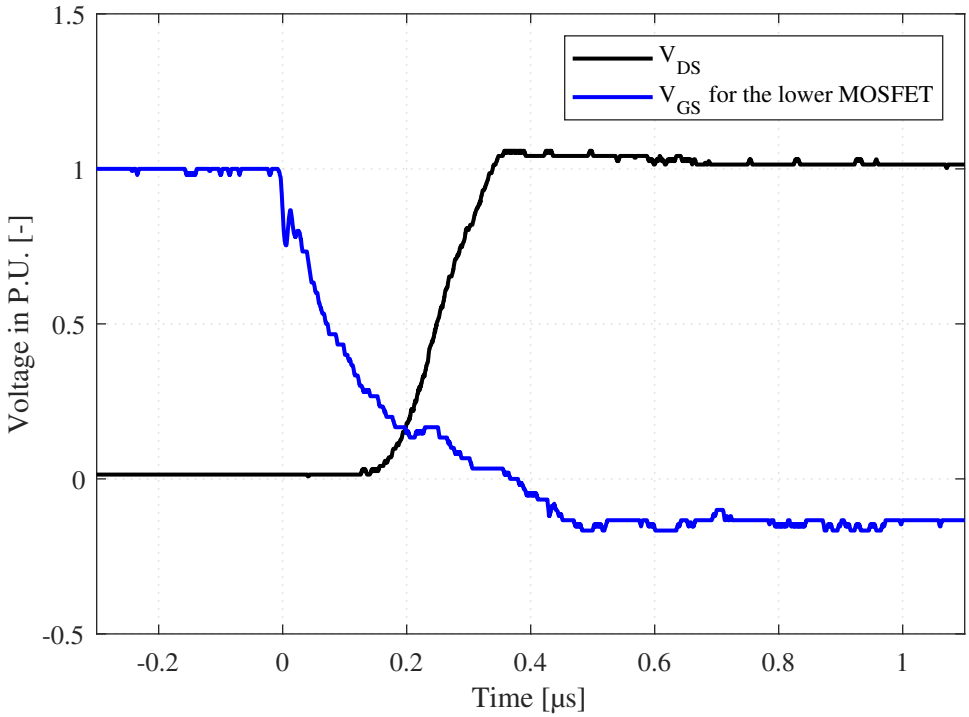


Figure 4.14: Measured drain-source voltage V_{DS} and lower MOSFET gate voltage V_{GS} during turn-off with negative current. Notice how it takes 150 ns for the phase voltage to start increasing after the gate starts to turn off. The voltages are shown in p.u. where $V_{\text{DS,base}} = 600$ V and $V_{\text{GS,base}} = 20$ V.

Figure 4.14 shows the C-phase and gate voltage during turn-off. It can be seen that there is a delay of 150 ns from when the gate voltage starts dropping to the switch starting to block the current. Together with the 355 ns visible in Figure 4.12 this adds up to 505 ns which corresponds to the inserted dead-time of 500 ns.

The dead-time should have been verified at full load as well, but since the inverter broke before full current was reached this was never measured.

4.3 DC-link

In this section, the capacitance needed in the DC-link will be identified and the current stress on the capacitors will be calculated. Finally some capacitor options will be shown.

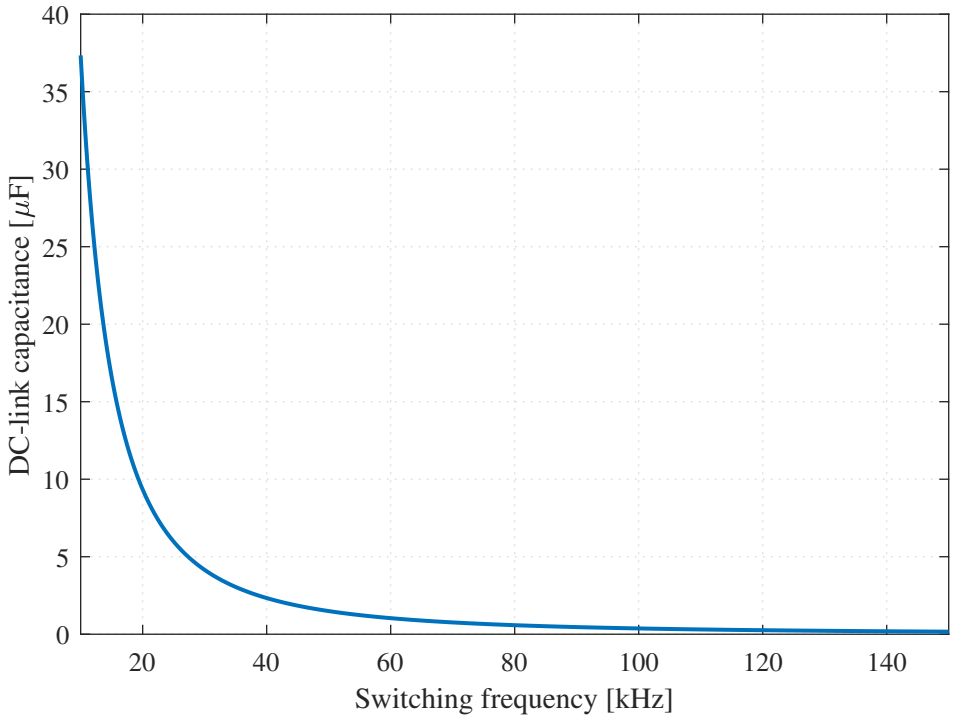


Figure 4.15: Minimum capacitance needed for the DC-link to limit the voltage ripple to 3.3 V at a battery voltage of 600 V with L = 1.5 mH depending on the switching frequency.

4.3.1 Capacitance

As mentioned previously, the DC-link needs to be properly designed to limit the voltage ripple over the battery. As can be seen in (2.38), the capacitance of the DC-link depends among other things on how much voltage ripple ΔU is allowed. The maximum voltage of the CFS battery is 580 V, while the maximum allowed battery voltage is 600 V. To prevent any ripple causing the battery voltage going higher than 600 V an allowed ripple of 3.3 V will be allowed. Using (2.38) with L = 1.5 mH, V_{DC} = 600 V and ΔU = 3.3 V and sweeping over f_{sw} the capacitance needed to limit the voltage ripple can be identified by selecting the lowest allowed switching frequency. However, as can be seen in Section 4.3.2 the limiting factor will become the current rating and not the capacitance.

Figure 4.15 shows the capacitance needed to limit the voltage ripple to the set value. As can be seen in (2.38), the capacitance is proportional to $\frac{1}{f_{\mathrm{sw}}^2}$. This means that the higher switching frequency that is used, the less capacitance will be needed. However, with increased switching frequency there is a higher requirement on the switching speeds which will lead to higher dV/dt and therefore problems appear with stray inductance and high demands on the drive circuit. The capacitance will be chosen to limit the voltage ripple within acceptable limits at f_{sw} = 50 kHz, which will therefore be the lower limit of allowed switching frequency in this inverter.

Table 4.4: Various capacitor candidates. Two MPF capacitors are presented as well as three ceramic alternatives. It can be seen that the ceramic capacitors are better at handling current stress while the MPF capacitors have a lower ESR.

Manufacturer		TDK	TDK	TDK	Vishay	Vishay
Series		FA series	SP series	LP series	MKP385e	MKP385e
Model number		B58035U7505M001	B58033I7106M001	B58031U7504M062	52712JPM2T0	53363KP[1]4T0
Capacitance	[µF]	2.5	5	0.25	2.7	3.3
Voltage (RMS)	[V]	700	700	700	1250	630
Voltage (Peak)	[V]	1000	1000	1000	2000	1008
Current (RMS)	[A]	26	33	7	19.3	11.7
ESR	[mΩ]	100	50	24	5	7
Material		Ceramic	Ceramic	Ceramic	MPF	MPF
Surface Area	[mm^2]	225.7	754.15	56	1260	795.5
Height	[mm]	9.1	11.5	4	45	35.5
Price	[SEK]	740	650	105	111	40
Volume	[mm^3]	2050	8670	112	56700	28200
I density	[mA/mm^3]	12.7	**3.80**	**31.3**	0.340	**0.414**
C density	[nF/mm^3]	1.22	0.576	1.12	0.0476	0.117

4.3.2 Current rating

Another of the design parameters of the DC-link capacitors is the current rating. They need to have a current rating such that they can handle the expected current stress. By using (2.36) and (2.39) the maximum current ripple and RMS current stress can be calculated. This gives that $\Delta I = 1.02$ A and $I_{\mathrm{C,RMS}} = 84.9$ A. This causes problems when choosing capacitors, and in turn leads to the current rating of the capacitor being the deciding factor and not the capacitance.

4.3.3 Capacitor selection

In Table 4.4 some capacitor alternatives are shown. These are just a selection of the capacitors that were investigated. What they have in common is that they can all be used for the application. It can be noted that none of these capacitors can carry the full current stress so it is required to connect multiple in parallel. The ceramic capacitors are shown to have quite high equivalent series resistance which should in turn cause them to heat up more. However, due to them being ceramic, they conduct heat better and therefore can handle a higher current than the Metallized Polypropylene Film (MPF) capacitors. One drawback is that they are more costly than the alternatives. However, when looking at the surface area they occupy, it can be noted that the the amount of MPF capacitors needed would take up much more space on the PCB.

The surface area used by the capacitors have an impact of where they can be placed on the PCB. To limit the stray inductance between the DC-link and the switches, the capacitors should be placed as close to the switches as possible. Therefore it is preferable that the capacitors occupy as small of a surface area as possible to make it easier to place them closer to the switches. Because of this, the two SP series ceramic capacitors as well as two LP series will be used. This gives a high current

rating over a very small surface area which enables a much more compact design of the power board. This means that the total capacitance is 10.5 µF resulting in a ripple of 469 mV at 50 kHz.

In addition to these ceramic capacitors a set of MPF capacitors were incorporated into the design of the power board. The reason for this was simply to have a contingency plan in case it would be shown during testing that more capacitance or current stress capability was needed. Thus the idea was never to actually use them, assuming that the calculations are correct. This made the power board (on which these capacitors are mounted) bigger, but overall risk for the project was reduced and in a future hardware revision these capacitors could potentially be removed from the design [5].

4.3.4 Experimental results

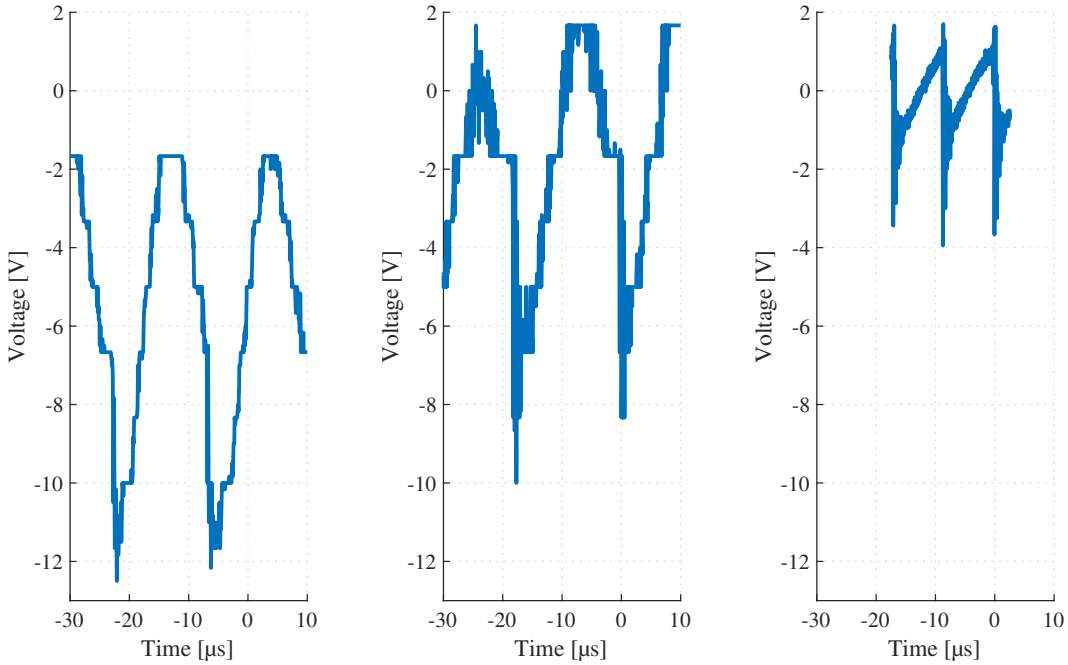
Because of the unfortunate hardware failure described in Section 4.1.2, the DC-link behaviour was not tested and studied in enough detail. For instance, no data was collected at 50 % duty cycle, which would have been interesting to see because that is the point where the ripple should be the worst according to (2.36). For the sake of transparency it was decided to present the data that was collected anyway, despite it's poor quality.

In Figure 4.16 three different test cases can be seen. In all of them, we can see the voltage ripple on the DC-link that is caused by the switching when the inverter is outputting 71 A RMS to the motor. By comparing Figure 4.16b with Figure 4.16c we can see that a doubling in switching frequency made the ripple decrease from around 11.5 V to 4.7 V, or by a factor of 2.4. According to (2.37) the voltage ripple should decrease by a factor of 4 when the switching frequency is doubled. One possible reason for this discrepancy could be noisy measurements. Another reason could be that the switch ripple contains high frequency components that the capacitors are not able to filter out. Interestingly, the shape of the waveform also changes from something that is between sinusoidal and triangular to something that looks more like a sawtooth pattern.

By instead comparing Figure 4.16a with Figure 4.16b we can see that a 20 % increase in bus voltage resulted an increase in ripple from 10.6 V to 11.5 V, or in other words an increase of 8.5 %. This is less than the linear dependency that (2.37) suggests. One explanation for this discrepancy is that the ceramic capacitors that were chosen have a significant capacitance variation at different voltage levels.

Another cause for concern is that the predicted magnitude of the ripple is completely wrong. Furthermore, correcting the capacitance to what is specified in the datasheet for 500 V, would result in a voltage ripple of 1.36 V and therefore higher than at 600 V, which is also not the case. These results are summarised in Table 4.5.

[5] Note that in the end, the MPF capacitors were never used. Thus, all results in this report were achieved with only the ceramic capacitors.



(a) 500 V, 30 kHz **(b)** 600 V, 30 kHz **(c)** 600 V, 60 kHz

Figure 4.16: DC-bus ripple waveform at three different operation points. Common for all three is that the inverter was outputting 71 A RMS during the test.

Table 4.5: Summary of DC-link voltage ripple results at three different test cases with an assumed total capacitance of 10.5 µF

Test case	Predicted [V]	Measured [V]
500 V, 30 kHz	1.09	10.6
600 V, 30 kHz	1.30	11.5
600 V, 60 kHz	0.326	4.70

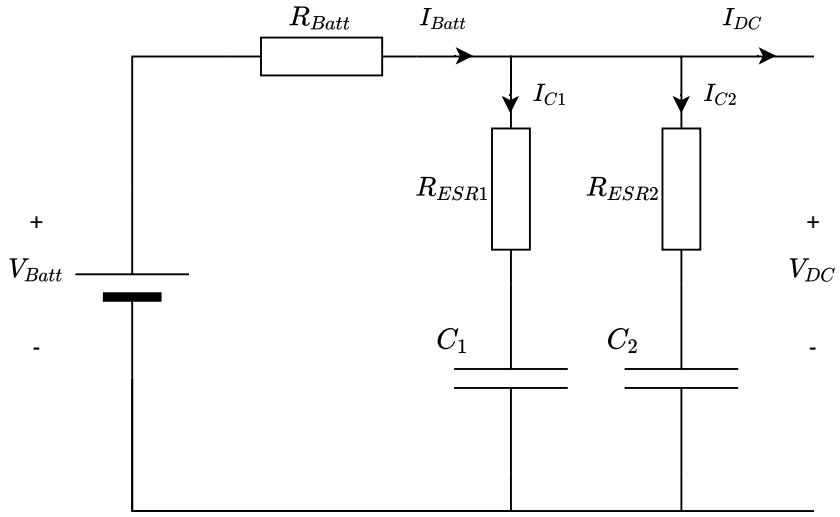


Figure 4.17: Equivalent schematic of the DC-link used in this thesis when including the capacitors' ESR. The capacitors' legs C_1 and C_2 are the equivalent of two additionally paralleled equal capacitors.

4.3.5 DC-link theory revisited

As can be seen in Section 4.3.4, the measured voltage ripple does not correspond to the predicted values, and are as much as 14.4 times bigger in test case at 600 V and 60 kHz. Furthermore, the theory shows that doubling the switching frequency should in turn result in a fourth of the voltage ripple which was not the case. Therefore a further analysis of this is required.

One major problem with the measurement is the uncertainty of the impact the power supply had on the voltage ripple. A Delta Elektronika SM-600-10 was used to power the inverter, but it should be expected that the power supply in itself wants to limit the voltage ripple to keep the desired voltage output. This could be corrected by inserting an inductor in series with the inverter to decouple the two systems. However, introducing more inductance in the system would create a resonant circuit which could in turn lead to further problems. Therefore great care needs to be taken when choosing the inductance to avoid self-resonance. To do these tests again would require a new inverter to be built since the device under test is now broken. As such, no new measurements can be taken which introduces a lot of problems with actually verifying the rest of this section. Still, an attempt at explaining the observed behaviour will be made.

The theory proposed in [13] uses a simplified version of a capacitor when deriving the equations used since they disregard the impact of the equivalent series resistance of the capacitor. This is not brought up in the paper and while it is a valid approximation when using low ESR capacitors such as film capacitors (which have a very low ESR, especially when multiple are usually used in parallel), the impact cannot be neglected when the ESR is high.

By including the ESR while excluding the equivalent series inductance, the equiva-

lent circuit would look like the one shown in Figure 4.17. This can be described as follows. The voltage over the battery can be calculated as

$$V_{\text{Batt}} = R_{\text{Batt}} I_{\text{Batt}} + V_{\text{DC}}. \tag{4.1}$$

Furthermore, we have that for both capacitors

$$C_1 \frac{dV_{\text{DC}}}{dt} = I_{\text{DC}} = \frac{V_{\text{DC}} - V_{\text{C1}}}{R_{\text{ESR1}}} \tag{4.2}$$

$$C_2 \frac{dV_{\text{DC}}}{dt} = I_{\text{DC}} = \frac{V_{\text{DC}} - V_{\text{C2}}}{R_{\text{ESR2}}}. \tag{4.3}$$

The currents can be described as

$$I_{\text{Batt}} = I_{\text{DC}} + I_{\text{C1}} + I_{\text{C2}} \tag{4.4}$$

and by inserting (4.2) and (4.3) into (4.4) we get,

$$I_{\text{Batt}} - I_{\text{DC}} = \frac{V_{\text{DC}} - V_{\text{C1}}}{R_{\text{ESR1}}} + \frac{V_{\text{DC}} - V_{\text{C2}}}{R_{\text{ESR2}}}. \tag{4.5}$$

By simplifying (4.5) and doing some rearranging the resulting DC-link voltage can now be calculated as

$$V_{\text{DC}} = \frac{(I_{\text{Batt}} - I_{\text{DC}}) R_1 R_2}{R_1 + R_2} + \frac{R_1 V_{\text{C2}}}{R_1 + R_2} + \frac{R_2 V_{\text{C1}}}{R_1 + R_2}. \tag{4.6}$$

This can then be implemented into MATLAB Simulink via a Laplace transform to simulate the entire system together with a PMSM. This was done by modifying an existing PMSM simulation used in the course *Electric Drives* at Chalmers, and provided by our supervisor Stefan Lundberg. By running this simulation at the same operation point as the last test in Table 4.5 the simulated values can be compared with the measured ones. It should be noted that an inductor is placed before the DC-link to force the capacitors to supply most of the current. The capacitors are implemented as two capacitors where C_1 is two 0.25 µF capacitors in parallel and C_2 is two 5 µF capacitors in parallel. The result of the simulation can be seen in Figure 4.18. It is very hard to see both I_{C1} and I_{Batt} since they are both very low compared to the other two currents. It should also be noted that the 5 µF capacitors share the majority of the current. This is due to the high ESR of the 0.25 µF capacitor forcing the current into the 5 µF capacitors via current sharing. Information about the motor used is available in [4].

Figure 4.19 shows the voltages in the same simulation as Figure 4.18, with the zoomed in part showing the resulting voltage ripple. As can be seen in Figure 4.19,

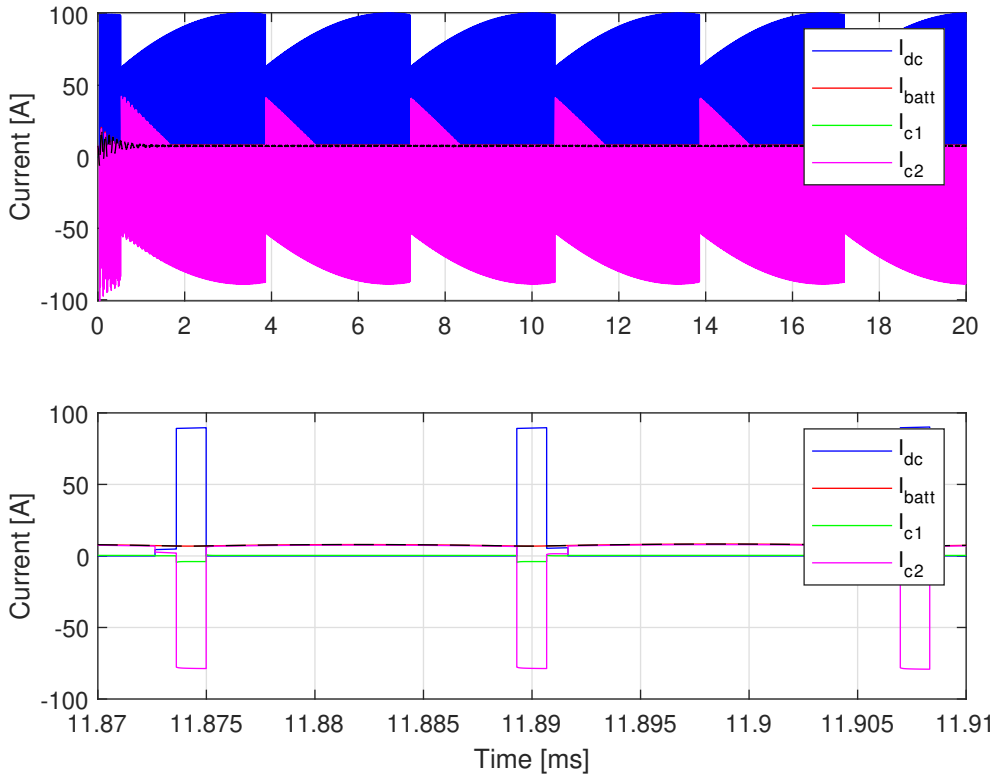


Figure 4.18: Upper plot shows the simulated currents of the DC-link over a switching period when running a PMSM at $I_{\mathrm{L}} = 71$ A RMS, $V_{\mathrm{DC}} = 500$ V and $f_{\mathrm{sw}} = 60$ kHz. Lower plot shows a more zoomed in plot with the most ripple.

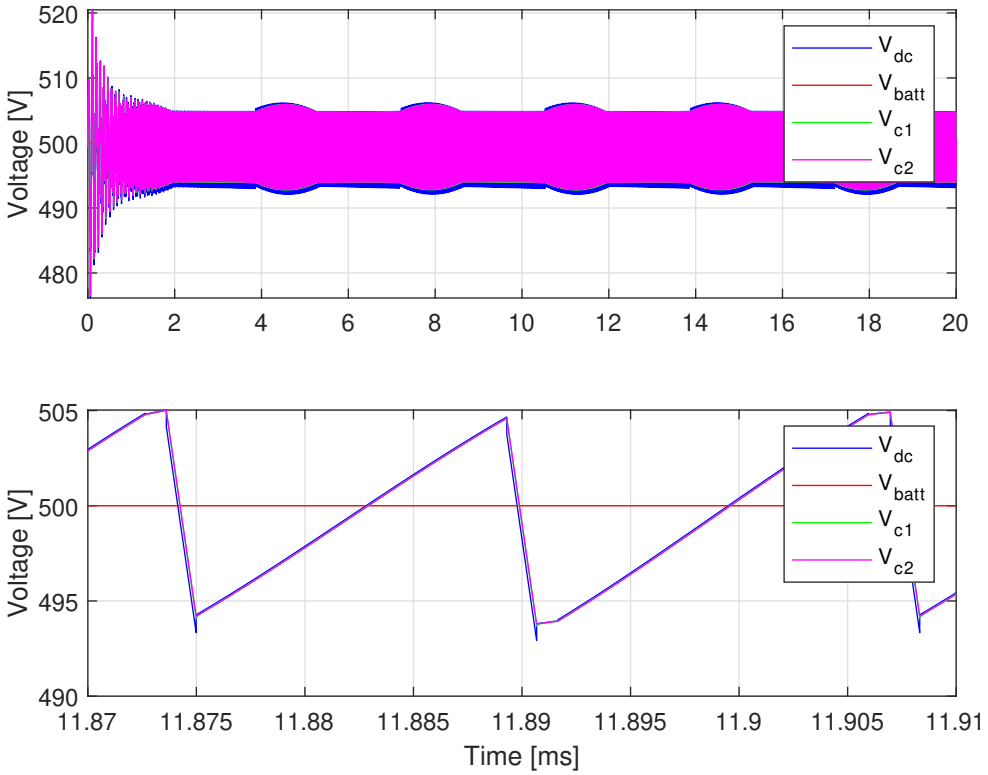


Figure 4.19: Upper plot shows the simulated voltages of the DC-link over a switching period when running a PMSM at $I_{\mathrm{L}} = 71$ A RMS, $V_{\mathrm{DC}} = 500$ V and $f_{\mathrm{sw}} = 60$ kHz. Lower plot shows a more zoomed in plot where the ripple is as highest can be seen.

the voltage ripple at 600 V and 60 kHz match quite well with the simulated values. A comparison of all the measured test cases and simulations together with the calculated values are shown in Table 4.6. There is a deviation, and furthermore the simulation does not follow the behaviour as expected from (2.38) where increasing the voltage while keeping the switching frequency the same should increase the voltage ripple. This further implies that something is wrong with the equation shown.

Table 4.6: Comparison of simulated, measured and calculated DC-link voltage ripple of the final design.

Test case	Calculated [V]	Measured [V]	**Simulated** [V]
30 kHz, 500 V	1.09	10.6	11.7
30 kHz, 600 V	1.3	11.5	9.9
60 kHz, 600 V	0.326	4.7	5.4

In [2], another method of calculating the current ripple is based around the term A·Sec. This can be derived by the capacitor current

$$I_{\text{cap}} = C\frac{dV}{dt}. \tag{4.7}$$

By rearranging this to solve for the capacitance we get

$$C = \frac{I_{\text{cap}}dt}{dV} \tag{4.8}$$

where $I_{\text{cap}}dt$ is called A·sec.

Since this is the amount of charge supplied by the capacitors, this would give the voltage ripple. By knowing the power factor and the modulation index M, a p.u. value for A·sec for the three operation points can be gotten from Figure 2.5 in [2]. The base value can the be calculated through (2.20) in the same report.

Table 4.7: Comparison between of the voltage ripple at the measured test cases as well as a new calculated ripple by the method presented in [2].

	30 kHz 500 V	60 kHz 500 V	60 kHz 600 V
M	0.16	0.14	0.14
Power factor	0.6212	0.6212	0.6212
A·sec PU	0.055	0.045	0.045
A·sec Base	3.4 mC	3.4 mC	1.7 mC
$\Delta V_{\text{DC,CalculatedNew}}$	17.81 V	14.57 V	7.29 V
$\Delta V_{\text{DC,Measured}}$	10.6 V	11.5 V	4.7 V
$\Delta V_{\text{DC,CalculatedOld}}$	1.09 V	1.3 V	0.326 V

As can be seen in Table 4.7 the method presented in [2] results in values closer to the measured values. However, the measured ripple is still just below half of the new calculated values. This error could be because the ceramic capacitors are quite sensitive to changes in temperature which has not been taken into consideration since the temperature of the capacitors was not measured during the test. These new calculated values does however seem closer to the real measurement and a new DC-link should be designed using the theory presented in [2]. This would require more research into the inverters operation since the ripple changes depending on modulation index as well as power factor. Therefore, the operating points of the inverter should be studied further as to find the highest ripple possible.

4.4 Current sensing

A list of sensor requirements was produced according to Table 4.8. From this table, a list of sensors that fulfil these requirements was produced as can be seen in Table 4.9. All of the sensors that are listed as valid happen to be of the hall effect type even though that was not a requirement.

Table 4.8: Current sensor requirements.

Property	Minimum	Motivation
Bandwidth [kHz]	100	Nyquist sampling theorem
Current capability [A]	170	Expected current
Availability	Yes	Must be possible to buy
Bi-directional	Yes	Bi-directionality is necessary for AC currents
Isolation voltage RMS [V]	1800	Mandated by the the FSG rules.

Table 4.9: Various valid current sensor options.

Property \ Manufacturer	LEM	Allegro	Melexis	AKM
	LA 150-TP	ACS773	MLX91216	CZ-3706
Bandwidth [kHz]	150	200	250	Unknown[6]
Accuracy [%]	0.5	1	See [7]	0.5
Max current [A]	212	200	See [7]	180
Isolation voltage RMS [V]	4300	4800	See [7]	3000
Area [mm^2]	1287	367	30	138
Height [mm]	33.5	7	1.5	2.25
Cost [SEK]	300	60	45	90

The Melexis MLX91216 does not provide a predefined path for the current, but is rather designed to measure the field strength over a PCB trace. This means that the implementation is more involved than the other two alternatives that already have a predefined current path. The LEM LA 150-TP requires a bipolar power supply, which the other two sensors do not require. The AKM CZ-3706 is an interesting choice because of its small size. However, while it can handle peaks of 180 A it can only handle 60 A continuously (and this is reduced further if heat is added from surrounding components). 60 A should be enough for normal operation, but does not allow extended overloading of the motor which might be interesting to do during testing. All in all, the Allegro ACS773 is the easiest to implement since it has a predefined current path, it can take the full current continuously and it only requires a single supply voltage. Therefore, this sensor was chosen.

[6]Bandwidth not specified in datasheet.
[7]Implementation dependent

4.5 Overcurrent protection

Following are the resulting circuits designed to handle the different overcurrent failure modes identified in Section 2.7.

4.5.1 Desaturation circuit

A desaturation circuit was also designed and placed on the gate driver board. The UCC21710-Q1 has a dedicated pin to detect overcurrent faults and a desaturation circuit was connected to it according to Section 2.7.1. An overcurrent limit was set at 350 A which is around two times the maximum allowed current through the motor. By picking $R_3 = 1$ kΩ, R_2 was calculated by solving (2.42) in regards to R_2. The blanking capacitor was then selected as $C_{\text{BLK}} = 100$ pF which resulted in a blanking time $t_{\text{BLK1}} = 276$ ns. To select R_1, care needs to be taken to ensure that the power loss over the resistor is not too high. For a 250 mW resistor this should then be selected as $R_1 > \frac{(V_{\text{DD}} - V_{\text{F}})^2}{0.25}$. For $V_{\text{DD}} = 20$ V and $V_{\text{F}} = 0.8$ V, the lowest resistance allowed should be $R_1 = 1475\ \Omega$. R_1 was then selected as 10 kΩ resulting in a second blanking time $t_{\text{BLK2}} = 92.1$ ns, resulting in a faster turn of at higher fault currents while remaining stable at lower fault currents.

The propagation delay of the UCC21710-Q1 from an overcurrent fault high to gate low is given as maximum 400 ns. Together with the Vincotech module's turn-off time, $t_{\text{d,off}} = 100$ ns, this would mean in case of an overcurrent, the MOSFET will turn off in less than 1 µs during both high and low fault currents, which is acceptable [16].

However, the circuit was never tested in real life due to measurements being extremely noisy. The gate drivers also turned off because of an overcurrent fault multiple times when there was no reasonable cause for it. This implies that the measured voltage was very noisy. The upper C gate driver also tripped more often than others, indicating a unique problem with that one which could be related to the PCB layout. This needs to be investigated further and all component values should be recalculated to maximise the capacitance.

4.5.2 Comparison circuit

Because of uncertain performance in the previously described desaturation circuit a contingency solution was also implemented, which is depicted in a simplified form in Figure 4.20. The circuit takes the current sensors' output signals as inputs (*I sense A*, *I sense B* and *I sense C*) to determine if an overcurrent event has occurred. It does so by taking the maximum of the three signals and comparing it to a reference value determined by the potentiometer. If the comparator outputs high, an overcurrent event has happened. The signal out from the comparator only is only high for the duration of the overcurrent event, and for that reason this signal is persisted with a lathing circuit to make sure that no further operation of the inverter is possible until the latch has been reset. The output signal from the latch can be used to drive all gates low, and thus putting the inverter in a safe state.

To prevent accidental trigger due to electrical noise, a low pass glitch filter was installed just before the signal goes in to the latch. The time constant of this filter has to be high enough as to not cause too much delay in case of a serious overcurrent event. This is not shown in Figure 4.20. Another important thing to note is that the circuit in Figure 4.20 is only half of the solution since it only checks for too large positive phase currents. For protection against excessive negative currents, an additional circuit with inverted logic was also used. This means that the diodes were flipped, the inputs to the comparator swapped and *R1* was pulled to *VCC* instead of ground.

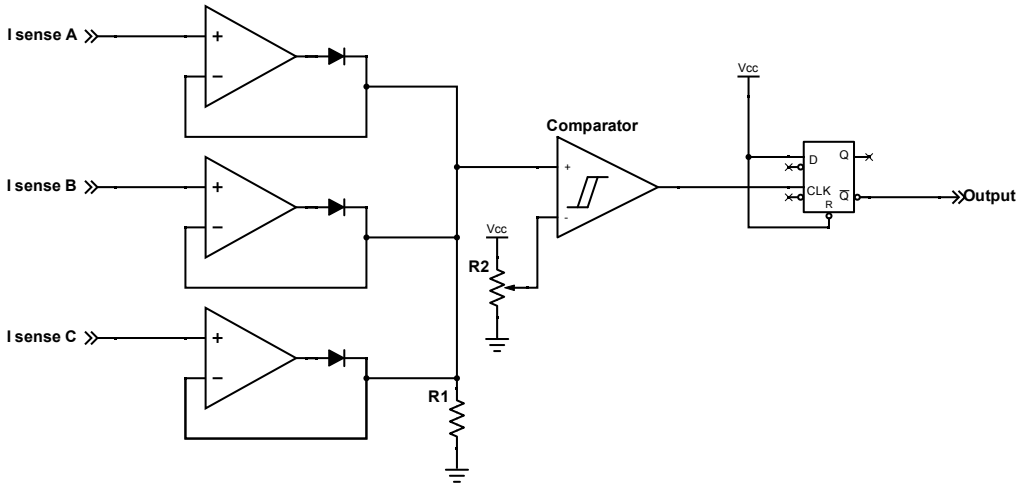


Figure 4.20: Simplified schematic showing how detection of excessive positive current is achieved. The current sensors' outputs are fed in as inputs to the circuit, and the output is used to drive the gates low in case of a detected overcurrent event. The trigger limit can be adjusted with a potentiometer.

The result is a circuit that is able to trigger overcurrent fault if the measured current is too high or too low (negative current is also considered). One potential problem with this circuit is that its response time is limited by the current sensor and any other components in the circuit such as the operational amplifier used to compensate to the voltage drop in the diodes. As mentioned in Section 2.7, a SiC power module might only survive a short circuit for as little as 3 µs. Thus, the total propagation delay from beginning of short circuit until current interruption should be kept lower than that to prevent critical device failure.

4.5.3 Motor protection circuit

The idea of making an analog circuit to mimic a melt fuse is to put the signal from a current sensor through a low pass filter, and to observe the output of this filter to determine if overcurrent has occurred. However, this is only a very brief description of the solution, and in reality it can be separated into a number of steps (which are also depicted in Figure 4.21:

- Current sensor

- AC to RMS equivalent DC
- Scaling
- Low pass filter
- Trigger point
- Latch

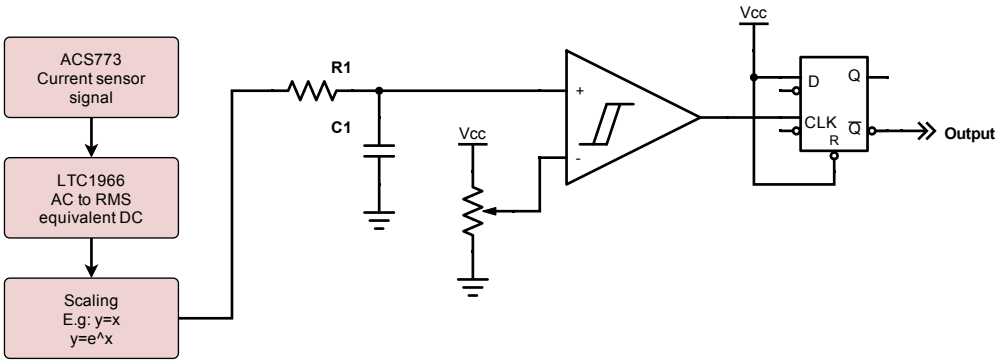


Figure 4.21: Simplified schematic showing the proposed motor protection circuit. This circuit protects one phase, and thus three are needed for full protection. A current sensor's output is fed in as input to the circuit, and the output is used to drive the gates low in case of a detected overcurrent event. The trigger limit can be adjusted with a potentiometer.

The signal produced by the current sensor (ACS773) is proportional to the motor phase current and centred around half of it's supply voltage. This means that before the signal can be fed into the low pass filter it has to be modified into an RMS heating equivalent signal. For this purpose the chip LTC1966 (which is an RMS to DC converter sometimes used in digital multimeters) was placed on the output of the current sensor. This has the effect of removing any DC-bias, as well as converting a sinusoidal signal into a DC signal.

The signal out from the LTC1966 can then be scaled in various ways before it is fed into the low pass filter. The simplest option is to not apply any scaling, but this might not yield the best performance. In Figure 4.22 and 4.23 no scaling (linear) is compared with scaling the current signal by squaring it or by applying an exponential scaling with base e to it. In practice, squaring an analog circuit requires analog multiplication which is not trivial. The exponential scaling option is easier to achieve since it only requires an operational amplifier, a diode and a resistor

The output from whatever scaling solution used can then be fed into the low pass filter. This filter should be tuned such that the overcurrent protection circuit trips after 2 seconds when a current of 200 A is applied to match the tripping characteristics of the reference fuse from IFÖ. The limit of 200 A was selected since

the current sensors (ACS773) are not able to measure much higher than that. For currents higher than or or equal to 200 A, the circuit in Section 4.5.2 will trigger directly.

The output from the low pass filter is then compared to a static voltage reference with an analog comparator, which in turn is connected to a latch. This means that if the current is above the set point for too long, the low pass filter output will rise beyond the static voltage reference, thereby triggering the comparator to send a signal to the latch which will remember the fault until manually reset. This signal can then later be used to prevent further operation of the inverter by turning off all MOSFETs in the VSI.

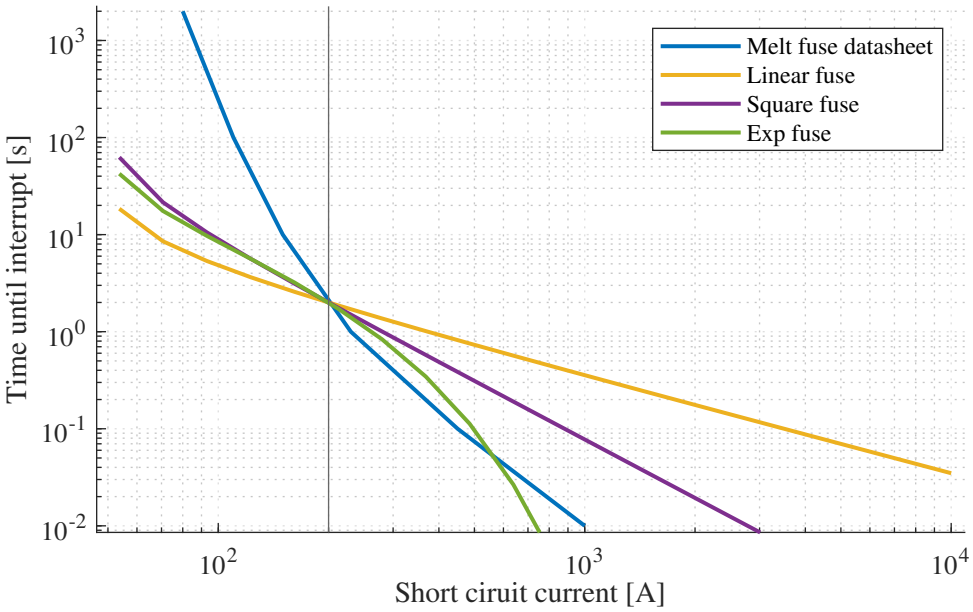


Figure 4.22: A comparison of different overcurrent protection solutions. Included in this comparison is a melt fuse (data points taken from datasheet [22]), a simulated circuit using the RMS current as input (linear), a simulated circuit using the square of the RMS current as input and a simulated circuit using the exponential of the RMS current (base e).

As can be seen from the simulated data in Figure 4.22 all proposed circuits react faster than the reference fuse for currents below 200 A, which make them at least as safe as the reference fuse. One potential problem could be that the proposed circuits are too sensitive; they might trip during normal operation. To test this the three different circuits were also tested using historic phase current data collected by CFS19 during an autocross run at a previous competition. This data represents a drive cycle type of load. As can be seen in Figure 4.23 none of the proposed circuits are too sensitive (i.e. none of the circuits ever trip). This means that all three types are feasible. Since the linear type is the simplest, that is the type that was designed and built. Unfortunately no verification data is available because of a prohibitive design mistake leading to the circuit never being fully operational.

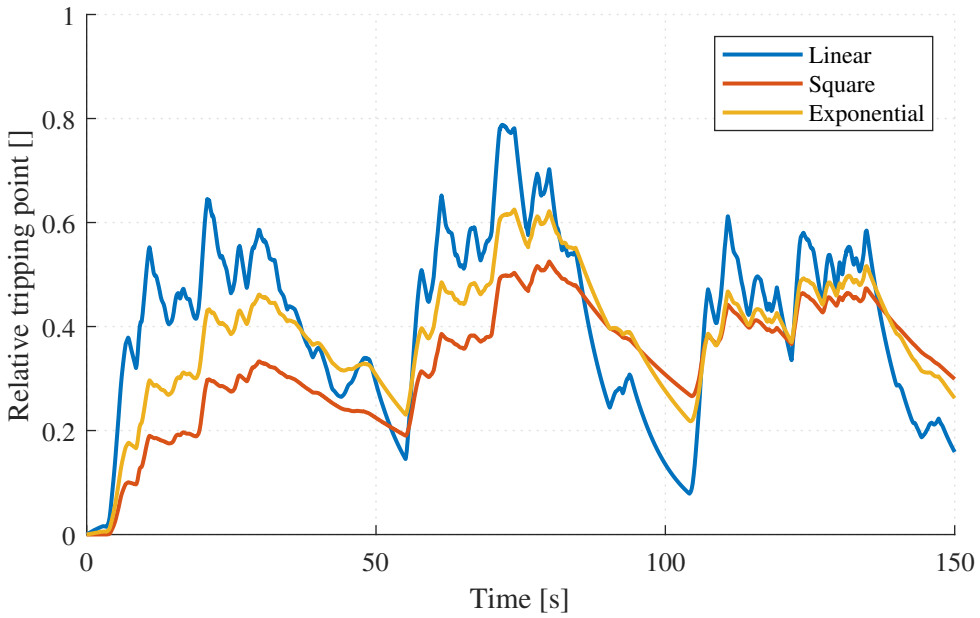


Figure 4.23: A comparison between the three different fuse circuits using current data from an autocross event. The curves are normalised such that if a signal reaches higher than 1 it is implied that an overcurrent event has occurred. In this case, neither of the circuits detected an overcurrent event.

4.6 PCB design

In this section the results of the PCB design will be presented. In total, four different PCBs were designed to fulfil all necessary functions of an inverter. This includes many low voltage circuits that have no academic value, but that are necessary or helpful for the project overall. As such, the focus of this section will be on the power board, since that is the PCB with all of the power components on it. For the sake of completion, the other PCBs will be discussed briefly as well.

To keep cost down, all PCBs were designed with only two copper layers even though this is not the best design in terms of signal integrity and noise rejection.

4.6.1 Power board

In Figure 4.24 two 3D renders of the resulting power boards are shown. The main functions of this PCB is to provide the DC-link, the switches, the current sensors and electrical connections. Additionally, this board provides a set of Y-capacitors, a voltage divider and discharge resistors.

The power board was designed to minimise the amount of stray inductance on the DC side of the switches. This was realised by implementing the current path for DC- and DC+ as similar planes on each side of the PCB. Because of the high voltage which the inverter operates at there is a need to have large isolation distances. For this reason the two planes can not be identical in shape which will lead to some

additional stray inductance.

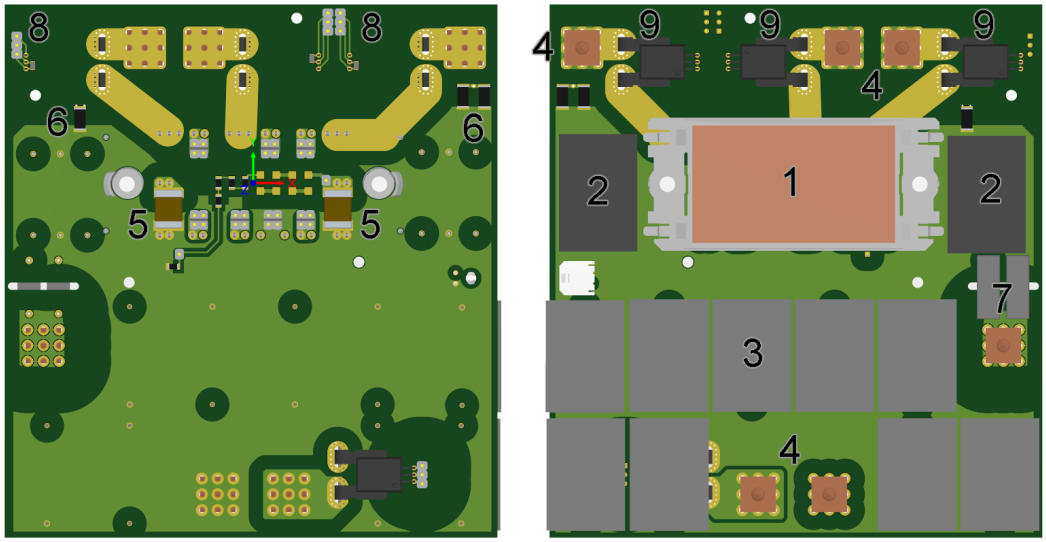


Figure 4.24: 3D render of the power board, front and back. 1: Power module. 2: SP type ceramic capacitors. 3: Film capacitors. 4: Power terminals. 5: LP type ceramic capacitors. 6: Discharge resistors. 7: Y capacitors and ground connection terminal. 8: Current sensor interface. 9: Current sensors.

The power board that was designed, built and tested is shown in Figure 4.24. It is a bit larger than the other PCBs to accommodate additional film capacitors. To show what is could be possible to build, assuming that additional capacitors are not needed, a mock-up of a smaller power board was made, which is shown in Figure 4.25. This board has a lower surface area as well as a lower height because of the removal of the film capacitors.

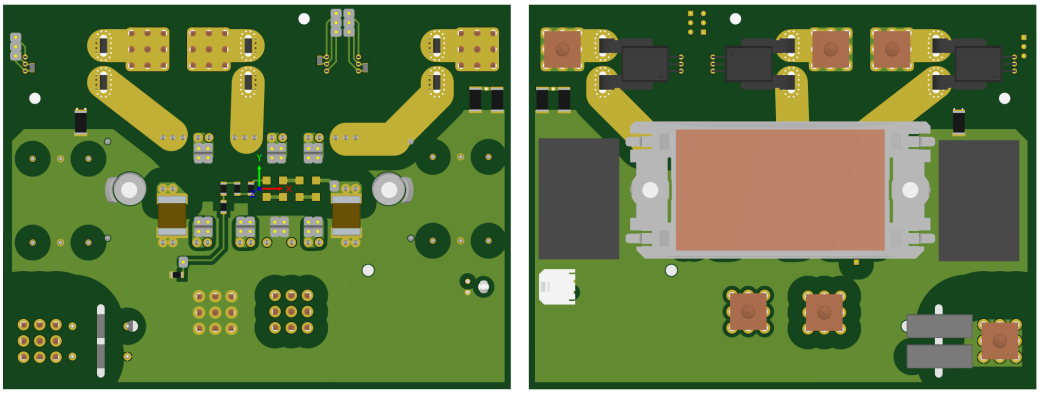


Figure 4.25: Mock-up of a smaller power board without film capacitors to show what is possible. The size of the PCB has been adjusted to be the same as the gate driver board and the communications board.

4.6.2 Gate driver board

The gate driver board's main purpose is to boost the signal from the processor such that it can safely turn on and off the MOSFETs such that the R_{on} of the MOSFETs are kept low. It also functions as galvanic isolation. This is accomplished by the IC UCC21710 from Texas Instruments, which also provides much of the desaturation functionality as well as galvanic insulation between the low voltage circuits and the high voltage circuits. In addition to this, for each gate there is a DC-DC converter that takes in 24 V from the low voltage side, and outputs 20 V and -5 V. These DC-DC converters are also galvanically insulated. The -5 V is then regulated down to -3 V through a voltage regulator as to not exceed the allowed lower gate voltage limit of the MOSFET.

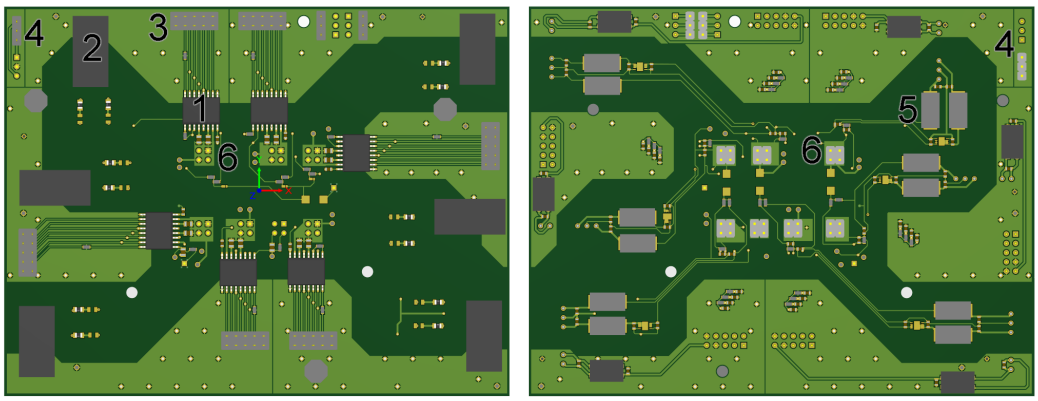


Figure 4.26: 3D render of the gate driver board, front and back. 1: Gate driver IC. 2: Isolated DC-DC converter. 3: Gate driver interface. 4: Current sensor interface. 5: Common mode chokes. 6: MOSFET gate interface.

4.6.3 Communications board

The communications board sits on top of the gate driver board and provides most of the low voltage circuits. Following is a list of some of the functions that this PCB provides:

- CAN
- RS232
- Overcurrent protection (high voltage and low voltage)
- Debugger
- Analog filters
- Electro-static discharge (ESD) protection
- Status LEDs

The communications board also provides the interface between the microcontroller and the gate drivers as well as all sensors. These functions will not be discussed any further in this section since they are outside the scope of this thesis. For more details about the high voltage overcurrent protection, see sections 2.7 and 4.5.

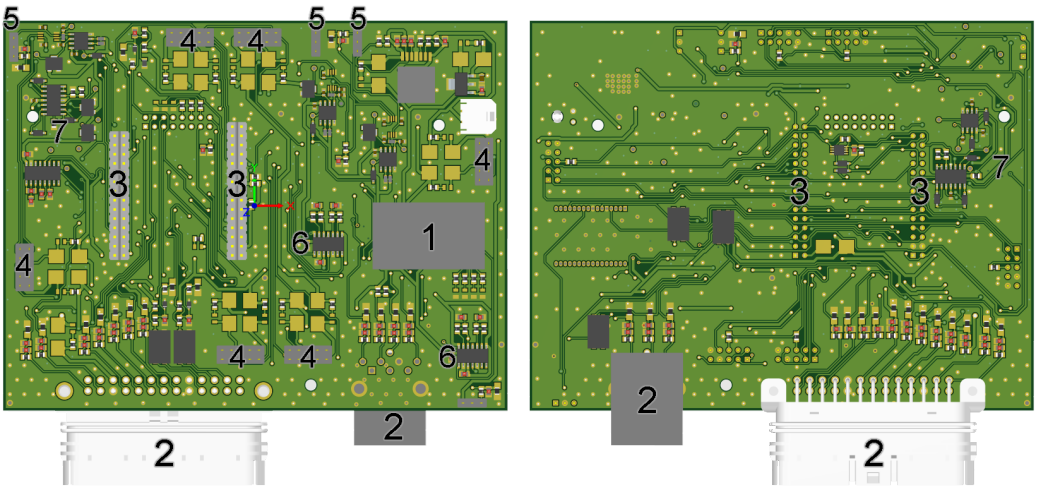


Figure 4.27: 3D render of the communications board, front and back. 1: On-board debugger. 2: Panel connectors to the environment. 3: Processor board interface. 4: Gate driver interface. 5: Current sensor interface. 6: CAN transceivers. 7: Analog overcurrent protections circuits.

4.6.4 Processor board

To make it easy to replace the microcontroller in case of device failure it was placed on a separate board which mates with the communications board using header pins. Additionally, all the necessary peripheral components (such as decoupling capacitors) were also placed on this board for the sake of proximity. The microcontroller used is an STM32H745, and a render of the PCB can be seen in Figure 4.28.

4.6.5 Assembly

The four PCBs presented are designed to fit together in a stack with pin and socket headers. The assembled inverter is shown in the photos in Figure 4.30, In Figure 4.29 a 3D render of the assembled board stack is shown. From this assembly measurements were taken, which are presented in Table 4.10. Additionally, a best case scenario where the MPF capacitors are removed and the power board is correspondingly made smaller is presented. A mock-up of this scenario is shown in Figure 4.25. The assembled inverter is shown in the photos in Figure 4.30 and for this inverter the larger power board is used.

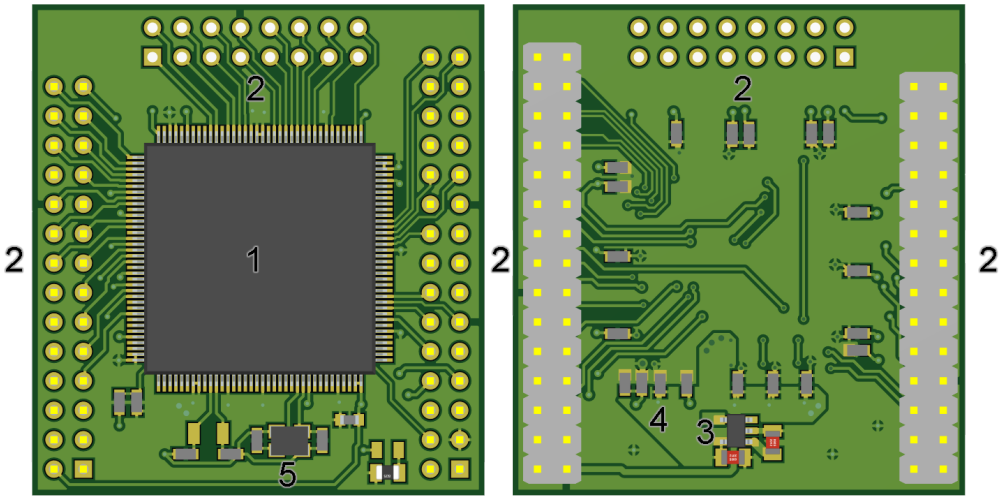


Figure 4.28: 3D render of the processor board, front and back. 1: Microcontroller. 2: Communications board interface. 3: 3.3 V regulator. 4: Decoupling capacitors. 5: Oscillator.

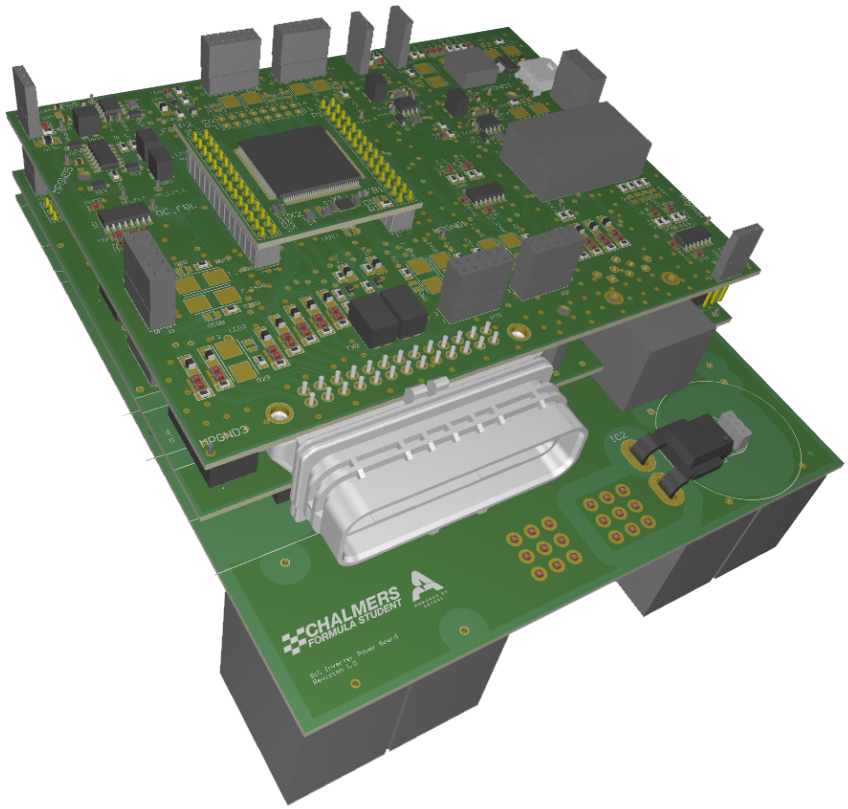
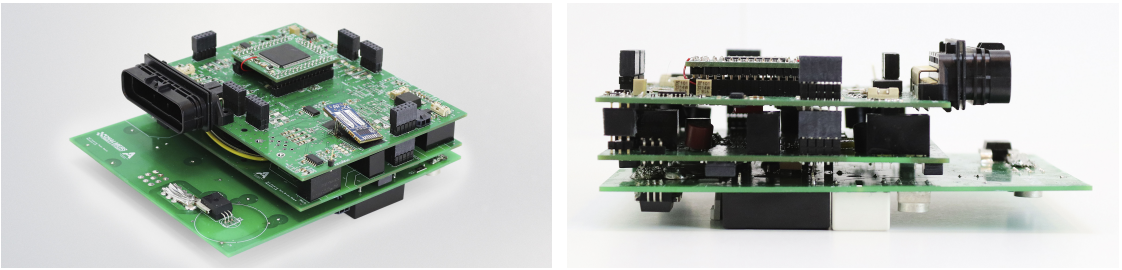


Figure 4.29: 3D render of the four PCBs assembled in a stack.

Table 4.10: Comparison of various product level properties, using the Aros High Power Cam - High Torque Density Formula Student inverter as a baseline comparison.

Property		As tested [8]	Best case [9]	Aros HPC-HTDFS
Height	[mm]	74.5	46	146
Width	[mm]	139	139	118.5 [10]
Length	[mm]	150	108	386
Volume	[l]	1.55	0.69	6.68
Reduction	[%]	**76.7**	**89.7**	N/A
Power	[kW]	34 [11]	34 [11]	34 [12]
Power density	[kW/l]	**21.9**	**49.2**	**5.1**
Mass	[kg]	0.46	<0.46[13]	3.5 [10]
Specific power	[kW/kg]	74	>74	9.7

As can be seen in Table 4.10, a volume reduction of 76.7 % was achieved, with possibility to reach up to 89.7 % reduction by removing the MPF capacitors. This also results in a power density of 21.9 kW/l, with a possibility to reach 49.2 kW/l by modifying the power board like previously discussed. The mass ended up at 0.46 kg with a specific power of 74 kW/kg. All of these comparisons have been made without a cooling solution, since that is outside of the scope of this project.



(a) Isometric view. **(b)** Side view.

Figure 4.30: Photographs of the device under test.

4.7 Total Harmonic Distortion

Figure 4.31 and 4.32 shows the currents as well as the FFT of the currents with the current controller using $\alpha = 100$ rad/s and $\alpha = 12000$ rad/s respectively. The

[8] The hardware that was actually built and tested.

[9] Reduced size as suggested in Section 4.6.1.

[10] Since the Aros HPC-HTDFS inverter is capable of driving two motors independently, the width and the mass presented is halved to keep comparisons fair.

[11] Unverified, but plausible. See Section 4.1.2

[12] Actual power capability is not public information, but for the purpose of Chalmers Formula Student this is what the inverter is capable of.

[13] This configuration was never built, and was therefore never actually possible to weigh. Since the only difference is that the power PCB would be smaller, the weight should be slightly lower than the device under test.

switching frequency was kept at 60 kHz and 2 Nm was requested by the controller. The motor was kept spinning at a constant electrical speed of 1500 rad/s. As expected the even harmonics are missing because of the half-wave symmetry of the sinusoidal current. Furthermore all multiples of three are cancelled because of the symmetric three-phase system. Thus only the fifth and seventh are really noticeable in Figure 4.31. With a higher bandwidth of $\alpha = 12000$ rad/s, the harmonics are suppressed. It should be noted that the 11th and 13th harmonic are also very low and the small bumps that are noticeable are not integers orders and therefore assumed to be noise.

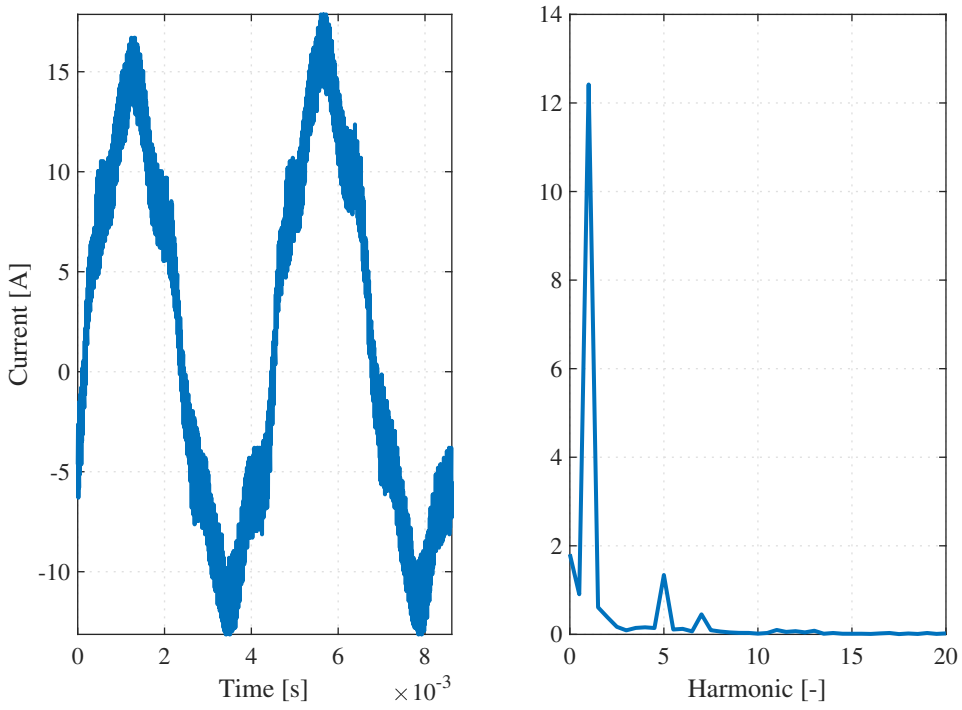


Figure 4.31: Currents at 2 Nm requested torque as well as the FFT of the measurement showing noticeable components of the fifth and seventh order. The speed was 1500 rad/s and the controller bandwidth was set to $\alpha = 100$ rads/s. The switching frequency was set to 60 kHz.

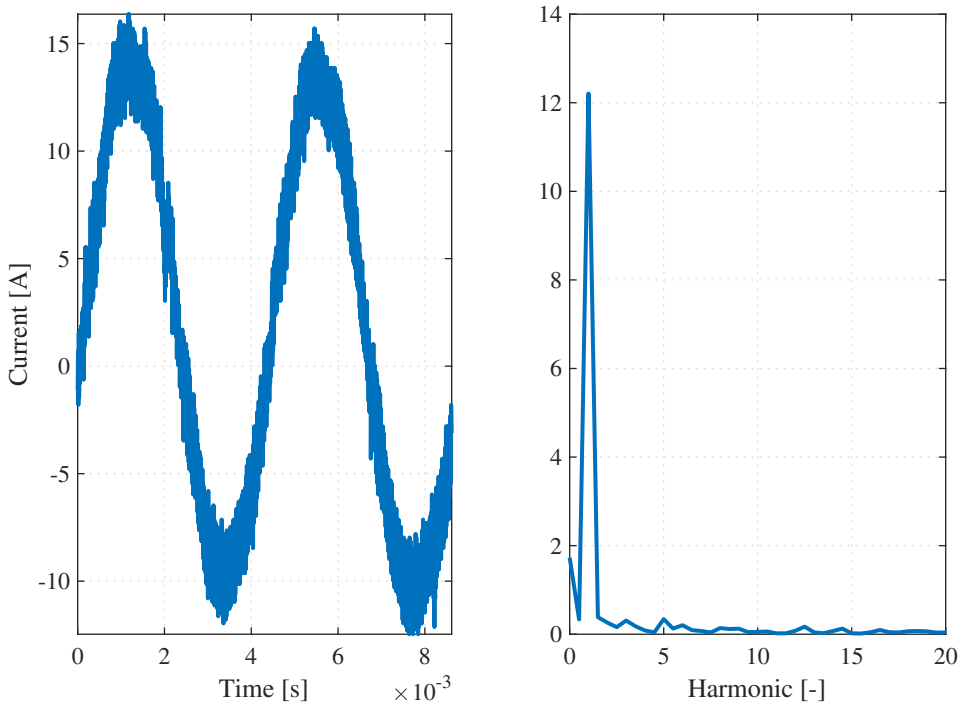


Figure 4.32: Currents at 2 Nm requested torque as well as the FFT of the measurement showing considerable smaller components of the fifth and seventh order compared to with a lower α. The speed was 1500 rad/s and the controller bandwidth was set to $\alpha = 12000$ rads/s. The switching frequency was set to 60 kHz.

The THD for both measurements are then $\text{THD}_{100} = 13.18\%$ and $\text{THD}_{12000} = 6.47\%$. Since the current is sampled at the peaks of the triangular carrier wave used to generate the PWM, it is sampled at twice the switching frequency. According to [9], an α of 12000 rad/s requires a sampling frequency of 20 kHz. Therefore it can be shown that by enabling a higher switching frequency of at least 10 kHz the distortion of the output current into the motor can be reduced.

It would however be interesting to study the THD at bandwidths both between 100 and 12000 rad/s as well as higher than 12000 rad/s. However, due to noise on the current measurements it was not possible to go higher than 12000 rad/s since the controller was so aggressive that it reacted on the noise. This means that even if it is theoretically possible to decrease the THD further, the current measurements become a limiting factor and unless improved, higher bandwidths are not possible. If the noisy current measurements are improved, then future work should further investigate the implications of the controller bandwidth on the THD.

5

Conclusions

A three phase voltage source inverter for use in a Formula Student car has been built and tested. A volume reduction of 77 % has been achieved, with a possibility for further reduction of up to 90 % in total withing grasp. This resulted in a specific power of 74 kW/kg and a power density of 22 kW/l, or up to 49 kW/l with suggested further improvements. Full current was not reached during testing, but the data seems to confirm the thermal modelling methods proposed, and full current might be possible with a flat cooling plate.

The inverter was designed to operate at a switching frequency of 50 kHz with phase currents up to 120 A RMS, but calculations show that frequencies up to 85 kHz should be possible. It has also been shown that compared to a reference IGBT solution, the proposed SiC solution could reduce the inverter losses by around 75 % if the inverter was instead designed to operate at 10 kHz.

The theory used to design the DC-link [13] was shown to be incorrect which resulted in approximately 10 times higher ripple voltage than predicted. An alternative method [2] was investigated which predicts the voltage ripple to less than a factor of 2. This theory does however show a dependency between the operation point of the inverter and the ripple. It was also possible to simulate the voltage ripple through a simple Simulink model that was shown to match very closely to the measured values. This should be further investigated with more operating points. Overall, further design and testing is required to ensure proper DC-link design methods.

It has been shown that with a higher switching frequency, a lower THD can be achieved. In one test case, the THD was reduced from 13 % to 6.5 %. The effects of this has not been fully explored, and in particular an evaluation should be made that compares motor efficiency and inverter efficiency at different switching frequencies.

A novel motor protection circuit has been presented and simulated with results indicating that it would act faster than a fuse, but still slow enough to avoid accidental tripping under short overload bursts. Because of a design error this circuit has not been verified, which is something that should be attempted in future work.

The desaturation circuit remained untested and caused problems because of be-

ing accidentally triggered by noise. The limits should be properly verified but the problem remains that they are very hard to access and measure on because of the compact design of the inverter and that any soldered cables will pick up so much noise from the switching that the measurements are rendered invalid.

The gate driver board required higher gate resistor values to reduce EMI and resulted in a slower turn-on and turn-off of the MOSFETs. This resulted in higher losses. It should be investigated if it is possible to use 1 Ω resistors and add snubber circuits to soften the switching.

Bibliography

[1] *Automotive ±10-A 5.7 kV RMS single channel isolated gate driver for SiC/IGBT with advanced protection*, Texas Instruments Incorporated, 2019, rev. B. [Online]. Available: https://www.ti.com/lit/gpn/ucc21710-q1

[2] X. Lu and F. Z. Peng, "Minimizing dc capacitor current ripple and dc capacitance requirement of the hev converter/inverter systems," in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 1191–1198.

[3] J. Zhu, H. Kim, H. Chen, R. Erickson, and D. Maksimović, "High efficiency sic traction inverter for electric vehicle applications," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 1428–1433.

[4] R. Lause and E. Lund, "Design and implementation of a pmsm control system for use in a formula student car," Master's thesis, Chalmers University of Technology, Gothenburg, 2020.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics. Converters, Applications and Design*, 3rd ed. John Wiley and Sons, Inc, 2003.

[6] S. Lundberg, "Performance comparison of wind park configurations," Chalmers University of Technology, Department of Electric Power Engineering, Tech. Rep., 2003.

[7] I. Colak, R. Bayindir, and E. Kabalci, "A modified harmonic mitigation analysis using third harmonic injection pwm in a multilevel inverter control," in *Proceedings of 14th International Power Electronics and Motion Control Conference EPE-PEMC 2010*, Sep. 2010, pp. T2–215–T2–220.

[8] M. Sajitha, J. Sandeep, and R. Ramchand, "Comparative analysis of different modulation techniques for three level three phase t-type npc inverter," in *TENCON 2019 - 2019 IEEE Region 10 Conference (TENCON)*, 2019, pp. 1529–1534.

[9] L. Harnefors, *Control of Variable-speed Drives*. Applied Signal Processing and Control, Department of Electronics, Mälardalen University, 2002.

[10] M. H. Rashid, H. S. H. Chung, K. Afridi, J. M. Alonso, I. Batarseh, A. Bryant, J. Carrasco, L. Chaar, A. K. Chattopadhyay, , and M. Chow, *Power Electronics*

Handbook : Devices, Circuits and Applications, 2nd ed. Elsevier Science & Technology, 2006.

[11] D. Shmilovitz, "On the definition of total harmonic distortion and its effect on measurement interpretation," *IEEE Transactions on Power Delivery*, vol. 20, no. 1, pp. 526–528, 2005.

[12] X. Mao, R. Ayyanar, and H. K. Krishnamurthy, "Optimal variable switching frequency scheme for reducing switching loss in single-phase inverters based on time-domain ripple analysis," *IEEE Transactions on Power Electronics*, vol. 24, no. 4, pp. 991–1001, 2009.

[13] M. Salcone and J. Bond, "Selecting film bus link capacitors for high performance inverter applications," in *2009 IEEE International Electric Machines and Drives Conference*, May 2009, pp. 1692–1699.

[14] J. W. Kolar and S. D. Round, "Analytical calculation of the rms current stress on the dc-link capacitor of voltage-pwm converter systems," *IEE Proceedings - Electric Power Applications*, vol. 153, no. 4, pp. 535–543, July 2006.

[15] TI Designs, "Current sensing with <1-µs settling for 1-, 2-, and 3-shunt foc inverter reference design," http://www.ti.com/lit/ug/tiducy7/tiducy7.pdf, 2019, [Online; accessed 2020-01-10].

[16] P. Diaz Reigosa, H. Luo, F. Iannuzzo, and F. Blaabjerg, "Investigation on the short circuit safe operation area of sic mosfet power modules," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–6.

[17] Formula Student Germany. (2019) FS Rules 2020 V1.0. https://www.formulastudent.de/fileadmin/user_upload/all/2020/rules/FS-Rules_2020_V1.0.pdf, accessed 2019-11-07.

[18] C. BUTTAY. (2006) Static characteristic of a imaginary insulated gate bipolar transistor (igbt). File: IvsV IGBT.png. [Online]. Available: https://commons.wikimedia.org/wiki/File:IvsV_IGBT.png

[19] Krishnavedala. (2011) Drain current as a function of the drain-to-source voltage and the gate-to-source bias over the threshold voltage. File: IvsV_mosfet.png. [Online]. Available: https://commons.wikimedia.org/wiki/File:IvsV_mosfet.svg

[20] M. Tooley, *Electronic Circuits: Fundamentals and Applications*, 5th ed. Taylor & Francis Group, 2019.

[21] W. Seruyange and K. Alomari, "Conceptual design and development of a traction power electronic converter," Master's thesis, Chalmers University of Technology, Gothenburg, 2017.

[22] IFÖ Electric. (2020) TECHNICAL DATA, HICAP ECO NH Fuse links. http://www.ifoelectric.com/eng/pdf/ifohicap_tekniska.pdf, accessed 2020-01-10.

[23] *Triple phase leg SiC MOSFET Power Module*, Microsemi Corporation, 2019,

rev. 0. [Online]. Available: https://www.microsemi.com/document-portal/doc_download/134005-aptmc120tam12ctpag-rev0-datasheet

[24] *flowPACK 1, 100 A Sixpack*, Vincotech GmbH, 2019, rev. 1. [Online]. Available: https://www.vincotech.com/fileadmin/user_upload/product_media/Vincotech_10-PG126PA010MR-L820F88T_FD-Rev_01.pdf

[25] *Dual 1200 V CoolSiC™ MOSFET Module*, Infineon Technologies AG, 2019, rev. 2.1. [Online]. Available: https://www.infineon.com/dgdl/Infineon-FF8MR12W2M1_B11-DataSheet-v02_01-EN.pdf?fileId=5546d46266a498f50166c59001393828

[26] *1200 V, 400 A Silicon Carbide Switching-Loss Optimized XM3 Half-Bridge Module*, Wolfspeed, 2019, rev. -. [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/1563/product/430/cab400m12xm3.pdf

[27] *Phase leg Fast Trench + Field Stop IGBT Power Module*, Microsemi Corporation, 2012, rev. 2. [Online]. Available: https://www.microsemi.com/document-portal/doc_download/7757-aptgt200a120g-datasheet

[28] *3000 series coldplate for the Wolfspeed XM3 module*, Wieland MicroCool, 2014. [Online]. Available: https://www.richardsonrfpd.com/docs/rfpd/CP3012.pdf

[29] *RxxP2xxyy DC/DC Converter*, RECOM, 2020, rev. 6/2020. [Online]. Available: https://recom-power.com/pdf/Econoline/RxxP2xxyy.pdf

A

Appendix 1

Author:	Date:	Rev:	Rev date:
UTV/BJ	2018-02-22	A	-

Technical data sheet
CFS18 stator/rotor

Stator/rotor

Active dimensions: D/d-L = 90/50-70 mm
Stator stack: 01-1010_Prel-B / 01-1011_Prel-B
Rotor: 2 x 01-1009_Prel-A
Rotor inertia: 1.37 kg*cm^2 /rotor section

Winding

Number of windings: 9
Phase interconnection: 3 in parallel per phase (1,4 and 7 etc), Y-connection
Number of winding turns: 41
Winding wire: Ø 1.12 mm (core dia)
Amount of winding wire: ~600 g
Phase to phase resistance: 100 mOhm ±5%
Phase to phase EMF: 55.9 VRMS ±5% @ 4000 rpm
Rated voltage: 600 VAC
High voltage testing (windings and temp. sensor): 1000 VAC, 2s and max 0.1 mA
Temperature class: F
Temperature sensor: KTY84 - 130

Cooling

Type: Circulating water, with optional antifreeze and anti-corrosion additives
Coolant inlet temperature: max 40 °C @ rated output power
Volume flow: min 9 l/min @ rated output power (ΔT 5 K)
Winding temperature increase: ~13 K/s @ peak torque

Performance

Rated torque: 10.8 Nm
Peak torque: 24.1 Nm

Rated speed: 11900 rpm
Max mechanical speed: 20000 rpm

Rated output power: 13.5 kW
Peak output power: 32 kW

Motor current: 48 A @ rated output power

Efficiency: 91% @ rated output power

Figure A.1: Datasheet for the CFS motors.

B

Appendix 2

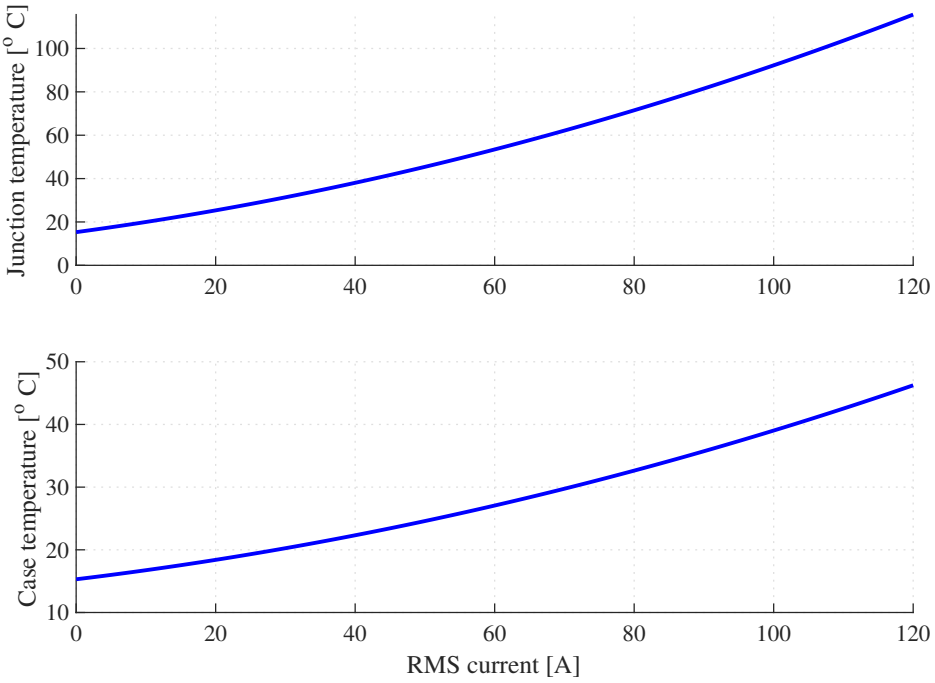


Figure B.1: Steady state temperatures of the selected module from Vincotech (10-PH126PA010MR-L820F86T) over different load currents. Coolant temperature adjusted to 15 °C and switching frequency adjusted to 30 kHz to represent real world test conditions.