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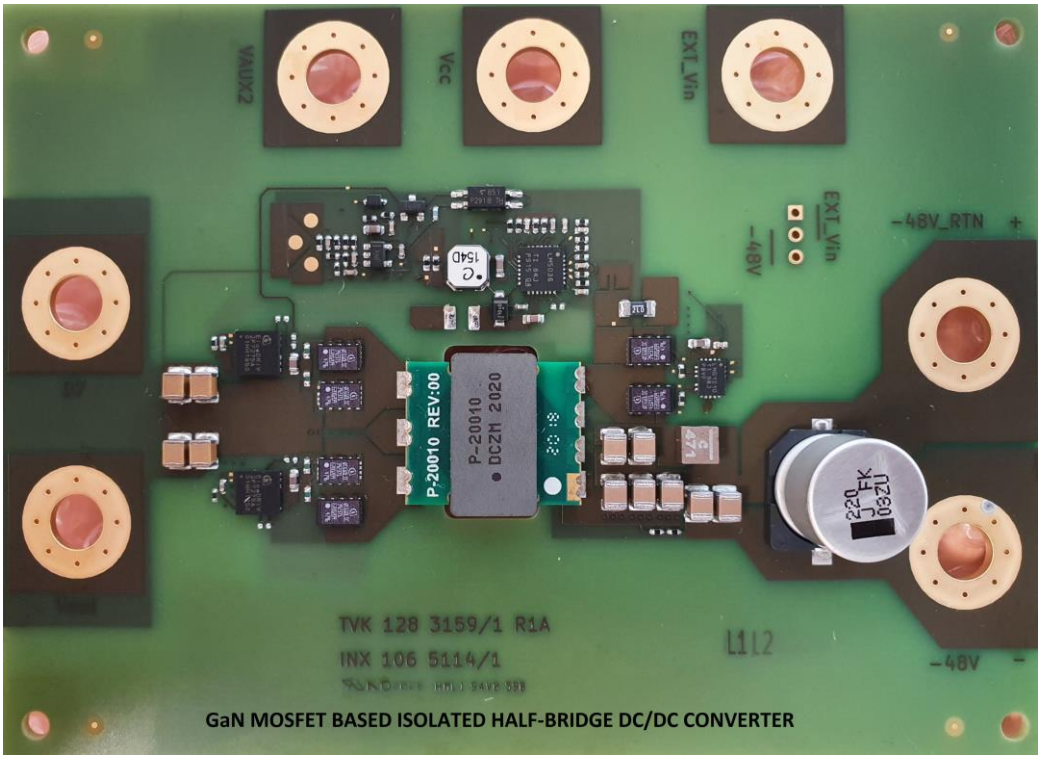

Design of Gallium Nitride MOSFET based DC/DC converter

Master of Science thesis in Electric Power Engineering

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Abstract

Most of the DC/DC converters operate with Silicon (Si) based MOSFET because of the matured technological advancements. Although it has the capability and the performance, new material like the Gallium Nitride MOSFET is offering better electrical performance in small package size. Hence, the Gallium Nitride (GaN) MOSFET is used in a DC/DC converter and its investigated.

The thesis focuses on the reduction in the module size with similar efficiency in comparison with the benchmarked Ericsson developed Silicon (Si) MOSFET based DC/DC converter. However, operating at the high switching frequency yields reduction in the overall converter module size. At the high frequency of 600 kHz, the planar ER18 transformer is designed with 40% reduction in the core area. Furthermore, the overall design of the GaN MOSFET based half-bridge DC/DC converter yields 27.8% shrinkage in the total power-train area.

Also, the efficiency of the GaN MOSFET based DC/DC converter is studied. From the simulation model, an overall efficiency of 94% is observed. In the hardware testing, the benchmarked Si MOSFET based half-bridge DC/DC converter yielded a maximum efficiency of 94.6% and the GaN MOSFET based half-bridge DC/DC converter achieved a maximum efficiency of 93.6%.

Keywords: Gallium Nitride MOSFET, Silicon MOSFET, Planar ER18 transformer, DC/DC converter, Efficiency

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Dinesh Raju and Prajwal Kuduvalli Srikanth, Gothenburg, November 2020

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1

Introduction

This chapter presents the background of the DC/DC converter and its development. Furthermore, the study describes the aim of the thesis and scope associated with it.

1.1 Background

For decades, one of the most popular power electronic switches (PES) are made of silicon (Si). Lots of research and development have been carried out to improve the performance of the Si MOSFETs, but currently, there is no drastic improvements [1]. Hence, the researchers started investigating different materials for better optimization. The most promising material is the gallium nitride (GaN) due to its wurtzite crystal structure. Generally, PES made from the wide band gap (WBG) semiconductor materials such as silicon carbide (SiC) and GaN offer much lower on-state resistance R_{ds-on} when compared to Si because of their high electron mobility, larger breakdown voltages and they can operate at high ambient temperature [2].

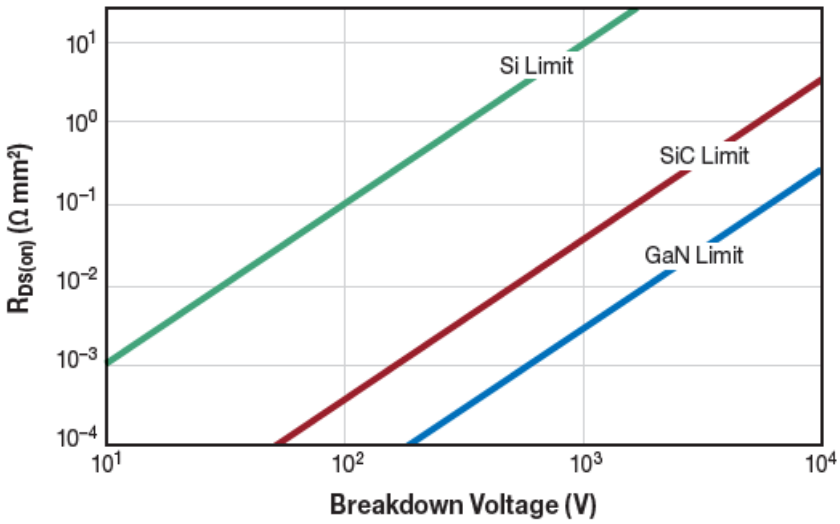

Figure 1.1: Theoretical R_{ds-on} for a one square millimeter device versus blocking voltage capability for Si, SiC, and GaN based power devices [1] [3].

GaN power transistors exhibit a high density of crystallographic defects due to their physical structure, this affects the electrical properties of the GaN material [2].

However, GaN power transistors are suitable for low power applications because of their lower thermal conductivity. Aiding to its performance, it has zero reverse recovery loss. Additionally, the overall size of the device is smaller than the Si power transistors, and it can operate at high frequencies. On the other hand, operating at high frequency, the GaN and SiC MOSFETs having lower gate and output charges creates high $\frac{dv}{dt}$ stress [2]. In this thesis, a performance comparison of Si and GaN MOSFET based isolated half-bridge DC/DC converter is made.

1.2 Previous work

There has been a lot of research on the development of GaN MOSFET based DC/DC converters aiming to minimize the overall losses [4]. A DC/DC converter operating with soft switching topology provides better efficiency in comparison with hard switching [5] [6]. However, there is insufficient information that aims for the overall module size reduction of a hard switching GaN MOSFET based isolated half-bridge DC/DC converter.

1.3 Purpose

The purpose of this thesis is to reduce the size of the GaN MOSFET based DC/DC converter module and achieving similar or higher efficiency in comparison with the currently used Si MOSFET based DC/DC converter at Ericsson AB.

1.4 Scope

The thesis focuses on the development of a GaN MOSFET based isolated half-bridge DC/DC converter with a similar specification of a benchmarked Si MOSFET based half-bridge DC/DC converter at Ericsson AB. In this thesis, hard switching of a GaN MOSFET based isolated half-bridge DC/DC converter is designed with high switching frequency by having reduced module size as a priority and similar efficiency as the existing DC/DC converter.

In this thesis, the design of the DC/DC converter is limited to voltage mode control with input voltage feedforward. The analog half-bridge pulse width modulation (PWM) based controller operating on the primary side of an isolated DC/DC converter is considered. To reduce the electrical stress across the PES, the thesis concentrates on the designing and implementation of passive snubbers. Furthermore, the design of a heatsink is excluded but can be incorporated if necessary.

2

Theory

In this section, the characteristics of the DC/DC converter and its associated components are explained.

2.1 DC/DC Converter

DC/DC switch mode converters are widely in use in different industries, for instance in telecommunication and automotive sector [7]. To have a regulated and desired DC voltage, converters with different topologies play a vital role. Additionally, isolation is provided to achieve galvanic isolation in the converter. Hence, most of the converters are designed with an electrically isolated transformer. In this thesis, the losses due to switches, inductors, and capacitors are considered.

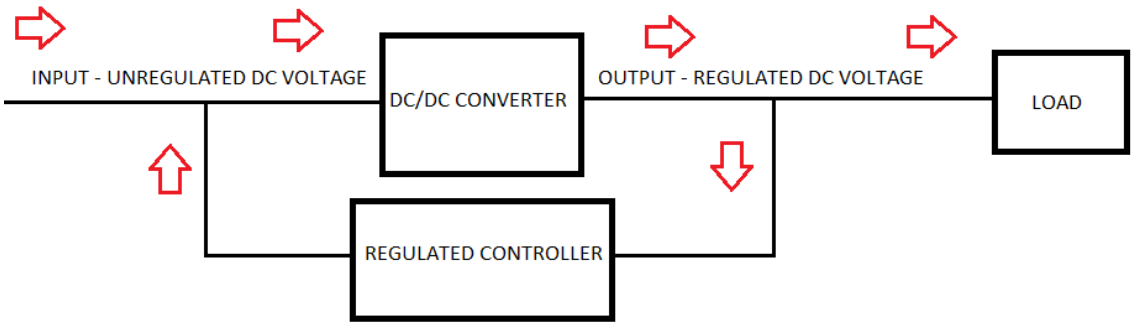

Figure 2.1: Basic block diagram of switch mode DC/DC converters [8].

The average DC output voltage may vary due to an unregulated input DC voltage if there is no closed-loop control. As shown in figure 2.1, the output DC voltage V_O is controlled by a controller. In PWM switching, V_O is regulated by varying the duty ratio D

$$D = \frac{t_{on}}{T_s} \tag{2.1}$$

where t_{on} is the pulse on duration and T_s is the total switching period.

These converters can operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). This thesis mainly focuses on the DC/DC converter operating in CCM condition.

2.1.1 Classification of DC/DC converters

In this section, the classification of DC/DC converters based on isolation and type of switching is discussed.

2.1.1.1 Based on isolation

A DC/DC converter can be of a non-isolated or an isolated type. In a non-isolated power converter, a common ground is shared between the input and the output. However, operating with a non-isolated power converter provides better efficiency, reduction in size and cost compared to an isolated power converter.

In an isolated DC/DC converters, a transformer is used to provide isolation between the primary and the secondary circuits. The transformer core can be excited in both unidirectional and bidirectional direction. This thesis mainly focuses on the transformer-based isolated DC/DC converter with zero airgaps in the core and having a bipolar core excitation. Table 2.1 shows different types of isolated DC/DC converters with maximum switching voltage.

Table 2.1: Different types of isolated DC/DC converters with maximum switching voltage

Topologies	Maximum switching voltage
Flyback DC/DC converter	$V_{in} + V_O \cdot (\mathrm{N}_P/N_S)$
Two-switch flyback DC/DC converter	V_{in}
Forward DC/DC converter	$2 \cdot \mathrm{V}_{in}$
Two-switch forward DC/DC converter	V_{in}
Active clamp forward DC/DC converter	$(V_{in}/(1\text{-}D))$
Half-bridge DC/DC converter	V_{in}
Push-pull DC/DC converter	$2 \cdot \mathrm{V}_{in}$
Full-bridge DC/DC converter	V_{in}
Phase shifted full-bridge DC/DC converter	V_{in}

where N_P and N_S are the primary and the secondary turns of a transformer-based isolated DC/DC converter.

2.1.1.2 Based on type of switching

A DC/DC converter can be of a hard switching or a soft-switching topology. In a soft-switching DC/DC converter, the resonant circuit is used for the transistor time commutation, which reduces the switching losses and electromagnetic interference (EMI).

In a hard switching DC/DC converter, the power electronic switches are operated at a specific switching frequency. But, operating at high switching frequency creates an increase in the EMI and stress across the PES. However, the electrical stress developed across the PES can be eliminated by incorporating snubbers. Also, by

having a low pass filter, the effect of the EMI can be minimized. Additionally, the hard switching DC/DC converter exhibit lower efficiency in comparison with the soft-switching DC/DC converter.

2.2 Design specification

In this thesis, the GaN MOSFET based DC/DC converter is designed to operate at 600 kHz. A nominal input voltage of −48 V is applied on the primary side of a GaN MOSFET based half-bridge DC/DC converter. The output voltage of the converter is expected to be 9 V and the output power to be 250 W. Table 2.2 shows the design specifications of the GaN MOSFET based isolated half-bridge DC/DC converter.

Table 2.2: Specification of the GaN MOSFET based isolated half-bridge DC/DC converter.

Parameter	Values
Input voltage	−48 V
Output voltage	9 V
Output power	250 W
Operating frequency	600 kHz
Output current	27.8 A
Output ripple current	30%
Output ripple voltage	03%

2.3 Half Bridge DC/DC converter

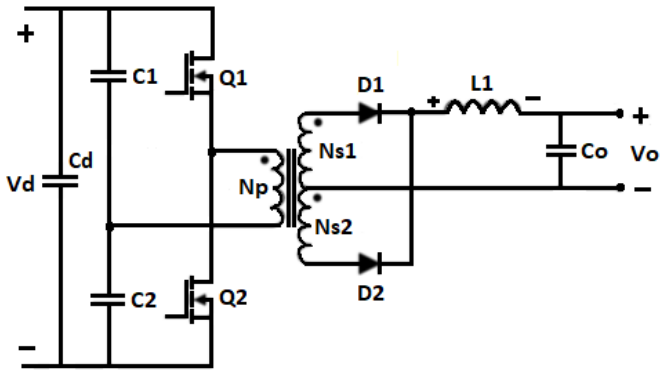

Figure 2.2: Basic schematic of an isolated half-bridge DC/DC converter.

Half-bridge DC/DC converter operates as a step-down converter, where V_O is controlled by using a pair of PES at the input. Traditionally, it consists of a bulk capacitor C_d, which reduces the input voltage ripple and the primary side capacitors

C_1 and C_2 provides a constant mid-point voltage. A half-bridge DC/DC converter consists of an isolated transformer with bi-directional core excitation, as shown in figure 2.2. The primary side MOSFETs Q_1 and Q_2 are operated in a sequence during the period to have $\frac{V_d}{2}$ voltage across the primary side of the isolated transformer. The diodes D_1 and D_2 rectify the secondary transformer voltage to a required V_O. To increase the overall operating efficiency, synchronous rectification is considered.

2.3.1 Basic topology overview

The operation of a half-bridge DC/DC converter can be explained in four different time intervals.

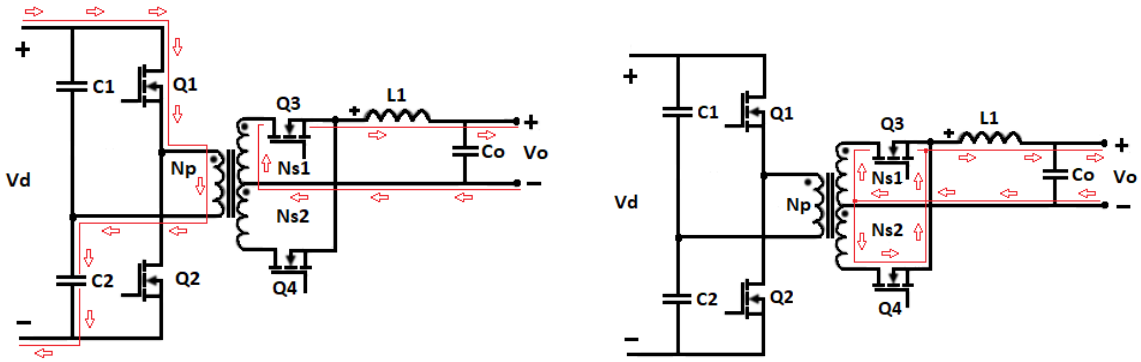

Figure 2.3: a) Time interval $[0 < t < D{\cdot}T_S]$ and b) Time interval $[D{\cdot}T_S < t < \frac{T_S}{2}]$.

During the time interval $[0 < \mathrm{t} < \mathrm{D}{\cdot}\mathrm{T}_S]$

In this time interval, the positive voltage V_d is applied across MOSFET Q_1, which starts conducting. This results in $\frac{V_d}{2}$ voltage across primary side of an isolated transformer as shown in figure 2.3a. On the secondary side of the transformer, the MOSFET Q_3 is forward biased and starts conducting. The output current flows through the inductor L_1 to deliver the required V_O.

During the time interval $[\mathrm{D}{\cdot}\mathrm{T}_S < \mathrm{t} < \frac{T_S}{2}]$

In this period, the MOSFETs Q_1 and Q_2 are switched off. Thus, there is no input voltage across the primary side of the isolated transformer. On the secondary side of the transformer, L_1 and C_O release the stored energy, thereby providing a constant V_O. During this interval, MOSFETs Q_3 and Q_4 are conducting, which result in the freewheeling stage, as shown in figure 2.3b.

During the time interval $[\frac{T_S}{2} < \mathrm{t} < \mathrm{D}{\cdot}\mathrm{T}_S + \frac{T_S}{2}]$

Similarly, the negative voltage V_d is applied across MOSFET Q_2, which starts conducting. This results in $\frac{-V_d}{2}$ voltage across the primary side of the isolated transformer as shown in figure 2.4a. On the secondary side of the transformer, the

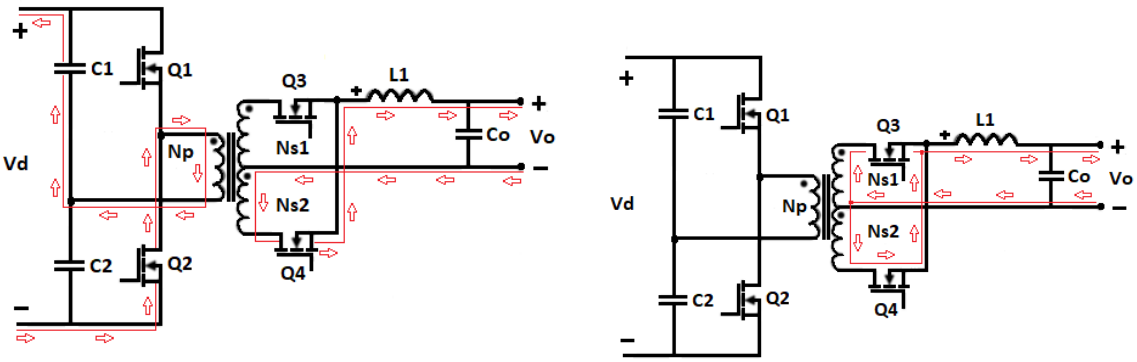

Figure 2.4: a) Time interval $[\frac{T_S}{2} < t < D \cdot T_S + \frac{T_S}{2}]$ and b) Time interval $[D \cdot T_S + \frac{T_S}{2} < t < T_S]$

MOSFET Q_4 is forward biased and starts conducting. The output current flows through the inductor L_1 to deliver the required V_O.

During the time interval $[\mathrm{D{\cdot}T}_S + \frac{T_S}{2} < \mathrm{t} < T_S]$

Similar to the interval $[D \cdot T_S < t < \frac{T_S}{2}]$, the MOSFETs Q_1 and Q_2 are switched off. There is no input voltage across the primary side of the isolated transformer. On the secondary side of the transformer, L_1 and C_O release the stored energy, thereby providing a constant V_O. During this interval, both MOSFETs Q_3 and Q_4 are conducting, resulting in the freewheeling stage again, as shown in figure 2.4b.

Figure 2.5 and 2.6 show the waveforms of a half-bridge DC/DC converter. The circuit is assumed to be operating in a steady-state condition. During the interval $[0 < t < D \cdot T_S]$, the voltage across the primary isolated transformer is given by,

$$V_{Pri} = \frac{V_d}{2} \tag{2.2}$$

Applying Kirchhoff's voltage law across the secondary side of the transformer, we get,

$$V_{Sec} - V_{Lx} - V_O = 0 \tag{2.3}$$

where V_{Sec} is the voltage across the secondary side of the transformer and V_{Lx} is the voltage across the inductor. Rearranging (2.3), the equation for V_{Lx} is given by,

$$V_{Lx} = V_{Sec} - V_O \tag{2.4}$$

Generally, the purpose of the transformers is to step up or step down the voltage by varying the turns ratio. Therefore, the transformer turns ratio is defined as,

$$\frac{V_{Pri}}{V_{Sec}} = \frac{N_P}{N_S} = \frac{I_{Sec}}{I_{Pri}} \tag{2.5}$$

where I_{Pri} and I_{Sec} are the primary and the secondary transformer currents. From (2.4) and (2.5), V_{Lx} is calculated by,

$$V_{Lx} = \frac{N_S}{N_P} \cdot \frac{V_d}{2} - V_O. \tag{2.6}$$

During the interval $[D \cdot T_S < t < \frac{T_S}{2}]$, there is no input voltage across the primary side of the transformer.

$$V_{Pri} = 0 \tag{2.7}$$

Again, applying Kirchhoff's voltage law across the secondary side of transformer

$$-V_{Lx} - V_O = 0 \tag{2.8}$$

Rearranging (2.8), V_{Lx} is defined for the respective time interval

$$V_{Lx} = -V_O. \tag{2.9}$$

From (2.6) and (2.9), during the interval $[0 < t < \frac{T_S}{2}]$, the average inductor voltage at steady state condition is zero.

$$V_L = \frac{1}{\frac{T_S}{2}} \cdot \int_0^{\frac{T_S}{2}} V_{Lx} \cdot dt = 0 \tag{2.10}$$

$$V_L = \frac{1}{\frac{T_S}{2}} \cdot \left[\int_0^{D \cdot T_S} V_{Lx} \cdot dt + \int_{D \cdot T_S}^{\frac{T_S}{2}} V_{Lx} \cdot dt \right] = 0 \tag{2.11}$$

$$V_L = \frac{1}{\frac{T_S}{2}} \cdot \left[\int_0^{D \cdot T_S} \left[\frac{N_S}{N_P} \cdot \frac{V_d}{2} - V_O \right] \cdot dt + \int_{D \cdot T_S}^{\frac{T_S}{2}} [-V_O] \cdot dt \right] = 0 \tag{2.12}$$

$$V_L = \frac{1}{\frac{T_S}{2}} \cdot \left[\left[\left[\frac{N_S}{N_P} \cdot \frac{V_d}{2} - V_O \right] \cdot D \cdot T_S \right] + \left[[-V_O] \cdot \left[\frac{T_S}{2} - D \cdot T_S \right] \right] \right] = 0 \tag{2.13}$$

$$V_L = \frac{\frac{T_S}{2}}{\frac{T_S}{2}} \cdot \left[\left[\left[\frac{N_S}{N_P} \cdot \frac{V_d}{2} - V_O \right] \cdot 2 \cdot D \right] - V_O \left[1 - 2 \cdot D \right] \right] = 0 \tag{2.14}$$

$$V_L = \left[\frac{N_S}{N_P} \cdot \frac{V_d}{2} \cdot 2 \cdot D \right] + [-V_O \cdot 2 \cdot D] - V_O + [2 \cdot V_O \cdot D] = 0 \tag{2.15}$$

Rearranging (2.15), the ratio of output voltage over input voltage for the interval $[0 < D \cdot T_S < \frac{T_S}{2}]$ is given by,

$$\frac{V_O}{V_d} = \frac{N_S}{N_P} \cdot D \tag{2.16}$$

Similarly, for the interval $[\frac{T_S}{2} < t < T_S]$, $\frac{-V_d}{2}$ voltage is applied across the primary side of the isolated transformer. Thus, due to the symmetry operation, the ratio of output voltage over input voltage for the interval remains the same.

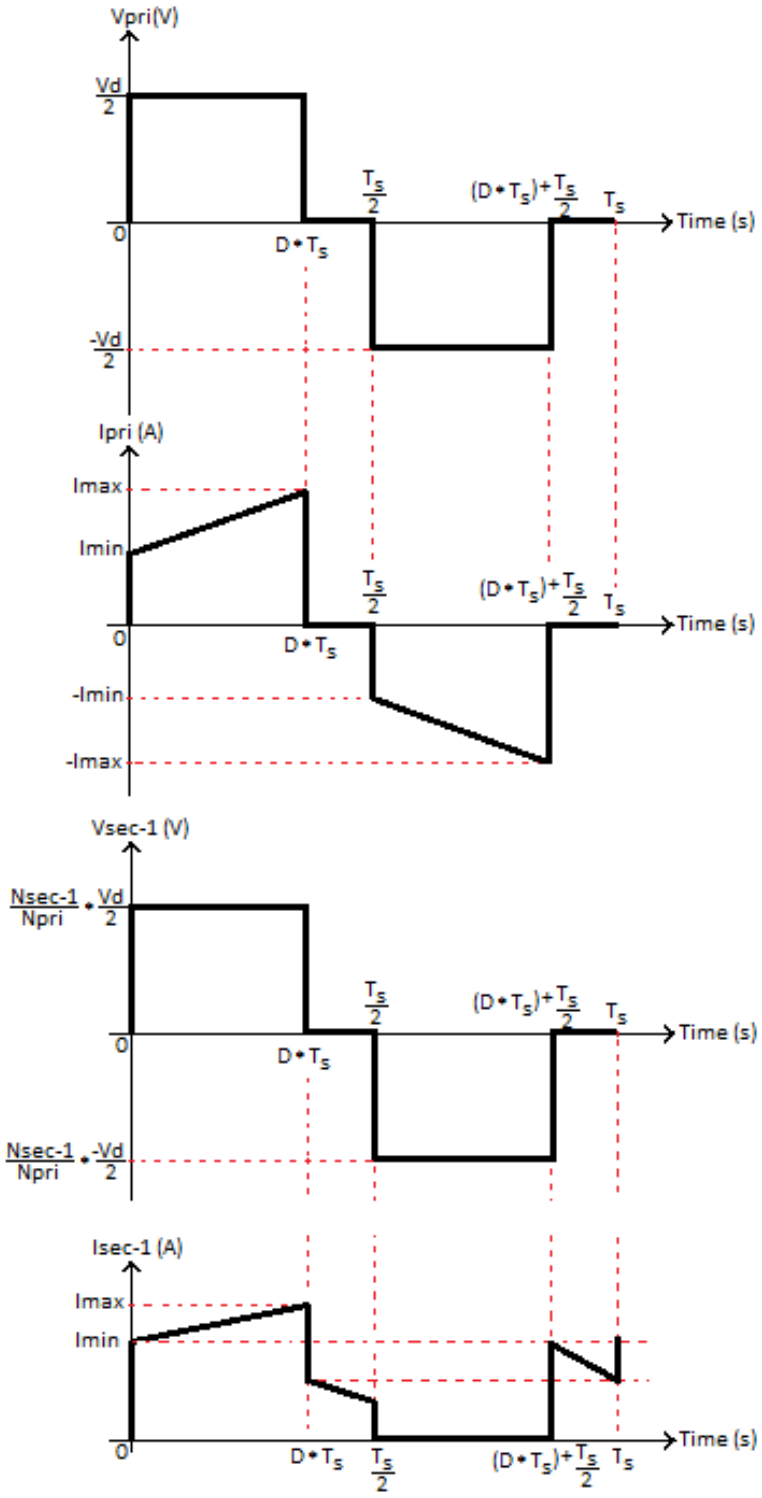

Figure 2.5: Half-bridge DC/DC converter waveforms. (a) Primary transformer voltage; (b) Primary transformer current; (c) Secondary - 1 transformer voltage; (d) Secondary - 1 transformer current.

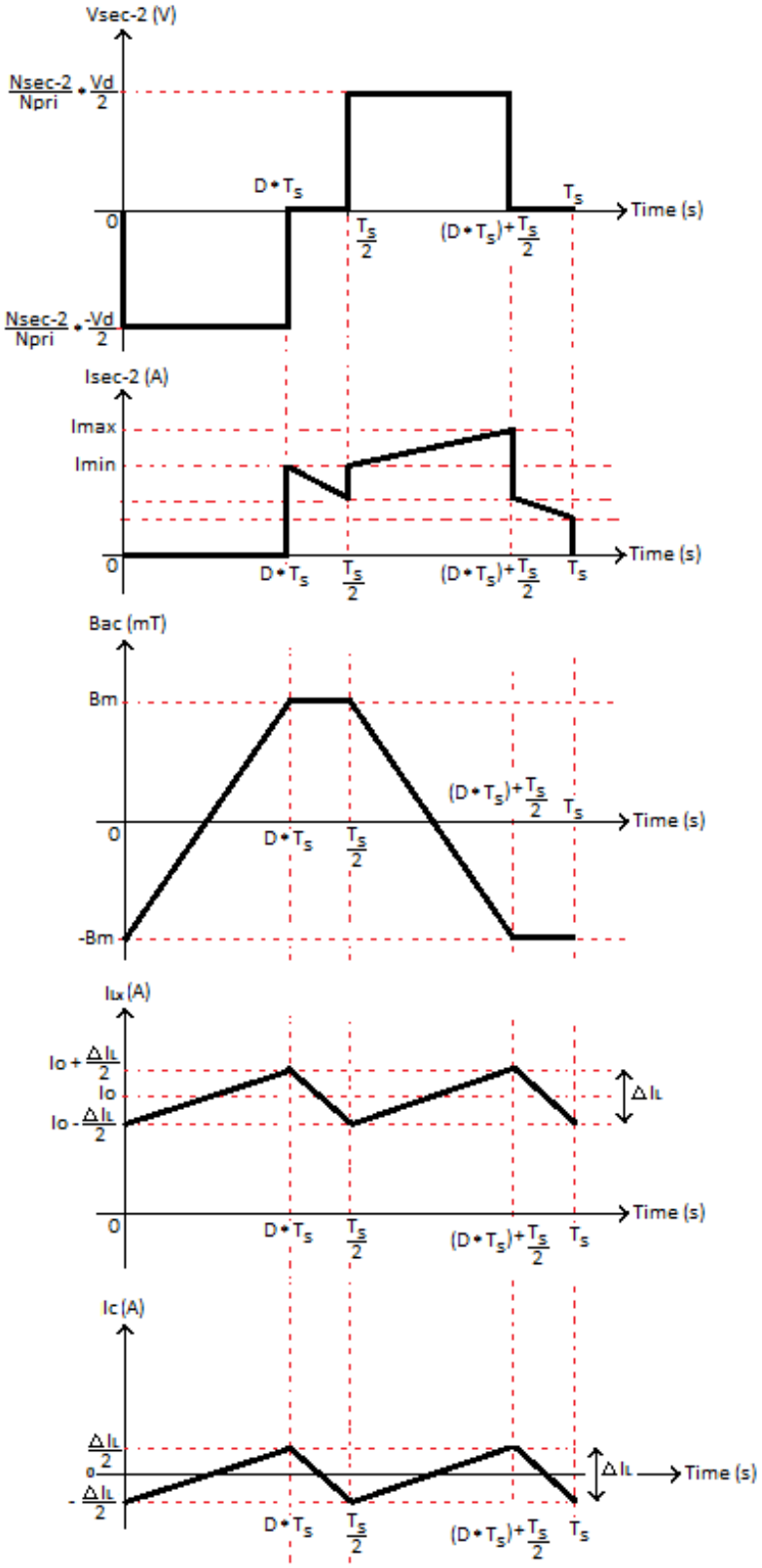

Figure 2.6: Half-bridge DC/DC converter waveforms. (a) Secondary - 2 transformer voltage; (b) Secondary - 2 transformer current; (c) Magnetic flux density of transformer; (d) Inductor current; (e) Capacitor current.

2.3.2 Circuit components

The half-bridge DC/DC converter consists of an isolated planar transformer with bidirectional core excitation. V_O is regulated by the voltage controller (LM5036) operating on the primary side of an isolated converter. The primary GaN MOSFETs are operated through the specifically designed (LMG1210) GaN driver from Texas instrument, which has a very low propagation delay and an adjustable dead time. Similarly, the synchronous GaN MOSFETs are operated through an isolated gate driver (2EDF7275K) from Infineon technologies AG. The other essential components as shown in figure 2.2 are explained in section 2.3.

2.4 Magnetic component design

In this section, the design of a high-frequency transformer and the output inductor for an isolated DC/DC converter are discussed.

2.4.1 Transformer design for isolated DC/DC converter

Traditionally, the high-frequency transformers are designed considering the maximum operating flux density B_{AC}, which depends on their core shapes and the core materials used. According to Faraday's law of electromagnetic induction, the electromotive force V is induced due to the rate of change of magnetic flux ϕ with respective to time t,

$$V = -N \cdot \frac{d\phi}{dt} \tag{2.17}$$

where N is the number of turns in the coil. But, the magnetic flux ϕ depends on the density of magnetic flux B_{AC} flowing through the core cross-section area A_e.

$$\phi = B_{AC} \cdot A_e \tag{2.18}$$

Thus, substituting (2.18) in (2.17), V can be expressed as,

$$V = -N \cdot A_e \cdot \frac{dB_{AC}}{dt} \tag{2.19}$$

Here, the isolated half-bridge DC/DC converter topology operating under CCM condition is considered. During the interval $[0 < t < D \cdot T_S]$, the primary MOSFET starts to conduct $\frac{V_{in}}{2}$ voltage across the primary winding of the transformer. Ideally, the flux transmission is considered to be linear in nature and lossless. The transformer ratios are expressed as,

$$\frac{V_{Pri}}{V_{Sec}} = \frac{N_P}{N_S} = \frac{I_{Sec}}{I_{Pri}} \tag{2.20}$$

Substituting (2.20) in (2.19), the induced voltage is expressed as,

$$\frac{V_{in}}{2} = N_P \cdot A_e \cdot \frac{\Delta B_{AC}}{\Delta t} \tag{2.21}$$

Rearranging the above (2.21),

$$D \cdot V_{in} = 4N_P A_e B_m f_{sw} \tag{2.22}$$

From the above (2.22), the magnetic flux density B_{AC} depends on the number of primary transformer turns N_P and the core cross-section area A_e. With a decrease in A_e, the core flux density B_{AC} increases, which gradually increases the core loss of the transformer. Also, an increase of N_P results in a decrease of B_{AC}, thus increasing the resistive losses. It's always a tradeoff between the core and the copper losses in the design of a transformer.

Traditionally, the design of the conventional copper-wound transformer depends on the available window area A_W for the specified core size. However, the complete window area is not available for the transformer winding. It mainly depends on the factor called window factor k_W. Normally, k_W of $0.4 \approx 0.7$ is available for the transformers, and it can go as low as 0.2 if there are multiple secondaries. Therefore, the product of A_W and k_W should be higher than the primary and secondary copper winding,

$$k_W \cdot A_W > N_P \cdot a_{WP} + N_{S_1} \cdot a_{WS_1} + N_{S_2} \cdot a_{WS_2} \tag{2.23}$$

where a_{WP}, a_{WS_1} and a_{WS_2} are the wire area cross-section of primary and secondaries of the transformer.

The voltage withstand capability of the winding depends on the core cross-sectional area A_e of the transformer. Similarly, the current-carrying capability through the winding depends on the thickness of the winding and the available window area A_W. Thus, the wire area cross-section of primary and secondaries are calculated by assuming the initial value of current density J and referring the standard wire gauge size (SWG),

$$\frac{I_{rms}}{J} = a_W \tag{2.24}$$

where I_{rms} is the RMS value of the current and a_W is the wire area cross-section. Generally, the peak current I_m is the product of I_{rms} and the form factor K_f.

$$I_m = I_{rms} \cdot K_f \tag{2.25}$$

Substituting (2.25) in (2.24), the wire area cross-section of primary a_{WP} is given by,

$$a_{WP} = \frac{I_{m_{Pri}}}{K_f \cdot J} \tag{2.26}$$

Similarly, substituting (2.26) in (2.23), this results in the equation for the window area in terms of the peak current and form factor for the primary and secondary side of the transformer.

$$k_W \cdot A_W > N_P \cdot \frac{I_{m_{Pri}}}{K_f \cdot J} + N_{S_1} \cdot \frac{I_{m_{Sec-1}}}{K_f \cdot J} + N_{S_2} \cdot \frac{I_{m_{Sec-2}}}{K_f \cdot J} \tag{2.27}$$

The product area A_P is the product of the core cross-sectional area A_e and the available window area A_W. This A_P gives the performance figure for the core selection.

$$A_P = A_e \cdot A_W \tag{2.28}$$

This thesis mainly focuses on the complete design of the planar transformer with the aid of performance figure for core selection.

2.4.1.1 Planar transformer

The design of a planar transformer plays a vital importance in high-frequency applications. It is a stacked multilayer PCB that can also be integrated into a multilayered power board [9]. These planar transformers exhibit a low profile depending on the requirements and also has excellent thermal characteristics with a very low leakage inductance [10]. In comparison with the conventional copper wound transformers, these transformers show nearly 50% to 60% lower heat resistance for the same core size [9]. This results in higher efficiency for the same core size in the planar transformer. Depending on the application and the frequency used, the selection of the core size and the core material is of high priority for designing of these planar transformers. Figure 2.8 shows the ER18 core planar transformer used in this thesis and arrangements for the mounting of the transformer on a PCB.

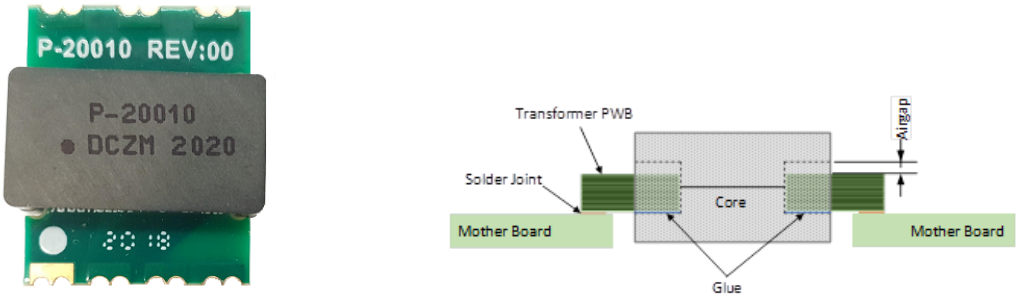

Figure 2.7: a) ER18 - Planar transformer and b) Mounting of planar transformer.

2.4.1.2 Core material selection

The high-frequency applications use softcore materials that provide a low withstand capability to an external magnetic field and hysteresis [12]. There are various core materials used depending on the application, namely, the level of core saturation, and temperature. The temperature plays a vital role in the core selection, operating beyond a specified temperature, the core tends to loose its magnetisation. The specific temperature is known as Curie temperature T_C. Some promising core materials are ferrites, iron powder, and soft iron. The advantage of using ferrite cores is that it provides high permeability with low operation losses when compared with the other core materials. The thesis mainly focuses on the planar transformer with a ferrite core material.

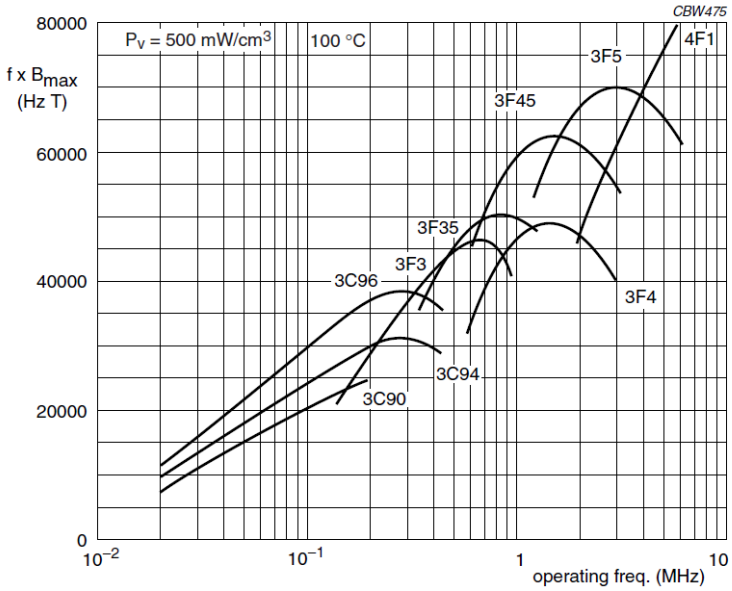

Figure 2.8: Performance curve of ferrite core materials at power loss density of 500 $\frac{\text{mW}}{\text{cm}^3}$ [11].

Figure 2.8 shows the performance curve of the ferrite core materials. The performance curve is a measurement of the power that can be handled by a ferrite core material at a predefined power loss density [11]. From figure 2.8, it is appropriate to choose a better core material for a high-frequency application. The ferrite core materials such as 3F3, 3F4, 3F35, and 3F36 are suitable core materials for operating at 600 kHz.

2.4.1.3 Magnetic core shapes

There are various core shapes suitable for different applications and their operating characteristics. For high-frequency applications, the planar magnetics with a low profile core provides low window height and high nominal inductance [13]. The magnetic core that includes simple bobbin winding such as ETD, EFD, EER and pot cores are not considered since the thesis focuses on a planar transformer with an integrated PCB. The planar E-I core provides flexible construction of window height, which yields a high volume density [14]. The planar ER core is a combination of E and pot core, which reduces the resistance across the winding and enhances the window area utilization [14]. When compared with an E-I core, the planar ER core provides improved thermal performance and provide higher efficiency. The thesis concentrates on the planar transformer with the ER core.

2.4.2 Output inductor

The output inductor L_x acts as an energy storage element during the operation of the half-bridge DC/DC converter, as explained in subsection 2.3.1. Assuming that the circuit is operating in a steady-state condition, the voltage across the inductor

is calculated by,

$$V_{Lx} = L_x \cdot \frac{di_{Lx}}{dt} \tag{2.29}$$

The small change in the inductor current Δi_L with respect to time Δt is given by,

$$V_{Lx} = L_x \cdot \frac{\Delta i_L}{\Delta t} \tag{2.30}$$

From the half-bridge DC/DC operation, change in the inductor current is approximately equal to 20% to 30% of output current I_O, which is given by,

$$\Delta i_L \approx 0.2 - 0.3 \cdot I_O \tag{2.31}$$

$$\Delta i_L = 30\% \cdot I_O = 0.3 \cdot 27.8\,\text{A} = 8.3\,\text{A} \tag{2.32}$$

By rearranging (2.6) and (2.30), the output inductor can be calculated by,

$$L_x \cdot \frac{\Delta i_L}{\Delta t} = \frac{N_S}{N_P} \cdot \frac{V_d}{2} - V_O \tag{2.33}$$

$$L_x = \frac{\left[\frac{N_S}{N_P} \cdot \frac{V_d}{2} - V_O\right] \cdot \Delta t}{\Delta i_L} \tag{2.34}$$

$$L_x = \frac{\left[\frac{N_S}{N_P} \cdot \frac{V_{d-max}}{2} - V_O\right] \cdot D_{min} \cdot \frac{T_S}{2}}{\Delta i_L} \tag{2.35}$$

2.5 Input capacitor

In a half-bridge DC/DC converter, the input bulk capacitor C_{in} is used to reduce the fluctuation of the source voltage and limit the inrush current. The energy stored in the capacitor provides sufficient holdup time that can regulate the output voltage during small interruption of the input supply [8]. Around 50% to 60% of nominal voltage V_{d-nom} is considered for V_{d-min}. η is the overall efficiency of the input supply [8]. The input bulk capacitance C_{in} is calculated by,

$$C_{in} = \frac{2 \cdot P_{out-rated} \cdot t_{hold-up}}{\left[V_{d-nom}^2 - V_{d-min}^2\right] \cdot \eta} \tag{2.36}$$

where $P_{out-rated}$ is the rated output power of the DC/DC converter.

2.6 Output capacitor

The output capacitors are used to reduce the output voltage ripple and withstand the transients that occur due to a change in the step load. The equivalent series resistance (ESR) of the output capacitor plays a vital role in the operation of the DC/DC converter. The value of ESR impacts the load transient and the output voltage ripple during the high-frequency operation. Hence it is recommended to have a low ESR value [8]. Thus, changes due to the load transients are given by,

$$\Delta V_O = -ESR \cdot \Delta I_O \tag{2.37}$$

2.7 Snubber circuit

Usually, the electrical stresses across the PES during the DC/DC converter operation would yield higher losses or even the possibility of breakdown. The snubbers are used in the DC/DC converter operation to reduce the stress and provide a safe operating area for a PES. Typically, RC snubbers are used in a DC/DC converter, where energy stored in the snubber capacitor is transferred through the snubber resistor [16]. It creates power dissipation across the snubber resistor in the form of heat. Depending on the power consumption, and design simplicity, the snubbers are classified as active and passive snubbers. The thesis mainly focuses on the implementation of a passive snubber, which is simple in its design. The snubber resistor R_{snub} is calculated by,

$$R_{snub} = \sqrt{\frac{L_o}{C_o}} \tag{2.38}$$

where L_o and C_o are the parasitic inductance and capacitance of the circuit. Similarly, the snubber capacitor C_{snub} is calculated by,

$$C_{snub} = a \cdot C_o \tag{2.39}$$

where a is the design factor depending on the operation of the circuit.

2.8 Control circuit

In this section, the control circuit of an isolated half-bridge DC/DC converter is discussed.

2.8.1 Closed loop - voltage control circuit

In this thesis, the output voltage V_O of an isolated half-bridge DC/DC converter is regulated using an analog feedback controller LM5036. As shown in figure 2.9, the output voltage V_O is sensed and amplified to a required level. The sensed output voltage is compared with the reference voltage to generate the amplified error voltage signal on the secondary of an isolated half-bridge DC/DC converter. The amplified error voltage signal is transmitted to the voltage controller across optocoupler isolation [17]. The internal PWM compares the error voltage signal with the reference ramp signal to generate adjustable duty ratios for the MOSFET operation. The MOSFETs are operated with adjusted duty cycle and dead time from the gate driver to achieve the required output voltage.

Traditionally, the closed-loop control provides a constant output voltage. The compensator provides the desired output by having a feedforward gain. The modelling of the system involves dynamic states modelling, linearize and simplification of the system, and finally obtaining the transfer function.

The dynamic states modelling is governed by basic circuit operation and its assumed that the circuit is operating in a steady-state condition. During the interval [0 <

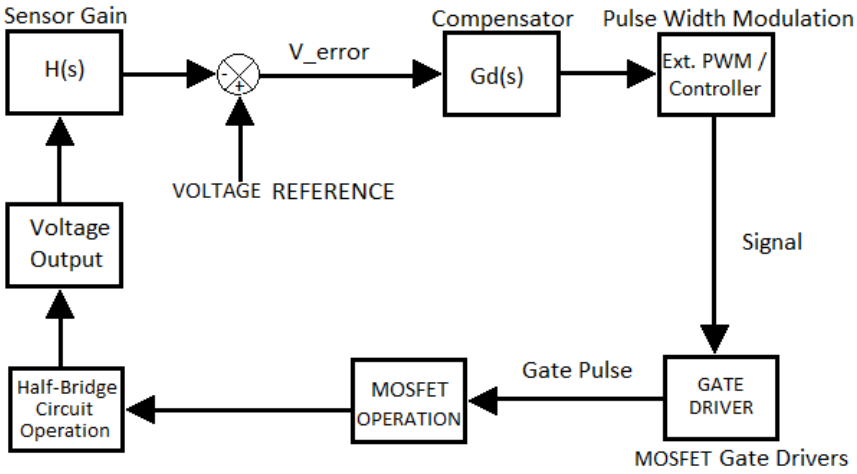

Figure 2.9: General layout of closed loop control system.

$t < \frac{T_s}{2}]$, average voltage across the inductor at steady-state condition is zero. From (2.12), the inductor voltage is calculated by,

$$L_x \cdot \frac{di_{Lx}}{dt} = \frac{N_S}{N_P} \cdot D \cdot \frac{V_d}{2} - V_O \tag{2.40}$$

$$\frac{di_{Lx}}{dt} = \frac{1}{Lx} \cdot \left[\frac{N_S}{N_P} \cdot D \cdot \frac{V_d}{2}\right] - \frac{1}{Lx}\left[V_O\right] \tag{2.41}$$

Similarly, the capacitor voltage for the interval $[0 < t < \frac{T_s}{2}]$ is determined by

$$\frac{dv_c}{dt} = \frac{1}{C} \cdot i_{Lx} - \frac{1}{RC} \cdot V_O \tag{2.42}$$

Thus, (2.41) and (2.42) gives the state space equation for a half-bridge DC/DC converter. The above equations are linearized by the state variables. The states of the system are represented as x_1 and x_2, duty ratio D as input u and output voltage V_O as y. Rewriting (2.41) and (2.42) gives,

$$\frac{dx_1}{dt} = \frac{1}{Lx} \cdot \left[\frac{N_S}{N_P} \cdot u \cdot \frac{V_d}{2}\right] - \frac{1}{Lx}\left[x_2\right] \tag{2.43}$$

$$\frac{dx_2}{dt} = \frac{1}{C} \cdot x_1 - \frac{1}{RC} \cdot x_2 \tag{2.44}$$

The system is said to be linearized if the system satisfies homogeneity and superposition. From (2.43) and (2.44), the state equations are simplified and linearized. Finally, by rearranging a linearized system the transfer function is obtained. Applying Laplace transforms for (2.43) and (2.44) we get,

$$S \cdot x(s) = \frac{1}{Lx} \cdot \left[\frac{N_S}{N_P} \cdot u(s) \cdot \frac{V_d}{2}\right] - \frac{1}{Lx}\left[y(s)\right] \tag{2.45}$$

$$S \cdot y(s) = \frac{1}{C} \cdot x(s) - \frac{1}{RC} \cdot y(s) \tag{2.46}$$

Rearranging (2.46) for linear state equation x(s), we get,

$$x(s) = C \cdot y(s) \left[S + \frac{1}{RC} \right] \tag{2.47}$$

Substituting (2.47) in (2.45),

$$S \left[C \cdot y(s) \left[S + \frac{1}{RC} \right] \right] = \frac{1}{Lx} \cdot \left[\frac{N_S}{N_P} \cdot u(s) \cdot \frac{V_d}{2} \right] - \frac{1}{Lx} \left[y(s) \right] \tag{2.48}$$

$$C \cdot S^2 \cdot y(s) + \left[S \cdot \frac{1}{RC} \right] \cdot y(s) + \left[\frac{1}{Lx} \right] \cdot y(s) = \frac{1}{Lx} \cdot \left[\frac{N_S}{N_P} \cdot u(s) \cdot \frac{V_d}{2} \right] \tag{2.49}$$

$$y(s) \left[S^2 + \frac{1}{RC} \cdot S + \frac{1}{Lx} \right] = \left[\frac{1}{Lx} \cdot \frac{N_S}{N_P} \cdot \frac{V_d}{2} \right] u(s) \tag{2.50}$$

$$\frac{y(s)}{u(s)} = \frac{\frac{1}{Lx} \cdot \frac{N_S}{N_P} \cdot \frac{V_d}{2}}{C \left[S^2 + \frac{1}{RC} \cdot S + \frac{1}{Lx} \right]} \tag{2.51}$$

Equation (2.51) shows the transfer function for the dynamic half-bridge DC/DC converter system under ideal condition.

2.8.2 Control circuit selection

In this thesis, the analog voltage controller LM5036 from Texas Instruments operating on the primary side of an isolated half-bridge DC/DC converter is considered. The LM5036 controller consists of 28 pins having quad flat no leads package (WQFN), as shown in figure 2.10. To reduce the output voltage ripple, the controller LM5036 has a regulated pre-bias start-up [17]. It has an integrated gate driver for the primary MOSFETs with minimum gate to source voltage V_{GS} of 9.5 V but, the GaN MOSFETs have a threshold V_{GS} of 5 V. Thus, a dedicated external primary gate driver LMG1210 is used. In the view of enhancing the efficiency and reliability, the controller LM5036 is adopted with current limitation in each cycle, which avoids saturation of the planar transformer and enhance the optimized use of the duty cycle [17].

From figure 2.10, the resistor RD_1 and RD_2 are used for adjusting deadtime for the synchronous MOSFETs. The input pin V_{in} can handle up to 100 V and the input transients can be reduced by introducing a low pass filter [17]. Using the relevant resistor, the RT pin is set to a required oscillator frequency f_{osci} given by,

$$R_T = \frac{1}{f_{osci} \cdot 1 \cdot 10^{-10}} \tag{2.52}$$

To start the half-bridge converter with a symmetric auxiliary supply, the under-voltage lockout (UVLO) of the controller LM5036 should be more than V_{UVLO} of 34 V. The over-voltage protection (OVP) for the converter is configured in the ON/OFF pin, where the converter gets shut down if the input voltage V_{in} exceeds 72 V. The optocoupler is biased using a 5 V regulated voltage from the reference (REF) pin. The RAMP pin in the controller generates signal modulation for the

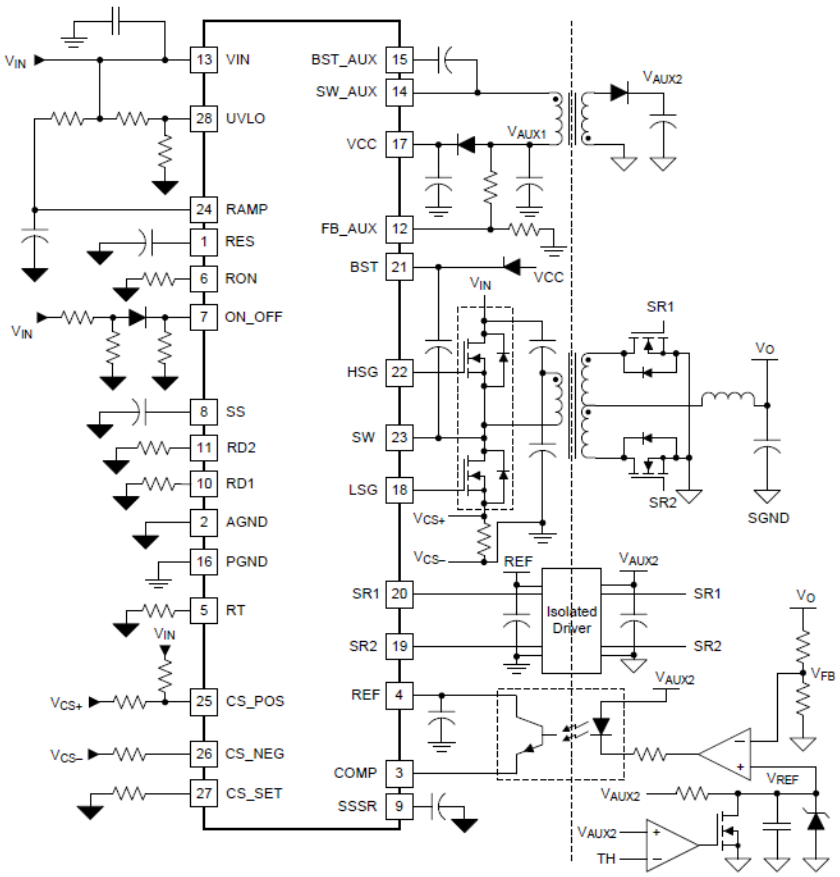

Figure 2.10: Controller LM5036 from Texas Instruments [17].

internal PWM. The COMP pin receives the amplified error signal and the resulting V_{comp} is compared with the soft starter capacitor voltage V_{SS}. The smaller signal of these is passed through an offset and followed by the voltage divider before comparing it with the RAMP signal. Further, the PWM compares the above small signal with the modulated ramp signal to have adjustable duty ratios [17].

2.9 High frequency gate drivers

In this section, the design consideration of the high-frequency gate driver and its selections are discussed.

2.9.1 Design consideration for gate drivers

It is important to consider design consideration for the gate driver since the GaN MOSFETs operate at high switching frequency in comparison with the Si MOSFETs. The false triggering of the gate due to high noise leads to failure of the GaN MOSFETs since it exhibits very low input capacitance and has a threshold V_{GS} of 5 V [18]. The gate needs to be protected from the Miller effect with the least gate impedance. The gate driver with single output topology requires a clamping diode

to control the Miller effect, as shown in figure 2.11. The selection of the individual gate resistors R_{G-on} and R_{G-off} improves the operation of GaN MOSFETs and performance of the gate driver stability.

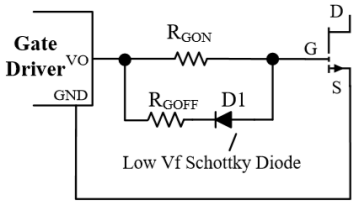

Figure 2.11: Design consideration of high-frequency gate driver [18].

The GaN MOSFETs have a small gate charge when compared to Si MOSFETs. The gate resistor R_{G-on} regulates the high voltage slew rates during turn-on [19]. The higher value of R_{G-on} reduces the operating f_{sw}, which increases the total losses. Alternatively, a lower R_{G-on} increases noise oscillations and increases switching losses [18]. The possible precautions are placing a higher frequency gate driver near to the MOSFET's gate, having a low inductance path, and a proper selection of R_{G-on} and R_{G-off} [18].

2.9.2 High frequency gate driver selection

The LMG1210 acts as an external primary high-frequency gate driver specialized for a half-bridge DC/DC converter operation. It consists of 19 pins with the least loop inductance WQFN package. The gate driver is controlled by considering an external PWM to generate deadtime or having an independent input pin, as shown in figure 2.12. In this independent input mode, the deadtime for the primary MOSFETs is generated from the controller LM5036, and the deadtime circuit in the gate driver is inoperative [20]. The RC filter and common mode choke in series with the controller input prevents the false triggering of the gate pulse. The low dropout regulator enhance the gate driver LMG1210 operation up to 18 V and it maintains an output voltage of 5 V [20]. The LMG1210 provides higher efficiency by having less reverse recovery loss across the diode. The driver is protected with over-temperature protection, where a temperature above 160 °C shuts down the high side while keeping the low side operating [20].

Similarly, the gate driver 2EDF7275K from Infineon Technologies is used for operating the isolated synchronous MOSFETs. It consists of 13 pins with a land grid array package (LGA), as shown in figure 2.13. The UVLO feature in the driver enhances the performance and reliability under different operating conditions [21]. The input supply of 5 V is applied to the input pin (VDDI) of the gate driver, and the switched low-dropout regulator (SLDO) pin is activated to regulate the input current. The input oscillations at the VDDI pin is damped by connecting an external resistor in series with the VDDI pin. The gate driver consists of a dual output channel, and each channel has to be powered independently [21]. In this thesis, the deadtime control pin (DTC) of the gate driver LMG1210 is inoperative since it is generated from

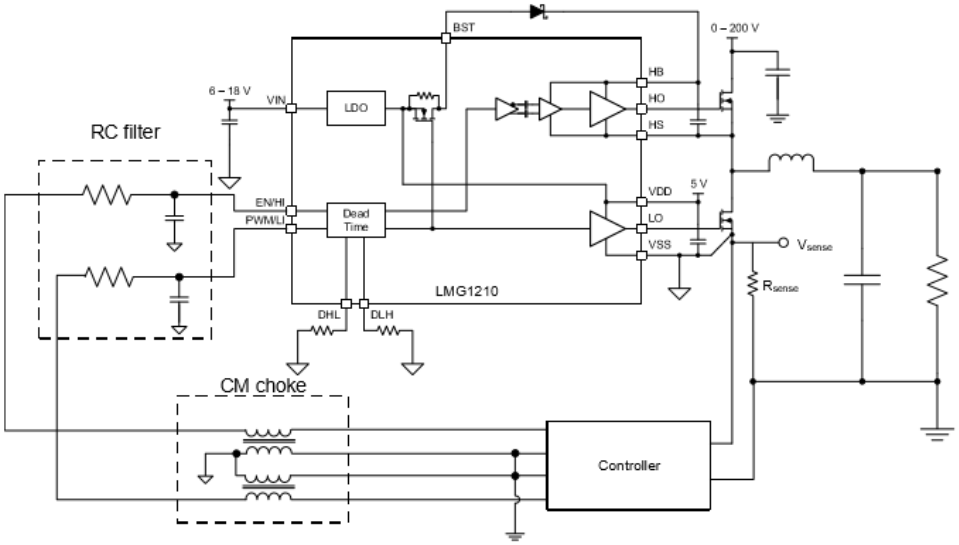

Figure 2.12: Gate driver LMG1210 from Texas Instruments [20].

the controller LM5036. The wide operating temperature and robustness provide a platform for different industry usage.

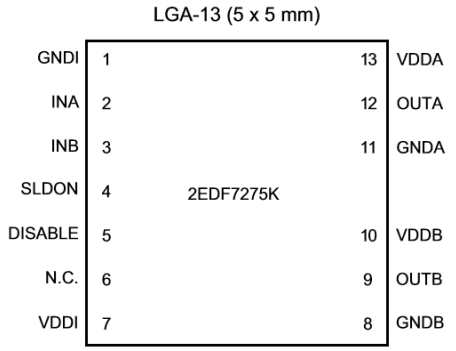

Figure 2.13: Gate driver 2EDF7275K from Infineon Technologies AG [21].

2.10 GaN MOSFET selection

The enhancement-mode GaN MOSFET operating during on and off states is as shown in figure 2.10. The GaN MOSFETs are chemically stable and robust due to the wurtzite crystal structure. This crystal structure in the GaN MOSFET creates electromechanical interaction resulting in a piezoelectric effect. This effect creates higher strain in the crystal structure which leads to a higher electric field compared to the Si MOSFET [23]. The strain is created by having a layer AlGaN on top of the crystal [23]. A lateral two-dimensional electron gas (2DEG) is induced due to the strain, which provides a channel in which the conduction of electrons takes place. The enhancement-mode GaN MOSFETs exhibits low R_{ds-on} and a total gate charge Q_G in comparison with the Si MOSFETs yielding less switching losses. Usually, the

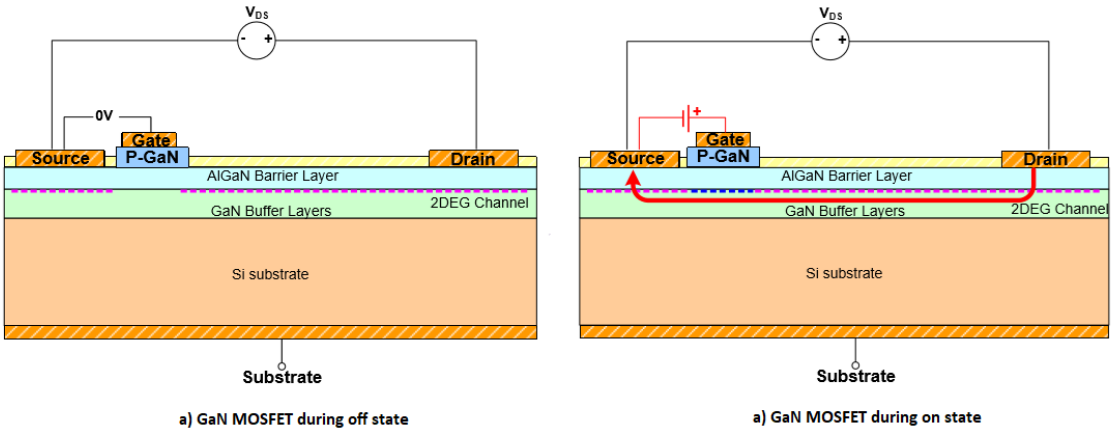

Figure 2.14: Enhancement mode GaN MOSFET during off and on states [22].

MOSFET's R_{ds-on} increases with its breakdown voltage . The cascode system of a high electron mobility GaN transistor (HEMT) in series with enhancement-mode Si MOSFET provides the least added R_{ds-on} with increasing the rated voltage. Figure 2.15 shows the effect of R_{ds-on} of an enhancement mode Si MOSFET to the cascode system. With an increase in rated voltage provides a least R_{ds-on} for the GaN MOSFETs. Additionally, the absence of a body diode in the GaN MOSFET results in zero reverse recovery loss and enhances the overall efficiency. Usually, MOSFETs with a body diode can experience a false turn-on due to internal parasitics. A high $\frac{dv}{dt}$ across the body diode during the reverse recovery leads to failure of the MOSFET [24]. The high reverse voltage drop during reverse recovery is a major hindrance in the GaN MOSFETs as channel resistance, and the threshold voltage adds to the reverse voltage drop [24]. In this thesis, GaN MOSFETs operating on the secondary side experiences larger currents during the conduction, which leads to a higher reverse voltage drop and reduction in the overall efficiency. It is recommended to have an anti-parallel diode across the GaN MOSFETs operating on the secondary side of the isolated half-bridge DC/DC converter to have better efficiency. The optimized dead time for the GaN MOSFETs enhances reliability and operation.

There are different manufacturers in the market with similar ratings for GaN MOSFETs. Some of the promising GaN MOSFETs from EPC are EPC2029, EPC2053, EPC2022, EPC2024, EPC2020, and EPC2032. These MOSFETs are differentiated and utilized depending on their voltage rating. Table 2.3 and 2.4 shows different MOSFETs from various manufacturers. The "GaN" MOSFET having the least R_{ds-on} reduces the conduction loss in comparison with similar MOSFETs. The "GaN" MOSFET having a similar gate charge that includes a steady-state charge Q_{SS} required to operate the gate. The "GaN" MOSFET with lower output charge Q_{OSS} provides short deadtime and improves high-frequency operation [25]. The temperature plays a vital role in the operation of GaN MOSFETs. A higher operating temperature reduces the mobility of electrons in the 2DEG channel and increases the R_{ds-on}. The GaN MOSFET doesn't exhibit an avalanche breakdown mechanism, which is quite common in Si and SiC MOSFETs.

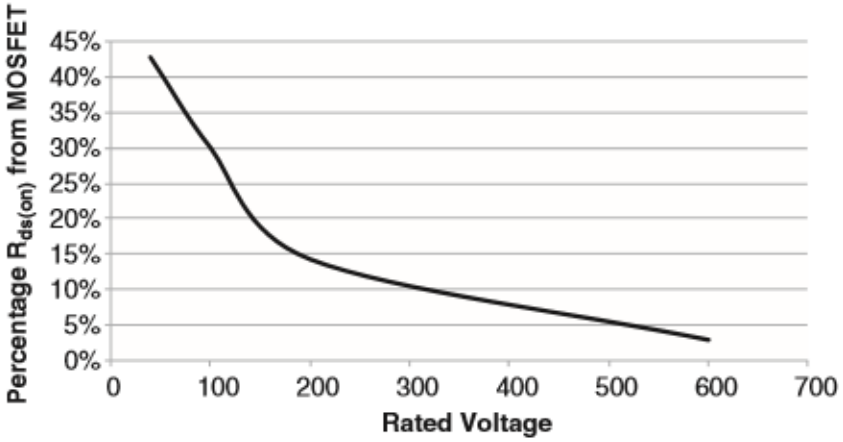

Figure 2.15: Graph depicts percentage of R_{ds-on} from MOSFET for respective rated voltage in cascode system [23].

Table 2.3: Primary side MOSFET specification with f_{sw} of 300 kHz for FET

Parameters	**EPC2029**	**EPC2053**	**GaN**	**EPC2022**	**GS61008P**
Drain to source voltage	80 V	100 V	100 V	100 V	100 V
Gate to source voltage	6 V	6 V	5 V	6 V	7 V
Maximum R_{ds-on}	3.2 mΩ	3.8 mΩ	3 mΩ	3.2 mΩ	7 mΩ
Total gate charge	13 nC	11.4 nC	14 nC	13.2 nC	8 nC
Gate to source charge	3.4 nC	4.1 nC	1.4 nC	3.4 nC	3.5 nC
Gate to drain charge	1.9 nC	1.5 nC	1 nC	2.4 nC	1.7 nC
Output charge	53 nC	45 nC	41 nC	71 nC	20 nC
Continuous drain current	48 A	48 A	76 A	90 A	90 A

Table 2.4: Secondary side MOSFET specification with f_{sw} of 300 kHz for FET

Parameters	**EPC2024**	**EPC2020**	**EPC2032**
Drain to source voltage	40 V	60 V	100 V
Gate to source voltage	6 V	6 V	6 V
Maximum on state resistance	1.5 mΩ	2.2 mΩ	4 mΩ
Total gate charge	18 nC	16 nC	12 nC
Gate to source charge	5.1 nC	3.9 nC	3 nC
Gate to drain charge	2.4 nC	2.3 nC	2 nC
Output charge	45 nC	50 nC	66 nC
Continuous drain current	90 A	90 A	48 A

The significant benefits of using GaN MOSFETs are their power efficiency and high switching frequency, which helps to reduce the overall size of the board compared to the Si counterparts. The superior physical property and fabrication process of the GaN material exhibits an overall reduction in the GaN MOSFET package size when compared with the Si MOSFET. Additionally, due to the less gate-source capacitance and drain-source capacitance, the rise time and fall time of the voltage

and current are quicker. As the switching of GaN MOSFETs is faster, it is of vital importance to minimize stray inductance in the PCB board. In the case of high stray inductance, the voltage peak will be higher, which will lead to an electrical breakdown of the MOSFET. In this thesis, "GaN" MOSFET is selected for both primary and secondary sides. On the secondary side, the cascode connection of MOSFETs with an anti-parallel diode is considered.

2.10.1 Reliability

The most vital factor that needs attention for using a MOSFET in any application is the reliability. Traditionally, all MOSFETs go through the following tests before they are introduced to industrial and domestic markets. The different tests include high-temperature reverse bias (HTRB), high-temperature gate bias (HTGB), humidity stressing (HT), and temperature cycling (TC). In the following subsections, the procedure of the tests performed is briefed. Likewise, even the GaN MOSFETs go through these testing. But are these tests valid for GaN MOSFETs? yes, because the GaN devices posses a similar physical structure to that of Si MOSFET.

2.10.1.1 High Temperature Reverse Bias Test

One of the most common reliability tests for power devices is the high-temperature reverse bias (HTRB) test. This test evaluates long-term stability under high drain-source bias, and it is intended to accelerate failure mechanisms that are activated through the use of biased operating conditions. During the HTRB test, the power device samples are stressed with 80% or maximum rated reverse breakdown voltage at an ambient temperature T_{j-max} typically 25 °C, for 1000 h [28].

2.10.1.2 High Temperature Gate Bias Test

This test majorly focuses on injecting the rated gate voltage under 150 °C for a prolonged period (about 1000 h). After the test, the power device needs to maintain the threshold voltage. The shift in the threshold should not be more than 25% of the rated threshold voltage for the power device to pass the testing [26].

2.10.1.3 Temperature Humidity Bias

The temperature humidity bias test (THB) is carried for a power device to check the die withstand capability and cracks on the die due to high humidity. These cracks occur because of the electrochemical migration and the aluminum corrosion [27]. In this THB test, the devices are exposed to 85% relative humidity (RH) and 85 °C for a period of 1000 h under maximum bias 80 V. EPC has investigated the impact of humidity on the GaN MOSFETs [28].

2.11 Power losses in the DC/DC Half-Bridge Converter

The factor that determines the overall efficiency of the system is the losses. These losses dissipate in the form of heat. In this subsection, different power losses in the half-bridge DC/DC converter are briefed.

2.11.1 GaN MOSFET losses

The primary contributors to the power losses in a switch-mode power supply are the power transistors. The prominent losses of a power MOSFET are conduction loss, switching loss, gate driver loss, and deadtime loss. In the low-frequency operation of the MOSFET, the conduction losses will be high, and in the high-frequency operation, the switching losses will be high. The conduction losses P_{COND} of the MOSFET depends on drain current I_d flowing through the R_{ds-on}. Thus, P_{COND} can be calculated by,

$$P_{COND} = I_d^2 R_{ds-on} D \tag{2.53}$$

The continuous turn-on and turn-off operation of the power MOSFET induce loss during each switching cycle. The switching loss P_{SW} develops electrical stress in the PES. The higher stress in MOSFET due to switching results in component failure. The P_{SW} for the MOSFET is calculated by considering rise time t_r and fall time t_f of the MOSFET for a specified switching frequency.

$$P_{SW} = \frac{V_{ds}}{2} I_d f_{sw} \frac{t_r + t_f}{2} \tag{2.54}$$

The gate of the MOSFET plays a vital role in turning on and turning off the MOSFET. These losses arise when trying to charge the MOSFET gate capacitor. The gate driver loss P_{Gate} is dependent on the gate-drain capacitor (C_{gd}) and the gate-source capacitor (C_{gs}) of the MOSFET. The MOSFET with low C_{gd} & C_{gs} is selected to minimize P_{Gate} and enhance the operating efficiency. P_{Gate} of the MOSFET can be found by,

$$P_{Gate} = V_{GS} Q_G f_{sw} \tag{2.55}$$

In ideal operation, the power switches turn on and turn off alternatively using a defined delay time known as the deadtime to avoid high current spikes in the system. The deadtime losses P_{DT} are a vital consideration in the operation of the DC/DC converters. P_{DT} includes the body diode conduction loss, diode reverse recovery loss, and output capacitance loss [29]. In GaN MOSFETs, the absence of a body diode eliminates the reverse recovery losses. But GaN MOSFETs have the provision of conducting reverse current through the 2DEG channel if the gate-drain voltage V_{GD} is higher than the threshold voltage V_{TH} [30]. Typically, this creates a higher voltage drop in comparison with the diode losses. Applying negative V_{GS-off} during turn-off of the GaN MOSFET would prevent false turn-on of the MOSFET [30]. Thus, the voltage drop V_{DT} due to deadtime is calculated by,

$$V_{DT} = V_{TH} + |V_{GS-off}| + V_{DS} \tag{2.56}$$

where V_{DS} is the voltage across drain to source. The P_{DT} for the half-bridge DC/DC converter is given by

$$P_{DT} = V_{DT} I_d f_{sw} (t_{dr} + t_{df}) \tag{2.57}$$

where t_{dr} and t_{df} are the rise time and fall time during deadtime interval.

Table 2.5 and 2.6 shows the calculated conduction and switching losses for different primary and secondary GaN MOSFETs for the input voltage of 48 V. The total power loss P_{loss} across the MOSFET is given by,

$$P_{Loss} = P_{COND} + P_{SW} + P_{Gate} + P_{DT} \tag{2.58}$$

Table 2.5: Rough estimation of primary side MOSFET losses comparison at input voltage of 48 V

Parameters	**EPC2029**	**EPC2053**	**GaN**	**EPC2022**	**GS61008P**
Conduction losses	0.3 W	0.4 W	0.3 W	0.3 W	1.5 W
Switching losses	1.7 W	1.2 W	1.3 W	1.5 W	1.1 W
Total power losses	2.1 W	1.6 W	1.6 W	1.8 W	2.5 W

Table 2.6: Rough estimation of secondary side MOSFET losses comparison at input voltage of 48 V

Parameters	**EPC2024**	**EPC2020**	**EPC2032**	**GaN**
Conduction losses	0.5 W	0.7 W	1.2 W	0.9 W
Switching losses	2.9 W	2.6 W	2.3 W	2.2 W
Total power losses	3.4 W	3.3 W	3.5 W	3.1 W

2.11.2 Passive RC snubber losses

As discussed in section 2.7, the design and implementation of snubbers enhances the overall performance of the converter by reducing electrical stress across the MOSFETs. The losses due to passive RC snubbers create a huge impact on the overall efficiency of the GaN MOSFET based half-bridge DC/DC converter. The snubber capacitor C_{snub} stores energy over a period, given by,

$$E_{snub} = \frac{1}{2} \cdot C_{snub} V^2 \tag{2.59}$$

where V is the voltage amplitude across the drain to source voltage V_{DS} of the "GaN" MOSFET. Thus, the power dissipated over a period across the drain to source voltage V_{DS} of the "GaN" MOSFET, given by,

$$P_{snub} = C_{snub} V^2 f \tag{2.60}$$

where f is the switching frequency of the "GaN" MOSFET.

2.11.3 Transformer losses

In this subsection, different transformer losses that influence the overall efficiency of the DC/DC converter are discussed.

2.11.3.1 Core loss

The high-frequency planar transformers dissipate energy in the magnetic core and windings. The transformer losses include iron loss, copper loss, stray loss, and dielectric loss. The alternative flux in the core causes core loss. The appropriate selection of the core shape and the core area determines the magnetic flux density B_m. B_m depends on the operating duty cycle D, the input voltage voltage V_d, number of primary turns N_P, selected core area A_e and the switching frequency f_{sw}.

$$B_m = \frac{D_{min} V_{d-max}}{4 N_P A_e f_{sw}} \tag{2.61}$$

$$B_m \propto \frac{1}{A_e} \tag{2.62}$$

From (2.62), the transformer with the least core area A_e exhibits the high magnetic flux density B_m. The planar transformer operating with an appropriate B_m reduces the temperature rise [10]. Thus, the core loss density P_V is calculated by

$$P_v = C_m \cdot f_{sw}^x \cdot B_m^y \cdot \left[(C_{t2} \cdot T^2) - (C_{t1} \cdot T) + C_t \right] \tag{2.63}$$

where C_m is the Steinmetz hysteresis coefficient, similarly x and y are numerical coefficients, C_{t2}, C_{t1} and C_t are the constants which are temperature (T) dependent. The product of core loss density P_V and core volume V_e gives the overall core loss of the planar transformer,

$$P_{CL} = P_v V_e \tag{2.64}$$

2.11.3.2 Winding losses

These transformer losses are variable according to the load requirements. The magnetic flux density B_m depends on the number of primary turns N_P. But having a constant core area, the magnetic flux density B_m can be varied by an integral multiple of the turns ratio. In this thesis, the turns ratio is 3:2 for the specified operating condition. The possible options would be 6:4 and 9:6. The higher turns ratio provides more voltage drop in the winding. It's always a tradeoff in selecting the number of winding turns and appropriate core areas for the transformer.

$$N_P \propto \frac{1}{B_m} \tag{2.65}$$

The winding loss P_{ac} of the planar transformer is calculated by squaring the RMS input current with respective ohmic resistance R_{ac} of the winding,

$$P_{ac} = I_{rms-ac}^2 \cdot R_{ac} \tag{2.66}$$

The proximity effect and skin effect are the important considerations that need attention during the design of the planar transformer. The induced circulating current due to a varying magnetic field induces excess power dissipation and redistribution of the current in the conductor [31]. During high-frequency excitation, the maximum current density is at the surface and decreases exponentially. Thus, skin effect due to surface current is given by,

$$\delta = \sqrt{\frac{2}{\omega \cdot \mu_o \cdot \sigma}} \tag{2.67}$$

where the permeability of free space μ_0 is $4\pi \cdot 10^{-7}$, ω is the operating frequency in radians, and σ is the conductivity of the winding material [31]. The Proximity effect is predominant when compared with the skin effect. In high-frequency applications, the currents are arranged non-uniformly in a specified area of the conductors resulting in an increase in resistance due to current crowding. Dowell's equation is used to calculate the power dissipation in each layer, and it is given by,

$$G_1(\Delta) = \Delta \frac{\sinh 2\Delta + \sin 2\Delta}{\cosh 2\Delta - \cos 2\Delta} \tag{2.68}$$

$$G_2(\Delta) = \Delta \frac{\sinh \Delta \cos \Delta + \cosh \Delta \sin \Delta}{\cosh 2\Delta - \cos 2\Delta} \tag{2.69}$$

where Δ is defined as the ratio of height of the winding layer h_i and skin depth δ for the specified frequency [31].

$$\Delta = \frac{h_i}{\delta} \tag{2.70}$$

Figure 2.16 shows the ratio of $\frac{R_{AC}}{R_{DC}}$ under a specified layer height and skin depth. The increase in the number of layers gradually increases the resistance at high frequencies. The interleaved winding in the transformer is recommended to have an even distribution of current between the intermediate layers. In the planar transformer, having higher copper thickness for the layer reduces the DC resistances. The possible solution to minimize AC resistance is to have a parallel winding connection. It's always a tradeoff in selecting the thickness of copper for the layer.

2.12 Design Concern

In this subsection, the design concerns for the GaN MOSFET and the planar transformers are discussed.

2.12.1 GaN MOSFET

Firstly, the power switches with an appropriate rating should be selected depending on the application they are used to. Generally, the switching of the GaN MOSFETs is fast, and hence the chances of excessive voltage surges due to the stray inductance are higher. This voltage surge can be decreased by lowering the $\frac{di}{dt}$ and the stray inductance [32]. Also, a capacitor connected parallel to the MOSFET can help in

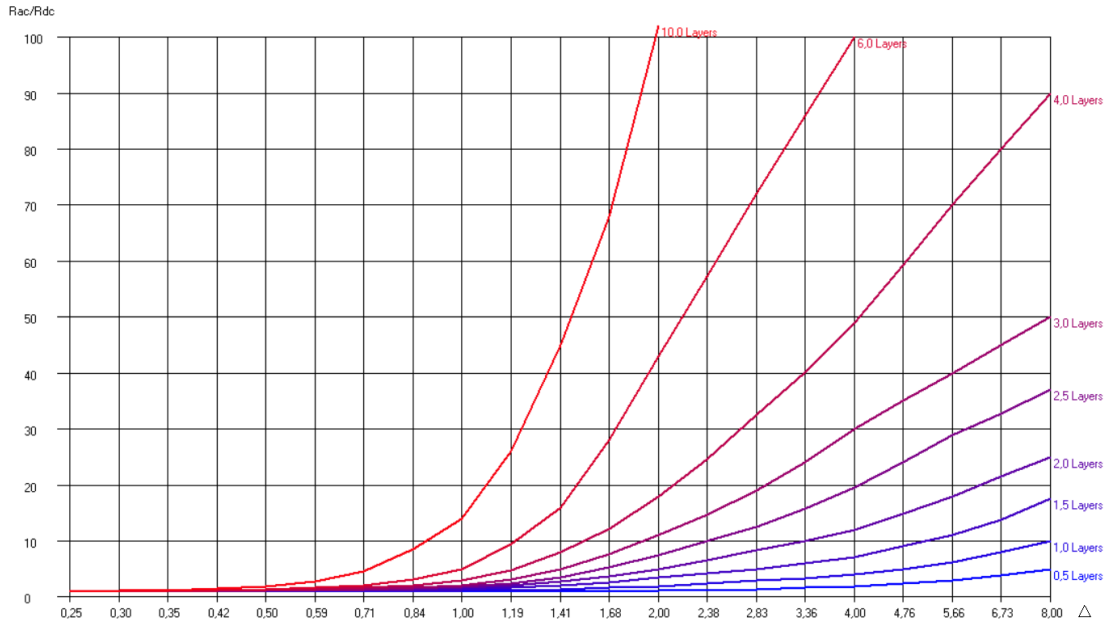

Figure 2.16: Simulated overall ratio of $\frac{R_{AC}}{R_{DC}}$ in each layer under specified layer height and skin depth.

reducing the stray inductance in the circuit and therefore helping in minimizing sudden surge of voltage to the MOSFETs.
A few recommended PCB design consideration for the use of GaN MOSFETs are,

- The placement of GaN MOSFETs on the primary side shall be close to the input capacitors to minimize the size of high frequency loop [33].
- It is recommended to place the GaN MOSFETs as close to the gate driver to reduce the inductance loop in PCB as possible.

2.12.2 Planar transformer

In the design of planar transformers, the windings are stacked horizontally, aiding less leakage inductance and strong coupling. Furthermore, an increase in the winding surface area leads to a proportional increase in interwinding capacitance. This interwinding capacitance provides a path for the EMI back to the source [34]. The higher transients due to the interwinding capacitance can lead to a failure of components. The factors influencing the interwinding capacitance are thicker insulation layer, a low dielectric constant for insulating material, and winding surface area [34].
The major design considerations for designing the planar transformers are,

- The symmetrical interleaved winding for planar transformer reduces the drastic increase in temperature rise and proximity effect.
- The effective utilization of window area or winding height leads to optimum design for the application.
- The selection of standard copper thickness considerably reduces the cost of manufacturing.
- Sufficient insulation thickness has to be maintained between the layers for safety reasons.

2.13 Design of feedback control loop

As discussed in subsection 2.8.1, the output voltage is regulated by adjusting the duty cycle from the controller's inbuilt gate drivers. In this thesis, the system stability is achieved by having the voltage mode control method. Generally, a type 3 compensation circuit is used in the DC/DC converters operating in CCM with voltage mode of control. Thus, utilizing type - 3 compensation provides an enhanced transient response in the operation of a GaN MOSFET based half-bridge DC/DC converter. The type 3 compensation provides a boost in phase margin at crossover frequency f_c. Figure 2.17 shows the simple type 3 compensation circuit used in this thesis.

Generally, the feedback control loops are expected to have faster transient responses. The faster transient responses are attained by having a higher crossover frequency. Practically, $(\frac{1}{10})^{th}$ of the operating switching frequency is selected as the crossover frequency.

The converter operating with different input voltages and load currents experiences an additional noise or the disturbance during the operation. These distortions tend to affect the overall stability of the system. The system stability plays a vital role in the operation of the GaN MOSFET based half-bridge DC/DC converter. Furthermore, the design of the compensation circuit aids the overall stability of the system.

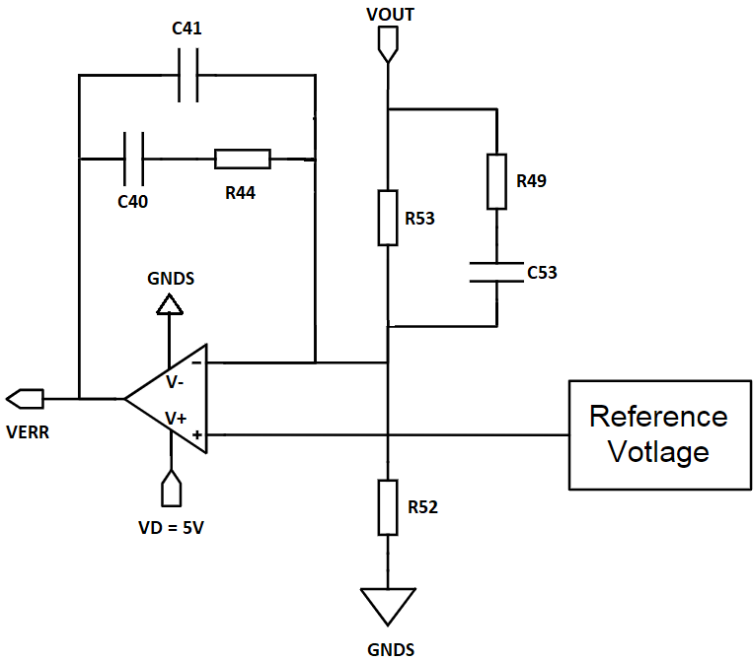

Figure 2.17: Simple type 3 compensation circuit used in DC/DC converter

A type 3 compensation consists of an integrator pole at the origin with two additional zero-pole pair [38]. In this thesis, the type 3 compensation circuit is designed using

the "K" factor method. The "K" factor is a simple mathematical technique that enhances the phase boost at the desired f_c [38]. As the factor "K" increases, the higher the phase boost. However, on the other hand, the gain penalty is associated with increasing the phase boost [38]. Hence, the optimum phase boost provides enhanced operation of the system. The factor "K" is calculated for designing the components for type 3 compensation. Initially, the phase boost provided by the two zero-pole pair is calculated by,

$$Boost = 2 \cdot \left[\tan^{-1}\sqrt{K} - \tan^{-1}(\frac{1}{\sqrt{K}})\right] \tag{2.71}$$

Furthermore, the phase boost can be calculated by,

$$Boost = PM - P_{GVD} - 90^{\circ} \tag{2.72}$$

where PM is the phase margin required, and P_{GVD} is the initial phase angle of the plant. From the trigonometry identity, we know that,

$$tan^{-1}(x) + tan^{-1}(\frac{1}{x}) = 90^{\circ} \tag{2.73}$$

Substituting (2.73) and (2.71), we get

$$Boost = 2 \cdot \left[\tan^{-1}\sqrt{K} + \tan^{-1}\sqrt{K} - 90^{\circ}\right] \tag{2.74}$$

Rearranging and simplifying (2.74) for the factor "K" we get,

$$K = \left[tan\left[\left[\frac{Boost}{4}\right] + 45^{\circ}\right]\right]^2 \tag{2.75}$$

Thus, the factor "K" is obtained from (2.75). Furthermore, the frequency of double zero f_z and the frequency of double pole f_p in the compensation circuit is calculated by,

$$f_z = \frac{f_c}{\sqrt{K}} \tag{2.76}$$

$$f_p = f_c \cdot \sqrt{K} \tag{2.77}$$

where f_c is the crossover frequency. From figure 2.17, the capacitors and resistors values can be calculated by,

$$C_{41} = \frac{1}{2\pi f_c G R_{53}} \tag{2.78}$$

where G is the amplifier gain at the crossover frequency f_c. Similarly, components R_{44}, C_{40}, R_{49} and C_{53} are calculated by,

$$C_{40} = C_{41}\,[K - 1] \tag{2.79}$$

$$R_{44} = \frac{\sqrt{K}}{2\pi f_c C_{40}} \tag{2.80}$$

$$R_{49} = \frac{R_{53}}{K - 1} \tag{2.81}$$

$$C_{53} = \frac{1}{2\pi\sqrt{K} f_c R_{49}} \tag{2.82}$$

The reference voltage V_{REF} is selected, such that the output voltage V_O is greater than the reference voltage. The current I_{BIAS} through the resistors R_{53} and R_{52} play a vital role in the selection of these resistors. Thus, the resistors R_{53} and R_{52} are calculated by,

$$R_{52} = \frac{V_{REF}}{I_{BIAS}} \tag{2.83}$$

$$R_{53} = \left[\frac{V_O - V_{REF}}{V_{REF}}\right] \cdot R_{52} \tag{2.84}$$

3

Case set-up

Figure 3.1: Overview and work flow of the master thesis

3.1 Base verification

The benchmarked Ericsson developed Si MOSFET based half-bridge DC/DC converter is operated at 280 kHz, where each Si MOSFET operates at f_{sw} 140 kHz. Table 3.1 shows specifications of the Si MOSFET used in the benchmarking, where Q_G and V_{GS} is high for both the primary and the secondary MOSFETs in comparison with the GaN MOSFETs. The conduction and the switching losses for both the primary and secondary side Si MOSFETs are tabulated.

Table 3.1: *Si* MOSFET specification with f_{sw} of 140 kHz for FET

Parameters	**BSC030N08NS5**	**BSC028N06NS**
Placement	Primary MOSFET	Synchronous MOSFET
Drain to source voltage	80 V	60 V
Gate to source voltage	20 V	20 V
Maximum on state resistance	3 mΩ	2.8 mΩ
Total gate charge	61 nC	37 nC
Gate to source charge	20 nC	12 nC
Gate to drain charge	13 nC	7 nC
Output charge	73 nC	43 nC
Continuous drain current	100 A	100 A
Conduction losses	0.5 W	0.9 W
Switching losses	1.7 W	2.4 W
Total power losses	2.2 W	3.2 W

The existing Si MOSFET based half-bridge DC/DC converter consists of an isolated ER23 planar transformer with 3F3 core material operating at 280 kHz. The controller is placed on the secondary side of the converter, and it adjusts the dead time during the MOSFET operation. The primary and secondary MOSFETs are operated by individual external gate drivers. Table 3.2 shows the different parameter values used for designing the planar ER23 transformer core.

3.2 Design of Planar transformer

In this section, the selection of planar cores and the design of the planar transformer are discussed.

3.2.1 Core selection

With the reduction in size as a top priority for an isolated half-bridge GaN MOSFET based DC/DC converter, the possible options for the planar transformer core would be ER23, ER18, and ER14.5. These planar ER cores have the same window height, but their window width varies with the core size. The higher core size has better thermal performance and a larger window area. Also, they exhibit higher nominal inductance compared to the smaller core sizes. The magnetic flux density B_{AC} increases with a decrease in core area A_e, which gradually increases the core loss.

Table 3.2 shows the suitable planar core shapes with 3F3 core material having zero air gap.

Table 3.2: Suitable core selection for half-bridge DC/DC converters with the 3F3 core material and [$\mu_{air-gap} \approx 0$] [15].

Parameter	**Notation**	**ER14.5**	**ER18**	**ER23**
Core factor [mm^{-1}]	$\Sigma(l/A)$	1.08	0.73	0.53
Effective core volume [mm^3]	V_e	333	667	1340
Effective magnetic length [mm]	l_e	19	22.1	26.6
Effective core area [mm^2]	A_e	17.6	30.2	50.2
Minimum core area [mm^2]	A_{min}	17.3	30.1	50
Mass of core half [g]	m	0.9	1.6	3.2
Nominal inductance [[$A_L \pm 25\%$] nH]	A_L	1400	2400	3400
Effective permeability	μ_e	≈ 1200	≈ 1100	≈ 1180
Window width [mm]	W_w	3.4	4.48	5.8
Window height [mm]	W_h	3	3	3.1

There are promising core materials such as 3F4, 3F3, 3F35 and 3F36 operating under the specific switching frequency f_{sw} of 600 kHz. Table 3.3 shows the Steinmetz hysteresis coefficient and other numerical coefficients for different core materials. In this thesis, the reduction of the component size is considered as the top priority. The different core shapes such as ER14.5, ER18, and ER23 are initially compared with the benchmarked ER23 core shape.

Table 3.3: Transformer core losses with different core materials and core size selection [9],[10]

Ferrites	C_m	**x**	**y**	C_{t2}	C_{t1}	C_t
3F4	$12{\cdot}10^{-4}$	1.75	2.9	$0.95{\cdot}10^{-4}$	$1.1{\cdot}10^{-2}$	1.15
3F3	$3.6{\cdot}10^{-9}$	2.4	2.25	$0.67{\cdot}10^{-4}$	$0.81{\cdot}10^{-2}$	1.14
3F35	$1.12{\cdot}10^{-7}$	2.19	2.71	$1.28{\cdot}10^{-4}$	$2.10{\cdot}10^{-2}$	1.80
3F36	$1.12{\cdot}10^{-7}$	2.19	2.71	$8.92{\cdot}10^{-5}$	$1.17{\cdot}10^{-2}$	1.28

Table 3.4: Parameters for calculating core loss in a high-frequency planar transformer

Parameter	**Value**
Number of secondary turns	2
Number of primary turns	3
Turns ratio	1.5
Maximum input voltage	60 V
Temperature	120 °C
Duty cycle	22.8%
Operating frequency	600 kHz

The 3F3 core material provides a reliable and enhanced planar transformer operation. Table 3.4 provides the parameter values for calculating the core loss. Using (2.63) and (2.64), the core loss P_{CL} for the planar transformer having different core shapes with the 3F3 core material is calculated and tabulated as shown in table 3.5. The decrease in the magnetic core area increases the operating magnetic flux density B_m resulting in a higher core loss.

Table 3.5: Transformer core losses with different core size selection [15].

Parameters	**Notation**	**ER14.5**	**ER18**	**ER23**
Effective magnetic length [mm]	l_e	19	22.1	26.6
Effective core area [mm^2]	A_e	17.6	30.2	50.2
Effective core volume [mm^3]	V_e	333	667	1340
Magnetic flux density [mT]	B_m	106.5	62.1	37.4
Power loss density with 3F3 $\left[\frac{\text{mW}}{\text{cm}^3}\right]$	P_v	1949.1	578.5	184.4
Approximate core loss with 3F3 [W]	P_{CL}	0.65	0.4	0.25

In this thesis, the planar transformer design tool is used to analyze and design a planar transformer. The design of a planar transformer is explained by considering different case studies, as discussed below.

3.2.2 Case A: Different core selections

For analyzing the performance of the planar transformer, it is designed considering each planar core, as shown in table 3.6. In this case, a stack of seven layers PCB with the copper thickness of 105 µm for each layer is considered for designing the planar transformers. The insulation thickness of 150 µm is considered between the layers. From table 3.6, the core loss for the ER14.5 is predominantly high in comparison with the ER18 and ER23 planar cores. The smaller core size provides higher flux density, which correspondingly increases the core loss. Considering the planar core ER14.5 would yield higher core and copper loss in comparison with the ER18 and ER23 planar cores. Thus, operating with the planar core ER14.5 would lead to thermal constraints for the operation of the planar transformer.

Table 3.6: Transformer losses with different core size selection having seven layers

Parameters	**Notation**	**ER14.5**	**ER18**	**ER23**
Effective core area [mm^2]	A_e	17.6	30.2	50.2
Effective core volume [mm^3]	V_e	333	667	1340
Magnetic flux density [mT]	B_m	107.7	62.8	37.8
Core loss with 3F3 material [W]	P_{CL}	0.6	0.4	0.24
Winding loss for Cu thickness of 105 µm [W]	P_{Cu}	4.35	4.05	3.8
Total losses in the transformer [W]	P_{Total}	4.95	4.4	4.05
Overall efficiency	η	98.05%	98.3%	98.4%

The winding loss comprises of both AC and DC resistances across the primary and secondaries of the planar transformer as shown in table 3.7.

Table 3.7: AC and DC resistances across primary and secondaries of planar transformer for Cu thickness of 105 µm

Parameters	ER14.5	ER18	ER23
AC resistance primary	8.9 mΩ	8.3 mΩ	7.9 mΩ
AC resistance secondaries	5.9 mΩ	5.5 mΩ	5.1 mΩ
DC resistance primary	6.9 mΩ	6.4 mΩ	6.1 mΩ
DC resistance secondaries	4.6 mΩ	4.25 mΩ	3.95 mΩ

3.2.3 Case B: Depending on number of layers

The parallel winding connection reduces both AC and DC resistances across the primary and secondaries of the planar transformer. In this case, the planar transformer is designed considering the planar core ER18 and ER23 as shown in table 3.8. A stack of 14 layers PCB with the copper thickness of 105 µm for each layer and having an insulation thickness of 90 µm between the layers is considered for designing the planar transformers.

Table 3.8: Transformer losses with parallel winding connections - 14 layers

Parameters	Notation	ER18	ER23
Effective core area	A_e	30.2 mm^2	50.2 mm^2
Effective core volume	V_e	694.6 mm^3	1340 mm^3
Magnetic flux density	B_m	62.8 mT	37.8 mT
Core loss with 3F3 material	P_{CL}	0.4 W	0.3 W
Winding loss for Cu thickness of 105 µm	P_{Cu}	2.45 W	1.9 W
Total losses in the transformer	P_{Total}	2.85 W	2.2 W
Overall efficiency	η	99.05%	99.15%

Table 3.9: AC and DC resistances across primary and secondaries of planar transformer for Cu thickness of 105 µm

Parameters	ER18	ER23
AC resistance primary	4.15 mΩ	3.9 mΩ
AC resistance secondaries	2.75 mΩ	2.6 mΩ
DC resistance primary	3.2 mΩ	3.0 mΩ
DC resistance secondaries	2.15 mΩ	2.0 mΩ

There is an improvement in the overall efficiency for the planar transformers ER18 and ER23 when compared to case A. The winding losses are drastically reduced to half in comparison with case A. There is a reduction in AC and DC resistances across the primary and secondaries of the planar transformer as shown in table 3.9.

Considering the reduction in overall module size as a priority, there has to be a trade-off between the selection of core size and its losses associated. Thus, the thesis focuses on designing the planar ER18 transformer having a stack of 14 layers PCB.

3.2.4 Case C: Depending on copper thickness for each layer

In this case, the effect of copper thickness for designing the planar ER18 transformer is analyzed. The insulation thickness of 90 µm is considered between the layers. Table 3.10 shows the design results with different standard copper thickness.

The design of the planar ER18 transformer with less copper thickness would yield high winding losses. The increase in the copper thickness substantially increases the window height of the ER18 transformer. Thus, a slight increase in the core loss is observed from the table 3.10. A better efficiency is observed between the copper thickness of 90 µm and 105 µm. Further increase in copper thickness above 105 µm would yield higher core loss.

Table 3.10: Transformer ER18 design considering different copper thickness with insulation thickness of 90 µm.

Parameters	**Cu-**70 µm	**Cu-**90 µm	**Cu-**105 µm	**Cu-**140 µm
AC resistance primary	5.15 mΩ	4.4 mΩ	4.15 mΩ	4.2 mΩ
AC resistance secondaries	3.4 mΩ	2.9 mΩ	2.8 mΩ	2.8 mΩ
DC resistance primary	4.85 mΩ	3.8 mΩ	3.2 mΩ	2.4 mΩ
DC resistance secondaries	3.2 mΩ	2.5 mΩ	2.15 mΩ	1.6 mΩ
Respective winding loss	2.5 W	2.15 W	2.0 W	2.05 W
Core loss with 3F3 material	0.4 W	0.4 W	0.4 W	0.45 W
Total losses in the transformer	2.9 W	2.55 W	2.45 W	2.45 W
Overall efficiency	98.85%	99%	99.05%	99.05%

3.2.5 Case D: Depending on insulation thickness between layers

In this case, the effect of different insulation thickness between the layers in designing the ER18 planar transformer is analyzed. The copper thickness of 90 µm for each layer is considered. As discussed in subsection 2.12.2, the interwinding capacitance is increased due to an increase in the winding surface area. The effect of interwinding capacitance is analyzed by varying the insulation thickness between the layers for the planar ER18 transformer. Table 3.11 shows the design results with different standard insulation thickness.

Table 3.11: Transformer ER18 design considering different insulation thickness between layers with copper thickness of 90 µm.

Parameters	D_a=70 µm	D_a=90 µm	D_a=105 µm	D_a=140 µm
Inter - winding capacitance	998 pF	777 pF	666 pF	499 pF
Respective winding loss	2.15 W	2.15 W	2.15 W	2.15 W
Core loss with 3F3 material	0.4 W	0.4 W	0.4 W	0.45 W
Total losses in the transformer	2.55 W	2.55 W	2.55 W	2.6 W
Overall efficiency	99.01%	99%	99%	98.99%

The design of the planar ER18 transformer with lower insulation thickness provides higher interwinding capacitance. Similarly, low interwinding capacitance is observed for higher insulation thickness. A high efficiency is observed between the insulation thickness of 90 µm and 105 µm. Further increase in insulation thickness above 105 µm would yield higher core loss.

From the above case studies, the promising and efficient planar ER18 transformer is designed. It involves a stacked 14 layers PCB with the copper thickness of 90 µm for each layer and the insulation thickness of 90 µm between the layers, as shown in figure 3.2. Furthermore, table 3.12 shows the design specification of the planar transformer, which includes the overall efficiency and losses associated with it. Figure 3.3 show winding connections for a stack of 14 layers PCB.

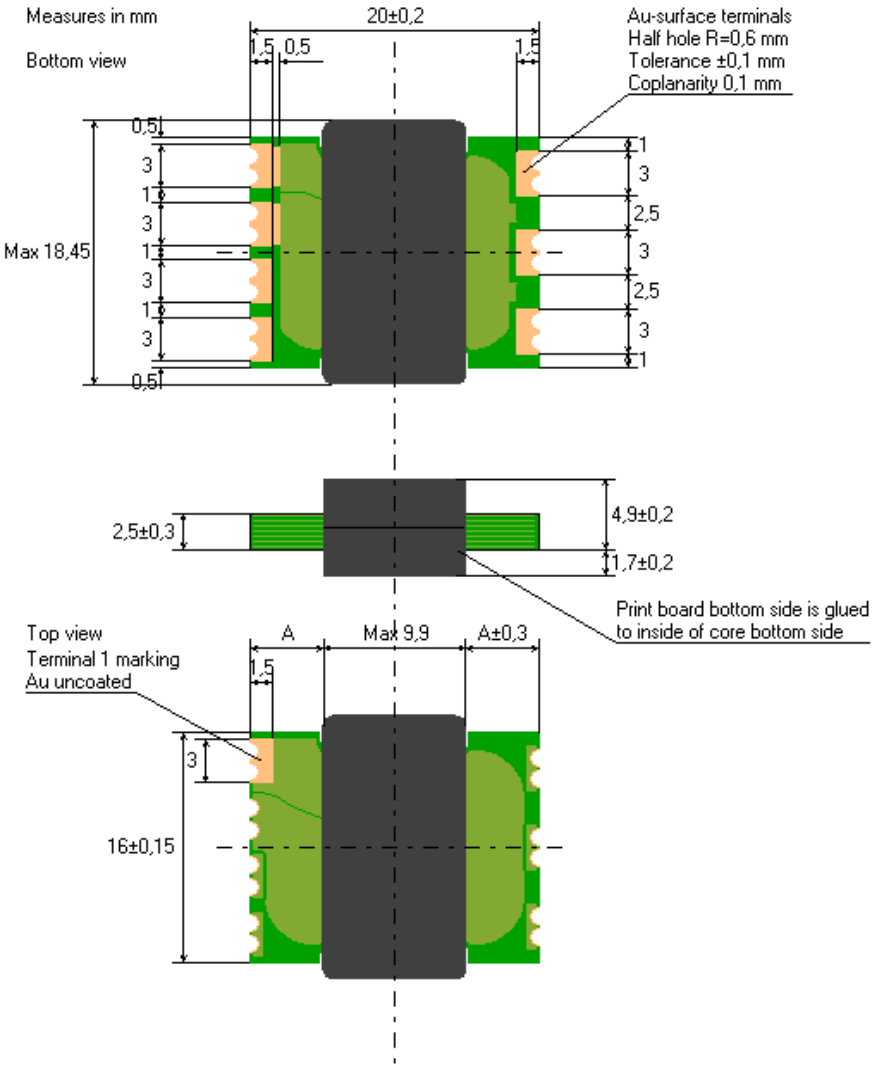

Figure 3.2: Overview of designed planar ER18 transformer

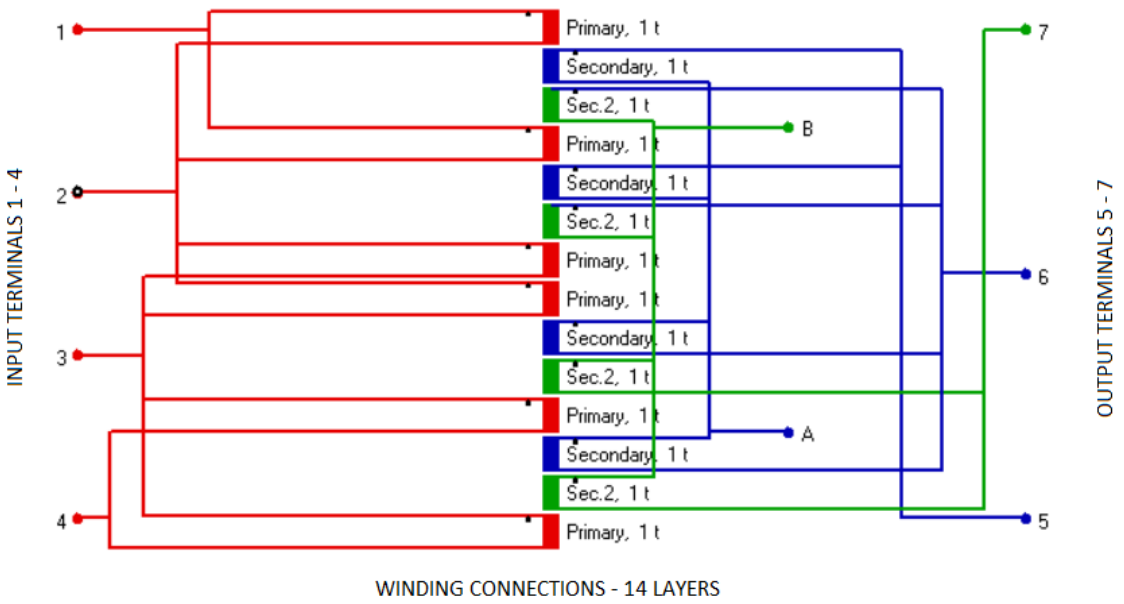

Figure 3.3: Planar ER18 transformer - Winding connections for 14 layers PCB

Table 3.12: Design specification of the planar ER18 transformer

Parameter	Values
Core loss with 3F3 material	0.4 W
Copper thickness	90 µm
Insulation thickness between the layers	90 µm
AC resistance primary	4.4 mΩ
AC resistance secondaries	2.9 mΩ
DC resistance primary	3.8 mΩ
DC resistance secondaries	2.5 mΩ
Respective winding loss	2.15 W
Total losses in the transformer	2.55 W
Overall efficiency	99%
Inter - winding capacitance	777 pF
Overall inductance	[21.60 ± 25%] µH

3.3 Design and selection of the inductor

The output inductor is designed to handle the maximum output ripple current. Table 3.13 shows the parameters for designing the output inductor. By inserting the design parameters in (2.35), the output inductor is calculated to be 495 nH.

The output inductor is selected based on the different operating conditions such as temperature, DC resistance (DCR), saturation current, and size of the inductor.

The higher inductor value provides less output ripple during the operation of the converter. For a high current operation, the inductor with the least DCR enhances the overall efficiency of the converter.

Table 3.13: Parameter values required for designing output inductor

Parameter	Notation	Value
Number of secondary turns	N_S	2
Number of primary turns	N_P	3
Maximum input voltage	V_{d-max}	60 V
Output voltage	V_O	9 V
Duty cycle	D_{min}	45.6%
Output current ripple	Δi_L	8.3 A
Switching time period	T_S	1.67 µs

Table 3.14 shows the different inductors suitable for operating the half-bridge isolated DC/DC converter. The inductor XAL1580-741 from COILCRAFT is selected since it provides the least DCR and has a saturation current of 86 A when compared to other inductors.

Table 3.14: Selection of suitable output inductor from COILCRAFT

Parameter	XAL1580	XAL1350	XAL1060
Inductance	740 nH	630 nH	680 nH
Maximum DCR	0.86 mΩ	1.7 mΩ	1.5 mΩ
Saturation current	86 A	74 A	52 A
Length of the inductor	16.4 mm	14.2 mm	11.8 mm
Width of the inductor	15.4 mm	13.2 mm	11.8 mm
Height of the inductor	8 mm	5 mm	6 mm

3.4 Design of feedback system for the controller

As discussed in section 2.13, the stability of the system enhances the overall performance. The feedback loop in this thesis is analyzed using a MATLAB simulation. The crossover frequency of 20 kHz is selected for enhancing the stability of the system. Figure 3.4 shows the bode plot of the plant at the corner frequency of 20 kHz. The magnitude gain of 16.9 dB and phase angle of $-112.1°$ is observed at the crossover frequency of 20 kHz. The type 3 compensation is used in this thesis for enhancing the stability of the system.

The "K" factor technique is used for designing the type 3 compensation. The reference voltage of 2.5 V is selected, which is less than the output voltage of 9 V. The resistors R_{52} and R_{53} are calculated by using (2.83) and (2.84). Furthermore, by using the magnitude gain and the phase angle of the plant, the factor "K" is calculated by using (2.75).

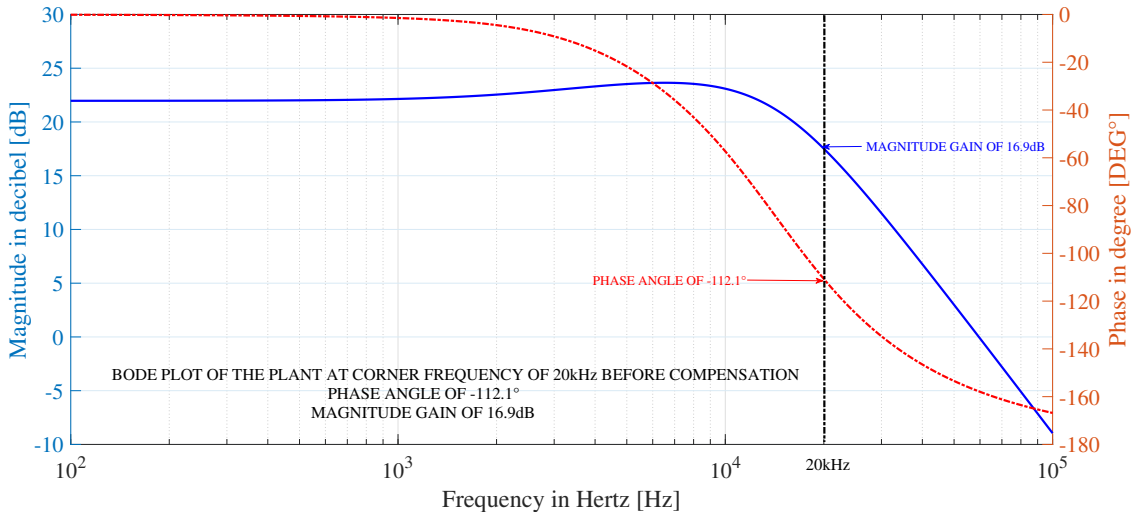

Figure 3.4: Simulated bode plot of the plant at the crossover frequency of 20 kHz

In this thesis, the type 3 compensation is designed with the required phase margin PM of 65°. Figure 3.5 shows the type 3 compensation with the component values. As discussed in section 2.13, the components involved in type 3 compensation are calculated.

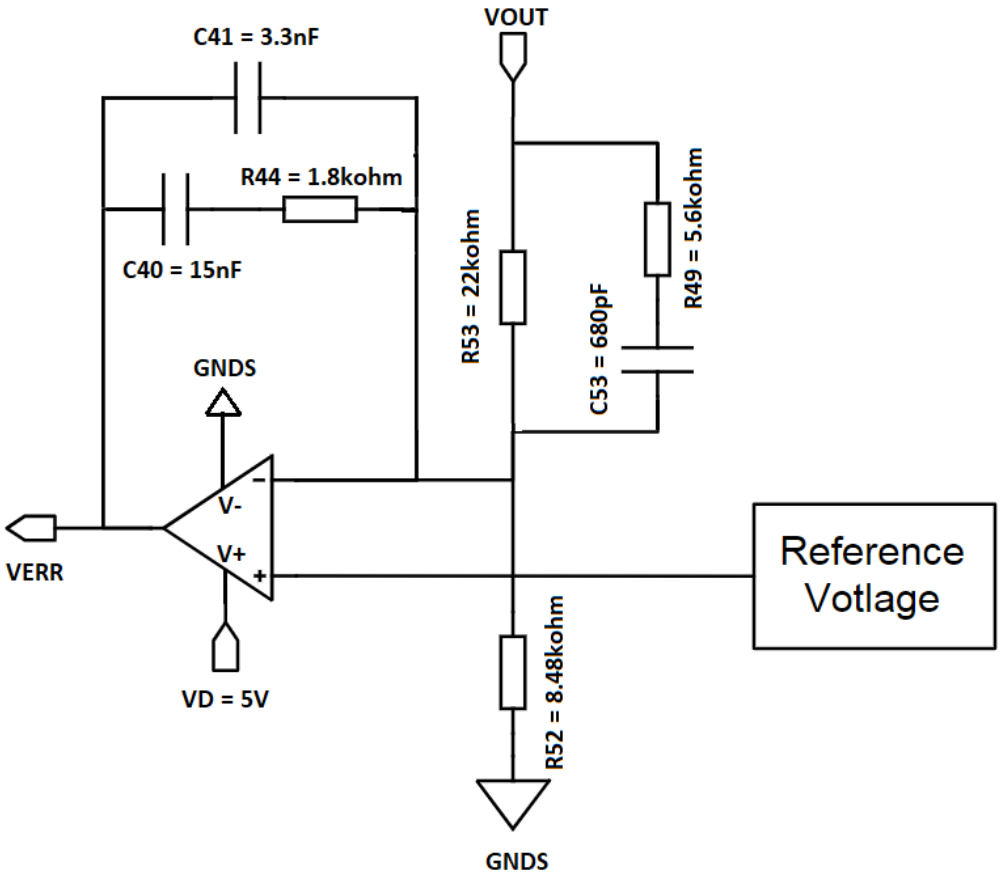

Figure 3.5: Calculated component values for type 3 compensation

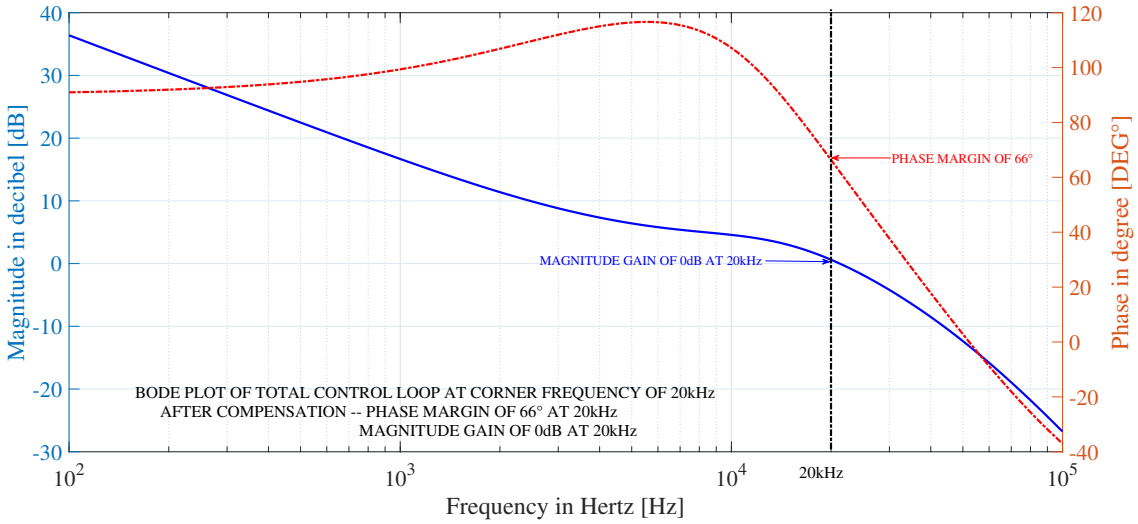

Figure 3.6: Simulated bode plot of the total control loop at the corner frequency of 20 kHz with type 3 compensation circuit

Figure 3.6 shows the bode plot of the total control loop at the corner frequency of 20 kHz. The magnitude gain of 0 dB and the phase angle of 66° is observed at the corner frequency of 20 kHz with the type 3 compensation circuit. The detailed type 3 compensation is explained in Appendix C.1.

4

Simulation Model

In this section, a simulation model of the half-bridge DC/DC converter and corresponding results are discussed. The simulations are performed using the LTspice software.

4.1 LTspice modelling

One of the ways to check the operation of an electrical circuit is by performing a simulation. The simulation model provides the overall performance of the module and components associated. The LTspice simulation provides a rapid simulation process with enhanced schematic and waveform viewer. In this simulation, the performance of the GaN MOSFET based half-bridge DC/DC converter is evaluated by operating at 120 °C.

The LTspice schematic is designed considering the operation of the planar ER18 transformer. Furthermore, the "GaN" MOSFET and the controller LM5036 are not available for the LTspice simulation due to the non-availability of the LTspice library file. The GaN MOSFETs EPC2020 and EPC2022 are considered for the primary and the secondary side MOSFETs. Similar to LM5036, the analog controller LM5035B from Texas Instruments is considered for the LTspice simulation. The controller LM5035B provides gate pulses for both primary and secondary GaN MOSFETs. The simulation doesn't include the losses due to parasitics and PCB conduction losses. Figure 4.1 shows the simulation model of the GaN MOSFET based half-bridge DC/DC converter. The overall operational performance is evaluated by considering different case studies.

4.1.1 Case A: Simulation without controller and snubber

In this case study, the GaN MOSFET based half-bridge DC/DC converter is simulated without considering the controller and snubber. For different input voltages, the performance of the converter is analyzed. Figure 4.2 shows the efficiency of the converter operating at 48 V input voltage for different load currents. A maximum efficiency of 97% is obtained by operating at 48 V input voltage and a load current of 27.8 A. The performance of the converter is considered to be ideal since the effect of the controller, snubbers, and parasitics are not considered. Figure 4.3 shows the efficiency comparison of different input voltages.

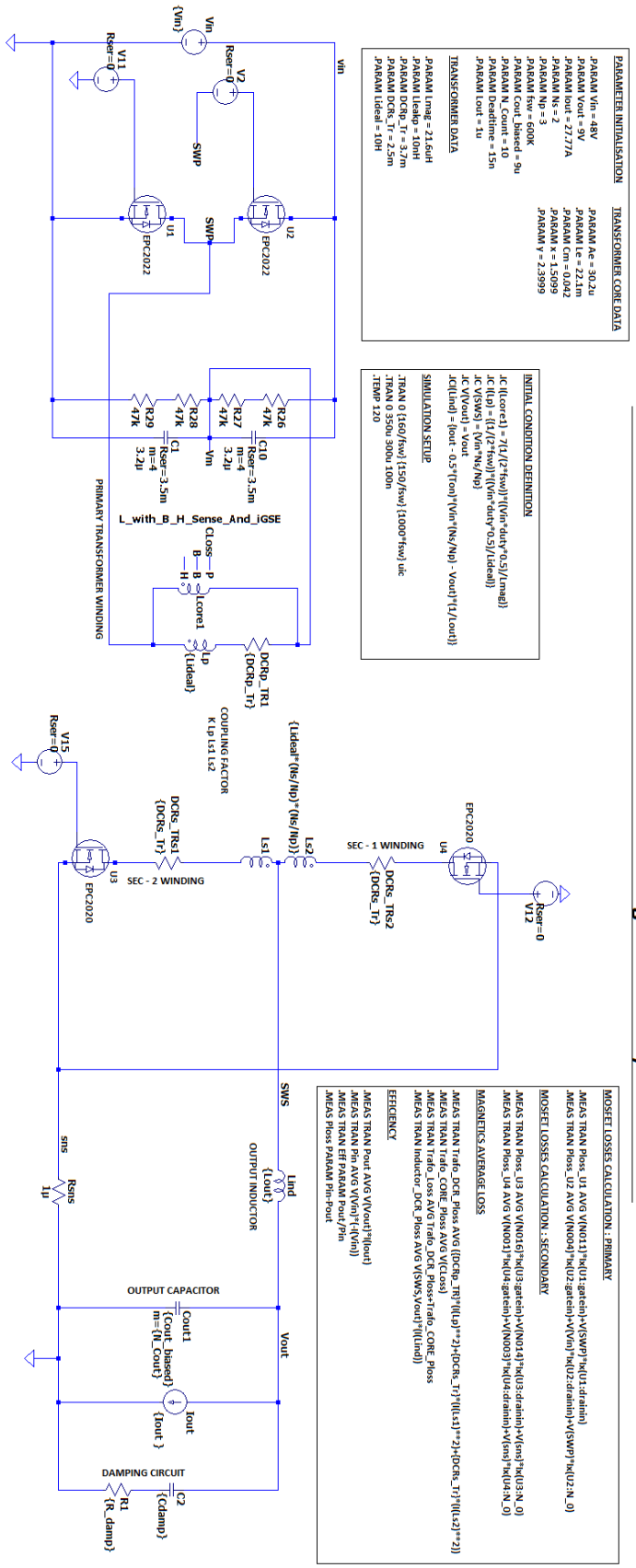

Figure 4.1: LTspice simulation model for the GaN MOSFET based isolated half-bridge DC/DC converter

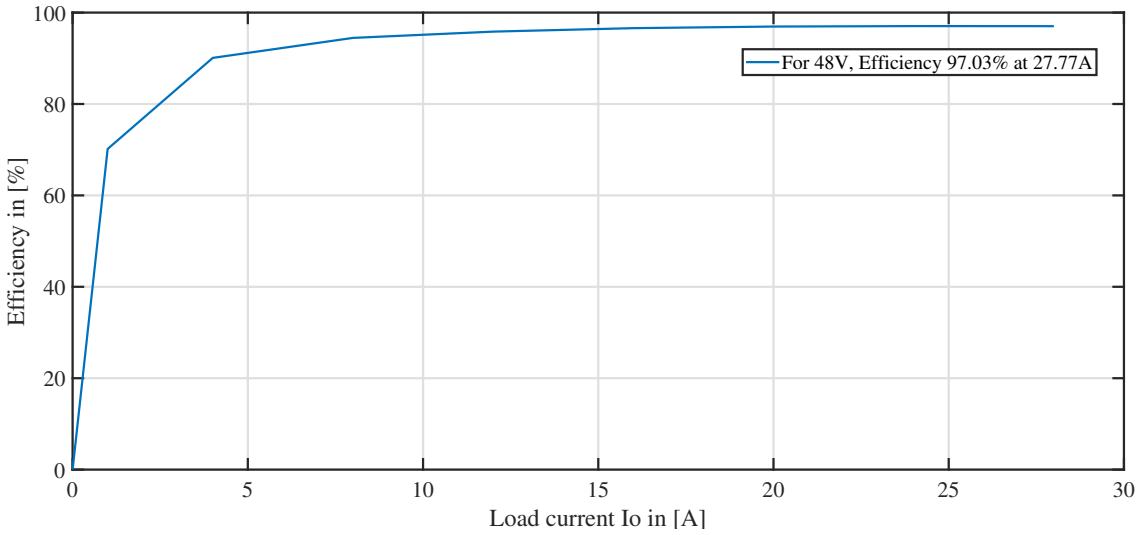

Figure 4.2: Simulated efficiency of the GaN MOSFET based half-bridge DC/DC converter operating at 48 V input voltage for different load currents without controller and snubber.

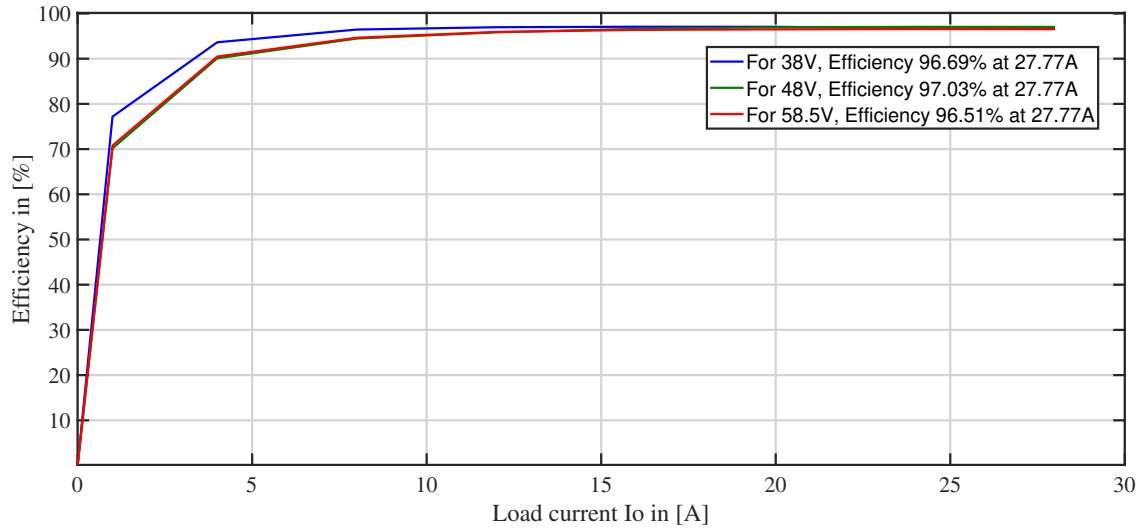

Figure 4.3: Simulated efficiency comparison of the GaN MOSFET based half-bridge DC/DC converter operating at different input voltages without controller and snubber.

4.1.2 Case B: Design of passive snubber

The simulation of the GaN MOSFET based half-bridge DC/DC converter without controller and snubber is considered as an ideal case. The converter operating without snubbers experiences a stress across the MOSFETs during its operation. Figure 4.4 shows the voltage ringing across the MOSFETs EPC2020 without the introduction of the snubber in the converter. As discussed in section 2.7, the snubbers are designed to reduce the voltage peaks and dampen the ringing across the drain to source of the MOSFETs.

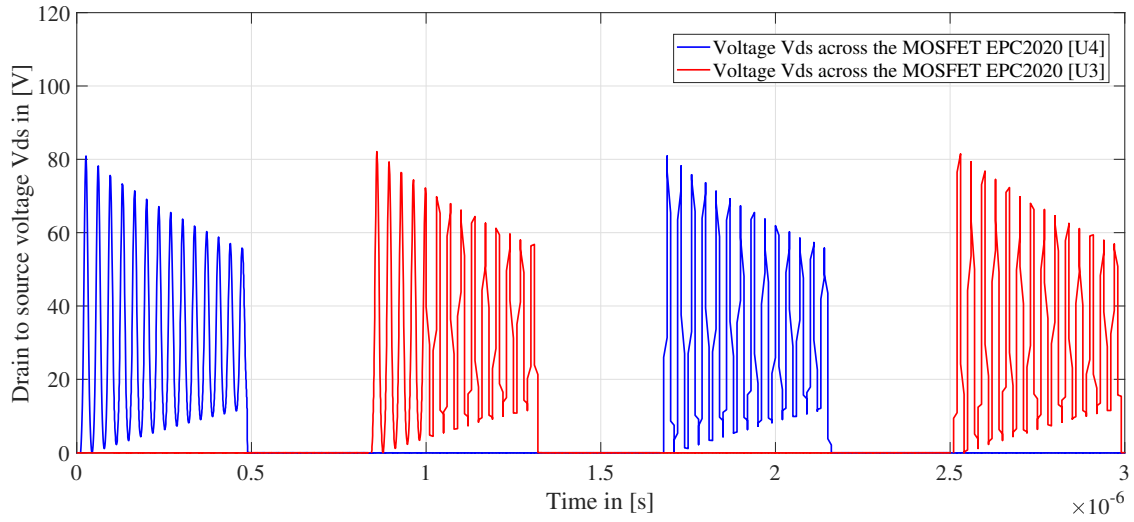

Figure 4.4: Voltage ringing is observed during the non-conduction of synchronous MOSFETs

To design the snubber, initially, the ringing frequency f_r between the voltage peaks are considered. Figure 4.5 shows the zoomed waveform of synchronous MOSFET U_4 from the time period 0.01 µs to 0.6 µs. The ringing frequency value between the voltage peaks is about 28.6 MHz.

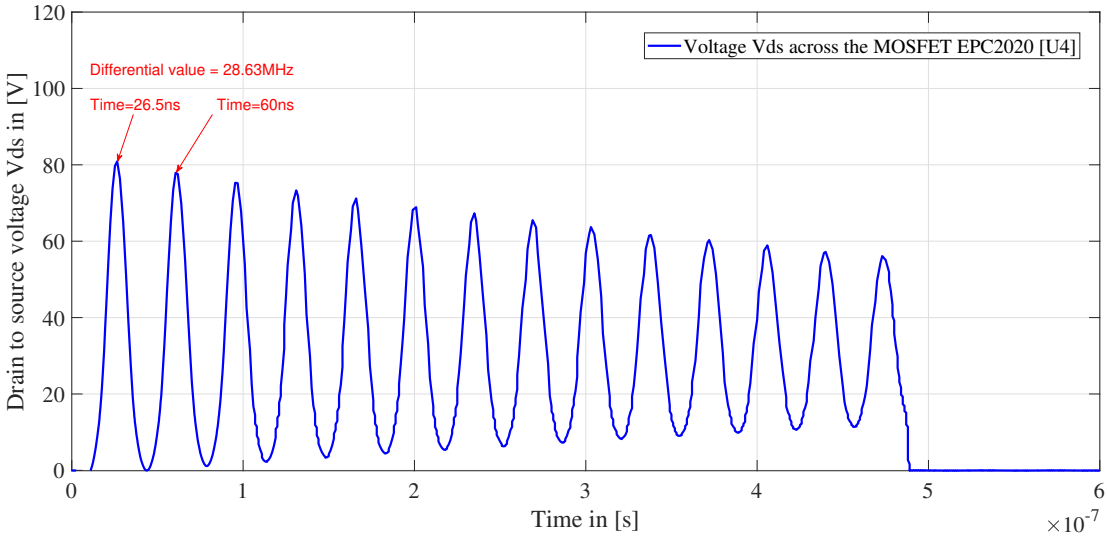

Figure 4.5: The blocking voltage V_{DS} across the synchronous MOSFET U_4 from the time period 0.01 µs to 0.6 µs with ringing frequency f_{r_1} of 28.6 MHz

A random capacitor C_1 of capacitance 10 nF is placed parallel across the secondary winding of the planar ER18 transformer. Again, the ringing frequency between the voltage peaks are considered. The value of the capacitor C_1 should be selected in such a way that it should atleast reduce to 50% of the initial ringing frequency f_{r_1}. Figure 4.6 shows the waveform after the introduction of the capacitor C_1. Now the ringing frequency f_{r_2} value is reduced from 28.6 MHz to 9.35 MHz, which is approximately a 63% reduction in the ringing frequency.

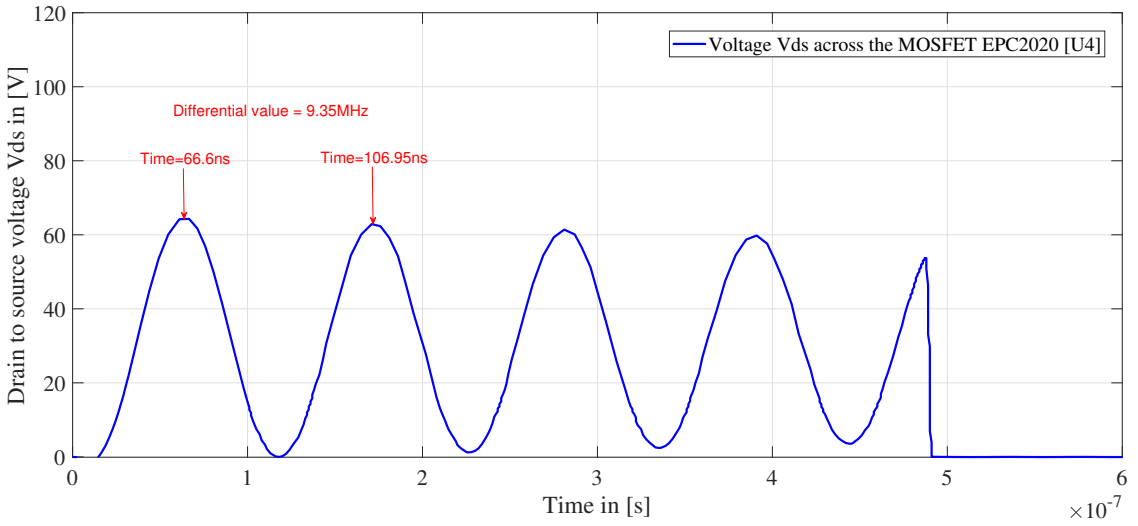

Figure 4.6: The blocking voltage V_{DS} across the synchronous MOSFET U_4 from the time period 0.01 µs to 0.6 µs with reduced ringing frequency f_{r_2} of 9.35 MHz

After obtaining a 63% reduction in the ringing frequency, the snubber capacitor C_{snub} and snubber resistor R_{snub} for the LTspice simulation are calculated using (2.38) and (2.39). The detailed calculation and selection of R_{snub} and C_{snub} is explained in Appendix A.1. A snubber capacitance of 2.4 nF and snubber resistance of 2 Ω is designed across the secondary transformer winding in the LTspice simulation. Figure 4.7 shows the reduction in ripple voltage across the synchronous MOSFETs after the insertion of RC passive snubbers.

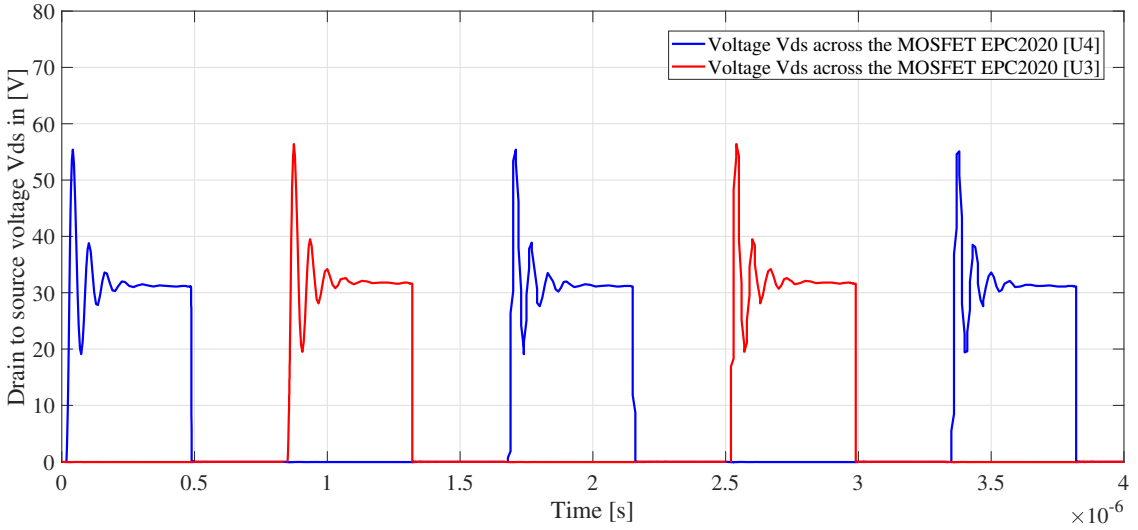

Figure 4.7: Reduction in voltage ripple V_{DS} across the synchronous MOSFETs after insertion of passive snubbers.

A similar procedure is followed for designing the passive snubbers across the primary wiwinding of the planar ER18 transformer. A snubber capacitance of 3.2 nF and snubber resistance of 2 Ω is designed across primary winding of the transformer in the LTspice simulation of the GaN MOSFET based DC/DC converter.

4.1.3 Case C: Simulation with controller and snubber

To evaluate the performance of the GaN MOSFET based DC/DC converter under closed-loop conditions, the voltage controller LM5035B with input feedforward from Texas Instruments is considered. The design parameters of the controller LM5035B for the LTspice simulation is explained in Appendix A.2.

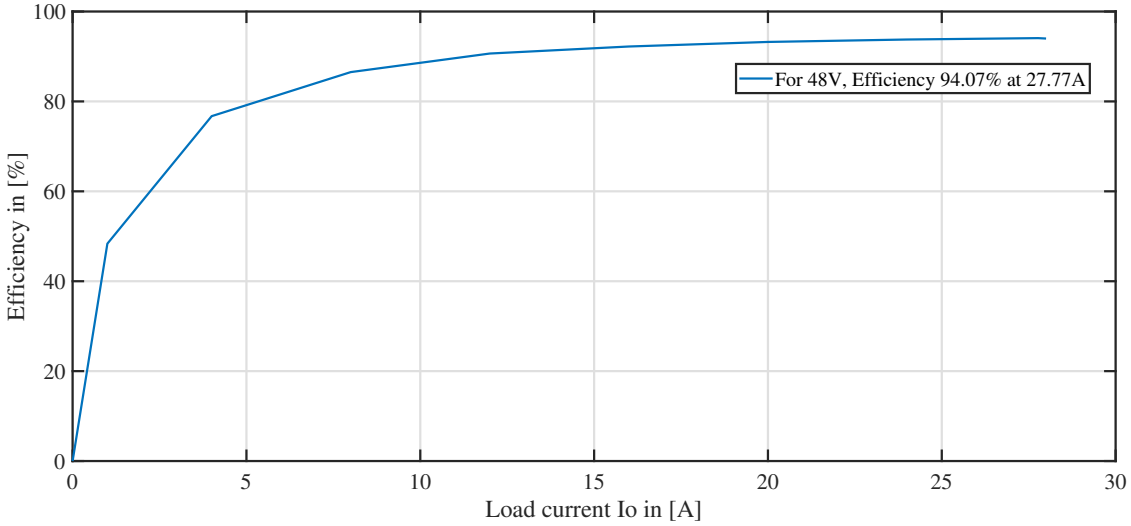

Figure 4.8: Simulated efficiency of the GaN MOSFET based half-bridge DC/DC converter operating at 48 V input voltage for different load currents with controller and snubber.

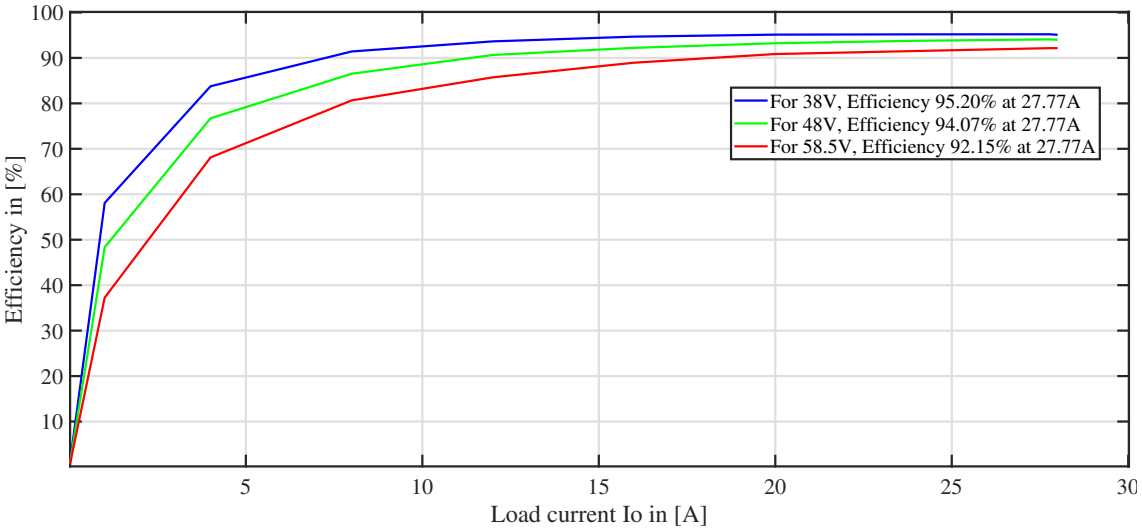

Figure 4.9: Simulated efficiency comparison of the GaN MOSFET based half-bridge DC/DC converter operating at different input voltages with controller and snubber.

In this case, the LTspice simulation of the GaN MOSFET based DC/DC converter provides a constant output voltage of 9 V. The snubbers are incorporated to re-

duce the stress across the MOSFETs. Figure 4.8 shows 94% efficiency of the GaN MOSFET based half-bridge DC/DC converter operating at nominal input voltage 48 V. For different input voltages, the performance of the GaN MOSFET based DC/DC converter is evaluated by applying different load currents. Figure 4.9 shows an efficiency comparison of the converter for the different input voltages. The lower efficiencies are observed in figure 4.9 in comparison with the earlier case 4.1.1 due to additional losses from the controller and snubber.

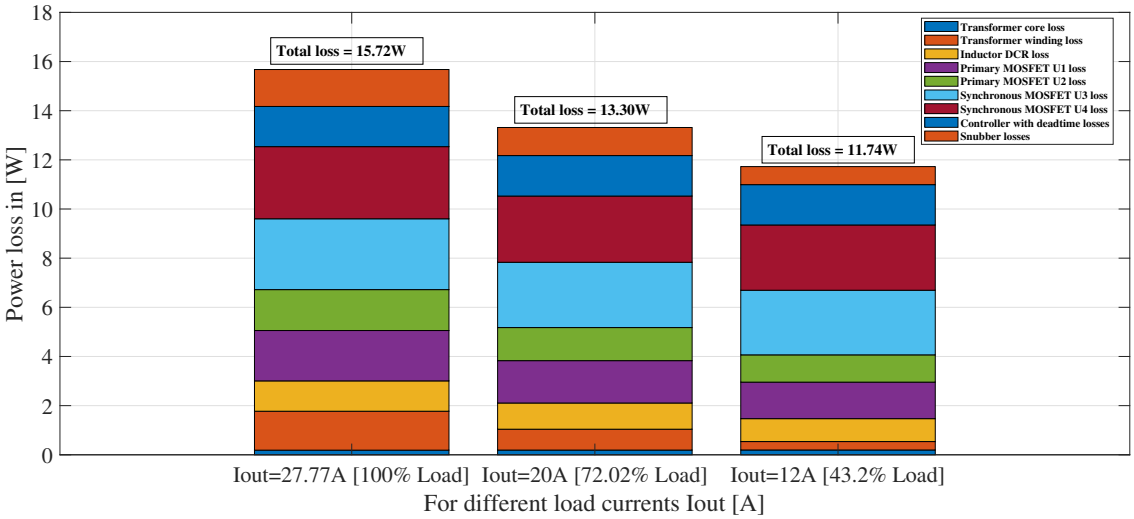

Figure 4.10: Total power loss in the GaN MOSFET based half-bridge DC/DC converter operating at 48 V input voltage for different load currents with controller and snubber.

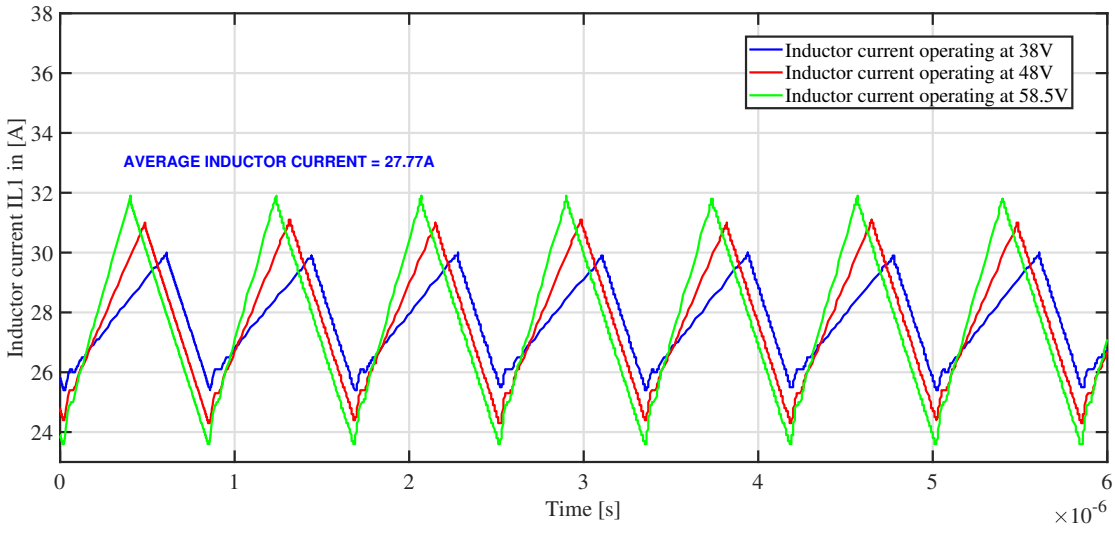

Figure 4.11: Simulation: Inductor current I_{L1} operating at an output current of 27.8 A for different input voltages

Figure 4.10 shows the detailed power loss in various components for the different load conditions. A total loss of 15.7 W is observed for the GaN MOSFET based half-bridge DC/DC converter operating at an output current of 27.8 A, which is 100%

load condition. The loss during the 100% load condition is comparatively higher when compared to 72% and 43% of load conditions. An increase in load current would provide higher losses in various components such as transformer winding, total losses across the primary and secondary MOSFETs, and snubbers.

Figure 4.11 shows the inductor current waveform operating at an output current of 27.8 A for different input voltages. The average output current in all the three cases is 27.8 A. The output ripple current depends on the operating input voltage and its respective duty ratio. Hence figure 4.11 shows different current peaks by operating at three different input voltages.

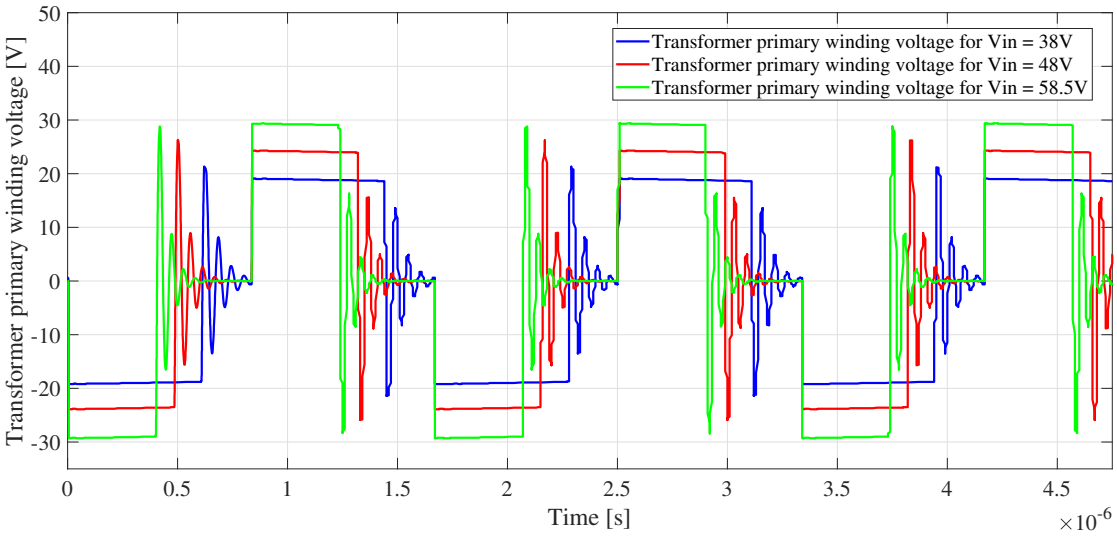

Figure 4.12: Simulation: Voltage across the primary side of the transformer for different input voltage

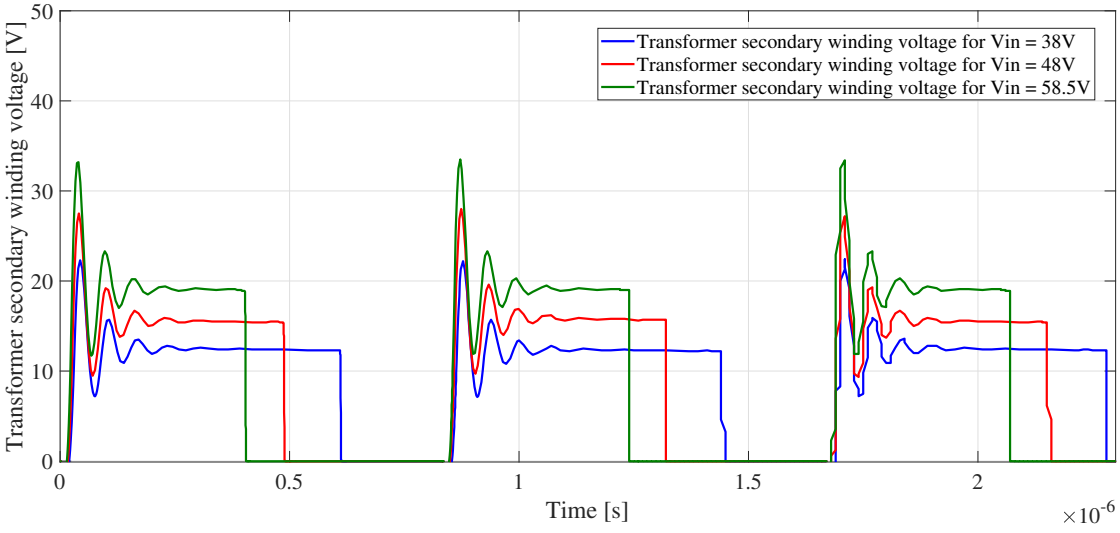

Figure 4.13: Simulation: Voltage across the secondary side of the transformer for different input voltage

Figure 4.12 and 4.13 shows the primary side and the secondary side voltage across the planar E18 transformer respectively, after introducing the snubber. The above voltage waveforms can be compared to theoretical voltage waveforms of the primary and secondary sides of the transformer, as described in section 2.3.

5

PCB design and hardware Implementation

In this section, schematic and PCB design considerations for the GaN MOSFET based isolated half-bridge DC/DC converter are discussed. The PCB designing is performed using KiCad software.

5.1 Schematics in KiCad software

An open-source software called KiCad is used for designing the electronic circuits. Initially, the design starts with schematic capture called Eeschema. Furthermore, the PCB layout with production files can be generated depending on the project requirement. After knowing the overall performance of the GaN MOSFET based isolated half-bridge DC/DC converter in the LTspice simulation, the next step towards hardware implementation is to start with the schematic for the DC/DC converter.

In the schematic, a bulk capacitance of 220 µF is considered at the input. A low pass LC filter is connected across the bulk capacitor before the power stage. Also, adding the filter provides attenuation of noise and surge from the power supply. The power stage consists of two "GaN" MOSFETs operating on the primary side and four "GaN" MOSFETs [two MOSFETs connected in parallel] operating on the secondary side of the converter. The primary and secondary side of the converter is isolated by using a planar ER18 transformer. The designed output inductor of 740 nH is connected across ten parallel output capacitors of 22 µF.

The output voltage of 9 V for the GaN MOSFET based isolated half-bridge DC/DC converter is maintained by having an LM5036 controller. The parameters for the controller LM5036 for hardware implementation is explained in Appendix B.1. The gate driver LMG1210 provides gate pulses for the primary GaN MOSFETs. Similarly, for operating the secondary side GaN MOSFETs, an external isolated 2EDF7275K gate driver is considered. Finally, the schematic is sketched with test points to ease while testing the PCB board. All the schematic components are assigned with respective footprints. The Eeschema provides an integrated electrical rule check, which checks for conflict and missing pins in the schematics. In this thesis, the schematic is electrically verified before generating netlists for the PCB layout. Most of the resistors and capacitors are selected with the 0402 component size.

5.2 PCB layout

The next step towards hardware implementation is the PCB layout design. In view of the reduction in package size, more PCB layers are considered for routing. A stack-up of a six-layer PCB with different copper thickness is shown in table 5.1.

Table 5.1: PCB layers

Layers	**Type**	**Thickness**	**Material**
Top layer	Cu layer + plating	70 µm	
	Prepeg	115 µm	FR4-Tg 170 °C
Inner layer-1	Cu layer	35 µm	
	Prepeg	450 µm	FR4-Tg 170 °C
Inner layer-2	Cu layer	35 µm	
	Prepeg	230 µm	FR4-Tg 170 °C
Inner layer-3	Cu layer	35 µm	
	Prepeg	450 µm	FR4-Tg 170 °C
Inner layer-4	Cu layer	35 µm	
	Prepeg	115 µm	FR4-Tg 170 °C
Bottom layer	Cu layer + plating	70 µm	
	Total stack-up thickness	1600 µm	

Initially, the PCB layout grid is set to 0.1 mm for placing and routing. Furthermore, the design consideration for the PCB layout is shown in table 5.2. The minimum track width is set to 175 µm, and similarly, the minimum via diameter is set to 0.4 mm.

Table 5.2: Design consideration for PCB layout

Parameter	**value**
Minimum track width	175 µm
Minimum via diameter	0.4 mm
Minimum via drill	0.2 mm
Minimum clearance	175 µm
Minimum mask clearance	0.06 mm
Solder mask minimum width	0.08 mm

The loaded netlist is imported for designing the PCB layout. The components are placed such that the least EMI and stray inductance are expected. A dimension of [125 mm · 90 mm] is considered for the PCB board. After completion of the PCB layout work, the relevant production files called Gerber files are generated. Similarly, the files related to the footprint position on the top and bottom layer of PCB are generated. These files are attached to the PCB manufacturers for the production of PCB boards. Figures 5.1 and 5.2 show the top and bottom PCB view of the GaN MOSFET based isolated half-bridge DC/DC converter.

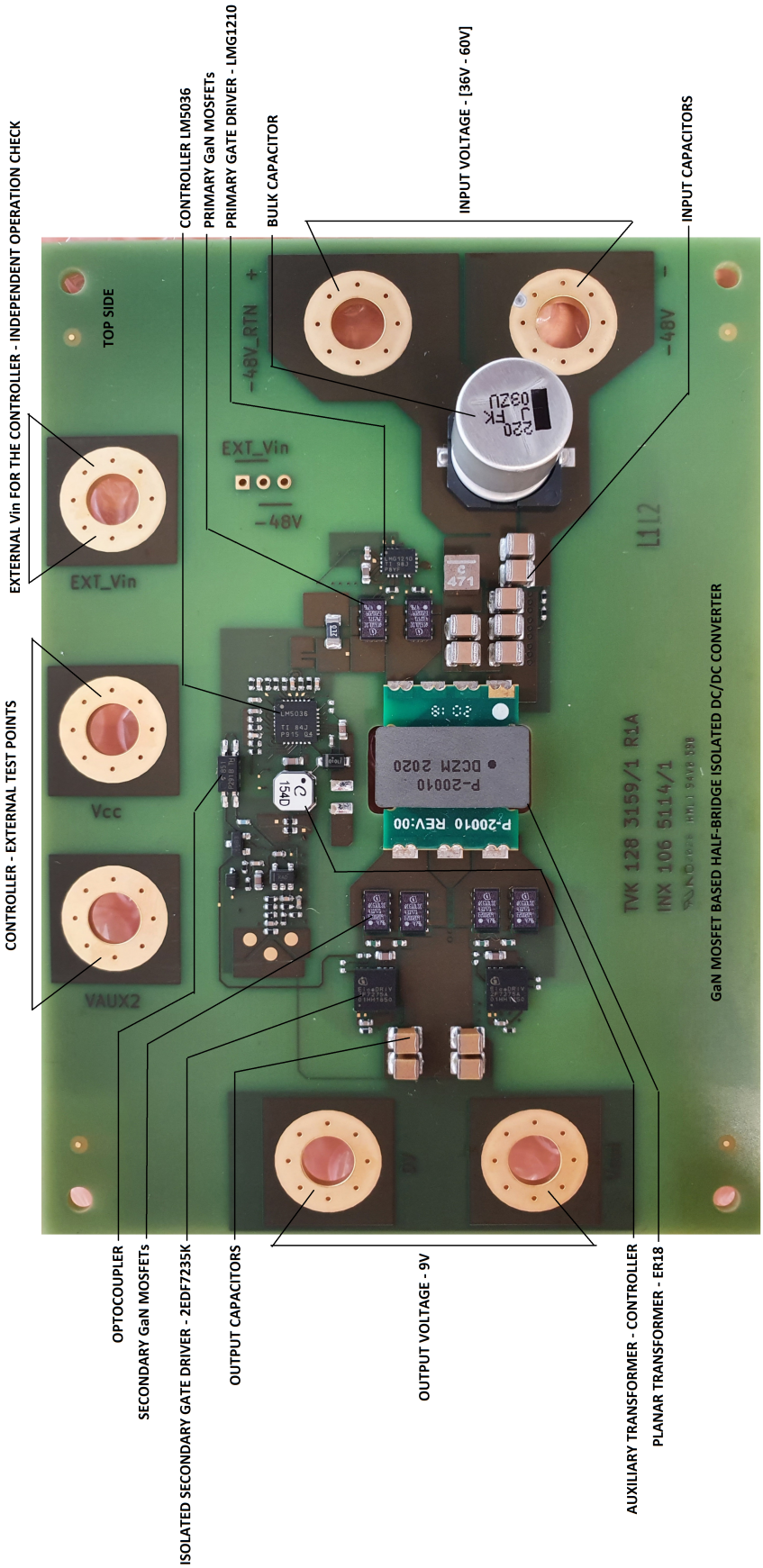

Figure 5.1: PCB top view of the GaN MOSFET based isolated half-bridge DC/DC converter

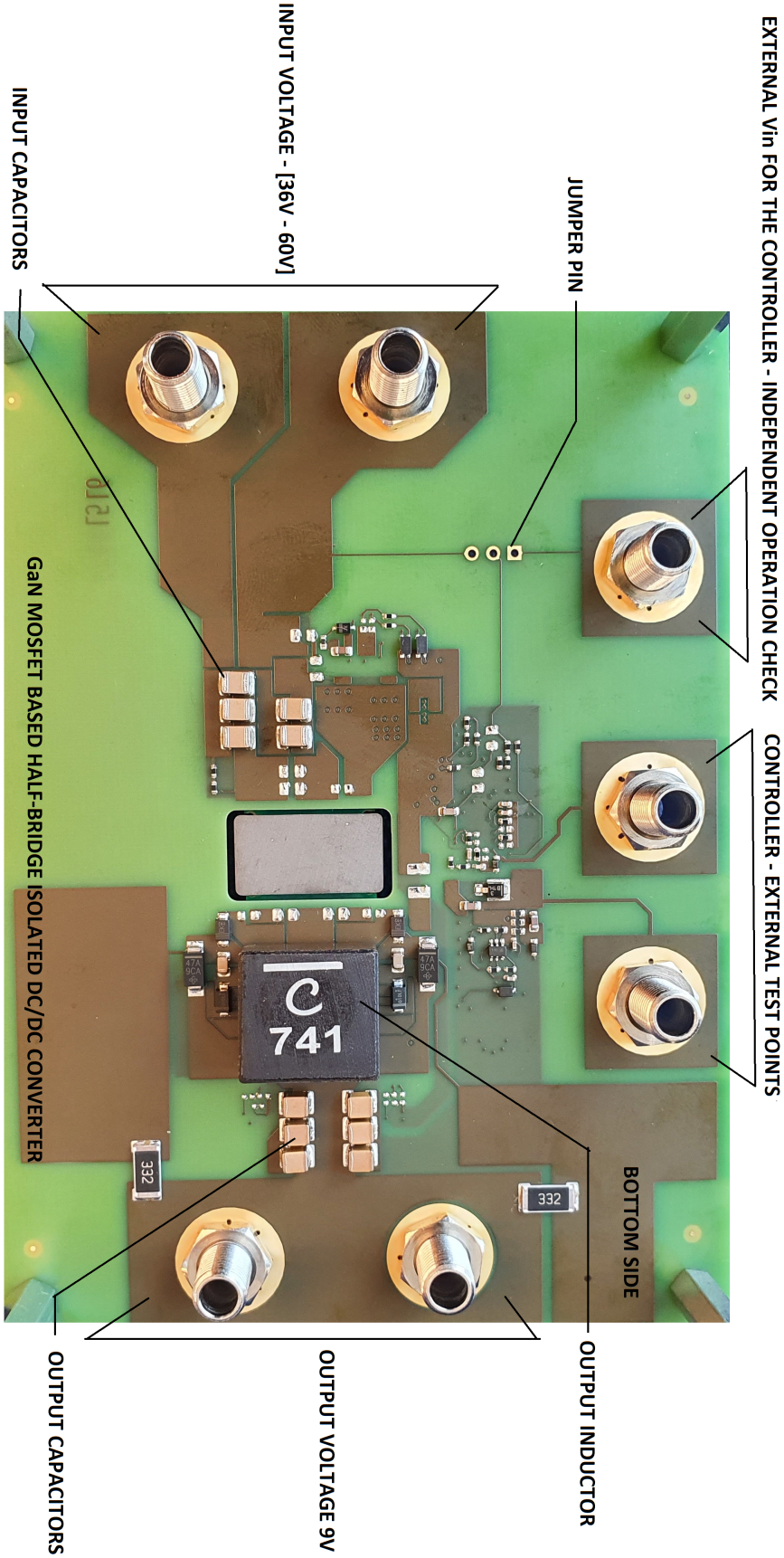

Figure 5.2: PCB bottom view of the GaN MOSFET based isolated half-bridge DC/DC converter

6

Hardware testing of the GaN MOSFET based half bridge DC/DC converter

In this section, the detailed study on the steady-state operation of the controller LM5036 is discussed. Furthermore, the effect of passive snubber and the operating thermal characteristics of the GaN MOSFET based half-bridge DC/DC converter are analyzed.

6.1 Steady-state operation of the controller LM5036

Initially, the jumper pin is connected between the external input voltage V_{in} and the controller circuit to examine the operation of the controller LM5036 independently, as shown in figure 5.2.

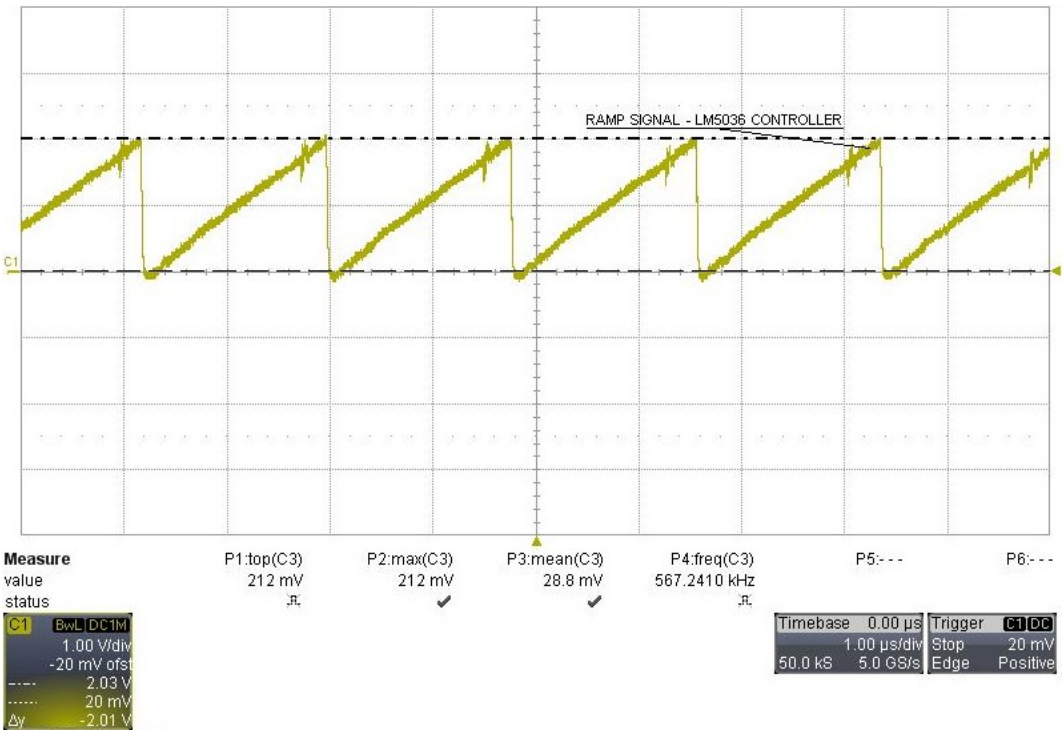

Figure 6.1: Measured sawtooth ramp signal of 2 V after the controller LM5036 start-up.

As discussed in subsection 2.8.2, the parameters for the controller LM5036 are calculated in Appendix B.1. Figure 6.2 shows the different operational modes for the controller LM5036. The GaN MOSFET based half-bridge DC/DC converter is enabled only when the auxiliary supply of the controller operates in the synchronous mode without any internal faults. This criterion is achieved when the controller voltage V_{in} exceeds UVLO with the reference and bias voltage above their undervoltage thresholds. The sawtooth ramp signal is actuated when the auxiliary supply of the controller operates in the synchronous mode without any internal faults. The designed parameter for the controller LM5036 provides the sawtooth ramp signal of 2 V, as shown in figure 6.1.

CRITERIA	VCC AND REF REGULATORS	AUXILIARY SUPPLY	HALF-BRIDGE CONVERTER
UVLO < V_{SD}	OFF	OFF	OFF
(V_{SD} < UVLO < V_{UVLO}) & (V_{IN} < V_{AUX_UVLO})	ON	OFF	OFF
(V_{SD} < UVLO < V_{UVLO}) & (VCC & REF > UV) & (V_{IN} > V_{AUX_UVLO})	ON	ON at ASYNC Mode	OFF
(UVLO > V_{UVLO}) & (V_{IN} > V_{AUX_UVLO}) & (VCC & REF > UV) & No Faults	ON	ON at SYNC Mode	ON
(UVLO > V_{UVLO}) & (V_{IN} > V_{AUX_UVLO}) & (VCC & REF > UV) & Any Faults	ON	ON at ASYNC Mode	OFF
(VCC & REF > UV) & (V_{IN} > V_{AUX_UVLO}) & AUX Current Limit	ON	ON at ASYNC Mode	NA

Figure 6.2: Operational modes for the controller LM5036 [17]

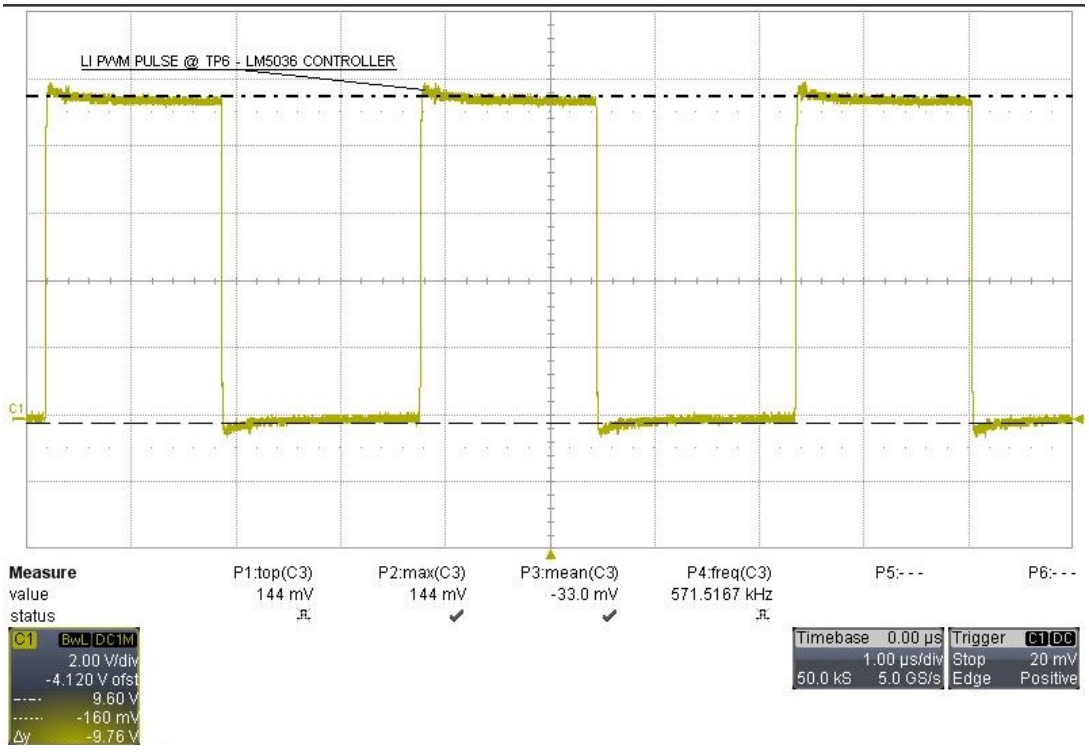

Figure 6.3: Measured LM5036 controller output - Half-bridge primary low-side MOSFET PWM gate pulse of 9.5 V

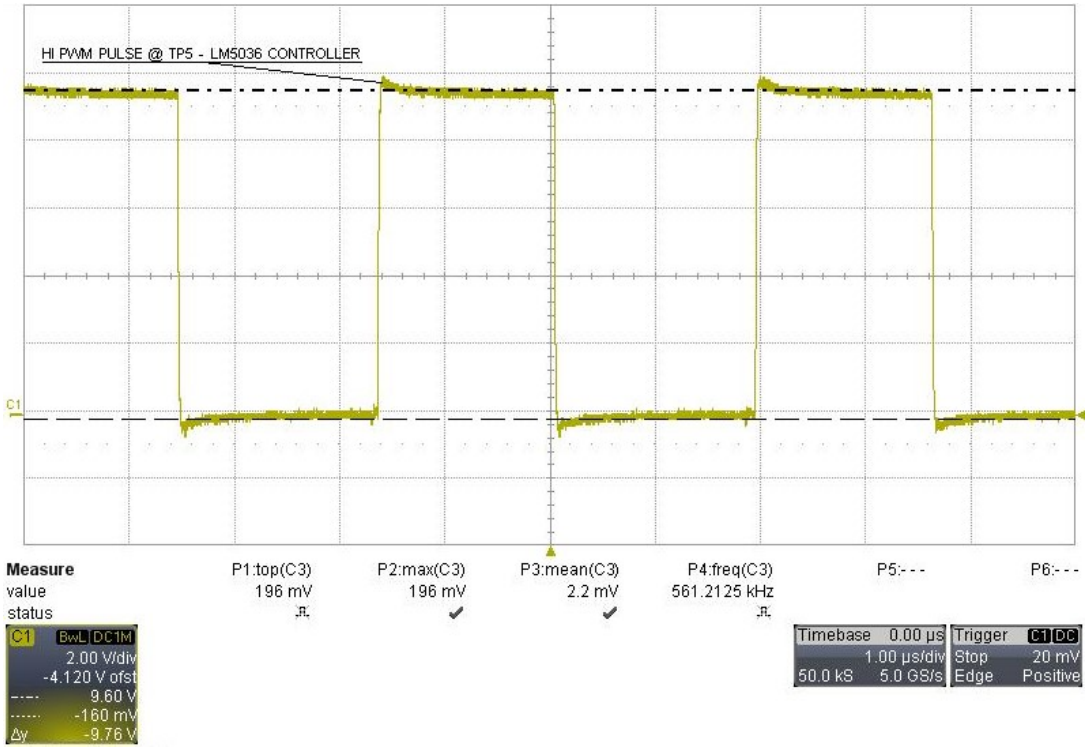

Figure 6.4: Measured LM5036 controller output - Half-bridge primary high-side MOSFET PWM gate pulse of 9.5 V

When the auxiliary supply of the controller operates in the synchronous mode without any internal faults, the sawtooth ramp signal and the gate pulses for both the primary and the secondary GAN MOSFETs are activated from the controller LM5036. Figure 6.5 shows the operational function block of the controller LM5036. As discussed in subsection 2.8.2, the controller LM5036 has an integrated gate driver for the primary MOSFETs with minimum gate to source voltage V_{GS} of 9.5 V. Here, the bias voltage is the source input for both the primary low-side and the primary high-side MOSFET gate pulse, as shown in figure 6.5. Figure 6.3 and 6.4 shows the primary low-side and primary high-side MOSFETs gate pulse of 9.5 V from the controller LM5036.

Similarly, the controller LM5036 has an integrated gate driver for the secondary MOSFETs with minimum gate to source voltage V_{GS} of 5 V. Here, the reference voltage V_{REF} is the source input for both the secondary synchronous MOSFETs gate pulse, as shown in figure 6.5. Figure 6.6 and 6.7 shows both secondary synchronous MOSFETs gate pulse of 5 V from the controller LM5036.

As discussed in subsection 2.8.2, the "GaN" MOSFETs have a threshold V_{GS} of 5 V. Thus, a dedicated external primary gate driver LMG1210 is used. Furthermore, an isolated gate driver, 2EDF7275K from Infineon Technologies AG, is used as a secondary side gate driver.

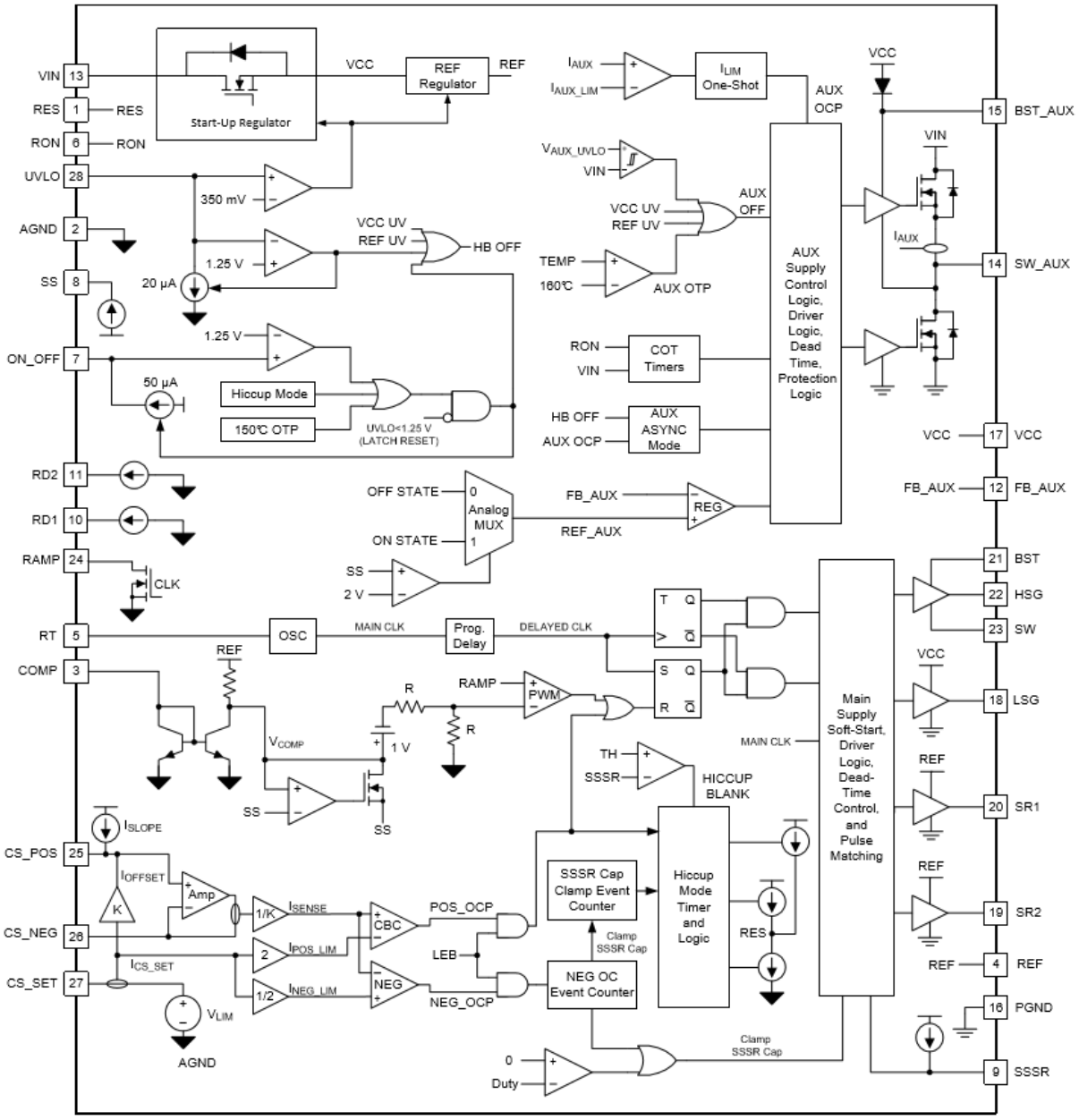

Figure 6.5: Functional block of the controller LM5036 [17]

Figure 6.8 and 6.9 show the primary low-side and primary high-side MOSFETs gate pulse of 5 V from the gate driver LMG1210. Similarly, figure 6.10 and 6.11 shows both secondary synchronous MOSFETs gate pulse of 5 V from the gate driver 2EDF7275K.

The operating temperature of the controller LM5036 plays a vital role in the synchronous operation of the controller's auxiliary supply. The controller operating above 150 °C leads to an asynchronous operation of the controller's auxiliary supply. The auxiliary current in the controller LM5036 is limited to 200 mA, exceeding the value leads to initiation of non-resettable off-timer [17], which provides additional protection for the circuit against the auxiliary over current.

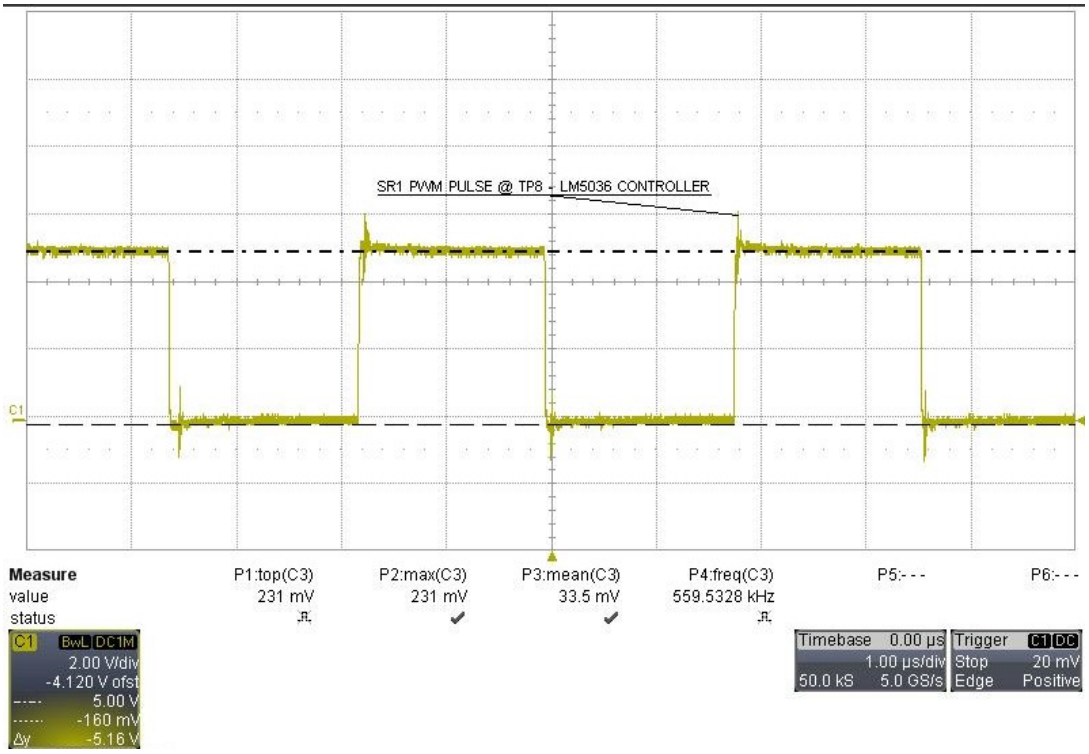

Figure 6.6: Measured LM5036 controller output - Half-bridge secondary synchronous MOSFETs SR_1 PWM gate pulse of 5 V

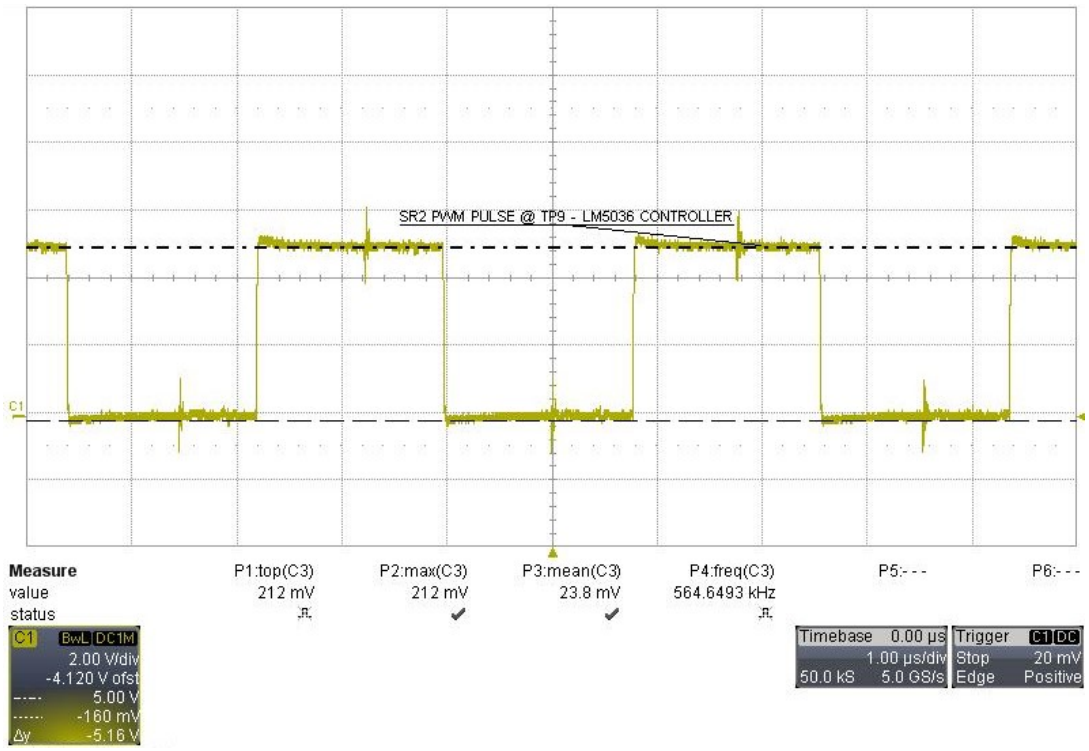

Figure 6.7: Measured LM5036 controller output - Half-bridge secondary synchronous MOSFETs SR_2 PWM gate pulse of 5 V

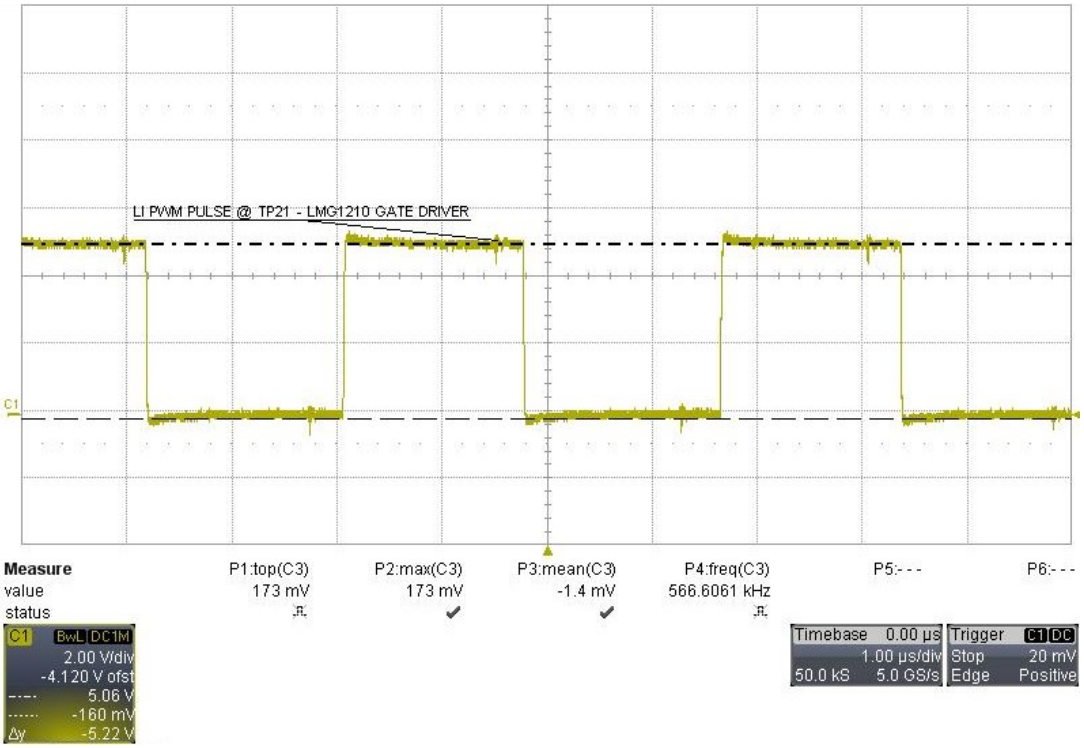

Figure 6.8: Measured LMG1210 gate driver output - Half-bridge primary low-side MOSFET PWM gate pulse of 5 V

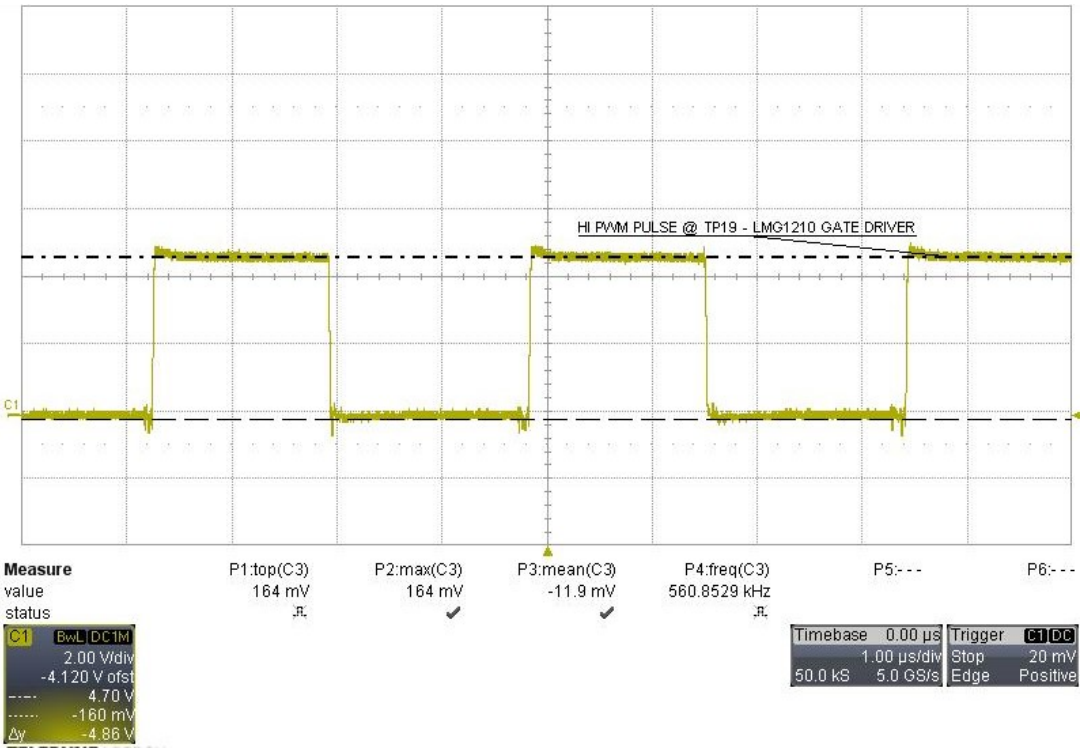

Figure 6.9: Measured LMG1210 gate driver output - Half-bridge primary high-side MOSFET PWM gate pulse of 5 V

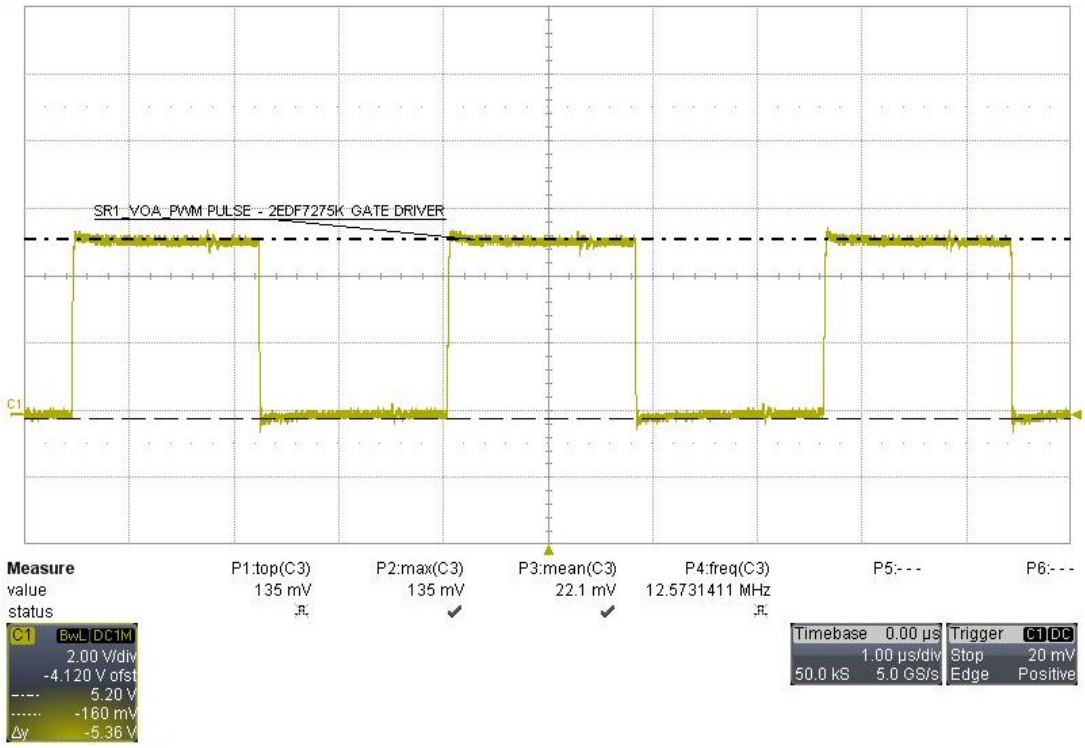

Figure 6.10: Measured 2EDF7275K gate driver output - Half-bridge secondary synchronous MOSFETs SR_1 PWM gate pulse of 5 V

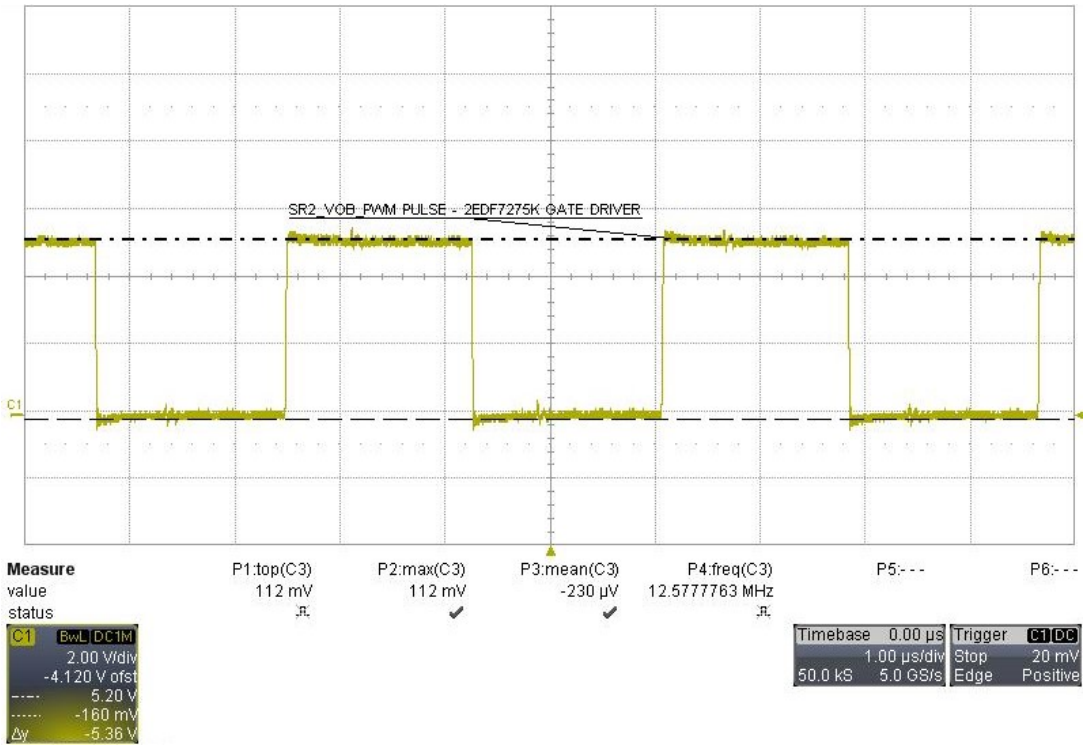

Figure 6.11: Measured 2EDF7275K gate driver output - Half-bridge secondary synchronous MOSFETs SR_2 PWM gate pulse of 5 V

6.2 Start-up of GaN MOSFET based half-bridge DC/DC converter

The controller LM5036 provides a fully-featured pre-biased start-up feature, which reduces the fluctuation in the output voltage [17]. The main requirement for the GaN MOSFET based half-bridge DC/DC converter is to have a regulated output voltage of 9 V. The pre-biased load condition is achieved by having pre-charged output capacitors before start-up [17].

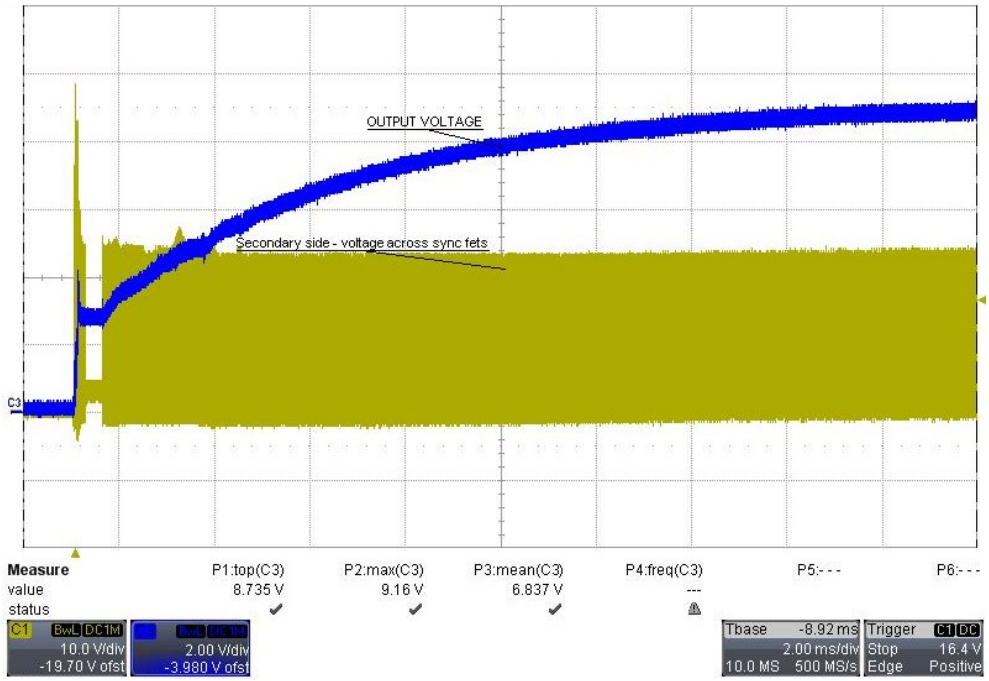

Figure 6.12: Measured pre-biased start-up of the GaN MOSFET based half-bridge DC/DC converter

Figure 6.12 shows the pre-biased start-up operation of the GaN MOSFET based half-bridge DC/DC converter. The start-up of the GaN MOSFET-based half-bridge DC/DC converter involves two different phases, namely the soft-start of the primary GaN MOSFETs and the soft-start of the synchronous GaN MOSFETs. The appropriate design values for the soft-start capacitor C_{SS}, and the synchronous soft-start capacitor C_{SSSR} provides hassle-free operation for the controller LM5036 [17].

During the initial start-up, if the soft-start voltage is below the threshold of 2.2 V, the primary auxiliary voltage and secondary auxiliary voltage produce an off-state voltage. The level of the off-state voltage initiates the reset circuit to discharge the output reference voltage [17].

During the synchronous mode operation of the auxiliary supply, the soft-start voltage increases above the threshold value of 2.2 V. Thus, the secondary auxiliary voltage reaches the on-state voltage of $V_{AUX2-ON}$, as shown in figure 6.13.

Furthermore, the reference capacitor soft-starts the output voltage V_o [17]. When the secondary side reference voltage exceeds the pre-bias voltage, the compensated current I_{COMP} starts to decrease. Thus, high power demand is created on the secondary side of the error amplifier. As a result, the synchronous soft-start capacitor C_{SSSR} starts to charge at the rate of 20 µA [17], which leads to a synchronous operation of the synchronous MOSFETs.

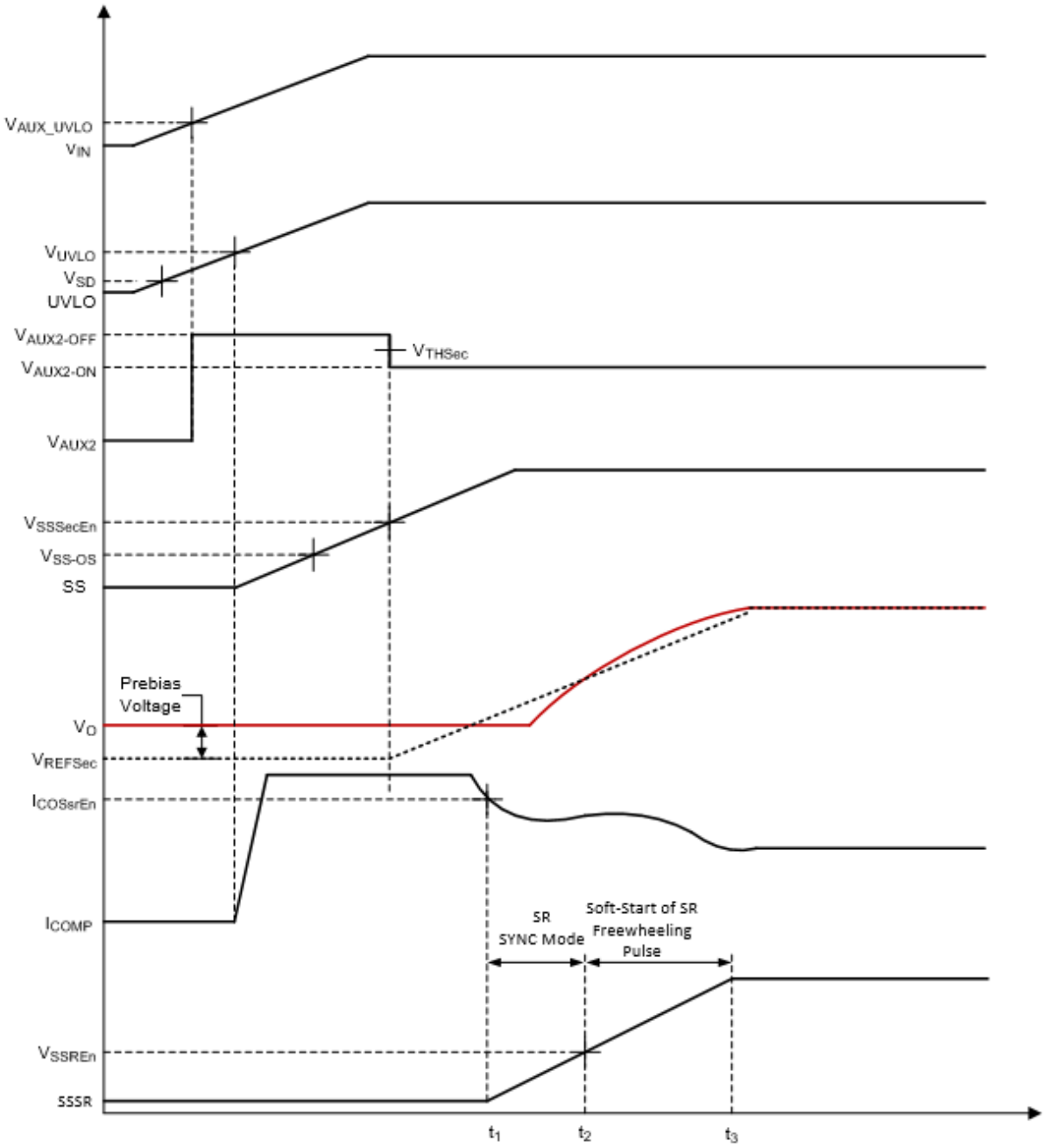

Figure 6.13: Pre-bias start-up in the controller LM5036 [17]

Figure 6.14 shows the voltage across the auxiliary supply switch node during steady state operation of the controller LM5036.

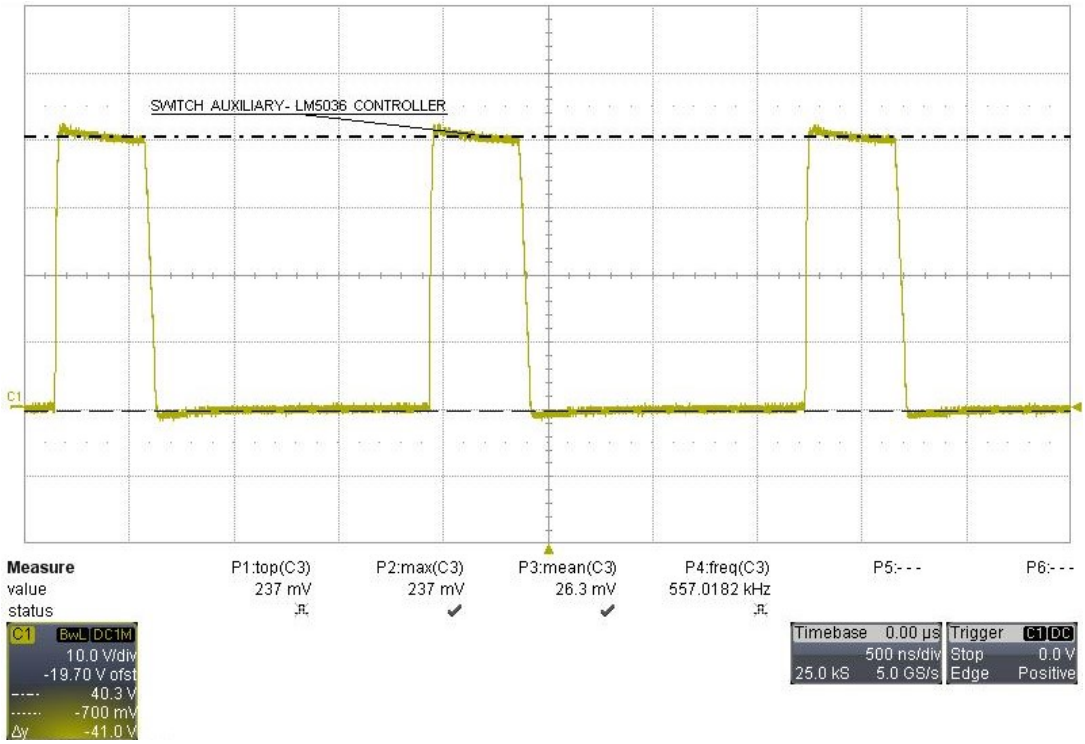

Figure 6.14: Measured voltage across the auxiliary supply switch node during steady state operation of controller LM5036

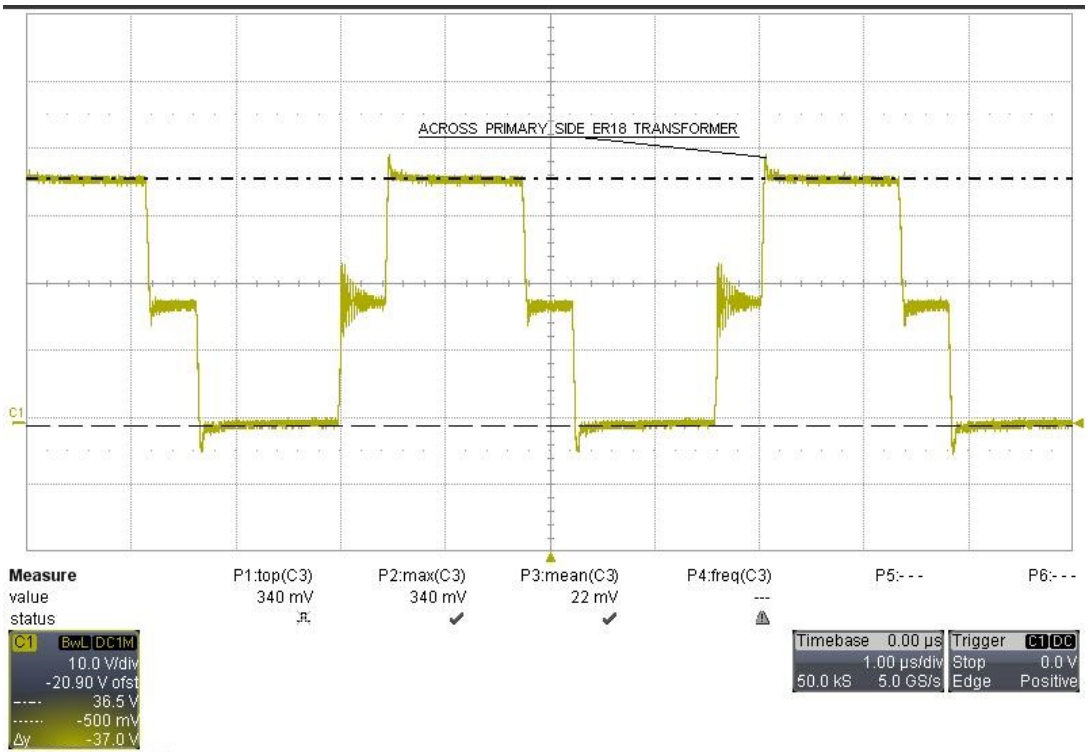

Figure 6.15: Measured voltage across the primary side of the transformer ER18 for the input voltage of 38 V

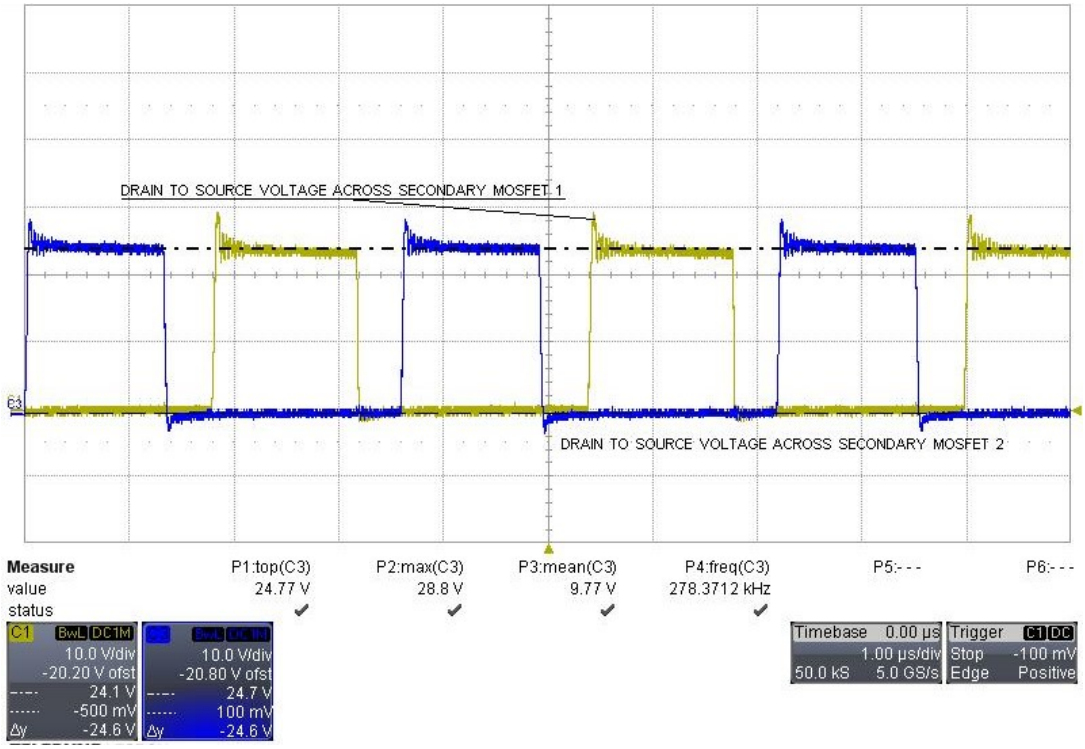

Figure 6.16: Measured voltage across the secondary side of the transformer ER18 for the input voltage of 38 V

Figure 6.15 and 6.16 shows the voltage across the primary side and the secondary side of the transformer ER18 for the input voltage of 38 V before introducing the passive snubber. The above voltage waveforms can be compared to the simulation voltage waveforms of the primary and the secondary sides of the transformer ER18, as discussed in subsection 4.1.3.

6.3 Design and implementation of passive snubber

During GaN MOSFET-based half-bridge DC/DC converter operation, the "GaN" MOSFETs experiences electrical stress in the absence of the snubbers. Figure 6.17 shows the blocking voltage V_{DS} across the synchronous MOSFET U_3 with ringing frequency f_{r_1} of 33.3 MHz.

As discussed in the subsection 4.1.2, initially a random capacitor of 10 nF is placed across the secondary transformer winding. Again, the blocking voltage V_{DS} across the synchronous MOSFET U_3 is measured with the reduction in the ringing frequency f_{r_2} of 13.3 MHz. Figure 6.18 shows the blocking voltage V_{DS} across the synchronous MOSFET U_3 with reduced ringing frequency f_{r_2} of 13.3 MHz after introduction of 10 nF. Now, the ringing frequency f_{r_2} is reduced from 33.3 MHz to 13.3 MHz, which is approximately a 60% reduction in the ringing frequency.

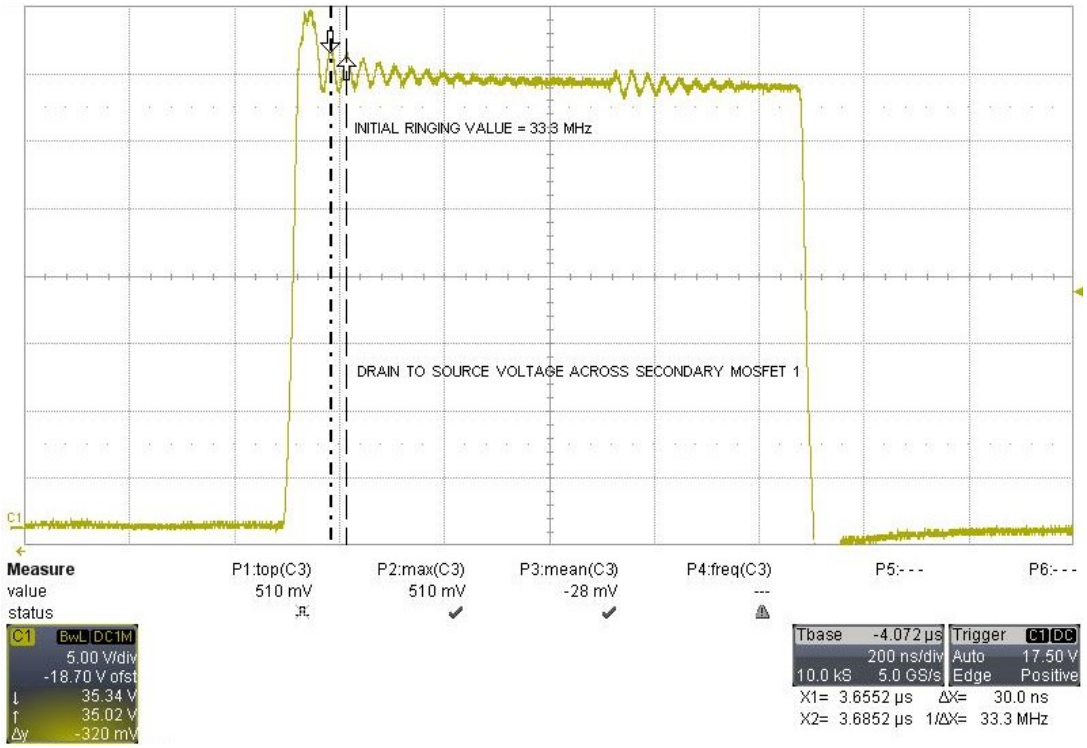

Figure 6.17: Measured blocking voltage V_{DS} across the synchronous MOSFET U_3 with ringing frequency f_{r_1} of 33.3 MHz

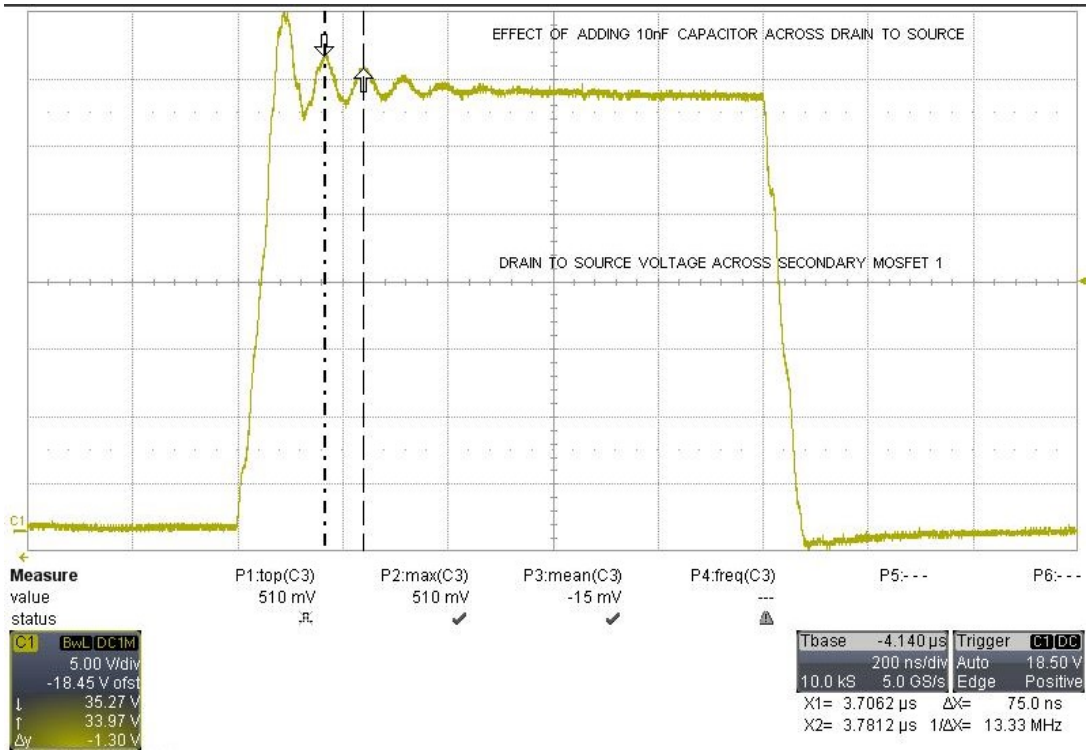

Figure 6.18: Measured blocking voltage V_{DS} across the synchronous MOSFET U_3 with reduced ringing frequency f_{r_2} of 13.3 MHz after introduction of 10 nF

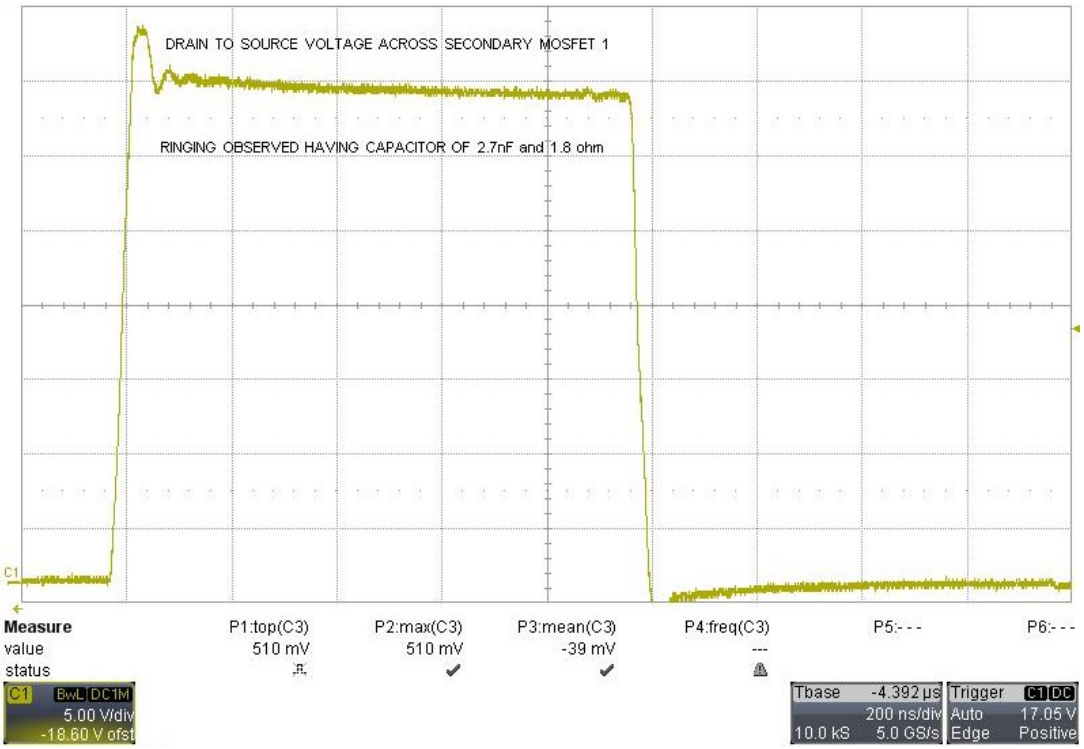

Figure 6.19: Measured reduction in the voltage ripple V_{DS} across the synchronous MOSFET U_3 after insertion of passive snubbers

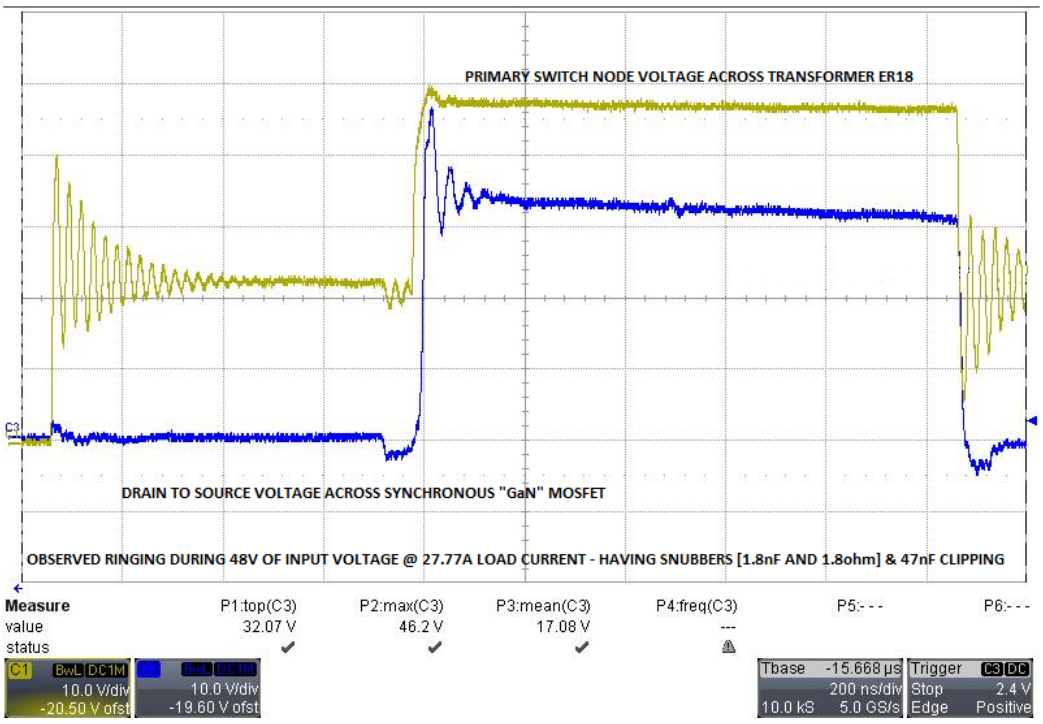

Figure 6.20: Measured voltage ripple V_{DS} across the synchronous MOSFET U_3 at 48 V of input voltage, 27.8 A of load current after insertion of 1.8 nF of snubber capacitance and 1.8 Ω of snubber resistance.

Thus, the snubber capacitor C_{snub} and snubber resistor R_{snub} are calculated using (2.38) and (2.39). Furthermore, a snubber capacitance of 2.7 nF and snubber resistance of 1.8 Ω are placed across the secondary winding of the planar ER18 transformer and its implemented in the hardware design of GaN MOSFET based half-bridge DC/DC converter. Figure 6.19 shows the reduction in the voltage ripple V_{DS} across the synchronous MOSFET U_3 after the insertion of RC passive snubbers.

In the view of improving the overall efficiency of the GaN MOSFET based half-bridge DC/DC converter, the losses across the passive RC snubber play a predominant role. Using (2.60), the losses across the snubbers are calculated. On the other hand, reducing the passive RC snubber values leads to high voltage ripple across the synchronous MOSFETs. In this thesis, a snubber capacitance of 1.8 nF and snubber resistance of 1.8 Ω are placed across the secondary winding of the planar ER18 transformer and implemented in the hardware design of the GaN MOSFET based half-bridge DC/DC converter to enhance the overall efficiency. Figure 6.20 shows the voltage ripple V_{DS} across the synchronous MOSFET U_3 at 48 V of input voltage and load current of 27.8 A.

6.4 Operating thermal characteristics

The operating temperature plays a vital role in the operation of the GaN MOSFET based half-bridge DC/DC converter. The reduction in the overall size of the module increases the overall operating temperature of the GaN MOSFET based half-bridge DC/DC converter. Figure 6.21 shows the measured operating temperature for various components under different load currents without external cooling.

TEMPERATURE - DEGREE CELSIUS	LOAD CURRENT [I_o] IN AMPS						
COMPONENTS	I_o = 0A	I_o = 2A	I_o = 4A	I_o = 6A	I_o = 8A	I_o = 10A	I_o = 12A
PLANAR TRANSFORMER ER18	62.8°C	66.5°C	71.1°C	81.1°C	89.1°C	99.6°C	108°C
CONTROLLER LM5036	51.2°C	53.1°C	55.6°C	61.8°C	66.8°C	72.4°C	77.6°C
AUXILIARY TRANSFORMER	59.6°C	60.5°C	63.3°C	68.8°C	74.5°C	79.7°C	85°C
PRIMARY GATE DRIVER LMG1210	44°C	46.1°C	49.6°C	56.9°C	62.4°C	68.8°C	75.2°C
2EDF7275K GATE DRIVER	50.8°C	53.2°C	57.8°C	68.8°C	73.8°C	83.2°C	86°C
PRIMARY "GaN" MOSFETS	43.7°C	45.6°C	49.4°C	58.4°C	64.9°C	72.3°C	79.9°C
SECONDARY "GaN" MOSFETS	49.5°C	52.7°C	57.3°C	69.4°C	78.6°C	88.3°C	97.1°C

Figure 6.21: Measured operating temperature for various components under different load currents without external cooling

As the load current increases, the temperature across each component increases. During the no-load condition, the maximum temperature of 63 °C is observed during the operation of the planar ER18 transformer. Similarly, at 43% load condition, the maximum temperature of 108 °C is observed across the planar ER18 transformer, as shown in figure 6.21. As the operating temperature increases, the overall performance of the component decreases. Furthermore, the higher temperature are observed across the secondary "GaN" MOSFETs. The GaN MOSFET based

half-bridge DC/DC converter operating beyond 120 °C requires an external cooling system.

TEMPERATURE - DEGREE CELSIUS	LOAD CURRENT [I_O] IN AMPS						
COMPONENTS	I_O = 0A	I_O = 1A	I_O = 4A	I_O = 12A	I_O = 20A	I_O = 24A	I_O = 28A
PLANAR TRANSFORMER ER18	33.6°C	34.1°C	34.4°C	37.5°C	47.5°C	58.1°C	69°C
CONTROLLER LM5036	30.2°C	31.2°C	31.7°C	33°C	35°C	37.2°C	39°C
AUXILIARY TRANSFORMER	35°C	35.2°C	36°C	36.6°C	38.2°C	39.2°C	40.4°C
PRIMARY GATE DRIVER LMG1210	27.2°C	28°C	29.2°C	32°C	34.1°C	38°C	41.9°C
2EDF7275K GATE DRIVER	30.4°C	31.6°C	31.8°C	33.6°C	40.1°C	44.1°C	45.5°C
PRIMARY "GaN" MOSFETS	25°C	26.3°C	28.6°C	34.5°C	44.8°C	54.3°C	63.5°C
SECONDARY "GaN" MOSFETS	28°C	29.3°C	32.3°C	40.6°C	55.8°C	65.9°C	73.4°C

Figure 6.22: Measured operating temperature for various components under different load currents with external cooling

Figure 6.22 shows the measured operating temperature for various components under different load currents with external cooling. During the no-load condition, a maximum temperature of 33.5 °C is observed during the operation of the planar ER18 transformer. Similarly, with external cooling at 100% load condition, the maximum temperature of 73.5 °C is observed across the secondary "GaN" MOSFETs, as shown in figure 6.22. Thus, by having an external cooling for the GaN MOSFET based half-bridge DC/DC converter, the overall operating temperature is limited.

6.5 Operating deadtime characteristics

As discussed in subsection 2.11.1, the reverse conduction of the GaN MOSFET predominantly affects the overall efficiency of the GaN MOSFET based half-bridge DC/DC converter. The absence of a body diode in the "GaN" MOSFET eliminates the reverse recovery losses.

In the controller LM5036, the delay resistors RD_1 and RD_2 play a vital role in adjusting the deadtime for the operation of the synchronous "GaN" MOSFETs. The internal oscillator in the controller LM5036 generates a clock pulse having a pulse width of 65 ns. But, the limitation in the controller LM5036 restricts such that the values of the delay resistors RD_1 and RD_2 should not be selected below 5 kΩ [17]. Furthermore, considering the minimum value of 5 kΩ for the delay resistors RD_1 and RD_2 would lead to higher deadtime losses during the operation of the GaN MOSFET based half-bridge DC/DC converter.

Figure 6.23 and 6.24 show the measured deadtime during the leading edge and the trailing edge of the drain to source voltage V_{DS} across the synchronous MOSFET U_3. Using the controller LM5036, a deadtime of 64 ns is observed on the leading edge and a deadtime of 77 ns is observed on the falling edge of the drain to source voltage V_{DS} across synchronous MOSFET U_3 during the full-load output current of 27.8 A. Using (2.57), the total deadtime loss of 3.6 W is observed across the leading

edge and the trailing edge of the drain to source voltage V_{DS} of the synchronous MOSFETs. The detailed calculation of deadtime is explained in Appendix D.1.

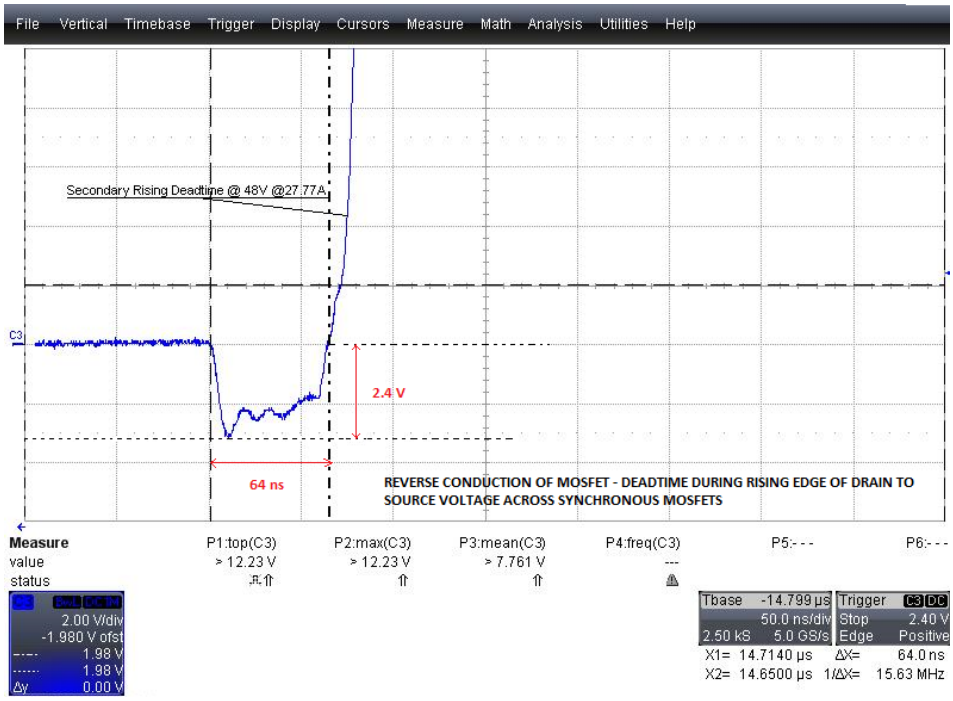

Figure 6.23: Measured deadtime during the leading edge of the drain to source voltage V_{DS} across synchronous MOSFET U_3

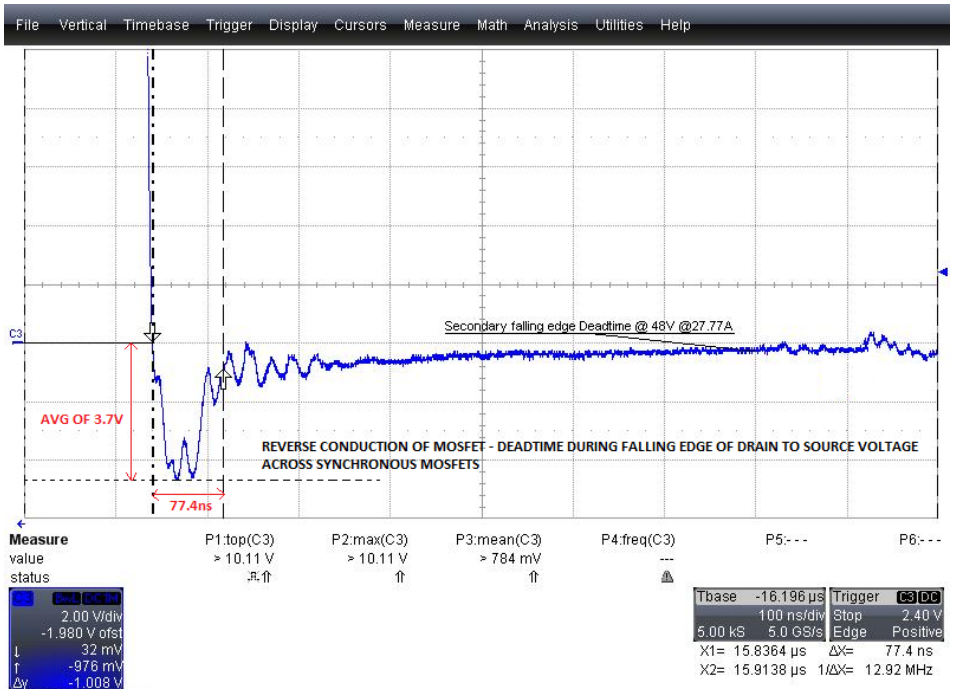

Figure 6.24: Measured deadtime during the trailing edge of the drain to source voltage V_{DS} across synchronous MOSFET U_3

7

Results and Discussions

In this section, the hardware testing results for both the benchmarked Si MOSFET based half-bridge DC/DC converter and newly designed GaN MOSFET based half-bridge DC/DC converter are discussed. Furthermore, the results are compared and analyzed concerning thesis objectives.

7.1 Hardware test results of benchmarked Ericsson developed Si MOSFET based half-bridge DC/DC converter

The benchmarked Ericsson developed Si MOSFET based half-bridge DC/DC converter is operated at 280 kHz. For different input voltages, the performance of the Si MOSFET based DC/DC converter is evaluated by applying different load currents.

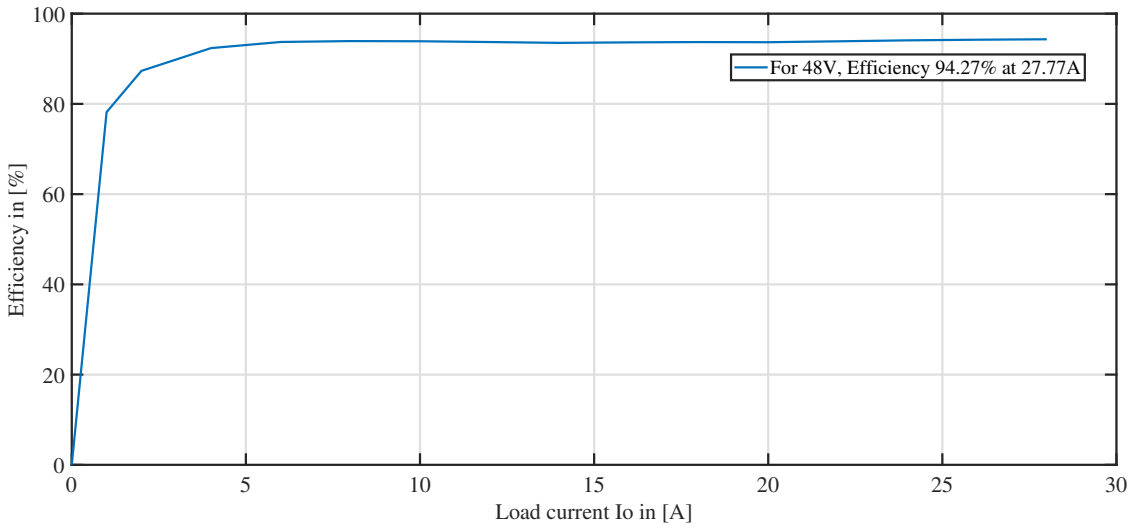

Figure 7.1: Measured efficiency of the benchmarked Si MOSFET based half-bridge DC/DC converter operating at 48 V input voltage with different load currents.

The deadtime adjustment for the MOSFETs plays a vital importance in the performance evaluation of the converter. With lower deadtime, the efficiency performance of the converter is enhanced. However, reducing the deadtime leads to cross conduction of the MOSFETs, which affects the thermal constraints of the converter. On the other hand, an increase in deadtime leads to less operating efficiency. Thus,

an optimum deadtime of 105 ns is considered for the performance evaluation of the Si MOSFET based half-bridge DC/DC converter. The converter efficiency of 94.3% operating at 48 V input voltage at 27.8 A is observed as shown in figure 7.1.

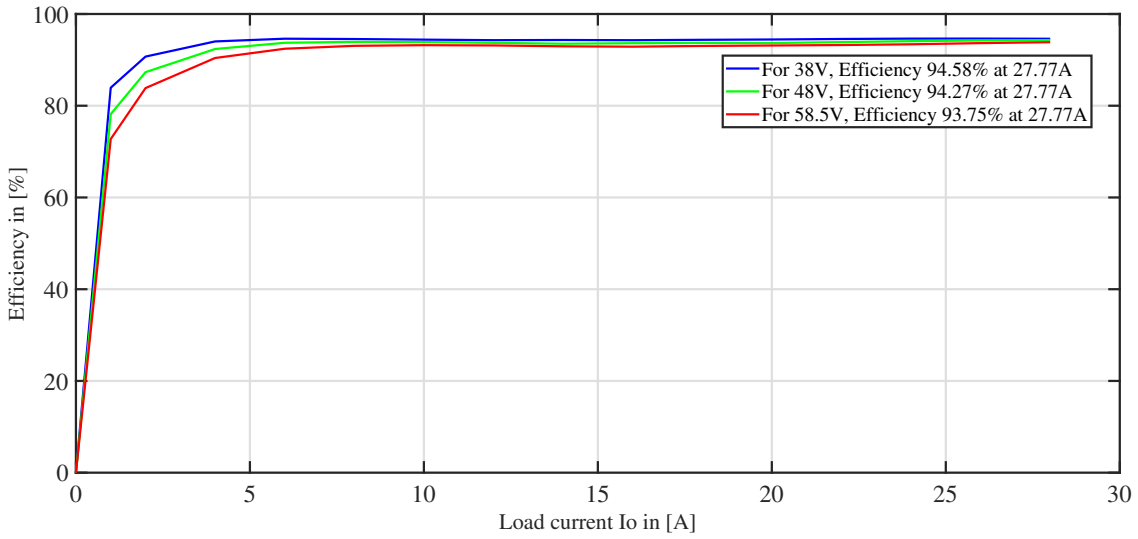

Figure 7.2: Measured efficiency comparison of the benchmarked Si MOSFET based half-bridge DC/DC converter operating at different input voltages with various load steps.

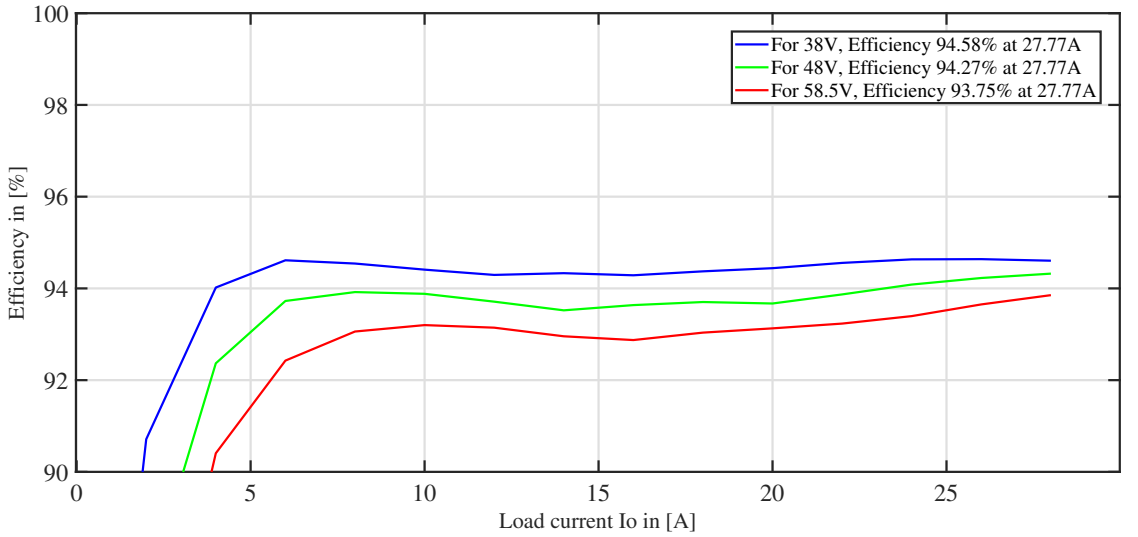

Figure 7.3: Zoom figure of the measured efficiency comparison of the benchmarked Si MOSFET based half-bridge DC/DC converter operating at different input voltages with various load steps.

Similarly, the maximum converter efficiency of 94.6% is observed by operating at an input voltage of 38 V. Figure 7.2 and 7.3 shows the efficiency comparison of the benchmarked Si MOSFET based half-bridge DC/DC converter operating at different input voltages with various load steps.

7.2 Hardware test results of the GaN MOSFET based half-bridge DC/DC converter

The GaN MOSFET based half-bridge DC/DC converter is operated at 600 kHz. Furthermore, the losses across the passive snubbers play a vital role in obtaining the overall performance of the GaN MOSFET based half-bridge DC/DC converter. The overall efficiency of the GaN MOSFET based half-bridge DC/DC converter is analyzed by considering the different input voltages for various load conditions.

7.2.1 With snubber capacitance of 2.7 nF and snubber resistance of 1.8 Ω

Figure 7.4 shows the measured efficiency comparison of the newly designed GaN MOSFET based half-bridge DC/DC converter with snubber capacitance of 2.7 nF and snubber resistance of 1.8 Ω operating at different input voltages with various load steps. An efficiency of 93.3% is observed for the converter operating at 38 V input voltage and load current of 15 A. Due to high on-state resistance R_{ds-on} in the synchronous "GaN" MOSFETs, the GaN MOSFET based half-bridge DC/DC converter operating at a full load current of 27.8 A experience a reduction in overall efficiency.

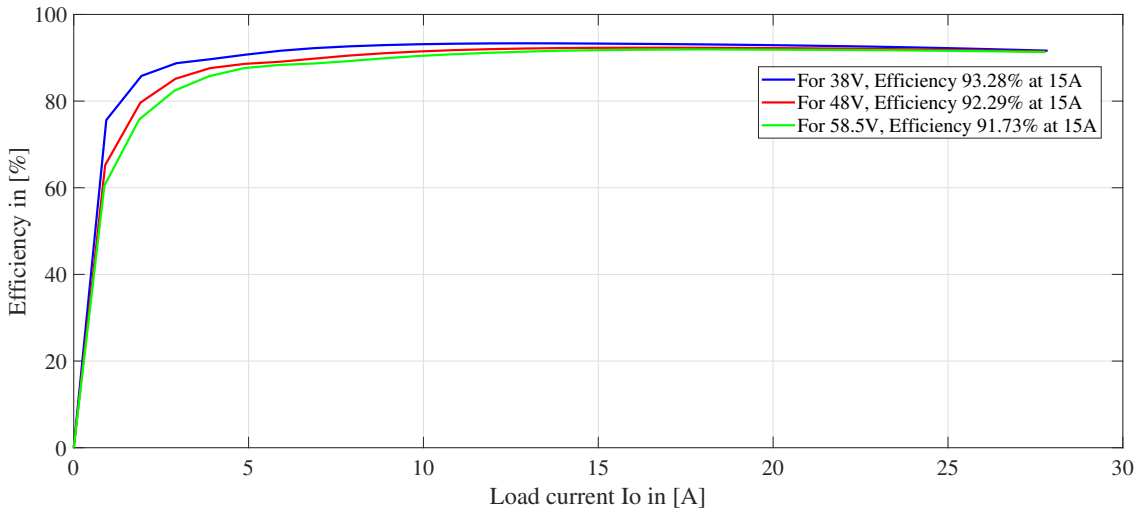

Figure 7.4: Measured efficiency comparison of the newly designed GaN MOSFET based half-bridge DC/DC converter with snubber capacitance of 2.7 nF and snubber resistance of 1.8 Ω operating at different input voltages with various load steps.

The snubber capacitance of 2.7 nF and snubber resistance of 1.8 Ω across the secondary winding induces the snubber loss of 1.4 W for each snubber, which reduces the overall efficiency. Figure 7.5 shows a zoomed figure of the measured efficiency comparison of the newly designed GaN MOSFET based half-bridge DC/DC converter with snubber capacitance of 2.7 nF and snubber resistance of 1.8 Ω operating at different input voltages with various load steps.

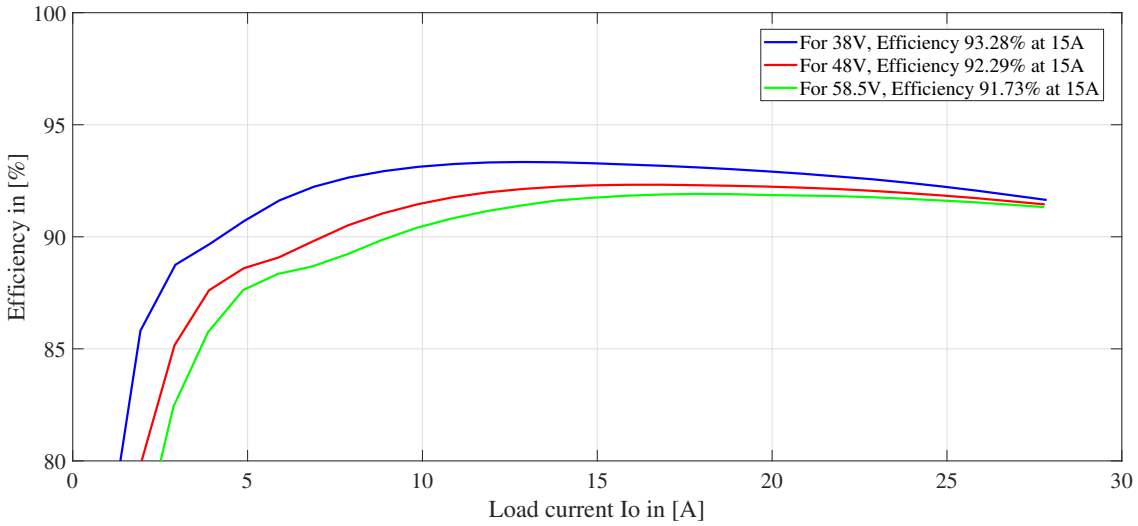

Figure 7.5: Zoom figure of the measured efficiency comparison of the newly designed GaN MOSFET based half-bridge DC/DC converter with snubber capacitance of 2.7 nF and snubber resistance of 1.8 Ω operating at different input voltages with various load steps.

7.2.2 With snubber capacitance of 1.8 nF and snubber resistance of 1.8 Ω

Figure 7.6 shows the measured efficiency comparison of the newly designed GaN MOSFET based half-bridge DC/DC converter with snubber capacitance of 1.8 nF and snubber resistance of 1.8 Ω operating at different input voltages with various load steps. The efficiency of 93.6% is observed for the converter operating at 38 V input voltage and load current of 15 A.

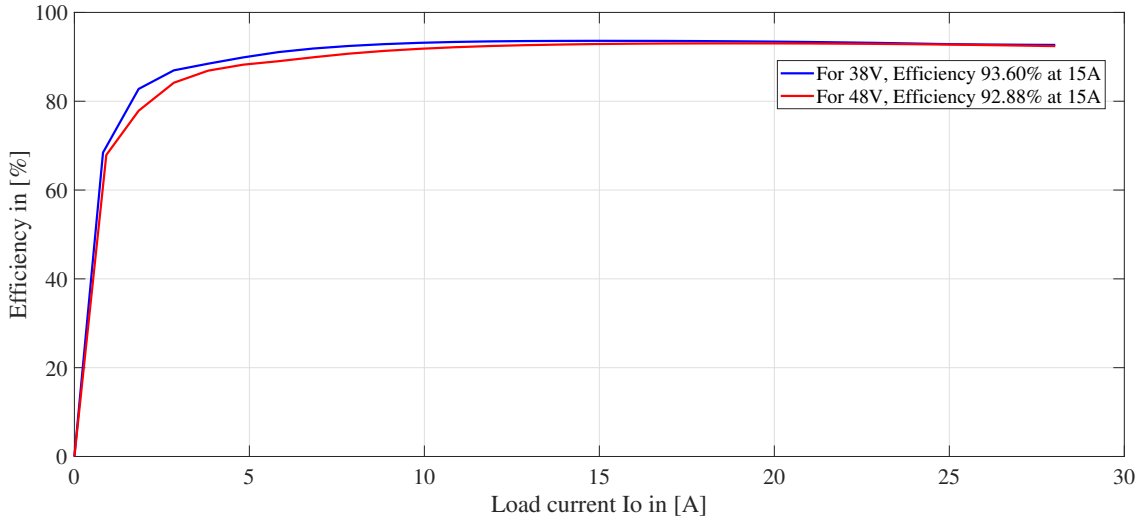

Figure 7.6: Measured efficiency comparison of the newly designed GaN MOSFET based half-bridge DC/DC converter with snubber capacitance of 1.8 nF and snubber resistance of 1.8 Ω operating at different input voltages with various load steps.

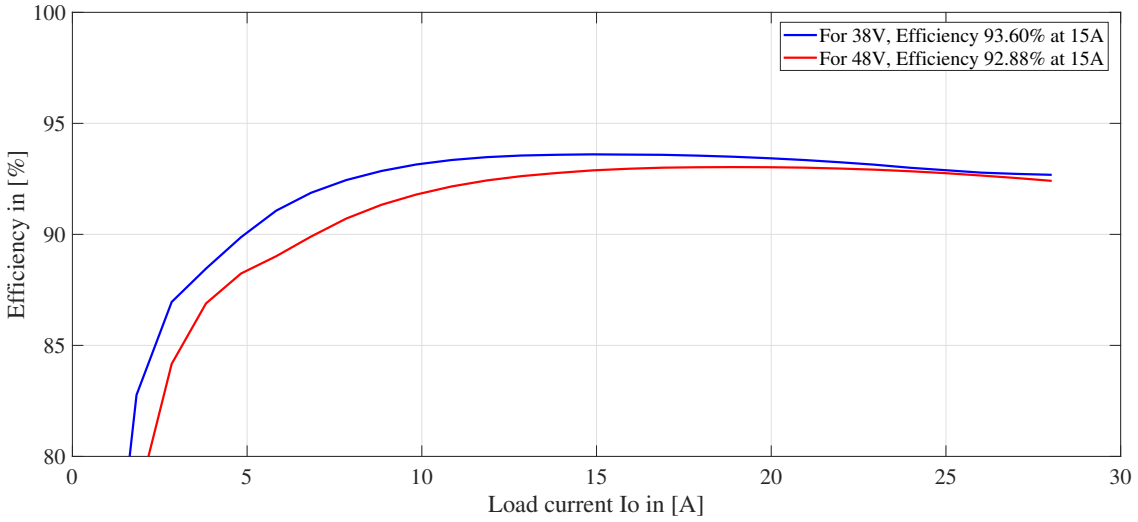

Figure 7.7: Zoom figure of the measured efficiency comparison of the newly designed GaN MOSFET based half-bridge DC/DC converter with snubber capacitance of 1.8 nF and snubber resistance of 1.8 Ω operating at different input voltages with various load steps.

The reduction in efficiency of the GaN MOSFET based half-bridge DC/DC converter operating at a full load current of 27.8 A is observed due to high on-state resistance R_{ds-on} in the synchronous "GaN" MOSFETs. The snubber capacitance of 1.8 nF and snubber resistance of 1.8 Ω across the secondary winding induces snubber loss of 1.2 W for each snubber. The reduction in the snubber value enhances the overall efficiency of the GaN MOSFET based half-bridge DC/DC converter from 93.3% to 93.6%. Figure 7.7 shows a zoomed figure of the measured efficiency comparison of the newly designed GaN MOSFET based half-bridge DC/DC converter with the snubber capacitance of 1.8 nF and snubber resistance of 1.8 Ω operating at different input voltages with various load steps.

7.3 Comparison

In this section, module size and efficiency comparison of the Si MOSFET based DC/DC converter and newly designed GaN MOSFET based half-bridge DC/DC converter are discussed.

7.3.1 Module size

The main objective of this thesis is to have a reduction in the overall module size of the GaN MOSFET based DC/DC converter in comparison with the Si MOSFET based DC/DC converter. The focus of this thesis is to reduce the area of the main power-train. The area of the power-train includes the ceramic input capacitors, primary side MOSFETS, planar ER18 transformer, secondary-side MOSFETs, output inductor, and ceramic output capacitors. The benchmarked Ericsson developed Si MOSFET based DC/DC converter has a power-train of length 7.5 cm and width of 3 cm.

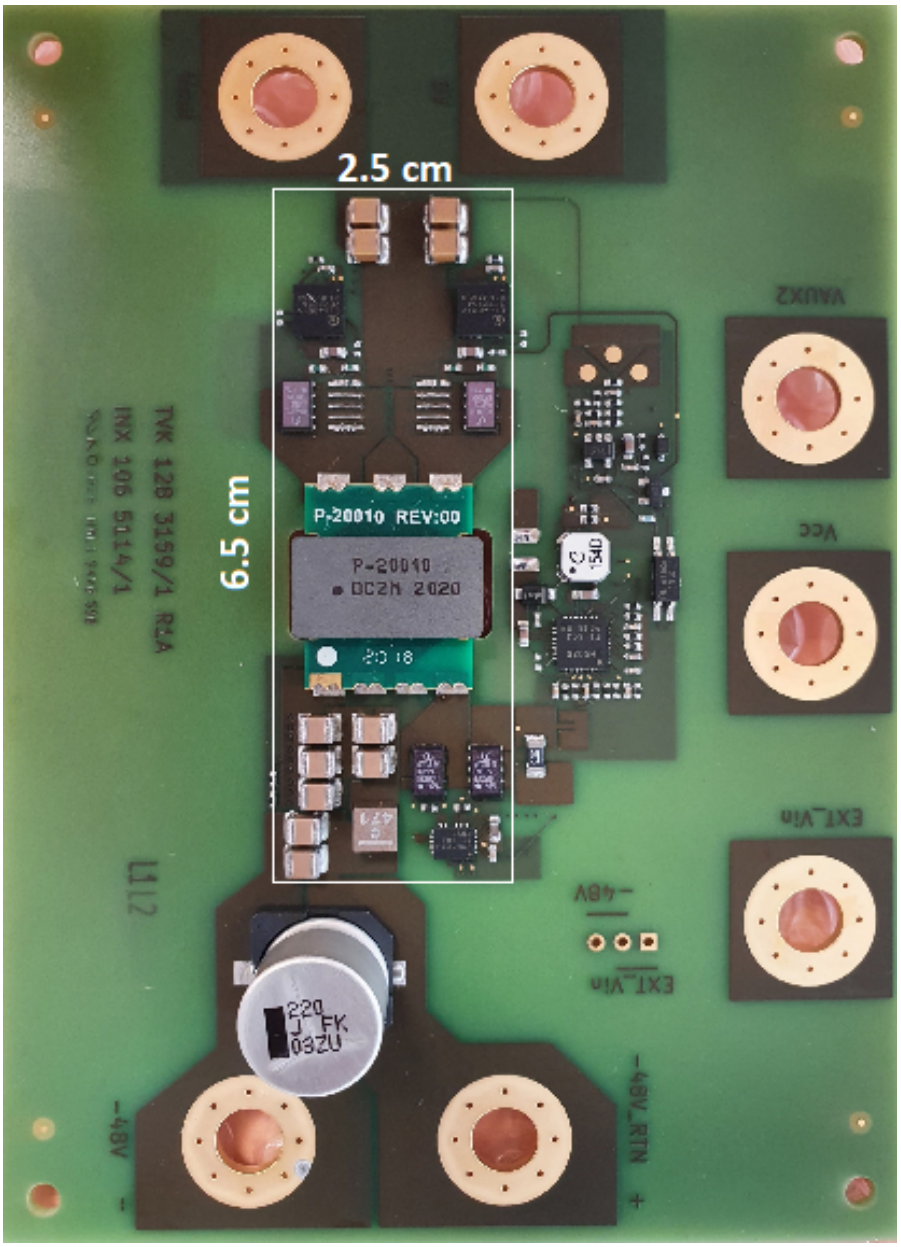

Figure 7.8: Measured power-train area in the newly designed GaN MOSFET based half-bridge DC/DC converter

The total power-train area of 22.5 cm^2 is measured in the benchmarked Ericsson developed Si MOSFET based DC/DC converter. In this thesis, the newly designed planar ER18 transformer has nearly about 40% reduction in core area compared planar ER23 transformer, which is used in benchmarked Ericsson developed Si MOSFET based DC/DC converter. The GaN MOSFET based half-bridge DC/DC converter has a power-train of length 6.5 cm and width of 2.5 cm, as shown in figure 7.8. The total power-train area of 16.25 cm^2 is measured in the newly designed GaN MOSFET based half-bridge DC/DC converter. Thus, about 27.8% reduction in power-train area is observed in the newly designed GaN MOSFET based half-bridge DC/DC converter in comparison with the benchmarked Ericsson developed Si MOSFET based DC/DC converter.

7.3.2 Efficiency

In this thesis, one of the main objectives is to have similar or better operating efficiency of a newly designed GaN MOSFET based half-bridge DC/DC converter in comparison with the benchmarked Ericsson developed Si MOSFET based DC/DC converter. As discussed in section 7.2, the GaN MOSFET based half-bridge DC/DC converter have an efficiency of 93.6% with a snubber capacitance of 1.8 nF and snubber resistance of 1.8 Ω operating at an input voltage of 38 V. Generally, the converter operating with a higher switching frequency experiences higher voltage spikes across the secondary windings of the transformer during the initial start-up.

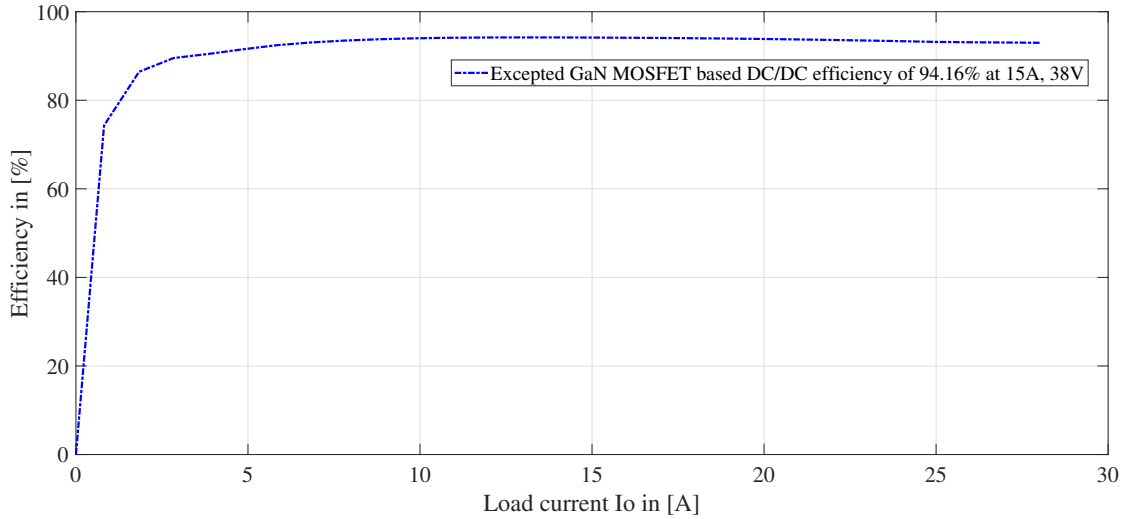

Figure 7.9: Expected enhanced efficiency of the GaN MOSFET based half-bridge DC/DC converter with elimination clipping circuit losses at 38 V for different load currents.

In this thesis, the clipping circuit is designed across the secondary windings of the planar ER18 transformer for the safe operation of the synchronous GaN MOSFETs. The pair of clipping circuit provides power dissipation of 0.9 W across the secondary windings of the planar ER18 transformer. Thus, by neglecting the clipping circuit losses, the overall efficiency of the GaN MOSFET based half-bridge DC/DC converter is enhanced. Figure 7.9 shows the expected enhanced efficiency of the GaN MOSFET based half-bridge DC/DC converter with the elimination of the clipping circuit losses at 38 V for different load currents. The overall efficiency of 94.2% is expected by neglecting clipping circuit losses in the GaN MOSFET based half-bridge DC/DC converter.

Figure 7.10 shows the measured efficiency comparison between the benchmarked Ericsson developed Si MOSFET based DC/DC converter and newly designed GaN MOSFET based half-bridge DC/DC converter for the input voltage 38 V and different load conditions. From figure 7.10, a dip in the efficiency at lower load currents due to high switching losses is observed for the newly designed GaN MOSFET based half-bridge DC/DC converter. A maximum efficiency of 94.2% is expected in the newly designed GaN MOSFET based half-bridge DC/DC converter, which is al-

most similar to the benchmarked Ericsson developed Si MOSFET based DC/DC converter efficiency of 94.6%. Figure 7.11 shows the zoomed figure of the measured efficiency comparison between the benchmarked Ericsson developed Si MOSFET based DC/DC converter and newly designed GaN MOSFET based half-bridge DC/DC converter for the input voltage 38 V and different load conditions.

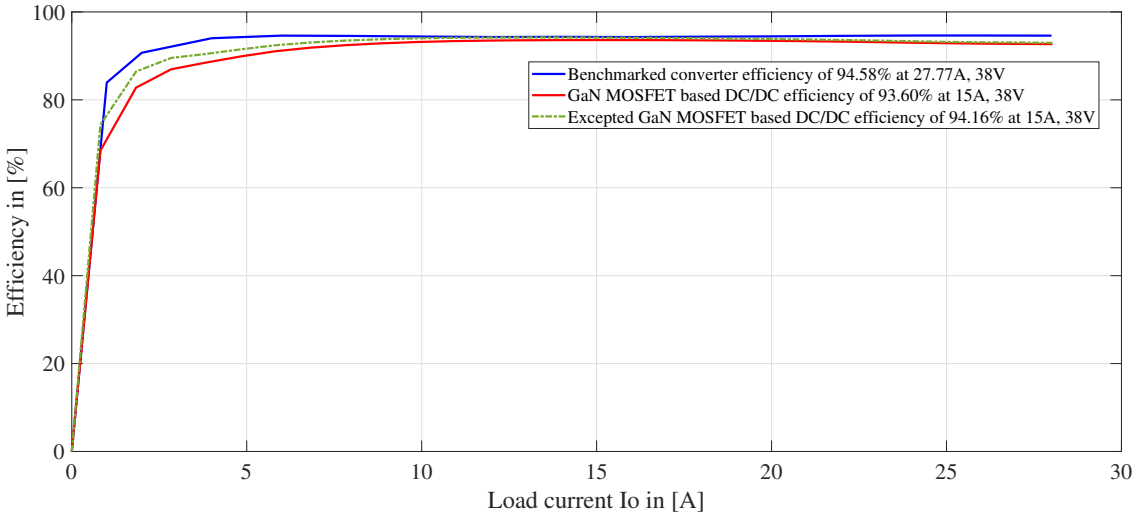

Figure 7.10: Measured efficiency comparison between the benchmarked Ericsson developed Si MOSFET based DC/DC converter and newly designed GaN MOSFET based half-bridge DC/DC converter for the input voltage 38 V and different load conditions.

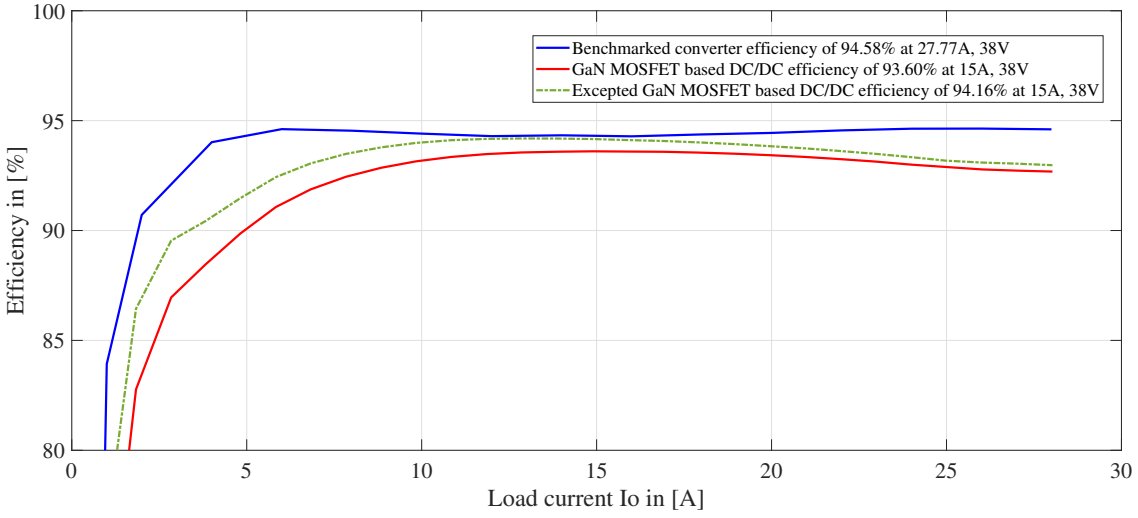

Figure 7.11: Zoom figure of the measured efficiency comparison between the benchmarked Ericsson developed Si MOSFET based DC/DC converter and newly designed GaN MOSFET based half-bridge DC/DC converter for the input voltage 38 V and different load conditions.

8

Conclusion

In this thesis, an isolated GaN MOSFET based half-bridge DC/DC converter is simulated, designed, and verified using hardware testing. Firstly, the benchmarked Ericsson developed Si MOSFET based DC/DC converter is analyzed. In the view of reducing the overall module of the converter, the GaN MOSFET based half-bridge DC/DC converter with a high switching frequency of 600 kHz is designed. For higher switching frequency, the planar ER18 transformer is designed with a 40% reduction in the core area in comparison with the earlier developed planar ER23 transformer. The overall simulation efficiency of 94% is achieved for GaN MOSFET based half-bridge DC/DC converter operating at an input voltage of 48 V under different load conditions.

The designed GaN MOSFET based half-bridge DC/DC converter has a power-train area of 16.25 cm^2, which is about 27.8% reduction in power-train area in comparison with benchmarked Ericsson developed Si MOSFET based DC/DC converter. The overall measured efficiency of 94.6% is observed for the benchmarked Ericsson developed Si MOSFET based DC/DC converter. Furthermore, the hardware testing of the GaN MOSFET half-bridge DC/DC converter prevails the overall efficiency of 93.6%. The enhanced efficiency of 94.2% is expected for the GaN MOSFET based half-bridge DC/DC converter, excluding clipping losses. Thus, a similar efficiency is observed with the GaN MOSFET half-bridge DC/DC converter in comparison with the benchmarked Ericsson developed Si MOSFET based DC/DC converter.

8.1 Future work

In this thesis, the design and development of a hard switching GaN MOSFET based half-bridge DC/DC converter with a reduction in module size is analyzed. The complete robustness test on the designed GaN MOSFET based half-bridge DC/DC converter requires further technical analysis, improvements, and necessary time frame. However, due to time constraint, the thesis focuses only on the reduction in module size and efficiency comparison with benchmarked Ericsson developed Si MOSFET based DC/DC converter.

There are possible improvements which can enhance the overall performance of the GaN MOSFET based half-bridge DC/DC converter. The losses due to a passive snubber can be minimized by implementing the active snubber. Furthermore, a suitable controller with the least deadtime can be implemented to reduce the deadtime

losses in the GaN MOSFET based half-bridge DC/DC converter. The controller with inbuilt gate drivers that provide appropriate gate pulses for GaN MOSFETs can eliminate the utilization of external gate drivers. For a detailed analysis of the GaN MOSFET based half-bridge DC/DC converter, a stable advanced feedback loop is necessary. As discussed in section 6.4, the implementation of a heat sink for GaN MOSFETs and a better cooling system would enhance the overall performance of the converter.

8.2 Ethical Aspects

The ethical aspects help in finding right and wrong in the conduct of a professional project, and this is made based on the IEEE codes of ethics [35]. There is three IEEE code of ethics which were important in our thesis, and they are illustrated below.

"To be honest and realistic in stating claims or estimate based on available data". As the GaN MOSFET based converters are not fully exploited, it is of importance to present with the exact data obtained from the simulation and measurement results, so, it would be helpful for future projects.

"To improve the understanding of technology, its appropriate applications and potential consequences". In this thesis, understanding the behaviour of new GaN MOSFET based material was the key which also helped to carefully design the converter for an appropriate application.

"To avoid injuring others, their property, reputation, or employment by false or malicious action". It is important to illustrate on what has been done and not to the end-user so that they are not in danger if they perform critical action like supplying extra load to the converter which will lead to the breakdown of the converter and stop them working.

8.3 Sustainability Aspects

In this section, the sustainability aspects of the thesis will be discussed along with the economical, ecological and social impact. Two cases for each of the subsections will be considered namely size, and efficiency as a priority. In many applications, the power electronic converter is used and the average lifetime of a power electronic converters are around 5-10 years. Once they come to the end of life they are considered as e-waste. Every year there is an increasing trend in e-waste which need to be reduced in order to conserve resources [36]. So, by improving the lifetime of the product the e-wastes can be reduced. Also, improving efficiency will yield more benefits. Analysis of the lifetime of the product can be done using the Life Cycle Assessment (LCA).

8.3.1 Economical & Ecological

The overall reduced converter module size decreases the component size, quantity of components used per board and the PCB board size, which will reduce landfills and therefore, can reduce the maintenance cost for the landfills. Considering efficiency as a priority, this will help in reducing the losses in the applications. Hence, optimized operational cost mutually benefits both the industries as well as the customers utilizing the product.

8.3.2 Social

The reduction in overall module size decreases the plastics waste used in manufacturing PCB. If the PCB is burned, it releases toxic gases which is bad for the society. Discharging capacitors before throwing to the landfills plays a vital role in social aspects. Also, for the product with a reduction in DC/DC converter size, yields in occupying less space.

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A

Appendix 1

A.1 Design of passive snubbers for LTspice simulation

To design the RC passive snubber, initially, the ringing frequency f_r between the voltage peaks are considered. The initial ringing frequency of 28.6 MHz is observed between the voltage peaks. A random capacitor C_1 is placed parallel to the MOSFET. The value of the capacitor C_1 should be selected in such a way that it should at least reduce to 50% of the initial ringing frequency. By adding the capacitor C_1 of capacitance 10 nF, the ringing frequency of 9.35 MHz is observed, which is approximately 63% reduction

After obtaining a reduction in the ringing frequency, the frequency shift ratio m is calculated as,

$$m = \frac{f_{r_1}}{f_{r_2}} = \frac{28.6\,\text{MHz}}{9.35\,\text{MHz}} = 3.05 \tag{A.1}$$

Furthermore, the parasitic capacitance C_o and inductance L_o for the circuit is calculated by,

$$C_o = \frac{C_1}{m^2 - 1} = \frac{10\,\text{nF}}{3.05^2 - 1} = 1.2\,\text{nF} \tag{A.2}$$

$$L_o = \frac{m^2 - 1}{(2\pi f_0)^2 C_1} = \frac{3.05^2 - 1}{(2\pi \cdot 28.6\,\text{MHz})^2 \cdot 10\,\text{nF}} = 25.9\,\text{nH} \tag{A.3}$$

The snubber capacitor C_{snub} is calculated by using the parasitic capacitance from (A.2). The snubber capacitance is selected, such that it is larger than the parasitic capacitance C_o by the factor value of 1 to 4. By increasing the factor value, the ringing across the MOSFET is reduced. But on the other hand, the snubber capacitance with higher factor value increases the snubber losses in the converter. Thus, the optimum factor value of 2 is considered for designing the snubber capacitor,

$$C_{snub} = 2C_o = 2 \cdot 1.2\,\text{nF} = 2.4\,\text{nF} \tag{A.4}$$

Similarly, the snubber resistor $R_{snub-max}$ is calculated by using the parasitic inductance from (A.3). The maximum value the snubber resistance provides complete dampening of the ripple across the MOSFET. But on the other hand, designing the snubber resistor with the maximum resistance would yield higher snubber losses in the converter. Thus, the optimum resistance of 2 Ω is considered for designing the snubber resistor,

$$R_{snub-max} = \sqrt{\frac{L_o}{C_o}} = \sqrt{\frac{25.9\,\text{nH}}{1.2\,\text{nF}}} = 4.65\,\Omega \tag{A.5}$$

In the LTspice simulation, the snubber resistance of 2 Ω and snubber capacitance of 2.4 nF is considered across the secondary winding of the planar ER18 transformer. Figure A.1 shows the flat ripple profile across the MOSFET, which contributes maximum snubber loss in the converter.

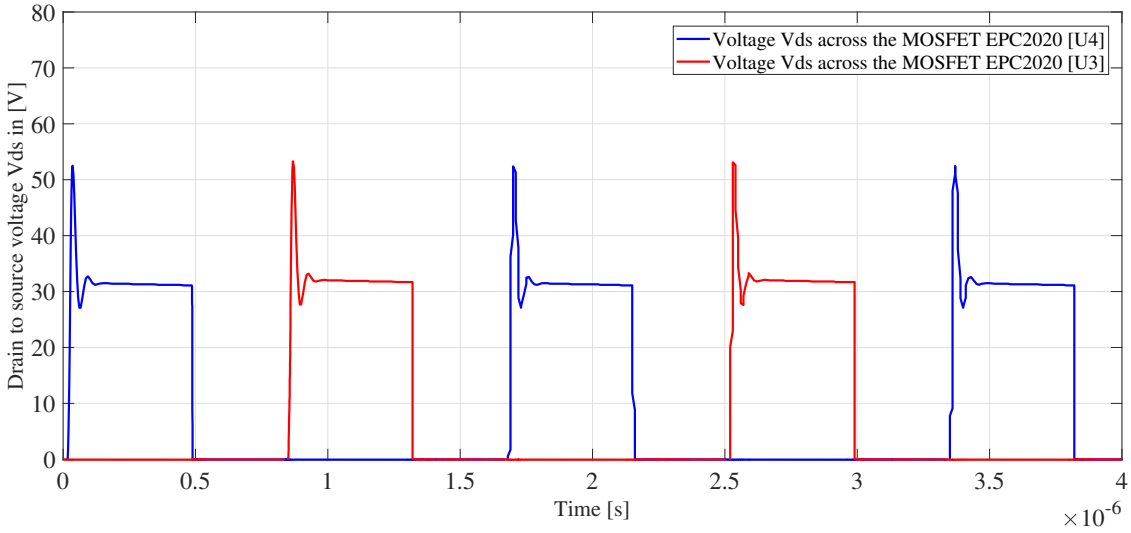

Figure A.1: RC snubber designed with snubber capacitance of 2.4 nF and maximum snubber resistance of 4.65 Ω operating at 48 V input voltage

Similarly, C_{snub} of 3.2 nF and R_{snub} of 2 Ω is designed across the primary winding of the planar ER18 transformer in the LTspice simulation of the GaN MOSFET based half-bridge DC/DC converter.

A.2 Design of controller LM5035B parameters for LTspice simulation

The LM5035B controller consists of 24 pins having quad flat no leads package (WQFN), as shown in figure A.2. The oscillator frequency for the controller LM5035B is set by connecting an external resistance R_T which is calculated by,

$$R_T = \left[\frac{1}{f_S} - 110\,\text{ns}\right] \cdot \left[6.25 \cdot 10^9\right] = \left[\frac{1}{600 \cdot 10^3} - 110\,\text{ns}\right] \cdot \left[6.25 \cdot 10^9\right] = 9.73\,\text{k}\Omega \tag{A.6}$$

where f_S is the converter operating frequency.

The controller LM5035B is protected from under-voltage lockout (UVLO) by having an external operating set-point [37]. The external voltage divider is designed for the operating set-point. The controller LM5035B will completely cease if the

UVLO pin voltage under 0.4 V. Similarly, if UVLO pin voltage is above 0.4 V and less than 1.25 V, the controller remains in standby operation, where auxiliary and VCC is activated, and the outputs of the controller are disabled [37]. When UVLO pin voltage is above 1.25 V, the typical performance of the controller LM5035B is observed [37]. The controller LM5035B activates when the input voltage exceeds

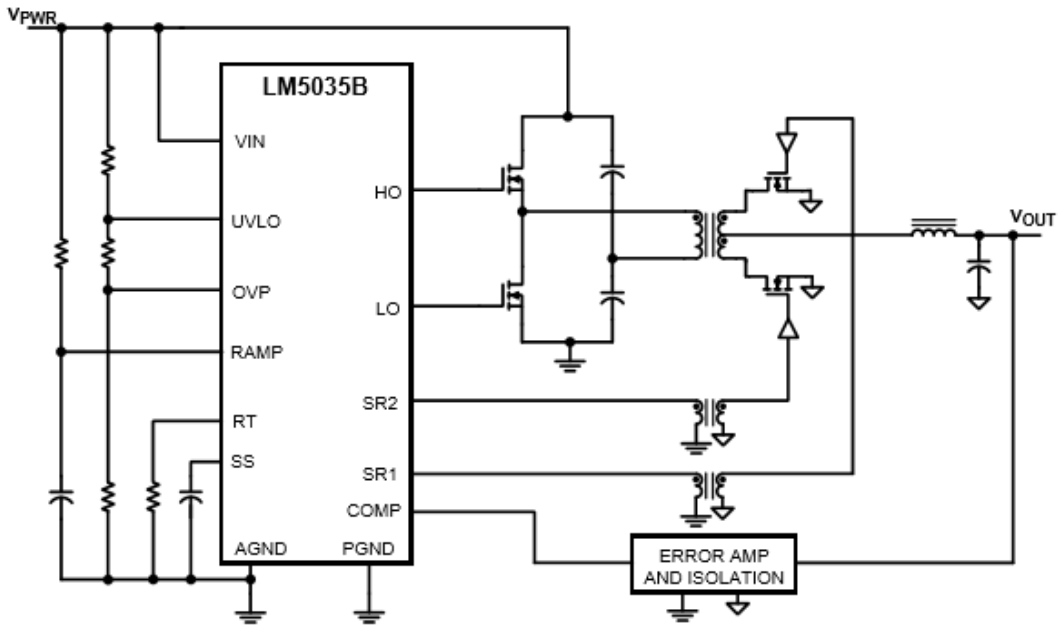

Figure A.2: Simplified diagram for the controller LM5035B [37]

the UVLO voltage of 34.2 V and turns off when it falls below 32.2 V. The internal current sink of 23 µA is enabled, which aids in calculating the external resistors R_1 and R_2.

The controller LM5035B is protected with the overvoltage, and other faults [37]. When OVP pin voltage exceeds 1.25 V, the output of the controller LM5035B is ceased [37]. An external voltage divider is provided to have an operational set-point. The outputs of the controller LM5035B are deactivated when the input voltage reaches 80.5 V.

Figure A.3 shows the design of an external voltage divider for controlling UVLO and OVP. Thus, the external voltage divider is calculated by,

$$R_1 = \frac{UVLO_{on} - UVLO_{off}}{23\,\mu\text{A}} = \frac{34.2 - 32.2}{23\,\mu\text{A}} = 86.6\,\text{k}\Omega \tag{A.7}$$

$$R_{comb} = \frac{1.25\,\text{V} \cdot R_1}{UVLO_{off} - 1.25\,\text{V}} = \frac{1.25\,\text{V} \cdot 86.6\,\text{k}\Omega}{32.2\,\text{V} - 1.25\,\text{V}} = 3.5\,\text{k}\Omega \tag{A.8}$$

$$R_3 = \frac{1.25\,\text{V}\,[R_1 + R_{comb}]}{OVP_{off}} = \frac{1.25\,\text{V}\,[86.6\,\text{k}\Omega + 3.5\,\text{k}\Omega]}{80.5\,\text{V}} = 1.4\,\text{k}\Omega \tag{A.9}$$

$$R_2 = R_{comb} - R_3 = 3.5\,\text{k}\Omega - 1.40\,\text{k}\Omega = 2.1\,\text{k}\Omega \tag{A.10}$$

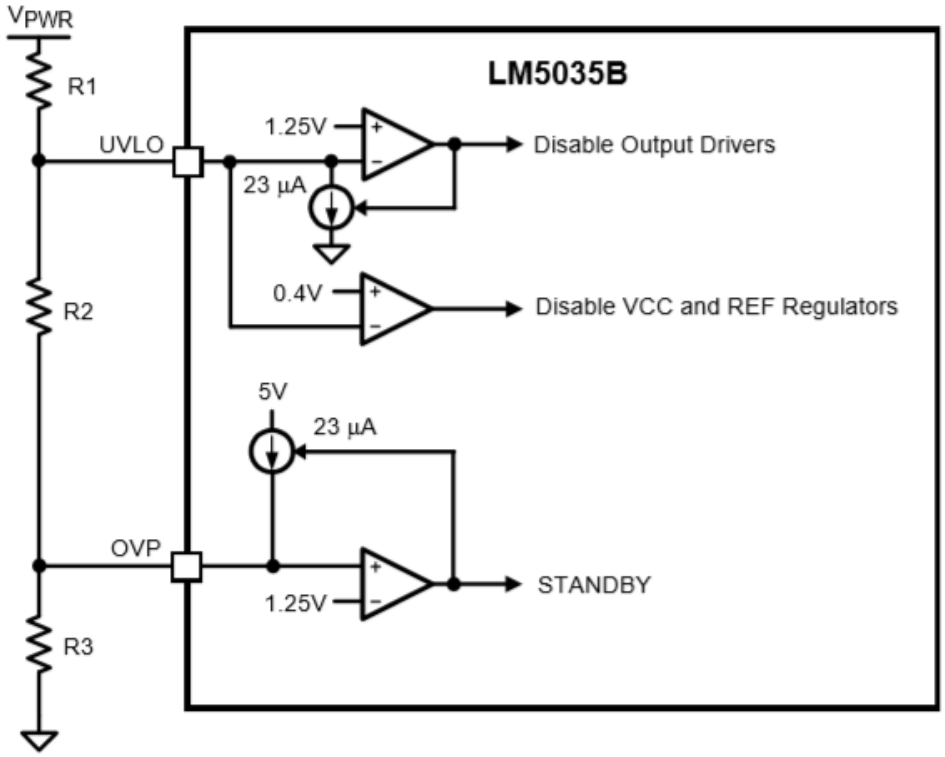

Figure A.3: Design of an external voltage divider for controlling UVLO and OVP [37]

For the controller feedforward, an external resistor R_F and C_F are connected across the input voltage and ground. Depending on the input voltage, the slope of the ramp signal is varied [37]. The feedforward ramp signal is compared with the error signal to adjust the duty cycles of the primary MOSFETs [37]. Thus, the parameter for generating a ramp signal is calculated by,

$$R_F \cdot C_F = \frac{T_{on} + 10\%}{ln\left[\left[1 - \frac{2.5}{V_{in}}\right]^{-1}\right]} \tag{A.11}$$

where V_{in} is the operating input voltage and correspondingly T_{on} is the value of on time. By considering V_{in} of 36 V and T_{on} of 625 ns in (A.11), we get,

$$R_F \cdot C_F = \frac{625\,\text{ns} + 0.625\,\text{ns}}{ln\left[\left[1 - \frac{2.5}{36\,\text{V}}\right]^{-1}\right]} = 9.55\,\mu\text{s} \tag{A.12}$$

Thus, by considering the value C_F of 470 pF, the value of 20.3 kΩ is calculated for R_F.

The stress and current surges during the initial start-up are reduced by using a soft start capacitor, which is connected to the (SS) pin, as shown in figure A.2. During the fault, the controller LM5035B is protected by discharging the capacitor. In this LTspice simulation, the capacitor C_{SS} of 100 pF capacitance is considered.

B

Appendix 2

B.1 Design of controller LM5036 parameters for hardware implementation

As discussed in subsection 2.8.2, the oscillator frequency for the controller LM5036 is set by connecting an external resistor R_T which is calculated by,

$$R_T = \left[\frac{1}{f_{osc} \cdot 1 \cdot 10^{-10}}\right] = \left[\frac{1}{600 \cdot 10^3 \cdot 1 \cdot 10^{-10}}\right] = 16.65\,\text{k}\Omega \tag{B.1}$$

where f_{osc} is the converter operating frequency.

Similar to LM5035B, the controller LM5036 is protected from the under-voltage lockout (UVLO) by having an external operating set-point [17]. If UVLO pin voltage drops 0.35 V, the controller LM5036 will be completely shutdown. Similarly, an internal current of 20 µA is enabled to reduce the UVLO pin voltage if it falls below 1.25 V [17]. As shown in figure B.1, the external resistors R_{UV1} and R_{UV2} are

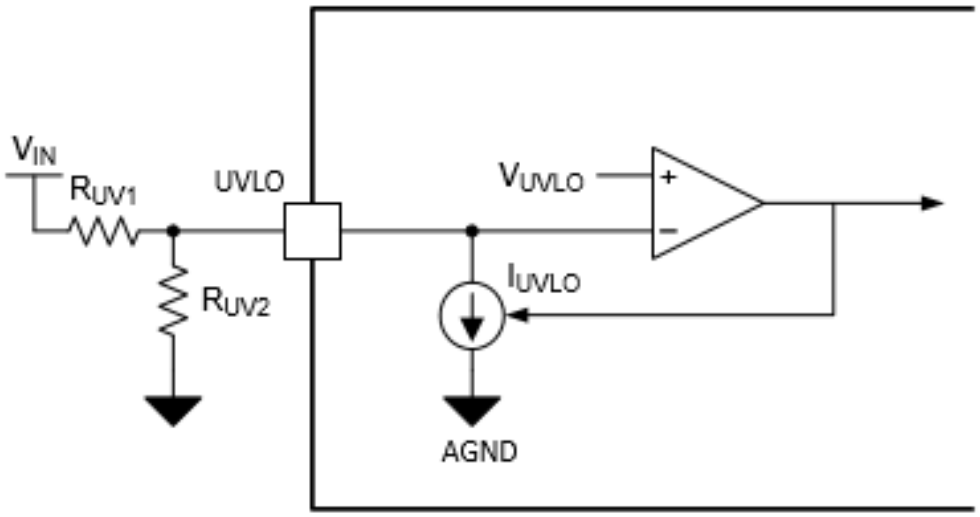

Figure B.1: Design of an external voltage divider for controlling UVLO in LM5036 controller [17]

calculated by,

$$R_{UV1} = \frac{V_{HYS(UVLO)}}{I_{UVLO}} = \frac{V_{HYS(UVLO)}}{20\,\mu A} = 94\,k\Omega \tag{B.2}$$

$$R_{UV2} = \frac{V_{UVLO} \cdot R_{UV1}}{V_{IN(ON)} - V_{UVLO} - [I_{UVLO} \cdot R_{UV1}]} = 4.2\,k\Omega \tag{B.3}$$

where $V_{HYS(UVLO)}$ is the hysteresis of UVLO and $V_{IN(ON)}$ converter operating voltage.

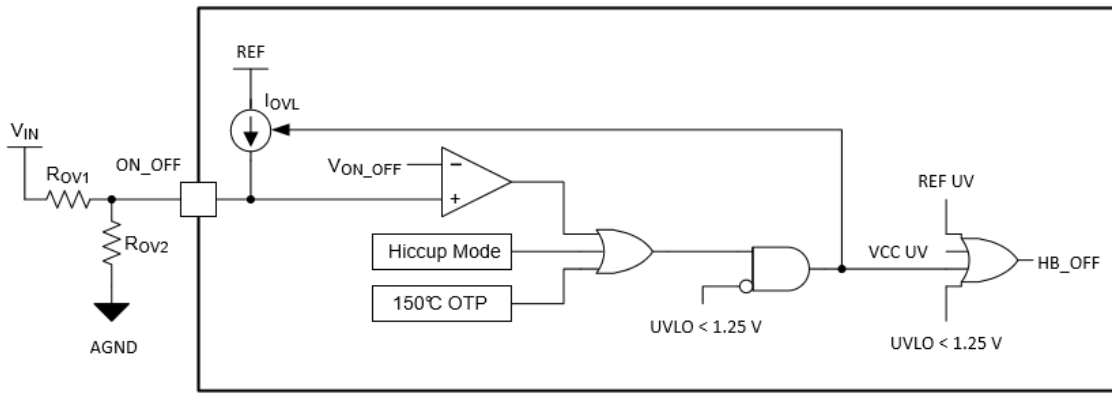

Figure B.2: Design of an external voltage divider for controlling OVP in LM5036 controller [17]

The overvoltage in the controller LM5036 is protected by having an external voltage divider. If any overvoltage or fault occurred, the pin current I_{OVL} of 50 µA is enabled such that the voltage at the ON/OFF pin is increased. If the voltage of the ON/OFF pin is more than V_{ON-OFF}, then the half-bridge operation is turned-off [17]. From figure B.2, the external resistors R_{OV1} and R_{OV2} are calculated by,

$$R_{OV1} = \frac{V_{HYS(OVP)}}{I_{OVL}} = \frac{V_{HYS(OVP)}}{50\,\mu A} = 44\,k\Omega \tag{B.4}$$

$$R_{OV2} = \frac{V_{ON-OFF} \cdot R_{OV1}}{V_{IN(OFF)} - V_{ON-OFF}} = 820\,\Omega \tag{B.5}$$

where $V_{HYS(OVP)}$ is the hysteresis of OVP and $V_{IN(OFF)}$ rising threshold of OVP [17].

The controller LM5036 provides input voltage feedforward by comparing an internally generated ramp signal against the error signal to adjust the duty ratios for the MOSFETs. Thus, the internal ramp signal is generated by having an external resistor of R_{FF} and capacitor C_{FF} connected across the input voltage and ground,

$$C_{FF} \cdot R_{FF} = \frac{-1}{f_{osc} \cdot ln\left[1 - \frac{V_{Ramp}}{V_{IN(min)}}\right]} \tag{B.6}$$

where V_{Ramp} is the expected ramp signal voltage. By considering minimum input voltage of 36 V and V_{Ramp} of 2 V in (B.6), we get,

$$C_{FF} \cdot R_{FF} = \frac{-1}{600 \cdot 10^3 \cdot ln\left[1 - \frac{2\,V}{36\,V}\right]} = 29.16\,\mu s \tag{B.7}$$

Thus, by considering the value C_{FF} of 1 nF, the value of 36 kΩ is calculated for R_{FF}. Similar to LM5035B, a soft start capacitor of 100 nF is connected to SS pin as shown in figure 2.10.

C
Appendix 3

C.1 Detailed calculation of type 3 compensation

As discussed in section 3.4, the components for the type 3 compensation are calculated. The total transfer function for the compensation circuit is given by,

$$H_{Err}(s) = \frac{v_{Err}(s)}{v_o(s)} = \left[\frac{\omega_{P0}}{s} \cdot \frac{\left[1+\frac{s}{\omega_{z1}}\right] \cdot \left[1+\frac{s}{\omega_{z2}}\right]}{\left[1+\frac{s}{\omega_{P1}}\right] \cdot \left[1+\frac{s}{\omega_{P2}}\right]}\right] \tag{C.1}$$

where ω_{P0} is the integrator pole, ω_{P1} and ω_{P2} corresponds to the second and third pole in the type 3 compensation. Similarly, ω_{z1} and ω_{z2} corresponds to second and third zero in the type 3 compensation. Figure C.1 shows the components that constitute integrator pole in the type 3 compensation, and it is calculated by,

$$\omega_{P0} = \frac{1}{R_{53} \cdot (C_{41} + C_{40})} \tag{C.2}$$

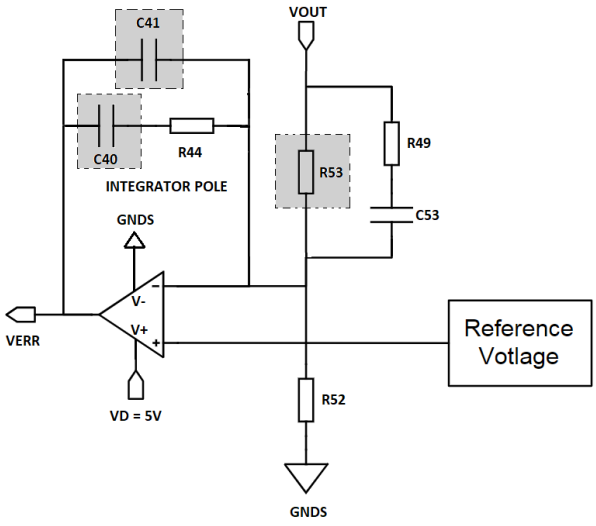

Figure C.1: Integrator pole in the type 3 compensation

Similarly, figure C.2 shows the components that constitutes second and third pole in the type 3 compensation and it is calculated by,

$$\omega_{P1} = \frac{1}{R_{49} \cdot C_{53}} \tag{C.3}$$

$$\omega_{P2} = \frac{1}{R_{44} \cdot \frac{C_{41} \cdot C_{40}}{C_{41} + C_{40}}} \tag{C.4}$$

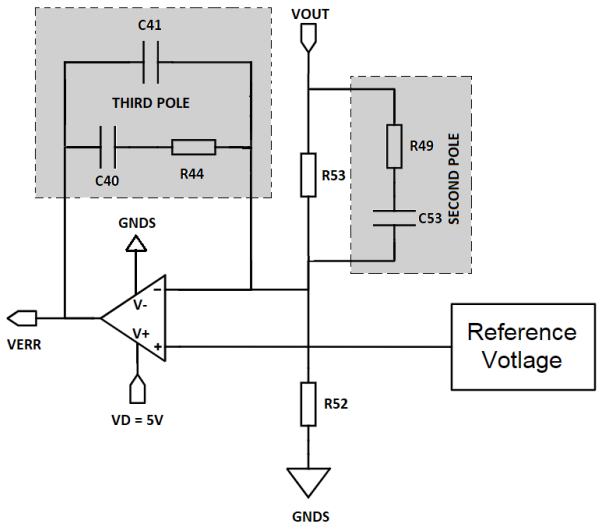

Figure C.2: The second and third pole in the type 3 compensation

Figure C.3 shows the components that constitutes first and second zero in the type 3 compensation and it is calculated by,

$$\omega_{z1} = \frac{1}{R_{44} \cdot C_{40}} \tag{C.5}$$

$$\omega_{z2} = \frac{1}{(R_{49} + R_{53}) \cdot C_{53}} \tag{C.6}$$

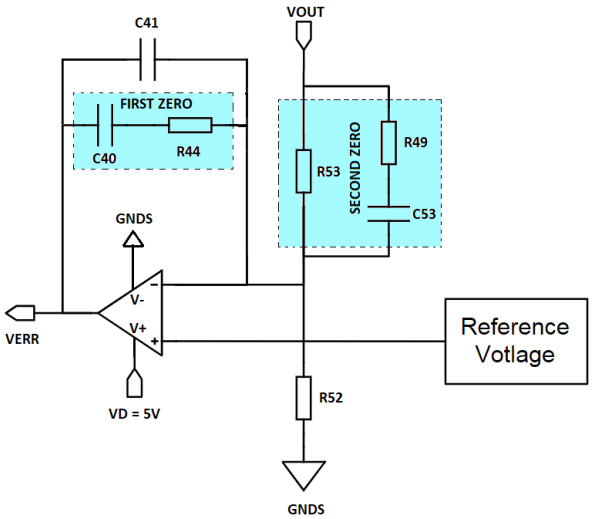

Figure C.3: First and the second zero in the type 3 compensation

D

Appendix 4

D.1 Future improvements in the GaN MOSFET based half-bridge DC/DC converter

The GaN MOSFET based half-bridge DC/DC converter is designed with passive snubber with high deadtime losses. However, the efficiency of the GaN MOSFET based half-bridge DC/DC converter can be improved by having the least deadtime and snubber losses. As discussed in section 6.5, a deadtime of 64 ns is observed on the leading edge and a deadtime of 77 ns is observed on the falling edge of the drain to source voltage V_{DS} across synchronous MOSFET U_3 during the full-load output current of 27.8 A. The deadtime loss in the GaN MOSFET based half-bridge DC/DC converter is calculated by,

$$P_{LE} = V_F I_S \left[\frac{t_{LE}}{t_s}\right] = 2.4\,\mathrm{V} \cdot 13.9\,\mathrm{A} \cdot \left[\frac{64\,\mathrm{ns}}{1.67\,\mu\mathrm{s}}\right] = 1.2\,\mathrm{W} \tag{D.1}$$

where P_{LE} power loss during leading-edge, V_F is the reverse conduction voltage of the synchronous GaN MOSFET, I_S is the average current flowing across the synchronous MOSFETs, t_{LE} is the leading edge deadtime and t_s is the overall time duration. Similarly, power loss during falling edge P_{FE} is calculated by,

$$P_{FE} = V_F I_S \left[\frac{t_{FE}}{t_s}\right] = 3.7\,\mathrm{V} \cdot 13.9\,\mathrm{A} \cdot \left[\frac{77\,\mathrm{ns}}{1.67\,\mu\mathrm{s}}\right] = 2.4\,\mathrm{W} \tag{D.2}$$

where t_{FE} is the falling edge deadtime. The total deadtime loss P_{DT} is calculated by,

$$P_{DT} = P_{LE} + P_{FE} = 3.6\,\mathrm{W} \tag{D.3}$$

In the future, the suitable controller with deadtime of 15 ns would enhance the overall efficiency of the GaN MOSFET based half-bridge DC/DC converter. With deadtime of 15 ns the losses can be calculated as,

$$P_{LE} = V_F I_S \left[\frac{t_{LE}}{t_s}\right] = 2.4\,\mathrm{V} \cdot 13.88\,\mathrm{A} \cdot \left[\frac{15\,\mathrm{ns}}{1.66\,\mu\mathrm{s}}\right] = 0.3\,\mathrm{W} \tag{D.4}$$

$$P_{FE} = V_F I_S \left[\frac{t_{FE}}{t_s}\right] = 3.7\,\mathrm{V} \cdot 13.88\,\mathrm{A} \cdot \left[\frac{15\,\mathrm{ns}}{1.66\,\mu\mathrm{s}}\right] = 0.5\,\mathrm{W} \tag{D.5}$$

$$P_{DT} = P_{LE} + P_{FE} = 0.8\,\mathrm{W} \tag{D.6}$$

Thus, with the reduction in deadtime to 15 ns, the approximate deadtime losses of 0.8 W can be achieved, which enhances the performance of the converter.

Similarly, the power dissipation P_{snub} across the pair of passive snubber in the GaN MOSFET based half-bridge DC/DC converter is calculated by,

$$P_{snub} = C_{snub} V^2 f = 2 \cdot 1.8\,\text{nF} \cdot 47\,\text{V}^2 \cdot 300\,\text{kHz} = 2.3\,\text{W} \tag{D.7}$$

The losses across passive snubber can be minimized by introducing the active snubber. By introducing the active snubber, the initial voltage spiking across the synchronous MOSFETs can be clipped. The approximate loss across the pair of the active snubber is estimated to be 1.1 W. Thus, the introduction of an active snubber and better deadtime from the controller would yield maximum efficiency.