CHALMERS
UNIVERSITY OF TECHNOLOGY

Design and Realization of Doherty Power Amplifier Based on Active Load-Pull Measurements

Master's thesis in electrical engineering

VASILEIOS TOKMAKIS

MASTER'S THESIS

Design and Realization of a Doherty Power Amplifier Based on Active Load-Pull Measurements

VASILEIOS TOKMAKIS

CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Microtechnology and Nanoscience
Microwave Electronics Laboratory
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2016

Design and Realization of Doherty Power Amplifier Based on Active Load-Pull Measurements
VASILEIOS TOKMAKIS

Supervisors: Tech. Lic. William Hallberg and Asst. Prof. Koen Buisman, Department of Microtechnology and Nanoscience
Dr. David Gustafsson, Ericsson AB

Examiner: Prof. Christian Fager, Department of Microtechnology and Nanoscience

Master's Thesis 2016
Department of Microtechnology and Nanoscience
Microwave Electronics Laboratory
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Gothenburg, Sweden 2015

Design and Realization of Doherty Power Amplifier Based on Active Load-Pull Measurements
VASILEIOS TOKMAKIS
Department of Microtechnology and Nanoscience
Chalmers University of Technology

Abstract

Energy-efficient power amplifiers capable of supporting advanced communication standards are essential for the expanding wireless infrastructure. The Doherty power amplifier (DPA) is one of the most common high efficiency power amplifier (PA) architectures. However, the DPA is significantly sensitive to model accuracy due to its complex design, leading to sub-optimal performance. A proposed solution to overcome this barrier of inaccuracy is to use measurement data from an experimental active load-pull setup. In this work, an active load-pull system was developed, tested and used in the characterization of a 10W GaN HEMT. The characterization data were used in combination with a new DPA design approach, intended to provide an improved efficiency and linearity tradeoff, to design and fabricate a DPA.

The developed active load-pull system was used for fast acquisition of load-pull data in a wide range of input and output power levels. The system was developed using modular components, allowing an easy adjustment to the specific needs of any future project.

The characterization of the GaN device was conducted by using a precursor development board (DB). The DB contained the device along with its stability network and second harmonic and baseband terminations. The DB was characterized at different power levels of interest and was used as is in the final DPA design.

The designed and fabricated DPA presented excellent performance with good agreement with the theoretical predictions, verifying the robustness of the implemented designed method. The DPA was designed to operate at 2.14 GHz and reached an output power level of 40.8 dBm, which was 1.5 dB less than the expected, and with a gain of 11.4 dB at back-off (BO) and 10.9 dB at full power (FP). The power added efficiency at 6.2 dB BO was 42.3 % and 50.1 % at FP. The phase response of the DPA presented a distortion of 8.8° at BO and 17.6° at FP.

The developed active load-pull system proved to be a powerful tool for characterizing transistors for PA design. However, the results indicate that the system needs further improvements in the accuracy of the measurements. That being said, this thesis is as an important milestone for the quest of making better PAs required for future wireless communication systems.

Keywords: Active Load-Pull, Doherty, DPA, Efficiency, GaN, Linearity, Power Amplifier.

Acknowledgements

This Master's thesis has been conducted at the Department of Microtechnology and Nanoscience at Chalmers University of Technology, Sweden, and Ericsson AB from January to December 2016. The work with the Master's thesis has been strongly supported by several persons that should be acknowledged.

First, I would like to thank Tech. Lic. William Hallberg and Asst. Prof. Koen Buisman for all the help and support they offered to me from the first day of this project. In addition, I would like to thank Dr. David Gustafsson and Dr. Kristoffer Andersson from Ericsson AB for the insightful conversations we had during the time at Ericsson and the guidance he offered to me throughout the whole time. A warm thank also to Prof. Christian Fager for being my examiner and he had his office door open always for me.

I would also like to acknowledge the support from Modelithics models utilized under the University License Program from Modelithics, Inc. and National Instruments Cop.

I would also like to thank my friends and tutors for their support throughout my academic life and their patience. A special thank you to my family, for being always supportive to me.

With that, Master's Thesis, a circle of studies at Chalmers University of Technology, closes for me. I am grateful that i had the opportunity to study in a university like Chalmers, which allowed me to develop further as person and as professional.

Vasileios Tokmakis, Gothenburg, December 2016

Notations and Abbreviations

Notations

γ	Back-off level
P_{avs}	Power available from source
P_{in}	Input power
P_{inj}	Injected power
P_L	Power delivered to the load
Γ_L	Load reflection coefficient
Γ_S	Source reflection coefficient
W_R	Voltage wave ratio
η	Drain efficiency
G_T	Transducer gain
G_p	Operational gain
PAE	Power-added efficiency
V_{gs}	Gate-source voltage
V_{ds}	Drain-source voltage
I_{ph}	Drain current phase
I_{ds}	Drain current
Z_s	Source impedance
$Z_{S,\ system}$	System source impedance

Abbreviations

ADS	Advanced Design System
BO	Output back-off
CW	Continuous wave
CAD	Computer aided design
DAQ	Data acquisition
DAC	Digital to analog converter
DPA	Doherty power amplifier
DB	Development board
DUT	Device under test
FPGAs	Field programmable gate arrays
IQ	In-phase/quadrature
LO	Local oscillator
PA	Power amplifier
PAPR	Peak-to-average power ratios
PPL	Phase-locked loop
PSU	Power supply unit
RF	Radio frequency
SOLT	Short, open, load and through
SPDT	Single pole double throw

Contents

1 Introduction 1

1.1 Motivation 1

1.2 Thesis contribution 2

1.3 Thesis Outline 2

2 Power Amplifier Measurement System 3

2.1 Theoretical considerations of load-pull systems 3

2.1.1 Power amplifier design methodologies 3

2.1.2 Load-Pull Basics 3

2.1.3 Passive Load-Pull 5

2.1.4 Active Load-Pull 6

2.1.5 Injection Power estimation 7

2.2 Design of an active load-pull system 9

2.2.1 System requirements 9

2.2.2 System Hardware Design 9

2.2.3 System Software Design 14

2.2.4 System Verification 20

3 Designing a Doherty Power Amplifier 25

3.1 Fundamentals of Doherty power amplifiers 25

3.2 Doherty power amplifier design strategy 26

3.2.1 Doherty power amplifier design goals 26

3.2.2 Design strategy steps 27

4 Device characterization development board 28

4.1 Development board design 28

4.1.1 Devices and substrate 28

4.1.2 Stability network 28

4.1.3 Harmonic terminations 30

4.1.4 Bias feed and baseband terminations 32

4.1.5 Fabrication Considerations 33

4.2 Development board measurements 34

4.2.1 Measurements considerations 34

4.2.2 Power levels 35

4.2.3 DC Bias sweeps 35
4.2.4 Load-pull of main development board 36
4.2.5 Load-pull of auxiliary development board 38
4.3 Measurement based design parameters 38
5 Measurement based Doherty power amplifier design 41
5.1 Input power divider 41
5.2 Input phase shifter 42
5.3 Main and auxiliary input matching networks 42
5.4 Output power combiner 43
5.5 Complete layout 44
6 Doherty power amplifier measurements 45
6.1 CW Measurements 45
6.1.1 Measurements with initial conditions 46
6.1.2 Main device gate voltage sweeps 47
6.1.3 Auxiliary device gate voltage sweeps 48
6.1.4 Input phase delay sweeps 49
7 Conclusion and future work 52
7.1 General conclusions 52
7.2 Future work 52
8 Bibliography 53

1 Introduction

1.1 Motivation

The never-ending quest for greater capacity and higher data rates in radio access networks puts increasing demands on the transmitters of the radio base stations. These demands must be met within the existing radio base stations carbon footprint. At the same time, network operators want to cut operating costs, in which energy consumption is a significant factor [1]. The increasing modulation complexity in the transmitted signals reduces the energy efficiency of the traditional transmitters due to increasing peak-to-average power ratios (PAPR). The power amplifier (PA), which is responsible for delivering the required transmitter signal power level, is dominating the overall transmitter power consumption. Energy-efficient PAs capable of supporting modern and future communication standards are therefore needed to reduce the carbon footprint and to avoid heating problems of an expanding wireless infrastructure [2].

The Doherty power amplifier (DPA) is one of the most commonly implemented architectures for high efficiency PAs [3, 4]. It was first proposed in 1936 [5], and is primarily an efficiency enhancement design technique which relates very well with the trends and needs of modern communication systems [6]. The DPA is an ideal candidate for maximizing the PA efficiency for signals in modulation schemes with high PAPR. While the DPA increases the efficiency significantly, it does however suffer from some drawbacks such as, low gain, low bandwidth, amplitude and phase distortion. Recently, in a new published design approach [7-9], a generalized DPA topology that presents a novel possibility to reduce the phase distortion while maintaining high efficiency was described.

The mentioned method can be used to improve the phase linearity of the DPA. Another aspect of the design process that can be improved is the dependency on simulation models. PAs are usually designed in simulation software using device models. Most of the device models used by the modern simulation tools, such as the Advanced Design System (ADS) from Keysight, can predict the behavior very accurately for the needs of conventional PA designs. The simulated design source and load impedances will result in power levels and efficiencies which will be very close to real measurements. This fact is not often true for DPA designs. The DPA is significantly sensitive to model accuracy due to its complex design. The largest drawback of these models is often that they are not capable of predicting the phase distortion accurately enough in large signal operation. As the DPA is very sensitive to phase changes between the main and auxiliary amplifier, significant degradation of the performance is observed in the final product [10].

A proposed solution to overcome this barrier of inaccuracy is to use measurement data from an experimental active load-pull setup, during the design process. The use of this approach has the benefit of eliminating simulation errors and should result in a more realistic performance outcome.

1.2 Thesis contribution

This thesis has two goals. The first goal was to fabricate a state-of-the-art DPA based on active load-pull measurements. The second and most important goal was the development of the experimental active load-pull setup. The load-pull setup was developed with a focus on measurements related to the DPA design. However, it was designed such that further development can be done, i.e. for future advanced research projects related to PAs. The load-pull setup has modular parts which can be adjusted for more complex tasks including measurements with wider bandwidth modulated signals and inclusion of harmonics.

1.3 Thesis Outline

This thesis describes the design and implementation of two distinct parts, the DPA and the load-pull measurement system. Because of the high dependency of the DPA design on the load-pull measurements, the load-pull system is discussed first. In Chapter 2, a brief introduction on the fundamental principles of load-pull systems is presented, as well as the actual design and implementation of the system, along with verification measurements. In Chapter 3, the DPA theory is briefly described, and the design strategy is explained. After that, in Chapter 4, the design and the measurements of the development board are presented. Using the results from the measurements of the development board, the design of the DPA is shown in Chapter 5, describing all the steps necessary to design the final amplifier. In Chapter 6, the DPA characterization is presented along with the measurement results of its performance. Finally, in Chapter 7, the overall results are discussed and considerations for future work are suggested.

2 Power Amplifier Measurement System

In this chapter, a brief introduction on the fundamental principles of load-pull systems is presented, as well as the actual design and implementation of the system, along with verification measurements.

2.1 Theoretical considerations of load-pull systems

In this section, the use of load-pull system in the PA design process is described. The fundamental principles are presented and discussed concisely.

2.1.1 Power amplifier design methodologies

The design methods of a power amplifier can be divided into two categories. The first category includes methods based on computer aided design (CAD). CAD relies on a nonlinear device model which predicts the behavior of the device. The second category is measurement based methods. In this design approach, the device is characterized in terms of relative design parameters, such as gain, input and output power levels and power added efficiency. Since it is essential to use impedance matching networks on the input and output of a transistor in order to maximize power transfer, output power, gain and efficiency, it is required to determine these ideal matching network impedances. This measurement technique is referred to as load-pull [11].

Usually, the characterization concerns only the device, but auxiliary circuits can also be included, such as the bias and matching networks in the form of preliminary development board (DB). The characterization of these DBs can lead to higher precision by including and compensating for extra imperfections induced by the auxiliary circuits. After the characterization of the device, the measured data will form the primary basis of the design.

The main benefit of this technique is that is faster compared to the time required to develop a complete nonlinear device model. In addition, it offers a robust design approach since the device is measured under realistic conditions. The limitations of obtaining the design targets are mainly set by the measurement system type and accuracy it can achieve, as is described in this chapter.

2.1.2 Load-Pull Basics

Load-pull is one of the most useful tools that can be employed to design circuits based on nonlinear active devices. Load-pull can be used in the design, testing and model verification of an amplifier design [12]. In its most fundamental definition, load-pull can be described as the process of specifically creating an a priori known impedance to a device under test (DUT) in a precisely controlled way, in order to create the optimum operation conditions and thus find the optimum performance of the device.

A load-pull system allows the determination of the appropriate matching impedance by adjusting the load reflection coefficient Γ_L that is presented to the DUT. Parameters that are needed in the design such as power delivered to the load (P_L), drain efficiency (η), operating power gain (G_T) and gain compression, and power-added efficiency (PAE) are measured for different values of Γ_L. By measuring for different values of Γ_L, for constant input power (P_{in}) or power available from source (P_{avs}) levels, contours of different performance parameters can be plotted on a Smith chart.

Figure 1 presents the basic principle of the load-pull operation on a DUT. The DUT is driven by a signal source with impedance Z_S and a load tuner is connected to the output port. A source tuner can also be placed in between the source and the input of the DUT if source pull operation is required.

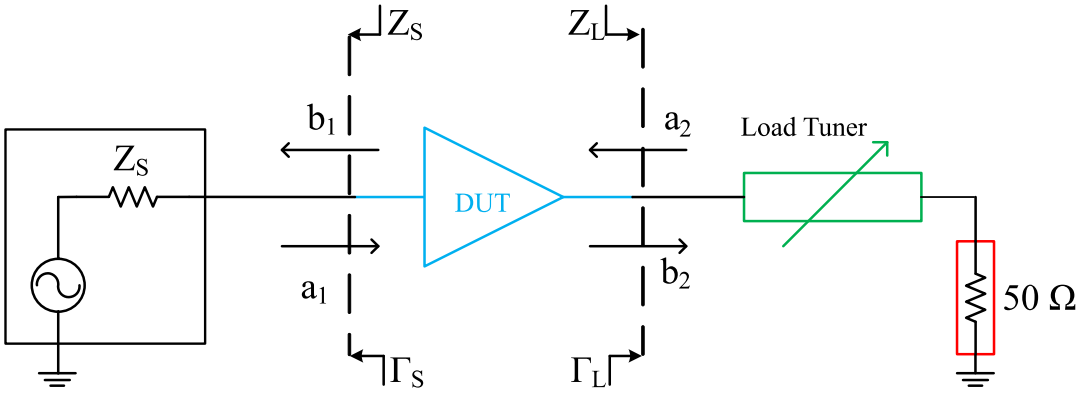

Figure 1. Basic principle of the load-pull operation on a DUT. The DUT is connected in its input (left side) to a signal source with impedance Z_S and optionally with a source tuner. On the output a load tuner is connected, providing the Γ_L variation. The reference plane for the measurement of Γ_L and Γ_S is indicated with the dashed lines.

The method is based on the measurement of traveling waves. As Figure 1 shows, two reference planes exist where the traveling waves are defined. The waves have complex values. A common convention is that the waves traveling into the DUT are denoted with the letter a, and waves emanating from the DUT with the letter b. At the input port, the wave a_1 is generated from the source and b_1 is the reflected wave from the DUT. The ratio of these two waves defines the input reflection coefficient Γ_{IN} of the DUT, see Eq. (1)

$$\Gamma_{IN} = \frac{b_1}{a_1} \tag{1}$$

At the output port, the wave a_2 and b_2 are defined. The b_2 wave is the one generated from the output of the DUT and the a_2 wave is the reflection from the load tuner. The load reflection coefficient Γ_L is defined as the ratio of the traveling wave a_2 over b_2, see Eq. (2). The reflection Γ_L is related to the load impedance Z_L according to Eq. (3), where Z_0 is the system impedance [13].

$$\Gamma_L = \frac{a_2}{b_2} \tag{2}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3}$$

The role of the load tuner is to vary the magnitude and phase of the reflected traveling wave a_2 and thus present a selected value of Γ_L to the DUT. The same principle applies also in the source tuner. Source pull measurements can provide similar design information for the input of the DUT. Since the current work doesn't include these type of measurements the reader can refer to [14-16] for further information. Figure 2 illustrates the effect of the reflected traveling wave a_2 variation and the consequential change in the Γ_L. A variation of the a_2 magnitude will translate into a radial move of the Γ_L (blue line) on the load reference plane and a positive increase of the a_2 phase will result to a clock-wise rotation (red line).

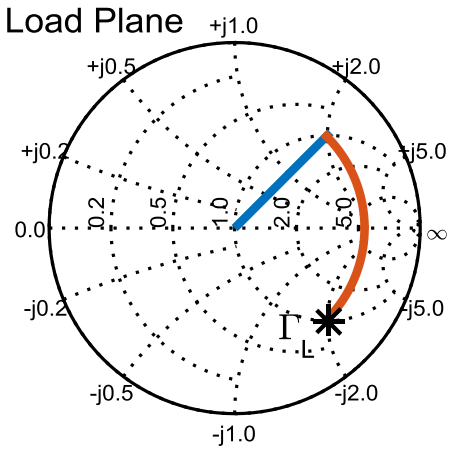

Figure 2. The effect of the reflected traveling wave a_2 variation to Γ_L. A variation of the a_2 magnitude will translate into a radial move of Γ_L (blue line) and an increase of the a_2 phase will result to a clock-wise rotation (red line).

The tuners can be active or passive, depending on the applications. In a passive tuner, mechanical movement of stubs achieves the variation of a2. In active load-pull, a_2 is varied by a magnitude and phase-controlled signal actively injected at the output of the DUT.

2.1.3 Passive Load-Pull

Passive load-pull [17], as the name implies, makes use of a passive load tuner in order to tune the reflection coefficient and present the necessary load impedance to the DUT. A typical configuration of a passive load-pull is shown in Figure 3. The system makes use of a load tuner based on mechanical sliding probe on a transmission line. The height of the probe from the transmission line adjusts the magnitude of Γ_L and the length distance variation of its position on the transmission line changes the phase of Γ_L. This kind of system is often preferred for its simplicity and high power handling capability. The major disadvantage of a passive load-pull system is the restriction on the maximum magnitude of reflection coefficient that can present to the DUT due to the losses of the tuner. Another drawback is the limited bandwidth of the tuner and the sweep times it can reach.

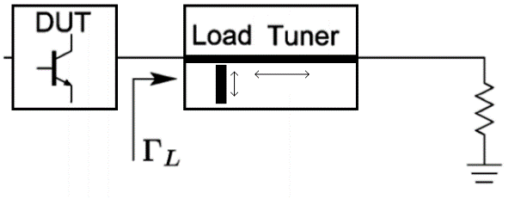

Figure 3. A typical configuration of a passive load-pull setup. The tuner is connected at the output of the DUT. The presented load impedance is varied by changing the position of the vertical probe. Vertical movements translate to Γ_L magnitude change and horizontal movements to phase rotations.

2.1.4 Active Load-Pull

Active load-pull systems, which are based on injection of signals at the DUT plane, possess the ability to synthesize high reflection coefficients by overcoming the inherent losses in the passive technique, and therefore can provide full Smith chart coverage [18, 19]. Active load-pull can actually reach areas beyond the smith chart and this is achieved by adding energy into the system, enough to overcome the DUT output and the losses of the system using additional amplifiers. The basic principle of this method is the manipulation of the reflection coefficient Γ_L by actively injecting an amplitude and phase controlled signal a_2 towards the DUT, as Eq. (4) describes.

$$\Gamma_L = \frac{a_2}{b_2} = \frac{A\, e^{j(2\pi f+\varphi)}}{b_2} \qquad (4)$$

In literature, [20-22] two main architectures for active load–pull have been promoted over time, i.e. the open loop and the closed loop configurations, which are briefly discussed next.

2.1.4.1 Closed-Loop Active Load–Pull Systems:

In this type of system, the output of the DUT is partially coupled and readjusted in amplitude and phase, and then after it receives further amplification is injected back to the DUT. As can be seen in Figure 4, the configuration creates a closed loop at the output of the DUT. The system presents quick response times and it suitable for real time adjustment of the Γ_L for fast measurements and it doesn't require a separate signal source [21]. The main drawback comes from its close-loop nature: it can induce oscillations that can damage the DUT. In order to avoid oscillations, special filtering techniques have to be implemented [23].

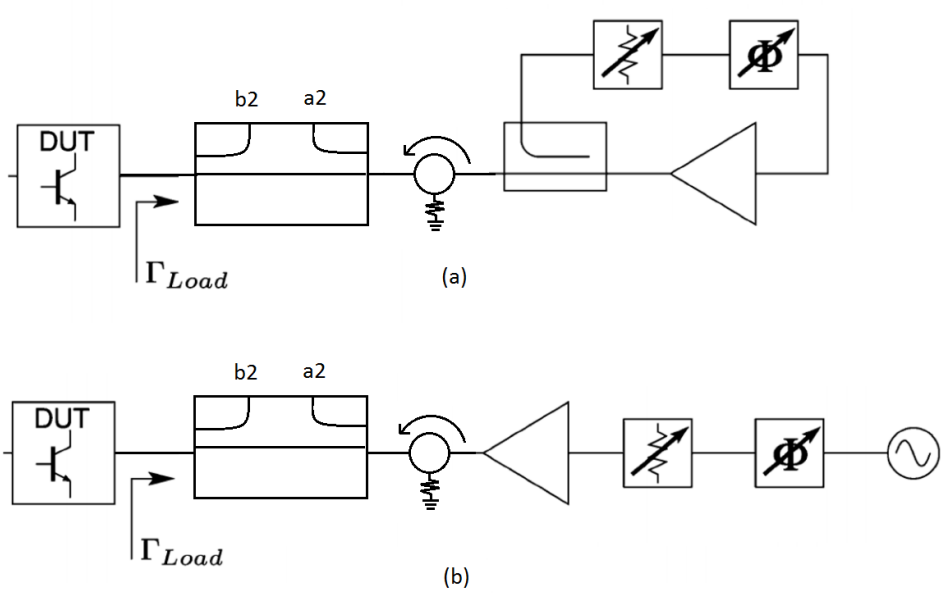

Figure 4. Typical configurations of a closed loop (a) and open loop (b) active load-pull systems [20].

2.1.4.2 Open-Loop Active Load–Pull Systems:

In the open loop systems, see Figure 4, a second signal generator creates a new signal properly adjusted without reusing the output of the DUT. The signal is injected towards the DUT, i.e. as the a_2 wave, and thereby creates the desired load reflection coefficient. Since the signal is not directly depended on the DUT generated wave, an iterative process is necessary to reach the wanted amplitude and phase of Γ_L. This makes the system slower compared to the closed-loop configuration. On the other hand, the open-loop configuration has the benefit of being oscillation free and the possibility to control the injected signal in the digital domain, which is more flexible and faster. These benefits come, however, at the expense of the need for an extra signal source.

The control of the amplitude and phase of the injected signal can be done by using attenuators and phase shifters or using in-phase/quadrature (IQ) modulators. A software routine can be used to control the iterative adjustment of the injected signal in the digital domain by using a converging algorithm. The travelling waves at the output of the DUT are measured through a coupler, located between the DUT and the pre-amplifier of the injected signal.

2.1.5 Injection Power estimation

A key design characteristic of any active load-pull system is the necessary power of the injected wave a_2 (P_{inj}). The value of P_{inj} is dynamically varied during a load-pull measurement and is depended on the magnitude of the load reflection coefficient and the power delivered to the load from the device (P_L). Therefore, the maximum achievable magnitude of the load reflection coefficient will be a function of both P_{inj} and P_L. Figure 5 illustrates a typical output setup of an active load-pull system, consisting of a DUT, a directional coupler, an isolator and a pre-amplifier for the injected signal. The calculation of P_{inj} is done according to the method described in [24].

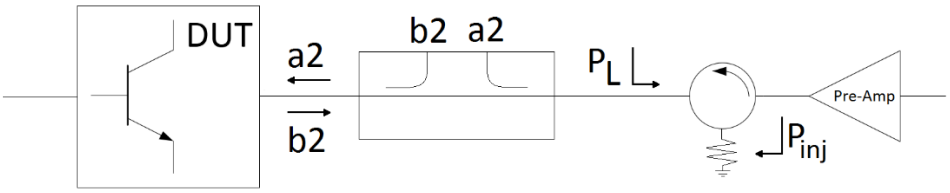

Figure 5. Typical output setup of an active load-pull system, consisting of a DUT, a directional coupler, an isolator and a pre-amplifier for the injected signal.

According to this approach, the fundamental problem associated with the implementation of the active load-pull systems is that they don't scale well to higher power levels. This is due to the large impedance difference between the optimum impedance required by the devices (usually about 10 Ohms) and the characteristic impedance of the measurement systems (50 Ohms). The ratio of the injected power and the delivered power to the load, which in the setup of Figure 5 is the termination load of the isolator $Z_0 = 50$ Ohm, can be expressed as:

$$\frac{P_{inj}}{P_L} = \frac{|\Gamma_L^2|}{1 - |\Gamma_L^2|} \tag{5}$$

where P_L is calculated from the traveling waves according to:

$$P_L = \frac{|b^2| - |a^2|}{2Z_0} \tag{6}$$

The behavior of Eq. (5) is shown in Figure 6. The plot shows that in order to achieve measurements at the edge of smith chart, the injection signal has to be 30 dB larger than the DUT P_L. Although a solution has been proposed to address this issue [25], it is not necessary for this work as the targeting maximum $|\Gamma_L|$ is approximately 0.9. The power ratio at this level is only 6 dB and easy to achieve it with the proper pre-amplifier.

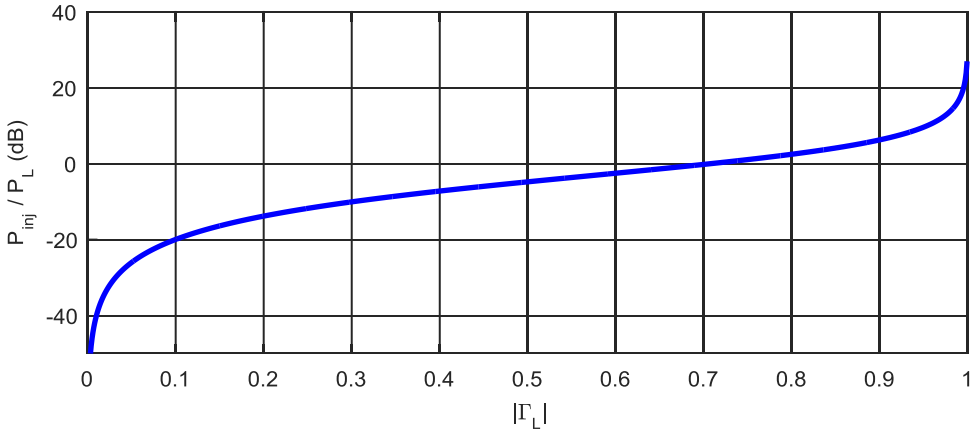

Figure 6. The required power ratio of the injected signal and the delivered power from the DUT for different values of $|\Gamma_L|$, see Eq. (5).

2.2 Design of an active load-pull system

2.2.1 System requirements

The experimental active load-pull setup was built to meet the minimum characterization requirements of the DPA design of this project. It is worth to be mentioned that the system was designed in a way that it is capable for further development in the future. This is achieved by using modular hardware and software parts. The benefit of using modular parts is that they can be replaced by others to meet specific requirements, for other projects without compromising the functionality of the system and without any major changes in the system architecture nor the software implementation. Thus, the system can be adjusted to operate at different frequencies, power levels, signal modulations and signal bandwidths. In addition, the system is suitable for multi-harmonic load-pull measurements and wideband modulation characterization. However, the modularity of the system comes at the cost of space, which for an experimental setup is an acceptable compromise.

The main system requirement is to provide a complete characterization of a device by presenting to it a range of load impedances covering most of the smith chart region for a wide range of input driving power levels. The characterization for this specific work was performed under a single tone signal with a center frequency f_0 at 2.14 GHz. The system had to have the ability to measure and export data measurements for the P_{avs}, P_{in}, G_t, G_p, PAE, η and Γ_{IN} for each load impedance. Also, power sweep capability for a specified load impedance was required. Additionally, the system had to provide S-parameter measurements, which are critical for the design process and easy to implement, consisting only of the necessary software code without requiring any hardware changes.

For the current DUT, the P_{avs} requirement was 32 dBm for deep compression characterization. To have some margin, the system was designed for a maximum P_{avs} of 38 dBm. Regarding the output power from the DUT, the system was designed to handle up to 50 dBm, which was more than sufficient for the estimated output of the projects DUT with P_L of 40 dBm.

The last design factor is the injection power level (P_{inj}) that will define the maximum load reflection coefficient presented to the output of the DUT. The limitation here comes from the available hardware for the project, which was the pre-amplifier for the injected signal, which had a maximum linear output power of 44.5 dBm. For a P_L of 40 dBm from the DUT, the system can achieve a maximum magnitude of $\Gamma_L = 0.86$, see Eq. (5). This value satisfies the DUT characterization requirements from model simulations.

2.2.2 System Hardware Design

The system was implemented using the National Instruments PXI Express Chassis PXIe-1085, see Figure 7. The chassis hosts a computer responsible for the data process, storage and the control software of the system. Additionally, the chassis hosts the two signal sources and the two receivers, which are modular and contain their own field programmable gate arrays (FPGAs). Also the chassis contains an internal 10 MHz reference clock which is used to synchronize all the system elements.

Figure 7. The NI PXI Express Chassis PXIe-1085 used for the system implementation along with the two NI 5792 receivers and two NI 5793 transmitters.

The block diagram of the system is shown if Figure 8. The system can be divided in two main areas: the drive side and the injection side. The drive side corresponds to the input port of the DUT and contains the driving signal generation and detection. On the other side, the injection side is connected to the output of the DUT and accounts for the injection signal generation and detection. The DUT is located in the middle of the system where red dashed lines indicate the calibrated reference planes. A short description of all the system components follows.

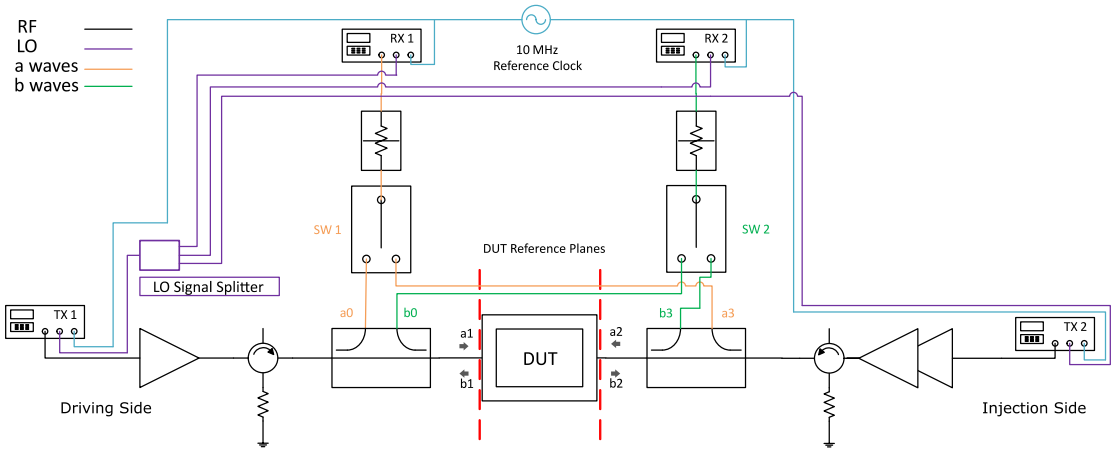

Figure 8. The block diagram of the active load-pull system.

2.2.2.1 Signal Generators

For signal generation, a RF NI 5793 transmitter was used on each side, respectively. The transmitters have an operational frequency range from 200 MHz to 4.4 GHz with a bandwidth of 200 MHz and output power of 5 dBm. Their wide bandwidth makes them ideal for future wideband modulation load-pull measurements. The RF transmitters are using a direct conversion architecture by converting the baseband signal using an IQ

modulator directly to the modulated RF transmitted signal. The up-conversion by the IQ modulator can be achieved with an internal local oscillator (LO) or an external source. Exploiting this property, as it can be seen in Figure 8, the LO signal is generated internally in driving transmitter (TX1) and with the use of a power divider is routed to the injection transmitter (TX2) and the two RF receivers (RX1, RX2). Also, a clock input is used from the chassis providing the 10 MHz reference clock which is used to synchronize the digital electronic controls for the digital to analog converters (DAC) inside the RF transmitter modules.

2.2.2.2 Pre- Amplifiers

Pre- Amplifiers are used at each side to bring the driving and injection signal to the appropriate power levels. At the driving side, an APO/040-4032 was used, i.e. an RF amplifier with a frequency range from 2 to 4 GHz, a gain of 32 dB, a gain flatness of ± 1.75 dB, a noise figure of 8 dB and output power of 40 dBm. At the injection side, two pre-amplifiers are used. The Mini-circuits ZKL-2+, with 33 dB gain and 15 dBm output power and the Marconi 6201B G, with 40 dB gain and 45 dBm output power.

2.2.2.3 Isolators

Immediately after the pre-amplifiers, isolators are used at both sides. Figure 9 shows the driving and the injection side isolators. Their role is essential; they prohibit the transmission of signal in the backward direction towards the pre-amplifiers. Capable of providing more than 40 dB of reverse isolation and dissipating up to 50 dBm of power, they are used to protect the transmitters and to keep the presented impedance constant at $Z_0 = 50$ Ohms. If the system did not have the isolators, the reflected waves from the DUT, especially the ones form the injection side, would create an equivalent load-pull effect to the preamplifiers and influence their performance. The isolators are enclosed by metallic cases to prevent radiated RF which may create interference by coupling into other system components. For the isolator at the injection side, a custom-made heat sink is added to allow for heat dissipation due to the high power levels that are present in this part of the system.

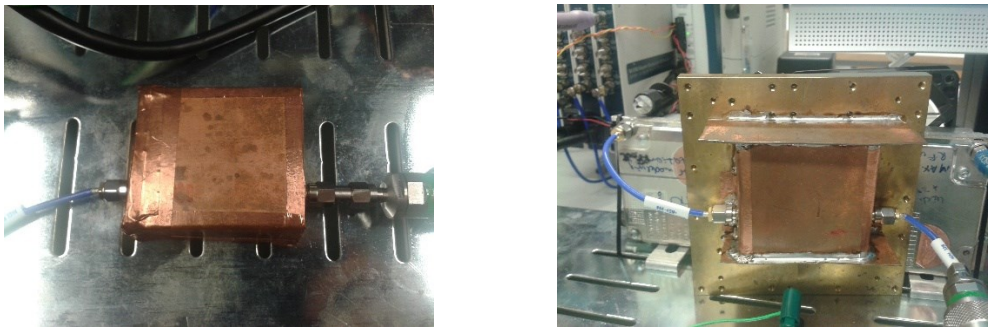

Figure 9. The driving side (left) and the injection side (right) isolators used for the system protection and impedance stabilization after the pre-amplifiers. The isolators are enclosed by metallic cases to prevent radiated RF. For the isolator at the injection side, a custom made heat-sink is added for heat dissipation due to the high power levels on that side.

2.2.2.4 Directional Couplers

The next components after the isolators, as can be seen in Figure 8, are the directional couplers. The Mini-circuits ZGBDC10-362HP+ directional couplers, with 10 dB coupling were used. The role of the directional couplers is to separate the forward and reverse signal i.e. the a_1, b_1 and a_2, b_2 traveling waves. By using couplers, four separate signals (traveling waves) are extracted and directed to the receivers. The separate outputs allow the measurement and calculation of the ratios of a and b waves and thus the corresponding reflection coefficients. The couplers can handle up to 250 Watts of power and they present low insertion loss of 0.18 dB and directivity of 22 dB. The outputs of the couplers are followed by attenuators regulating the power levels of the wave signals to the appropriate power levels for the switch arrays. A total attenuation of 18 dB and 30 dB was inserted for the driving and injection side, respectively.

2.2.2.5 Switch Arrays

The use of switches in an active load-pull setup is not a common solution. The common method for most active load-pull systems is to employ four receivers to detect the four traveling waves from the outputs of the couplers. In this system, only two receivers were available which introduced the need to route the four signals to the two receivers. This problem can be solved by using single pole double throw (SPDT) switches that direct a, and b waves. The connection of the switch arrays is shown in Figure 10. When the switch arrays are set for transmission form port 1 (P1), the a_0 and b_0 waves are detected. When they are set from port 2 (P2), the a_3 and b_3 waves are detected. The a_0, b_0 and a_3, b_3 waves are uncalibrated waves, i.e. they are in the plane between the couplers and the switch arrays. They are denoted with this specific notation so they can be differentiated from the calibrated waves, i.e. the waves in the DUT reference plane, which are denoted a_1, a_2 and b_1, b_2. All of these waves and planes are illustrated in Figure 8.

The introduction of switches into the system, even if it reduces the cost by using only two receivers, creates an isolation problem. The isolation is defined as the magnitude of a signal that gets coupled across an open circuit to other paths. The level of the necessary isolation depends highly on the DUT gain. Insufficient isolation levels affect mostly the b_1 and b_2 measurement accuracy and decreases also the dynamic range of the system. A simple example to illustrate this problem is this: Consider a DUT with 20 dB gain and a good matching on the input port with $|b_1|$ = -20 dB. The DUT is driven with a signal of 0 dBm, creating an output with $|b_2|$ = 20 dBm. If the switch isolation is 40 dB the influence of b_2 on b_1 is 100% and the depending on the phase of the two signals the combination can be constructive or destructive creating wrong measurement data. An addition of 20-30 dB of extra isolation is necessary so the effect of b_2 on b_1 is insignificant. For the design of this system a minimum level of isolation was set at 80 dB. Each switch has limited isolation between P1 and P2. In order to increase the isolation, cascaded switches in series are used as shown in Figure 10, i.e. creating a 2-stage switch array. The benefit of the switch arrays is that they add up the isolation level of each switch element.

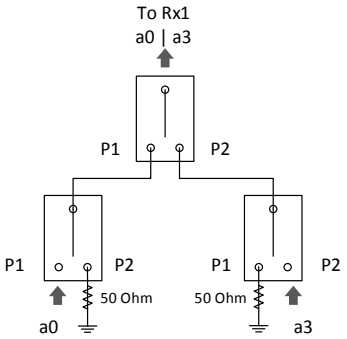

Figure 10. The switch array (SW1) of the drive side. The switch array is connected to the two couplers and routes the a waves to TX1. Each switch element has 45 dB isolation between P1 and P2, adding up to 90 dB of total isolation. The same architecture is used and in the injection side, where the b waves are routed.

The configuration relies on 50 Ω termination of the unused ports in the first stage elements. When the switch is set at P1, the a_0 wave can pass through the switch array from the 1st and 2nd stage with very low losses. At the same time at, P2 of the 2nd stage is matched, improving the total isolation. The same principle also applies in the case of routing the signal from P2 accordingly.

For the construction of the 2 necessary switch arrays, the Mini-circuits ZX80-DR230-S+ and Macom MASW-008543 were used. They provide 50 dB and 55db of isolation from common port and P1/P2, respectively. The Macom MASW-008543 was provided as an IC package and the design and implementation of a functional switch was required. A basic layout providing the bias circuitry and RF connectors was designed. The assembled switch is shown in Figure 11. In total, four of these were fabricated for the two 1st stages of the arrays.

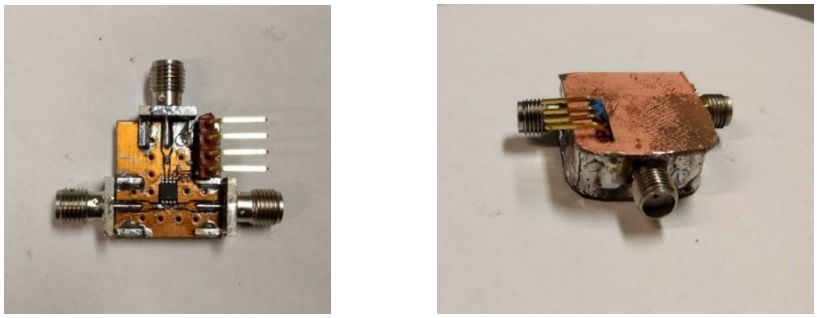

Figure 11. The assembled switch (left) and the final component (right) after the addition of a metal casing for isolation from RF radiation coupling.

The measurement results of the switch array are presented in Figure 12. These plots show the signal received at RX1, when the SW1 is set to P1 and when it is set to P2. During the measurement, the a_0 wave is 0 and the a_3 wave is at its maximum level. At P1, the only detected signal is the leakage from port 2 to port 1. The control of the switch arrays is done through digital input/output ports from the TX1 and TX2 with a minimum switching time between ports of 2 μs. The final performance of the switch arrays was satisfactory by achieving more than 90 dB of isolation between port positions.

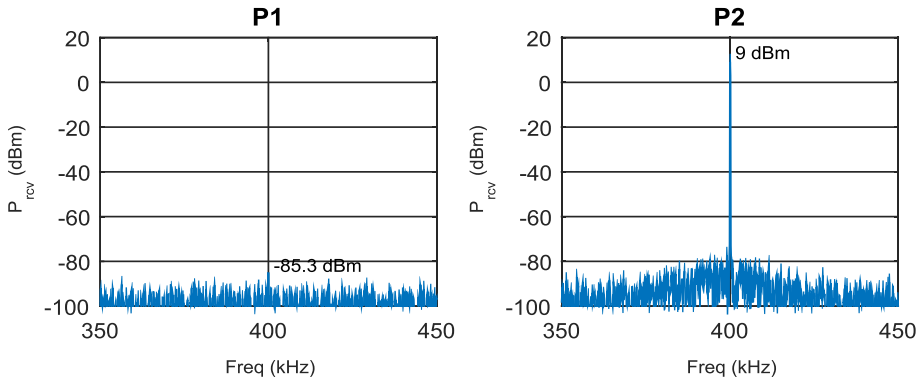

Figure 12. Plots of the signal received from RX1, when the SW1 is set to P1 (left) and P2 (right). During the measurement, the a_0 wave is 0 and the a_3 wave is at its maximum level. When SW1 is set to P1, the only detected signal is the leakage from port 2 to port 1. When SW1 is set to P2, the a_3 wave passes through the switch to RX1.

2.2.2.6 Signal detection

For the signal detection, two RF NI 5792 receivers were used. The receivers use also the same direct conversion architecture as the transmitters. The receivers have an operational frequency range from 200 MHz to 4.4 GHz with a bandwidth of 200 MHz and maximum P_{in} of 20 dBm. The receiver module allows the use of an external LO signal source, similarly to the transmitters, thus making it possible to use the same LO signal generated from TX1 to the rest of the components TX2, RX1 and RX2.

2.2.2.7 Power supply unit

Finally, the last system component is the DC bias power supply unit (PSU) for the DUT biasing. As PSU the Agilent 6626A is used, which can provide DC measurement of voltage and current for the gate and drain bias of the DUT. The PSU is connected using a GBIP port to the main system computer and is controlled by the developed software during the measurements. The PSU provides the data required for determining the power consumption of the DUT.

2.2.3 System Software Design

For the design of the system software that controls the complete active load-pull setup, the development environment LabVIEW from National Instruments (NI) was used. The software application that was developed for the current system consists of the following basic function blocks in two main categories:

System Configuration and control

- The user control panel
- The initialization and control block of the NI 5792 and NI 5791 instrument modules
- The generation of the digitally synthesized signal block
- The signal transmission block
- The signal reception block

Active Load-Pull Control

- The Active load-pull control and data processing block

2.2.3.1 System Configuration and control

The user has the capability to operate the system through the control panel. In the control panel, all the necessary settings and inputs can be set and different types of measurement can be performed, such as load-pull for single or multiple input power levels or power sweeps for a constant load impedance. The control panel is shown in Figure 13. It consists of the system settings of the transmitters and receivers, the settings and status display of the impedance convergence algorithm and the measurement data displays. In the system settings, the user can specify the frequency at which the measurement will be performed, the sample rate and number of samples of the transmitted signal and the signal characteristics, i.e. the single tone frequency offset from the carrier, its phase and amplitude. Also the power levels of the input power and the maximum injected power and the impedance convergence algorithm operation can be set. In the measurement data displays, two smith charts present the measured data points of the load impedance and the reflection coefficient (right chart) and their corresponding input reflection coefficient (left chart) and all the measurement elements for each point such as gain, efficiency and output power.

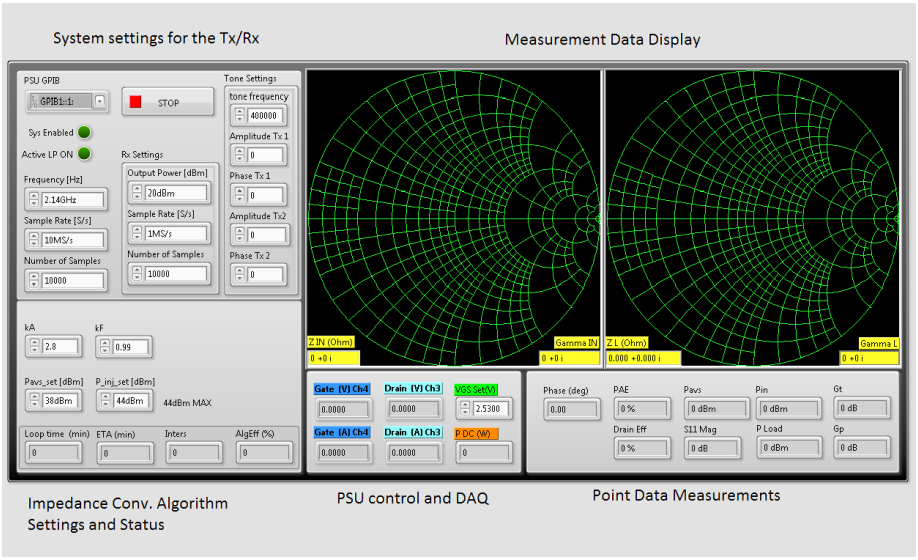

Figure 13. The control panel of the load-pull system, implemented in the LabVIEW environment. The panel is divided in sections consisting of the system settings, convergence algorithm setting, PSU control and data displays.

The initialization and control block of the NI 5792 and NI 5791 instrument modules makes use of code blocks from the internal LabVIEW libraries. The block contains functions that handle the necessary operations for setting the clocks, the signal routes, triggering and data acquisition. The same function block is used for the two transmitters and the two receivers. The block turns on initially the device and checks the current status of it. Next, the LO signals are routed accordingly from the internal LO of TX1 to the rest of the modules. The modules clocks are set to use their internal clocks which are synchronized with a Phase-locked loop (PPL) using as a reference the 10 MHz reference clock of the chassis and the carrier frequency is set. The rest of the final configuration settings, regard the trigger setting (for device synchronization proposes) and the data streaming from the modules to the host computer.

A digitally synthesized signal was implemented for each transmitter. The purpose of that signal is to create an offset from the carrier frequency in order move away from the LO leakage with its associated phase noise and utilize a part of the spectrum with minimum noise. This action increases the dynamic range of the measurement setup by more than 30 dB. The effect can be seen in the spectrum plot of RX1 and RX2 in Figure 14. The figure shows the frequency offset spectrum from the carrier frequency of 2.14 GHz for a span of 1 MHz when no incoming signal is present. In the center of the plot, the detected peak corresponds to the leaked power from the LO. Different spurs are detected with lower power levels at 50 kHz and 310 kHz. A suitable area with minimum noise was selected to be at 400 kHz offset from the carrier frequency. For this purpose, a digitally synthesized signal was generated with an offset frequency of 400 kHz.

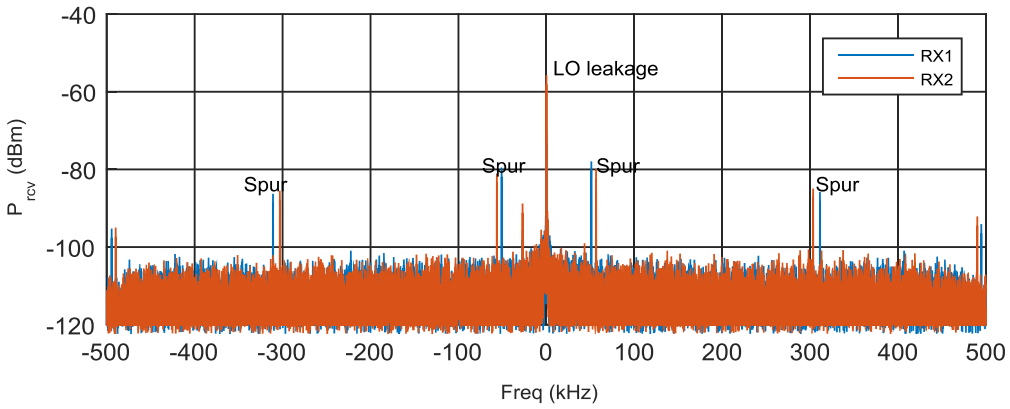

Figure 14. The spectrum plot of RX1 and RX2 as received when no signal generation is active. At the center, with the highest peak is present the LO leakage with -58 dBm power. Spurs are detected with lower power levels at 50 kHz and 310 kHz.

The generation of the digitally synthesized signal block consists of a continuously running loop where two single tone orthogonal sinusoidal signals (I and Q components of the signal) are generated for each transmitter, TX1 (driver signal) and TX2 (injection signal). The number of samples was chosen to be 10000 samples as a default value with a sample rate of 10 MS/s. Both of the signals have the same frequency offset of 400 kHz but the amplitude and phase of the two signals can be adjusted separately. The amplitude of the TX1 signal is set according to the desired power level of the measurement and its phase is by default zero. The amplitude and phase of the TX2 signal cam be adjusted manually or by the impedance convergence algorithm, which is described later. The generated signals, in I/Q form, are feed directly to the signal transmission block. The signal transmission block handles the data transfer from the host computer to the memory buffers of the transmitter modules, where they are transmitted continuously in repeat mode.

As the signals are transmitted, the signal reception block is ready to capture the received signals from the receivers RX1 (a waves) and RX2 (b waves). The block consists of a continuously running loop where the data acquisition function transfers the data from the receiver modules to the host computer and performs a Fourier transform of the time domain signals to the frequency domain. A signal peak detection function is used to detect the signal peaks and the extract the amplitude and phase information.

2.2.3.2 Active Load-Pull Control

The Active load-pull control and data process block is the main function block, controlling all the essential operations for the active load-pull, and is consisted of:

- The switch control
- The PSU data acquisition (DAQ)
- The data calibration
- The absolute power calibration
- The impedance convergence algorithm
- The data display and export function

Switch control and PSU DAQ

The switch control is achieved by utilizing the digital I/O ports of the TX1 and TX2. The switches are controlled with a 5V or 0V signal for the P1 and P2 accordingly. This control can be implemented with a digital HI or LOW and controlled from the VI. The switching speed between P1 and P2 is set at 30 ms in order to provide enough settling time between transitions.

The PSU data acquisition function is provided by the LabVIEW internal library and is used to establish data communication through the GBIP port with the Agilent 6626A PSU. The function reads the data from the two utilized channels and measures the DUT's gate and drain voltage and current values. From this data, it calculates the DC power consumption.

Data calibration

The data calibration is responsible for the application of the calibration functions to transform the raw acquired data to calibrated data represented at the DUT reference plane. The calibration method used is based on a combination of 1 port 3-term and 2 port 8-term error models used for the calibration of network analyzers [26] . The method makes use of a standard calibration procedure using a short, open, load and through (SOLT) calibration standards. The method creates seven error correction factors by solving a set of linear equations which are functions of the measured and the standards S-parameter values.

The first three error correction factors, e_{00}, e_{11} and Δ_x are found by solving the set of 3 linear equations with 3 unknowns for Port 1 (driver side) as follows:

$$e00 + \Gamma_{short}\,\Gamma_{short,M1} e11 - \Gamma_{short}\Delta_e = \Gamma_{short,M1} \quad (7)$$

$$e00 + \Gamma_{open}\,\Gamma_{open,M1}\, e11 - \Gamma_{open}\Delta_e = \Gamma_{open,M1} \quad (8)$$

$$e00 + \Gamma_{load}\,\Gamma_{load,M1}\, e11 - \Gamma_{load}\Delta_e = \Gamma_{load,M1} \quad (9)$$

The same procedure is applied also in Port 2 (injection side) for the next 3 error correction factors, e_{33}, e_{22} and Δ_y:

$$e33 + \Gamma_{short}\,\Gamma_{short,M2}\, e22 - \Gamma_{short}\Delta_y = \Gamma_{short,M2} \quad (10)$$

$$e33 + \Gamma_{open}\,\Gamma_{open,M2}\, e22 - \Gamma_{open}\Delta_y = \Gamma_{open,M2} \quad (11)$$

$$e33 + \Gamma_{load}\,\Gamma_{load,M2}\, e22 - \Gamma_{load}\Delta_y = \Gamma_{load,M2} \quad (12)$$

where, $\Gamma_{(short,open,load)}$ are the calibration standards values and

$$\Gamma_{(short,open,load)M1} = \frac{b_0}{a_0} \tag{13}$$

the measured reflection coefficients of the calibration standards at Port 1 and

$$\Gamma_{(short,open,load)M2} = \frac{b_3}{a_3} \tag{14}$$

the measured reflection coefficients of the calibration standards at Port 2. The last error correction factor is the k and is calculated as:

$$k = \frac{S_{21}\left(b_3/a_3\right)e_{22} - S_{21}\left(b_3/a_0\right)\Delta_y}{\left(b_3/a_0\right) - S_{11}\left(b_3/a_0\right)\ e_{11}} \tag{15}$$

where, S21 and S11 are the S- parameters of the through calibration standard. The seven error correction factors are used to construct the transformation matrix **T** as follows:

$$T = \begin{bmatrix} T_1 & T_2 \\ T_3 & T_4 \end{bmatrix} \tag{16}$$

with

$$T_1 = \begin{bmatrix} -\Delta_x & 0 \\ 0 & -k\Delta_y \end{bmatrix} \qquad T_2 = \begin{bmatrix} e_{00} & 0 \\ 0 & ke_{33} \end{bmatrix} \tag{17}$$

$$T_3 = \begin{bmatrix} -e_{11} & 0 \\ 0 & -ke_{22} \end{bmatrix} \qquad T_4 = \begin{bmatrix} 1 & 0 \\ 0 & k \end{bmatrix}$$

After the T matrix is complete it can be used to correct the measured waves a_0, b_0 and a_3, b_3 by transforming them to the actual values of the DUT reference plane a_1, b_1 and a_2, b_2 using the relation:

$$\begin{bmatrix} a_1 \\ a_2 \\ b_1 \\ b_2 \end{bmatrix} = T^{-1} \begin{bmatrix} b_0 \\ b_3 \\ a_0 \\ a_3 \end{bmatrix} \tag{18}$$

The absolute power calibration implements the power correction functions on the measured wave amplitudes and exports the calibrated absolute power levels, gain and efficiency.

For the input power to the DUT the P_{avs} is calculated as:

$$P_{avs} = |a_0|^2 A_1 \tag{19}$$

where A1 is the input power correction factor and is calculated by measuring the power level with a 50 Ω power meter at the Port 1 DUT reference plane. Then the power that goes in to the DUT Pin is calculated as:

$$P_{in} = P_{avs} \frac{1 - |\Gamma_{IN}|^2}{1 - |\Gamma_{IN} e_{11}|^2} \tag{20}$$

The output power from the DUT is accordingly calculated as the power available from the network (P_{avn}):

$$P_{avn} = |b_3|^2 A_2 \tag{21}$$

where A2 is output power correction factor and is calculated by connecting a known through between Port 1 and Port 2 and equating the corrected P_{avs} with the measured P_{avn}. Finally, the power delivered to the load (PL) calculated as:

$$P_L = P_{avn} \frac{1 - |\Gamma_L|^2}{1 - |\Gamma_L e_{22}|^2} \quad (22)$$

The transducer gain (Gt) then calculated as:

$$G_T = \frac{P_L}{P_{avs}} \quad (23)$$

and the operational gain (G_p) as:

$$G_p = \frac{P_L}{P_{in}} \quad (24)$$

Finally, the PAE and η calculated as:

$$PAE = \frac{P_L - P_{in}}{P_{DC}} 100 \quad (25)$$

$$\eta = \frac{P_L}{P_{DC}} 100 \quad (26)$$

Impedance convergence algorithm

The impedance convergence algorithm is an iterative function and performs the most essential operation of the software. Its purpose is to control the amplitude and phase of the injected signal (a_1) in order to present the predefined load impedances and their corresponding reflection coefficients to the DUT. The algorithm is based on the simple difference minimization between the amplitude and phase of the current presented load reflection coefficient ($\Gamma_{L,\,i}$) and the defined value of the desired load reflection coefficient ($\Gamma_{L,\,set}$). The function operates by normalizing the $\Gamma_{L,\,i}$ and $\Gamma_{L,\,set}$ to the system impedance coefficient Γ_{system} which can be a non 50 Ω complex value. The normalization is done as:

$$\Gamma_{L,set,norm} = \frac{\left(\frac{1+\Gamma_{L,set}}{1-\Gamma_{L,set}}\right) 50 - \Gamma_{system}}{\left(\frac{1+\Gamma_{L,set}}{1-\Gamma_{L,set}}\right) 50 + \Gamma_{system}} \quad (27)$$

and

$$\Gamma_{L,i,norm} = \frac{\left(\frac{1+\Gamma_{L,i}}{1-\Gamma_{L,i}}\right) 50 - \Gamma_{system}}{\left(\frac{1+\Gamma_{L,i}}{1-\Gamma_{L,i}}\right) 50 + \Gamma_{system}} \quad (28)$$

Then the normalized values used as a function of the amplitude and phase of the injection signal transmitter according to the equations:

$$A_{TX2,i} = \left[\left(|\Gamma_{L,set,norm}| - |\Gamma_{L,i,norm}|\right)k_A\right] + A_{TX2,(i-1)} \quad (29)$$

$$F_{TX2,i} = \left[\left(angle(\Gamma_{L,set,norm}) - angle(\Gamma_{L,i,norm})\right)k_F\right] + F_{TX2,(i-1)} \quad (30)$$

where k_A and k_F are the step constants depended from the DUT and its bias conditions and they found empirically. The function runs iteratively and at each iteration minimizes the distance between the current value and the set value. The convergence termination criterion is set at amplitude difference < 0.01 and phase difference $<0.3^{o}$.

The performance of this convergence algorithm quantified in terms of its efficient use of the load-pull system. An ideal system, with 100% efficiency, would require only one measurement per impedance point. The algorithm presents high efficiency of the order 20-50 % corresponding to 40-100 measurement points per minute.

2.2.3.3 S parameters measurements

A software version dedicated to make use of the hardware for S parameters measurements, as a Network vector analyzer (VNA), was also developed. For this operation mode, no physical changes in the hardware were necessary and only changes in some of the software code blocks were made. All the previous system configuration and control VIs were reused and a new VI for the VNA control was created. The injected signals on both ports was set to have the same number of samples and sample rate. The signal power was set at -10 dBm on both ports. The main software difference was the data calibration function. For the calibration of the data was used the 2 port 8-term error correction model with switch-term correction.

The system can measure S parameter on 2 port components at a single frequency This operation mode was developed to act as an intermediate development step of the active load-pull system, due to the many similarities between the two system basic operation principles as well as it provides a verification method for the data calibration function.

2.2.4 System Verification

After the system was developed, a set of verification measurements was performed. The verification of measurement data integrity and accuracy is based on the comparison of measurement results from the system, in active load-pull and VNA operation mode, with simulation results of simple, well-known, passive elements. The basic principle relies on the fact that the simulation model of such passive devices, which in this case was a set of transmission lines with different electric length, is very accurate and can simulate the behavior of them precisely.

Figure 15. Verification transmission lines with 4 electric length sizes, TL1, TL2, TL3 and TL4 with lengths of 20, 23, 27 and 50 mm respectively.

A set of 50 Ω transmission lines with different electrical lengths, fabricated on Rogers duroid 5870 substrate, were used for the verification of the measurements. The transmission lines, TL1-4 with lengths of 20, 23, 27 and 50 mm respectively, are shown in Figure 15. One verification measurement was performed for the active load-pull operation mode and one for the VNA operation mode. For the active load-pull mode verification, a load-pull measurement of the 20mm transmission line was done over the whole smith chart and a load-pull simulation in ADS with exactly identical settings was performed for comparison. The measurement results are shown in the plot of Figure 16 for the G_T measurements and in Figure 17 for the P_L measurements. The plots consists of the simulation data (continuous lines) and measured data (dashed lines) for constant gain and power levels. The P_{avs} of the measurements was set to 0 dBm and the frequency was 2.14 GHz. The error between the measurement and simulation results varies with $|\Gamma_L|$. As can be seen also in the plots, there is a shift of the gain and power circle contour centers from the smith chart center with is caused by the non-50 Ω system impedance of the driving port. The gain error and the power error are defined as:

$$e_{gain} = \left|G_{T,Sim} - G_{T,Meas}\right| \, dB \; for \; each \; \Gamma_L \tag{31}$$

$$e_{power} = \left|P_{L,Sim} - P_{L,Meas}\right| \, dBm \; for \; each \; \Gamma_L \tag{32}$$

where Γ_L can be any value on the smith chart. The gain error varies from 0 dB to 1.2 dB and the power error from 0 to 1.6 dBm. The error magnitudes increase with the magnitude of Γ_L and they reach their highest values at the edges of the smith chart. These measurements show the system accuracy levels for the power and gain measurements in the load-pull operation mode.

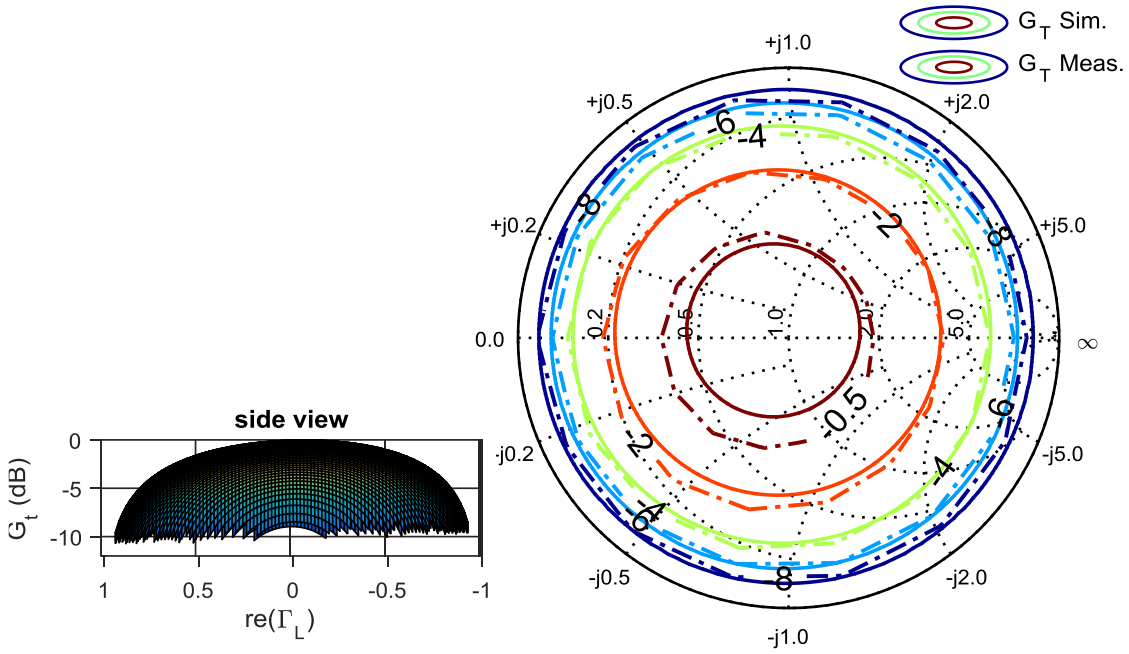

Figure 16. Measurement results for the transducer gain (G_T) from the simulation data (continuous lines) and measured data (dashed lines) for constant gain levels. The constant gain levels are for -8, -6, -4 -2 and -0.5 dB. The P_{avs} of the measurements was set to 0 dBm and the frequency was 2.14 GHz. The error between the measurement and simulation results varies from 0 to 1.6 dBm

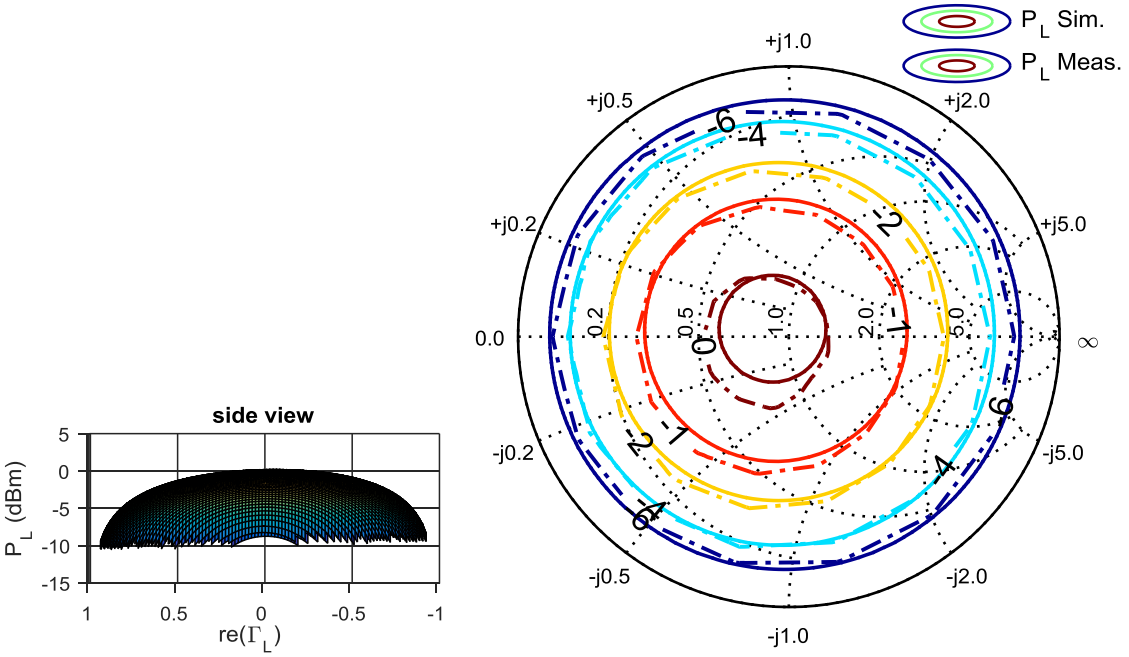

Figure 17. Measurement results for the power delivered to the load (P_L) from the simulation data (continuous lines) and measured data (dashed lines) for constant power levels. The constant power levels are for -6, -4 -2, -1 and -0 dBm. The P_{avs} of the measurements was set to 0 dBm and the frequency was 2.14 GHz. The error between the measurement and simulation results varies from 0 to 1.2 dB.

For the VNA operation mode, the S parameters of the transmission lines were measured and simulated accordingly at 2.14 GHz. The results for the simulation data are presented in Table 1 and for the measured data in Table 2.

Table 1. Simulation data for the S parameters of the verification transmison lines.

Simulation Data	S_{11} (dB∠ deg)	S_{12} (dB∠ deg)	S_{21}(dB∠ deg)	S_{22} (dB∠ deg)
TL1	-53 ∠-14.5	-0.023 ∠-71.8	-0.023 ∠-71.8	-53 ∠-14.5
TL2	-52 ∠-25.5	-0.026 ∠-82.6	-0.026 ∠ -82.6	-52 ∠ -25.5
TL3	-52 ∠-39.5	-0.031 ∠-97.0	-0.031 ∠ -97.0	-52 ∠ -39.5
TL4	-53 ∠-76.9	-0.057 ∠-179.6	-0.057 ∠ -179.6	-53 ∠ -76.9

Table 2. Measurement data for the S parameters of the verification transmison lines.

Measurement Data	S_{11} (dB∠ deg)	S_{12} (dB∠ deg)	S_{21}(dB∠ deg)	S_{22} (dB∠ deg)
TL1	-36 ∠-31.6	-0.129 ∠ -72.5	-0.060 ∠ -72.6	-41 ∠-31.6
TL2	-38 ∠ -20.4	-0.125 ∠ -83.1	-0.058 ∠ -83.3	-37 ∠ -35.7
TL3	-33 ∠ -44.3	-0.112 ∠ -97.7	-0.081 ∠ -97.7	-35 ∠ -14.5
TL4	-32 ∠ -85.1	-0.178 ∠ -179.5	-0.132 ∠ -179.2	-33 ∠ -108.6

Both of the measurements show the good match of the transmission line, as expected, on port 1 and 2 as it can be seen from S_{11} and S_{22} in Table 1 and Table 2. The most important measurement results is that phase measurement of the S_{12} and S_{21} agree very well with a maximum error of $+0.7^{o}$, which indicates an excellent accuracy. The amplitude of S_{12} and S_{21} contains a larger error but within the expected levels of accuracy of power and gain measurement.

A verification measurement was performed for the active load-pull operation mode using an active device. The verification of the power and efficiency measurements was done in power sweep mode. The active device was a power amplifier using the Cree CGH40006P, a 6 W RF Power GaN HEMT, mounted on a demonstration test board CGH40006P-AMP. The test board datasheet contains measurements of transducer gain and drain efficiency versus output power for default bias conditions [27]. A measurement of a power sweeps under the exact same bias conditions and with a presented load impedance of 50 Ω was made to illustrate the accuracy of the system. The results for the gain and drain efficiency are shown in the plots of Figure 18 and Figure 19.

The results show a good level of reproduction accuracy in gain with maximum error of -0.4 dB and -4.5% in drain efficiency. Also, the results indicate a good level of system power calibration and system linearity at high power levels.

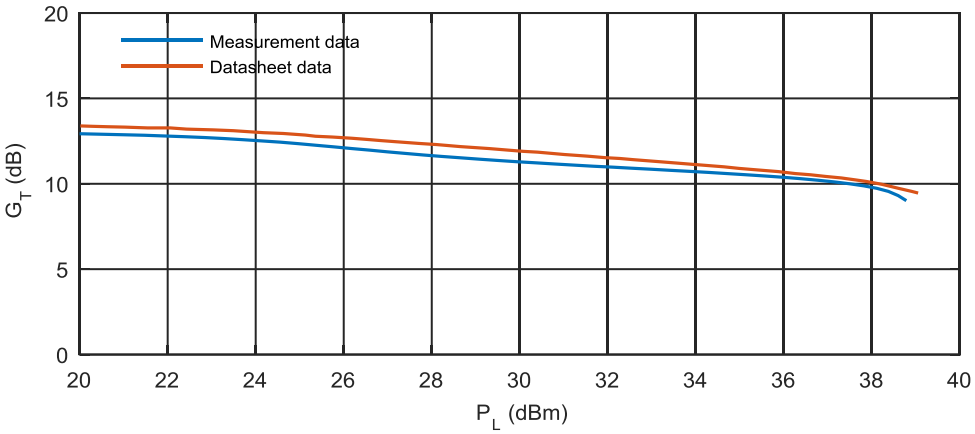

Figure 18. Comparison of the measured transducer gain (G_T) versus the delivered power (P_L), with the test amplifier datasheet measurment. The results show a good level of reproduction accuracy in gain with maximum error of -0.4 dB.

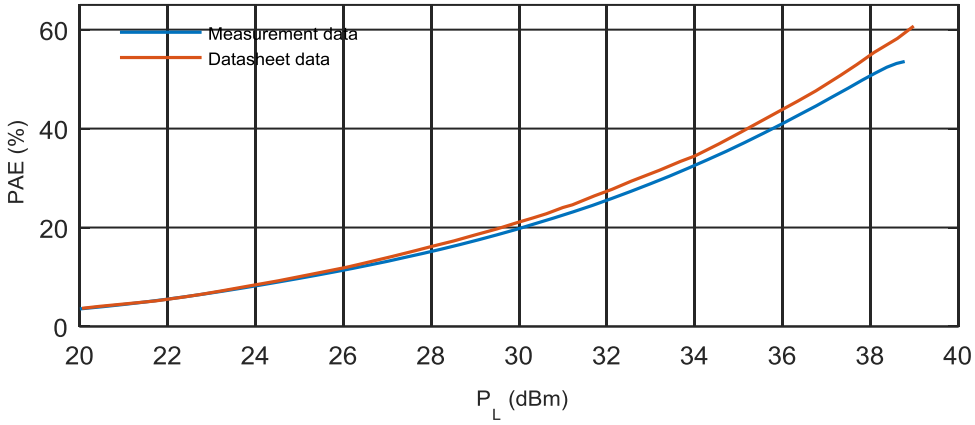

Figure 19. Comparison of the measured PAE versus the delivered power (P_L), with the test amplifier datasheet measurment. The results show a maximum error of -4.5%.

3 Designing a Doherty Power Amplifier

3.1 Fundamentals of Doherty power amplifiers

The importance of the DPA in the modern era of wireless communications is undeniably crucial because of the efficiency enhancement it can provide [3]. A number of publications describe and illustrate the principles of operation and the modern trends that has driven the evolution of this 80-years old idea [28, 29]. In this chapter, the fundamental principles of the DPA operation are briefly described. Extensive descriptions of DPAs have been given by Cripps et al. [6, 30, 31].

Figure 20 shows the basic DPA architecture in its simplest form. The DPA architecture consists of two devices, the *main device* and the *auxiliary device,* connected together in a specific way. The final maximum RF output power of the DPA is the combined power of both devices. The back-off efficiency is improved thanks to the principle of load modulation, where the load termination is modulated according to an efficiency optimal trajectory versus output power. The input signal is separated by an input power divider and is fed into the two devices. These two branches have a phase offset of 90-degrees. At low input power, the auxiliary device is off, i.e. not conducting any current, by being biased in class C operation. The main device, normally biased in class AB, is terminated with a load optimum for a back-off (BO) output power level. Beyond this power level, the auxiliary device starts to conduct. The injected output current from the auxiliary device modulates the load of the main device inversely promotional to the power, thanks to the quarter-wave transformer. At a maximum power level (full power - FP), both the main and auxiliary devices reach saturation. This results in the following efficiency versus output power of the DPA: one efficiency peak at BO and one efficiency peak at FP, with a single-ended class-AB efficiency profile up until BO and a small valley in between BO and FP.

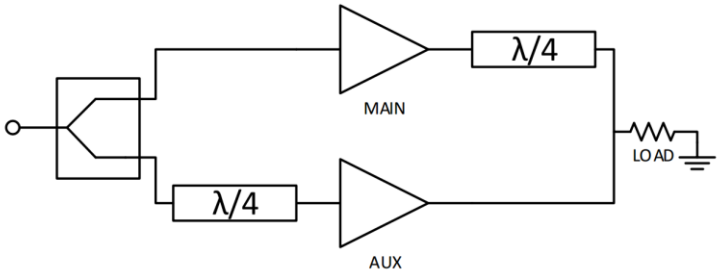

Figure 20. The basic DPA architecture in its simplest form. The DPA consists of a main and an auxiliary device. The input driving signal is split with a power divider and fed into the devices. A set of quarter-wave transformers are used in the input and output of the auxiliary and main devices, respectively.

The main drawback of the classical design approach is its non-linear behavior. Ideally, gain and phase responses of the DPA are linear. For real transistors, the DPA is non-linear due to parasitics. For real transistors the gain is often compressed to reach high efficiency. The phase in the high power region is very non-linear due load modulation, as consequence of the Miller effect [32-34].

In [7-9] a new design approach providing an improved efficiency and linearity tradeoff was presented. This method is built upon a generalization of the topology presented in [35, 36]. This generalization treats the output combiner network as a black-box reciprocal and lossless 3-port combiner with the third port terminated with a load. It also assumes the phase difference between the two branches to be arbitrary (θ), see Figure 21. The reciprocal and lossless 3-port combiner with the third port terminated with a load can be represented by a reciprocal and lossy 2-port combiner, where the load termination is included. This conversion simplifies derivation and analysis significantly. All network parameters are solved for presenting optimum impedances to both devices at BO and FP. Additionally, the black-box combiner approach can integrate matching networks into the combining network, which is very useful for practical designs.

In this work, the DPA design was based on the design approach in [7-9]. Details of this approach are discussed in more detail in the next session.

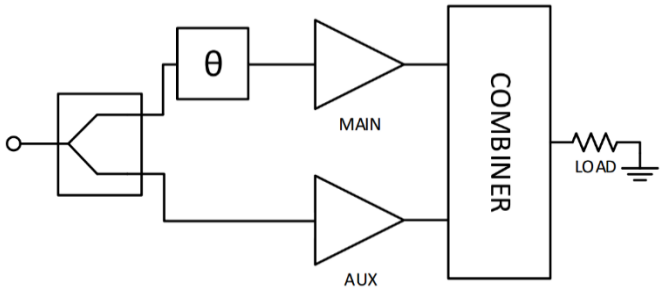

Figure 21. Block level schematic of the proposed DPA architecture according to [35, 36]. The DPA consists of the main and auxiliary devices. A power splitter feeds the driving signal into their inputs. A phase shifter (θ) is introduced before the auxiliary PA. At the output of the devices, a combiner network combines the outputs of the devices in an optimal way.

3.2 Doherty power amplifier design strategy

In this section, the design performance goals of the DPA are set first. After that, the design strategy steps are presented and explained.

3.2.1 Doherty power amplifier design goals

The target design goals were mainly focused on finding a good tradeoff between efficiency and linearity of the DPA. The DPA was designed to have symmetrical devices, i.e. same device sizes so the same test board design can be used for both of them, and to have equal split of the input power (- 3 dB) for high gain. The DPA was designed to operate at 2.14 GHz. The minimum output power goal was set to 17 W (≈42.3 dBm). The

maximum gain compression was aimed to be less than 1 dB and the phase distortion had to be less than 10^{o}.

3.2.2 Design strategy steps

The initial step was the design and fabrication of a development board (DB). The DB contained the device, which the DPA was based on, along with accompanying networks that handle the stabilization of the device, bias circuitry and second harmonic terminations. The DB formed a sub-circuit block of the final DPA design. This means that it is going to be placed in the final design as is, without the need of shifting reference planes. The design of the DB was completely based on model simulations using the ADS simulation suite.

After the DB was designed and fabricated, it was subjected to load-pull measurements. This step is crucial, as the measurement based design parameters of the final DPA will be based on these measurement data. By implementing this step, all the inaccuracies and errors generated from the simulation models of the device and the lumped components, are eliminated. The design accuracy will instead be set by the accuracy level of the active load-pull system. The active load-pull system described in Chapter 2 was used to perform the measurements. These measurements were used to characterize the DB in terms of gain, power, efficiency, and phase contours over areas of interest in the Smith chart, corresponding to scans of different load impedances. The black-box combiner parameters are functions of optimum impedances presented to the main and auxiliary devices at BO and FP. Thus, the DB is measured in four different states: as main device at BO, as main device at FP, as auxiliary device at FP and as auxiliary device at BO. The auxiliary device at BO is not conducting and can therefore be characterized by S-parameters, rather than load-pull data. The optimal values of the load impedances at the different stated are selected by making compromises between gain, gain compression, power, efficiency and phase distortion. As part of the characterization source terminations have to be selected. They are selected to be the conjugates of the input impendences. To summarize, the required data inputs for the combiner network parameters and the phase delay are:

- Optimal load impedances at full output power for the main ($Z_{opt,\ m,\ FP}$) and auxiliary ($Z_{opt,\ a,\ FP}$) device.
- Optimal load impedance at back-off for the main device ($Z_{opt,\ m,\ BO}$).
- The off state output impedance of the auxiliary device ($Z_{off,\ a}$).
- Source impedances for optimal input matching, for both devices ($Z_{s,\ m}$) and ($Z_{s,\ a}$).

With all these data, the DPA behavior, i.e. gain, gain compression, power, efficiency and phase distortion, can be calculated at BO and FP [7-9].

The acquisition process of the required data is described in Chapter 4. The output combiner S-parameters and the phase delay were calculated and realized according the method in [36]. Finally, the sub-circuits for the main and the auxiliary devices, the input power slitter, the phase shifter, the input matching networks and the combiner are put together, and the DPA design is completed.

4 Device characterization development board

In this chapter, the design of the development board is presented. First, designing and implementation considerations are presented and discussed. Then, load-pull measurement data of the development board are presented. Finally, measured load-pull data of the board is analyzed to find optimum DPA performance, and the required DPA design parameters are extracted.

4.1 Development board design

In this section, the design of the development board using simulations is presented. The model used for the device is provided by the vendor and the models for the lumped element components are from the Modelithics LCR library. For the distributed elements, such as the transmission lines, models from the ADS internal libraries were used along with EM co-simulations using the Momentum RF solver.

4.1.1 Devices and substrate

For the development board, the device Cree CGH40010 was selected. It is a 10 W unmatched gallium nitride (GaN) high electron mobility transistor (HEMT), which offers high efficiency and gain in the desired frequency range [37]. The flexibility of an unmatched transistor is required for the DPA design method in this work.

All circuit boards were made with the substrate Rogers 4350B. It has a low dielectric tolerance and low losses, making it suitable for the desired operation frequency. A version with dielectric thickness of 0.5 mm and silver coated copper conductor, with 17 µm thickness was selected. The technical specifications can be found in [38].

4.1.2 Stability network

The first step of the design process was to check the stability of the device. The device presented a very high gain and it was potentially unstable for frequencies below 7 GHz. In order to stabilize it, a stability network was placed at the input of the device. Unfortunately, unconditional stability for all frequencies resulted in great gain reduction. Therefore, the device is made unconditionally stable out-of-band and conditionally stable around the operational frequency. The topology of the implemented stability network is shown in Figure 22. The network acts as a band pass filter around the operational frequency.

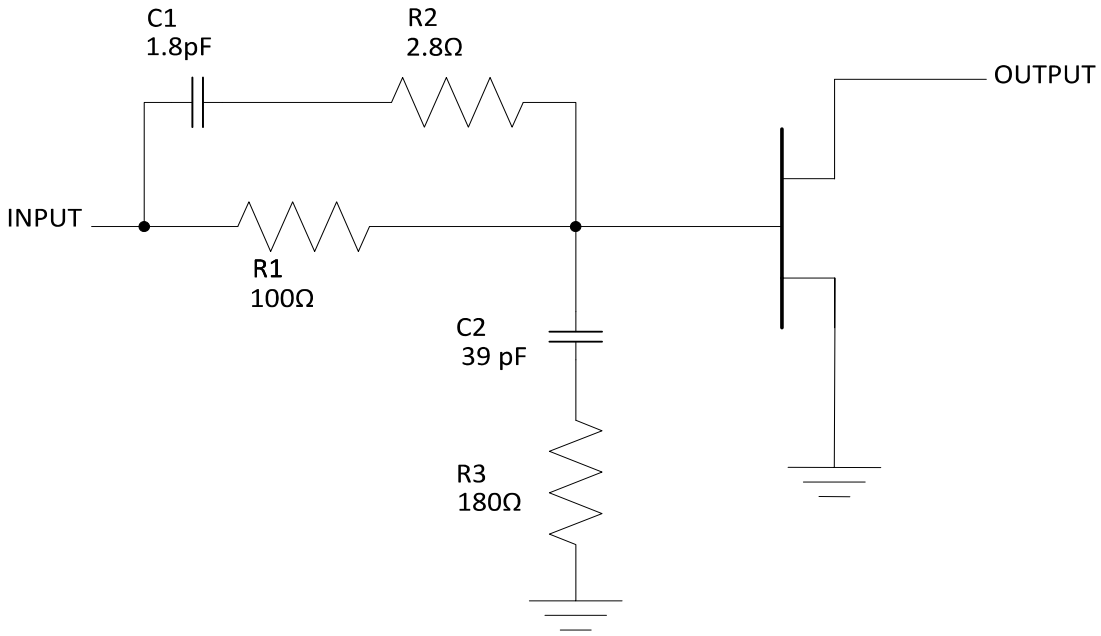

Figure 22. The topology of the stability network for the main device. The same topology is used for the auxiliary device with the only difference that R2 is changed to 5.1 Ω for unconditional stability.

Rollet's two-part stability factor (K and Δ) [39] for the stabilized device is presented in Figure 23. The condition K>1 and |Δ|<1 guarantees unconditionally stability. The stability factor expresses stability for one set of bias points. For large signals, it can be approximated that the device operates continuously along all sets of bias points in the load line. The figure presents the data of the worst case scenario from sweeps of all possible bias points. The stabilization network makes the device unconditionally stable out-of-band and conditionally stable around the operational frequency, as intended. For the worst case scenario, the K factor reaches the minimum value of 0.75. For the auxiliary device however, some optimal load impedances fall inside the unstable region. Increasing the resistance of R2 to 5.1 Ω in case of oscillation behavior solves this problem.

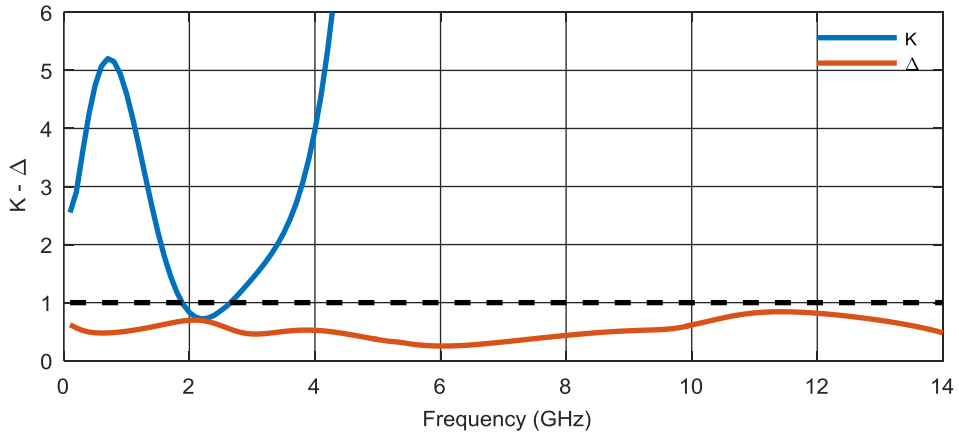

Figure 23. K- Δ stability simulations for the main device.

4.1.3 Harmonic terminations

The harmonic load and source termination are important design elements of power amplifiers, providing efficiency and gain enhancement [40]. Since the load-pull measurement system in this thesis does not employ harmonic control, second harmonics are terminated at the input and output of the development board. It is assumed that 3rd and higher harmonic terminations only have a minor influence on DPA performance. Optimal second harmonic terminations are extracted from load and source-pull simulations of the stabilized devices. In order to execute the simulations, some initial estimations regarding the bias voltages of the device had to be made for the main and auxiliary devices. At that point in the design process, it was not possible to specify the exact values of the gate bias voltages nor the fundamental load and source impedances. Therefore, they are estimated. The main device class AB bias was selected as V_{gs} = -2.9 V, with quiescent current I_q =100 mA. This bias level is selected for a maximally flat gain response. The auxiliary device class C bias was selected as V_{gs} = -6 V. The voltage was selected so the auxiliary device starts to conduct 8 dB backed-off from the maximum power of the main device.

Based on the previous voltage bias estimations an iterative series of 2nd harmonic load-pull and source-pull simulations were performed. The values of fundamental load and source reflection coefficients, used in the 2nd harmonic simulations, were selected from the fundamental simulations. The simulations were performed for the 3 states of the development board (see Section 3.2.2), the Main device operating at BO and FP and the auxiliary device operating at FP. The results from the 2nd harmonic simulations for Γ_L and Γ_{IN} at the 3 states are shown in Figure 24 and Figure 25.

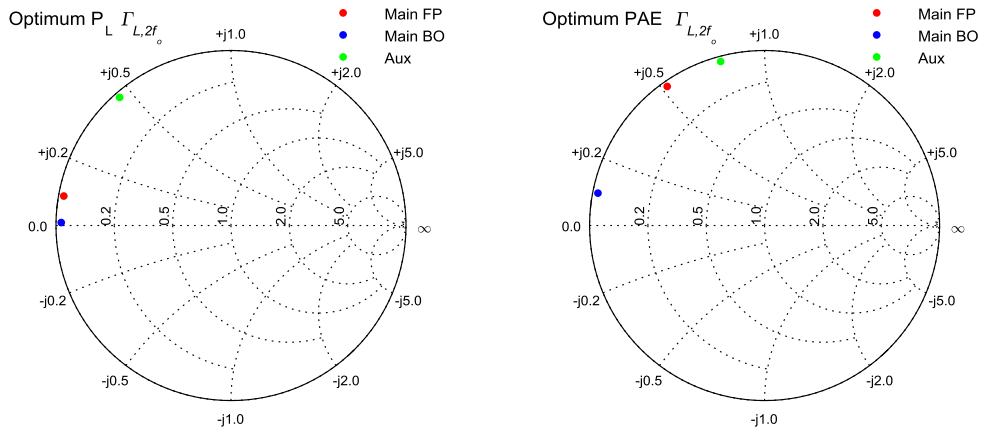

Figure 24. Plots of the optimum second harmonic load reflection coefficients ($\Gamma_{L,\,2f_0}$) with maximum P_L (left) and PAE (right) for the three states of the development board (main Full Power, main Back-off power and auxiliary at Full power). The optimum points are located at the edge of the smith chart at all cases but they have different angles varying from 120° to 180°.

Figure 24a shows the optimum load reflection coefficients for maximum P_L and Figure 24b for maximum PAE. As it can be seen from the plots, all Γ_L points are located near the edge of the smith chart but they have different $\angle\Gamma_L$. The values of $\angle\Gamma_L$ are different for P_L and PAE and they also show strong dependence on the amplifier state. The variance of P_L between states is 0.5 dB and while PAE changes 5%. A similar behavior is noticed for Γ_S. The results are shown in the Figure 25a for P_L and Figure 25b for PAE. The variance

between the optimum points is 0.2 dB for P_L and 2% for the PAE. The difference between the worst and best 2nd harmonic load termination is 2 dB and 20% for P_L and PAE respectively. For the source termination, the improvement is less significant, i.e. in the order of 0.3 dB for P_L and 3.5% for PAE.

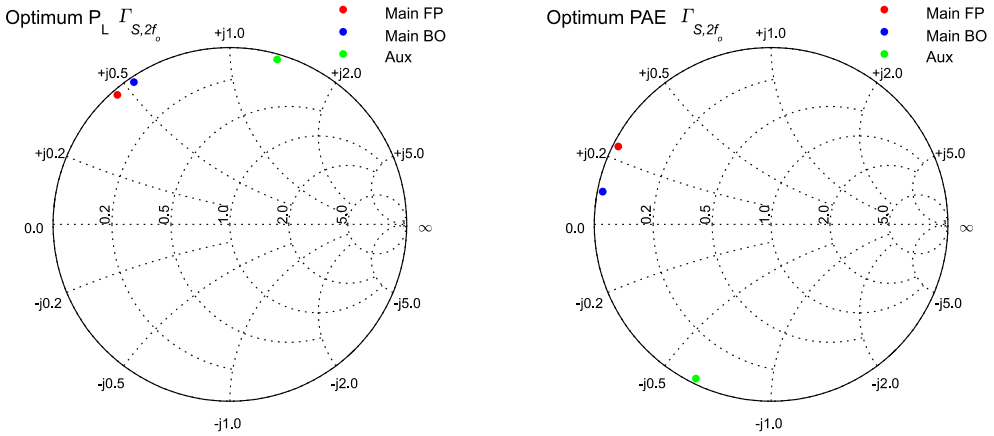

Figure 25. Plots of the optimum second harmonic input reflection coefficients ($\Gamma_{S,2fc}$) with maximum Γ_L (left) and PAE (right) for the three states of the development board (main Full Power, main Back-off power and auxiliary at Full power). The optimum points are located at the edge of the smith chart at all cases but they have different angles varying from 80° to 170°.

For simplification reasons, in the fabrication and measurement aspects, a single input and a single output 2nd harmonic termination network was designed for all of the 3 states. The selected values of Γ_L and Γ_S for the 2nd harmonic termination are shown in Figure 26. The values were selected in such a way that they present a good compromise between PL and PAE for all the 3 states.

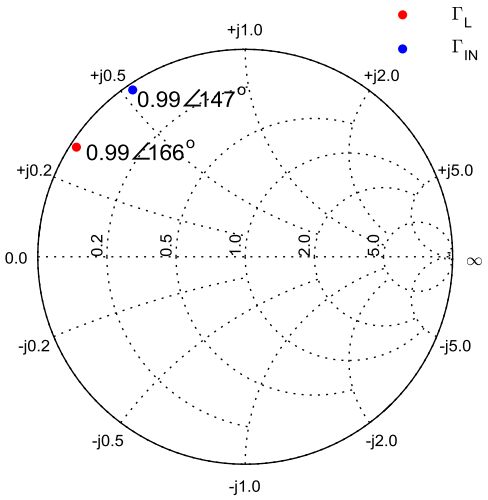

Figure 26. Plot of the selected optimum Γ_L and Γ_S values for the design of the 2nd harmonic termination networks, included in the development board. The values were selected for a good compromise between PL and PAE for the 3 different states the development board was tested (as Main device at FF, Main device at BO and as Auxiliary device at FP).

The 2nd harmonic terminations were design in such a way that they are not affected by any impedance changes caused by the fundamental frequency matching networks. Figure 27 shows the schematic of the implemented 2nd harmonic termination networks with the stabilized device. The networks are implemented using λ/4 open stubs with the appropriate rotation lines at the input and the output [41, 42]. The transmission lines electrical lengths are shown in the schematic below.

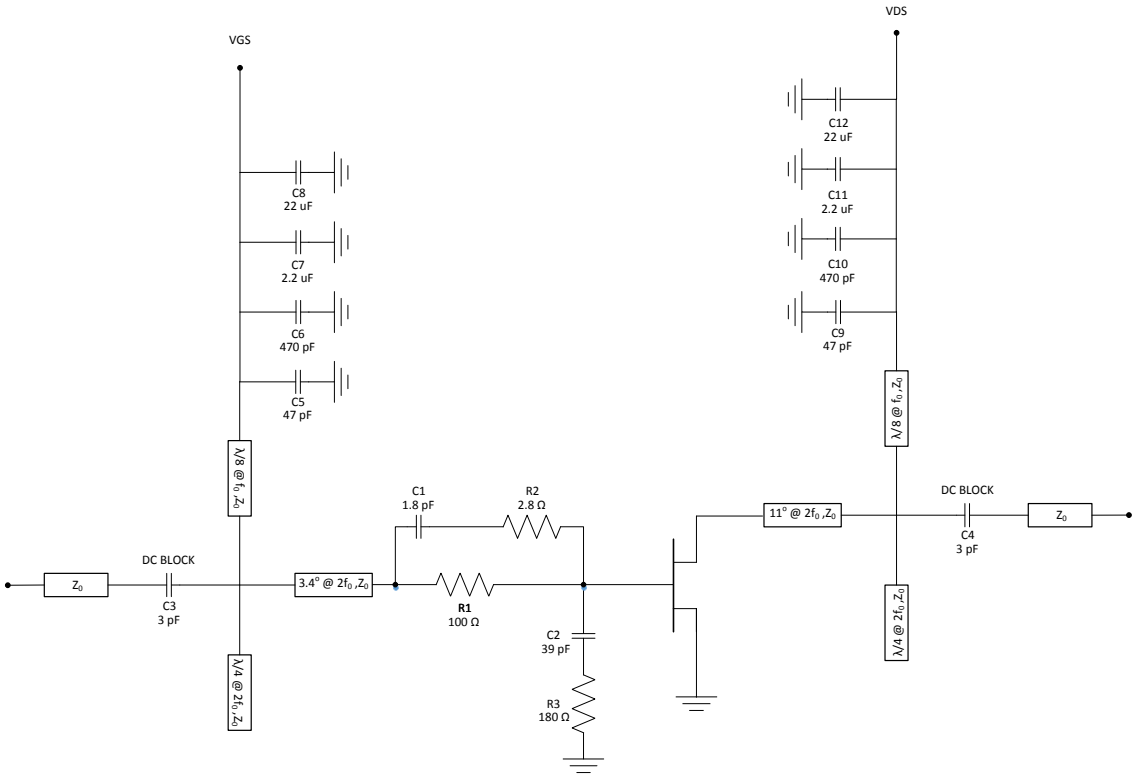

Figure 27. The complete schematic of the development board. The board includes the device with the stability network at its input, along with the 2nd harmonic terminations. The bias feed lines are integrated with the harmonic termination and include the capacitor arrays for the proper baseband termination. The board also includes DC block capacitors followed by 50 Ω (Z_0) transmission lines, thus making it suitable for measurements using the active load-pull system.

4.1.4 Bias feed and baseband terminations

The bias feed networks for the gate and drain of the device are shown in the schematic in Figure 27. The bias networks are integrated with the 2nd harmonic termination networks and they contain also baseband terminations [43]. The baseband termination designed to present baseband impedance Z_{BB} to the device output of less than 1 Ohm, from 10 kHz to 30 MHz. Series of parallel decoupling capacitors were placed on the bias, with increasing capacitance values. The simulation results of the baseband termination are shown in Figure 28.

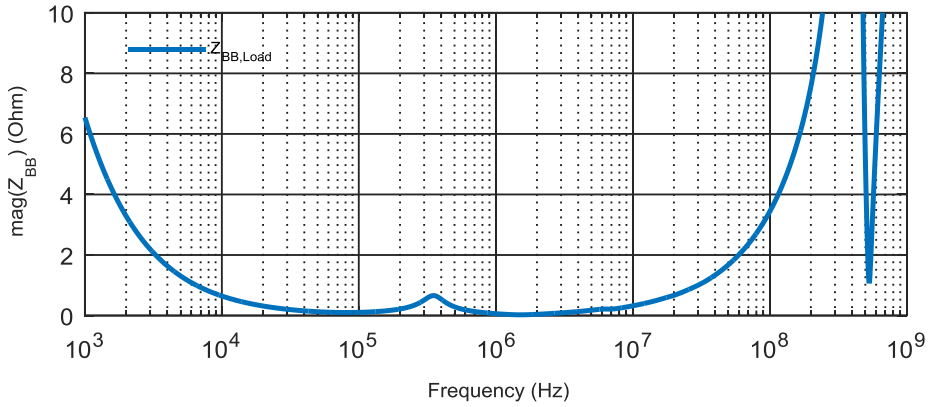

Figure 28. Plot of the magnitude of baseband load impedance $Z_{BB,\,Load}$ as seen from the device output as a function of frequency. The desired goal was set to be less than 1 Ω in the frequency range from 10 kHz to 30 MHz.

4.1.5 Fabrication Considerations

The development board is shown in Figure 29. During the assembly a reflow oven was used for the soldering process. A copper heat sink was added for proper cooling of the device and for mechanical stability. No connectors were attached for the RF connections due to the use of an external connection fixture (Anritsu, Universal Test Fixture UTF-3680 [44]). The reference plane of the measurements is located at the edges of the board as indicated with the red lines.

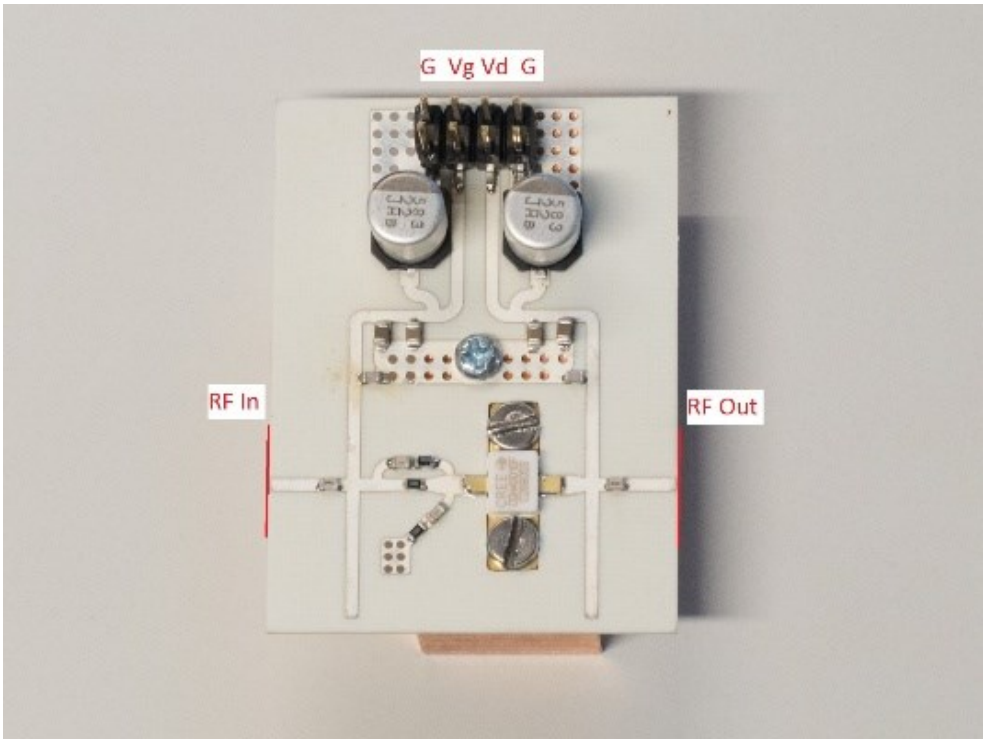

Figure 29. The fabricated development board. The figure shows the Main device configuration. The development board was also used for the Auxiliary device with the only design difference the stabilization resistor as described in Section 4.1.2.

4.2 Development board measurements

In this section the measurements of the development board are presented. For the characterization of the development board, a series of measurements using the active load-pull system were performed. Some aspects of the measurement considerations are discussed. The results of the DC and load-pull measurements are presented and analyzed.

4.2.1 Measurements considerations

A preliminary set of measurements was realized to locate the maximum power levels and their corresponding Γ_L points. With this information, the later measurements were focused on impedances and bias points of interest, saving large amounts of acquisition time. The characterization and post-processing was completed in four steps:

1. DC bias sweeps
2. Acquisition of raw load-pull data
3. Data transformations
4. Selection of optimum Γ_L points

All steps were performed once for the main device and once for the auxiliary device. The raw data from the load-pull measurements contained measured data points of P_L, G_T, PAE and voltage wave ratio (W_R). The voltage phase is defined as:

$$W_R = \frac{b_3}{a_0} \tag{33}$$

For the later use of the data, it was necessary to transform the W_R to the drain current phase (I_{ph}) for source impedances (Z_s), different from the system source impedance ($Z_{S,\,system}$). The $Z_{S,\,system}$ is constant, with a value close to 50 Ohm, and only depends on the impedance of the system components at the driving side. The reason for this transformation is that the method for the combiner design requires performance contours for a constant P_{avs} relative to a specific $\Gamma_{s,}$ as an input data. The relation between W_R and I_{ph} can be expressed as:

$$I_{ph} = \angle\left(W_R + \frac{1+\Gamma_L}{1+\Gamma_{IN}}\right) + \angle\left(\frac{Z_{IN}}{Z_{IN}+Z_S}\right) - \angle(Z_L) \tag{34}$$

The second transformation of the raw data that had to be done was the transform of P_{in} for different Z_s. The relation between P_{in} and P_{avs} is:

$$P_{avs} = \frac{P_{IN}\,|1-\Gamma_{IN}\Gamma_S|^2}{(1-|\Gamma_S|^2)(1-|\Gamma_{IN}|^2)} \tag{35}$$

Another, significant aspect of the data process was the interpolation over different P_{avs} levels. In order to obtain smooth data between power levels, small steps of increased power needed to be applied. For this reason, a further improvement of the impedance-scanning algorithm had to be implemented that decreased the acquisition time significantly.

4.2.2 Power levels

As stated before, the final performance goals of the DPA (3.2.1), the desired P_L of the DPA is 42.3 dBm. The back-off level was set to $\gamma = 8$ dB. The selected P_L level for the main device at BO is 34.3 dBm. The value of P_{avs} at this P_L level depends on the G_T, which in turn depends on the operation bias point. With a preliminary set of measurements, it was found that the G_T is approximately 14.3 dB, corresponding to a $P_{avs,\ m,\ BO}$ of 20 dBm and $P_{avs,\ m,\ FP}$ of 28 dBm. For the auxiliary PA, the $P_{avs,\ a,\ BO}$ also has to be 20 dBm, due to the symmetric architecture.

4.2.3 DC Bias sweeps

A DC bias sweep was measured for the main PA. The gate voltage (V_{gs}) swept from -5V to -2V, for a constant drain voltage (V_{ds}= 28 V). The results of the sweep are shown in Figure 30. The plot also shows in comparison the model simulation results under the same conditions. A small shift to higher values of the V_{gs} is noticed in comparison with the simulation curve. The V_{gs} values of interest are located in deep class AB bias points from -2.5 to -2.9 V corresponding to quiescent I_{ds} values of 10 to 100 mA. The selection of the exact V_{gs} value was based entirely on the G_T flatness and drain current phase (I_{ph}) response.

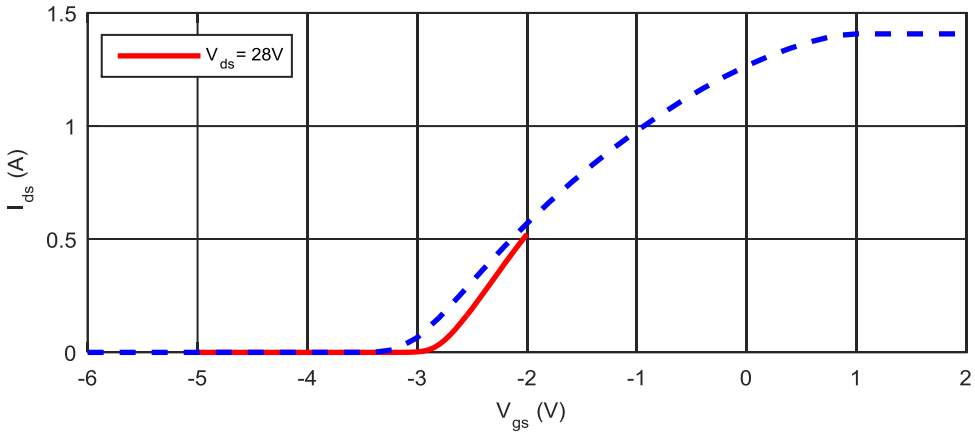

Figure 30. Measured Gate voltage (V_{gs}) versus drain current (I_{ds}) for constant drain voltage (V_{ds}= 28 V) (red line). Also plotted together the simulation results under the same conditions (blue dashed line).

For the determination of $V_{gs,}$ a series of load-pull measurements for different P_{avs} and V_{gs} values were acquired. The data were processed and interpolated over the different power levels. The data process resulted in power sweeps of selected load impedance areas for different V_{gs} values. The results of the interpolated power sweeps of the main device for the G_T and I_{ph} are shown in Figure 31. The power sweeps correspond to a Γ_L close to the optimum regions at the back-off power level of the main device.

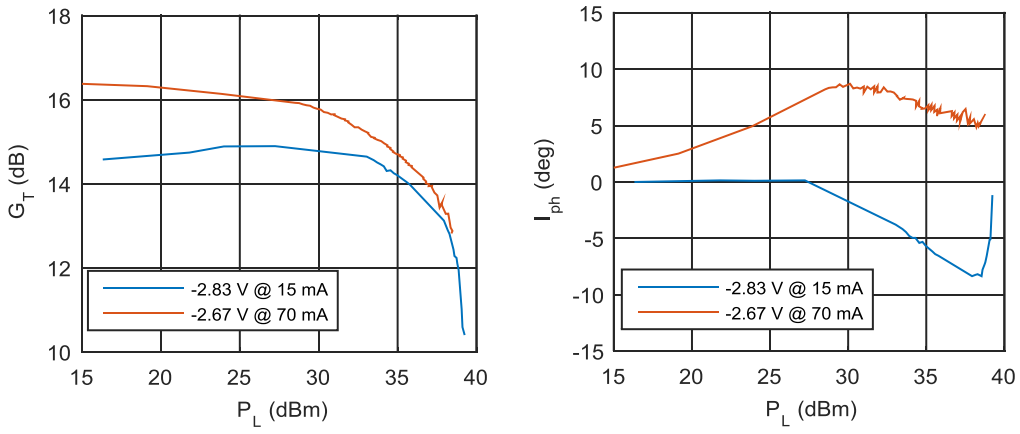

Figure 31. Power sweeps (P_L) of the main device extracted from interpolated load-pull data for the gain (G_T) and the drain current phase (I_{ph}). The sweeps are presented for two different values of Vgs (-2.83 and -2.67 V) for a Γ_L close to the optimum regions at the back-off power level. The apparent noise at high power levels is due to the interpolation of the measurement data.

The selection of the exact optimum Γ_L was not important for of determining bias. The bias can be tuned slightly later without affecting optimum Γ_L. The apparent noise at high power levels is due to the interpolation of the measurement data. Note that at low power levels the measurement data is sparser and thus the curves are not perfectly smooth.

From Figure 31, it can be seen that a suitable choice for a flat gain response and small drain current phase distortion is the bias point with V_{gs} = -2.83 V and I_{ds} = 15 mA. The selected bias point results in lower gain and behavior that is more flat. The phase distortion of this bias point is small and constant at low driving levels and at higher levels it reaches a maximum of 9°. The device at that level in not fully compressed, since the load modulation starts after that power level. The higher bias points exhibit an increasing phase distortion from low drive levels reaching a maximum difference of 8° and then they drop again in lower levels.

For the selection of the auxiliary V_{gs} bias point bias sweeps were performed. The criterion for the proper V_{gs} value was that the necessary turn on $P_{avs,\,m,\,BO}$ level that had to be 20 dBm, which is the BO power level of the DPA. The V_{gs} value corresponding to that power level is -5.6 V.

4.2.4 Load-pull of main development board

After the determination of the gate bias points of the main amplifier, two load-pull measurements were performed, one at back-off (BO) power operation and one at full power (FP) operation. The corresponding P_{avs} levels of this operation levels are 20 dBm and 28 dBm, respectively. The results are shown in the plots of Figure 32 and Figure 33. The plots are correspond to Γ_S = -0.50 -0.35i, which is the conjugate of Γ_{IN} for the optimum Γ_L value of the main device at BO power level. The plots were transformed for this value because the design aims to maximizing PAE at the BO state. The plots contain contour measurements of P_L, PAE and the drain current phase $\angle I_{ds}$. In the figures, the locations of the scanned areas are shown in the smith chart as well as magnified version of them.

From the measurements of the main PA, in Figure 32, it can be seen that P_L varies from 33 to over 36 dBm. The PAE reaches a maximum level of 54% and $\angle I_{ds}$ shifts between

-10° and 20°. The peak P_L value is located outside the scanned area, which is not of great importance since the desired P_L at the BO state is around 34-35 dBm.

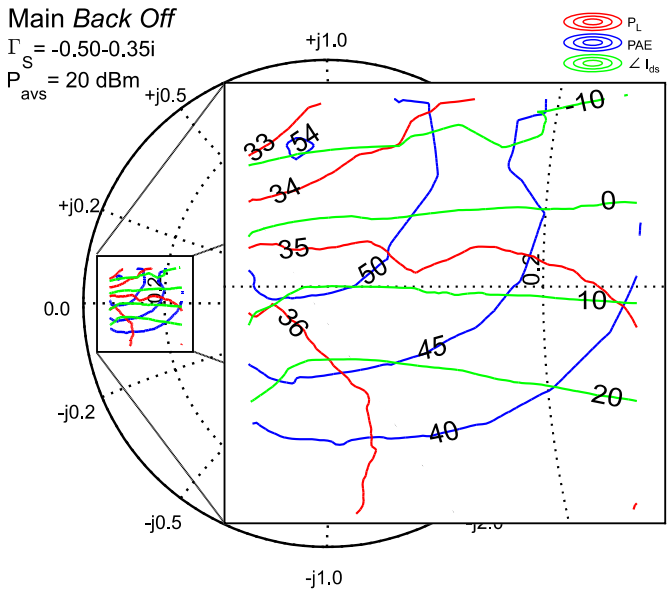

Figure 32. Load-pull measurement of the main development board at the BO state. The corresponding P_{avs} for this state is 20 dBm. The measurement results are transformed for Γ_S = -0.50 -0.35i, which is the conjugate value of the optimum Γ_{IN} at this state. The plot shows the contours of P_L, PAE and drain current phase (l_{ph}).

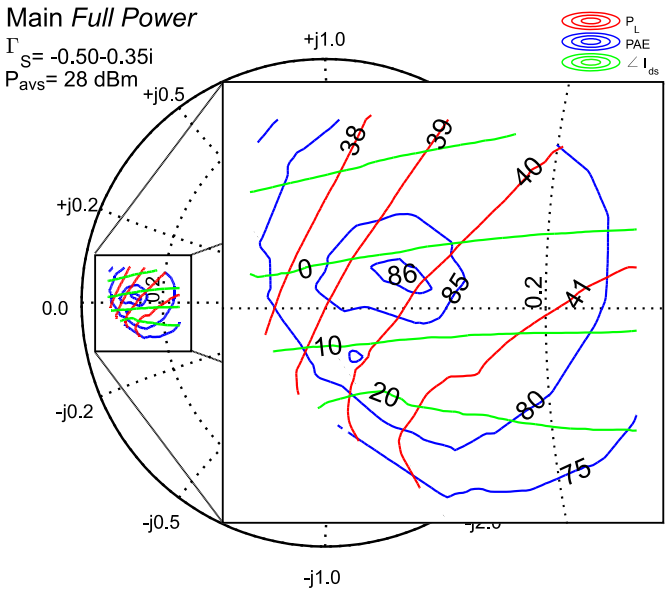

Figure 33. Load-pull measurement of the main development board at the full power state. The corresponding P_{avs} for this state is 28 dBm. The measurement results are transformed for Γ_S = -0.50 -0.35i, which is the conjugate value of the optimum Γ_{IN} at the back-off state. The plot shows the contours of P_L, PAE and drain current phase (l_{ph}).

In Figure 33, the measurement results show that the main device can reach, at FP operation, P_L levels higher than 41 dBm with PAE reaching a peak value of 86%. The peak value of PAE appears to be higher than the theoretical one for a class B PA (78.5%). This

is caused by the level of accuracy in the delivered power measurement the system can provide. As described in Section 2.2.4, the measurement error close to the edge of the smith chart can be as high as 1 to 1.2 dB. The $\angle I_{ds}$ varies from -10° to 20°.

4.2.5 Load-pull of auxiliary development board

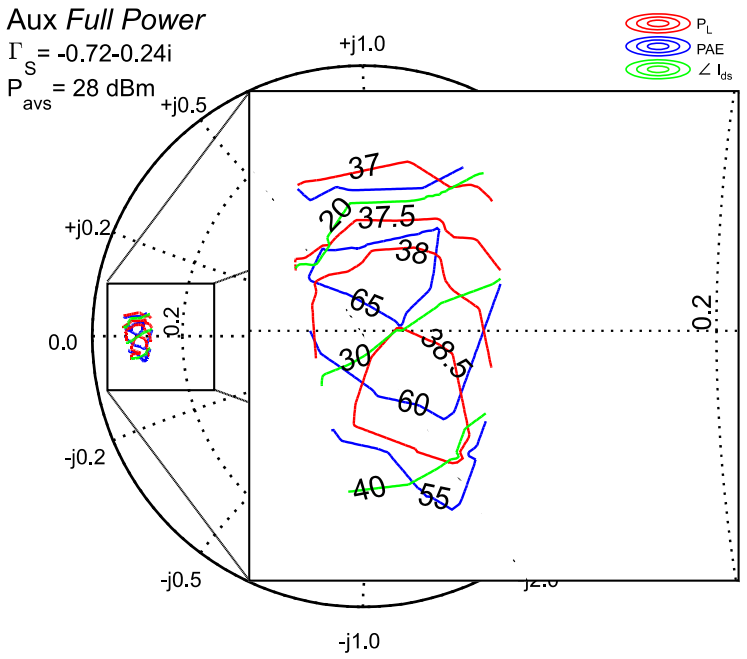

Figure 34. Load-pull measurement of the auxiliary development board at the full power state. The corresponding P_{avs} of the state is 28 dBm. The measurement results are normalized for Γ_S = -0.72 -0.24i, which is the conjugate value of Γ_{IN} of corresponding optimum Γ_L. The plot shows the contours of P_L, PAE and drain current phase (I_{ph}).

The load-pull measurement, for the auxiliary device is shown in Figure 34. The plot is transformed for Γ_S = -0.72 -0.24i, which is the conjugate Γ_{IN} for the optimum Γ_L value of the auxiliary device at FP power level. The auxiliary device can reach P_L levels of 38.5 dBm with peak PAE up to 65%, with the $\angle I_{ds}$ varying between 20° and 40°.

4.3 Measurement based design parameters

For the extraction of the measurement based design parameters of the DPA, a sweep of different Γ_L values for the main and auxiliary devices at FP operation state was performed. The purpose of the sweep was to find the optimum combination of Γ_L and Z_L, yielding the best possible performance compromise. A sweep of eight different $Z_{L,\,m,\,FP}$ for eight different $Z_{L,\,a,\,FP,}$ resulting in 64 impedance combinations, were examined. The selected impedances are shown in Figure 35 for the auxiliary and main devices. The optimum impedance of the main device at BO ($\Gamma_{L,\,m,\,BO}$) state was initially selected and remained as constant through the sweep. The selected value of $\Gamma_{L,\,m,\,BO}$ was -0.78+0.09i, corresponding to $Z_{L,\,m,\,BO}$ = 6.16+2.78j Ohm. The point was selected for maximum PAE, minimum gain compression and minimum drain current phase distortion. The PAE and $\angle I_{ds}$ for this selected point are 51.5% and -6° respectively, in the BO state. The P_L at this impedance is

34.3 dBm and the G_T is 14.3 dB. The Γ_{IN} of the selected point is -0.51+0.36i. The conjugate value of it was used for the Γ_S presented to main device.

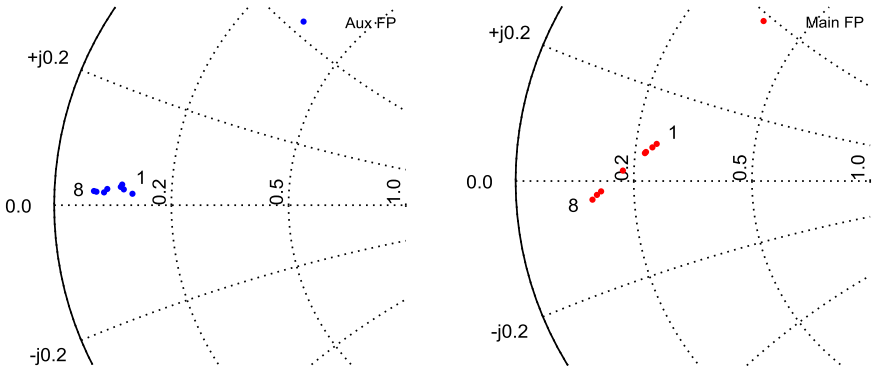

Figure 35. Selected impedances for the sweep of different impedances of the auxiliary device (left) and main device (right). The sweep resulted to 64 different combination of impedances for the main and auxiliary devices with slightly different expected performances.

The DPA performance results of the sweep for different combinations of impedances for the main (Z_m) and auxiliary (Z_a) devices is shown in Figure 36 [8]. The plot shows the predicted values of the DPA performance in PAE and voltage phase distortion difference (ΔPhase) between FP and BO states. As can be seen, the optimum combination is Z_{m5} and Z_{a4}. Due to a mistake during the data process, which affected the voltage phase distortion values, the combination Z_{m8} and Z_{a1} was selected for the final design. All data for the selected impedances and their measured performance is show in Table 3.

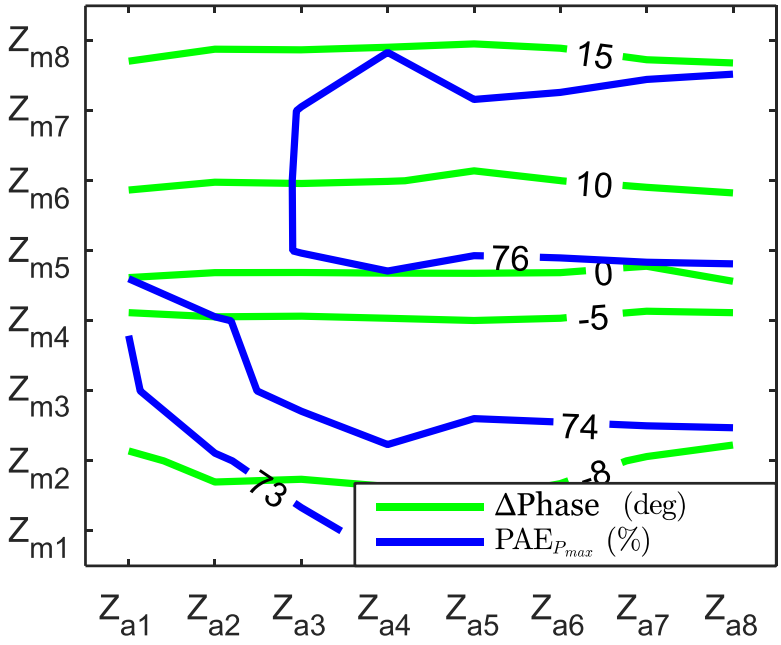

Figure 36. DPA performance result predictions for 64 combinations of main and auxiliary impedances (Z_m and Z_a). The predictions refer to final DPA PAE and phase difference between the output voltages at FP and BO states.

Table 3. The final selected combination Z_{ms} and Z_{a1} of load impedances for the three states of operation for the main and auxiliary devices and the measured performance at that points, along with the source impedances of each state.

Op. State	*P_{avs} (dBm)*	*P_L (dBm)*	*PAE (%)*	*$\angle I_{ds}$ (^{o})*	*$Z_{L,\ opt}$ (Ohm)*	*Z_S (Ohm)*
Main BO	20	34.3	51.5	-5.9	6.16+2.78i	12.84-14.80i
Main FP	28	40.5	82.7	15.4	6.03 -1.66i	12.84-14.80i
Aux FP	28	37.5	60.5	29.3	6.25+1.03i	7.05-7.97i

The Z-parameters of the test board, necessary for the design method used [45], were measured using the system in small signal acquisition mode. The results are shown in Table 4.

Table 4. Z parameters measurement at 2.14 GHz for the main and auxiliary devices.

PA	*Z11*	*Z12*	*Z21*	*Z22*
Main	10.53 + 6.78i	71.35 -21.81i	-0.12 - 1.17i	4.50 - 3.91i
Aux	6.82 + 2.01i	-0.35 - 1.64i	-0.40 - 1.62i	0.62 - 5.25i

Using the design method and calculations described in [45], the final output combiner Z parameters and the input phase delay of the phase shifter are calculated from the optimum impedances above. The results are shown in Table 5.

Table 5. Calculated Z parameters of the output DPA combiner and the input phase delay.

	Z11	*Z12*	*Z21*	*Z22*
2 port Combiner	8.14+0.26i	-1.77+3.71i	-1.77+3.71i	0.39+0.13i
Input phase delay	-92.9^o			

The predicted DPA performance values, for lossless input matching and output combiner networks is shown in Table 6.

Table 6. DPA predicted performance

	8 dB Back-Off	*Full Power*
P_L (dBm)	34.3	42.3
G_T (dB)	11.3	11.2
PAE (%)	49.6	74.1
Phase (^{o})	-	16.0

5 Measurement based Doherty power amplifier design

In this chapter is presented the design process for the DPA. The design parameters used here were derived in the previous chapter, in Table 5 and the source impedances in Table 3. Figure 37 shows the block element schematic of the DPA used for the design. The architecture contains a power divider at the input, a phase shifter (θ), the input matching networks, the two test boards and the combiner. The design of the DPA components was implemented in ADS, using the micro-strip libraries for the transmission lines and the Modelithics libraries for the passive components.

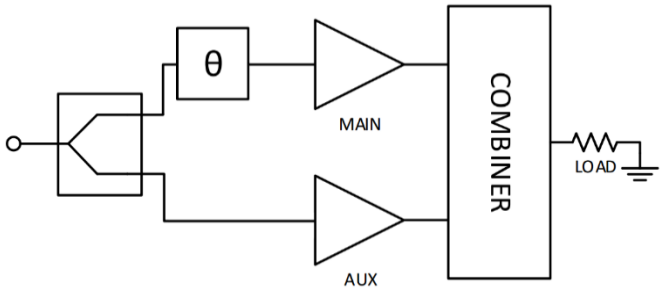

Figure 37. The block schematic used for the DPA design.

5.1 Input power divider

For the input power division, a Wilkinson divider was implemented. The DPA is designed for symmetric operation with equal split of the driving signal between the main and auxiliary devices. A compact Wilkinson divider is a suitable solution for the need of this design. The divider was designed with the classic approach, described in [39], with 50 Ω nominal impedance. The EM simulated S-parameters and the layout of the divider are shown at Figure 38.

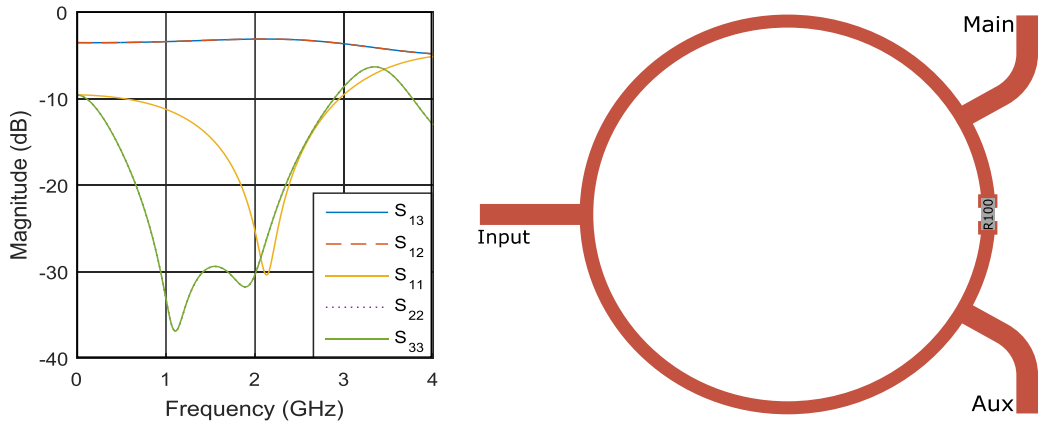

Figure 38. The EM simulated S-parameters and the layout of the Wilkinson divider.

5.2 Input phase shifter

A phase shifter was introduced into the DPA design. The position of the phase shifter in the circuit is shown in Figure 37. The phase shifter can be used to vary the absolute voltage phase delay between the main and auxiliary device. The shift of the phase can be achieved by cutting off and moving the horizontal transmission line to a new position. For the connection between the square corners copper tape can be used. The new positions have constant phase steps of 13.7°. Four steps were designed, as Figure 39 shows, capable of varying the phase difference from 85.2° to 126.3°. It is also possible to decrease the phase difference by positioning the horizontal transmission line closer to the input and output of the shifter. This approach is not recommend due to the high uncertainty in the phase shift, as no visible marks declare an exact position.

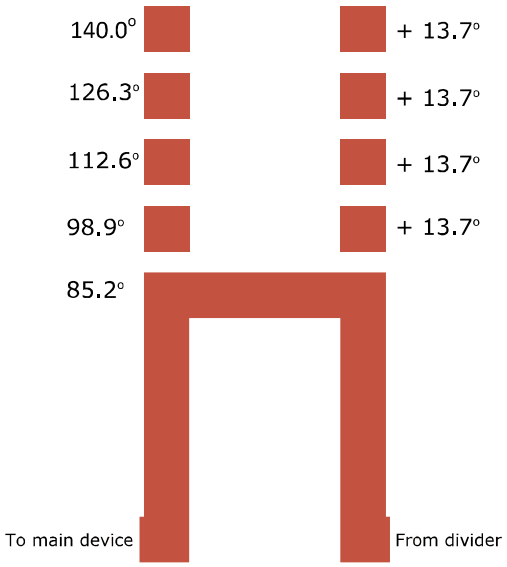

Figure 39. The layout of the phase shifter. The phase step is 13.7°. The phase can be shifted from 85.2° to 140.0°.

5.3 Main and auxiliary input matching networks

The input matching networks were designed to present Γ_S according to the specifications of Table 3. The schematics of the networks are shown in Figure 40. The left schematic is for the main device and the right for the auxiliary device. The impedance of the transmission lines was kept at $Z_0 = 50$ Ohm. The networks are connected to the divider with offset transmission lines. The length of the offset lines was adjusted for design symmetry. The offset line form the main device side accounts also for the phase shifter. The final impedances from the EM simulation are 12.51-13.97j Ω for the main device and 7.25-6.98j Ohm.

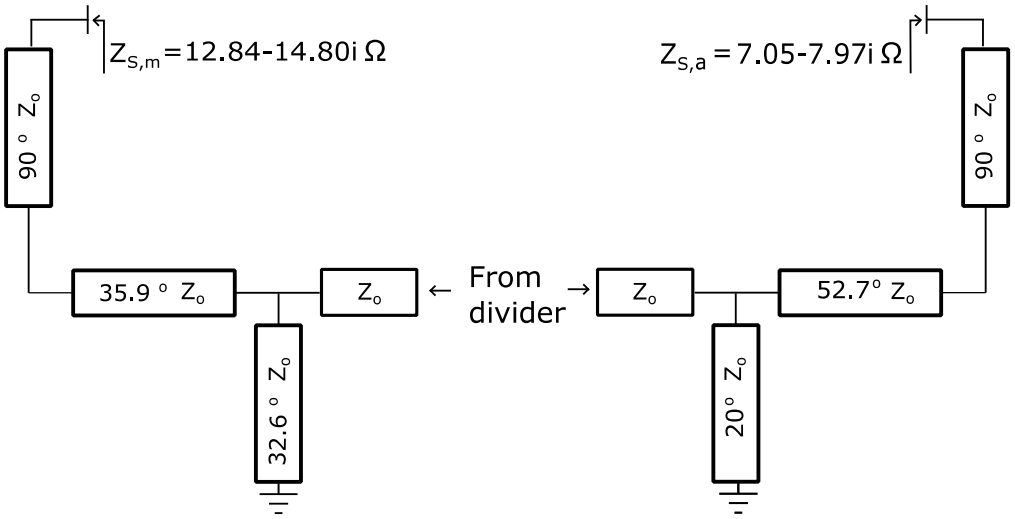

Figure 40. The input matching networks for the main device (left) and the auxiliary device (right). The networks provide the optimum gain matching. The transmission lines have characteristic impedance of $Z_0 = 50$ Ohm.

5.4 Output power combiner

For the realization of the combiner, the following method can be used [36]. Initially, the reciprocal and lossy 2-port combiner is converted into a reciprocal and lossless 2-port network cascaded with a resistance and cascaded again with another reciprocal and lossless 2-port network. Then, the reciprocal and lossless 2-port networks are easily realized with equivalent T or Pi networks. The T or Pi networks can be realized with transmission lines or lumped components. The resulting Z parameters of the combiner network is shown in

Table 7 and the schematic in Figure 41. The difference of the actual achieved Z parameters from the target ones is less than 1% and is mainly caused form manufacturing tolerance restrictions. A difference of this level cannot affect the final performance in any significant way.

Table 7. EM-Simulated Z-parameters of the realized combiner network when the output (port 3) is terminated with 50 Ω load. The Main device is at port 1 and the auxiliary at port 2. The achieved values are compared with the desired ones form Table 5

	Z11	*Z12*	*Z21*	*Z22*
Target values	8.14+0.26i	-1.77+3.71i	-1.77+3.71i	0.39+0.13i
Achieved values (EM sim.)	7.43+0.26i	-1.42+3.09i	-1.42+3.09i	0.67+0.46i

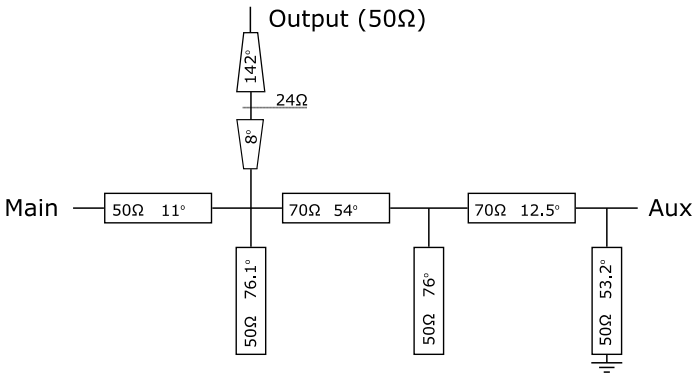

Figure 41. Schematic of the output combiner. The combiner was designed to have the Z-parameters of Table 5. The Main device is at port 1 and the auxiliary at port 2.

5.5 Complete layout

The complete layout of the DPA is shown in Figure 42. All the elements are arranged according to the block diagram of Figure 37. Starting from the bottom, the Wilkinson divider splits the input signal to the main device at the left and to the auxiliary device at the right. The phase shifter follows the divider output for the main device branch. Next, the fundamental input matching networks are located, followed by the second harmonic matching networks and the stabilization networks. The main and auxiliary devices are connected together with the combiner, located between them, which connects the output port at the top of the layout.

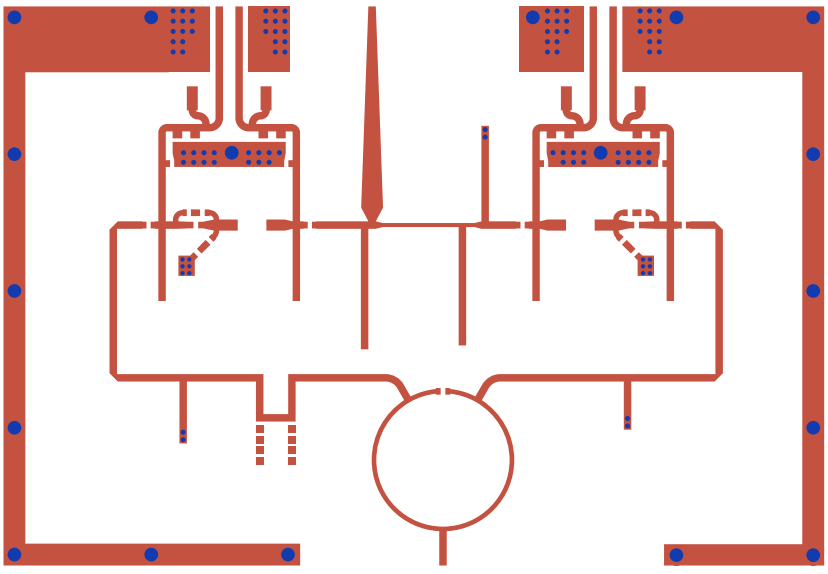

Figure 42. The final layout of the DPA. The layout is composed of the block elements as showed in Figure 37. The figure shows the top conducting layer. The ground plane on the bottom layer is a continuous metal sheet. The ground via holes are indicated with blue color. The dimensions of the layout border are 120 x 80 mm.

6 Doherty power amplifier measurements

The final DPA layout was sent for fabrication. The assembly and soldering of the SMD components was done using a reflow oven. The connectors and large components were soldered manually. Two copper heat sinks were placed beneath each device, providing additional mechanical stability. The fabricated DPA is shown in

Figure 43. The DPA was measured with power sweeps under continuous wave (CW) stimulus, as presented next.

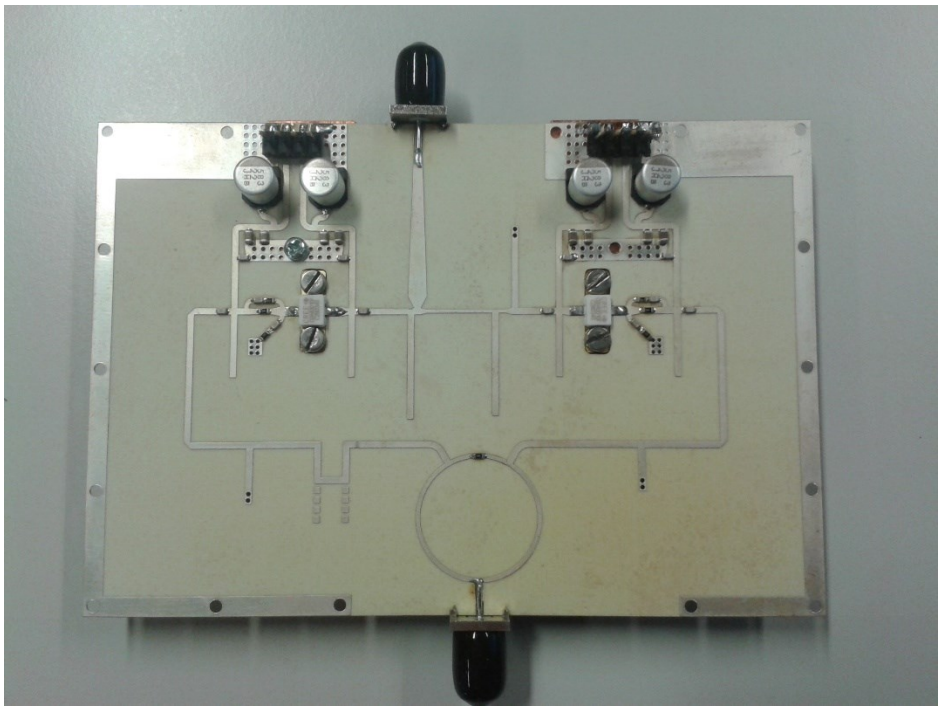

Figure 43. The assembled DPA.

6.1 CW Measurements

Continuous wave measurements were performed on the DPA using the load-pull system. The input power was swept from -10 to 36 dBm, while the load impedance was kept constant at 50 Ohm. The power sweep was performed initially with the bias conditions used for the characterization of the development boards. Additional power sweeps as functions of main and auxiliary device gate voltage ($V_{gs,\ main}$ and $V_{gs,\ aux}$) were performed, in order to find the optimum bias points of the DPA. Also the effect of the input phase difference between the main and auxiliary device was explored by adjusting the phase shifter in different positions and perform power sweeps for a selected combination of main and auxiliary gate voltages. The measurement results are presented and discussed next.

6.1.1 Measurements with initial conditions

Figure 44 shows the power sweep results of the DPA with the initial bias conditions used in the development board characterization. The initial bias conditions were $V_{gs,\ main}$ = -2.83 V corresponding to $I_{ds,\ main}$ = 15 mA and $V_{gs,\ aux}$ = -5.6 V. The plot shows the gain G_T, phase and PAE versus the output power delivered to the load. The phase is taken directly from the measured data and is defined as:

$$Phase = \angle \frac{b_2}{a_1} \tag{36}$$

From the plot it can be seen that the maximum output power is 40.9 dBm. The DPA gain shows an increasing response form 7 dB up to 11 dB in low input powers, while in the higher input power level drops again down to 9 dB. The gain behavior at the low power region can be improved by fine tuning $V_{gs,main}$. The PAE of the PA exhibits a high peak at -4 dB back off power level reaching 55 % while at FP it drops to 50 %. The BO level is not close to the targeted one (8 dB) and adjustment of the $V_{gs,\ aux}$ is necessary. The phase distortion reaches a maximum level of 23° at the BO operation level and drops down to 18° at FP level.

As the results demonstrate, the desired performance of the DPA is not achieved and fine tuning of the bias points is necessary. In the next sections, sweeps of the gate voltages of the main and auxiliary device show how the proper tuning leads to performance values closer to the desired ones.

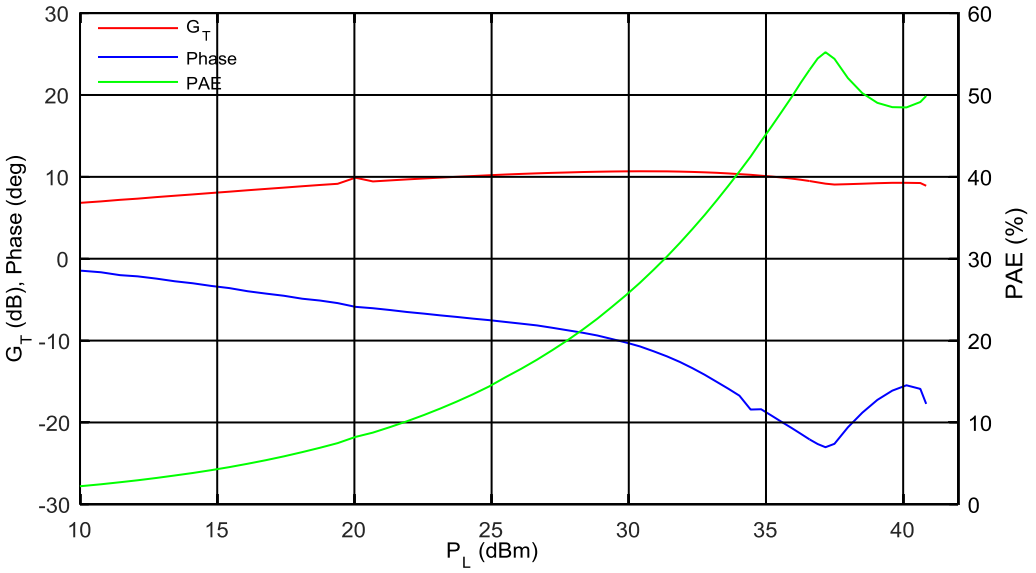

Figure 44. Power sweep of the DPA with the initial bias conditions used in the characterization process of the development boards. The $V_{gs,\ main}$ = -2.83 V and $V_{gs,\ aux}$ = -5.6 V.

6.1.2 Main device gate voltage sweeps

A sweep of the $V_{gs,\ main}$ was performed from -2.80 V to -2.65 V with 0.5 V steps and the DPA performance was measured for an adjusted value of $V_{gs,\ aux}$ = -4.4 V. The measurement results for the G_T, PAE and V_{Phs} are shown in the next figures.

Figure 45 shows the G_T response of the DPA to the change of the $V_{gs,\ main}$ voltage. As the voltage is increased towards to a Class-A operation point, the gain at the low input power levels increases also resulting to a flat response in the area of -2.75 to -2.70 V. The maximum delivered power increases also a little.

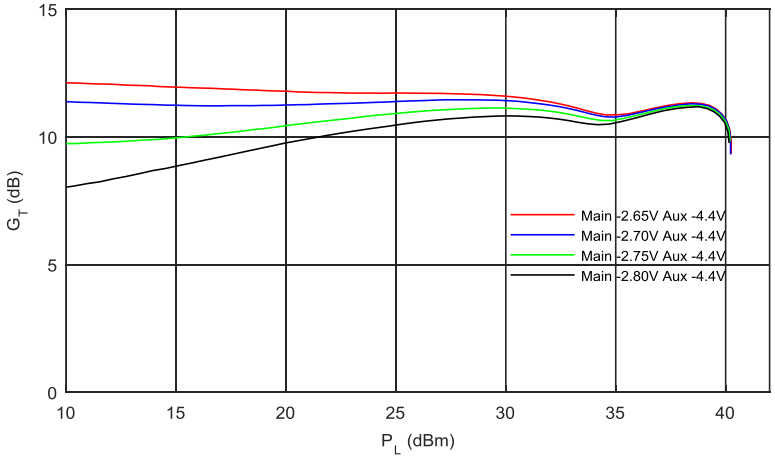

Figure 45. G_T as a function of delivered power P_L for $V_{gs,\ main}$ sweeps.

Figure 46 shows the PAE response of the DPA as the $V_{gs,\ main}$ voltage changes. As expected the DPA PAE is not affected significantly in any way, except the of the lower input power levels where PAE decreases slightly as the voltage is increased. This effect is caused form the increase of the $I_{ds,\ main}$ as is set to a bias point closer to Class-A. The increase of the quiescent $I_{ds,\ main}$ results in a decrease of the PAE, even thought of the increased gain in these input power levels.

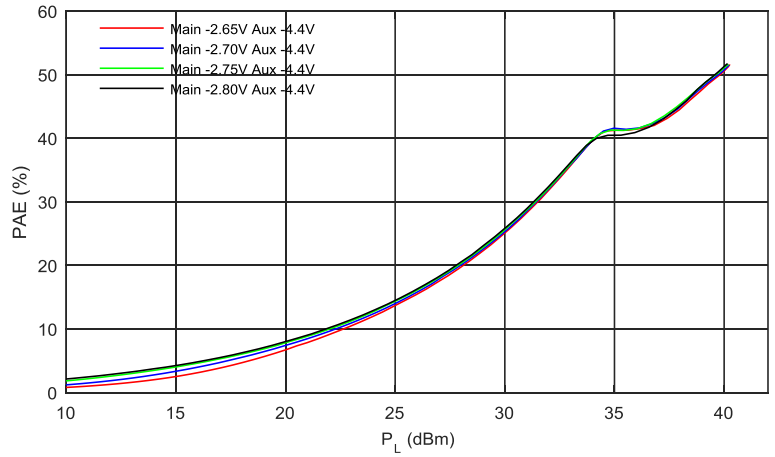

Figure 46. PAE as a function of delivered power P_L for $V_{gs,\ main}$ sweeps.

Figure 47 shows the phase response of the DPA as the $V_{gs,\ main}$ voltage changes. The results show that phase is highly depended from the $V_{gs,\ main}$. The maximum phase distortion varies from -14° to +10° for the $V_{gs,\ main}$ sweeps. From the results the optimum choice is $V_{gs,\ main}$ = -2.75 V, which gives a maximum phase distortion of +3° to -4° at BO levels and +7° at FP levels.

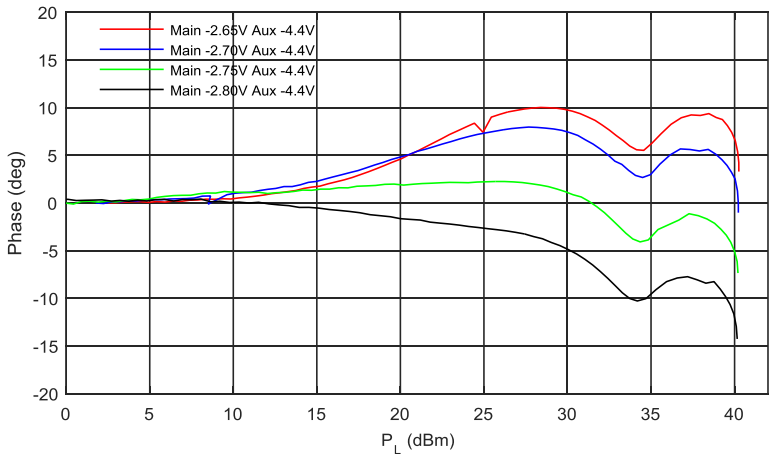

Figure 47. Phase as a function of delivered power P_L for Vgs, main sweeps.

Considering all the DPA performance measurement and their dependence from the $V_{gs,\ main}$ the optimum bias point for the main device was selected to be -2.75 V. Using this bias point the $V_{gs,\ aux}$ were swept for properly tuning the BO level performance.

6.1.3 Auxiliary device gate voltage sweeps

Figure 48 shows the G_T response of the DPA to the change of the $V_{gs,\ aux}$ voltage. As the bias point of the auxiliary device increases from -5.4 V to -4.4 V with were $V_{gs,\ main}$ = -2.75 V the BO level shifts to lower values. The gain between the BO and FP increases from 9.4 up to 11.3 dB. Also the maximum delivered power decreases slightly from 40.8 dBm to 40.2 dBm.

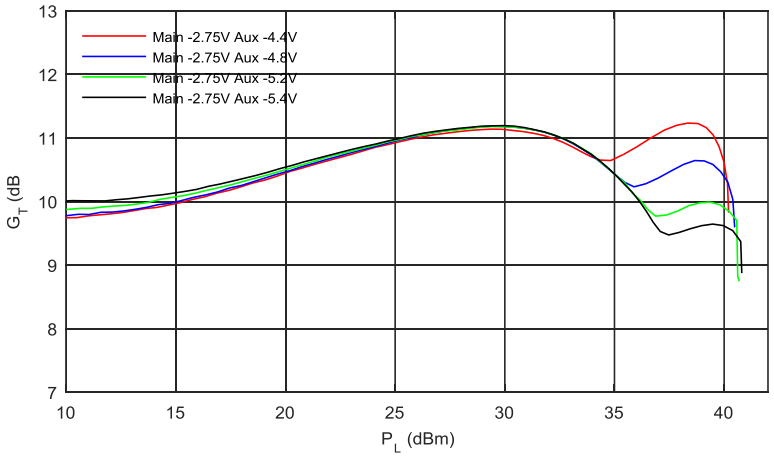

Figure 48. G_T as a function of delivered power P_L for V_{gs}, aux sweeps.

In Figure 49 the PAE of the DPA is plotted as function of delivered power for the different values of $V_{gs,\ aux}$ voltage. Both the BO peak and the FP point are affected by this change. The BO peak shifts to lower BO levels for higher $V_{gs,\ aux}$ voltages. The maximum delivered power shifts to lower levels, as in Figure 48, but the PAE increases slightly from 50% to 52%.

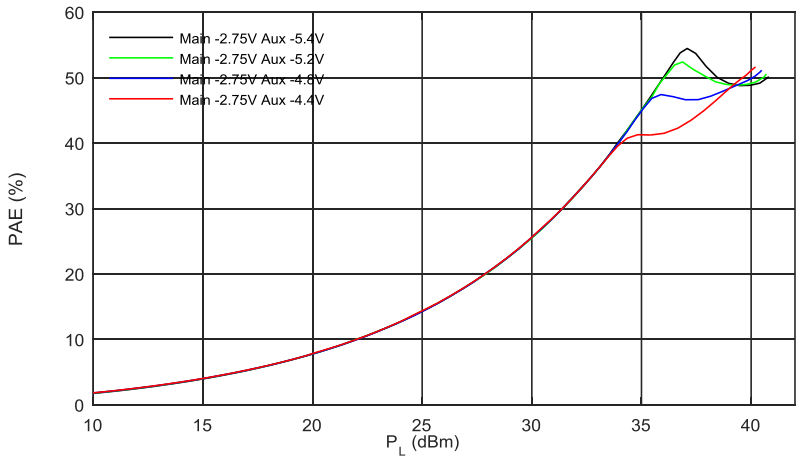

Figure 49. DPA PAE as a function of delivered power P_L for V_{gs}, aux sweeps.

Figure 50 shows the DPA phase response as a function of delivered power for $V_{gs,\ aux}$ sweeps. From the plots it can be seen that the minimum phase distortion is achieved for a bias point of $V_{gs,\ aux}$ = -4.4 V, with -4° at BO and -7° at FP. Considering, all the information from these plots and emphasizing in linearity, the $V_{gs,\ aux}$ = -4.4 V is selected as an optimal bias point for the auxiliary device.

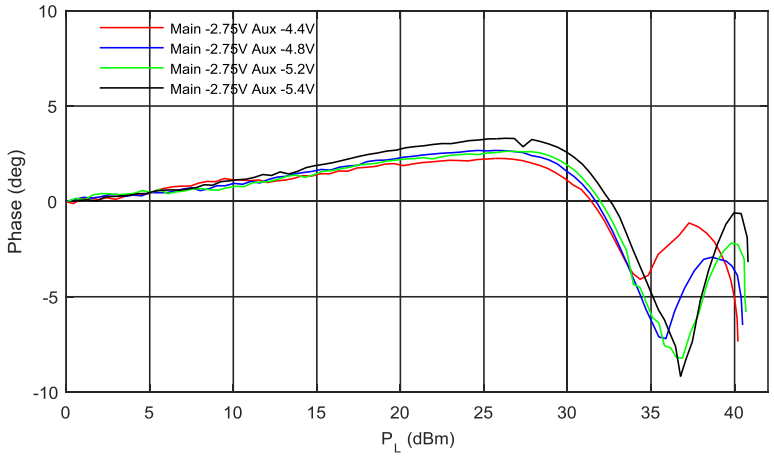

Figure 50. DPA Phase as a function of delivered power P_L for V_{gs}, aux sweeps.

6.1.4 Input phase delay sweeps

As discussed before, and detailed in the Section 5.2, a shift in the voltage phase delay between the main and auxiliary device can be adjusted by the phase shifter. By using the phase shifter, three different phase shifts were introduced, and the performance of the DPA was measured as function of delivered power. The next pictures shows the results. Phs0 is

defined as the original phase delay and is equal to -85.2° and was used in the previous measurements. Phs1 and Phs2 are measurements using increasing phase delays according to the predefined steps also discussed in 5.2. The phase delay for Phs1 is -98.9° and for Phs2 is -112.6°.

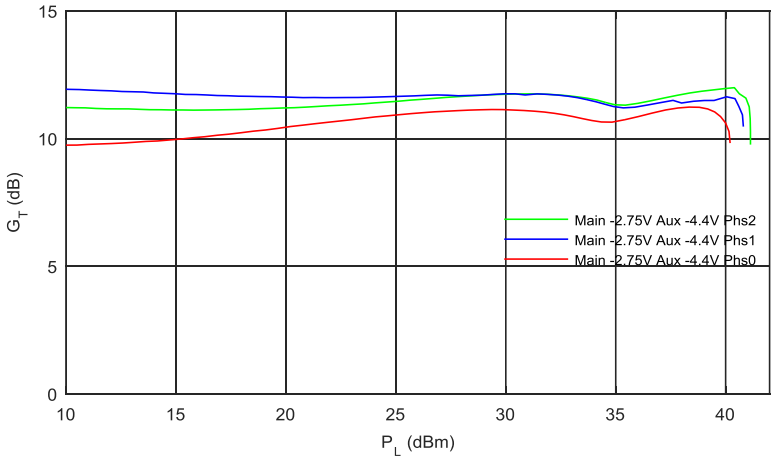

Figure 51. DPA G_T as a function of delivered power P_L for input phase delay sweeps.

In Figure 51 the DPA G_T as a function of delivered power P_L for these three input phase delays can be seen. Increasing the phase delay results in higher delivered power and also affects the DPA G_T flatness and level. The optimum value is seen as achieved for input phase phs1. It worth to mention that the gain behavior of the Phs0 state seems lower than expected and this can be probably caused due to input mismatching.

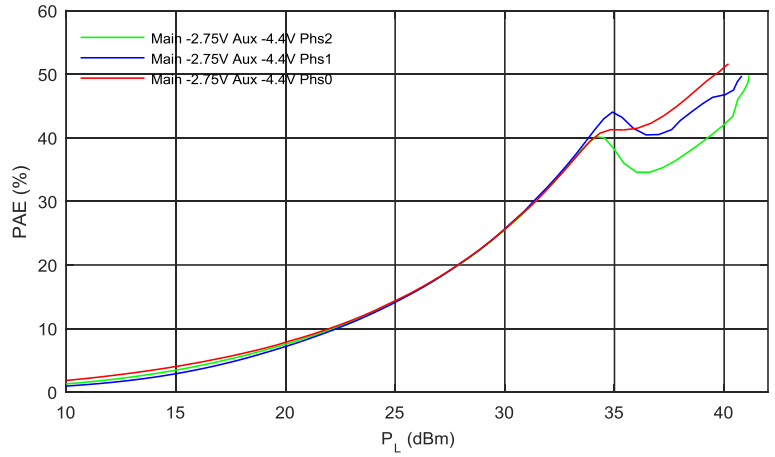

Figure 52. DPA PAE as a function of delivered power P_L for input phase delay sweeps.

In Figure 52 the PAE is presented as function of delivered power P_L. The main effect of the phase delay is the PAE behavior between the BO and FP levels. The optimum response is again the choice of input phase Phs1, corresponding to the highest BO efficiency where PAE reaches 43%, while at FP reaches 50%. The maximum delivered power is also

affected and slightly lower, but yields a good compromise between power at FP and efficiency at BO.

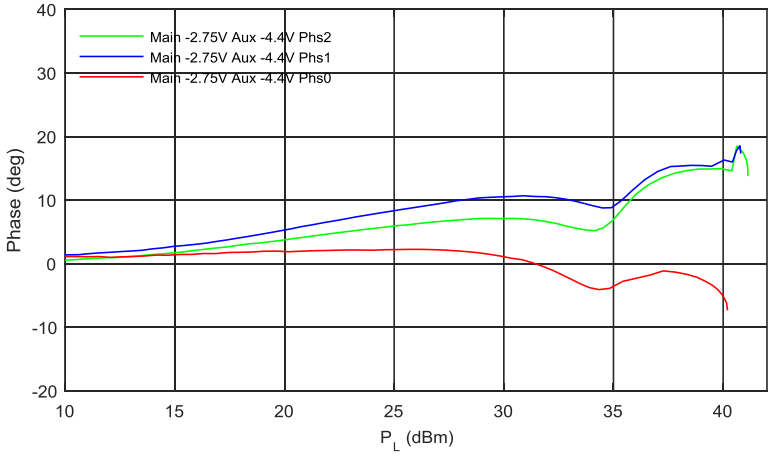

Figure 53. DPA Phase as a function of delivered power P_L for input phase delay sweeps.

In Figure 53 it can be seen how the DPA phase response is affected form the different input phase delays. While the initial Phs0 gives the smallest variations between 4° and -7° the other phase states increase the DPA phase distortion to higher values, reaching 16° in the BO levels. While this result shows that the Phs1 is not the optimum choice, is the one that behaves very close to the predicted values of Table 6.

Considering the data from the last plots the Ph1 is selected as the optimum input phase delay between the main and auxiliary devices. This result is also in agreement with the theoretical calculation of Section 4.3, where the optimum input phase delay was calculated to be -92.9°. The phase shifter was able to provide the discrete values of Phs0 = -85.2^0 and Phs1 = -98.9°. From the two values the closest to the desired one is Phs1.

Table 8 shows the initial uncorrected and the final measured performance values and the theoretical predictions from Section 4.3. The difference between the final results and the predictions is probably caused form the losses of the combiner as during the theoretical calculations they are not taken under consideration. This affects mainly the FP P_L and PAE. Also here we should mention that the predicted high PAE at FP is also incorrect as is highly depended from the LP measurement error of the used system. From the total overview of the data it can be concluded that the employed method can offer good design approximation of the final performance but further improvement of the LP system accuracy is necessary.

Table 8. The final measured performance values and the theoretical predictions.

	Initial Measurement		***Final Measurement***		***Theoretical Predictions***	
	4 dB Back-Off	*Full Power*	***6.2** dB Back-Off*	*Full Power*	*8 dB Back-Off*	*Full Power*
P_L (dBm)	36.9	40.9	**32.5**	**40.8**	34.3	42.3
G_T (dB)	9.2	9.4	**11.4**	**10.9**	11.3	11.2
PAE (%)	55.2	50.4	**42.3**	**50.1**	49.6	74.1
Phase (°)	23.1	18.3	**8.8**	**17.3**	-	16.0

7 Conclusion and future work

In this chapter the general conclusions and the future work are presented and discussed.

7.1 General conclusions

In this work, an active load-pull system was developed, tested and used in the characterization of a 10W GaN HEMT. The characterization data were used in combination with a new DPA design approach, intended to provide an improved efficiency and linearity tradeoff, to design and fabricate a DPA.

The developed active load-pull system was used for fast acquisition of load-pull data in a wide range of input and output power levels. The system was developed using modular components, allowing an easy adjustment to the specific needs of any future project.

The characterization of the GaN device was conducted by using a precursor development board (DB). The DB contained the device along with its stability network and second harmonic and baseband terminations. The DB was characterized at different power levels of interest and was used as is in the final DPA design.

The designed and fabricated DPA presented excellent performance with good agreement with the theoretical predictions, verifying the robustness of the implemented designed method. The DPA was designed to operate at 2.14 GHz and reached an output power level of 40.8 dBm, which was 1.5 dB less than the expected, and with a gain of 11.4 dB at back-off (BO) and 10.9 dB at full power (FP). The power added efficiency at 6.2 dB BO was 42.3 % and 50.1 % at FP. The phase response of the DPA presented a distortion of 8.8^{o} at BO and 17.6^{o} at FP.

The developed active load-pull system proved to be a powerful tool for characterizing transistors for PA design. With the proposed measurement based design technique, it is possible to realize high performance DPAs also without nonlinear transistor models available.

7.2 Future work

As the results indicated the system needs further improvements in the accuracy of the measurements. Further development of the system can include the improvement of the used hardware and the calibration methods that are used. Also the software can be improved so the data acquisitions are faster by implementing more sophisticated impedance scanning algorithms. The modular character of the system allows the expansion of it for used in different PA characterization tasks. Another expansion possibly is the introduction of harmonic and baseband measurements. Considering the above this thesis project can provide solid ground for future projects in the development of the LP system and PA design.

8 Bibliography

[1] E. B. Haghighi, "The effect of free cooling on reducing total energy consumption for telecommunication base stations," in *Telecommunications Energy Conference (INTELEC), 2015 IEEE International*, 2015, pp. 1-5.

[2] S. Mclaughlin, P. M. Grant, J. S. Thompson, H. Haas, D. I. Laurenson, C. Khirallah, *et al.*, "Techniques for improving cellular radio base station energy efficiency," *IEEE Wireless Communications,* vol. 18, pp. 10-17, 2011.

[3] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho, and B. Kim, "The Doherty power amplifier: Review of recent solutions and trends," *IEEE Transactions on Microwave Theory and Techniques,* vol. 63, pp. 559-571, 2015.

[4] J. Kim, J. Cha, I. Kim, and B. Kim, "Optimum operation of asymmetrical-cells-based linear Doherty power amplifiers-uneven power drive and power matching," *IEEE Transactions on Microwave Theory and Techniques,* vol. 53, pp. 1802-1809, 2005.

[5] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proceedings of the Institute of Radio Engineers,* vol. 24, pp. 1163-1182, 1936.

[6] S. C. Cripps, "RF power amplifiers for wireless communications," *IEEE Microwave Magazine,* vol. 1, pp. 64-64, 2000.

[7] M. O. W. Hallberg, C. Fager, "Current scaled Doherty amplifier for high efficiency and high linearity," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, pp. 1-4.

[8] M. O. W. Hallberg, D. Gustafsson, K. Buisman, C. Fager, "A Doherty Power Amplifier Design Method for Improved Efficiency and Linearity," *IEEE Transactions on Microwave Theory and Techniques,* vol. PP, pp. 1-14, 2016.

[9] W. Hallberg, "Frequency Reconfigurable and Linear Power Amplifiers Based on Doherty and Varactor Load Modulation Techniques," Licentiate dissertation, Dept. of Microtechnology and Nanosience, Chalmers University of Technology, 2016.

[10] J. M. Rubio, J. Fang, R. Quaglia, V. Camarchia, M. Pirola, S. D. Guerrieri, *et al.*, "A 22W 65% efficiency GaN Doherty power amplifier at 3.5 GHz for WiMAX applications," in *Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), 2011 Workshop on*, 2011, pp. 1-4.

[11] F. M. Ghannouchi and M. S. Hashmi, *Load-pull techniques with applications to power amplifier design* vol. 32: Springer Science & Business Media, 2012.

[12] G. Simpson. (March 2015, A Beginner's Guide To All Things Load Pull.

[13] M. S. Hashmi, F. M. Ghannouchi, P. J. Tasker, and K. Rawat, "Highly reflective load-pull," *IEEE Microwave Magazine,* vol. 12, pp. 96-107, 2011.

[14] P. Colantonio, F. Giannini, E. Limiti, and V. Teppati, "An approach to harmonic load-and source-pull measurements for high-efficiency PA design," *IEEE Transactions on Microwave Theory and Techniques,* vol. 52, pp. 191-198, 2004.

[15] J. Essing, F. Malekzadeh, A. van Roermund, and R. Mahmoudi, "Hybrid multi-harmonic load-and source-pull system," in *Microwave Measurement Symposium (ARFTG), 2012 80th ARFTG*, 2012, pp. 1-4.

[16] T. Gasseling, E. Gatard, C. Charbonniaud, and A. Xiong, "Assets of source pull for NVNA based load pull measurements," in *Microwave Measurement Conference (ARFTG), 2012 79th ARFTG*, 2012, pp. 1-5.

[17] M. Marchetti, "Mixed-signal active load Pull: the Fast track to 3g and 4g aMPliFiers," *Microwave Journal,* vol. 53, pp. 108-+, 2010.

[18] G. P. Bava, U. Pisani, and V. Pozzolo, "Active load technique for load-pull characterisation at microwave frequencies," *Electronics Letters,* vol. 18, pp. 178-180, 1982.

[19] Y. Takayama, "A new load-pull characterization method for microwave power transistors," in *1976 IEEE-MTT-S International Microwave Symposium*, 1976, pp. 218-220.

[20] M. Marchetti, M. J. Pelk, K. Buisman, W. C. E. Neo, M. Spirito, and L. C. N. d. Vreede, "Active Harmonic Load Pull With Realistic Wideband Communications Signals," *IEEE Transactions on Microwave Theory and Techniques,* vol. 56, pp. 2979-2988, 2008.

[21] V. Teppati, A. Ferrero, and U. Pisani, "Recent advances in real-time load-pull systems," *IEEE Transactions on Instrumentation and Measurement,* vol. 57, pp. 2640-2646, 2008.

[22] M. Spirito, L. de Vreede, M. de Kok, M. Pelk, D. Hartskeerl, H. Jos, *et al.*, "A novel active harmonic load-pull setup for on-wafer device linearity characterization," in *Microwave Symposium Digest, 2004 IEEE MTT-S International*, 2004, pp. 1217-1220.

[23] V. Camarchia, V. Teppati, S. Corbellini, and M. Pirola, "Microwave Measurements. Part II-Nonlinear Measurements," *IEEE Instrumentation & Measurement Magazine,* vol. 10, pp. 34-39, 2007.

[24] Z. Aboush, J. Benedikt, and P. TASKER, "High power harmonic active load-pull using broadband impedance transformers," in *High frequency postgraduate student colloquium*, 2004, pp. 145-150.

[25] Z. Aboush, J. Lees, J. Benedikt, and P. Tasker, "Active harmonic load-pull system for characterizing highly mismatched high power transistors," in *IEEE MTT-S International Microwave Symposium Digest, 2005.*, 2005, p. 4 pp.

[26] D. Rytting, "Network analyzer error models and calibration methods," *White Paper, September,* 1998.

[27] I. Cree, "CGH40006P 6 W, RF Power GaN HEMT," ed, 2015.

[28] R. Pengelly, C. Fager, and M. Ozen, "Doherty's Legacy: A History of the Doherty Power Amplifier from 1936 to the Present Day," *IEEE Microwave Magazine,* vol. 17, pp. 41-58, 2016.

[29] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE microwave magazine,* vol. 7, pp. 42-50, 2006.

[30] S. C. Cripps, *Advanced techniques in RF power amplifier design*: Artech House, 2002.

[31] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, *et al.*, "Power amplifiers and transmitters for RF and microwave," *IEEE transactions on Microwave Theory and Techniques,* vol. 50, pp. 814-826, 2002.

[32] L. Piazzon, R. Giofre, P. Colantonio, and F. Giannini, "Investigation of the am/pm distortion in doherty power amplifiers," in *Power Amplifiers for Wireless and Radio Applications (PAWR), 2014 IEEE Topical Conference on*, 2014, pp. 7-9.

[33] L. C. Nunes, P. M. Cabral, and J. C. Pedro, "AM/PM distortion in GaN Doherty power amplifiers," in *Microwave Symposium (IMS), 2014 IEEE MTT-S International*, 2014, pp. 1-4.

[34] L. Piazzon, R. Giofre, R. Quaglia, V. Camarchia, M. Pirola, P. Colantonio, *et al.*, "Effect of load modulation on phase distortion in doherty power amplifiers," *IEEE Microwave and Wireless Components Letters,* vol. 24, pp. 505-507, 2014.

[35] M. Özen and C. Fager, "Symmetrical doherty amplifier with high efficiency over large output power dynamic range," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1-4.

[36] M. Özen, K. Andersson, and C. Fager, "Symmetrical Doherty power amplifier with extended efficiency range," *IEEE Transactions on Microwave Theory and Techniques,* vol. 64, pp. 1273-1284, 2016.

[37] C. Inc., "Cree CGH40010," vol. Rev 4.0, ed, 2015.

[38] R. Corporation, "RO4350B datasheet," in *RO4000® Series High Frequency Circuit Materials*, ed, 2016.

[39] D. M. Pozar, *Microwave engineering*: John Wiley & Sons, 2009.

[40] Y. Chung, C. Hang, S. Cai, Y. Chen, W. Lee, C. Wen, *et al.*, "Effects of output harmonic termination on PAE and output power of AlGaN/GaN HEMT power amplifier," *IEEE microwave and wireless components letters,* vol. 12, pp. 421-423, 2002.

[41] D. Y.-T. Wu and S. Boumaiza, "10W GaN inverse class F PA with input/output harmonic termination for high efficiency WiMAX transmitter," in *Wireless and Microwave Technology Conference, 2009. WAMICON'09. IEEE 10th Annual*, 2009, pp. 1-4.

[42] S. Gao, P. Butterworth, S. Ooi, and A. Sambell, "High-efficiency power amplifier design including input harmonic termination," *IEEE Microwave and Wireless Components Letters,* vol. 16, pp. 81-83, 2006.

[43] M. Akmal, J. Lees, S. Bensmida, S. Woodington, V. Carrubba, S. Cripps, *et al.*, "The effect of baseband impedance termination on the linearity of GaN HEMTs," in *Microwave Conference (EuMC), 2010 European*, 2010, pp. 1046-1049.

[44] Anritsu, "Universal Test Fixture 3680 Series," *Technical Data Sheet,* 2013.

[45] W. Hallberg and C. Fager, "Current scaled Doherty amplifier for high efficiency and high linearity," in *Microwave Symposium (IMS), 2016 IEEE MTT-S International*, 2016, pp. 1-4.