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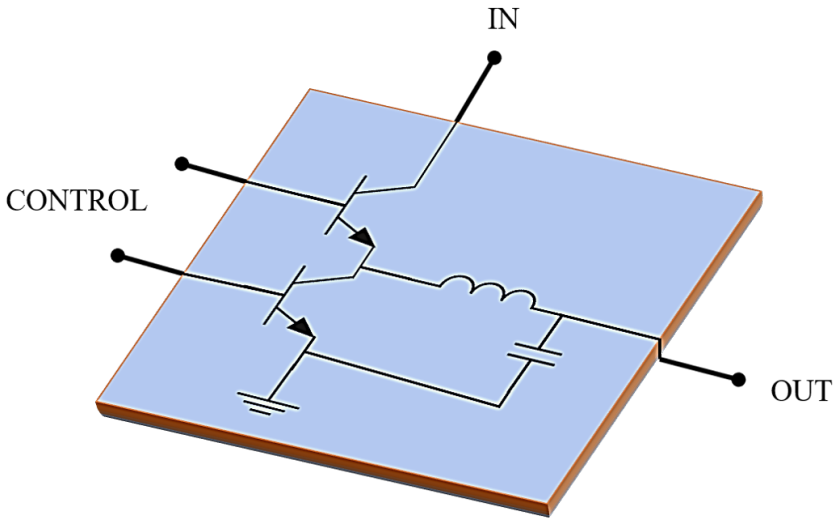

Power System-on-Chip for Future Airborne Sensor Systems

Feasibility Analysis

Master's thesis in Wireless, Photonics and Space Engineering

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Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2019

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Cover: Illustration of a power System-on-Chip in the form the power stage of a conventional Buck converter.

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Abstract

This thesis looks into the requirements on technology to realize a fully integrated GaN power System-on-Chip for a switched mode DC-to-DC converter that could be used in future airborne sensor systems. A fully integrated power stage would save much space and weight, which is beneficial in any application and, especially, for airborne applications. The topologies considered include conventional Buck-type converters, interleaved Buck converters and switched capacitor converters. The target input voltage is 270 V and the power stage conversion ratio is 10-to-1. Focusing primarily on optimizing steady state efficiency the necessary integrated passive components are designed and simulated. It is identified that an advanced technology for multi-layered or very thick conductors is a requirement, and based upon these two new inductor topologies are proposed. The multi-layered inductors utilize two coupled layers of 5 µm thick spiral conductors and the very thick inductors use a single conductor layer with a 30 µm conductor. A simple linear model is also presented to describe the most important performance characteristics for commercial GaN devices, the correlation between parasitic drain-source capacitance and the maximum tolerated drain-source voltage and current. Finally, complete power stage design examples are presented alongside approximate on-chip area requirements for the analyzed active and passive components. The performance of the designs are verified with simulations and the multi-layered inductors provide power stages with optimum efficiencies of 46% to 65% at switching frequencies in the 70 to 150 MHz range. The very thick inductors reach efficiencies of 61% to 71% operating at 40 to 80 MHz.

Keywords: Power, System-on-Chip, GaN, DC-to-DC, Converter, Buck, MMIC, Multi-layer, BCB, Inductor.

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Emil Bjärehäll, Gothenburg, May 2019

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List of Abbreviations

2DEG Two Dimensional Electron Gas. 9

ADS Advanced Design System™. 27, 28, 42, 58
AESA Active Electronically Scanned Array. 1, 5

BC Buck Converter. 14, 15, 17–20, 27, 28, 30–36, 51–53, 55–61

CMO Continuous Mode Operation. 17–20, 25, 32, 35, 39, 53, 57, 58
CMOS Complementary Metal Oxide Semiconductor. 25

DMO Discontinuous Mode Operation. 17

ESR Equivalent Series Resistance. 19, 20, 27, 31, 35, 39, 40, 42, 43, 45, 47, 52–58, 61, 62

FCMO Forced Continuous Mode Operation. 18, 19, 31
FEM Finite Element Method. 42, 49, 54
FoM Figure of Merit. 3, 7, 11

HEMT High Electron Mobility Transistor. 5, 8, 9, 27, 51

IBC Interleaved Buck Converter. 20–22

LP Low Pass. 4, 14, 15, 61

MIBC Modified Interleaved Buck Converter. 22, 23, 32–35, 55–57, 61
MMIC Monolithic Microwave Integrated Circuit. 2, 3, 39, 43, 61, 62

PA Power Amplifier. 1, 2, 5, 9, 62, 63

RF Radio Frequency. 2, 8, 9, 28

SCC Switched Capacitor Converter. 12, 23, 36, 37, 58–61
SoC System-on-Chip. 2, 5, 40, 62

VSDR Voltage Step Down Ratio. 3, 4, 12, 13, 17, 18, 20, 21, 25, 36, 58, 59, 61

WBG Wide Band Gap. 2, 9

ZVS Zero Voltage Switching. 23, 25, 30

List of Symbols

$\Delta\phi$	IBC or MIBC branch phase difference	[rad]
Δi_{p2p}	Inductor flywheel current ripple peak-to-peak	[A]
$\Delta V_{\text{out, p2p}}$	Output voltage ripple	[V]
ϵ_0	Permittivity of free space	$[\text{m}^{-3}\,\text{kg}^{-1}\,\text{s}^4\,\text{A}^2]$
η	DC-to-DC converter efficiency	[−]
ω	Angular frequency	$[\text{rad}\,\text{s}^{-1}]$
VSDR	The ratio $V_{\text{in}}/V_{\text{out}}$	[−]
A	Parallel plate area for integrated capacitors	$[\text{m}^2]$
C_1	Transfer capacitor 1 in SCC topology	[F]
C_2	Transfer capacitor 2 in SCC topology	[F]
C_{f}	Flywheel capacitance	[F]
$C_{\text{oss-H}}$	High side device specific C_{oss}	[F]
$C_{\text{oss-L}}$	Low side device specific C_{oss}	[F]
C_{oss}	Parasitic output capacitance	[F]
C_{o}	Output filter capacitor for the SCC topology	[F]
C_{t}	Coupling capacitor in MIBC topology	[F]
d	Plate separation in parallel plate capacitor	[m]
$D_{\text{high, ON}}$	Duty cycle of high side ON-state	[−]
E_{BD}	Breakdown electric field strength	$[\text{V}\,\text{cm}^{-1}]$
f_{sw}	Switching frequency	$[\text{s}^{-1}]$
i^+	Inductor current increase at flywheel charging	[A]
i^-	Inductor current decrease at flywheel discharge	[A]
$i_{\text{ds, max}}$	Maximum rated transistor drain-source current	[A]

i_{in}	Input current to a DC-to-DC converter	[A]
i_{L}	Inductor flywheel current	[A]
i_{max}	Maximum instantaneous current in BC topology	[A]
i_{out}	Output current of a DC-to-DC converter	[A]
k	Relative permittivity constant	[−]
L_{f}	Flywheel inductance	[H]
N	Number of IBC or MIBC branches	[−]
P_{cond}	Power loss brought by device R_{ON}	[W]
P_{Coss}	Power loss brought by parasitic device capacitance	[W]
P_{ESR}	Power loss brought by inductor ESR	[W]
P_{gate}	Power loss brought by device gate charging	[W]
P_{in}	Injected power to a DC-to-DC converter	[W]
P_{loss}	Total power loss for a DC-to-DC converter	[W]
P_{out}	Output power of a DC-to-DC converter	[W]
P_{sw}	Power loss brought by finite switching speed	[W]
R_{load}	The resistive output load of a DC-to-DC converter	[Ω]
R_{ON}	Drain-source resistance of a device in its ON state	[Ω]
T_{sw}	Period time at switching frequency f_{sw}	[s]
V_{BD}	Maximum rated transistor drain-source voltage	[V]
V_{ds}	Drain-source voltage of a transistor	[V]
V_{out}	Output voltage of a DC-to-DC converter	[V]
v_{sat}	Carrier saturation velocity	[$\text{cm}\,\text{s}^{-1}$]
w	Widening parameter	[−]
Z	Impedance	[Ω]
Z_0	Characteristic impedance	[Ω]

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1
Introduction

Starting with the global electrification in the early 1900s a great portion of the energy demands by modern civilization has been towards the generation of electricity. A growing population, an ever more convenient way of life and globalization has spurred the development and research of new and more efficient ways of producing, transporting/transforming and using electricity. In 2014 the global production of electricity reached 23.8 PWh, which constitutes roughly 1/5 of the global energy consumption at 109.6 PWh [1]. The same year, it is reported that 8.3% of the generated electricity is lost in transformation and distribution [2]. Consequently, all development and research towards a better performing electricity supply chain, from generation to end-use, is both relevant and important for finding solutions to the omnipresent problems of environmental issues, sustainability, and management of natural resources.

1.1 Background

As a manufacturer of advanced airborne sensor systems, Saab is continuously pursuing better performing, more efficient, lighter and spatially smaller electrical components and subsystems to remain competitive on the defense market. Consequently, the strive for developing fully integrated circuits to replace discrete implementations is self-explanatory. As an example, modern active electronically scanned array (AESA) Radars use hundreds of active antenna elements and creates opportunities for advanced beam-forming and using the same system for a multitude of different surveillance tasks. Consequently, there is a need for a method to efficiently supply and modulate the bias of the PA in each antenna element. Both rapidly, and with a small, preferably completely integrated, circuit since one is needed for each element. Especially, the importance of minimizing the size and weight cannot be stressed enough, as hardware moves closer to the antenna in modern AESA systems the associated power supply chains pose a major bottleneck.
It is in Saab's interest to continuously monitor developments within highly efficient, fast, integrated power electronics and investigate where and to which extent it can be implemented in Saab's range of products.

1.1.1 Integrated and Discrete DC Voltage Converters

In literature there is a clear separation within the field of sub 1.5 kV DC-to-DC converters into two system types, namely discrete implementations and fully integrated

implementations. Understandably, for voltages closer to the high end at 1.5 kV and high power levels implementations tend towards physically larger designs based on discrete (i.e. lumped) components. At the other end, with voltages closer to the supply needs of modern integrated circuits at a maximum of 4 V a need for rapid voltage modulation and space constraints has brought forth fully integrated voltage converters and System-on-Chip (SoC) solutions as the dominant design in many applications [3]. The existing power SoC achieve full integration by increasing the frequency of operation, which lowers the required passive component values [4].
Interestingly, while lumped realizations of DC voltage converters are easily found at any voltage and power level the fully integrated systems are constrained at low voltages and often by operation at frequencies inherited from their discrete counterpart. While much progress has been made on realizing fully integrated voltage converters at a few volts that can be modulated at an ever higher maximum rate, such as in [5, 6], it is very seldom that such a design will challenge the maximum voltage and power levels instead of the control speed. Higher power and voltage fully integrated DC voltage converters exist in a limbo between lumped electric power circuits and MMIC RF circuits. This gap is very interesting for achieving much higher power density for voltage converters and, together with the rapid development of WBG materials, such as GaN (Gallium Nitride), over last decades, a revolution of this sector of voltage converters could be at hand [7].

1.1.2 GaN for Higher Power Density

With conventional Si-based MOSFETs, efforts towards increasing the maximum voltage tolerances of fully integrated converters are not lucrative. While the Si-based processes are very mature and indeed ideal for creating low voltage, fully integrated, DC-to-DC converters the material enforces strict limits as the voltage and power level is increased. WBG materials such as GaN feature much higher breakdown fields at similar electron mobility as Si, which makes smaller devices with higher voltage ratings a possibility [7]. Despite that these properties have long been known the lagging maturity of GaN processes initially hindered development in the power electronics sector.
However, with its well-suited material properties for high voltage applications, GaN developed rapidly as the high-performance material of choice for PAs, for example within radar- and communication-systems [7, 8]. During the last decades this development has continued and, piggybacking on the successful RF systems, GaN only very recently started emerging as an alternative semiconductor material for power electronics, promising higher power density [7].
An example of the benefits of WBG materials was demonstrated in 2016 during the Google/IEEE Little Box Challenge. The competition encouraged companies to develop the smallest possible 2 kW inverter with an efficiency of $\geq 95\%$. The winning design utilized a highly integrated design based on GaN as opposed to more conventional Si. A conventional 2 kW inverter in Si can reach a power density of approximately $0.2\,\mathrm{kW\,dm^{-3}}$, using integrated GaN the best design reached a power density of $8.85\,\mathrm{kW\,dm^{-3}}$ [9].
Decreasing converter size and weight is not without its challenges. Typical high-

efficiency voltage converters are of switched mode type, i.e. they utilize periodically switched active components together with passive components to transform the voltage. The physical size and weight of the voltage converter system depend heavily on the size of the passive components which in turn depends on the rate at which the active components are switched, the switching frequency f_{sw} [4, 6]. Essentially, the required size of every passive component will decrease with increasing f_{sw} meaning that higher switching frequencies should imply a smaller and lighter converter [6]. However, difficulties arise as high switching frequencies require smaller active components to keep the parasitic effects at a minimum and smaller devices feature lower voltage tolerances and higher resistance values. Also, MMIC passive components have much higher parasitic resistive losses in comparison to their larger counterparts which degrades the efficiency of fully integrated designs [6].

1.2 Power System-on-Chip

The focus of this work will rapidly turn to switched mode DC-to-DC converters since these types of converters can successfully provide both component values that could make full integration possible and high efficiency, a Figure of Merit which is of highest priority [4]. In Figure 1.1 a schematic view of a conventional Buck-type switched-mode DC-to-DC converter is shown. This work will focus on the highlighted power stage which is the most crucial part of any switched mode voltage converter. The specifics of the power stage components, the transistors, and passive filter components, mandates the capabilities of the entire converter system in terms of what switching frequency, size, voltage step down ratio (VSDR), power and efficiency that is obtainable. As an inspiration, in [10], a fully integrated AC-transformer was developed with inductors that push the limits of integrated passive performance and many GaN transistors already exist that can tolerate voltages up 600 V meaning that fully integrated DC converters at voltages much higher than a few volts is not an unreasonable request. It remains to study how well the performance of existing active devices translates to lower voltages and higher frequencies and to what extent the high-performance passive components can be mimicked in the Chalmers In-House GaN process.
The remaining subsystems will not be analyzed in detail and will only be briefly described in the coming Sections. The transistor drive stage is mandatory to operate the DC-to-DC converter but the feedback circuitry, additional LP-filtering at input and output and galvanic isolation from the high voltage source are optional, depending on the system requirements for input/output ripple and safety.

1.2.1 Transistor Drive Stage and Feedback Circuitry

Switched mode converters necessitate control circuitry to drive the active components, which is generally done by modulating the gate-source voltage to switch the transistors T1 and T2 between their ON and OFF-states. The details of this switching schedule will determine the VSDR and the purpose of the drive stage is to provide the voltage waveforms to the gates of T1 and T2 that gives the wanted, not necessarily constant in time, VSDR and V_{out}. The drive circuitry can operate

with or without feedback circuitry that creates a control loop that can be used for more precise steering towards a varying or invariant target output voltage.

1.2.2 Galvanic Isolation

For safety reasons, galvanic isolation between the high voltage side and low voltage side is demanded in any practical implementation of a DC-to-DC converter with a large VSDR. This could in practice be added as a pre- or post-stage in the converter schematic from Figure 1.1 and its purpose is to eliminate the possibility of any direct metallic contact between the input and output side. This would eliminate a potential current rush through the converter, to sensitive lower voltage components, in case a transistor or any other crucial component fails.

1.2.3 Input and Output Filtering

The voltage source which generates the high input DC voltage (which in many applications is an AC generator together with an AC-to-DC converter) cannot, in general, be assumed to respond instantaneously to changes in current draw. Therefore, input low-pass filtering is implemented in DC-to-DC converters to decouple the rapid, f_{sw}, changes in current draw from the output of the generator. Moreover, additional LP filtering (besides the LP characteristics of the L_{f} and C_{f} combination that is included in the power stage from Figure 1.1) could be necessary at the output of the DC-to-DC converter since a ripple with frequency f_{sw} is superpositioned on the DC signal V_{out}.

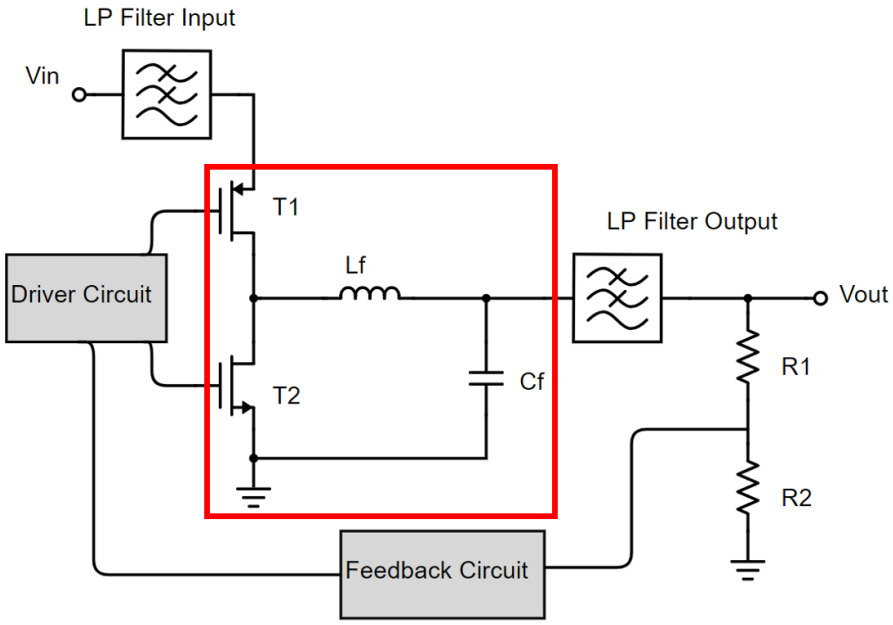


Figure 1.1: The DC-to-DC power stage of a switched mode Buck converter highlighted in red. Together with the feedback circuitry, the transistor driver stage, input and additional output filtering the power stage converters a high DC voltage `Vin` to a low lower DC voltage `Vout`. Not shown is a possible galvanic isolation stage that could be added as a pre- or post-stage.

1.3 Aim

The aim of this thesis is to develop a fully integrated GaN DC voltage converter power stage, an integral part of a power SoC, to be used in airborne sensor systems and investigate what requirements this poses for the active and passive components. In an airborne AESA radar system many steerable DC-to-DC converters, ideally one per PA and antenna element, would be beneficial for system performance. Meaning that compactness is of high priority and the relevant input/output voltage levels are set by the electrical standards of the aviation industry. As a reference the interface standard *Aircraft Electric Power Characteristics* by the US Department of Defense [11] standardizes the onboard DC supply voltage to 270 V and 28 V which has resulted in PAs that most commonly utilize 28 V biasing. Consequently, a DC-to-DC converter that steps down 270 V to 28 V would be most appropriate for existing standards.
At the same time, more compact and efficient DC-to-DC converters capable of high-frequency modulation have a much broader appeal as well. The aforementioned Little Box Challenge is a good example of how large space and weight reductions can be once the level of integration increases, even in consumer electronics. As an example, similar size and weight reductions can, in theory, be achieved for phone chargers, laptop chargers, and transformers in electric vehicles [4].

1.4 Report Structure

In Chapter 2 a brief overview of the material properties of GaN and the development of GaN HEMTs is presented, a more detailed explanation to why GaN is preferable over Si and SiC is also given. Chapter 3 describes different DC-to-DC converter topologies and their respective requirements of passive components with a theoretical approach and in Chapter 4 the performance of the most suitable topologies is verified through simulations. In Chapter 5 a design space for the passive components extending the Chalmers In-House GaN process is established by simulations and measurements. Lastly, Chapter 6 presents schematic design drafts of fully integrated voltage converter stages and concluding remarks, including suggestions for future work, are found in Chapter 7.

2
GaN HEMT Technology

Traditionally, either Si or SiC has been used in voltage converters at low (up to 48 V) and high voltage levels respectively. As seen in Table 2.1 [12] the fairly high mobility of Si allows for high-frequency switching and miniaturization of DC-to-DC voltage converters, while the high breakdown field of SiC allows for high voltage levels, even up to 1 kV [4]. GaN combines these two strengths and allows for both high-speed switching and high voltages [4].
Another figure of merit important for efficient power conversion is the achievable ON-resistance R_{ON} as a function of the breakdown voltage. As seen in Table 2.1, for SiC the theoretical lower limit for R_{ON} at a breakdown voltage of 1000 V is on the order of $10^{-2}\ \Omega\,\mathrm{mm}^2$ while GaN has a theoretical minimum ON-resistance on the order of $10^{-3}\ \Omega\,\mathrm{mm}^2$ [8]. A lower R_{ON} brings smaller losses during conduction, which helps improve the efficiency of any voltage converter.
Moreover, the Johnson figure of merit [13],

$$\mathrm{FoM}_{\mathrm{Johnson}} = \frac{v_{\mathrm{sat}} E_{\mathrm{BD}}}{2\pi} \tag{2.1}$$

is a relevant measure for how well suited a material is for high power applications, where v_{sat} is the saturation velocity and E_{BD} is the breakdown field strength. As seen in Table 2.1 the $\mathrm{FoM}_{\mathrm{Johnson}}$ of GaN is roughly 60% higher compared to SiC.

Table 2.1: Comparison of some electrical properties of Si, SiC, and GaN at 300 K.

	Si	**SiC (6H)**	**GaN**
Band Gap [eV]	1.12	3.03	3.45
Electron Mobility [$\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}$]	1500	500	1250
Hole Mobility [$\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}$]	600	20	850
Breakdown Field [$\mathrm{kV\,cm}^{-1}$]	300	2500	3300
Sat. Velocity [$10^7\ \mathrm{cm\,s}^{-1}$]	1	2	2.5
$\mathrm{FoM}_{\mathrm{Johnson}}$ [$10^{11}\mathrm{V\,s}^{-1}$]	4.8	79	131
Minimum R_{ON} [$\Omega\,\mathrm{mm}^2$][A]	$\approx 10^1$	$\approx 10^{-2}$	$\approx 10^{-3}$

[A] Order of magnitude, which gives a breakdown voltage of 1000 V

2.1 Properties of Commercial GaN HEMTs

In Figure 2.1 commercial GaN HEMTs are compared as function of their maximum rated drain-source voltage and the ratio between the parasitic output capacitance C_{oss} and the maximum drain-source current. The same is done for a selection of transistors made in Si and SiC, for details see Appendix A. Essentially, a low $C_{\text{oss}}/i_{\text{ds, max}}$ ratio allows efficient converter operation at higher frequencies and currents [5], and a high maximum breakdown voltage allows for safe operation at higher voltages. As seen in Figure 2.1 the material properties of GaN is also visible on a device level. Up to 600 V rated breakdown voltage, GaN provides the best opportunity for low loss and high-frequency operation. However, there is a clear gap of available GaN devices between the HEMTs with breakdown voltages ≤ 200 V (meant for RF applications) and HEMTs with breakdown voltages around 600 V (meant for power applications). In general, manufacturers offer the lower voltage HEMTs as bare-die devices while the higher voltage HEMTs are fully packaged, again highlighting the difference in integration level between RF and power applications, mentioned in Section 1.1.1. The airborne application, with its standardized 270 V voltage, places this work at the edge between integrated and discrete voltage converters and, consequently, in a gap of available commercial active devices. Investigating this middle ground of devices is crucial for finding what performance that is obtainable on the system level.

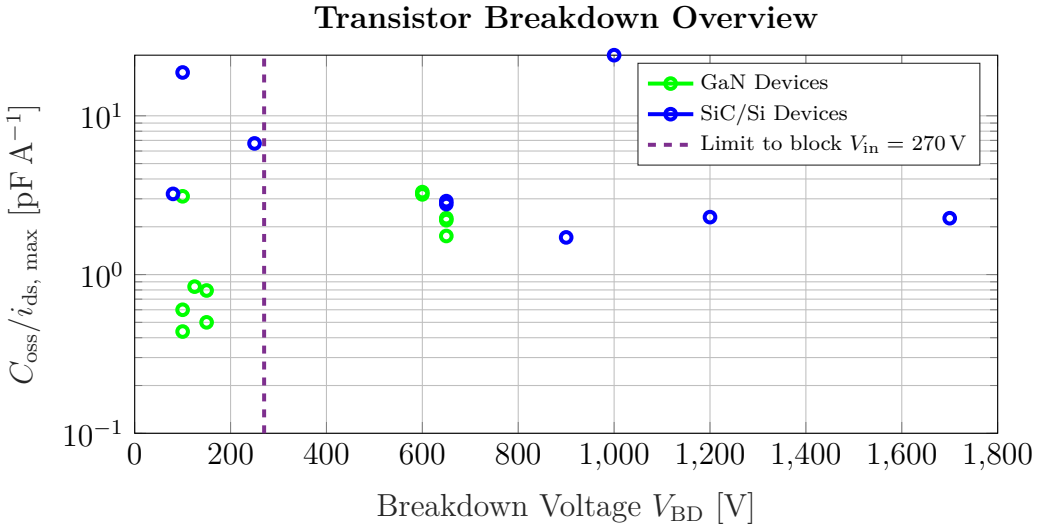


Figure 2.1: The ratio $C_{\text{oss}}/i_{\text{ds, max}}$ for different commercial devices in GaN, Si, and SiC for the respective rated breakdown voltage of each device. More details are available in Appendix A.

2.2 GaN HEMT Development

The first depletion mode GaN HEMTs was presented in the middle of the 1990s and the first commercial device was introduced by Eudyna Corp.™ in 2004 [8]. By forming heterostructure interface between AlGaN and GaN a Two Dimensional Electron Gas (2DEG) emerges at the interface which greatly enhances the electron mobility [4, 8]. This 2DEG, which was first described for GaAs in 1979 [8, 14], forms an electron channel between source and drain, and gives GaN HEMTs their inherent depletion-mode (or normally ON) characteristics [15].
AlN, which is doped with different amounts of Ga to form AlGaN, and GaN form a rather unique due of two semiconductor compounds with comparatively wide bandgaps (3.4 eV and 6 eV) and similar lattice constants (3.16 Å and 3.11 Å) [16]. The lattice alignment makes so that high quality and large semiconductor structures can be made without much material strain and the larger bandgap of the involved materials creates the foundation for devices with higher voltage tolerances. All while the higher mobility brought by the 2DEG are inherited as well. Consequently, GaN HEMTs are well suited for usage in wide bandwidth RF PAs, where both the voltage tolerances and the speed (electron mobility) are crucial parameters [17]. In RF applications, GaN competes with materials such as GaAs as the semiconductor of choice for high-speed HEMTs. GaN can operate at higher temperatures and voltages compared to GaAs which has resulted in much attention for GaN within microwave power amplifiers [7]. In 2009 the first enhancement-mode GaN HEMT was introduced, and making good use of the associated normally-OFF characteristics, applications within power electronics started to emerge in the early 2010s [5, 18, 19]. In this arena WBG materials such as GaN are again crucial for achieving higher voltage and more efficient voltage converters while at the same time allowing for an increased level of integration and miniaturization.

3

DC-to-DC Voltage Converters

This Chapter provides a brief background of DC-to-DC voltage converters. While the target function of any DC-to-DC converter is simple, either stepping up or stepping down the input voltage level, there is a large variety of different circuit topologies that offer beneficial properties in certain applications, regarding the obtainable efficiency and required passive components.

The efficiency, η, will be defined as the ratio between the average power injected into a converter P_{in} and the average power at the output delivered to a resistive load P_{out}. More precisely it holds that

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{< i_{\text{out}} >< V_{\text{out}} >}{< i_{\text{in}} >< V_{\text{in}} >} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \tag{3.1}$$

where $< \cdot >$ denotes time average. In any practical switched mode DC-to-DC converter there will be a ripple in both the input and output current and voltage levels meaning that η in general is time varying. Since ripple is unwanted and often small compared to the average voltages and currents the η time-average definition in (3.1) suffices as a FoM for comparison.

3.1 Resistive Voltage Divider

The simplest possible DC-to-DC voltage converter is the resistive voltage divider, presented in Figure 3.1. This converter uses simple voltage division across two series resistors, R_1 and R_2. The relationship between V_{in} and V_{out} for an open load is simply

$$V_{\text{out}} = \frac{R_2}{R_1 + R_2} V_{\text{in}} \tag{3.2}$$

and, to get a voltage step-down ratio of 10, R_1 should be chosen as $9R_2$.

The resistive voltage divider is very lossy, and consequently seldom used in practice. However, the resistive voltage divider provides a minimum efficiency which any other more complex topology must surpass to be worthwhile. A 270 V to 28 V resistive voltage divider operating at an output power of 30 W at a 50 Ω load would have a theoretical efficiency of around $\eta = 10\%$. Any DC-to-DC converter must as a system (including driver and control circuitry) offer higher efficiency than this to be a better solution.

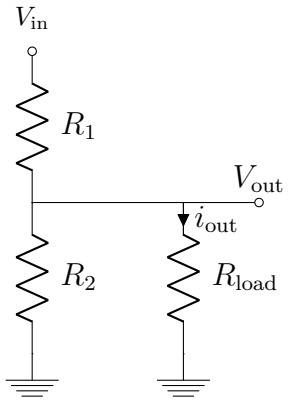


Figure 3.1: Schematic of the simplest DC-to-DC converter, the resistive voltage divider.

3.2 Switched Capacitor Converter

There exist many different versions of DC-to-DC converters that could be categorized as switched capacitor converters (SCC) [20]. These converters make use of active components, transistors, and drive circuits that control their switching between the conducting ON-state and non-conducting OFF-state to charge and discharge capacitors in a periodic fashion [21].

In figure 3.2 the topology a of SCC proposed in [19] is presented. By toggling transistors T1-T8 according to a specific schedule, at any switching frequency f_{sw}, it is possible to series charge capacitors C_1 and C_2 with V_{in} and then discharge C_1 and C_2 in parallel, yielding a VSDR of 2 and $V_{\text{out}} = 0.5V_{\text{in}}$ [19]. The very same topology, applying a different control sequence of transistors T1-T8, can perform either the inverse operation, i.e. operate at a voltage step up ratio of 2, or simply pass the voltage V_{in} to V_{out} at a voltage conversion ratio of unity. More specifically, the device control sequence required for any of the three possible operation states is presented in Table 3.1 [19].

Besides the series-parallel type of switched capacitor converter that is presented in Figure 3.2, there exist other types, utilizing different proportions of switches, diodes, and capacitors to perform the same task [21]. In general, switched capacitor converters feature no easy way of actively changing the voltage conversation ratio by manipulating the control sequence, the VSDR is fixed for a particular choice of components [19, 22]. At least if optimum efficiency is sought [20]. However, designing around more than two capacitors (and adding more active elements in conjunction) can allow for an arbitrary integer or rational VSDR [22]. Furthermore, it should be noted that a voltage ripple, consisting of f_{sw} and its harmonics, will be present at the output port V_{out}. Consequently, a filtering capacitor C_{o} is often added in parallel at the output to suppress the ripple to a tolerable level [19].

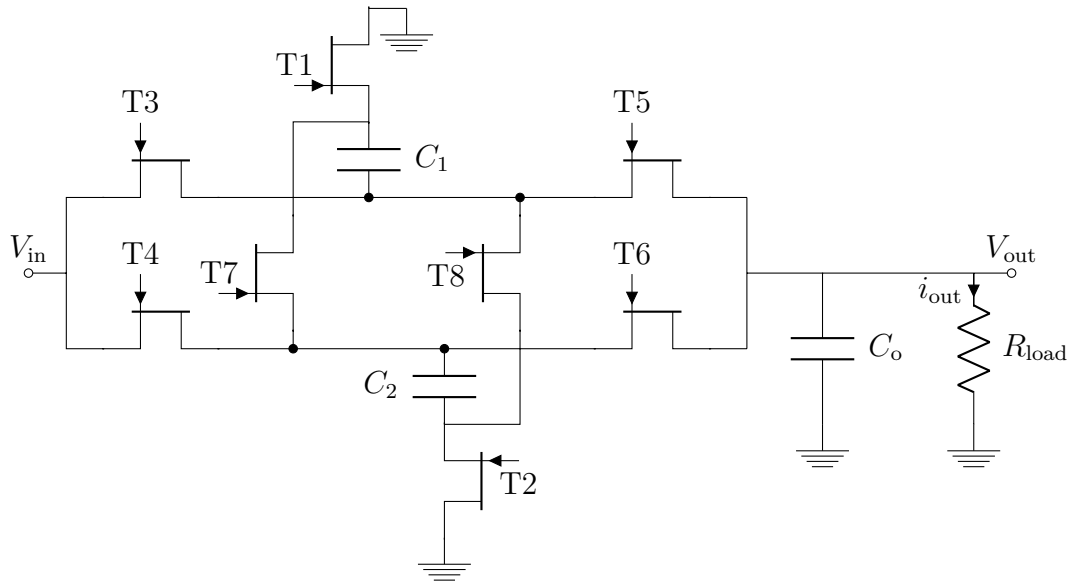


Figure 3.2: Series-parallel switched capacitor converter capable of a fixed VSDR of 2. By operating T1-T8 with different control schemes (from Table 3.1) conversion ratios of 1-to-1 and 1-to-2 are also possible.

Table 3.1: Control schedule for devices in the switched capacitor converter from Figure 3.2 in its three different modes. State A and B both have a duty cycle of 50%.

Voltage conversion	ON in state A	ON in state B
2:1	T1 T4 T5 T8	T2 T3 T6 T7
1:1	T1 T4 T5 T8	T1 T4 T5 T8
1:2	T1 T3 T6 T8	T2 T3 T6 T7

3.2.1 Ideal Switched Capacitor Converter Passive Requirements

There is a link between the transfer capacitance of $C_1 = C_2 = C_{\text{trans}}$, the switching frequency f_{sw} and the voltage conversion ratio. Considering a VSDR of 2 each capacitor acquires a charge of Q each ON period, assuming the charging current is large or the time period long enough, where

$$Q = C_{\text{trans}} \frac{(V_{\text{in}} - V_{\text{out}})}{2}. \tag{3.3}$$

Similarly, in every OFF period, both capacitors are discharged and a charge of $2Q$ flows to the output. Consequently, with a switching frequency of f_{sw} the maximum average output current i_{out} is

$$i_{\text{out}} = 2Qf_{\text{sw}} = C_{\text{trans}} (V_{\text{in}} - V_{\text{out}}) f_{\text{sw}}. \tag{3.4}$$

As an example the required capacitance C_{trans} required for a switched capacitor converter with an input of $V_{\text{in}} = 270\,\text{V}$ and a VSDR of 2 is plotted as a function of switching frequency for different output currents in Figure 3.3.

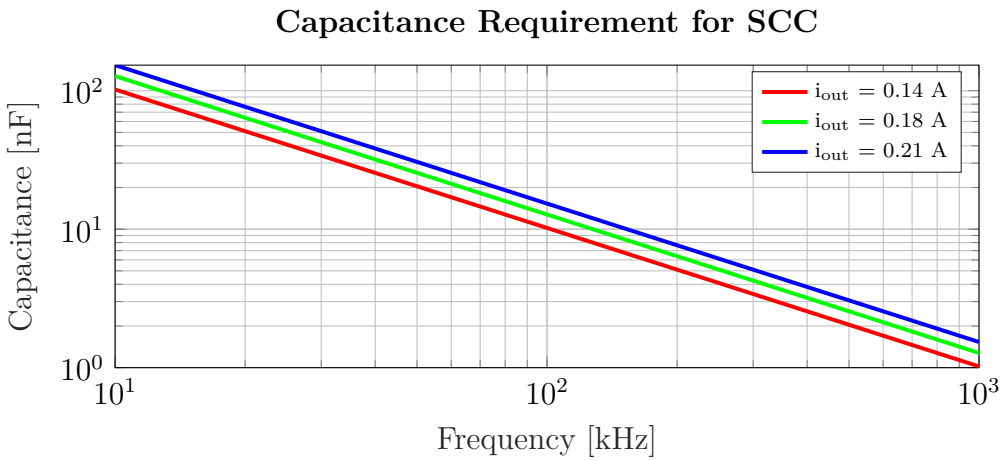


Figure 3.3: Required transfer capacitance values as a function of switching frequency for currents representing an output power of approximately 20 W, 25 W and 30 W respectively. Here $V_{in} = 270$ V.

3.3 Buck Converter

One of the most common switched-mode DC-to-DC converter topologies is the Buck Converter (BC). This voltage converter utilizes switching either a single transistor and a diode (nonsynchronous) or two transistors (synchronous) to perform the desired voltage conversion [23, 24, 25]. Together with passive components C_f and L_f forming a flywheel circuit. The nonsynchronous and synchronous Buck converter is presented in Figure 3.4 and 3.5 respectively.

The operation of the two variants is similar, the high side transistor TH is opened to charge the flywheel circuit. In the case of the nonsynchronous BC the diode will conduct and discharge the same circuit as soon as TH is closed. In a synchronous topology the low side transistor TL is opened after closing TH allowing for the same discharging procedure but with greater abilities to control the timing between switching of TL [24]. In either case, when the high side transistor toggles between ON and OFF the node voltage above TL, or the diode, assumes either the input voltage V_{in} (TH is ON) or approximately 0 V (TH is OFF). In the synchronous case, the low state of the node voltage is affected by the ON-resistance of the device and in the nonsynchronous case, this voltage is mandated by the properties of the diode. Ideally, this node voltage switches instantaneously between the two states giving rise to a square wave. The flywheel passives, C_f and L_f act as a low pass (LP) filter, suppressing the high frequency components of the square voltage wave yielding an average DC voltage [26]. By manipulating the ratio between the ON and OFF state for the high side transistor this average voltage can be set to an arbitrary level lower than V_{in}. However, depending on the combination of passive components, the switching frequency f_{sw} and the output current (output load) the Buck converter can reach different modes of operation [26].

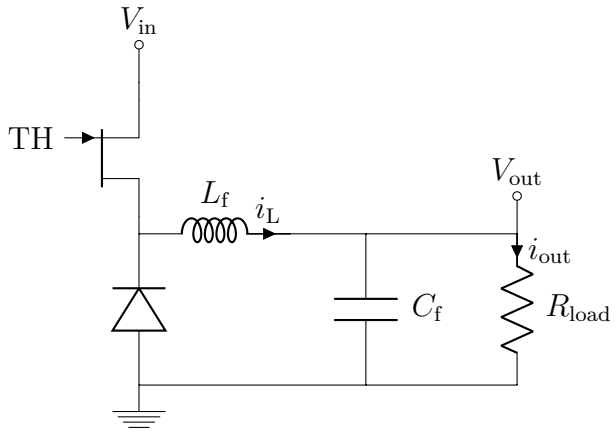


Figure 3.4: Schematic view of a nonsynchronous Buck converter, one control signal is supplied to transistor TH to switch between the ON and OFF state.

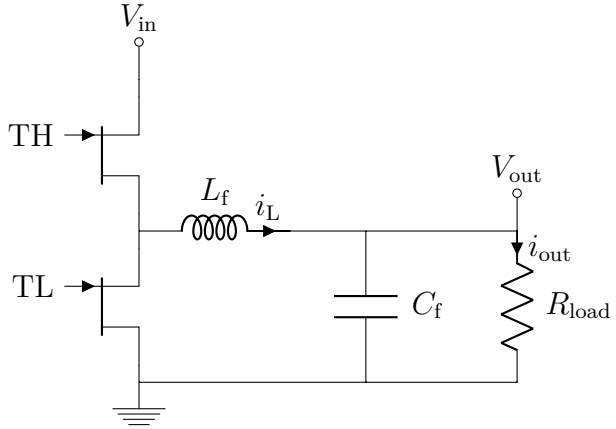


Figure 3.5: Schematic view of a synchronous Buck converter. Different control signals are fed to the gates of transistors TH and TL to make them act like opposing switches.

3.3.1 Buck Power Stage Operation

Assuming the case of a synchronous BC with ideal control signals operating at f_{sw}, the high side transistor is toggled in a square wave fashion so that it is in its ON state with a duty cycle $D_{\text{high, ON}}$ and the low side transistor is ON whenever the high side transistor is OFF, i.e. operating with a duty cycle of $1 - D_{\text{high, ON}}$. In the ideal case, the relationship between the injected high voltage and the output voltage V_{out} is simply the average voltage in the node [23, 24],

$$V_{\text{out}} = D_{\text{high, ON}} \times V_{\text{in}}. \tag{3.5}$$

In practice, however, the voltage V_{out} will fluctuate slightly as the inductor L_{f} and capacitor C_{f} is charged and discharged. In other words, the LP filter formed by passives will not be ideal, and a ripple composed of f_{sw} and its harmonics, will be present in V_{out}. Moreover, any parasitic resistive losses in the circuit will contribute with some voltage drops that lowers V_{out} below the level expressed in (3.5) [27]. To compensate this, $D_{\text{high, ON}}$ can be increased.

As L_f is charged (when TH is ON and TL is OFF) and discharged (when TH is OFF and TL is ON) the current through the inductor, i_L, will rise and fall at a rate determined as [24]

$$\frac{d}{dt}i_\mathrm{L} = -\frac{V_\mathrm{L}}{L_\mathrm{f}} \tag{3.6}$$

where V_L is voltage across L_f. When TH is ON it holds that $V_\mathrm{L} = V_\mathrm{in} - V_\mathrm{out}$ and from (3.6) it can be deduced that the current i_L, through the inductor towards R_load, increases linearly with time. The maximum value i_L reaches within before TH is turned OFF again, denoted i_L^+ is consequently [24, 25]

$$i_\mathrm{L}^+ = \frac{V_\mathrm{in} - V_\mathrm{out}}{L_\mathrm{f}} D_{\text{high, ON}} T_\mathrm{sw} \tag{3.7}$$

where T_sw is the period time i.e. $1/f_\mathrm{sw}$. Equivalently, (3.6) governs the decreasing rate of the current i_L as well. Once TH is OFF and TL is ON the voltage across the inductor switches polarity as now V_out is the high voltage compared to the node voltage of 0 V. During this state the inductor current decreases with i_L^- given by [24, 25]

$$i_\mathrm{L}^- = -\frac{V_\mathrm{out}}{L_\mathrm{f}}(1 - D_{\text{high, ON}})T_\mathrm{sw}. \tag{3.8}$$

Thus i_L forms a triangular current ripple, repeditivley increasing linearly with i_L^+ during $D_{\text{high, ON}}T_\mathrm{sw}$ and then decreasing with i_L^- during $(1 - D_{\text{high, ON}})T_\mathrm{sw}$ [24, 28]. At steady state the current increase and decrease are equal, it holds that $|i^-| = |i^+|$ and, the average inductor current level, $< i_\mathrm{L} >$, equals the output current $i_\mathrm{out} = V_\mathrm{out}/R_\mathrm{load}$. The inductor current i_L is schematically plotted in Figure 3.6.
The largest instantaneous current in the power stage, i_max, that both the flywheel inductor and the transistors TH and TL must withstand is the average output current i_out and the amplitude of the current ripple, at steady state this means [23]

$$i_\mathrm{max} = i_\mathrm{out} + i_\mathrm{L}^+ = i_\mathrm{out} + \left|i^-\right|. \tag{3.9}$$

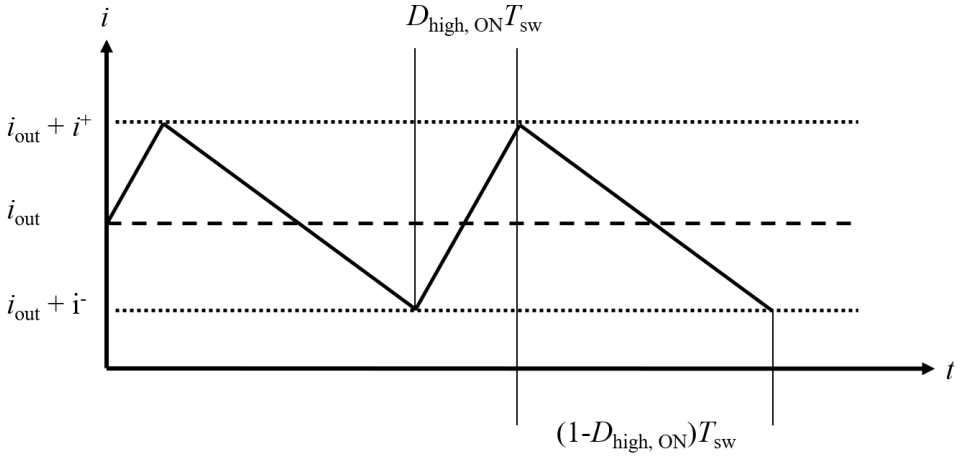


Figure 3.6: Schematic graph of the inductor current over time, in continuous mode the current oscillates between $i_\mathrm{out} + i^-$ and $i_\mathrm{out} + i^+$ while the output current of the converter is the average, i_out.

3.3.2 Continuous Mode Operation (CMO)

The criteria for continuous mode operation (CMO) is also illustrated in Figure 3.6, the inductor current remains, at all times, positive. It is easy to see that if the output current draw i_{out} is too small (e.g. brought by a too high impedance load) the low levels of i_{L} could approach zero or negative values. By definition CMO is when i_{L} is strictly positive at all times. If CMO is fulfilled the most beneficial property is that the simple relationship between duty cycle and VSDR from (3.5) is asserted and the situation is the same for both the synchronous and non-synchronous designs.
In CMO the peak-to-peak magnitude of the inductor current triangular ripple, $\Delta i_{\text{p2p}} = i_{\text{L}}^{+} + i_{\text{L}}^{-}$, is determined by the flywheel inductor L_{f} and the switching frequency f_{sw} as [23]

$$\Delta i_{\text{p2p}} = \frac{V_{\text{out}}\left(V_{\text{in}} - V_{\text{out}}\right)}{L_{\text{f}} f_{\text{sw}} V_{\text{in}}} \tag{3.10}$$

and can thus be reduced by increasing either L_{f} or f_{sw}. This current ripple through the inductor is associated with a voltage ripple, $\Delta V_{\text{out, p2p}}$, given by [28]

$$\Delta \text{V}_{\text{out, p2p}} = \frac{T_{\text{sw}} \Delta i_{\text{p2p}}}{8 C_{\text{f}}}. \tag{3.11}$$

Voltage ripple at the output of a voltage converter is in general unwanted and often and can, clearly, be reduced by a larger capacitor C_{f} in combination with high switching frequencies f_{sw}.
It should be noted that the BC has an inherent problem with light-loads, i.e. high impedance loads that draws little current. As the output current approaches 0 either L_{f} or f_{sw} from (3.10) must approach infinity to suppress the current ripple and stay in CMO. Also, higher VSDR makes the term $(V_{\text{in}} - V_{\text{out}})$ larger, further necessitating either an increase in L_{f} or f_{sw}.

3.3.3 Discontinuous Mode Operation (DMO)

If the output load of a non-synchronous Buck converter draws less current than $\Delta i_{\text{p2p}}/2$ the converter will enter discontinuous mode operation (DMO) as the flywheel inductor current becomes zero for part of one phase [24].
In the case of the non-synchronous BC the output voltage and current can still be stabilized at a desired operating point even in DMO. However, the simple relationship between input and output voltage that holds for CMO, (3.5), is no longer valid. Instead, the output voltage of a non-synchronous BC in discontinuous mode, is given by

$$V_{\text{out}} = \frac{2V_{\text{in}}}{1 + \sqrt{1 + \frac{8L_{\text{f}}}{D_{\text{high, ON}}^2 R_{\text{load}} T_{\text{sw}}}}} \tag{3.12}$$

which not only depends on V_{in} and $D_{\text{high, ON}}$ but also L_{f}, T_{sw} and the output load R_{load} [24]. For this reason, discontinuous mode non-synchronous Buck converters are usually avoided, because the control circuitry necessary for precision output voltage steering becomes very complex at these small output current levels.

3.3.4 Forced Continuous Mode Operation (FCMO)

For synchronous BC no diode will stop the inductor flywheel current from being negative and all relationships and equation for CMO can be extended to hold for average output currents smaller than Δi_{p2p} [25, 29]. For this reason, synchronous Buck converters offer easy steerability over a large spectrum of output currents and can realize the same VSDR with smaller a flywheel inductance compared to the non-synchronous topology [29]. However, with Si devices FCMO is traditionally avoided because running a current in the direction opposite of the body diode shows higher resistive loses than vice versa. Meaning that CMO is preferred over FCMO for primarily efficiency reasons. With GaN devices, which feature much lower possible R_{ON} (see again Table 2.1) FCMO might be a more attractive trade-off for smaller L_{f} and lower f_{sw}.
Furthermore, if a converter operating in FCMO is presented to an open load, and the average output current is 0 the flywheel circuit will still conduct, and consequently stand-by power consumption becomes an issue. Because of this, voltage converters that apply FCMO usually make use of auxiliary circuitry that forces the low side switch to turn OFF before entering or going to deep, into FCMO [29].

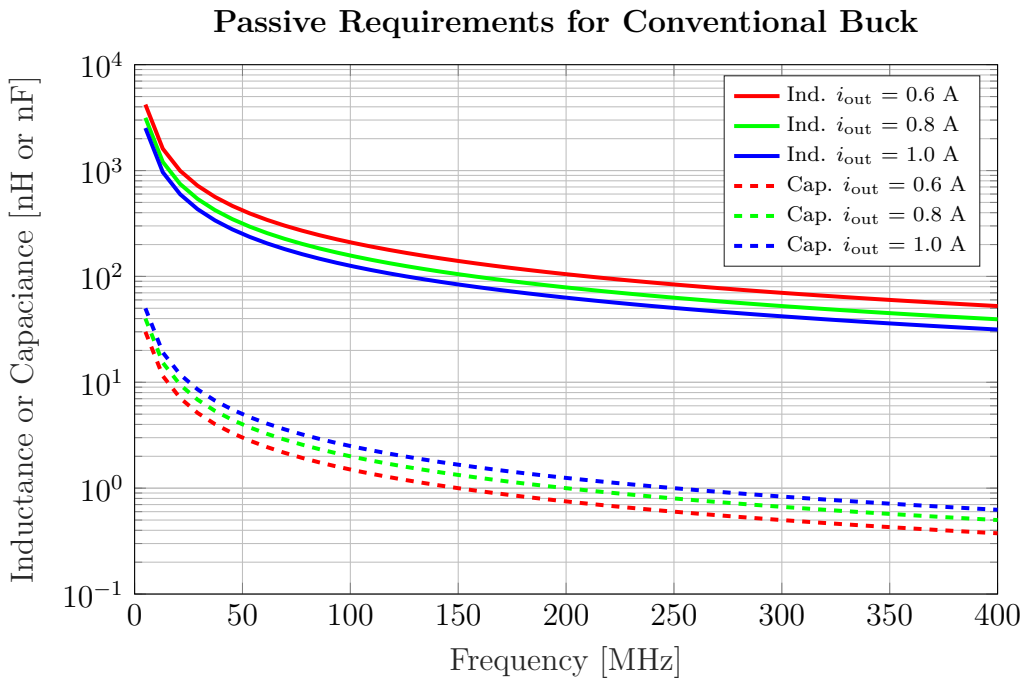


Figure 3.7: The component values for the flywheel inductor L_{f} and capacitor C_{f} as a function of switching frequency, for an ideal, 270 to 28 V, Buck converter operating at an output current of 0.6, 0.8 and 1 A (19 W, 22 W and 28 W). The inductor current ripple is the limit for CMO and the voltage ripple is fixed at 1 V peak-to-peak.

3.3.5 Ideal Buck Converter Passive Requirements

Using equations (3.10) and (3.11) the required component values for the inductor L_f and capacitor C_f can be plotted as a function of frequency for a specific input voltage, output voltage, current ripple, voltage ripple and output power level. The minimum component values for the passives in an ideal synchronous Buck converter that steps down 270 V to 28 V and operates at the edge between CMO and FCMO mode at different output current levels is presented in Figure 3.7. The CMO constraint means that the graph at every frequency represents a peak-to-peak ripple current that is twice that of the output current. The allowed peak-to-peak voltage ripple, which according to (3.11) is determined by the capacitor C_f, was arbitrarily chosen to 1 V.

3.3.6 Buck Converter Loss Factors

Assuming the same transistors are used on the high and low side of a synchronous Buck converter the conduction losses in the converter is given as [27, 30]

$$P_\mathrm{cond} = \left(i_\mathrm{out} + \frac{\Delta i_\mathrm{p2p}^2}{12} \right) R_\mathrm{ON} \tag{3.13}$$

meaning that smaller output current levels, ripple currents and ON-resistance R_ON is advantageous. Moreover, the switching loss increases with frequency as [30]

$$P_\mathrm{sw} = 0.5 V_\mathrm{in} i_\mathrm{out} \left(t_\mathrm{r} + t_\mathrm{f} \right) f_\mathrm{sw} \tag{3.14}$$

where t_r and t_f are the rise and fall time of the drain-source voltage of transistor. Also, there exist a charging loss associated with the parasitic output source-drain capacitance of each transistor. This loss can be calculated as [30]

$$P_\mathrm{Coss} = \frac{1}{2} \left(C_\mathrm{oss\text{-}L} + C_\mathrm{oss\text{-}H} \right) V_\mathrm{in}^2 f_\mathrm{sw} \tag{3.15}$$

where $C_\mathrm{oss\text{-}L}$ and $C_\mathrm{oss\text{-}H}$ denotes the output capacitance of the high and low side transistor respectively. Another charging loss associated with the active components is the gate charge loss [27, 30],

$$P_\mathrm{gate} = \left(Q_\mathrm{G\text{-}L} + Q_\mathrm{G\text{-}H} \right) V_\mathrm{gs} f_\mathrm{sw} = \left(C_\mathrm{G\text{-}L} + C_\mathrm{G\text{-}H} \right) V_\mathrm{gs}^2 f_\mathrm{sw} \tag{3.16}$$

where $C_\mathrm{G\text{-}H}$ and $C_\mathrm{G\text{-}H}$ is the gate capacitance of each transistor. This gate charging loss will represent a minimum power the driver circuitry must deliver to the gates of the transistors to effectively toggle them between their ON and OFF states. Lastly, any real passive component will feature some parasitic equivalent series resistance (ESR) which will induce a voltage drop and power loss. This is most notable for the flywheel inductor, and the associated losses can be easily calculated as [30]

$$P_\mathrm{ESR} = \mathrm{ESR}_\mathrm{inductor} \times i_\mathrm{out}^2. \tag{3.17}$$

Traditionally, the dominating loss factors for conventional BC is the conduction loss (3.13) followed by the switching loss (3.14) and the charge loss (3.15). If a fully integrated design is not sought, switching frequencies in the 10 to 500 kHz suffices

in keeping the switching losses low while the lumped components, and transistors, offer sufficiently small system size and high efficiency. As seen in Table 2.1 the ON-state resistance of GaN semiconductors is an order of magnitude smaller than SiC, meaning that GaN as a material promises lower conduction losses for any converter design [31]. Moreover, GaN transistors feature approximately 6 times lower gate charge levels, Q_{G} when compared to SiC and smaller output capacitance C_{oss} as well [31]. As f_{sw} increases, and the system size decreases, other, conventionally neglected loss terms become more important. The inductor ESR for an integrated component is much higher compared to its lumped counterpart, meaning that P_{ESR} from (3.17) becomes more of an issue.

3.4 Interleaved Buck Converter

An extension to the conventional Buck converter described in Section 3.3 is the Interleaved Buck Converter (IBC), presented in Figure 3.8. Essentially, the IBC topology uses two, or more, Buck-type voltage conversion stages in parallel where each branch is driven with the same control ON/OFF-scheme but with a phase difference, $\Delta\phi$ of

$$\Delta\phi = \frac{2\pi}{N} \tag{3.18}$$

where N is the number of interleaved Buck-type branches [32]. As seen in Figure 3.8 the branches share the same flywheel capacitance but make use of individual inductors meaning that adding additional branches, i.e. phases of operation, makes for additional passive components, more active devices, and more sophisticated control circuitry that can provide the N different phases. The gains of implementing this multi-phase Buck architecture, however, comes from a decreased average current through the inductor of each branch, $\propto N^{-1}$, and a decreased overall output current ripple from adding the out-of-phase current waves of each branch. More specifically, the normalized output current ripple (compared to the single phase Buck ripple) is calculated as

$$\frac{\Delta i_{\mathrm{p2p,\,IBC}}}{\Delta i_{\mathrm{p2p,\,BC}}} = \frac{N\left(D_{\mathrm{high,\,ON}} - \frac{\mathrm{floor}\{ND_{\mathrm{high,\,ON}}\}}{N}\right)\left(\frac{\mathrm{floor}\{ND_{\mathrm{high,\,ON}}\}+1}{N} - D_{\mathrm{high,\,ON}}\right)}{D_{\mathrm{high,\,ON}}(D_{\mathrm{high,\,ON}}-1)} \tag{3.19}$$

where the function floor $\{ND_{\mathrm{high,\,ON}}\}$ is the largest integer not exceeding the product $ND_{\mathrm{high,\,ON}}$ [32]. Using (3.19), the resulting normalized output current ripple is presented for different numbers of phases in Figure 3.9. As seen the reduction at a duty cycle of $D_{\mathrm{high,\,ON}} = 0.1$ is less than 40% for $N = 4$ while the ripple suppression is much larger for higher duty cycles (i.e. lower VSDR).

Any reduction of the current ripple through the flywheel inductor suggest a lowering of the required inductance to maintain CMO. However, in the case of the IBC the average current through each branch is reduced with a factor of two which increases the required inductance for CMO. Consequently, the IBC can use smaller inductance values for L_{f1} and L_{f2}, compared to the BC, only when $\Delta i_{\mathrm{norm}} \leq 0.5$.

Another benefit of the IBC topology is duty cycle doubling (compared to the single stage BC) which makes the ON-state pulses from the control circuitry to high side

transistor easier to realize at high VSDR (inherently small $D_{\text{high, ON}}$). Duty cycle doubling is brought by the fact that each flywheel branch in the IBC encompasses an average current of $i_{\text{out}}/2$, effectively working at an output voltage of $2V_{\text{out}}$ (which corresponds to $2D_{\text{high, ON}}$) at a maintained power level [33].

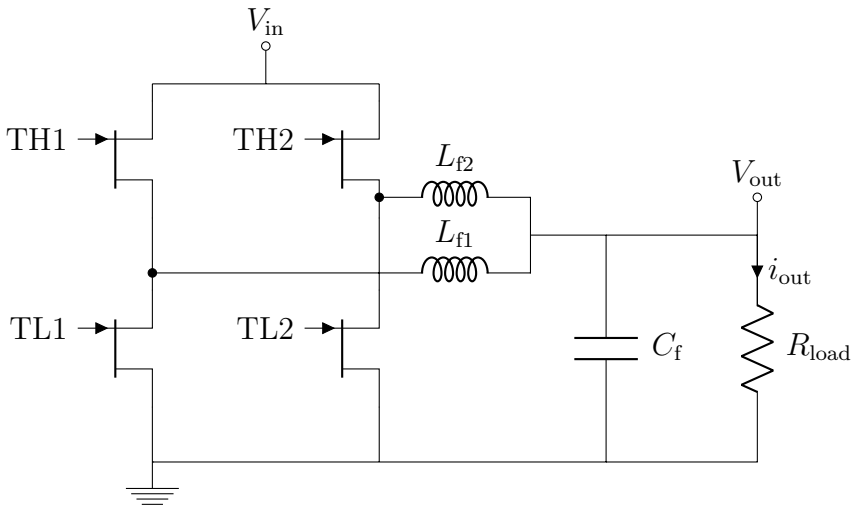


Figure 3.8: Principle design of an $N = 2$ IBC, the transistor pairs are driven 180° out of phase.

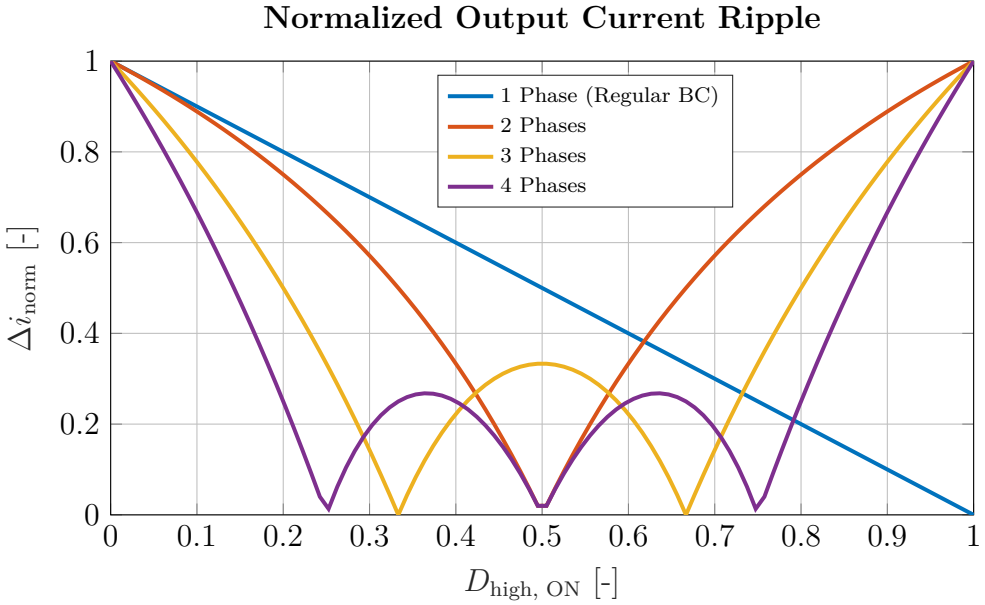


Figure 3.9: The normalized output ripple current from (3.19) as a function of the duty cycle for a conventional Buck converter and interleaved converters with 2, 3 or 4 phases.

3.5 Modified Interleaved Buck Converter

Another alteration of the Buck converter is the series capacitor Buck converter or Modified Interleaved Buck Converter (MIBC) which is presented in Figure 3.10. By inserting a series capacitor the voltage stress across the high side transistors TH1, TL1 and TL2 are effectively decreased with a factor of two, otherwise, the MIBC operates very similar to its two-phase IBC counterpart [33, 34]. As for the current ripple reduction, the MIBC shows the same dependence on duty cycle as the IBC from Figure 3.9 [33].
The MIBC also introduces an additional design parameter, namely the coupling capacitor C_t. Its size will influence how much voltage ripple that will be added on top of the $V_\mathrm{in}/2$ intermediate voltage. In [35], an expression for the intermediate voltage ripple is found as

$$\Delta V_\mathrm{intermediate} = \frac{D_\mathrm{high,\,ON} i_\mathrm{out}}{2 C_\mathrm{t} f_\mathrm{sw}}. \tag{3.20}$$

Lastly a limitation with the MIBC topology is that both high side transistors cannot be turned ON simultaneously, effectively limiting the maximum duty cycle to $D_\mathrm{high,\,ON} = 0.5$ and a maximum output voltage of $V_\mathrm{out} = V_\mathrm{in}/4$ [33, 34].

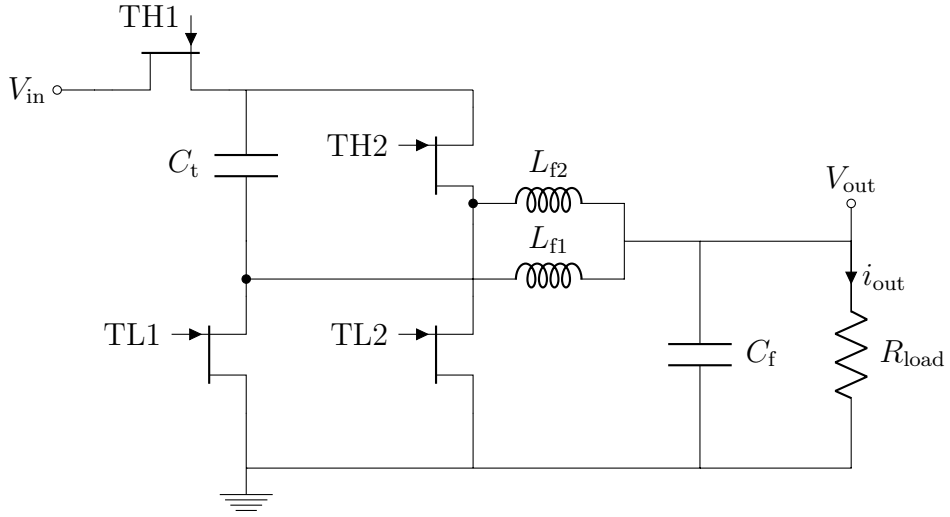


Figure 3.10: Schematic overview of the Modified Interleaved Buck Converter topology.

3.6 Switched Capacitor and Buck Converter Combination

In [19], a switched capacitor voltage converter is used in conjunction with a single phase conventional Buck converter to convert input voltages in the range of 25 to 200 V to 35 V at 30 W, with an efficiency of above 85%. This implementation is, however, not fully integrated and uses discrete 2× 422 nH inductors as L_{f} and 1 µF capacitors for power transfer in the SCC for instance [19].
The MIBC described in Section 3.5 makes implicit use of the very same mechanism that a switched capacitor converter cascaded with a Buck converter utilizes. Namely, to reduce the voltage strain on the high-side Buck switch with capacitors [19].

3.7 Switched Mode Converter Control Signals

Higher frequency voltage converters bring benefits such as increased power density, however, drawbacks as increased switching losses must also be considered. Zero Voltage Switching (ZVS), a so-called soft-switching technique, is employed to mitigate the switching loses as higher switching frequencies are pursued [36]. With ZVS the driver signal is set up in such a way that no transistor is switched between its ON and OFF state while there still is a voltage across the source and drain. Despite ideal control signals, with instant rise and fall behavior, the parasitic capacitance C_{oss} of each device will bring a lingering drain-source voltage that does not change as rapidly. Potentially extending the ON state of the high side transistor TH into the ON state of the low side transistor TL, allowing a current to flow directly from V_{in} to ground, degrading the efficiency [36].
In practice, for all Buck type converters, a sufficiently long dead time t_{dd} should be introduced between the toggling of transistors TH and TL to ensure that the intrinsic output capacitance, $C_{\text{oss-H}}$ and $C_{\text{oss-L}}$, of each device, has time to discharge [37]. This dead time should not be excessively long though, as it introduces other losses, meaning that the dead time should be chosen carefully and implemented with precision to guarantee efficient operation [37].
In this thesis, the dead time will be implemented by a widening factor w used as a scaling parameter for the pulse width for the low side transistor. By convention, the duty cycle, $D_{\text{high, ON}}$, for control square waves is an expression for the ratio of one pulse period spent in the high state. Now, the high side transistor control signal is defined as

$$V_{\text{high, control}} = \text{Square}\left(f_{\text{sw}}, D_{\text{high, ON}}, \frac{D}{f_{\text{sw}}}, t\right) \tag{3.21}$$

where the function $\text{Square}\,(f, D, \delta, t)$ defines a square wave with a period time of $1/f$, a duty cycle of D and a time delay of δ. Equivalently, for the low side transistor control, which should go into OFF-mode once the high side switch is ON, this control signal can be written as

$$V_{\text{low,control}} = \text{Square}\left(f_{\text{sw}}, 1 - D_{\text{high, ON}}, \frac{1}{f_{\text{sw}}}, t\right). \tag{3.22}$$

Now, to optimize the switching scheme the widening parameter w is included as a parameter in the control voltage for the low side transistor as

$$V_{\text{low, control}} = \text{Square}\left(f_{\text{sw}}, w(1 - D_{\text{high, ON}}), \frac{1}{f_{\text{sw}}}, t\right) \tag{3.23}$$

effectively introducing a dead time t_{dd} before and after TH is turned ON. The corresponding control signals are exemplified in Figure 3.11 with $D_{\text{high, ON}} = 0.88$, $f_{\text{sw}} = 77\,\text{MHz}$ for $w = 1.0$ and $w = 0.9$ respectively. More details of the Square-function are presented in Appendix B.

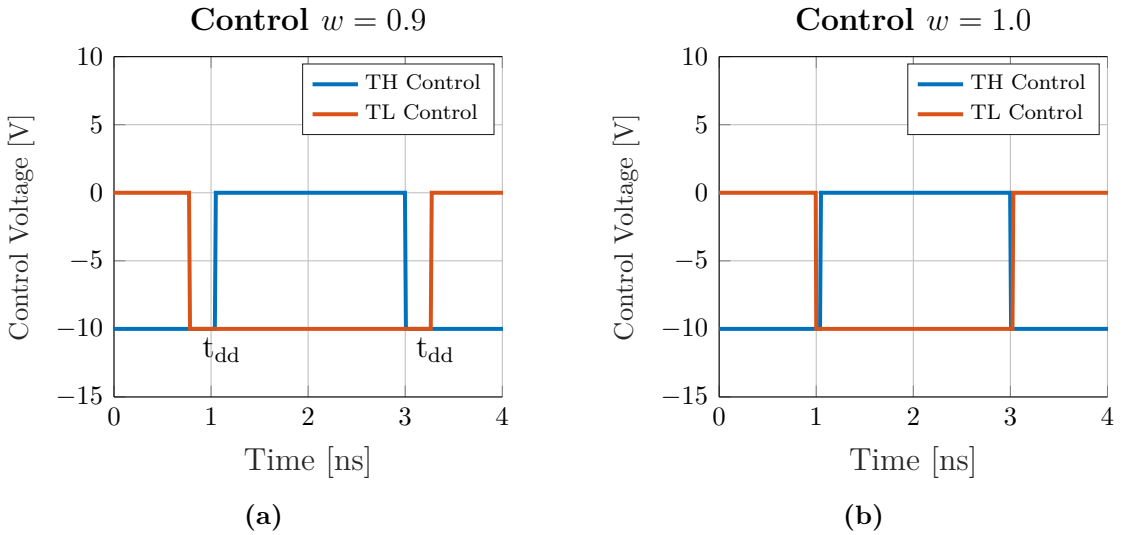


Figure 3.11: The control signals for the high and low side transistor in a BC with widening parameter $w = 0.9$ makes the OFF state for the low side switch longer, introducing a dead time t_{dd} when both TH and TL are OFF (a). With no dead time, $w = 0$, there is a risk for conduction through both devices (b).

3.8 Integration Challenges for DC-to-DC Converters

In Table 3.2 a selection of Buck-type voltage converters in CMOS and GaN are presented. Indeed, both technologies offer converters that utilize switching frequencies venturing into 100s of MHz but it is exclusively with GaN that high f_{sw} is combined with higher voltages. In [5] an extra-large inductor is used to tolerate low load currents while remaining in CMO and in [38] the small inductor suggests full integration is possible despite the choice to use a discrete counterpart. Besides not challenging an input voltage of a few 100s of volts GaN implementations have clearly already been used at higher than convention voltages and frequencies, paving the way for full integration.
Ideally, to increase the level of integration in any of the presented switched mode voltage converter topologies, the switching frequency is increased until a satisfactory small value of the required passive components is reached, again [38] is an example. Most critical is the size reduction of the flywheel inductors in the Buck-type converters. Traditionally, these converters use switching frequencies on the order of 10 kHz up to a few 100 kHz [39] and consequently large discrete inductors ranging from 1 to 100 µH have been required. These inductances are out of reach for monolithic integration [40]. The necessity of large, non-integrated inductors can be circumvented using higher frequencies. However, even though the critical requirements for passive components for a given VSDR and input voltage decreases as $\propto 1/f_{sw}$ the physical size of the passive components will in general not decrease as rapidly [39]. Design considerations and unavoidable parasitics from interconnections and semiconductor devices inhibit the reduction in physical size with frequency from being as rapid as $\propto 1/f_{sw}$ [39].
Moreover, as f_{sw} increases the more sophisticated, high precision, control schemes are necessary to minimize the different types of switching losses that increase $\propto f_{sw}$. This, together with the unavoidable gate charge loss from (3.16), means that increasing the switching frequency might not show a severe increase in losses in the power stage, thanks to ZVS or equivalent, but instead the most important losses will originate from the driver circuitry. As evidence of this, in [18] a system-wide efficiency, including both the power stage and the control circuitry, of 64.1% is reported at 200 MHz. This was achieved at an input voltage of 30 V, a VSDR of 2 and with an off-chip 470 nH flywheel inductor. However, the power stage efficiency is $\approx 90\%$, meaning that for this implementation, at 200 MHz the losses associated with the control circuit dominate those of the power stage. In [37] the large power dissipation and heat generated by the integrated driver circuit is reported as one of the main challenges in realizing a GaN Buck converter operating at above 10 MHz.

Table 3.2: Comparison between Buck-type voltage converters in CMOS and GaN technology.

Work	[18]	[36]	[6]	[3]	[5]	[38]
Technology	GaN	GaN	CMOS	CMOS	GaN	GaN
Frequency	500 kHz	3 MHz	100 MHz	170 MHz	200 MHz	400 MHz
$\mathbf{V}_{\text{in}}$	48 V	28 V	1.2 V	1.2 V	30 V	20 V
$\mathbf{V}_{\text{out}}$	1.2 V	3.3 V	0.9 V	0.9 V	15 V	10 V
$\mathbf{i}_{\text{OUT}}$	4.5 A	6 A	180 mA	150 mA	33 mA	0.5 A
Inductor	1 µH[3]	33 nH	8 nH[2]	2 nH[1]	470 nH[3]	12.5 nH[3]
Efficiency	78%	93%	84%	75%	60%[4]	72.5%

[1] Fully integrated
[2] Package integrated
[3] Discrete
[4] For driver and power stage combined

4

Voltage Converter Simulations

With ADS simulations the DC-to-DC converter topologies put forth in the previous Chapter will be further analyzed and verified. As an approximation the Angelov transistor model [41] was used with a minimum set of parameters to model the current and voltage behaviour of symmetric GaN HEMTs.

4.1 Ideal Buck Converter Simulations

In order verify that the simulation setup, and the utilized transistor model, successfully captures the operation of the BC ~~an~~ as ideal as possible converter is constructed in the software. Using ideal passive components (ESR = 0, $C_f = 5\,\text{nF}$ and $L_f = 300\,\text{nH}$), transistor models with minimal output capacitance, $C_{oss} = C_{ds} = 1\,\text{fF}$, and ideal square wave control signals a highly efficient BC can be simulated. In Figure 4.1 the output voltage and current of the converter operating at $f_{sw} = 50\,\text{MHz}$, $V_{in} = 270\,\text{V}$, $D_{\text{high, ON}} = 0.1$ and $P_{out} = 26.3\,\text{W}$ is shown as a function of time after turn-on. In steady state, at 10 µs, the voltage ripple is approximately 1 V peak-to-peak and the current ripple is approximately 35 mA peak-to-peak. As Figure 3.7 suggests a Buck Converter (BC) operating at this frequency with these component values should be on the verge of reaching discontinuous operation. The flywheel inductor current i_L at steady state $t+10$ µs, presented in Figure 4.2, verifies this as the current comes close to 0 during discharge. Resembling closely the expected triangle wave appearance as suggested by theory [23]. In this configuration, simulations show a simulated efficiency of $\eta = 96\%$.

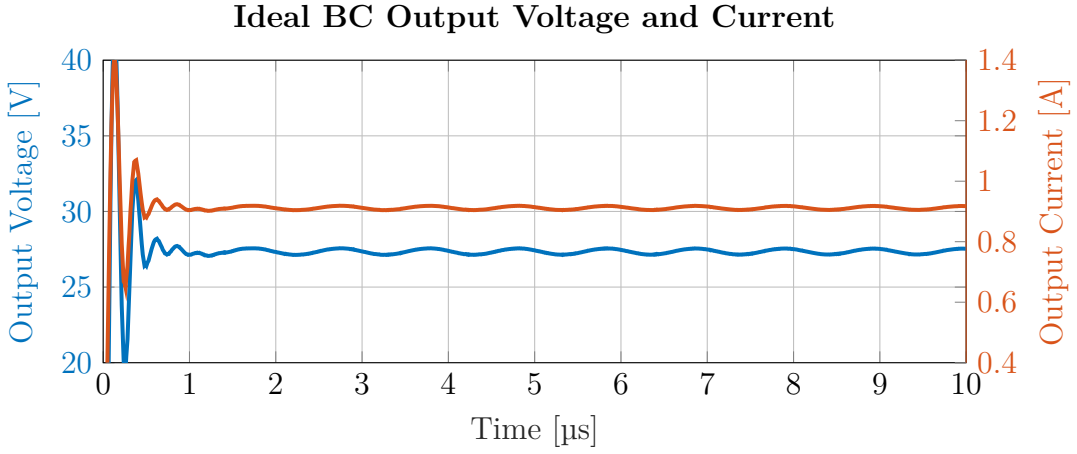


Figure 4.1: The simulated output voltage and current of an ideal 50 MHz BC.

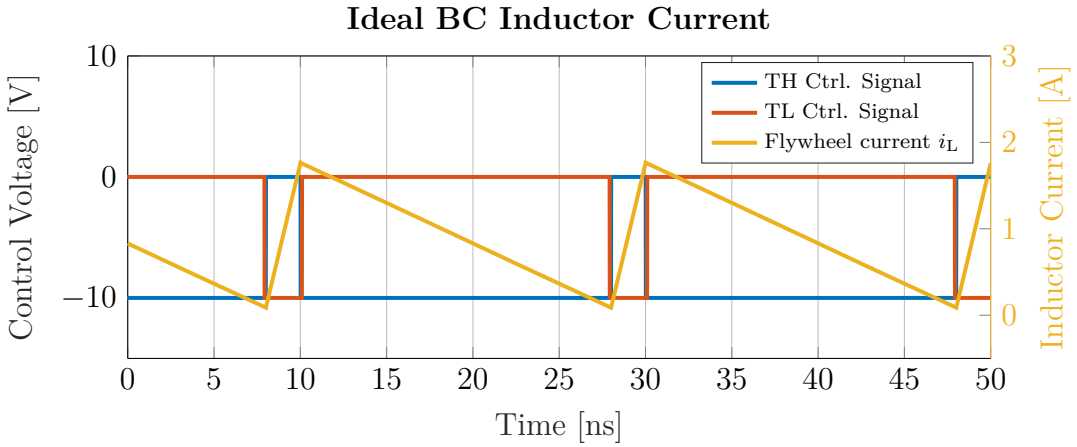


Figure 4.2: The simulated inductor flywheel current and control signals for the ideal BC at steady state ($t + 10$ µs).

4.1.1 Transistor Model Parameters for BC

The results from the ideal BC simulations show that the particular ADS setup is successful in capturing the behavior of the converter. More important, however, it is describing how nonidealities will impede on the performance of the ideal circuit. The Angelov model, used to simulate the transistor behavior, includes many parameters that are not essential for simulating the transistor operation in a low-frequency regime (compared to RF). However, the current at maximum transconductance IPK0 and the source-drain capacitance C_{ds} (i.e. the output capacitance C_{oss}) will affect the converter efficiency to a large extent.
In the Angelov model, IPK0 is approximately half the saturation current through the transistor. Effectively, IPK0 will cap the current through any of the transistors to 2IPK0 and thus choosing a too low value will effectively act as a very high R_{ON} value for part of the ON-period in each transistor. In Figure 4.3 the ideal BC efficiency is simulated for a range of different IPK0 values. As seen, efficiency decreases rapidly as IPK0 approaches 1 A, implying a saturation current of 2 A, the expected maximum current through the transistors as explained in equation (3.9). From Figure 4.2 (where IPK0 = 2.7) it is verified that the unhindered inductor current indeed reaches almost 2 A. These loss effects appearing for currents larger than 2IPK0 originate from the sophisticated transistor model and are unwanted in the ideal simulations, as a perfect transistor (with $R_{\text{ON}} = 0$) is not expected to dissipate any power in current saturation. To circumvent this, a large enough IPK0 = 2.7 is used in all simulations to keep the transistors in the linear region. In practice, this implies that the transistors utilized are large enough to not enter saturation.
The output capacitance C_{oss} will in part delay the shift in drain-source voltage across the high side transistor when it is switched by the control signal and in part limit the rise and fall time of V_{ds}. With ideal, instantly fast, control signal toggling and negligible output capacitance for the transistors V_{ds} jumps from V_{in} to 0 very rapidly. Introducing a non-negligible C_{oss} will result in a finite rise and fall time of V_{ds} as well as delay, as illustrated in Figure 4.4. A large enough output capacitance will limit

the maximum switching frequency, and minimum ON-state duty cycle, since V_{ds} will not have time to switch between 0 to V_{in} within a time of $D_{\text{high, ON}}T_{\text{sw}}$. Allowing simultaneous conduction of both transistors and efficiency degradation.

In Figure 4.4 the drain-source voltage for the very small output capacitance of 0.2 pF coincides perfectly with the ON-signal to the high side transistor and the OFF-signal to the low side transistor. Thus, it is noted that higher output capacitance and more sluggish V_{ds} toggling can be compensated to some degree by increasing the OFF-state period time of the low side transistor using w and introducing a delay. Figure 4.5 shows the efficiency with and without control optimization for different output capacitances. As seen the theoretical efficiency, as suggested by (3.15) can be approached with control signal optimization and introduction of dead time.

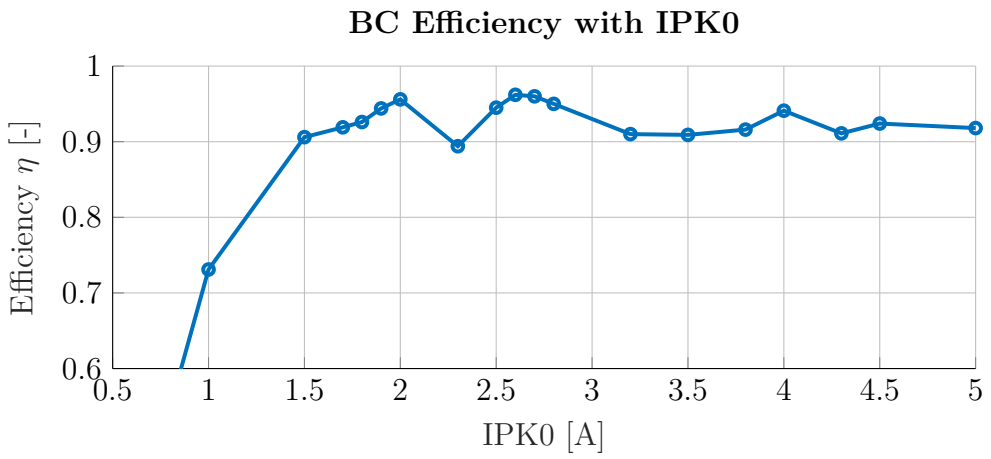


Figure 4.3: Efficiency of the BC with different IPK0 for the Angelov transistor model.

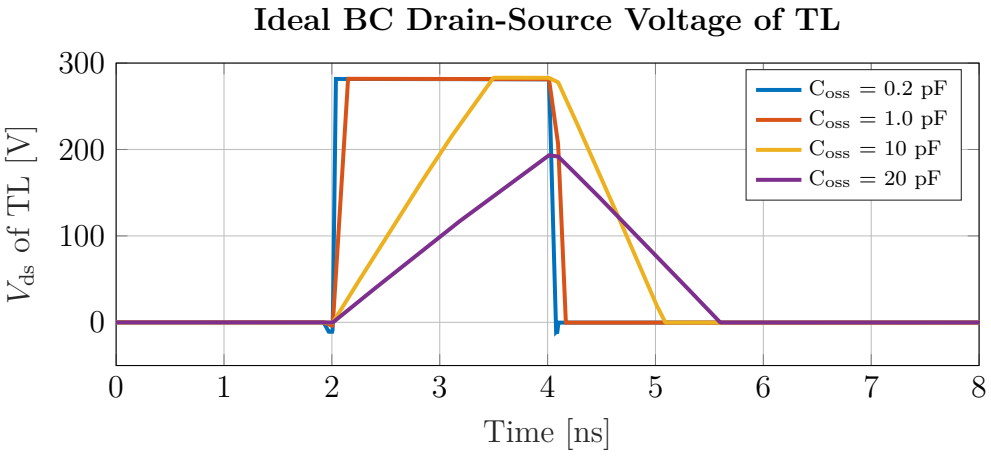


Figure 4.4: Drain-source voltage across the high side transistor for different values of the output capacitance at steady state ($t + 10$ µs).

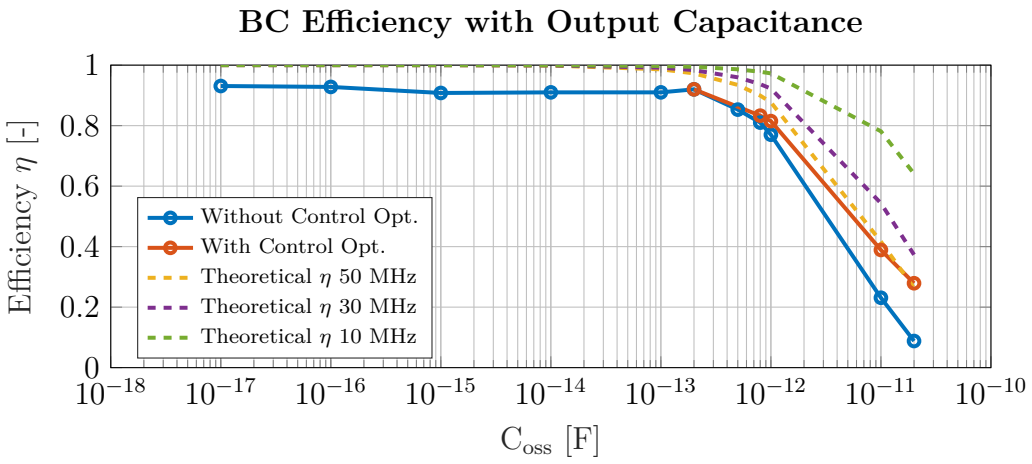


Figure 4.5: The efficiency of the simulated Buck Converter operating at 50 MHz for different output capacitance values, together with the efficiency η as suggested by the design equations for a selection of switching frequencies.

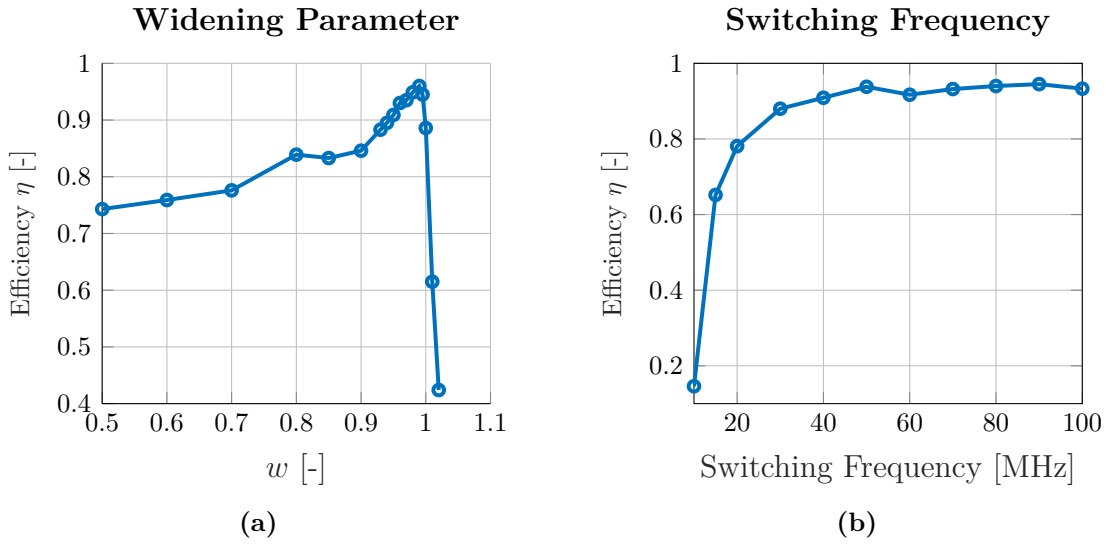


Figure 4.6: BC efficiency for different w of the control signal to TL (a) and the simulated efficiency of the ideal Buck Converter operating at different switching frequencies (b).

4.1.2 Control Signal Considerations for BC

Utilizing control signals with proper dead time is crucial for maintaining high efficiency. In the case of the ideal BC with close to instantaneous rise and fall time of the control signals a slight widening of the low side OFF-pulse is still necessary to avoid simultaneous conduction through both devices. In Figure 4.6a, the efficiency of the converter is shown for different w, as expected efficiency falls quickly once the limit for ZVS (i.e. a widening factor of 1.00) is passed. Too much widening of the OFF state for the low side transistor (i.e. small w) introduces additional dead time losses.

With the ideal 50 MHz BC setup ($L_f = 300\,\text{nH}$ and $C_f = 5\,\text{nF}$ with an ESR of 0) the effects of changing the switching frequency is shown in Figure 4.6b. With ideal transistors and passives there is no performance degradation from increasing the frequency, since C_{oss} from (3.15) is small enough and the driver is assumed ideal. However, as frequency is decreasing efficiency in the simulation starts to degrade. After passing the threshold of FCMO at approximately 35 MHz the peak-to-peak inductor current ripple increases, and the losses here originate from the limited IPK0-value of the Angelov model which limits the maximum current.

4.1.3 Passive Components ESR for BC

The maximum efficiency is limited by the resistive losses present in the circuit. Hence, for a more realistic estimation of the overall efficiency, the impact of the ESR in the passive components is studied. Introducing non-zero ESR for the passive components, the flywheel inductor L_f and the flywheel capacitor C_f, degrades the converter efficiency. The ESR of L_f will at the same time introduce a voltage drop not accounted for in the $V_{out} = D_{\text{high, ON}} V_{in}$ relationship, effectively lowering the output voltage at a given duty cycle. To provide a fair comparison the duty cycle is altered to compensate the voltage decrease. In Figure 4.7 the output voltage is in each point approximately 28 V but the ON-state duty cycle must be increased together with the ESR to achieve this. Increasing the ESR of C_f, on the other hand, will not change the average i_{out} or V_{out}, however, as the quality factor of the capacitance decreases the output voltage ripple increases, passing 3 V peak-to-peak at an ESR of 2 Ω and saturating at a peak-to-peak ripple of $V_{out} = 28\,\text{V}$ at an ESR of approximately 15 Ω. As seen in Figure 4.7 the theoretical efficiency degradation, calculated using (3.17), is mimicked closely.

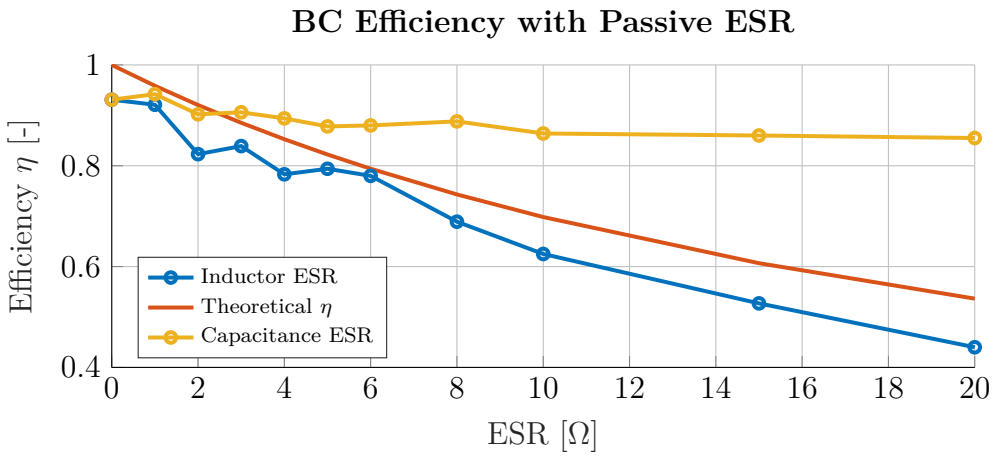


Figure 4.7: The efficiency of the BC with increasing ESR for the flywheel inductor and capacitor. The duty cycle $D_{\text{high, ON}}$ has been increased to provide 28 V at the output for increasing L_f ESR.

4.2 Modified Interleaved Buck Converter Simulations

The MIBC topology introduces additional transistors and necessitates two sets of control signals with a phase difference of 180°. Again, to demonstrate workings of the topology and verify the simulations an ideal MIBC analyzed first. Extending upon the ideal BC from Section 4.1 with $L_\mathrm{f} = 300\,\mathrm{nH}$, $C_\mathrm{f} = 5\,\mathrm{nF}$, $f_\mathrm{sw} = 50\,\mathrm{MHz}$ and creating an MIBC version, with two phases, a coupling capacitor $C_\mathrm{t} = 5\,\mathrm{nF}$ and a duty cycle of $D_{\mathrm{high,\,ON}} = 0.2$ the resulting flywheel inductor current of each branch in the converter is presented in Figure 4.8. As seen, the current ripple reduction from (3.19) is not enough to compensate the lowering of the average current level in each branch to keep the converter operating in CMO. Using 500 nH inductors instead, the inductor flywheel current, output voltage and output current from Figure 4.9 and 4.10 is obtained, showing positive flywheel currents, continuous mode operation and the correct output voltage and current.

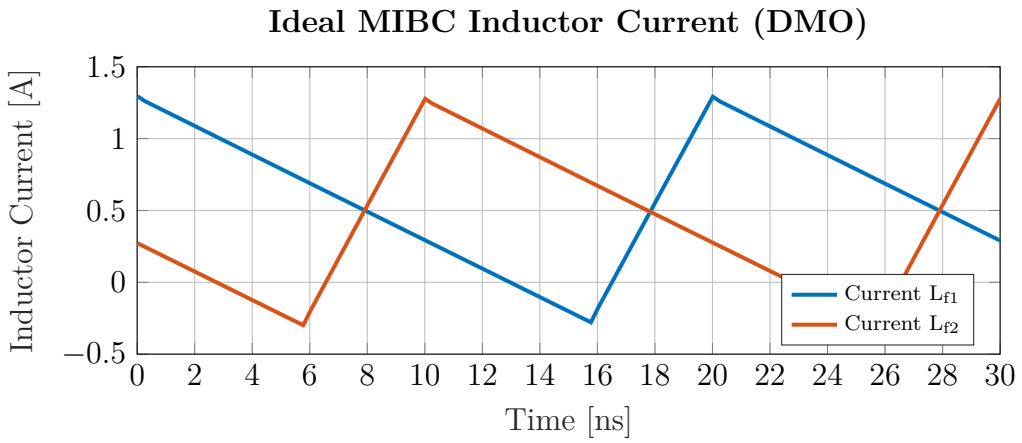


Figure 4.8: Flywheel inductor current through each branch of the MIBC for $L_{\mathrm{f1}} = L_{\mathrm{f2}} = 300\,\mathrm{nH}$ at steady state ($t + 10\,\mu\mathrm{s}$). The converter is in FCMO.

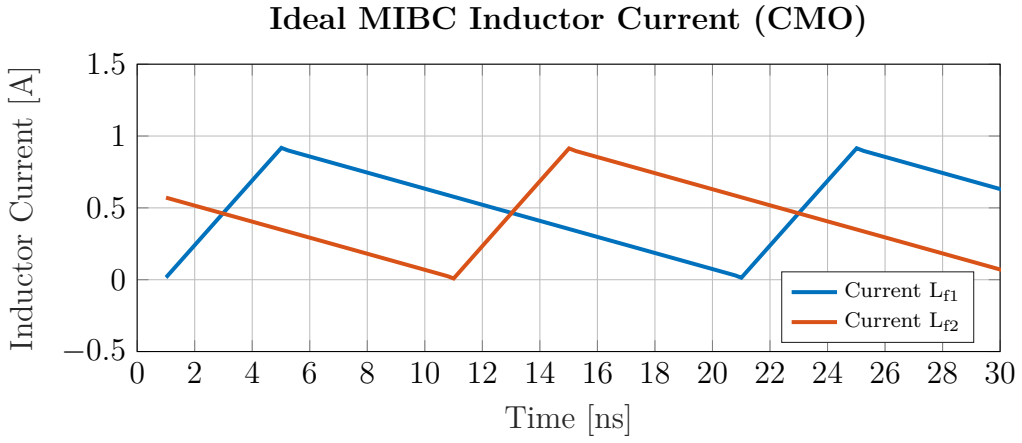


Figure 4.9: Flywheel inductor current through each branch of the MIBC for $L_{\mathrm{f1}} = L_{\mathrm{f2}} = 500\,\mathrm{nH}$ at steady state ($t + 10\,\mu\mathrm{s}$). The converter is in CMO.

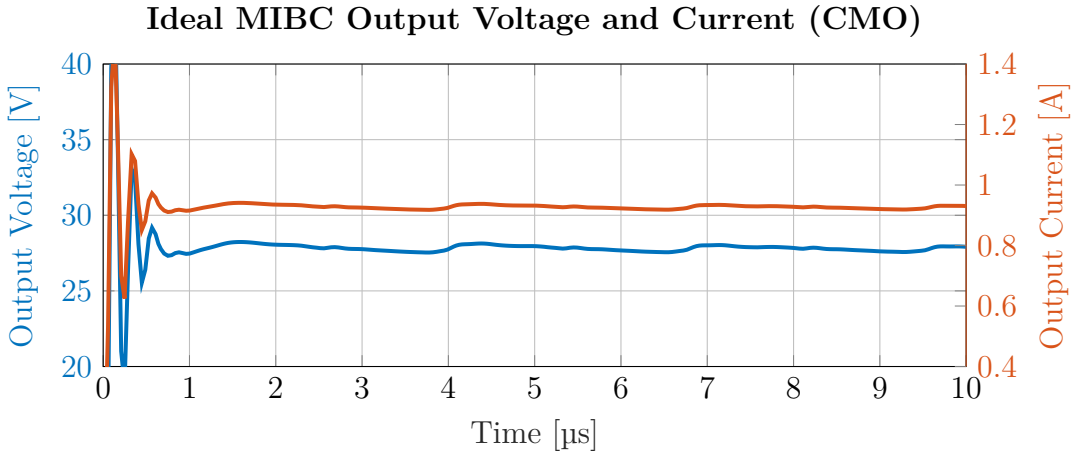


Figure 4.10: The output voltage and current as the MIBC reaches steady state.

4.2.1 Transistor Model Parameters for MIBC

The simulated efficiency for the MIBC operating at $f_{sw} = 50$ MHz with different output capacitance values C_{oss} for the transistor model is plotted in Figure 4.11, together with the corresponding curve for the BC from Figure 4.5. For almost all capacitances the MIBC preforms better than the BC and comes closer to the theoretical efficiency for the BC from 3.15 even without control signal optimization. This is explained in part by the lower switching voltage of the high side transistor TH1 and in part by duty cycle doubling. The MIBC operates at $D_{\text{high, ON}} = 0.2$ (compared to $D_{\text{high, ON}} = 0.1$ for the BC) and is consequently less sensitive to the V_{ds} pulse widening brought by C_{oss}, shown in Figure 4.4, when compared to the BC. Once the rapid efficiency decline starts at around $C_{oss} = 1\,\text{pF}$ the switching losses are the dominant loss factor and, when comparing the BC and the MIBC, the MIBC tolerates almost exactly twice output capacitance of the BC at the same efficiency.

Moreover, since the maximum voltage stress across TH1, TL1, and TL2 is half that of TH2 it is interesting to investigate scenarios where the low voltage transistors all have the same output capacitance C_{oss} while TH2 has different values. This should mimic the scenario where a transistor with higher voltage tolerances (and thus tending towards higher C_{oss}) is used as TH2 and smaller transistors with lower maximum voltage ratings are used as TH1, TL1, and TL2 respectively. In Figure 4.12 the efficiency of the MIBC for different values of C_{oss} of TH2 is plotted for the scenarios when the C_{oss} of the remaining transistors is either 0.1 pF or 1.0 pF. As seen, using different devices in the high and low voltage positions should improve efficiency in all scenarios.

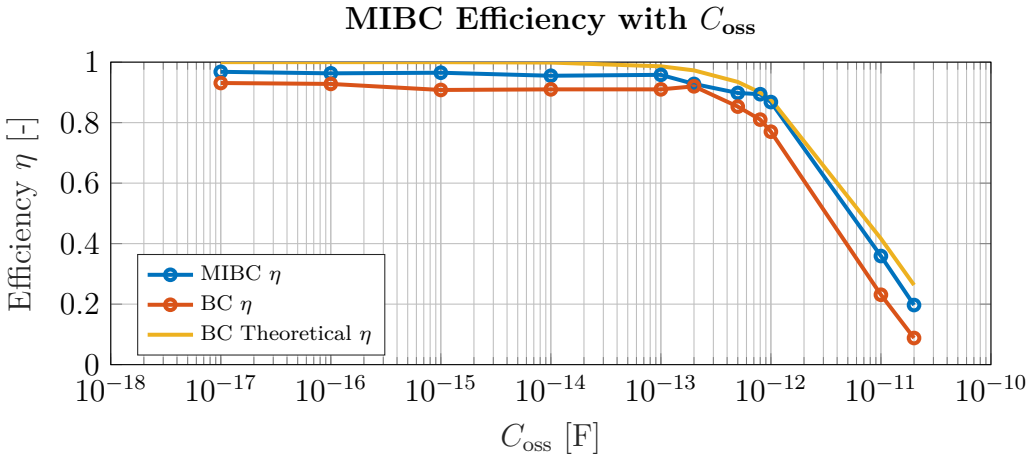


Figure 4.11: Simulated efficiency η for the MIBC at 50 MHz with increasing output capacitance C_{oss}, compared to the BC and the theoretical curve.

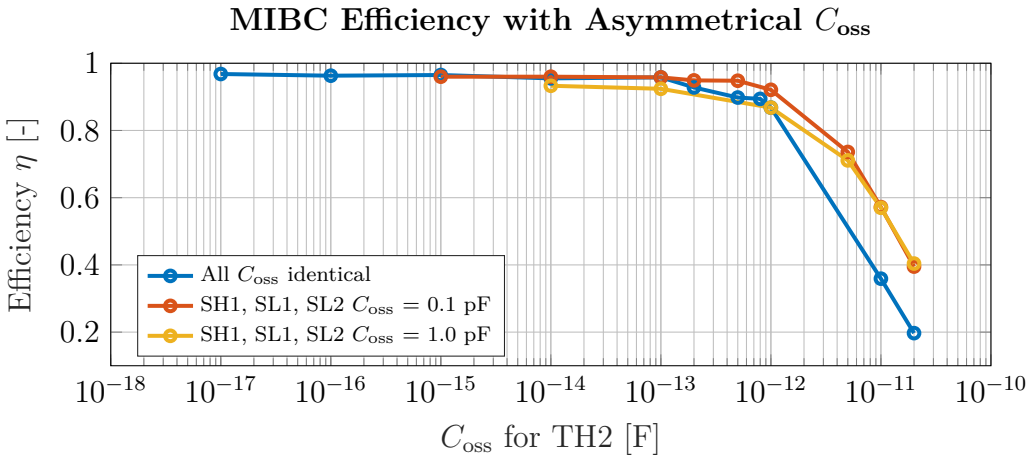


Figure 4.12: The efficiency of the MIBC once C_{oss} is both the same and not the same for the low voltage transistors (TH1, TL1, and TL2) and the high voltage transistors (TH2).

4.2.2 Control Signal Considerations for MIBC

The MIBC shows a similar dependence on w as the BC as seen in Figure 4.13. For the same reasons, to avoid simultaneous conduction through all devices, a widening factor of $w < 1.00$ is necessary for negligible (1 fF C_{oss}). Smaller values of w will be required to compensate for the V_{ds} sluggishness if C_{oss} is increased, to maintain efficiency.

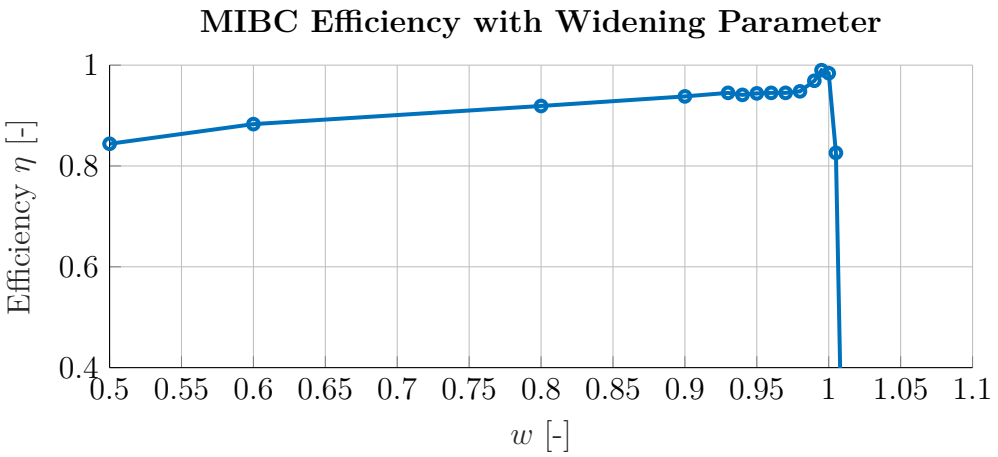


Figure 4.13: The impact on efficiency of making the OFF-state of the low side transistors shorter ($w > 1.00$) or longer ($w < 1.00$).

4.2.3 Passive Component ESR for MIBC

It is important to highlight how the obtainable efficiency decreases with resistive losses in the MIBC, and compare these to the corresponding losses in the BC topology. Introducing ESR to the flywheel capacitor C_t in the MIBC shows results very similar to the BC. In Figure 4.14 the efficiency for different ESR levels for the flywheel inductors and capacitor is shown. Since the power loss in each inductor is $\propto i_{out}^2$ and each branch carries half the current of a single branch regular BC the efficiency degradation with ESR is not as severe. However, as stated in Section 4.2 larger inductors are needed to keep the converter in CMO which would bring inherently higher inductor ESR levels for the MIBC.

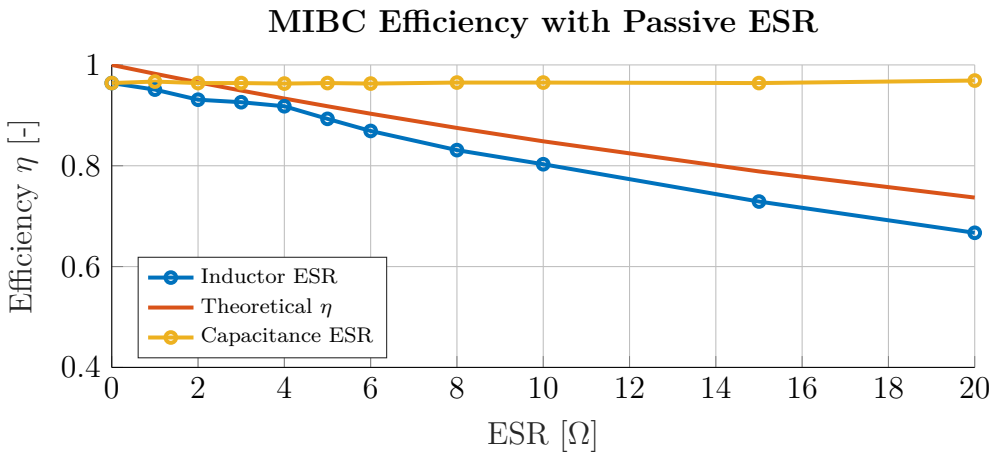


Figure 4.14: Efficiency degradation of the MIBC as the ESR of the flywheel inductors and capacitor is increased. To compensate a decreasing V_{out} the duty cycle is tuned to always provide ≈ 28 V delivered at the output of the converter.

4.3 Switched Capacitor Converter Simulations

The switched capacitor converter in Section 3.2 is here considered operating as a VSDR = 2 stage, preceding a BC with VSDR = 5. Targeting switching frequencies a factor of 100 below those of the BC topologies, which operate at 10s of MHz, a switched capacitor converter with operating at 400 kHz is simulated and the output voltage and current from Figure 4.15 are acquired at an output power of approximately 25 W. It is also verified that the output voltage indeed is half the input voltage, i.e. approximately 135 V. This result was acquired with comparatively large (in regards of the switching frequency and output current) capacitors $C_1 = C_2 = 15\,\text{nF}$ and $C_o = 20\,\text{nF}$. Interestingly, the theoretical capacitance value from equation (3.4) and Figure 3.3, with $C_1 = C_2 = 3\,\text{nF}$, provides comparatively poor efficiency. In Figure 4.16 the efficiency, and output voltage, is plotted as a function of $C_1 = C_2$ for an SCC operating at 200 kHz and 400 kHz respectively. As seen, the capacitance from the theoretical relationship (3.4) denoted as C_{min}, does not guarantee close to unity efficiency for each frequency. C_{min} is rather the capacitance at which the efficiency increase stagnates. Due to the limited maximum current through the transistors and various charging effects, larger capacitors are beneficial when operating close to current balance limit proposed in equation (3.4). The intrinsic capacitance properties of the transistors are not considered in (3.4) which serves as an additional explanation as to why close to unity efficiency is not reached with only $C_1 = C_2 = C_{\text{min}}$.

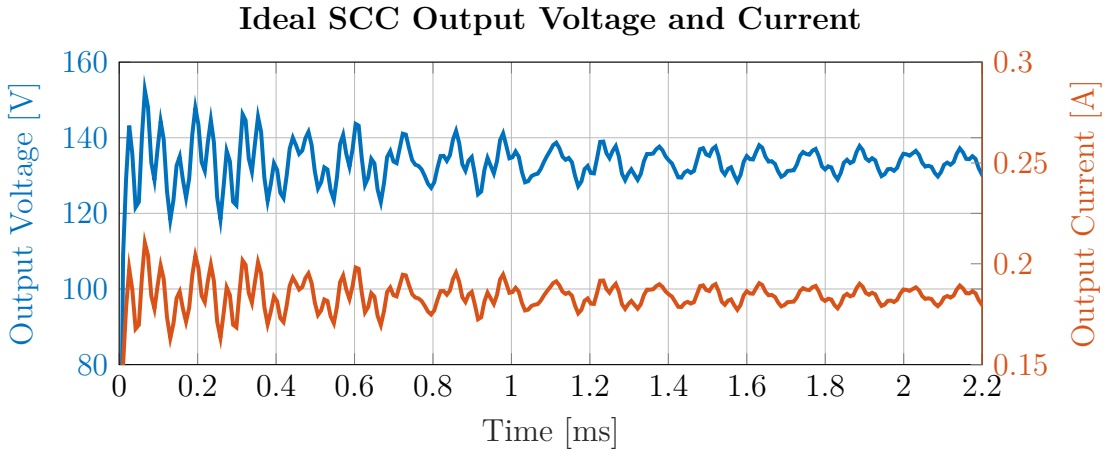


Figure 4.15: The output voltage and current as the SCC reaches steady state at $f_{\text{sw}} = 400\,\text{kHz}$ with $C_1 = C_2 = 15\,\text{nF}$ and $C_o = 20\,\text{nF}$.

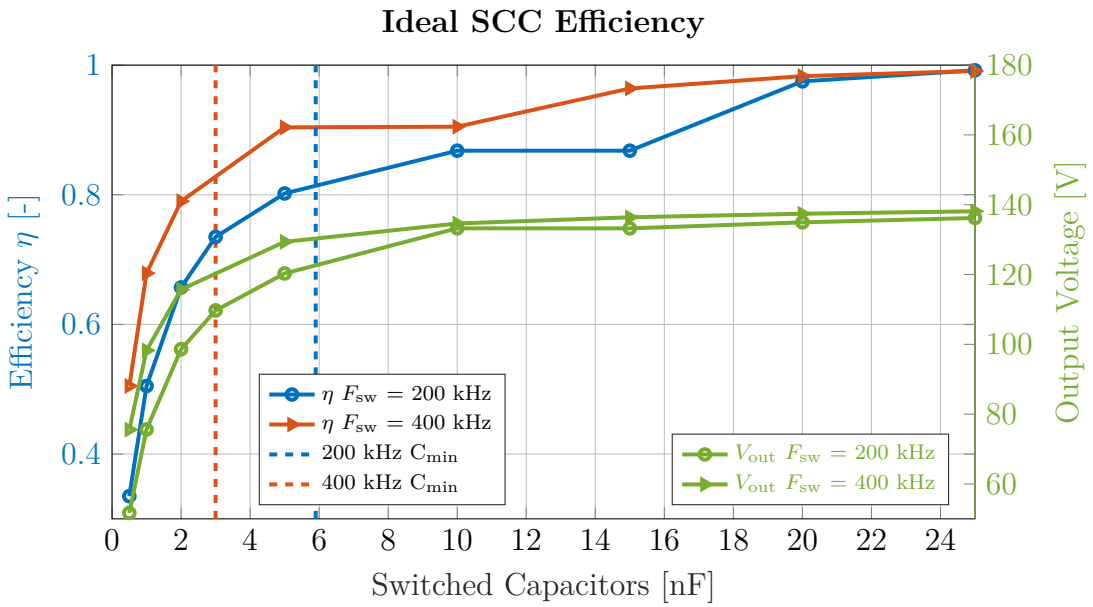


Figure 4.16: The efficiency and output voltage of an ideal SCC at 200 kHz and 400 kHz. Also indicated are the theoretical minimum capacitance values needed for 25 W output power from Figure 3.3.

4.3.1 Transistor Model Parameters for SCC

If the transistors in the SCC feature a parasitic output capacitance C_{oss} the switching losses will degrade efficiency. In Figure 4.17 the efficiency for a 400 kHz SCC is shown for C_{oss} values between 1 fF and 500 pF. Compared to the different Buck-type converters topologies the switching losses for the SCC start to dominate at approximately 10 times higher capacitance values. Which is explained by the roughly 10 times lower switching frequency and the linear relationship between switching losses, C_{oss} and f_{sw} from (3.15). Intuitively, lower switching frequencies makes for less issues with parasitic output capacitance.

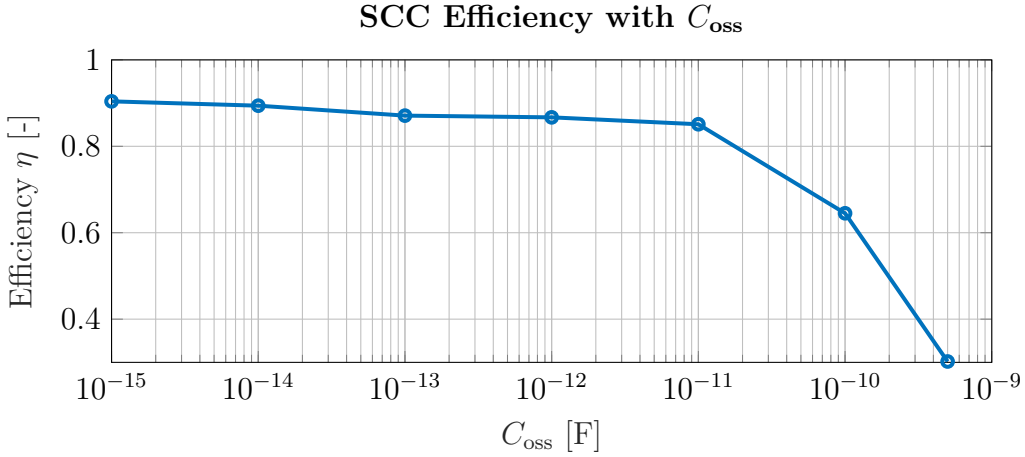


Figure 4.17: Efficiency decrease as C_{oss} increases for the SCC topology operating at 400 kHz with $C_1 = C_2 = 5$ nF.

5
Passive Components

The parasitic capacitance of active devices and the details of the control signals are evidently crucial for obtaining high-efficiency DC-to-DC converters. Also, as seen in Figure 5.3 and 4.14 the ESR of the passive components, primarily the inductors, will impair the efficiency. As the ESR of integrated passives is in general much higher compared to their discrete counterparts new inductors will be designed in an attempt to side-step an important bottleneck of integrated power systems.

5.1 Integrated Inductors

For any Buck-type DC-to-DC converter the flywheel inductor is a critical design aspect. As described in (3.10) the output ripple current is inversely proportional to L_f, meaning that a sufficiently large inductor is necessary to guarantee CMO and in keeping the maximum current through any of the devices low.
This poses an important issue for fully integrated voltage converters as the performance of integrated inductors is poor compared to their lumped counterparts. In Table 5.1 some of the largest, fully integrated, inductors described in literature are compared to commercial off-the-shelf discrete inductors, the magnetic SPM5030T-R20M by TDK [42] and the air-core 2222SQ-221E by Coilcraft [43]. It is clear that the obtainable L/ESR ratios for integrated inductors is much worse compared to the commercial discrete alternatives. Advanced processes that can incorporate magnetic materials, such as in [44], can boost the performance of integrated inductors (mainly the inductance per unit volume) but no MMIC process can fully bridge the gap between lumped and integrated inductors.

Table 5.1: Comparison between commercial off-the-shelf lumped inductors and a few integrated counterparts at 10 MHz.

Inductor	R20M	SQ-221E	[10]	[10]	[45]	[44]
Integrated	No	No	Yes	Yes	Yes	Yes
Magnetic	Yes	No	No	No	No	Yes
Ind. [nH]	200	220	205	103	159	270
ESR [Ω]	0.4	0.17	0.85	1.03	0.40	1.22
Area [mm²]	26	55	4	4	2	3
Thickness [µm]	3000[A]	5700[A]	100	30	150	45
Ratio [nH/Ω]	500	1340	241	100	398	221

[A] Total component package height

5.2 Inductors in Chalmers GaN-on-SiC Process

In the GaN process under development at Chalmers the GaN-layer is grown on top of a 500 µm SiC substrate layer (dielectric constant of 9.66) and an underlying ground metal plate. The SiC is then processed and thinned down to feature a smooth 100 µm layer. These steps produce the two bottom-most layers of each technology presented in Figure 5.1. As of recently the inclusion of two separate isolation layers of BCB (dielectric constant of 2.65) and associated gold conductor layers, `M2` and `M3`, is under development. This provides extra design freedom for passive components and could decrease the total chip area required for any design, as the geometries of the passive components can be stacked.
To investigate in what respect the multi-layer BCB back-end should be utilized, and expanded, to better suit the needs of a power SoC three technology sets with associated inductors will be analyzed further. The details of the integrated inductors in each technology are presented graphically, in Figure 5.1, and more in detail in Table 5.2. The first technology, Standard MMIC (S), is limited to one layer BCB and features the single layer S-inductors with 3.5 µm conductor thickness (`M2`) and a thin 0.4 µm under-path connecting the center of the spiral to the outside (`M1`). The S-inductors have been manufactured and can be both simulated and measured experimentally.
The Multi-layer (M) inductors are realized in an enhanced BCB process with multiple layers, allowing for stacked spiral inductors in `M2` and `M3` with a separating BCB-layer between. An example M-inductor is presented in Figure 5.2a. Lastly, Thick (T) inductors with very thick conductors, inspired by the integrated transformer designs from [10, 45] are also analyzed with thick conductors in `M2` but with no `M3`. An example design of a T-inductor is presented in Figure 5.2b. Instead of utilizing two coupled layers with thinner conductors, the enhanced thick technology will allow a reduction of the ESR rather than increased inductance per unit area. In all three technologies the bottom-most BCB layer, which separates the spiral from the SiC, will be referenced to as the buffer.

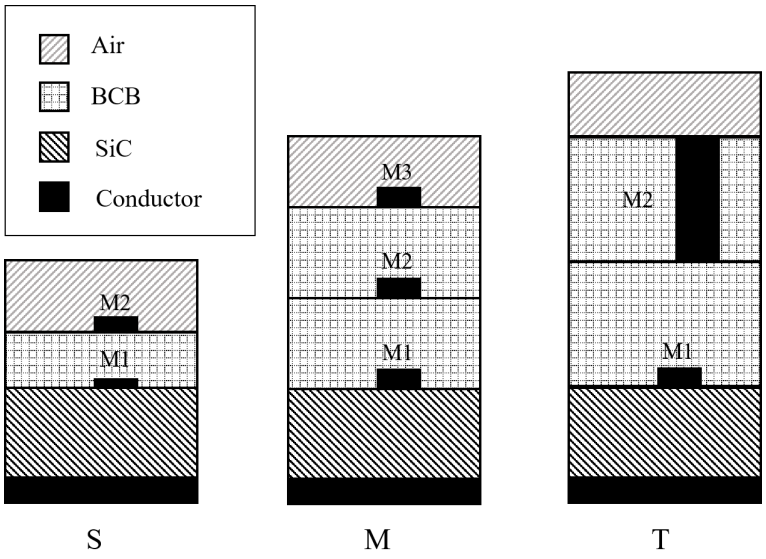
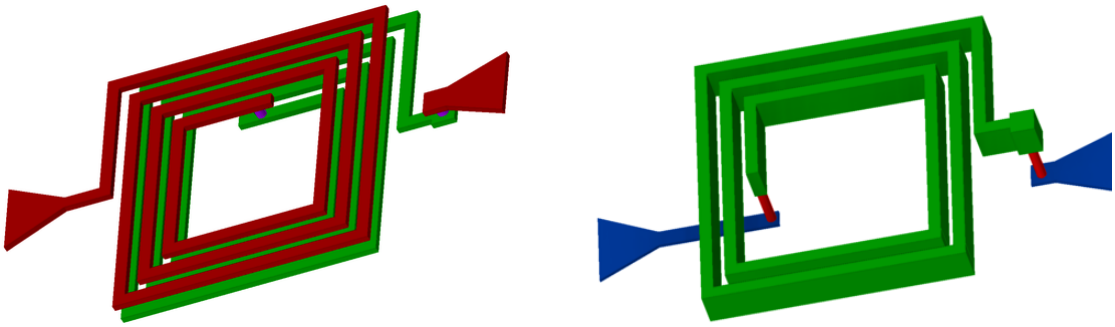


Figure 5.1: Overview of the S-, M-, and T-type technology realized with the Chalmers In-House GaN technology and the BCB back-end under development (not to scale).



(a) **(b)**

Figure 5.2: An example multi-layer inductor with ports in `M3` (brown) and vias connecting to `M2` (a). A thick inductor with ports in `M1` (blue) and spiral windings in `M2` (b).

Table 5.2: Comparison between the parameters of the S-, M-, and T-type inductors.

Technology	**Standard MMIC**	**Multi-layer**	**Thick**
Inductor layers	`M2`	`M2` and `M3`	`M2`
Separation BCB	N/A	10 µm	N/A
Buffer BCB	≤5 µm	10 µm	30 µm
N. of turns	3 to 6	≥ 6	≥ 6
Conductor thickness	3.5 µm[A]	5 µm	30 µm
Conductor width	10 µm	20 µm	20 µm
Conductor separation	10 µm	20 to 30 µm	20 µm to 30 µm
Area	≤ 0.1 mm^2	≤ 9 mm^2	≤ 9 mm^2

[A] The under-path conductor is 0.4 µm thick

5.3 S-parameter Sweep

S-parameter measurements and FEM-simulations are first performed on existing integrated S-inductors to verify how well simulations in ADS agree with real circuit performance. Using a Vector Network Analyzer the S-parameters of inductors can be determined by probing samples of the circuits. The focus lies on calibrating and measuring in a frequency range representative of relevant switching frequencies, i.e. from 1 MHz to 500 MHz.

5.3.1 Analysis of S-parameters

From the measured S-parameters of an inductor both the inductance and the parasitic ESR of the inductor can easily be extracted. For a simple series element, such as a single inductor, with impedance Z the $ABCD$-parameters are written as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \tag{5.1}$$

and since the simple model for the inductor impedance is

$$Z = \mathrm{ESR}(\omega) + j\omega L(\omega) \tag{5.2}$$

both the inductance (proportional to $\mathrm{Im}\{Z\}$) and ESR (equal to $\mathrm{Re}\{Z\}$) can be extracted from the B-parameter. More specifically the B-parameter is extracted from measured S-parameters as

$$B = Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}}$$

where B and S are functions of frequency and Z_0 is the characteristic impedance, in this case $Z_0 = 50\,\Omega$ [46]. Consequently, the inductance L and parasitic ESR can be extracted from an S-parameter sweep as

$$L(\omega) = \frac{1}{\omega}\mathrm{Im}\{B\} = \frac{1}{\omega}\mathrm{Im}\left\{ Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}} \right\} \tag{5.3}$$

$$\mathrm{ESR}(\omega) = \mathrm{Re}\{B\} = \mathrm{Re}\left\{ Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}} \right\}. \tag{5.4}$$

5.3.2 Result from S-parameter Measurements

The resulting inductance and ESR of the existing S-inductors as they appear after extraction from the S-parameter measurements, using (5.3) and (5.4), is presented in Figure 5.3.

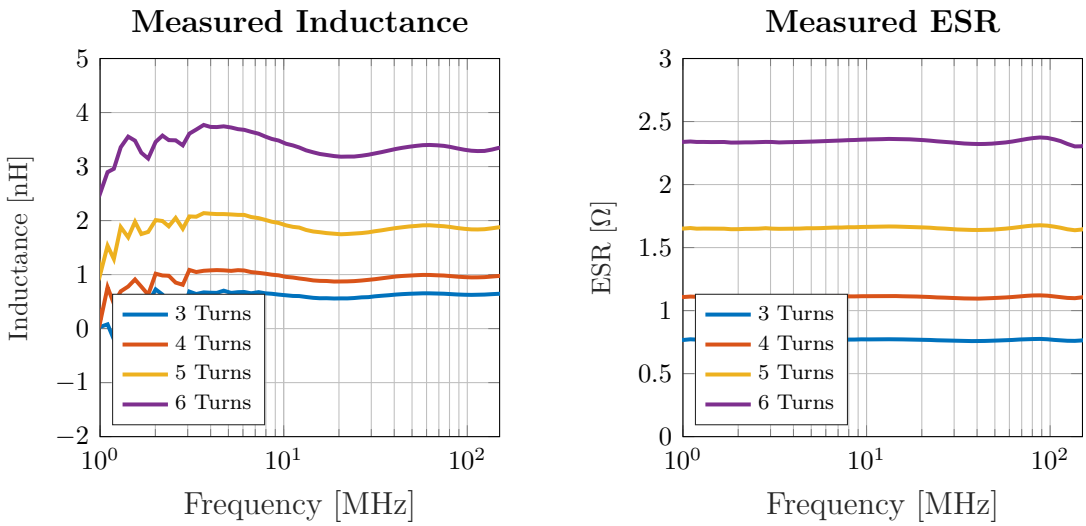


Figure 5.3: The extracted inductance and ESR from S-parameter measurements for four different S-inductors with a varying number of turns.

5.3.3 Simulation Results for S-, M-, and T-inductors

The simulated inductance together with the corresponding ESR, for a selection of measured and simulated components, is plotted in Figure 5.4. An L/ESR-ratio of 43.7 nH Ω^{-1} was on average acquired for the T-inductors while the corresponding fit for the M-inductors gave 13.5 nH Ω^{-1} with two metal layers of thickness 5 µm. Also shown in Figure 5.4 are the measured and simulated fits of the L/ESR-ratio for the standard MMIC inductors, providing only 1.9 nH Ω^{-1} in simulations and 1.4 nH Ω^{-1} in measurements. The resemblance between the measured and simulated standard inductors is strong albeit their L/ESR-ratio is low compared to the larger inductors in the different enhanced technologies.

Moreover, the simulated gain in L/ESR-ratio with $5 + 5$ µm as opposed to $2.5 + 5$ µm for the M-technology is substantial, increasing with 80% from 7.5 nH Ω^{-1} to 13.5 nH Ω^{-1}. By limiting the size of the T- and M-inductors to 3 mm $\times$ 3 mm the maximum obtainable inductance is effectively limited as well. For the T-inductors the highest simulated inductance at 50 MHz is 440 nH with 10.9 Ω ESR, which required 28 windings. Even though the difference is slight, higher L/ESR-ratio values were obtained with the largest possible outer dimension for the T-inductors. For the M-inductors L/ESR decreased after venturing outside outer diameters of approximately 1 mm. The M-inductors could provide well over 600 nH in the simulations, however, as the ESR ventures above 50 Ω this design region is of little interest.

Moreover, all simulated inductors show a strong frequency dependence of the L/ESR-ratio. In Figure 5.5 this frequency dependence is exemplified for specific M- and T-inductors both featuring an inductance of approximately 220 nH at 50 MHz and requiring an area of 1.4 mm^2 and 9 mm^2 respectively.

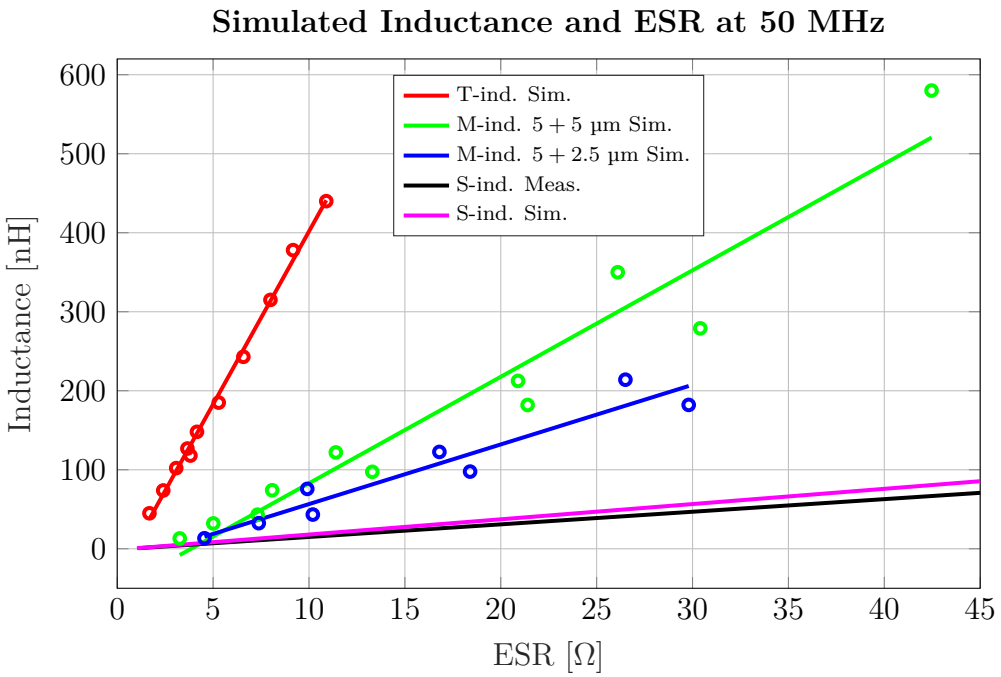


Figure 5.4: The simulated and measured inductance as a function of the ESR for T-, M-, and S-inductors with different conductor separations. Circles represent ADS FEM-simulation and the lines are fitted linear functions for each inductor type.

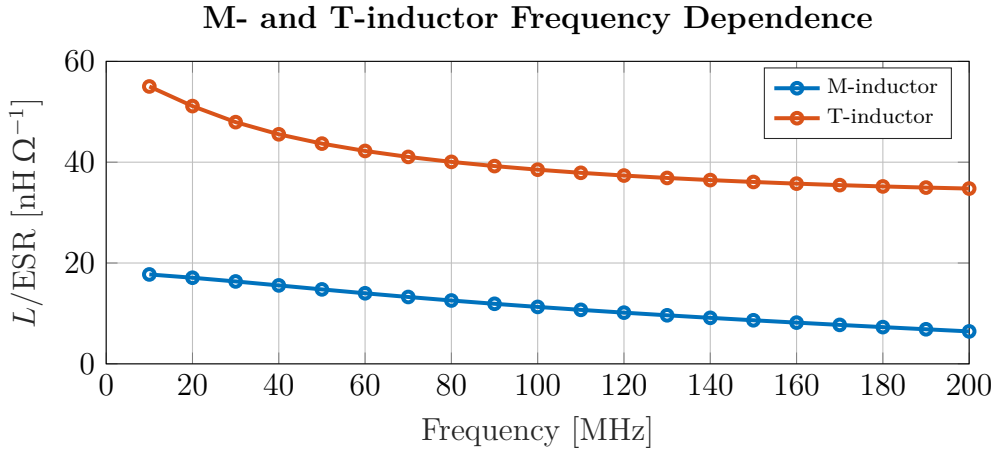


Figure 5.5: The frequency dependence of the L/ESR-ratio for an M- and T-inductor respectively both featuring approximately 220 nH at 50 MHz.

5.3.4 Substrate Parameters for M- and T-inductors

The properties of the substrate layers play an important role in the performance of the M- and T-inductors. As the thickness of the BCB and conductors increase the manufacturing process rapidly becomes more complex, expensive, and prone to errors. Keeping the process as simple as possible while pursuing better performing inductors is an important trade-off.

In the case of the M-inductors the 10 µm thickness of the BCB buffer layer and the center layer, that separates the two conductor levels, was not arbitrarily chosen. In Figure 5.6 the L/ESR-ratio has been simulated for different thicknesses of the center BCB layer, it is clear that the benefit of increasing this layer beyond 10 µm are minuscule. In the same way, an increasing buffer thickness also improves performance, but with only a slowly increasing L/ESR-ratio across the entire simulated thickness range. Consequently, a buffer layer thickness of 10 µm is deemed sufficient. The impact of the buffer thickness on M-inductor performance is presented in Figure 5.7.

For the T-inductors also the increase in L/ESR with buffer thickness is comparatively slow, which can be seen in Figure 5.8. The most rapid performance gains for the T-inductors are instead found for increasing conductor thickness, up to approximately 30 µm, as presented in Figure 5.9. In Figure 5.10 the conductor thickness is varied for a buffer thickness of 30 µm, showing a similar behavior as is in Figure 5.9 meaning that the impact of the buffer and conductor thickness on L/ESR are mutually independent. If the M-inductors see diminishing performance returns from venturing over 10 µm buffer and center separation and this sets a goal for developing the existing process, the situation is the same for T-inductors using conductor and buffer thicknesses of 30 µm.

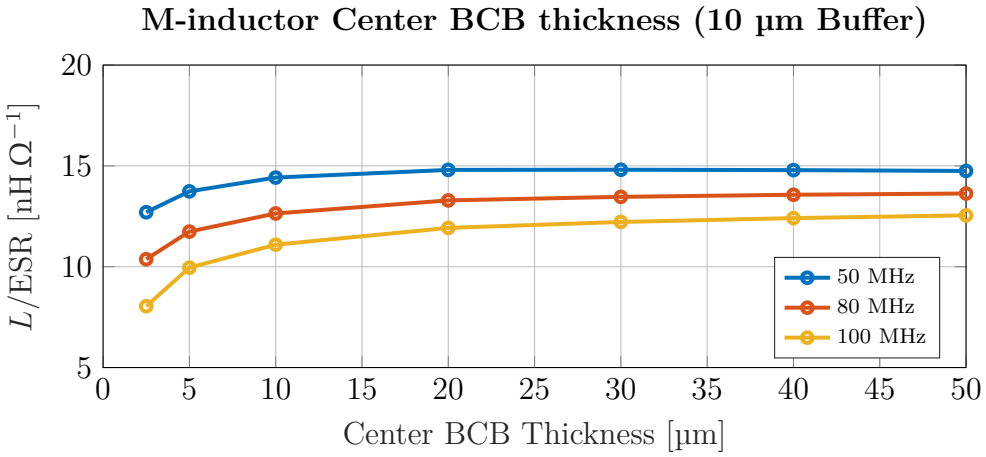


Figure 5.6: The thickness of the BCB layer that separates the two conductor layers in the M-inductors and the resulting L/ESR-ratio. (10 µm buffer thickness)

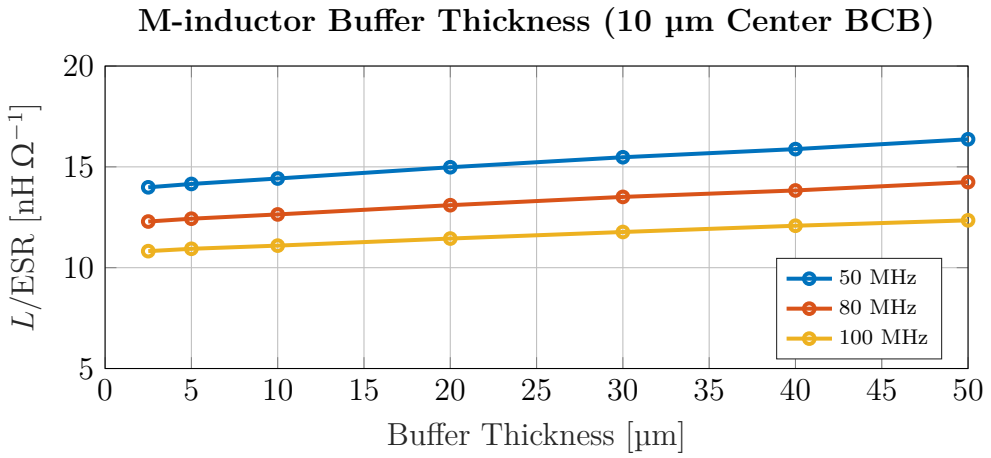


Figure 5.7: Performance (L/ESR) for the M-inductors with buffer BCB thickness.

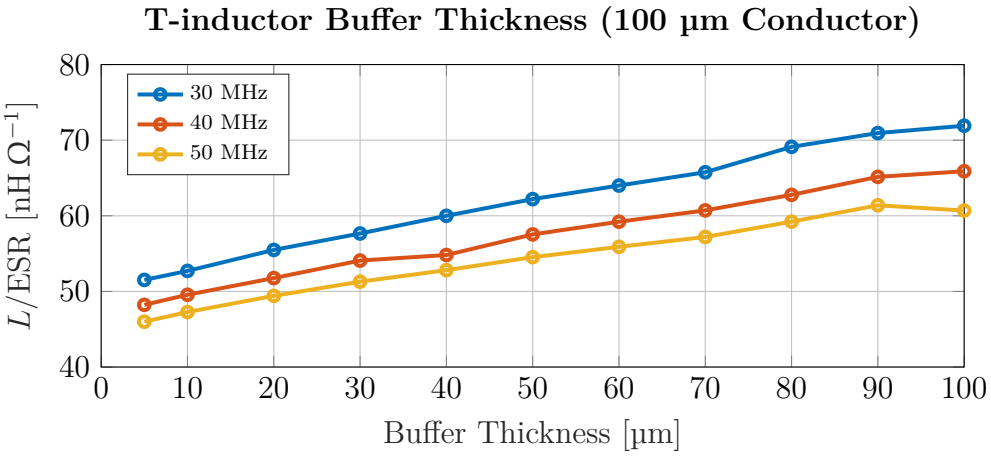


Figure 5.8: The impact of buffer thickness on the L/ESR-ratio for the T-inductors (100 µm conductor).

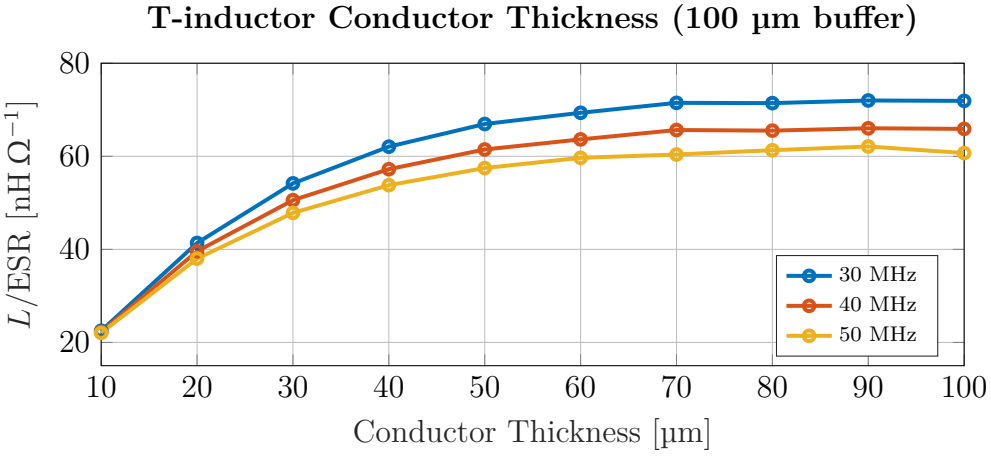


Figure 5.9: T-inductor performance for different conductor thicknesses (100 µm buffer).

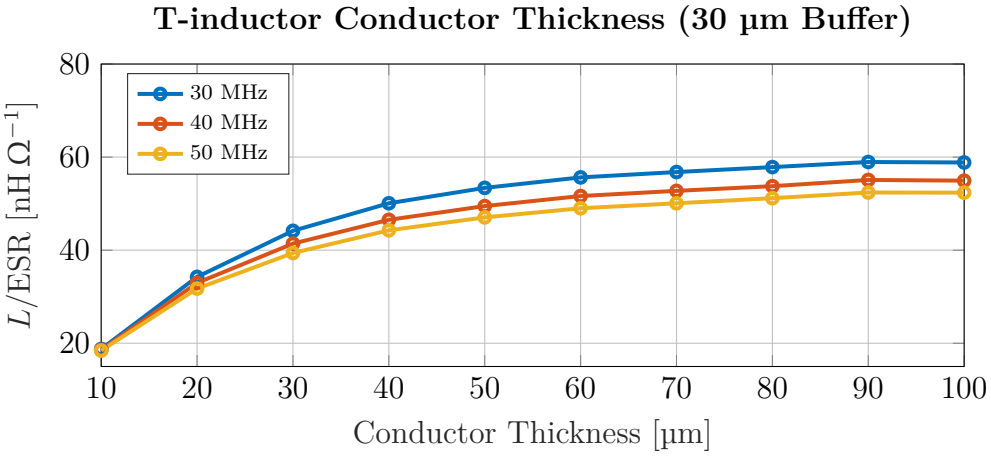


Figure 5.10: With a buffer thickness of 30 µm the same decrease in L/ESR with decreasing conductor thickness is observed.

5.4 DC Breakdown Measurements for S-inductors

To determine the current handling capabilities of the standard technology a DC supply will be used to sweep the current through the inductors. Starting from 0 A with a Keithley 2420 power supply the goal is to incrementally increase the current until the inductor structure fuses. By continuously reading the current and voltage level set by the supply, the breaking point can easily be spotted as the point where the inductor does no longer behave resistive.
The maximum DC current that could be passed through each of the 9 existing S-inductors is plotted in Figure 5.11. As seen the maximum current before the inductors fuse ranges from 1.19 A to 1.38 A. In Figure 5.12, the visible effect of the fusing is presented, it is clear that the critical part of the inductor is the thin (0.4 µm) under-path that connects the center of the coil to one of the ports. As the number of turns increases, this under-path grows longer and the fuse current should intuitively decrease as a longer transmission line should feature higher ESR, dissipate more heat, and consequently break at lower current levels. This trend is clearly visible in Figure 5.11, the exception being the inductor with wider coil conductors. However, the under-path is at the same time wider in this device explaining the improved current tolerances. Lastly, it is observed that inductors with wider center separation show a decreased maximum current tolerance but the difference compared to the standard layout diminishes as the number of turns increases.

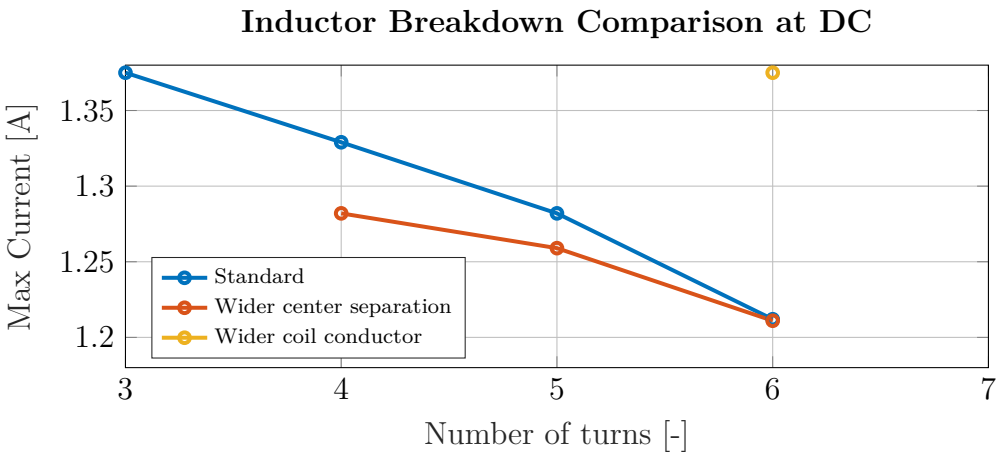
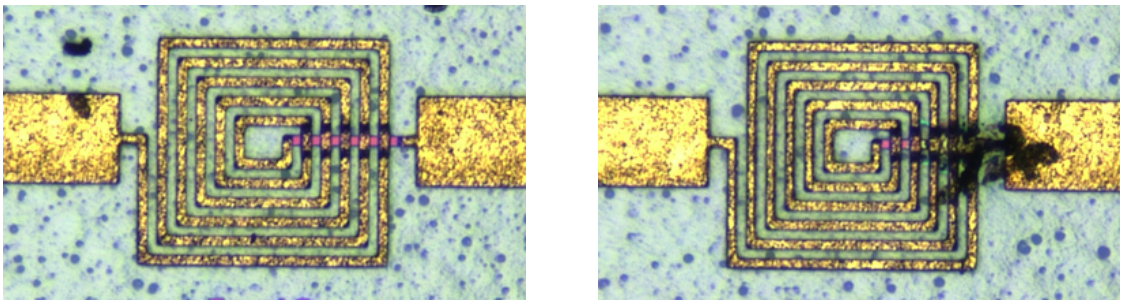


Figure 5.11: Measured breakdown current for the 9 different existing S-inductors.



(a) **(b)**

Figure 5.12: Images showing the same S-inductor design (6 turns standard), where (a) is in working condition and (b) has fused after a high current was supplied.

5.5 Integrated Capacitors

Integration of capacitors also poses challenges for a fully integrated voltage converter. In theory, a parallel plate capacitor can be designed for an arbitrary capacitance using the simple equation [47]

$$C = \frac{k\epsilon_0 A}{d} \tag{5.5}$$

where k is the dielectric constant for the isolating material, $\epsilon_0 = 8.854 \times 10^{-12}\ \mathrm{F\,m^{-1}}$ the permittivity of free space, A the plate area and d the plate separation. As seen, high density capacitors benefit from high-k dielectric materials. Using Silicon Dioxide (SiO_2) or Silicon Nitride (Si_3N_4) with $k = 3.9$ and $k = 7.5$ respectively [48] the capacitance densities in Figure 5.13 can be obtained. Since the dielectric materials feature a field strength of $10^7\ \mathrm{V\,cm^{-1}}$ [48] there exists a lower limit of the plate spacing depending on the desired stress voltage tolerance. As shown in Figure 5.13 the minimum plate spacing to allow a maximum voltage of 300 V is approximately 300 nm, limiting the capacitance density to $0.2\,\mathrm{nF\,mm^{-2}}$. Also presented in Figure 5.13 is the simulated capacitance density for either a $2 \times 2\ \mathrm{mm^2}$ square

capacitor and a 1×4 mm^2 rectangular capacitor. As seen, the theoretical expression (5.5) gives results similar to the FEM simulations, however, the simulations take into account edge effects, a finite conductor thickness and a ground plane while (5.5) assumes a free space environment, infinitely thin conductors and does not treat the frequency dependent edge effects [47].

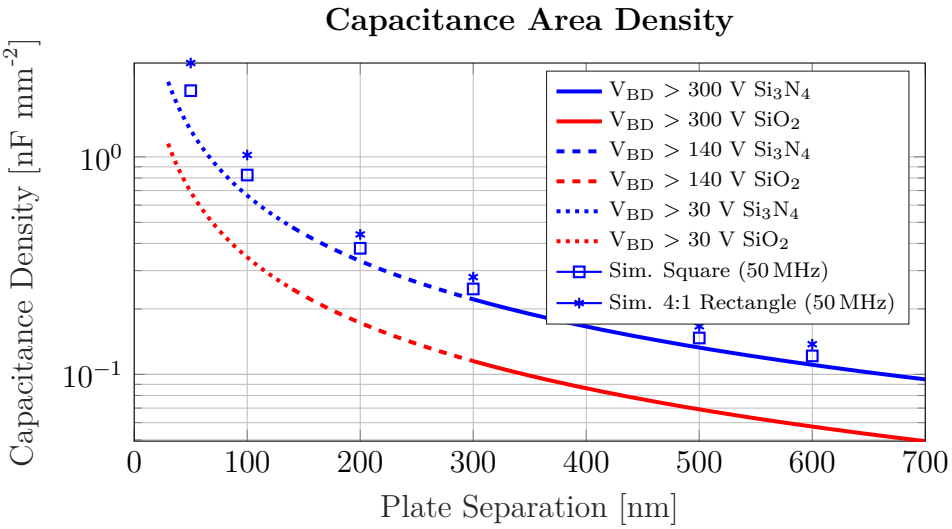


Figure 5.13: The capacitance density obtainable with SiO_2 or Si_3N_4 as dielectric media as a function of the plate separation d and the breakdown voltage V_{BD}. Results both from theory and FEM simulations at 50 MHz.

6

Integration Feasibility

Using the simulated result from the different DC-to-DC converter topologies in Chapter 4 and the simulated properties of the passive components from Chapter 5 two sets of fully integrated DC-to-DC converters are proposed. The first set uses the enhanced multi-layer technology and offers the M-inductors while the second set uses the thicker technology the associated T-inductors. The details of which were presented in Table 5.2.

Applicable to both design sets are realistic assumptions of the GaN HEMT performance which is covered in Section 6.1 and some further design assumptions are made in Section 6.2. An overview of all the final analyzed DC-to-DC power stages is found in Table 6.1.

The S-technology, and associated S-inductor performance, is not well suited for realizing these DC-to-DC converters and thus not analyzed in detail. For reference, with an assumed inductor performance of $1.9\,\mathrm{nH}\,\Omega^{-1}$ the optimum BC design (in terms of minimum $P_{\mathrm{ESR}} + P_{\mathrm{Coss}}$) reaches an theoretical efficiency of $\eta = 43.3\%$ at 180 MHz.

Table 6.1: All the simulation parameters used to reach the optimum efficiency for each design in the multi-layer (M) and thick (T) technology respectively. More details of the technologies and inductors are covered in Table 5.2. $P_{\mathrm{loss,\ min}}$ is the minimum simulated loss.

Technology	Multi-layer (M-inductors)			Thick (T-inductors)		
	BC	MIBC	SCC+BC	BC	MIBC	SCC+BC
f_{sw} [MHz]	77	100	0.6 and 150	40	60	0.6 and 80
η Theory	47.6%	50.1%	66.4%	63.8%	66.6%	71.9%
η Sim.	47.4%	46.8%	65.0%	61.6%	64.8%	71.1%
P_{out} [W]	26.3					
$P_{\mathrm{loss,\ min}}$ [W]	29.0	26.2	14.2	16.4	14.3	10.7
Area [mm^2]	3.5	9.5	35	11.5	26	35.5
$D_{\mathrm{high,\ ON}}$	0.17	0.28	0.17	0.14	0.25	0.14
L_{f} [nH]	173	2 × 250	80	230	2 × 440	150
L_{f} ESR [Ω]	17	23	8	8.3	10.9	3.8
C_{f} [nF]	3					

6.1 GaN HEMTs for Power SoC

To bridge the gap in GaN devices with breakdown voltages between 100 and 600 V a linear fit between the two localized GaN groups in Figure 6.1 is utilized. Specifically, the least squares fit gives

$$\frac{C_{\text{oss}}}{i_{\text{ds, max}}} = 0.0037 \times V_{\text{BD}} + 0.2112 \tag{6.1}$$

with C_{oss} in pF. Furthermore, the efficiency of a conventional BC stepping down 270 V to 28 V at 25 W is easily linked to the $C_{\text{oss}}/i_{\text{ds, max}}$-ratio, these 90% efficiency limits for different f_{sw} are also presented in Figure 6.1 for reference. To develop accurate approximations for the on-chip area requirements it is assumed that the transistor size scales with the maximum rated drain current and that a GaN transistor rated for 3 A requires approximately 750 µm×200 µm or 0.2 mm^2 accounting for vias and providing some design margin.

Moreover, the feasibility analysis will primarily focus on the trade-off between C_{oss} and inductor ESR, which are the most important factors determining system loss, switching frequency and size. The conduction losses from equation 3.13 are on the order of 1 W for GaN devices in this application with $R_{\text{ON}} = 0.5\,\Omega$ (see Appendix A) and $i_{\text{out}} =$ 1 A and both smaller and, more importantly, independent of the switching frequency. Meaning that its influence on the design considerations here is negligible.

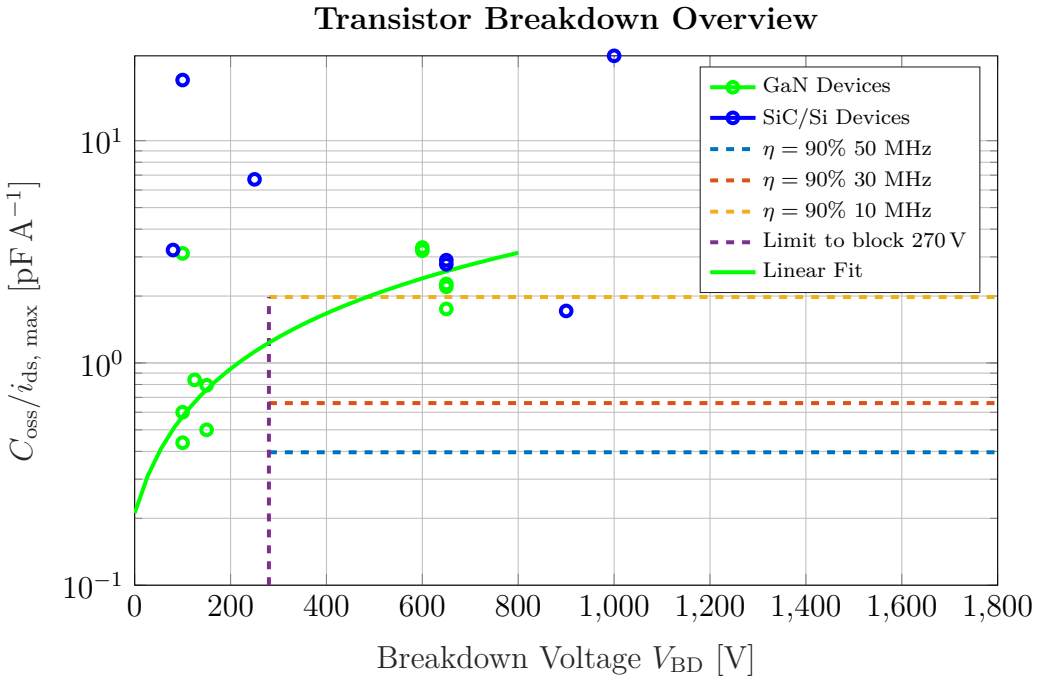


Figure 6.1: Performance metrics for devices in GaN, Si and SiC together with a linear fit between the two groups of GaN devices and efficiency boundaries for a conventional BC with regards to C_{oss} loss only. More details of the devices in Appendix A.

6.2 Passive Components

The performance of inductors in the M-technology is mandated by the simulated sets of M-inductors in Figure 5.4, providing approximately $10\,\mathrm{nH}\,\Omega^{-1}$. The T-technology provides inductors with an increased performance which scales with the conductor thickness, providing 40, 32 and $20\,\mathrm{nH}\,\Omega^{-1}$ with $3\,\mathrm{mm} \times 3\,\mathrm{mm}$ inductors and a conductor thickness of 10, 20 and 30 µm respectively (Figure 5.10).

The capacitance density, as well as the associated breakdown voltage, is set by (5.5) and is inversely proportional to the plate separation. It is assumed that the same technology enables capacitors with arbitrary and different plate spacing (at least two thicknesses are needed). If the highest required voltage tolerance mandates the capacitance density of also the low voltage capacitors much precious circuit area will be lost. This is by no means an industry standard, but similar capacitor design freedom is occasionally offered in industry. In the commercial D01GH-process by OMMIC two different integrated capacitors are offered, showing different capacitance density and breakdown voltage [49].

6.3 Area Estimation of BC Topology

With the M-inductor performance a single stage 270 to 28 V BC is not an attractive design option. In a single stage BC the output current goes through a single flywheel inductor, and the ESR of this inductor degrades the efficiency very rapidly, as seen in Figure 4.7. This means that technologies with higher L/ESR- ratios, such as the T-technology, will be more favorable for realizing an efficient BC.

6.3.1 Multi-layer Technology

In CMO and at 26.3 W output the peak current through the high side device is, from (3.9), 2 A. A GaN transistor with 2.1 A $i_{\mathrm{ds,\,max}}$ and $V_{\mathrm{BD}} = 280\,\mathrm{V}$ would according to the linear performance fit in (6.1) have $C_{\mathrm{oss}} = 2.6$ pF. Using this together with the loss expressions for P_{ESR} and P_{Coss}, (3.17) and (3.15), the theoretical losses caused by inductor ESR and parasitic device capacitances can be calculated as a function of frequency for the BC. In Figure 6.2 these losses are plotted separately and as a sum, there exists a region of minimum loss of 29 W around 77 MHz. At this frequency an inductance of 173 nH is required. Such a component requires approximately $1.0\,\mathrm{mm}^2$ of circuit area and features an ESR of $17.3\,\Omega$ with the $10\,\mathrm{nH}\,\Omega^{-1}$ assumption.

Simulations show a maximum efficiency of $\eta = 47.4\%$ at 77 MHz with a 173 nH and a 3 nF flywheel inductor and capacitor that keeps $V_{\mathrm{out,\,p2p}} \leq 2$ V. This agrees well with the suggested loss from Figure 6.2 which suggests an efficiency of $\eta = 47.6\%$. A schematic overview of the on-chip space requirements of the different components is presented in Figure 6.3, much space remains for integrating input filter and driver circuitry in this design option.

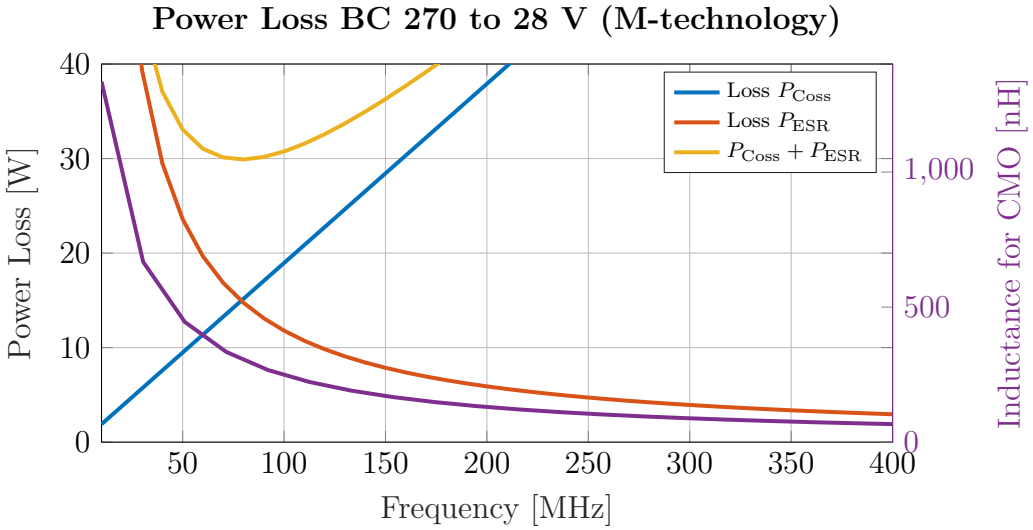


Figure 6.2: The power loss from inductor ESR and parasitic device capacitance as a function of frequency for a BC realized in the M-technology, at an output power of 26.3 W.

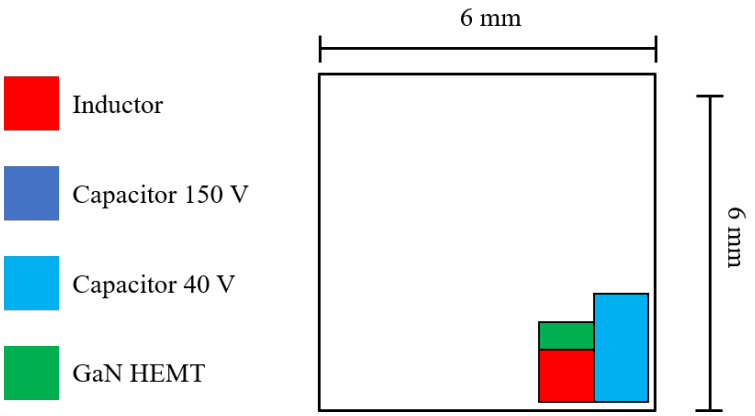


Figure 6.3: A schematic drawing of the space requirements for each component type in the suggested integrated Buck converter using the M-technology.

6.3.2 Thick Conductor Technology

Using the T-technology and allowing for T-inductors with conductor thicknesses of 10, 20 and 30 µm higher inductance to ESR ratios are achievable. In Figure 6.4 the sum of the loss factors P_{ESR} and P_{Coss} for different conductor thicknesses is compared, showing minimum loss at lower frequencies compared to the same topology in the M-technology (Figure 6.2). More specifically, the graphs in Figure 6.4 suggest efficiencies of 55.5, 61.2 and 63.8% for 10, 20 and 30 µm conductor thickness respectively, at 26.3 W. Simulations with $C_{\text{oss}} = 2.6\,\text{pF}$ and inductor performance from the FEM simulations verify these numbers by approaching the theoretical efficiencies to within 3 percentage points in each case. With 30 µm conductor thickness the simulated efficiency is 61.6% at an optimum switching frequency of 40 MHz, with the required 340 nH and 8.5 Ω inductor. A schematic of the required component area is plotted in Figure 6.5.

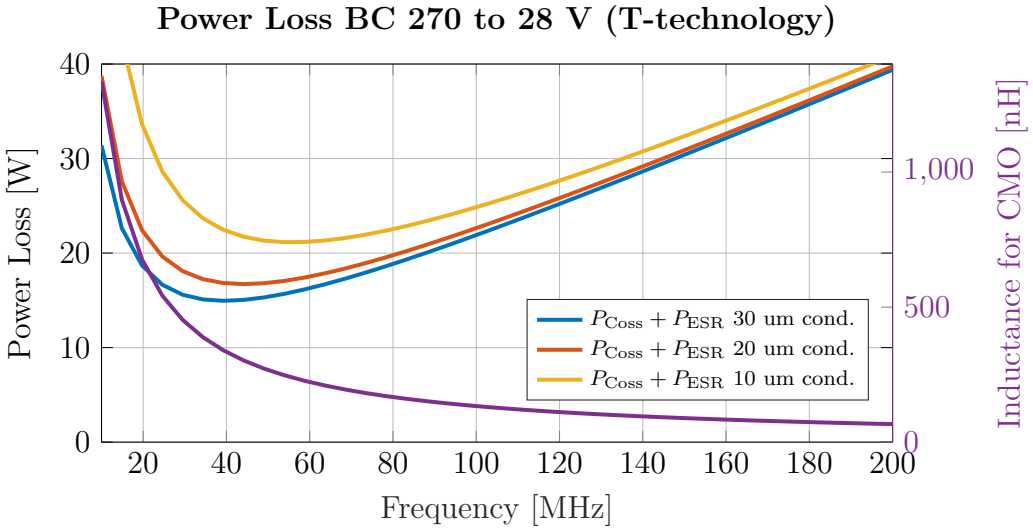


Figure 6.4: The sum of the loss terms together with the required inductance for CMO at 26.3 W output power in the T-technology.

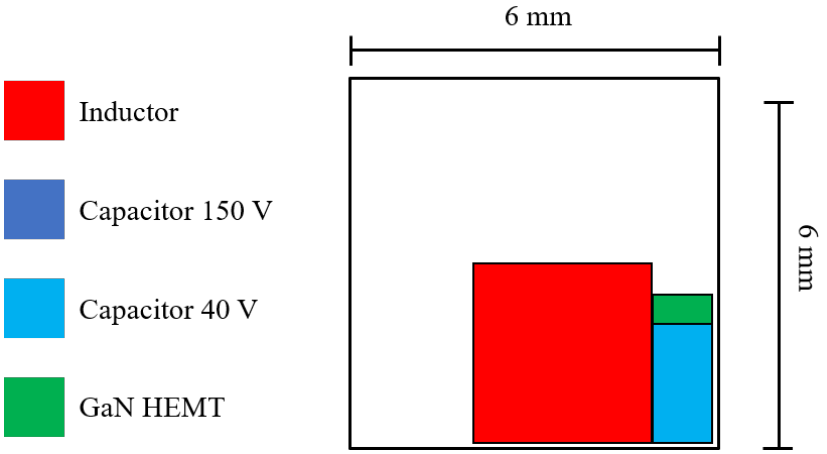


Figure 6.5: The approximate component area for a conventional BC realized with T-inductors with 30 µm conductor thickness.

6.4 Area Estimation of MIBC Topology

Compared to the BC a two-phase MIBC is less sensitive to flywheel inductor ESR. As seen in Figure 4.14 a theoretical efficiency of 75% is still obtainable with inductor ESR of 20 Ω. Moreover, utilization of different active devices with low voltage transistors as TH1, TL1 and TL2 and a high voltage transistor as TH2 did show efficiency improvements in Figure 4.12. As before, using the fit (6.1) gives $C_{oss} =$ 2.6 pF for TH2. For the the other transistors a voltage tolerance of 150 V and current tolerance of 2.1 A $i_{ds,\,max}$ gives an approximate parasitic output capacitance of 1.6 pF. As opposed to the situation with the BC the same equations, (3.17) and (3.15), cannot be applied directly to the MIBC, especially if different transistors

with different C_{oss} are used. As an attempt the parasitic losses can be approximated as the average,

$$P_{\text{Coss, MIBC}} = \frac{1}{4}\left(3C_{\text{oss-L}} + C_{\text{oss-H}}\right) V_{\text{in}}^2 f_{\text{sw}}, \tag{6.2}$$

where $C_{\text{oss-L}}$ and $C_{\text{oss-H}}$ in this case are 1.6 pF and 2.6 pF respectively. Furthermore, as half the output current goes through each branch, the inductor ESR losses for the MIBC are expressed as

$$P_{\text{Inductor, MIBC}} = 2 \times \text{ESR}_{\text{inductor}} \times \left(\frac{i_{\text{out}}}{2}\right)^2 \tag{6.3}$$

i.e. the half of the corresponding losses for the conventional BC. These loss approximations are applied both to the M- and T-technology realization.

6.4.1 Multi-layer Technology

With the loss relationships, (6.2) and (6.3), the power losses from Figure 6.6 are acquired for an MIBC realized with M-inductors. The highest efficiency reached in simulations is $\eta = 45.8\%$ at 100 MHz with $L_{\text{f}} = 250\,\text{nF}$ (ESR $= 25\,\Omega$), $C_{\text{f}} = 3\,\text{nF}$ and $C_{\text{t}} = 2\,\text{nF}$. With a power loss of 26.2 W from Figure 6.6 at an output power of 26.3 W, implying an efficiency of 50.1%, the simulated result is close to the governing theoretical equations. An approximation of the needed circuit area to realize this design is presented in Figure 6.7.

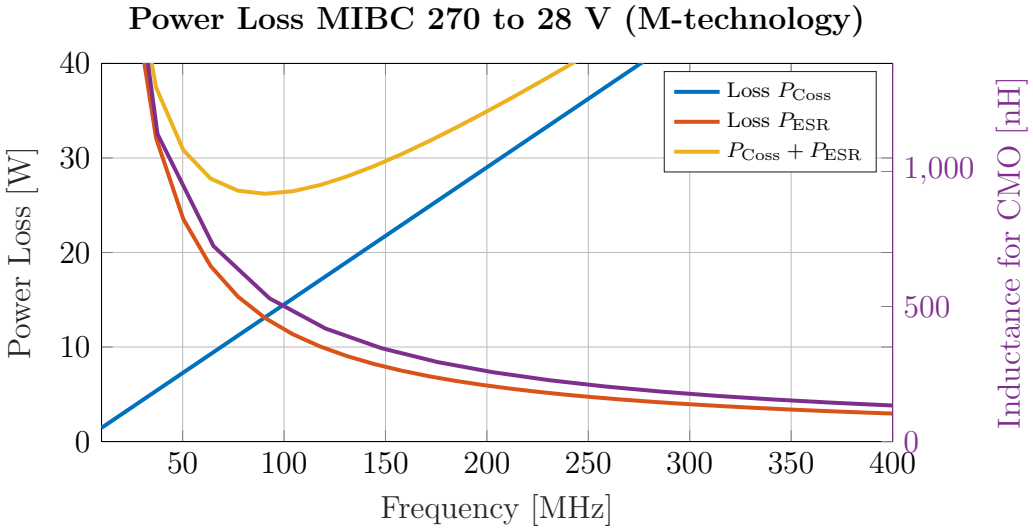


Figure 6.6: The power loss due to parasitic capacitance and inductor ESR for the MIBC realized with the M-technology.

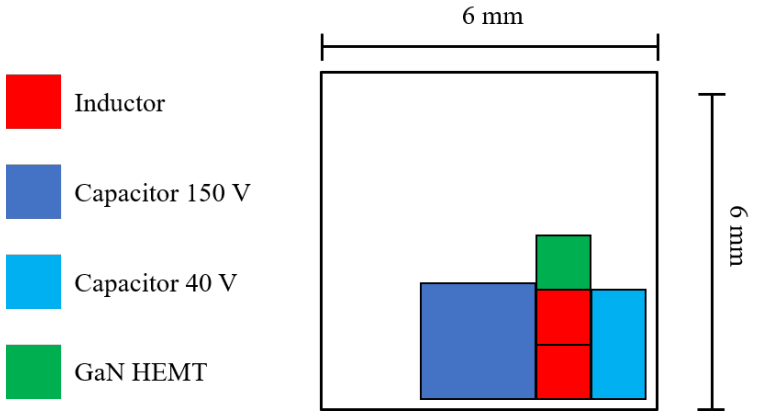


Figure 6.7: An approximate plot of the area requirement for each component type for realizing an MIBC in the M-technology.

6.4.2 Thick Conductor Technology

The optimal switching frequency for an MIBC with T-inductors is compared for different conductor thicknesses in Figure 6.8. By forcing CMO the required inductance in each branch is much higher compared to the BC. Limiting the inductor footprint to 3 mm × 3 mm the highest inductance simulated for a T-inductor with 30 µm buffer and 30 µm conductor thickness is 440 nH with an ESR = 10.9 Ω. This puts a lower limit of 60 MHz to operate the T-technology MIBC with 3 mm × 3 mm inductors. Fortunately, the valleys of minimum loss in Figure 6.8 stretches into 60 or even 70 MHz without much trade-off. At 60 MHz and with C_t = 2 nF the efficiency at 26.3 W output power of the MIBC with T-inductors is 59.6, 64.7 and 66.6% for 10, 20 and 30 µm conductor thickness respectively. Again these η values are verified to within 3 percent points in simulations.

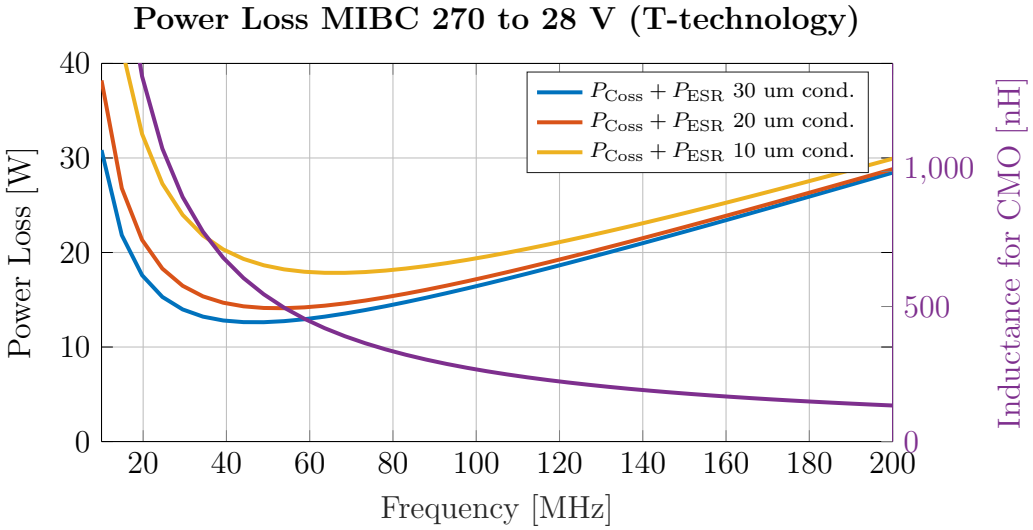


Figure 6.8: The power loss as a function of frequency for the MIBC topology with different conductor thicknesses in the T-inductors.

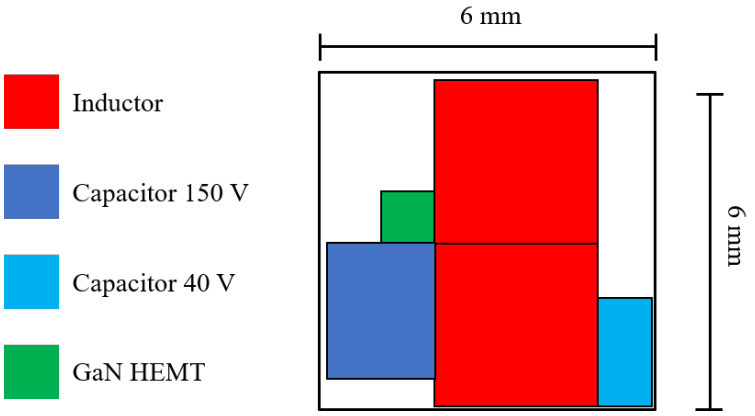


Figure 6.9: The size of each component type for an MIBC realized with T-inductors with 30 µm conductor thickness operating at 60 MHz.

6.5 Area Estimation of SCC and BC Topology

For a SCC at 400 kHz providing a VSDR of 2 the parasitic output capacitance of the transistors is not as big of an issue compared to the Buck-type topologies with higher VSDR. One of the commercially available GaN transistors in Figure 6.1, the GS0650041L from GaN Systems ($C_{\text{oss}} = 7.7$ pF, $i_{\text{ds, max}} = 3.5$ A and $V_{\text{BD}} = 3.5$ A), would in theory be able to operate a SCC at 400 kHz at an efficiency of $\eta = 90\%$ with $C_1 = C_2 = 5$ nF, promising higher efficiencies with larger capacitors. Interpolating with (6.1) however gives, as before, $C_{\text{oss}} = 2.6$ pF as an even better approximation for the transistors. More of a design concern for the SCC is the size of the capacitors C_1, C_2 and C_{o}. Using Si_3N_3 and a plate spacing of 150 nm (to withstand a maximum voltage of 150 V) a capacitance density of around 0.4 nF mm^{-2} is achievable. How much area that can be allocated for capacitors C_1, C_2 and C_{o} of the SCC depends on the properties of the BC stage in each technology.
With a VSDR = 2 SCC as pre-stage of the BC the benefits in the design of the BC are many. The voltage stress that each transistors needs to tolerate decreases from 270 V to 135 V and, consequently, the expected C_{oss} of the devices decreases to 1.6 pF. This means that the switching frequency can be increased with maintained or improved efficiency and smaller flywheel inductors can be used with lower ESR.

6.5.1 Multi-layer Technology

In Figure 6.10 the loss factors P_{Coss} and P_{ESR} is plotted as function of frequency for a BC operating at 26.5 W at the edge of CMO with an M-inductor. As seen the optimum switching frequency is found within 150 to 250 MHz where the sum of the two loss terms equals approximately 10.9 W, implying an efficiency of 72.6%. ADS simulations show an efficiency of 71.1% at 150 MHz with an 80 nH L_{f} inductor (ESR = 8 Ω) and a 3 nF capacitor C_{f}. The circuit footprint of the inductor is 1 mm^2 and, from Figure 5.13, a 2 mm^2 capacitor with plate separation of 40 nm can provide the required capacitance while maintaining a maximum voltage of 40 V.

Allowing some design margin and accounting for the transistors of the VSDR = 5 BC the needed circuit area is approximately 4 mm^2.

This leaves 32 mm^2 to encompass the switched capacitors, transistors and output capacitor of the SCC on a 6 mm × 6 mm chip area. Accounting for the six active devices 30.1 mm^2 is available for the remaining capacitors. Sharing the space equal between C_1, C_2 and C_o gives 3 × 4 nF which can sustain a voltage of 150 V. Simulating the SCC with these passive components at 200 kHz to 1 MHz gives a maximum simulated efficiency of 91.4% at 600 kHz. Assuming no additional losses the efficiency for the SCC and BC combination is approximated as the product of the efficiencies, giving $\eta = 65.0\%$. A schematic graph of the circuit space usage is presented in Figure 6.11.

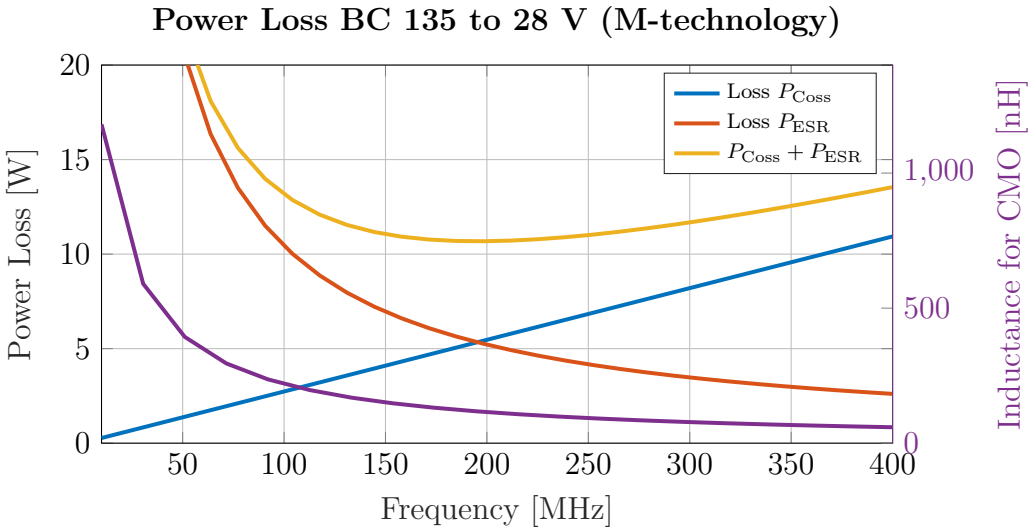


Figure 6.10: The most important loss factors for the 135 V to 28 V BC in the M-technology operating at an output of 26.3 W.

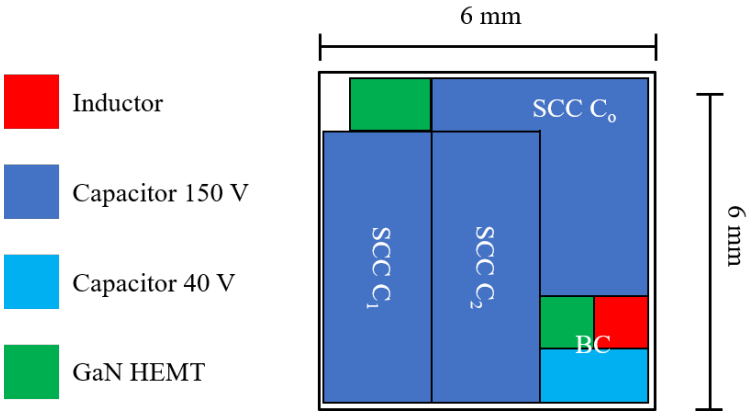


Figure 6.11: A schematic view of the approximate space requirements for the different components of the BC and SCC combination. Realized in the M-technology.

6.5.2 Thick Conductor Technology

The power loss for a BC in the T-technology stepping down 135 V to 28 V is compared for different conductor thicknesses in Figure 6.12. With inductances no larger than 100 nH efficiencies of 74.6, 80.4 and 82.4% can be expected for 10, 20 and 30 µm conductor thickness respectively at 80 MHz. The preceding SCC, however, does not benefit from the thicker conductors or buffer layer of the T-technology, meaning that this pre-stage will be less efficient compared to the M-Technology due to less circuit area being available. The capacitors $C_1 = C_2 = C_o$ must be no larger than 3 nF to fit on the 6 mm × 6 mm chip together with the BC. The simulated efficiency of the SCC operating at 600 kHz is 87.3% meaning that the combination could potentially reach an efficiency of 71.9%. The required area by each component type is presented in Figure 6.13.

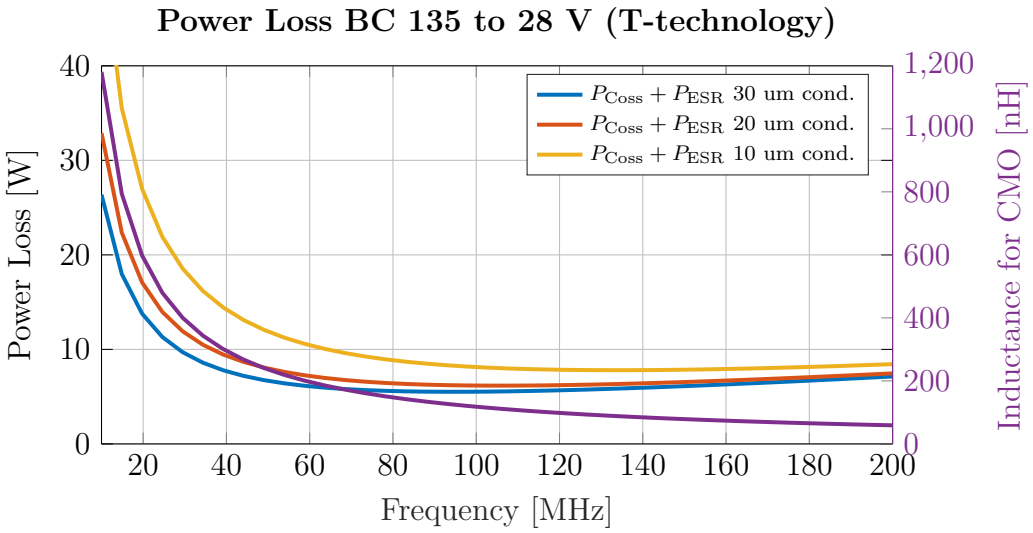


Figure 6.12: The power loss for a 135 to 28 V BC realized in T-technology with different conductor thicknesses.

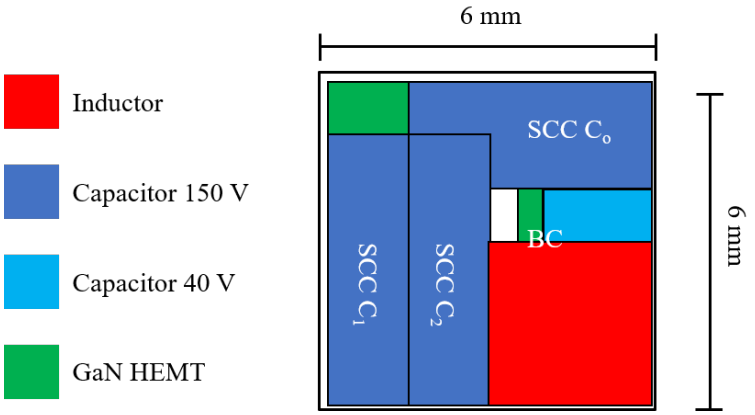


Figure 6.13: The circuit area required by each component for implementing a SCC and BC combination converter with T-inductors.

7
Conclusions

This thesis presented different, fully integrated, design drafts of switched mode power stages that challenge the gap between low voltage integrated and high voltage discrete DC-to-DC converters with high VSDR. It is by no means an all-encompassing collection of suggestions for how this particular gap in DC-to-DC converters can be filled. For instance, many relevant resonant converter topologies have not been covered and the performance of the involved active and passive components originate from simple extrapolations of existing devices or processes, neither of which purposely designed for switched mode power applications.

The suggested designs from Table 6.1 show that fully integrated power stages with efficiencies as high as 65% and 72% are in theory obtainable using the M- and T-technologies respectively, which serves as expanded versions of the Chalmers In-House GaN process. All designs require less than 36 mm^2 chip area and offer different amounts of free space available for any of the supporting circuits, such as those needed for input LP filtering and control, needed for a complete DC-to-DC converter system.

The benefits of the T-inductors in being better suited for power applications than those realized with the M-technology is not evident by just focusing on the improvement in η for the various topologies. Indeed, an increase of up to 16 percentage points for the BC and MIBC converters is a considerable improvement but, even more importantly, is the decreased switching frequency by approximately a factor of 2 for the T-technology. The narrow power stage focus of this thesis does not make the lower switching frequencies justice in terms of potential system-wide efficiency. The T-technology design examples utilizes switching frequencies between 40 and 80 MHz, still very high compared to SiC converters operating at similar voltage levels (on the order of 100 kHz), but promising control circuitry that is more efficient and easier to realize compared to the 77 to 150 MHz required by the M-technology counterpart. It is interesting that while this work has strived for miniaturization by integration of switched-mode power stages the necessity of larger inductors, albeit still realizable in MMIC, was discovered. Increasing the switching frequency to allow for smaller inductances must be met with physically larger inductors featuring lower ESR and the ability to handle the multiple amps of current without much loss.

In summary, the simulated performance and properties of the BC, MIBC and, especially, the SCC + BC topologies are feasible options for fully integrated power stages. In terms of efficiency, these designs are comparable to the previous works presented in Table 3.2 while adding the property of being fully integrated, operating at higher VSDR, and at higher voltage levels. With the assumptions, limitations, and simulations used in this report, nothing suggests that the claim of fully integrated

switched mode power stages at voltage levels of a few 100s of volts is unreasonable with GaN devices.

7.1 Future Work

Further research could expand the findings of this thesis with important information. Especially by focusing more in detail on either the GaN devices in a power application setting or on the here much-neglected control circuitry whose efficiency while driving the power stages suggested in Chapter 6 is crucial. Out of all these aspects of a potential power SoC in GaN MMIC technology that has not been covered here, and would bring valuable insight once addressed, the most important points include:

A. A more in-depth analysis of which GaN transistors can be used in the different converter topologies. The summary of commercially available devices in Figure 2.1 and 6.1 does not, necessarily, give a correct picture of what performance (in terms of $C_{\text{oss}}/i_{\text{ds, max}}$ and V_{BD}) that is obtainable in the intermediate region around $V_{\text{BD}} = 300\,\text{V}$. Custom design of dedicated devices for fully integrated switched-mode DC-to-DC converters could potentially change the device landscape presented quite considerably. Since all topologies are tightly coupled to the transistor parameters new findings in this area could make designs more efficient and feasible. To experimentally measure the turn-on and turn-off times, i.e. the dV/dt performance, of GaN devices at the relevant voltage levels would also provide valuable insight. Primarily for finding the most optimum switching scheme that should be strived for in the control circuitry design.

B. To approach a useful prototype, much further work is needed to realize the control circuitry, and potentially the feedback circuitry, (from Figure 1.1) in the same MMIC process as the power stage. The performance of the surrounding integrated control circuitry will impose new constraints on the power stage and development of these parts side by side is necessary to achieve optimal system efficiency, which is more important than the power stage efficiency studied here.

C. Investigating how lower ESR for passives in the regime of large (200 to 500 nH) integrated inductors can be realized. Inspired by the 100 µm thick 200 nH inductors in [10] and how rapidly the simulated ESR drops once the trace thickness of an integrated spiral inductor is increased (e.g. see Figure 5.9) finding a way of easily manufacturing thicker conductor traces or lowering the ESR by other means is interesting.

D. The environment in which the power SoC operates puts different emphasis on the trade-off between efficiency, steerability, and size. Additional work is required for tailoring the choice of topology and component selection depending on the specifics of the final application. For instance, the converter could be used for providing envelope tracking, meaning that the output voltage is modulated and used as bias for a PA which can operate closer to compression at a wide range of output power levels. As opposed to constantly operating at a single design power, envelope tracking increases efficiency [5]. Analysis of

a fully integrated GaN DC-to-DC converter in this aspect would require more insight into the PA itself, the signal it amplifies and the entire surrounding control circuitry displayed in Figure 1.1.

E. Evaluating the thermal properties of the power stage is another important aspect not covered here. The stated power losses from Table 6.1 are on the order of 10s of watts, which is much considering a fully integrated solution on a 6 mm × 6 mm chip. An investigation of how to effectively dissipate this heat is crucial. Moreover, it has been assumed that the designed M- and T-inductors will be able to tolerate the maximum current of approximately 2 A in the designs, because their conductors are much thicker compared to the C-inductors. However, the maximum current tolerance is not expected to scale linearly with the conductor thickness, as thermal effects will be limiting and break the component once too much heat is generated. Further work should focus on verifying the DC (and AC at relevant f_{sw}) current tolerances of the M- and T-type inductors.

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A

Commercial GaN, Si, and SiC Devices

The commercial devices represented in Figure 2.1 and 6.1 are listed with more details in Table A.1 below.

Table A.1: The details of the commercial GaN, Si, and SiC devices used in Figure 2.1 and 6.1.

Brand	**Model**	$\mathbf{C_{oss}}$**[pF]**	$\mathbf{V_{BD}}$ **[V]**	$\mathbf{i_{ds}^{max}}$ **[A]**	$\mathbf{R_{ON}}$ **[Ω]**	**Type**
CREE	CGHV1J006D	0.35	100	0.8	2.30	GaN
CREE	CGHV1J025D	1.2	100	2	0.60	GaN
CREE	CGHV60040D	1.6	150	3.2	0.56	GaN
CREE	CGHV40050	5.0	150	6.3	N/S	GaN
CREE	CGHV40200PP	7.3	125	8.7	N/S	GaN
GaN S.	GS0650041L	7.7	650	3.5	0.50	GaN
GaN S.	GS0650081L	14.0	650	8	0.23	GaN
GaN S.	GS66502B	17.0	650	7.5	0.20	GaN
Infineon	IGT60R190D1S	40.0	600	12.5	0.19	GaN
Infineon	IGO60R070D1	102.5	600	31	0.07	GaN
GaN S.	GS61004B	140.0	100	45	0.02	GaN
CREE	C2M1000170J	12.0	1700	5.3	1.00	SiC
STM	STP7N65M2	14.5	650	5	0.98	Si
CREE	C2M0280120D	23.0	1200	10	0.28	SiC
STM	LET20030C	29.0	80	9	N/S	Si
STM	STN2NF10	45.0	100	2.4	0.26	Si
STM	STD4NK100Z	53.0	1000	2.2	5.60	Si
CREE	C3M0065090J	60.0	900	35	0.07	SiC
STM	SCTH35N65G2V7	125.0	650	45	0.06	SiC
STM	STAC3932B	134.0	250	20	N/S	Si

B

Details of Control Square Wave

More specifically, the function Square (f, D, δ, t) is extracted from the Fourier series representation of a square wave in time domain. Namely

$$\text{Square}\,(t) = \sum_{n=0}^{n=\infty} a_n \cos\left(n\omega_0 t\right) \tag{B.1}$$

where the coefficients a_n are given by

$$a_n = 2\frac{A}{n\pi}\sin\left(n\pi\frac{T_p}{T}\right) \tag{B.2}$$

where ω_0 is the angular frequency, A the high state value, T_p the time spent in the high state per period and T the period time. This can be simplified since $T_p/T = D$ and $\omega_0 = 2\pi f$ which gives

$$\text{Square}\,(t) = \sum_{n=0}^{n=\infty} 2\frac{A}{n\pi}\sin\left(n\pi D\right)\cos\left(n2\pi f t\right) \tag{B.3}$$

and, after introducing a time delay δ the definition of the function Square (f, D, δ, t) is obtained as

$$\text{Square}\,(f, D, \delta, t) = \frac{2A}{\pi}\sum_{n=0}^{n=\infty}\frac{\sin\left(n\pi D\right)}{n}\cos\left(n2\pi f\left[t-\delta\right]\right). \tag{B.4}$$

In the report, and simulations, to mathematically describe the control signals exactly a constant C needs to be added to the Square (f, D, δ, t) function in order to translate it to a square wave jumping from a negative low-state value up to zero. As opposed to oscillating from $-A/2$ to $+A/2$ as is the default scenario.

C

Results from C-inductor Measurements

The resulting inductance and ESR as extracted from the *S*-parameter analysis of the C-inductors are tabulated in Table C.1 together with the maximum DC current before the component fused.

Table C.1: Properties of the measured commercial inductors at 50 MHz (inductance, parasitic series resistance, and Q-value) and at DC.

N. of Turns	L [nH]	ESR [Ohm]	Q-value	i max [A]
3	0.72	1.13	0.141	1.375
4	0.93	1.20	0.170	1.329
4[A]	1.40[A]	1.49	0.207	1.282
5	1.83	1.82	0.223	1.282
5[A]	2.32[A]	2.06	0.247	1.259
6[B]	2.67[B]	2.01	0.292	1.375
6[A]	3.88[A]	2.79	0.307	1.211
6[C]	3.89[C]	3.02	0.284	1.189
6	3.26	2.57	0.280	1.212

[A] Wider center separation
[B] Wider winding conductor
[C] Pillar-type inductor