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MARIJANA KRIVIĆ Department of Microtechnology and Nanoscience
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Graphene field-effect transistors for high frequency and flexible electronics

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MARIJANA KRIVIĆ

Supervisor: Marlene Bonmann
Examiner: Andrei Vorobiev

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Department of Microtechnology and Nanoscience
Terahertz and Millimetre Wave Laboratory
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

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MARIJANA KRIVIĆ
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Abstract

Graphene field-effect transistors (GFETs), owing to graphene's intrinsically high velocity of charge carriers in combination with flexibility, are considered as key components for development of the new generation of advanced electronics for applications in the areas of high data rate communication, high-resolution sensors, imaging etc. It is well recognised now, that the development of GFETs, operating in the amplifying mode, is challenging due to relatively high differential drain conductance, resulting from the zero energy bandgap in the monolayer graphene, which prevents the drain current saturation and, hence, limits the transistor power gain. However, there is an additional possible effect of the high drain conductance in GFETs – the correspondingly high dissipating power which can result in additional degradation of the transistor high frequency performance due to Joule heating, i.e. self-heating, which is particularly pronounced in GFETs on polymer flexible substrates with inherently low thermal conductivity. This effect has been insufficiently addressed so far. The objectives of this Master's thesis are both theoretical and experimental study of the GFET self-heating, its effect on the transistor high frequency performance and optimisation of the transistor design with the aim to reduce the self-heating.

In this work, GFETs on rigid (Si/SiO_2) and flexible polymer (Kapton) substrates have been designed, fabricated and characterised. The key issues of fabrication of GFETs on flexible substrates, e.g. misalignment during e-beam lithography, have been identified, discussed and addressed. A number of thermal resistance models allowing for evaluation of the GFET channel temperature defined by the self-heating have been considered. The models appropriate for certain GFET layouts and layered structure, on both Si/SiO_2 and Kapton substrates, have been selected and applied. This allowed for considering GFET design optimisation for lower thermal resistance with the aim to reduce the self-heating effect. The actual GFET channel temperature has been measured by the means of infrared imaging and applying method of the thermo-sensitive electrical parameters, i.e. gate and drain currents, which showed a good agreement with the modelling. Finally, the effect of the self-heating on the high frequency performance of the fabricated devices has been analysed.

Keywords: graphene field-effect transistors, Joule heating, self-heating, thermal resistance, high frequency electronics, flexible electronics, Kapton, infrared imaging, thermo-sensitive electrical parameters.

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1
Introduction

A monolayer of carbon atoms arranged in a hexagonal lattice, namely, graphene, was first isolated by the researchers Geim and Novoselov in 2004 [27]. From that point on, graphene's unique band-structure and remarkable thermal and electronic properties have drawn a tremendous attention in the fields of electronics and physics.

Due to graphene's high charge carrier mobility and high velocity of saturation, graphene field-effect transistors (GFETs) have a potential of contributing, particularly, to the large market of high frequency electronics. Their recent development showed a promising trend in the values of their maximum frequency of oscillation (f_{max}) and cut-off frequenciy (f_T) [28]. However, so far, GFETs still lag significantly behind III-V semiconductor HEMTs, although, they're growing comparable with the widely used Si MOSFETs [29]. Another of graphene's valuable merits are flexibility and transparency. When compared to the other transparent or flexible conducting materials like ITO and organic semiconductors, who's mobility doesn't go above a couple of $cm^2V^{-1}s^{-1}$, graphene's mobility is outstanding which gives it a good prospect in contributing to flexible electronics. Graphene high frequency transistors fabricated on a flexible substrate have been shown to be robust enough to sustain a repeated a fatigue test with minor changes in high frequency performance [30]. Demonstrated robustness and high performance give ground to the development of the high frequency flexible electronics, for which there are high prospects in today's and future technologies.

Alongside these advantages, there are plenty of drawbacks in the development of the actual graphene devices. From a physical standpoint – a lack of bandgap which prevents the true current saturation and prevents the graphene transistor to turn off and from a practical standpoint – a lack of large area high quality graphene sheets. Another drawback is related to the fact that graphene's properties degrade when in contact with other materials as well as the very high contact resistance in metal-graphene contacts [31].

1.0.1 Objective

The objective of this master's thesis has been motivated by the recently developed integrated 200 GHz graphene FET based receiver on the Si/SiO_2 substrate [32] and graphene - based terahertz detector on plastics [33]. The developed flexible detector gives ground for the first graphene based flexible heterodyne receiver. The crucial components of such receiver are amplifiers. However, as opposed to a detector, an amplifier has to be biased. This mode of work unavoidably introduces a substantial amount of Joule heating which, due to the inherent low thermal conductivity of flexible substrates, might cause performance issues.

In this work, GFETs on rigid (Si/SiO_2) and flexible polymer (Kapton) substrates have been designed, fabricated and characterised. The key issues of fabrication of GFETs on flexible substrates, e.g. misalignment during e-beam lithography, have been identified, discussed and addressed. A number of thermal resistance models allowing for evaluation of the GFET channel temperature defined by the self-heating have been considered. The models appropriate for certain GFET layouts and layered structure, on both Si/SiO_2 and Kapton substrates, have been selected and applied. This allowed for considering GFET design optimisation for lower thermal resistance with the aim to reduce the self-heating effect. The actual GFET channel temperature has been measured by the means of infrared imaging and applying method of the thermo-sensitive electrical parameters, i.e. gate and drain currents, which showed a good agreement with the modelling. Finally, the effect of the self-heating on the high frequency performance of the fabricated devices has been analysed.

1.1 Graphene – physical properties

Graphene is a planar carbon allotrope in which the atoms are arranged in a hexagonal lattice, bound together with covalent bonds. Carbon has four valence electrons and in its elemental form and they occupy the $2s$ and $2p$ orbitals. When arranged in a graphene crystal lattice, one of the $2s$ electrons is excited to the $2p_z$ orbital with the help of the energy gained from the neighbouring nuclei. This arrangement has the effect of lowering the overall energy of the system and thus, it is more stable. The $2s$ orbital interacts with the $2p_x$ and $2p_y$ orbitals and forms three sp^2 hybrid orbitals. The interactions of the sp^2 hybrid orbitals form so called σ-bonds, which are the strongest type of covalent bonds and are responsible for graphene's strength and mechanical properties. The $2p_z$ orbital forms the covalent π-bonds and its electrons are weakly bounded to the nuclei what makes them relatively delocalised. These delocalised elecrons are responsible for the graphene's electronic properties [1].

Carbon atoms in graphene's lattice are separated by roughly 1.42 Å. Graphene's lattice can be characterised by a Bravais lattice, shaded blue on the figure 1.1a, with atoms A or B as its basis. Bravais lattice is a periodic spatial function that is a representation of the arrangement of the atoms in the crystal lattice and as such it is referred to as the *direct lattice*. The most basic unit cell of the Bravais lattice is called the *primitive unit cell*. For a cell to be categorised as a primitive unit cell, it needs to contain exactly one Bravais lattice point and to recreate the lattice when translated through all the Bravais lattice vectors without leaving gaps or overlapping. Graphene's primitive lattice cell is an equilateral parallelogram shaded green on the figure 1.1a bounded by so called *primitive vectors* a_1 and a_2, with a length of 2.6 Å. The grey shaded area on the figure 1.1a is the Wigner-Seitz primitive unit cell, defined just for the mere convenience of its construction (it's edges are connections of the bisection points of the Bravais lattice points) since determining the primitive unit cells is not so apparent in 3D lattices. The graphene reciprocal lattice is depicted on figure 1.1b and it is a result of discrete Fourier transform of the Bravais lattice. As such, it is a function defined in reciprocal space, also referred to as the *momentum space* or *k-space*. Vectors b_1 and b_2 are a transform of vectors a_2 and a_2 to the reciprocal space and they're the basis for the graphene's reciprocal lattice. The shaded hexagonal in figure 1.1b is referred to as the first Brillouin zone which is important for describing the electronic bands of solids.

An expression that describes graphene's electronic band structure reasonably well can be obtained by solving the time-independent Schrödinger equation in 3D space. Using the nearest-neighbour-tight-binding theorem and paying attention that the result wavefunction satisfies the Bloch theorem, that expression looks as follows:

$$E_{\pm}(\mathbf{k}) = \pm t\sqrt{3 + f(\mathbf{k})} - t' f(\mathbf{k}) \tag{1.1}$$

where

$$f(\mathbf{k}) = 2\cos(\sqrt{3}k_y a) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right) \tag{1.2}$$

and where t and t' are the tight-binding factors. The plus sign refers to the conductance (π^*) and minus to the valence (π) band. Since this function is periodical, its nature can fully be depicted by the first period called the first Brilluion zone which is plotted on figure 1.1d. The most interesting of graphene's properties comes from the points where the conductive and valence bands touch. Around these points the bands resemble a cone-like shape. Since the bands touch only in these particular points, graphene cannot be categorised as a metal and because of the absence of the bandgap between the bands, it cannot be classified as a regular semiconductor either which is why graphene is considered a semi-metal or a zero-bandgap semiconductor.

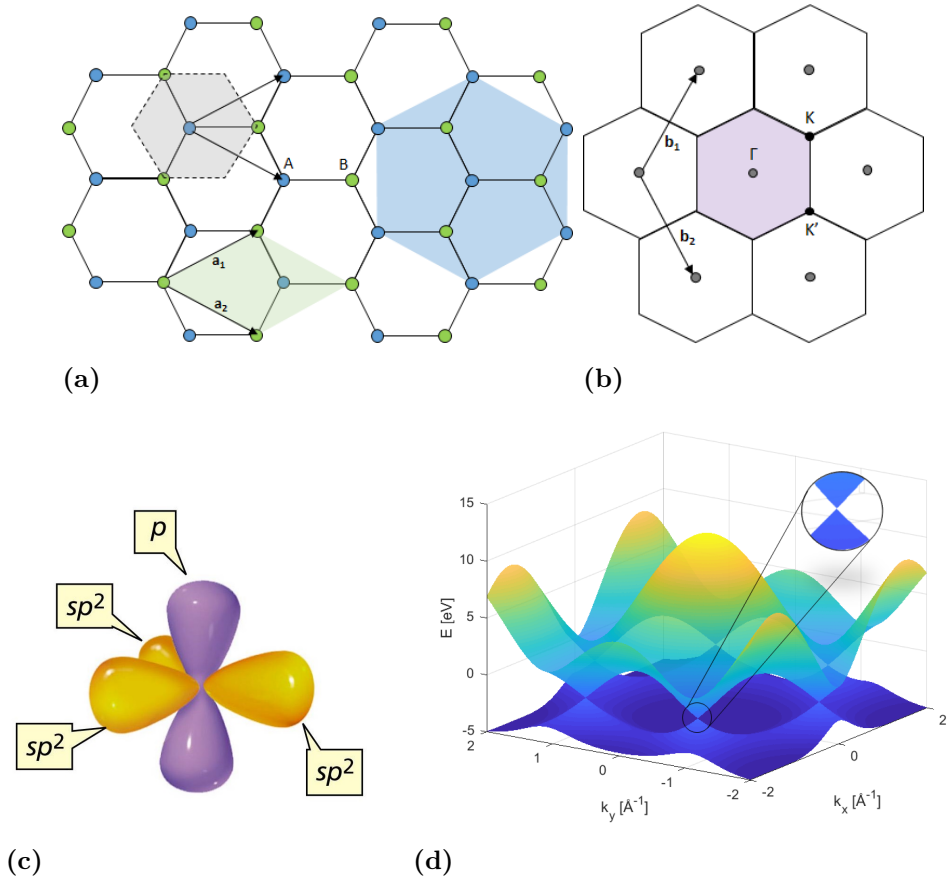


Figure 1.1: Graphene's direct (a) lattice with Bravais lattice shaded blue, primitive lattice shaded green and Wigner-Seitz primitive unit cell shaded grey. Graphene's reciprocal lattice (b) with the shaded first Brilluion zone. Schematical representation of hybridised orbitals [1] (c). (d) the first Brilluion zone of the graphene's dispersion relation plotted for the tight-bonding parameters t = 2.7eV, t' = -0.2t with magnified Dirac cone.

If no external electrical or magnetic field is applied and without any impurity atoms, the Fermi energy will be positioned at the touching point of the bands. The touching point of the cone-shaped band structures is frequently referred to as the Dirac point. Around it, within approximately $\pm 0.6\,\mathrm{eV}$, graphene's energy dispersion can be approximated by the following linear relation:

$$E(k)_{\pm} = \pm\hbar v_F \sqrt{k_x^2 + k_y^2} \tag{1.3}$$

where $\hbar$ is the reduced Planck constant and v_F is Fermi velocity defined by $v_F = (1/\hbar)(\partial E/\partial k)$ at the Fermi energy and equals to 10^6 m/s. Linear dispersion relation represents the so-called massless particles, particles with zero effective mass. Massless particles' dynamics is described by Dirac's relativistic quantum mechanical wave equation, hence the name Dirac points for the bands' touching points.

Furthermore, the density of states (DOS) $g(E)$ for graphene can be calculated from:

$$g(E) = \frac{2}{\pi(\hbar v_F)^2}|E| \tag{1.4}$$

with the help of which the charge carrier concentration can be calculated by:

$$n = \int_0^{E_{max}} g(E) f(E_F) dE = \frac{2}{\pi\hbar^2 v_F^2} \int_0^{E_{max}} \frac{E}{1 + exp(\frac{E-E_F}{k_B T})} dE \tag{1.5}$$

For the special case of intrinsic graphene in equilibrium, the carrier density can be calculated form:

$$n_i = \frac{\pi}{6}\left(\frac{k_B T}{\hbar v_F}\right)^2 \tag{1.6}$$

where k_B is the Boltzmann constant, and T is temperature. From this expression, it follows that, at the room temperature, the intrinsic carrier density is around $10^{11} cm^{-2}$. The amount of charge carriers at the Dirac point in equilibrium is often referred to as the *residual carrier density*.

Material	Graphene	Si	GaAs	InP	GaN	MoS_2	Phosphorene
m_e^*/m_0	0	0.98	0.067	0.073	0.22	0.6	0.2
E_g (eV)	0	1.12	1.42	1.34	3.45	1.8	1.5
μ_e (cm^2/Vs)	200000	1400	8500	4000	500	100	2200
v_{sat} (10^7m/s)	6	1	0.7/2.73	0.67	1.4	0.3	1
κ (W/cmK)	20-40	1.56	0.5	0.68	1.95	1.31	1.01

Table 1.1: Comparison of relevant properties of semiconductor materials used or with a potential to be used in high-frequency electronics. Data extracted from [6–19]

A comparison of relevant parameters when it comes to high frequency electronics in different materials is listed in table 1.1. Si, GaAs, InP and GaN are bulk semiconductor materials, commonly used in high frequency devices and such devices have substantially developed technologies. Even though graphene shows superiority when it comes to thermal conductivity, saturation velocity and carrier mobility, the technology of graphene devices has yet to be optimised. MoS_2 is listed as a representative of transition metal dichalcogenides (TMDCs). Although it has a substantial bandgap, its high frequency performance is limited by its low carrier mobility [10].

Phosphorene is a phosphorus monolayer. Its properties are suitable for high frequency electronics and in addition, it has a bandgap that can be modulated by the number of its layers [6].

The high graphene carrier mobility of 200 000 cm^2/Vs has been reported in [19] in monolayer graphene suspended in vacuum. However, when graphene is placed on a substrate, its electrical characteristics significantly degrade and its carrier mobility can fall even below 10 000 cm^2/Vs. Such steep degradation of mobility is related to various substrate-induced scattering mechanisms such as ionised impurity scattering and surface phonon scattering [1].

1.2 Graphene FETs

FET stands for *field-effect transistor*, a family of transistors whose principle of work is based upon their gate electrode capacitatively controlling the density of carriers in the channel, an active region between the other two electrodes, namely, drain and source. In this way, the gate electrode controls the conductivity in the channel.

The members of the family of FETs are distinguished based on how this gate capacitor is formed. In a type of a FET considered in this thesis, the gate capacitor is formed as a junction of metal, oxide and semiconductor, therefore MOSFET. As has been shown before, graphene cannot be categorised as a semiconductor which is why MOSFETs with graphene as a channel material are named graphene FETs or GFETs. A simple schematics of a GFET with a top-gate electrode design that will be considered in this work is shown on figure 1.2.

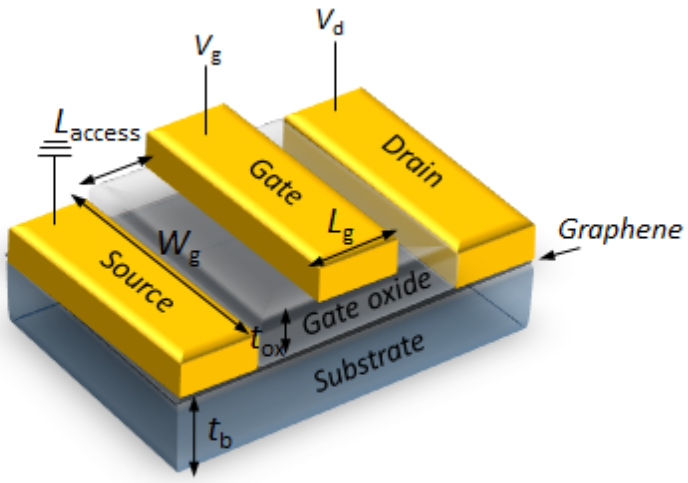


Figure 1.2: Schematic representation of a top-gate GFET crossection.

Current in a FET channel can be calculated from:

$$I_{ds} = \frac{qW_g}{L_g} \int_0^{L_g} n(x) v_{drift}(x) dx \tag{1.7}$$

where q is elementary charge, L_g length of the channel, W_g its width, $n(x)$ density of carriers distribution in the channel and v_{drift} the drift velocity. From this equation, it can be seen that the channel current is directly proportional to the drift velocity which can be calculated by:

$$v_{drift} = \frac{\mu E}{\sqrt[\gamma]{1 + \left(\frac{\mu E}{v_{sat}}\right)^{\gamma}}} \tag{1.8}$$

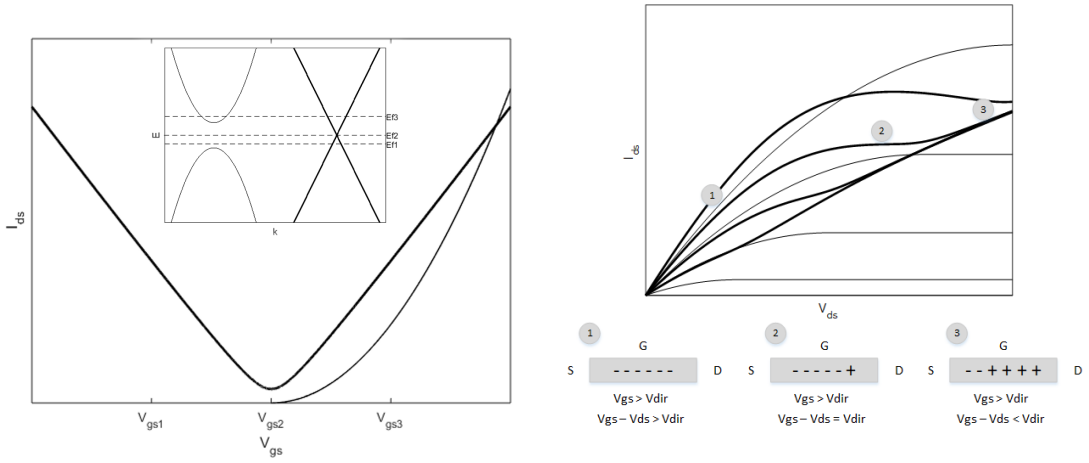
where E is an electric field between source and drain, μ channel material carrier mobility, v_{sat} velocity of saturation and γ is the fitting parameter. For low enough values of E this expression can be reduced to:

$$v_{drift} = \mu E \tag{1.9}$$

It is apparent that the influence of the velocity of saturation increases compared to the carrier mobility due to higher electric fields when scaling the gate length.

Transfer characteristics and dispersion relation comparison of a generic long gate n-type MOSFET and a GFET are shown on figure 1.3a. Applied gate voltages V_{gs1}, V_{gs2} and V_{gs3} correspond roughly to Fermi levels E_{f1}, E_{f2} and E_{f3} in the dispersion relation graph, respectively. A typical MOSFET stops conducting, or rather, *turns off* below a certain threshold voltage (in this case it would correspond to V_{gs2}). Voltages below the threshold voltage correspond to to Fermi energies inside the bandgap where the density of states is zero. In case of a GFET, because of the lack of bandgap, instead of turning off, it changes polarity and continues conducting. This phenomenon, the ability to conduct both holes and electrons is referred to as *ambipolarity*. The part of the dispersion relation around the Dirac point (touching point of graphene's bands) has very low density of states. This means that the density of carriers and thus the current, will drop when the Fermi level reaches that point.

A comparison of the output characteristics of a generic GFET and a MOSFET is shown on figure 1.3b. A standard MOSFET output characteristics can be described with two regions: linear and saturation region. Linear region is characterised by the steady current increase with the drain voltage, where the drain and source are connected by the conductive channel. After a certain bias point, the Fermi energy at the part of the channel closer to the drain reaches the bandgap and the channel is *pinched-off*. After this point, the current saturates, i.e. stops increasing with the drain voltage. When it comes to a GFET, current starts off with linear growth. However, when the Fermi energy at the channel reaches the Dirac point, there is a slight saturation, however, not due to the channel pinch-off but due to the carrier velocity saturation. This saturation has shown to be dependent of the amount of impurities in the channel, quality of graphene interfaces and temperature [3,34]. Due to ambipolarity, further increase in drain bias results in the change of the channel polarity, and the so called *second linear region*.



(a) **(b)**

Figure 1.3: Comparison of a generic long gate MOSFET (thin line) and GFET (bold line) transfer (a) and output (b) characteristics.

1.3 High frequency GFETs

In high frequency applications of highest importance is to assure that the fast signal change on the input will cause an equally fast change of the signal on the output of the system. In terms of FETs' parameters, a high frequency voltage on the gate should produce the same high frequency drain-source current. A parameter that is described by the change of the drain-source current in dependence on the change of gate voltage is called transconductance or g_m:

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=const.} \tag{1.10}$$

Since it is desirable that the output changes only with the change of input, at the working point it would be convenient that the output current doesn't change with the output voltage. A parameter that describes this relation is referred to as the output conductance or g_d:

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}=const.} \tag{1.11}$$

A two-port network small signal model of a generic GFET is shown on figure 1.4. C_{gs} and C_{gd} are gate-source and gate-drain capacitances, R_G, R_D and R_S are gate, drain and source resistances, respectively. r_{ds} represent the channel resistance. Figures of merit of high frequency transistors are the maximum oscillation frequency f_{max} and the cut-off frequency, f_T. f_{max} is defined as the frequency at which the unilateral gain (U) of the transistor is equal to 0 dB. f_T is defined as the frequency at which the current gain, h_{12} is equal to 0 dB. If we analyse a GFET as a four-port network, U and h_{12} can be calculated from its scattering parameters as follows:

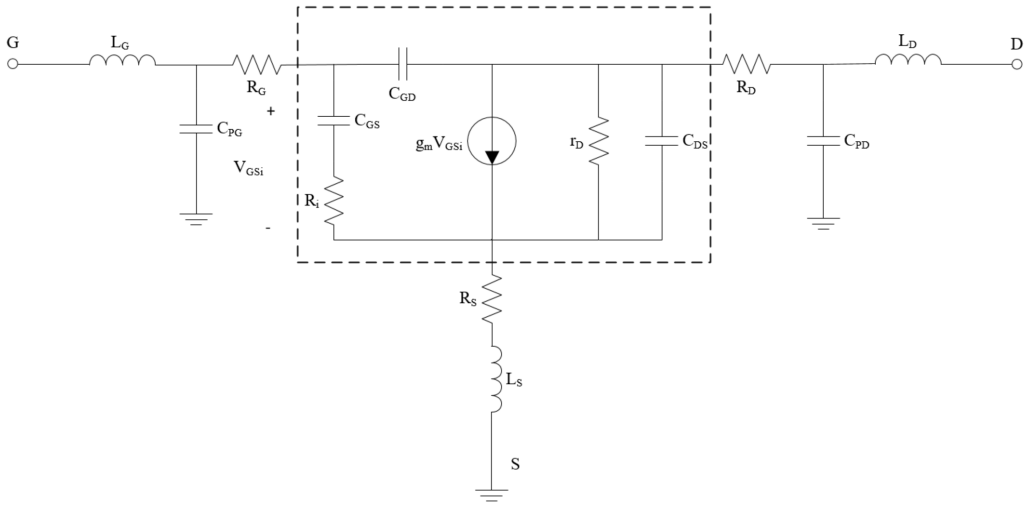


Figure 1.4: Schematics of a small signal two-port network model of GFET. The area inside the dashed rectangle represents the intrinsic parameters of the transistor.

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{1.12}$$

$$U = \frac{\left|S_{12} - S_{21}\right|^2}{\det\left[1 - SS^*\right]} \tag{1.13}$$

From the two-port network small signal model the expressions for f_{max} and f_T can be found in relation to the transistors' parameters:

$$f_{max} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}\Big(R_i + R_S + R_G\Big) + g_m R_G \frac{C_{gd}}{C_{gs}}}} \tag{1.14}$$

$$f_T = \frac{g_m}{2\pi\Big(C_{gs} + C_{gd}\Big)} \frac{1}{1 + g_{ds}\Big(R_S + R_D\Big) + \frac{C_{gd} g_m (R_S + R_D)}{C_{gs} + C_{gd}}} \tag{1.15}$$

In most applications in electronics, f_{max} plays a bigger role in the overall performance of a transistor. From the equations above, it can be seen that a the value of g_m plays a large role in the high frequency performance of a transistor while large g_d would degrade both f_T and f_{max}.

1.4 Flexible substrates

As shown in table 1.2 compared to table 1.1, polymer substrates, have a significantly lower thermal conductance compared to the commonly used semiconductor substrates. As a result, Joule heating due to the applied bias poses a significant

problem. In addition to that, polymer substrates have relatively low working temperatures, meaning that the substantial heating in biased devices could cause localised melting. This is particularly relevant for the devices biased for the amplifier mode of work. In table 1.2 is shown a comparison of relevant parameters of potential flexible substrate materials. Polyethylene terephthalate (PET) is a common, readily available and widely used polymer. Although flexible GFETs have successfully been fabricated on PET, its thermal properties are inferior to those of the other available polymer materials. Polyethylene naphthalate (PEN) is a polymer engineered to have slightly better properties than PET. However, polyimides (PI) still show the superior properties by comparison. Polyimide produced by the company DuPont and branded as Kapton has been commonly used as a substrate for flexible electronics [21]. Kapton has a rather high glass transition temperature (a temperature at which polymers start to melt) ranging from 300 to 400 °C depending on the measurements. This is why, in this work, Kapton has been chosen as a substrate. Surface roughness of Kapton has been measured by the scanning probe microscopy (SPM). The result of the measurement on a 5 μm×5 μm area a Kapton sample is shown on figure 1.5. The surface features don't go above 6 nm in this part, however, a large couple-of-hundred-nanometers feature can frequently be found on this sample.

Material	PET	PEN	PI
Glass transition temperature (°C)	81	155	360-410
Thermal conductivity (W/mK)	0.15-0.24	0.15	1-2
Young modulus (GPa)	2.8-3.1	6.1	2.5
Surface roughness (nm)	46-47	20	44

Table 1.2: Some of the relevant properties of the considered flexible substrates. Data extracted from [20–26].

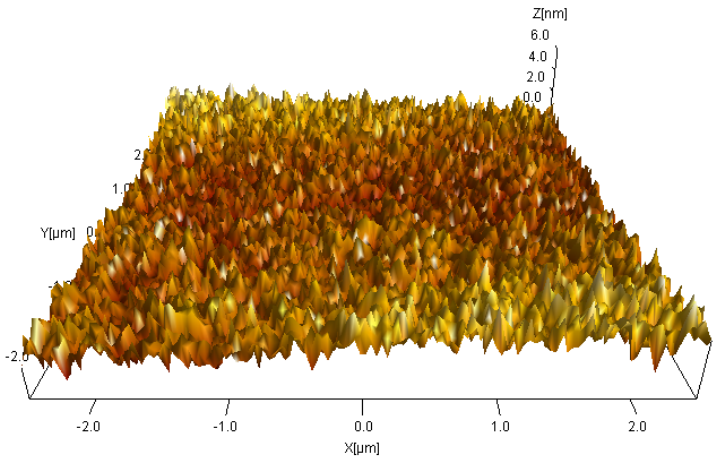


Figure 1.5: Scanning probe microscopy (SPM) image of a part of a Kapton sample.

2
Methods and results

2.1 Heating models

Joule heating or self-heating is one of the biggest challenges when it comes to the performance of microelectronic devices overall [35]. This is why a special attention should be paid to the its management during the device's design. Power MOSFETs are a type of transistors especially designed to withstand a high magnitude of bias power and in their design, Joule heating management is of the highest importance. This is why there has been a significant amount of research on heat modelling of this particular type of transistor.

A GFET operating at high fields required to reach a high f_{max} described in [29] has comparable power density in the channel as some of the power MOSFETs considered in [4] (roughly $1\,\mathrm{mW}/\mu\mathrm{m}$). The performance of a transistor is strongly dependent on the channel operating temperature. Analytical models of the heating have been represented in the publications by V. E. Dorgan et al. [3], H. F. Cooke [2] and two publications by M. Darwish et al. [4,5], the former for one-material substrate (used for Kapton substrate) and the latter for stacked two material substrate (used for Si/SiO_2 substrate). Modelled devices in these references are mostly power field-effect transistors that are used in high power applications and where the thermal management is necessary and the models have shown a good correspondence to the empirical measurements on such devices.

Generally, the rise of the channel temperature is directly proportional to the power dissipated (P_{diss}) in the channel (i.e. power of the Joule heating):

$$\Delta T = R_{th} P_{diss} \tag{2.1}$$

where R_{th} is thermal resistance, a parameter defined by both the type and geometry of the materials that compose the modelled structure. The above cited references model this parameter differently. In *Cooke model*, heating is quantified as the average rise of the temperature on the biased device's surface and it's based on the calculation of the thermal resistance of a multifinger structure by the analogy to the electrostatic capacitance of multiple, coupled transmission lines. In both of the *Darwish models* the maximum channel temperature is calculated based on the solution to the spacial Laplace temperature equation and the *Dorgan model* uses a simple thermal resistance expression following from the Fourier law of heat conduction. However, in all of the cited models, a multi-finger FET (a FET with multiple gate electrodes, a frequent design choice when it comes to power MOSFETs) has been modelled as shown on figure 2.1, with gate lines as localised heat sources. The

parameters taken into consideration are gate length L_g, gate width W_g, gate separation and the thickness of the substrate t_b and the effect of the gold contacts on top has been neglected.

Thermal resistance is proportional to $1/\kappa$ where κ is thermal conductivity, a parameter which is defined by the type of the material. Thermal conductivity is a parameter that changes with temperature. This dependence varies with the type of the material and usually needs to be determined empirically. However, the trend usually follows the equation

$$\kappa = aT^b [Wm^{-1}K^{-1}] \tag{2.2}$$

where T is the temperature and a and b are the fitting parameters. For Kapton, these parameters have been determined in [22], 5.24×10^{-3} and 1.02 for a and b respectively. It is important to note that these measurements have been conducted only for the temperatures from 5 to 300K. Given values suggest a rising trend of the value of thermal conductivity. Above the room temperature, thermal conductivity usually decreases with temperature [36] which is why it this expression probably cannot be generalised to the temperatures above 300K. In this work, for the simplicity's sake, the thermal conductivity will be assumed to be constant, however, it's temperature dependence will not be disregarded.

The estimation of the channel temperature according to the cited models with regards to the different parameters is plotted on the figure 2.2 for a Kapton substrate and compared to the biased GFET on Kapton channel temperatures measured by infrared microscopy in [37] and figure 2.3 for Si/SiO_2 substrate. It is apparent that there is a discrepancy between the different models. The IR measurements seem to correlate with the *Cooke* model if assumed that the thermal conductivity equals 2 which can be calculated from the parameters given in [22] however, according to the Kapton datasheet [21], this value might be an overestimation making the true temperature of the device even higher.

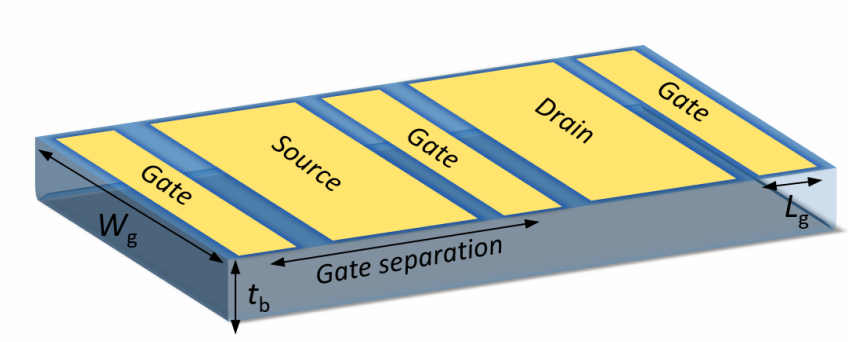


Figure 2.1: Schematic representation of the way the devices have been modelled in the considered publications, with gate lines as localised heat sources. The parameters taken into consideration are gate length L_g, gate width W_g, gate separation and the thickness of the substrate t_b.

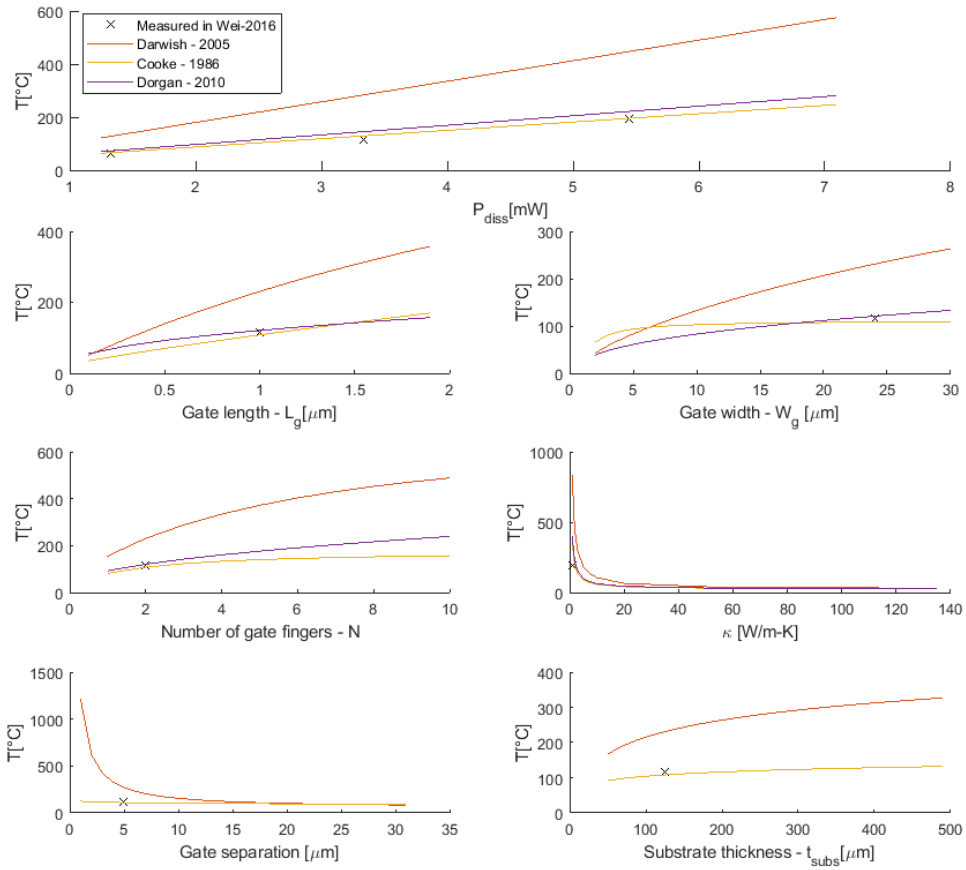


Figure 2.2: Plotted temperature estimation from the models [2–4] on a Kapton substrate with regards to different transistor parameters. If not changing in the graph the parameters are $L_g = 1\,\mu$m, $W_g = 24\,\mu$m, gate separation $= 5\,\mu$m, $t_{substrate} = 125\,\mu$m, $\kappa = 2$.

2.2 Design

In order to investigate these models experimentally, a couple of different layouts have been designed. A typically used two-finger design GFET design is represented on figure 2.4b. In order to investigate the applicability of the models, transistors with varying gate width, length, separation and gate finger number have been designed an fabricated. A slight different type of a transistor design is shown on figure 2.4a. Its gates are positioned in a way that would prevent the gates from heating each other. Scanning electron microscopy (SEM) photo of a transistor without the pads is shown on figure 2.4c together with the schematics of a cross section of a GFET design used in this work. A simple top-gate design is used and fabricated on a 125 μm thick Kapton substrate.

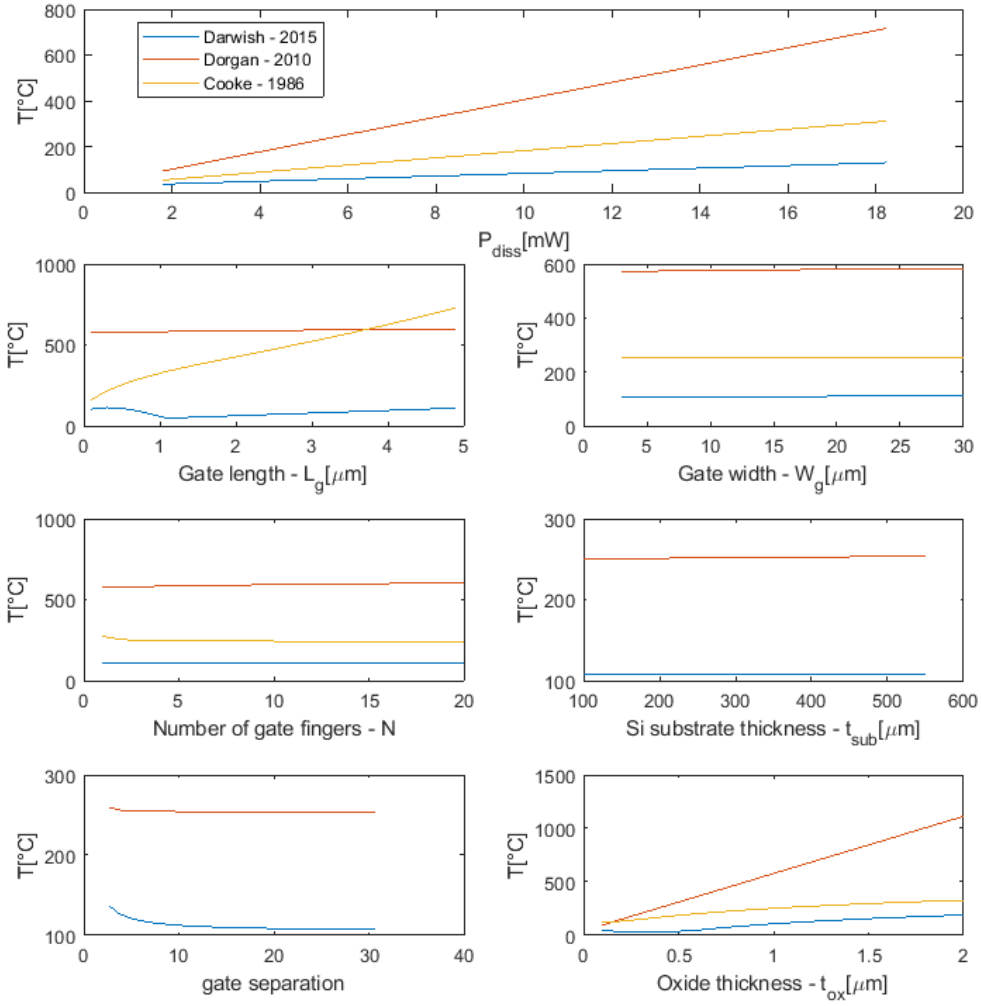


Figure 2.3: Plotted temperature estimation from the models [2,3,5] for a GFET on a Si/SiO_2 substrate with regards to different transistor parameters. If not changing in the graph the parameters are $L_g = 1\,\mu m$, $W_g = 15\,\mu m$, gate separation $= 20\,\mu m$, $t_{substrate} = 550\,\mu m$, $t_{ox} = 1\,\mu m$, $\kappa_{ox} = 1.4$, $\kappa_{Si} = 150$.

2.3 Fabrication

2.3.1 Fabrication recipe

The fabrication recipe was adapted from the previously developed GFETs on Si/SiO_2 substrate reported in Bonmann et al. [29]. The reported devices showed an excellent high-frequency performance which is in part accounted to very low contact resistance and to the addition of a protective oxide layer on top of graphene prior to the graphene mesa formation which keeps the channel protected during the processing. In this work, that recipe was adapted for the fabrication on a polymer

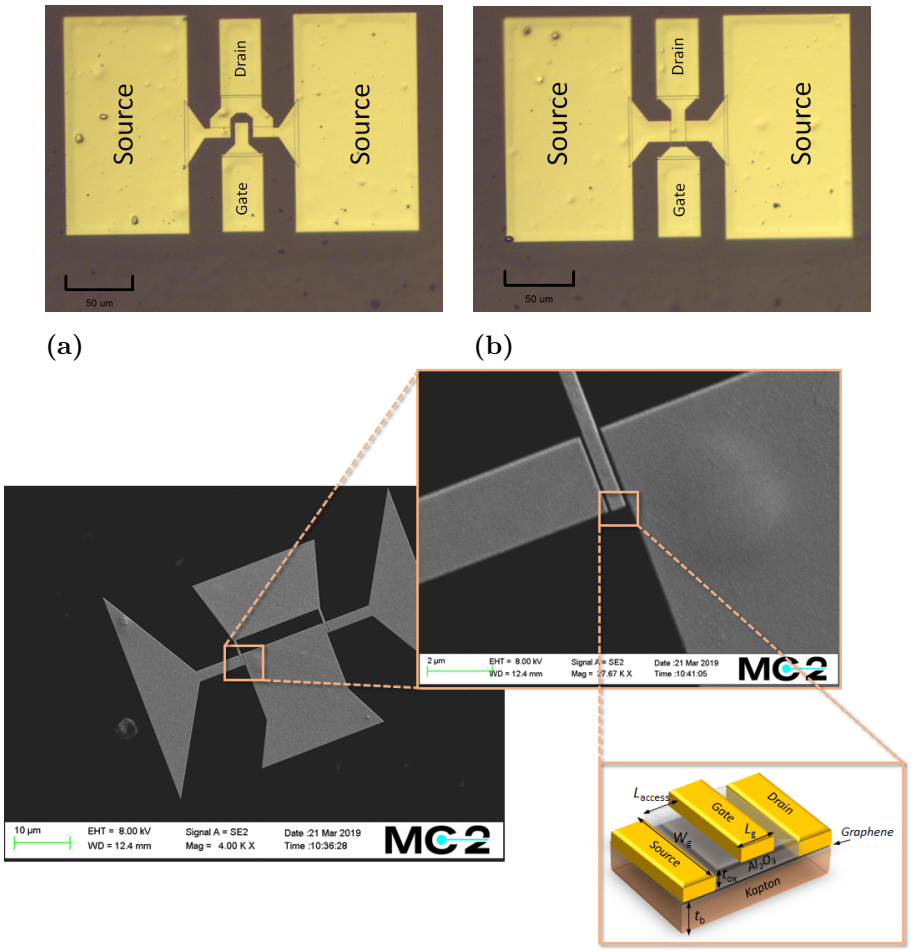


Figure 2.4: Microphotos of the fabricated devices with two different designs (a), (b). SEM photo of a fabricated GFET without contact pads and schematics of its cross-section.

substrate. Two fabrication flows used in fabrication of the samples considered in this work are depicted on the figure 2.5, one containing the protective oxide step and the other that doesn't. The flows go as follows:

1. **Graphene transfer to the substrate**
   A (chemical vapour deposition) CVD grown graphene was manufactured and transferred to a Kapton substrate by Graphenea.
2. **Protective oxide layer**
   The oxide protective layer is formed on the graphene by evaporating 10 Å of aluminium that is subsequently thermally oxidised by baking in the convection oven at 160 °C for 5 minutes. This process is repeated 4 times, resulting in a oxide thickness of 5.6 nm.
3. **Mesa formation**
   The patterns for the mesas are defined by the electron beam lithography (EBL). If it has been previously formed, the aluminium oxide is etched by the solution BOE:water 1:10. Subsequently, the graphene outside the defined

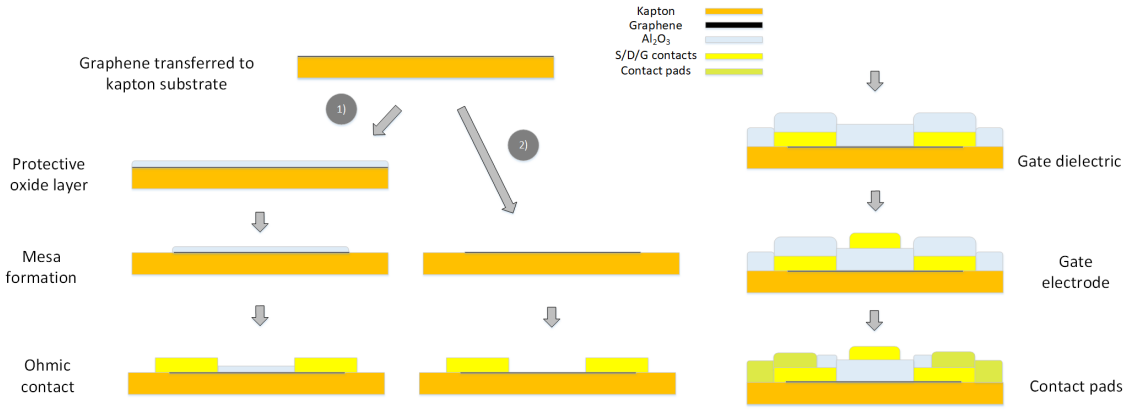


Figure 2.5: Schematic representation of the fabrication flows.

mesa pattern is removed by RIE[1].

4. **Ohmic contacts**
   Ohmic contacts are formed between the source and drain contacts and graphene after the protective layer of oxide has been removed in the areas patterned by the EBL by evaporating sequentially Ti/Pd/Au 10Å/150Å/2500Å and performing lift-off.
5. **Gate oxide**
   The gate oxide is formed by repeating the following process 7 times if the protective oxide layer has been done or 11 times otherwise: evaporating 10 Å of aluminium that is subsequently thermally oxidised by baking in the convection oven at 160 °C for 5 minutes. The resulting oxide layer (including the protective layer) should be ∼15.4nm thick.
6. **Gate electrodes**
   The gate electrodes ave been patterned by the EBL and have been formed by evaporating sequentially Ti/Au 100Å/2900Å and performing lift-off.
7. **Contact pads**
   In order to make the on-chip probe measurements more convenient, contact pads have been formed for gate, drain and source contacts by depositing Ti/Au 100Å/2900Å.

2.3.2 Obstacles during the fabrication process

Working with a flexible substrate in a process environment adapted to rigid substrates turned out to be not trivial. The sample chips fabricated in this work had a very low yield (⩽10%). This can be accounted to a number of reasons.

- Misalignment
  Keeping the flexible substrate as close as possible to perfectly flat during the electron beam exposure process is one of the most crucial things in the this fabrication process. However, if the flexible substrate is not formed by spinning the polymer on top of the rigid substrate and if the substrate has a significantly high Young modulus (meaning: it's quite flexible), misalignment can cause a

[1]RIE - reactive ion etching, BOE - buffered oxide etch

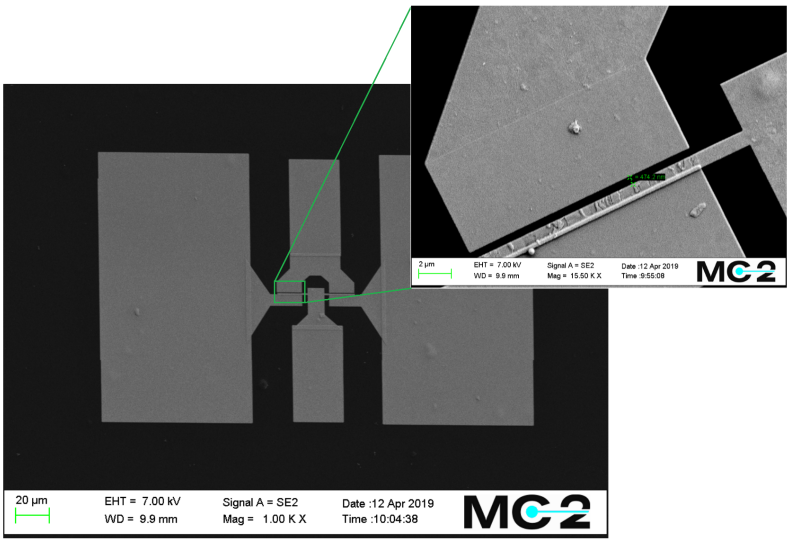


Figure 2.6: SEM photo of a GFET with a misaligned gate electrode

problem if the device design contains small features, in this case, the access length (the separation between the gate electrode and source/drain contacts) was set to 100nm. Usually, during processing, the flexible substrates are bonded to a rigid substrate (i.e. silicon wafer). Due to the lack of knowledge of the bonding method that would keep the substrate sufficiently flat, stay stable during the whole fabrication process and ensure an easy detachment at the end, a metal frame was used instead. A typical misalignment of the gate electrode is represented on figure 2.6. Usually, it is misplaced by up to 500nm. The solution for this would be to increase the access length a couple of hundreds of nanometers to ensure that the gate electrode stays at least within the channel area. This will, in turn, increase the non-gated channel area, which will increase the overall channel resistance.

- Overexposure
  Overexposure can be identified as local or general widening of the developed pattern compared to the original. It a consequence of the proximity effect in e-beam litoghraphy, an effect caused by electron scattering because of which the exposure dose distribution is wider than the scanned pattern. This effect is taken into account when generating the pattern files for e-beam exposure in a way that the sharp edges and very small features get lower exposure dose. However, if the initially assigned exposure dose is too high, even this compensation will not help. One indicator of overexposure is shown on figure 2.7. The gate with the length of 0.5μm is a relatively small feature compared to the rest of the gate electrode. The exposure dose was clearly too high which caused widening of the gate at one segment. A transistor containing this defect will presumably result in short circuited gate. Proximity effect is a consequence of the interaction of the primary electron beam with both the substrate and the resist therefore, the exposure dose should be defined for every EBL processing step.
- Scattered graphene mesas

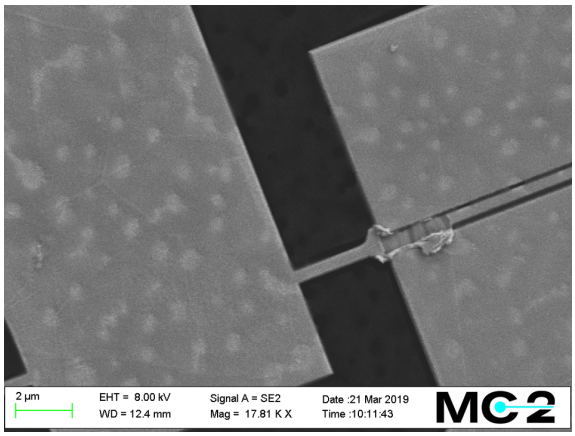


Figure 2.7: SEM photo of a GFET gate overexposure consequence

While a very high contact resistance can be explained by the incomplete oxide etching, frequently, the drain-source resistance is so high that the GFET seems to be open. This might be caused by the scattering of the graphene mesas that has been observed after drying the sample with meas with a nitrogen gun which has been observed before. Taking into account the fact that graphene binds to the substrate only by the weak Van der Waals forces, delamination during processing is probable.

2.4 Thermal imaging

Thermal imaging is frequently used when there's a need to investigate the heating and heat distribution in a biased electronic device. In microelectronics, thermal imaging is usually performed using infrared microscopy. Infrared microscope contains a light detector specially designed to detect photons from the infrared part of the spectrum that would be emitted by the device heated by Joule heating, typically around the mid-infrared range, 3-8 μm, which would correspond to the blackbody temperatures 362 - 966K.

In this case, thermal imaging of transistors under bias was performed using QFI InfraScope III with response band range from 2 to 4 μm. The transistors were biased using dual-channel Keithley Source Meter 2604B. The results of imaging are shown on the figure 2.8 and figure 2.9 for a GFET on a Kapton and Si/SiO_2 substrate respectively. Reference imags, i.e. images of an unbiased transistor that is used in order to compensate for the different material emissivities are shown on figure 2.8a and figure 2.10b. Polished gold has a significantly low whereas Kapton has substantially high emissivity. SiO_2 is transparent to the infrared radiation so the photons from that area come from the Si layer below. The increase of temperature due to the rise of the applied drain voltage is shown on figure 2.8b-e and figure 2.9b-e.

On figure 2.10a and figure 2.10b compared are the maximum temperatures measured in the thermal images and the temperature estimations based on the models discussed in section 2.1. The results are plotted with regards to the intrinsic power density in the channel instead of the drain voltage in order for the graphs

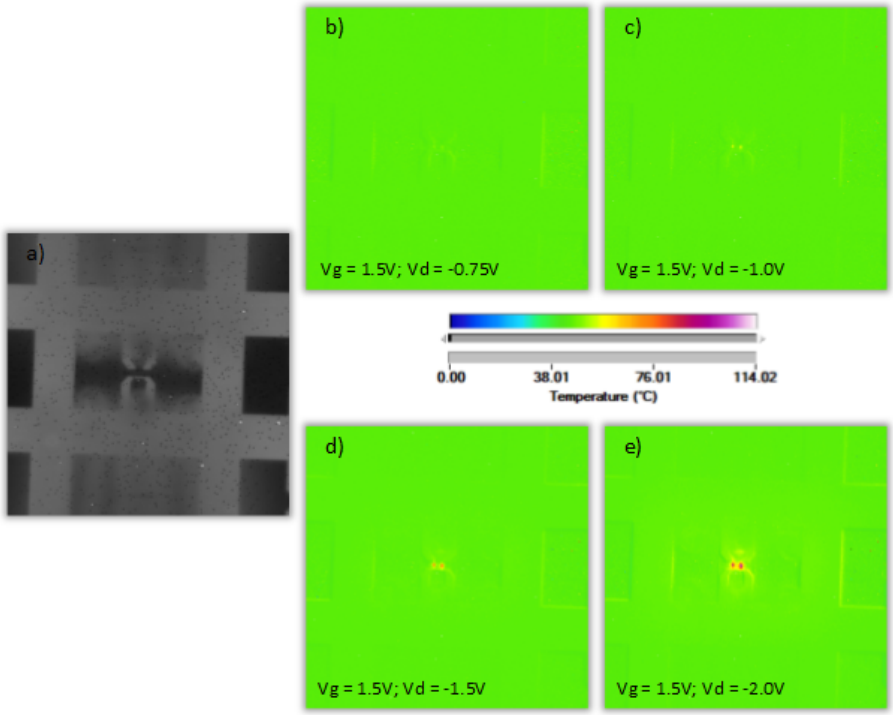


Figure 2.8: Infrared images of a GFET on Kapton substrate with $W_g = 2 \times 15\mu$m and $L_g = 0.5\mu$m under different bias conditions.

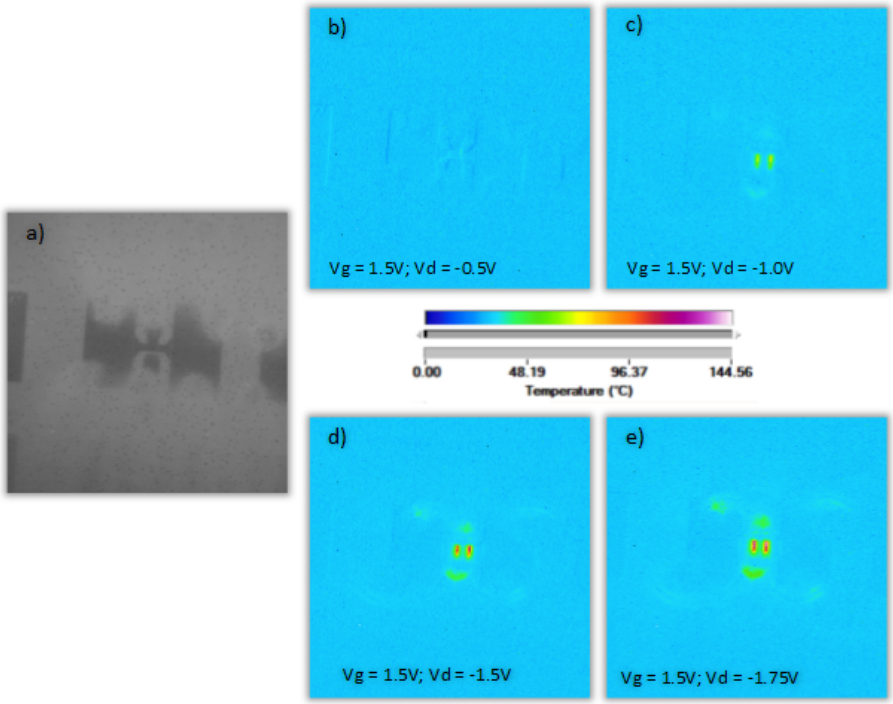
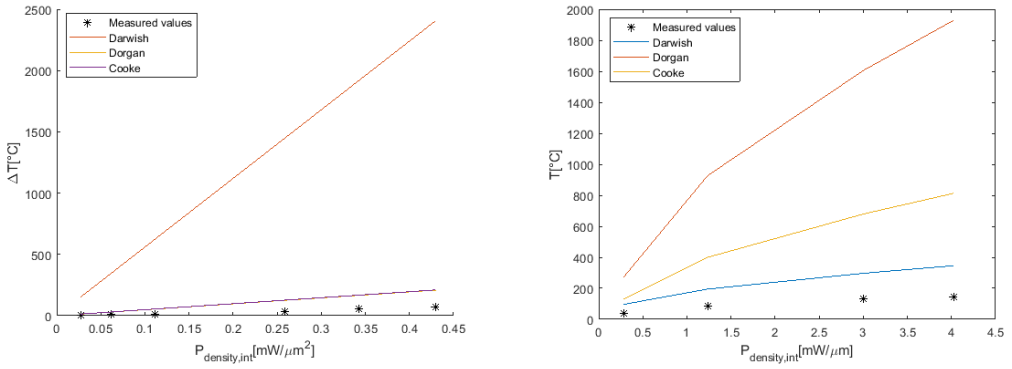


Figure 2.9: Infrared images of a GFET on SiO_2/Si substrate with $W_g = 2 \times 15\mu$m and $L_g = 0.5\mu$m under different bias conditions.

to be more easily comparable with the GFETs with different gate area and contact resistance (the voltage inside the channel is calculated by $V_{int} = V_d - R_C I_d$). Clearly, there is a discrepancy between the results. Due to the relatively long wavelengths of the photons in the response range, the diffraction limit of the microscope may be the factor that causes the underestimated temperature values. Even using the maximum available magnification on this microscope – x15, a pixel in the acquired thermal image has the resolution of 1.5 μm [38]. Furthermore, the heated areas are mainly covered with gold and its very low emissivity might have caused the inaccurate measurements [39].



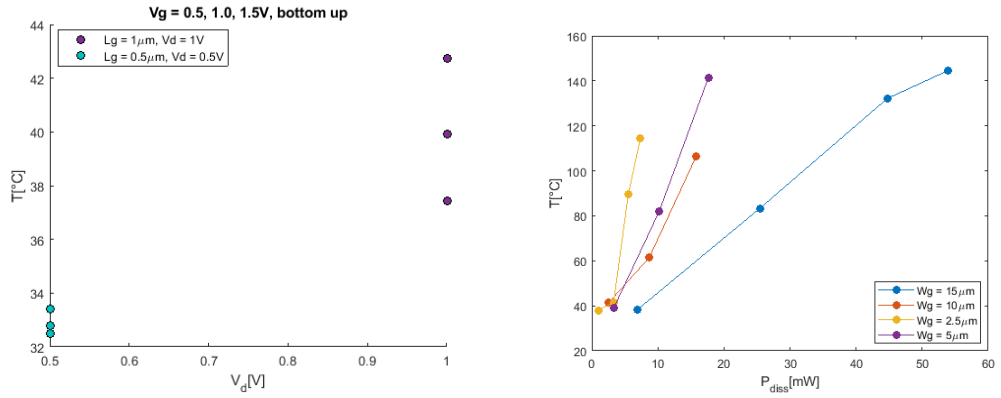
(a) **(b)**

Figure 2.10: Comparison of the maximum temperatures measured by IR microscopy with some of the heating models.

Even though the absolute values of the temperatures measured via thermal imaging are questionable, the relative values can be discussed. A comparison of the measured temperatures for the GFETs on Si/SiO_2 substrate with different gate lengths and widths is shown on 2.11a and 2.11b. Clearly, for the same field, the heating is reduced in the transistors with smaller gate length which is convenient since scaling down the gate length increases the high-frequency performance as well. Heating also seems to be decreasing for the transistors with larger gate widths. The reduction in heating may not be much when considering the devices worikng at room temperatures, however, it might be useful for devices working in cryogenic conditions.

2.5 External heating effects on GFET characteristics

In this section the change of the GFET characteristics due to external heating will be discussed. On figure 2.12 presented are the transfer and output characteristics of a GFET on a Si/SiO_2 substrate. The measurements are performed by biasing the transistor using dual-channel Keithley Source Meter 2604B and the external heating has been applied by heating of the sample holder (chuck) and regulated by Temptronic ThermoChuck. The temperature of the externally applied heating is



(a) **(b)**

Figure 2.11: Comparison of the temperatures for devices with different gate widths and lengths.

designated with T_0. Clearly, the output resistance changes with heating, because of which the drain current drops. The gate leakage current increases due to the applied voltage on the gate but also due to the heating.

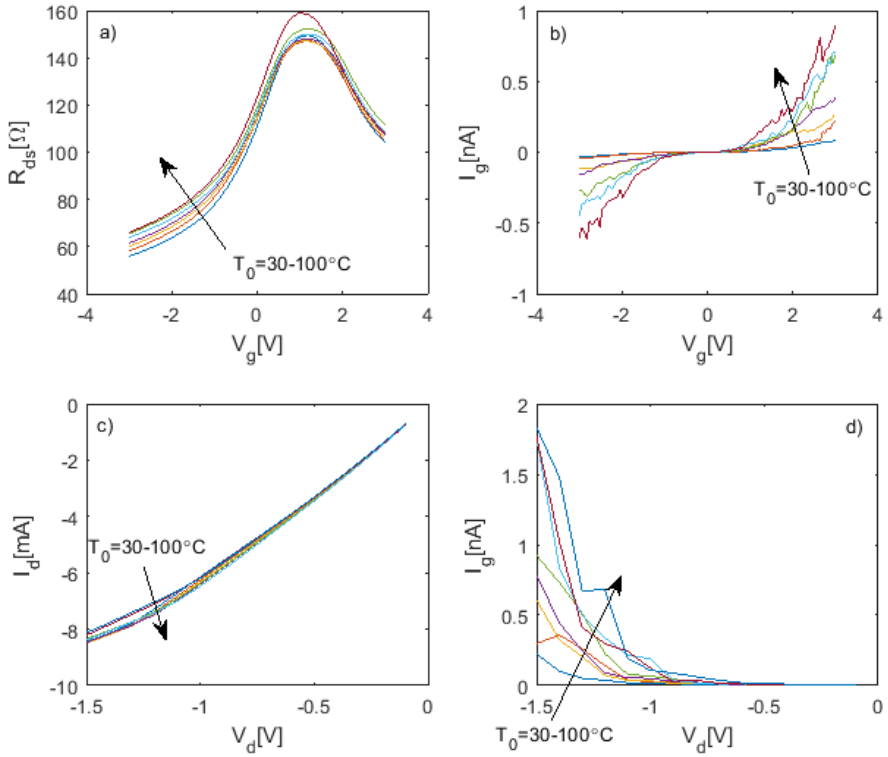


Figure 2.12: External heating effects on GFET transfer (a), output (c) characteristics as well as on the gate leakage current in both cases – (b), (d).

2.6 Thermosensitive electric parameters

Due to the limitations of the infrared microscopy, other methods for determining the channel temperature had to be used to resolve the discrepancy between the thermal imaging measurements and models. A number of thermosensitive electric parameters (TSEPs) have been compared in [40]. Using TSEPs, the biased device itself functions as a temperature sensor. In this work, gate leakage current (I_g) and drain current (I_d) have been measured and analysed as TSEPs.

As discussed before, the rise of temperature in a transistor channel can be modelled by the equation (2.1) from which follows that ΔT is directly proportional to the applied bias power. The proportionality factor in this case is the thermal resistance which is an unknown. However, if the change of I_g or I_d due to heating and due to the applied bias power is known, the thermal resistance can be determined by:

$$R_{th} = \frac{\Delta I_g}{\Delta P_{diss}} \frac{\Delta T}{\Delta I_g} = \frac{\Delta I_d}{\Delta P_{diss}} \frac{\Delta T}{\Delta I_d} \tag{2.3}$$

where, T is the (unknown) maximum temperature in the transistor channel and T_0 is the (known) temperature of the externally applied heating:

$$T = T_0 + \Delta T = T_0 + R_{th} \Delta P_{diss} \tag{2.4}$$

In order to find the thermal resistance, I_g and I_d have been measured as TSEPs on one of the fabricated GFETs. The external heating has been applied by heating of the sample holder (chuck), and regulated by Temptronic ThermoChuck. The temperature has been swept from 25°C to 80°C. The transistor has been biased by Keithley Source Meter 2425. The transistor dimensions are $L_g = 0.5\mu m$, $W_g = 2 \times 15\mu m$ and the gate fingers separation is 25μm. The results of measurements and the calculated differentials are shown on figure 2.14 and figure 2.13. It is clearly visible that the both I_g and I_d change with changing both externally applied heating and self-heating due to the increasing bias power and thus can serve their purpose in estimating the temperature as TSEPs.

Gate leakage current shows an exponential increase due to both applied bias voltage and heating. It is mostly determined by the gate resistance which is determined by the gate oxide and its temperature dependence is well studied, while the drain current depends more on the nature of the graphene channel and it might vary due to trapping and de-trapping mechanisms. However, in GFETs, the gate leakage current is also affected by the oxide-graphene interface states.

The final result of the equation (2.3) is shown on the figure 2.15a for a GFET on Kapton substrate. The values of thermal resistance extracted from the drain current converge roughly to 9.9×10^4K/W, whereas the mean of the values for R_{th} extracted from the gate leakage current, corresponding to the highest V_d (the current change due to heating is the highest at this point) is close to 6.7×10^4K/W. The R_{th} values vary for different externally applied heating because the thermal conductivity κ changes with temperatuere. The same measurement has been done on a GFET on Si/SiO_2 substrate and the result is shown in the figure 2.15b. The R_{th} converges to the values that equal roughly 1.7×10^4K/W in case of I_g measurements and

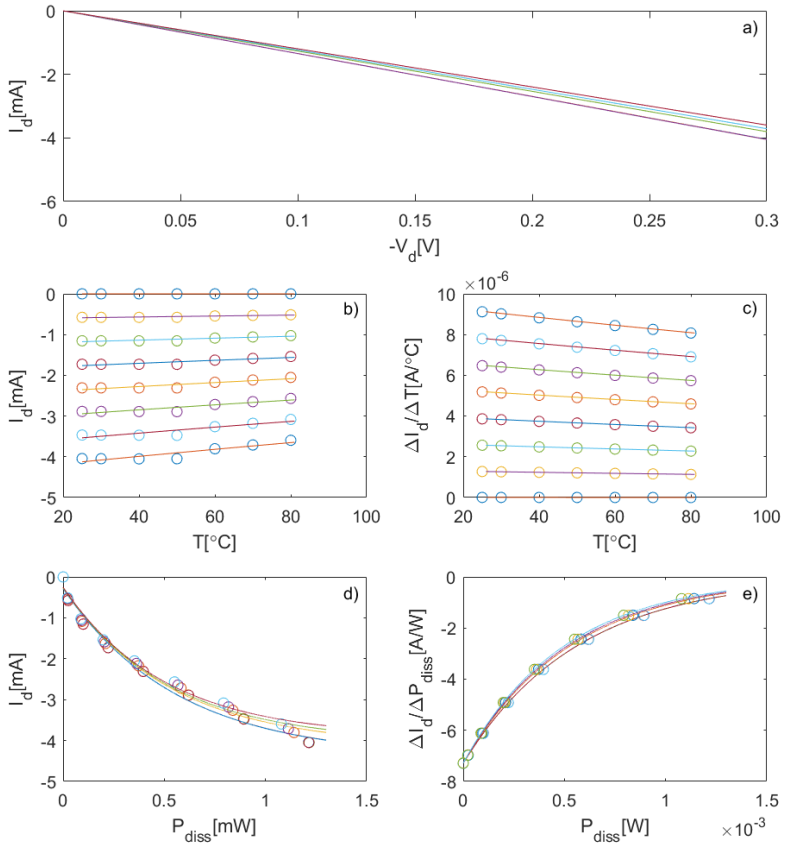


Figure 2.13: Measured output characteristics of a GFET on Kapton with varying externally applied heating $T_0 = 25{,}30{,}40{,}50{,}60{,}70{,}80\,°C$ (a). Dependence of the drain current to the externally applied heat (b) and applied bias power (d). Differentials extracted from the measurements: (c) $\Delta I_d/\Delta T$ and (e) $\Delta I_d/\Delta P_{diss}$.

3.1×10^4K/W in case of I_d measurements. In table 2.1 compared are the R_{th} values extracted via the TSEP method with the models discussed before. Even though the results all fall within the same order of magnitude, the small discrepancy between the values would still cause a significant difference in the calculated temperature, i.e. for the discrepancy of 1.2 $\times 10^4$ K/W (like between values extracted from I_g and I_d measurements) for applied bias power of 1 mW, the resulting difference in the rise of temperature would be 12 °C which could not account for a very precise temperature estimation. However, if we would take the R_{th} values extracted from I_g more accountable because the leakage current is mostly determined by the oxide and thus more stable, according to the table 2.1 *Darwish-2015 model* approximates well the thermal resistance in GFET on Si/SiO_2, while the *Dorgan model* works better for the Kapton substrate.

The temperature estimation for heating of a GFET on Kapton is plotted on figure 2.16. The full line represents the temperature estimation modelled in the *Dorgan model* while the squares represent the temperature estimated from the I_g measurements. While the agreement is pretty good, the amount of heating due to

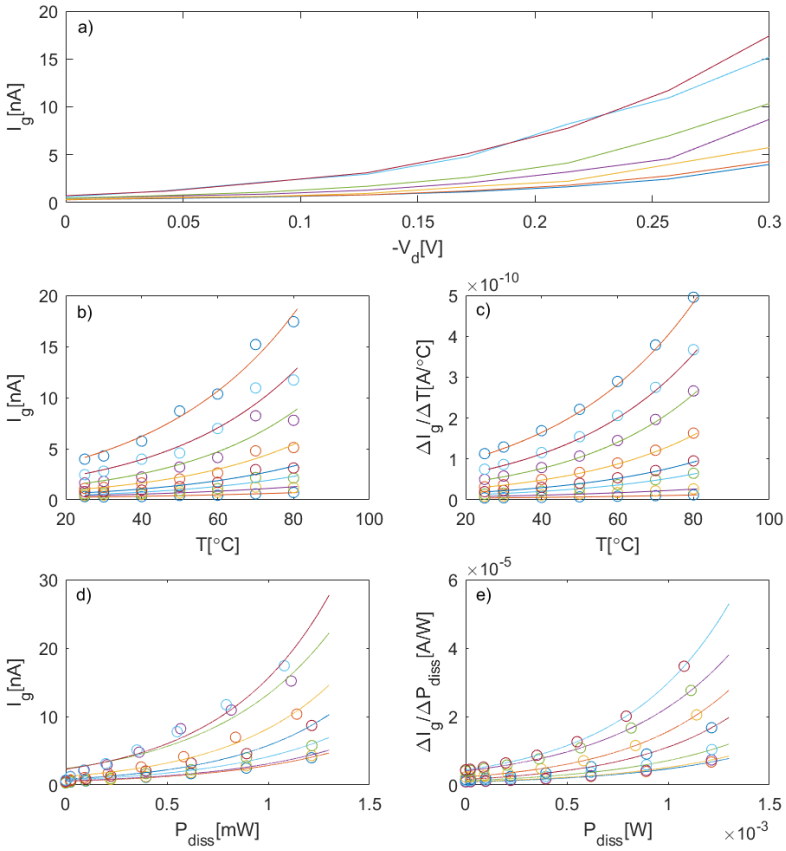
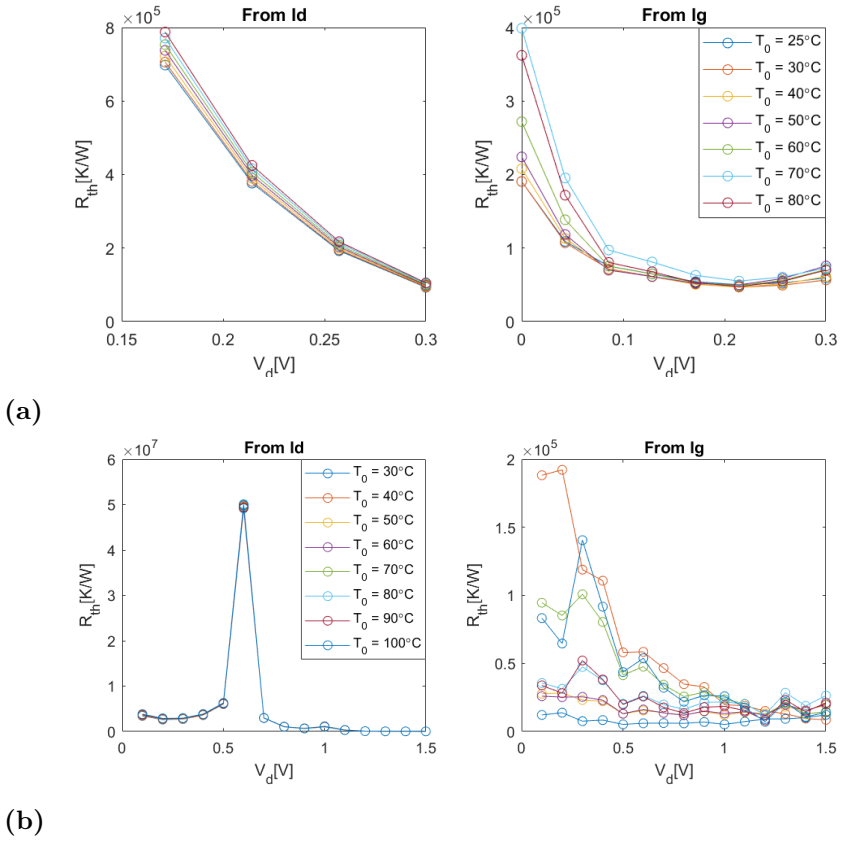


Figure 2.14: Gate leakage current measurements with respect to the applied drain voltage and externally applied heating T_0 = 25,30,40,50,60,70,80 °C (a). (b), (d) dependence of the gate leakage current to the externally applied heat and applied bias power, respectively. (c), (e) $\Delta I_g/\Delta T$ and $\Delta I_g/\Delta P_{diss}$ differentials extracted from the measurements.

the bias applied on the actual channel and not on the contacts (P_{int}) suggests that the heating is not localised as it should be in an ideal case.

Substrate	from I_g	from I_d	Darwish-2015/2005	Dorgan-2012	Cooke-1986
Si/SiO_2	1.7	3.1	1.67	7.01	3.18
Kapton	6.7	9.9	3.56	6.46	4.62

Table 2.1: Comparison of thermal resistance (R_{th}) values expressed in $\times 10^4$ K/W extracted from I_g and I_d measurements and three different models.



(a)

(b)

Figure 2.15: Thermal resistance extracted from gate leakage current and drain current for a GFET on Kapton (a) and on Si/SiO_2 substrate (b).

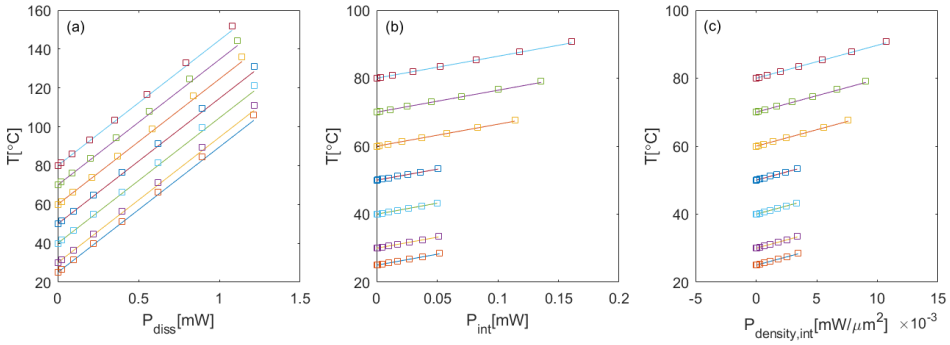
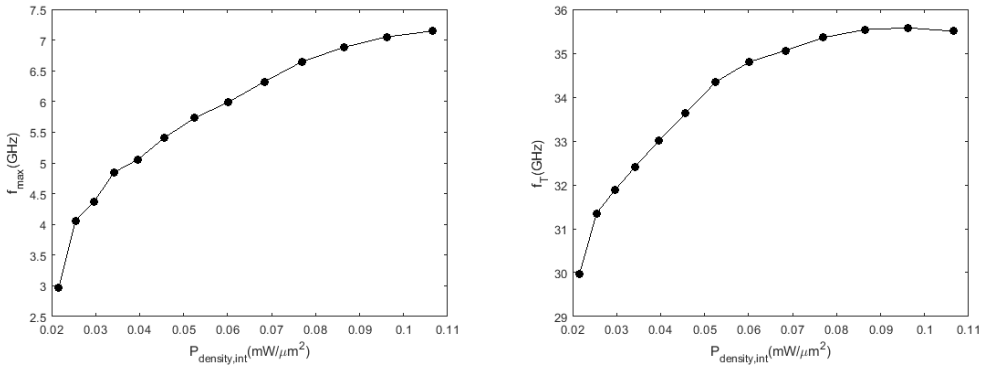


Figure 2.16: Temperature estimation of the channel heating due to the applied bias and external heating. The full line represents the temperature estimation modelled in the *Dorgan model* while the squares represent the temperature estimated from the I_g measurements. (a) shows the estimation versus the applied bias power while (b) shows the bias power applied internally, $P_{int} = (V_d - R_C I_d) I_d$ where R_C is the contact resistance which in this case equals 70 Ω. (c) shows the estimated temperature versus internally applied power density ($P_{density,int} = P_{int}/(L_g W_g)$).

2.7 High-frequency performance

Despite all of the fabrication and performance issues, some of the measured transistors reached the values of f_{max} and f_T of a couple of gigahertz. These tran-

sistors also showed to have the lowest contact resistance (around 80 Ω for W_g = 25 μm). The measurements of f_{max} and f_T of the best performing measured GFET on Kapton are shown on figure 2.17. When considering a figure of merit used to compare the high frequency performance of transistors with different gate lengths – $f_{max} \cdot L_g$, the measured transistor reaches 3.5 GHz·μm. This value is comparable to the current state-of-the-art for the GFETs on flexible substrate which is reported to be 8.4 GHz·μm [41].



(a) **(b)**

Figure 2.17: Measured f_{max} and f_T for the best preforming transistor measured.

2.8 Heating effects on high-frequency performance

In this section, the effects of heating on the high-frequency parameters and performance of a GFET on Kapton are investigated. The results of this analysis for the GFETs on Si/SiO_2 substrate are reported in [42]. On figure 2.18 plotted are the results of the f_{max} and f_T measurements with respect to applied bias power density and external heating. In the case of f_{max}, the detrimental effects of the external heating are clearly visible however, the measurements of f_T are not consistent in this regard.

On figure 2.19 plotted are some of the parameters relevant to the high-frequency performance. g_d and g_m are extracted from the measurements while the self-heating temperature is calculated from the *Dorgan model* which has shown a good agreement with the measurements in the previous section and shown on the figure 2.19c. The temperature dependent carrier mobility μ and saturation velocity v_{sat} have been calculated from the following expressions [3]:

$$\mu(n,T) = \frac{\mu_0}{1+(n/n_{ref})^{\alpha}} \frac{1}{1+(T/T_{ref}-1)^{\beta}} \tag{2.5}$$

$$v_{sat}(n,T) = \frac{2}{\pi}\frac{\omega_{OP}}{\sqrt{\pi n}}\sqrt{1-\frac{\omega_{OP}^2}{4\pi n v_F^2}}\frac{1}{N_{OP}+1} \tag{2.6}$$

where $N_{OP} = 1/[1-\exp \hbar\omega_{OP}/k_BT]$ and ω_{OP} are the the optical phonon occupation energy and frequency. Fermi velocity, $v_F = 8.5 \times 10^5$ m/s, $n_{ref} = 10^{17}$ m^{-2}, T_{ref} =

300 K. Due to the lack of knowledge of the optical phonon energy in polymers, the value for graphene has been used and equals $\hbar\omega_{OP} \approx 160$eV, which might be an overestimation. The heating effect on the charge carrier concentration n has shown to be negligible compared to the shift of the Fermi energy, i. e. self-gating as shown on both figure 2.19f where n has been extracted from the measurements and in figure 2.19i where n is calculated using the equation (1.5) for relevant temperatures.

Both figure 2.19 and figure 2.18 show a some detrimental effect of external and self-heating to the high-frequency parameters. However, due to the very high contact resistance of the considered GFET (230 Ω), not enough bias voltage could have been applied to the channel itself (most of the voltage drop would be on the contacts) which didn't produce a current high enough to heat the device substantially and show the true self-heating effects as are presented in the GFETs on Si/SiO_2 substrate in [42].

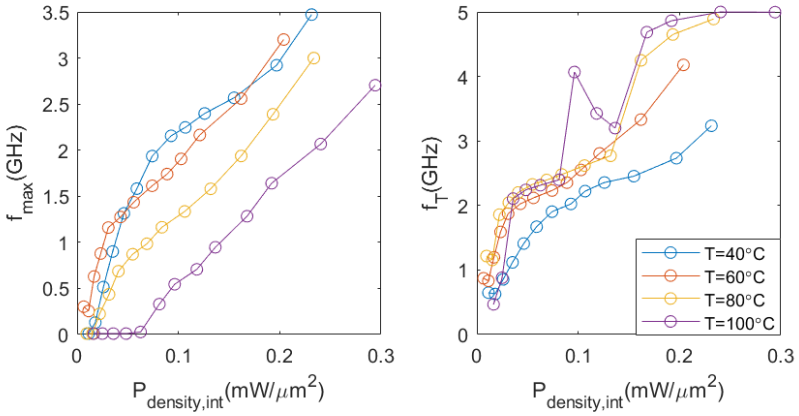


Figure 2.18: Measured dependence of f_T and f_{max} on applied bias power density and externally applied heating.

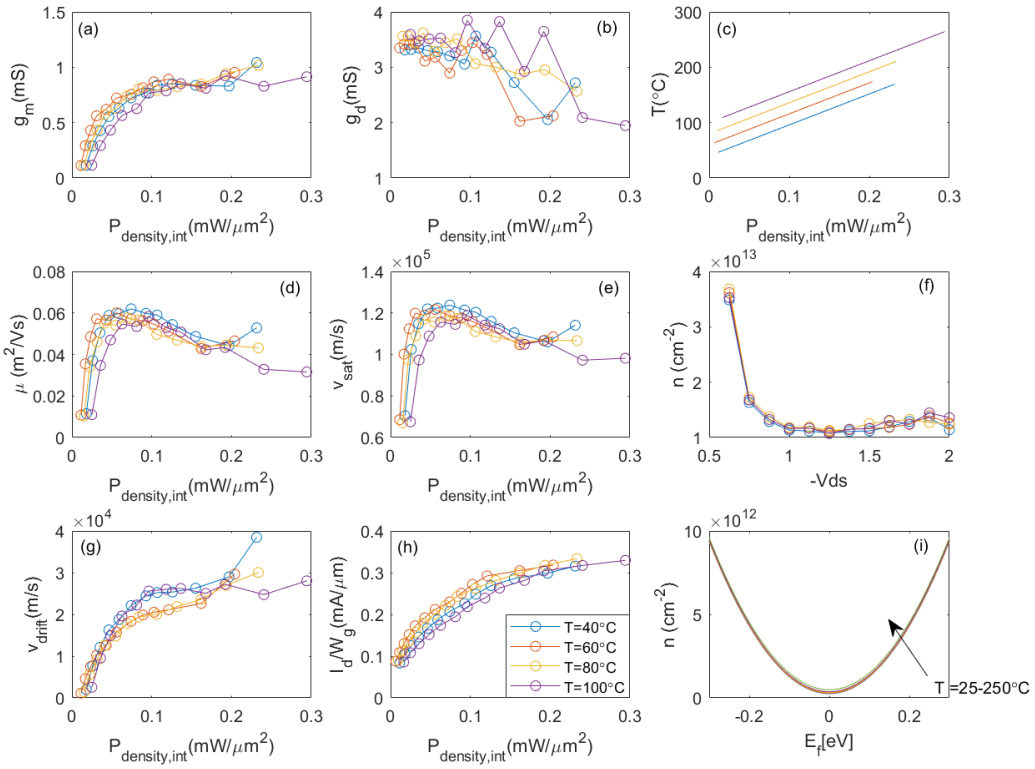


Figure 2.19: Relevant high-frequency parameters extracted from the measurements and their dependence to the applied external heating (designated by T on the legend in (h)) and self-heating (a),(b),(d)-(h). The temperature of the applied external heating and estimated self-heating is represented on (c). (i) the change in n calculated for the shift in E_f and relevant temperatures.

3
Conclusion

Graphene is a promising material when it comes to the high frequency flexible electronics applications. However, there are still a number obstacles to be solved in order for it to reach its full potential and developed technology.

Alongside the common problems of a lack of high quality large graphene sheets and contact resistance, flexible substrates bring with them additional complications in fabrication process and in device's performance via heating due to the applied bias power, i.e. self-heating. Effects of self-heating in GFETs on flexible substrates are crucial to understand but insufficiently addressed. Despite the analysis provided in this work of some of the potential models for heating in GFETs, more investigation on this topic is needed in order to determine a good analytical model of the true temperature in a GFET channel.

Proper understanding and modelling of the heating effects are important for optimisation of these devices. Although minor optimisations with regards to the thermal efficiency of GFETs can be achieved by the design adjustments, in order to enable further development of biased graphene-based flexible electronics, high thermal conductivity flexible substrates are required.

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