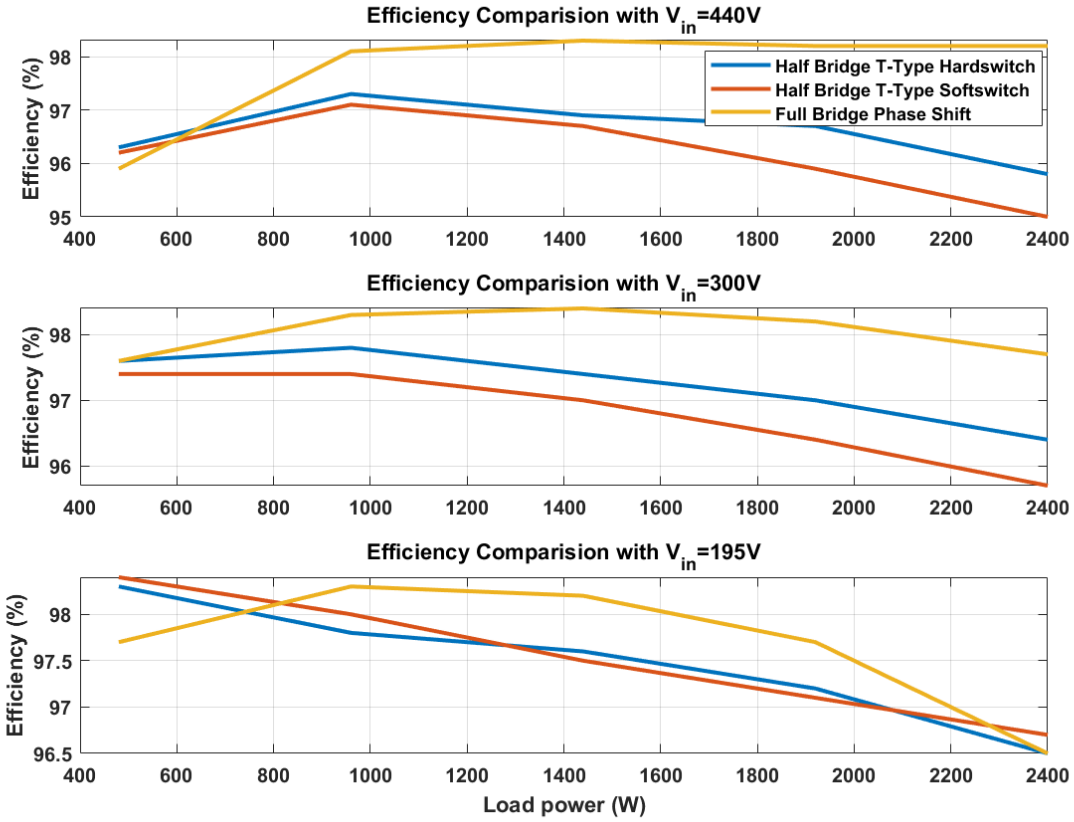

Comparison between two-level and three-level DC/DC converters

Master's Thesis in Sustainable Electric Power Engineering and Electromobility

Tianche Jiang, Mingshan Chen

DEPARTMENT OF ELECTRICAL ENGINEERING

CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2024
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Tianche Jiang, Mingshan Chen

Supervisor: Amir Parastar, Volvo Cars
Examiner: Mebtu Beza, Department of Electrical Engineering

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Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Sweden
Telephone +46 31 772 1000

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Tianche Jiang
Mingshan Chen
Department of Electrical Engineering
Chalmers University of Technology

Abstract

As automotive industry is developing rapidly, electric vehicles (EVs) have became a popular idea for green transportation due to its zero tailpipe emissions. One of the key parts on the EV board is the step-down DC/DC converter which is used to transfer power from high-voltage side battery to low-voltage side battery. To protect batteries on both sides, this DC/DC converter is always selected as isolated buck converter. This thesis project simulates, analysis and compares two-level and three-level isolated topologies, which are phase-shifted full bridge (PSFB) and T-Type converters in terms losses, efficiency and cost. In addition, since semiconductor technology is also growing quite fast, the new switching technology is used in selected topologies to check the difference between new switching device technology and traditional switching devices.

Firstly, the operation principles of different topologies with voltage, current waveform and parameter selection are presented, which is followed by the theoretical comparisons about transformer turns ratio, voltage stress, current waveform with rms current, MOSFET losses, transformer design and its losses calculation. In order to have more realistic results and a fair comparison, simulation of different topologies with same input and output voltage is done with PSpice. Then, the data exported from simulations are used to calculate MOSFET losses and efficiency while the transformer loss calculation is based on both simulation data and real model. The final results show that PSFB has high efficiency while all topologies are operating with the same switching techniques, but T-Type converter has potential to increase efficiency by replacing the middle bridge SiC MOSFETs with Si MOSFETs.

Keywords: DC/DC converter, Phase Shifted Full Bridge converter (PSFB), T-Type converter, Zero-Voltage switching (ZVS).

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Firstly, thanks to our supervisor Amir Parastar from Volvo Cars, for his guidance and help. We had weekly meetings through all the stages of the project and every time he gave us useful advice and led us to the correct direction. When we faced difficulties, we received not only technical support but also emotional support from him. Without any of these, we could not have finished the project successfully.
Then thanks to our examiner Mebtu Beza from Chalmers University of Technology. He recommended us to the Master's Thesis project and gave us many critical advices in the details. Also thanks to his lecturing in the course Power electronic converters which provided us with the foundations of power electronics knowledge.
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Tianche Jiang, Mingshan Chen, Gothenburg, November 2023

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

EV	Electric Vehicle
ZVS	Zero Voltage Switching
NPC	Neutral Point Clamped
PSFB	Phase Shifted Full Bridge
SiC	Silicon Carbide
GaN	Gallium Nitride
Si	Silicon
PWM	Pulsewidth Modulation
rms	Root Mean Square

Nomenclature

Below is the nomenclature of parameters that have been used throughout this thesis.

Parameters

L_r	Resonant inductance
C_r	Resonant capacitance
L_m	Magnetizing inductance
V_{dc}	DC-link voltage
D	Duty cycle
n	Turns ratio
V_o	Output voltage
i	Current
t	Time
$R_{ds(on)}$	MOSFET on-state resistance
iL_r	Current through resonant inductor
i_{int}	Initial current
L	Output filter inductance
t_{on}	MOSFET on time, also duty cycle time
R_{diode}	MOSFET body diode resistance
W_{ind}	Inductive energy
W_{cap}	Capacitive energy
C	Parasitic capacitance
$i_{r.int}$	Resonant inductor initial current
T_r	Resonant time
V_{peak}	The peak value of resonant voltage
L_{lk}	Leakage inductance
I_o	Output current

V_s	Transformer secondary side voltage
V_p	Transformer primary side voltage
i_{sec}	Transformer secondary side current
$i_{int.sec}$	Transformer secondary side initial current
Δt_{eff}	Effective duty cycle time
i_{fw}	Freewheeling current
D_{eff}	Effective duty cycle
D_{loss}	Duty cycle loss
n_{PSFB}	Turns ratio of the transformer of PSFB converter
n_{T_type}	Turns ratio of the transformer of T-type converter
$V_{DS.max}$	Maximum drain-source voltage of MOSFET
i_{pri}	Transformer primary side current
i_{rms}	RMS current
T	Switching period
Δt_{fw}	Freewheeling time
$\Delta t_{fw'}$	Freewheeling time of hard-switched T-type converter
t_{rv}	MOSFET voltage rise time
t_{fi}	MOSFET current fall time
$t_{sw.off}$	MOSFET switch off time
P_{off}	Turn off loss
f_{sw}	Switching off loss
P_{sw}	Switching losses
P_{on}	Turn on loss
$t_{sw.on}$	MOSFET switch on time
t_{fv}	MOSFET voltage fall time
t_{ri}	MOSFET current rise time
P_{cond}	Conduction loss
P_{switch}	Switch (MOSFET) losses
J	Current density
I_{wire}	Current through transformer wire
A_{wire}	Cross section of transformer wire
$N_{p-groups}$	Number of groups of transformer primary side wires
I_{p-rms}	RMS current of transformer primary side
$N_{s-groups}$	Number of groups of transformer secondary side wires

I_{p-rms}	RMS current of transformer secondary side
h	Rectangular wire height
w	Rectangular wire width
L_1	Total length of transformer primary side wire
$N_{windings}$	Number of transformer windings
N_{turns}	Number of turns of each transformer windings
L_2	Total length of transformer secondary side wire
L_s	Series inductance
N_s	Number of turns of the winding of series inductor
$\Re$	Reluctance in flux path
l_{total}	Total length of flux path
l_{airgap}	Length of air gap in the flux path
μ_0	Permeability of air
μ_r	Relative permeability
A_{core}	Cross section of transformer core
$N_{1-groups}$	Number of groups of resonant inductor wires
$V_{core-with-airgap}$	Core volume after subtract airgap
V_{core}	Total core volume
B_m	Maximum flux density
ψ	Flux linkage
Φ	Flux
P_{copper}	Copper loss
R_{pAC}	Primary winding AC resistance
R_{sAC}	Secondary winding AC resistance
F_{RB}	AC-to-DC winding resistance ratio
N_l	Number of layers of foil windings
h_B	Foil thickness
δ_ω	Skin depth
R_{DC}	DC resistance
η	Converter efficiency
P_{out}	Converter output power
P_{in}	Converter input power
R_{on}	MOSFET on-state resistance or body diode resistance
V_{sw}	Switching voltage

I_{sw}	Switching current
W_{sw}	Switching energy
$P_{copper.p}$	Primary side copper loss
$P_{copper.s}$	Secondary side copper loss
$P_{copper.series}$	Series inductor copper loss
$R_{series-AC}$	Series inductor AC wire resistance
R_{on}	MOSFET on-state resistance or body diode resistance
V_{sw}	Switching voltage
I_{sw}	Switching current
W_{sw}	Switching energy
$P_{j,t}^{PV}$	Active power from solar generation

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1

Introduction

1.1 Background

In recent years, the automotive industry is growing rapidly with the development of power electronic technologies and lithium-ion batteries, which makes electric vehicles (EVs) becoming an advanced topic compared with traditional petrol or diesel vehicles due to its sustainability [1]. The simplified EV board is shown as Figure 1.1 with blue arrows show the charging mode and red arrows display the operation mode [2].

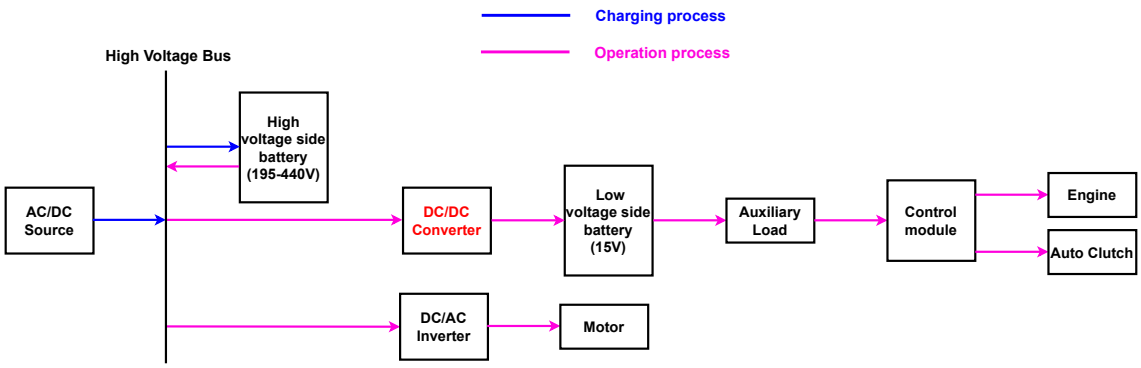

Figure 1.1: Simplified block diagram of EV board

During the charging process, the high-voltage side battery is getting charged through high-voltage bus by AC/DC source. In the operation mode, the high-voltage side battery will transfer power through DC/AC inverter to finally control the motor while it will also charge the low-voltage side battery through the DC/DC converter so that the auxiliary load such as heat, light and audio system can be supported and the control module can be triggered to control the engine and auto clutch. Therefore, it can be easily seen that how important the DC/DC converter block is in the EV board to transfer power from high-voltage side to low-voltage side working as a step-down converter. Meanwhile, to separate the batteries on both sides, usually this DC/DC converter is selected as center-taped isolated DC/DC converter to keep safety between both sides.

1.2 Isolated DC/DC topologies in EVs

The most widely used isolated DC/DC topologies in EVs are resonant LLC topology and full bridge topologies including full bridge hard switch and phase shifted full bridge converter with different control strategies.
Resonant LLC converter as shown in Figure 1.2 is a kind of resonant converter which could operate at high input voltages and high frequencies, because it has significantly small switching losses due to zero voltage switching (ZVS) turn on of primary side MOSFETs achieved by LC resonant circuit consists of one shunt inductor L_m in parallel with the primary winding of the transformer, one resonant inductor L_r, and one resonant capacitor C_r [3].

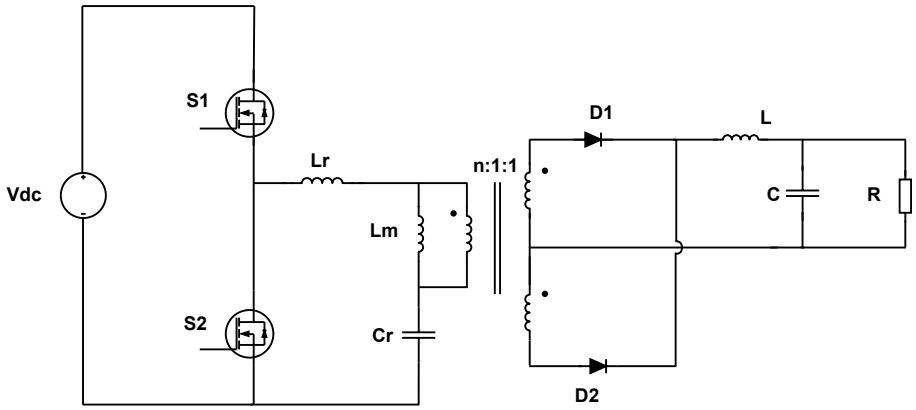

Figure 1.2: Resonant LLC Converter

For full bridge hard switch and phase shifted full bridge converter, they share the same schematic as shown in Figure 1.3 but have different controlling schemes, which finally causes that full bridge hard switch converter is a hard switched converter and phase shifted full bridge could achieve ZVS turn on with LC resonant circuit consists of resonant inductor L_r and parasitic capacitor of MOSFETs ($S1$ to $S4$). Therefore, full bridge hard switch converter has more switching losses compared with resonant LLC converter due to its hard switching modulation [3]. Meanwhile, since phase shifted full bridge converter is operated with zero voltage switching (ZVS) technique, it has less switching losses compared with full bridge hard switch converter [4].

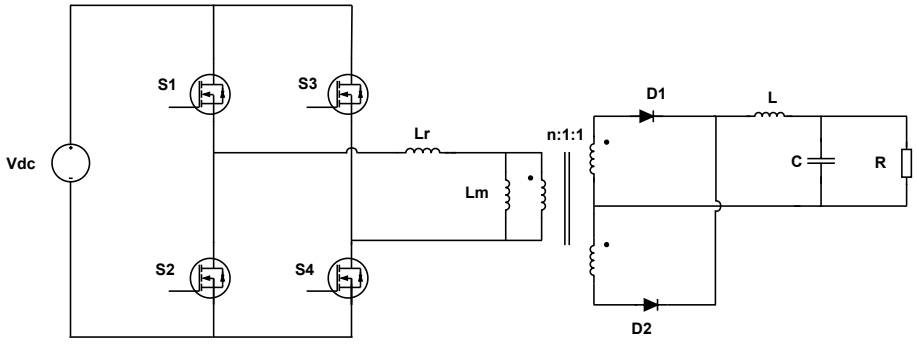

Figure 1.3: Full Bridge Converter

1.3 Definition of voltage levels

Considering the definition of voltage levels in DC/DC converters, it can be expressed as the number of pole voltages. As shown in Figure 1.4, when the pole is connected to T1, the pole voltage is V_{dc}; when the pole is connected to T2, the pole voltage will be 0 which makes a two-level topology. For three-level topology, there will be one extra throw T0 connected to the middle as in Figure 1.5, so the pole voltages can be V_{dc}, $V_{dc}/2$ and 0 which means it has three voltage levels.

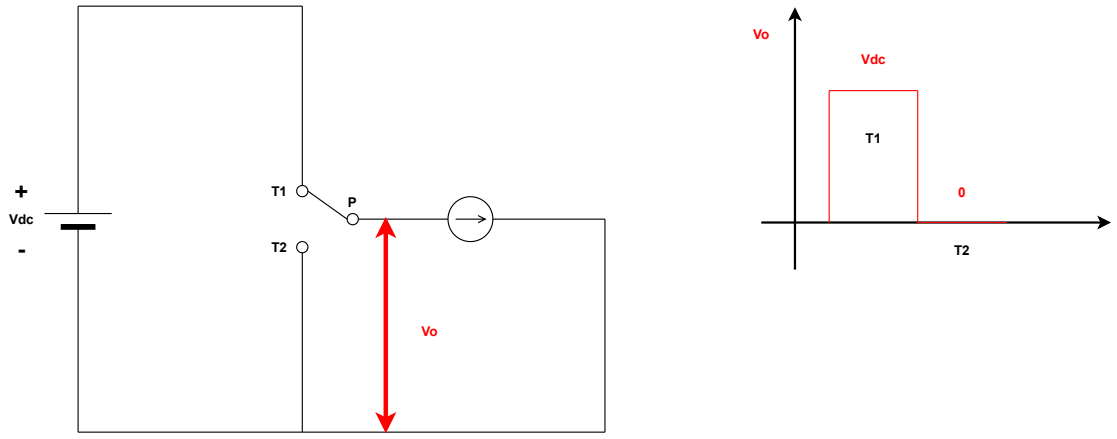

Figure 1.4: Two-level topology

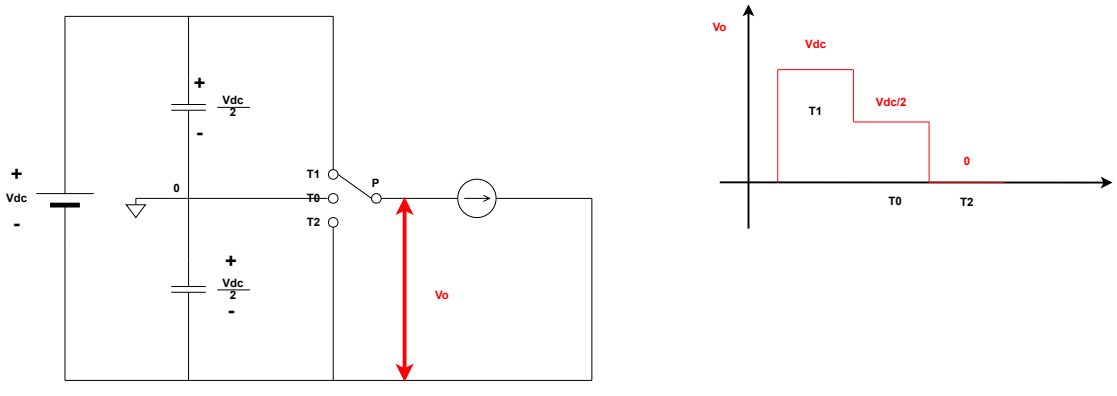

Figure 1.5: Three-level topology

1.4 Topology selection and power semiconductor devices

The most typical three-level topology is actually neutral point clamped (NPC) converter which could draw the input current and generate output voltages with low distortion [5]. However, when it comes to three-level converter, there is one more topology which is called T-Type converter as shown in Figure 1.6. Compared with

NPC, T-Type converter is less complex to operate and the clamped diodes are eliminated which could reduce the conduction losses since T-Type converter only requires four active switches on primary side [6]. Hence, T-Type converter can be considered as a three-level converter in the comparison with phase shifted full bridge (PSFB) converter which is a traditional two-level topology used in EVs with soft switching modulation.

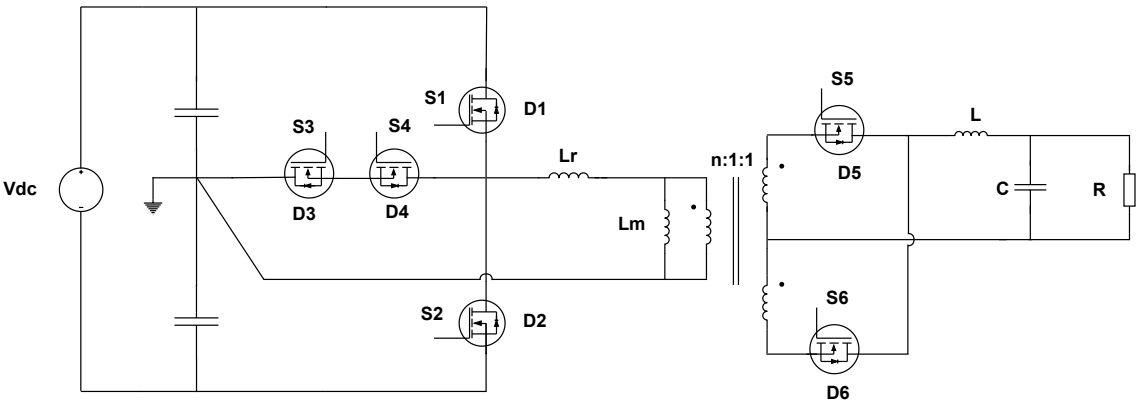

Figure 1.6: Half Bridge T-Type Converter

The commonly used DC-DC power electronic systems in EVs are operating under 400V or 800V voltage levels of batteries. However, only 400V system is considered here to test the performance of new switching devices which is wide band material semiconductor could lower power losses of the converter when switching frequency is increased [7]. There are two kinds of wide band semiconductors — Silicon Carbide (SiC) and Gallium Nitride (GaN). As wide-bandgap materials, SiC and GaN could advance the performance of power electronic switches — SiC capable of several kilovolts, while GaN has just reached one kilovolt ratings [8]. Compared with Si switches, SiC switches have better voltage blocking, lower switching losses, and improved high temperature performance due to its higher bandgap energy [9]. Meanwhile, GaN semiconductor devices has zero reverse recovery loss due to the absence of a substrate diode which means the reverse current only going through the source-drain channel so it will have lower switching losses compared with Si semiconductors [10]. Moreover, as such similar kinds of materials with same benefits of lower switching losses and better performance in higher frequency compared with traditional material Si, they also show similar experimental results in terms of converter efficiency and loss distribution, but GaN switches have higher purchase price compared with SiC switches [11].

In order to have an easier comparison, it is quite useful to do simulation for the selected topologies to have some practical results. In this case, only SiC switches is used to show the performance of new switching device technologies and find the difference between wide band and traditional semiconductors; due to similarity between the two materials and lower cost of SiC compared with GaN switches. Furthermore, transformer and gate driver are simplified in the simulation to make it simpler and

reduce the simulation time. Since the comparison has to be practical, the total cost of components in topologies should also be considered as a part of it.

1.5 Purpose

The purpose of this thesis is to simulate and compare two-level topology in this case is PSFB and three-level topology which is T-Type converter with different switching device technologies in terms of power losses, efficiency and cost. The two topologies are analyzed under the same input voltage level (400V), output voltage (15V) and maximum output current (160A) while parts of the switches in T-Type topology are modified to find the potential and limitations of it.

1.6 Limitations

In this thesis, only the metioned two DC/DC topologies simulated with pulsewidth modulation (PWM) are discussed and compared. Since there is no time to go for new topologies, the comparison only stops at T-Type converter with both soft and hard switching modulations. Meanwhile, only SiC MOSFET is applied to show the performance of new switching device technologies in the selected topologies. Moreover, the gate driver is simplified as ideal voltage signals with small series resistor while the battery is represented with DC voltage source in simulation, so these parts of losses are also ignored. However, even the transformer in simulation is formed with ideal inductors, the transformer losses are still part of loss analysis in this thesis by hand calculation using real transformer models and data exported from simulation. Hence, only power conversion losses are considered in the analysis and efficiency calculation of each topology.

1.7 Scope

This report has five chapters except for this one. After this chapter, firstly all the theoretical analysis of selected topologies are given in Chapter 2 which is followed by the theoretical comparison between different topologies in different aspects in Chapter 3. Then, the description about how the losses and efficiency calculation could be done based on simulation models is displayed in Chapter 4. After that, Chapter 5 presents all the comparison results and simple discussions about them. Finally, this thesis report is going to be ended with a conclusion of current work and some discussions about future work.

2

Theory

This chapter basically describes the topologies and operation principles of two different types of isolated DC-DC converters, which are one type of two-level converter, and one type of three-level converter, respectively. The waveform of MOSFETs gate voltage, transformer voltage and current and output current are shown in figures. The switching pattern of the DC/DC converters are also considered and introduced:for the two-level converter, only soft switching mode is introduced, but for the three-level converter, both hard switching and soft switching mode are introduced. The method for deriving the parameter whose value influences the switching mode of the three-level converter is introduced as well.

2.1 Two-Level Converter

The schematic of PSFB converter is displayed in Figs 2.1 and 2.2. S_1-S_4 in Figure 2.1 represent the primary side MOSFETs, D_1-D_4 represent the body diode of those MOSFETs while the parasitic capacitances of these MOSFETs are not shown in the figure but will be mentioned in the explanation of the circuit's operation principle since they are used to achieve soft switching process. Meanwhile, PSFB has one more inductor in series with the leakage inductance of the transformer to achieve soft switching, so the series inductance shown in the figure is the total resonant inductance including the leakage inductance of the transformer. The transformers used in both the two-level converter and the three-level converter have a center-tapped secondary winding which can be treated as two separate secondary windings, so the turns ratio will be n:1:1 as shown in Figure 2.1. Also in this case, rectifying diodes D_5 & D_6 are substituted by MOSFETs S_5 & S_6, which can be controlled to perform the rectification function, as shown in Figure 2.2. This is because the secondary side has high current, using MOSFETs will reduce the conduction loss since MOSFETs has lower on-state resistance than diodes.

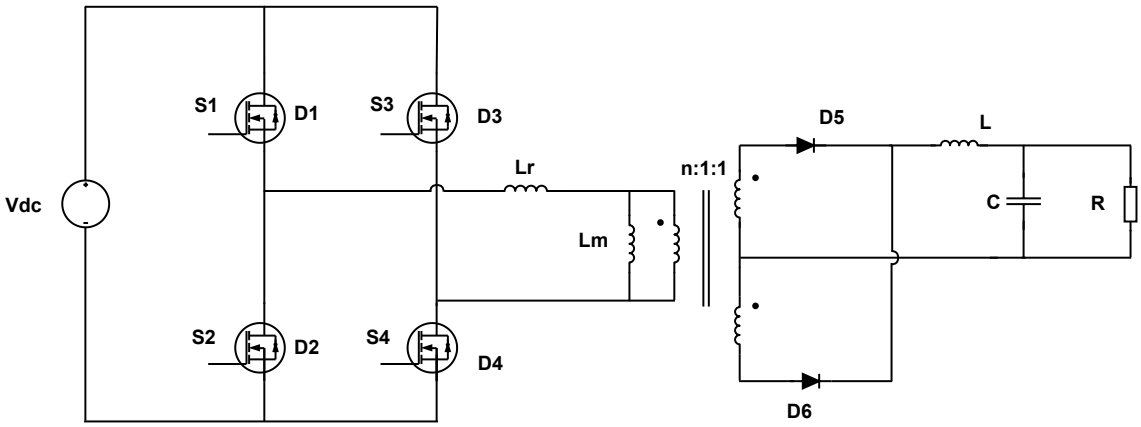

Figure 2.1: PSFB Converter with diodes

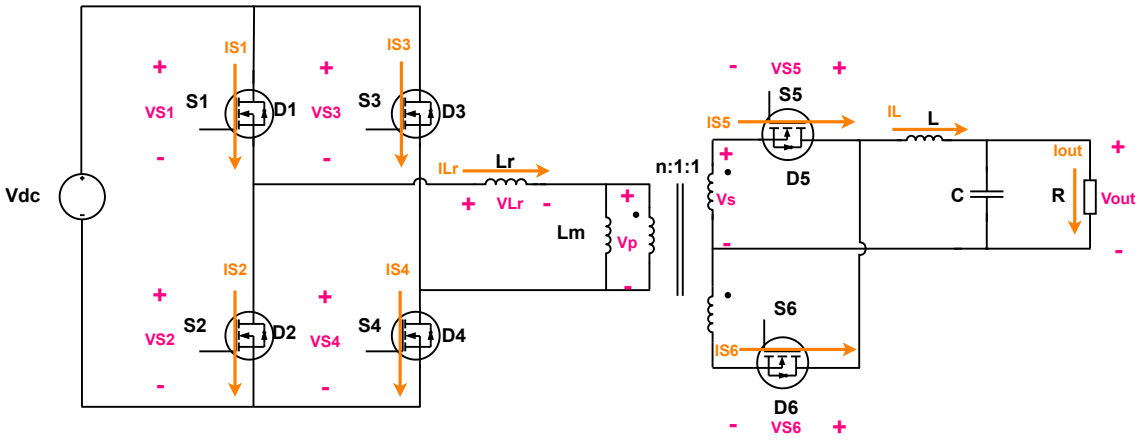

Figure 2.2: PSFB Converter with MOSFETs

The reason why PSFB converter is two-level converter, refer to the description in section 1.3 and Figure 1.4, is because the output voltage of each bridge leg of it is two-level voltage. In Figure 2.3, V_{lead} represents the leading leg output voltage while V_{lag} represents the lagging leg output voltage. In Figure 2.4 and 2.5, it can be seen that both of these two legs have two-level output voltage, which proves that PSFB converter is a two-level converter. More detailed analysis about the generation of this voltage is shown in section 3.2.

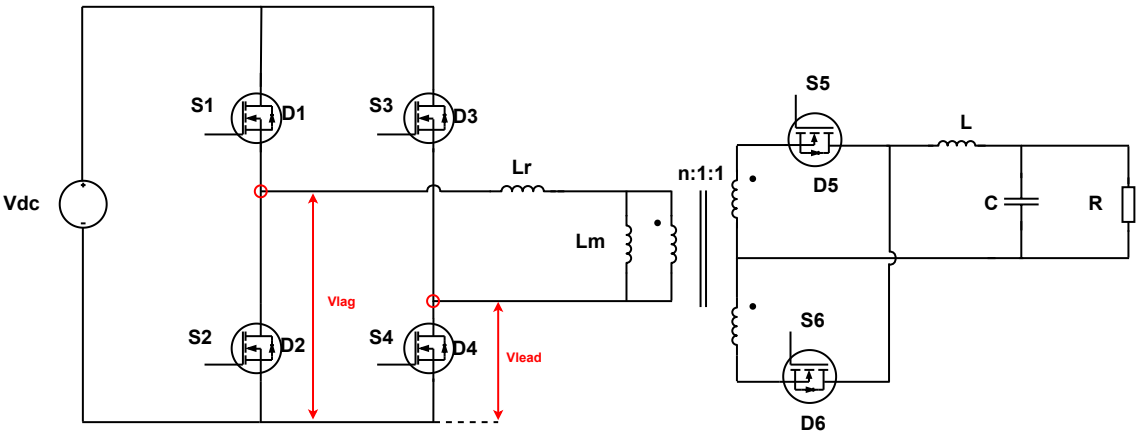

Figure 2.3: PSFB Converter leg output

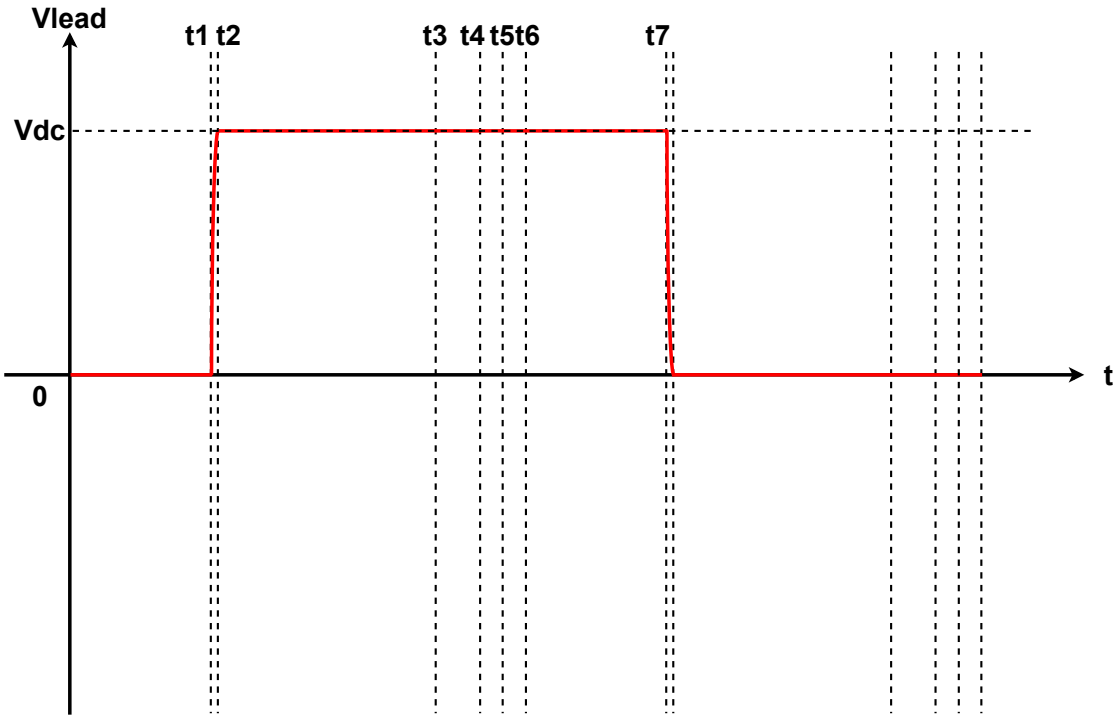

Figure 2.4: PSFB leading leg output

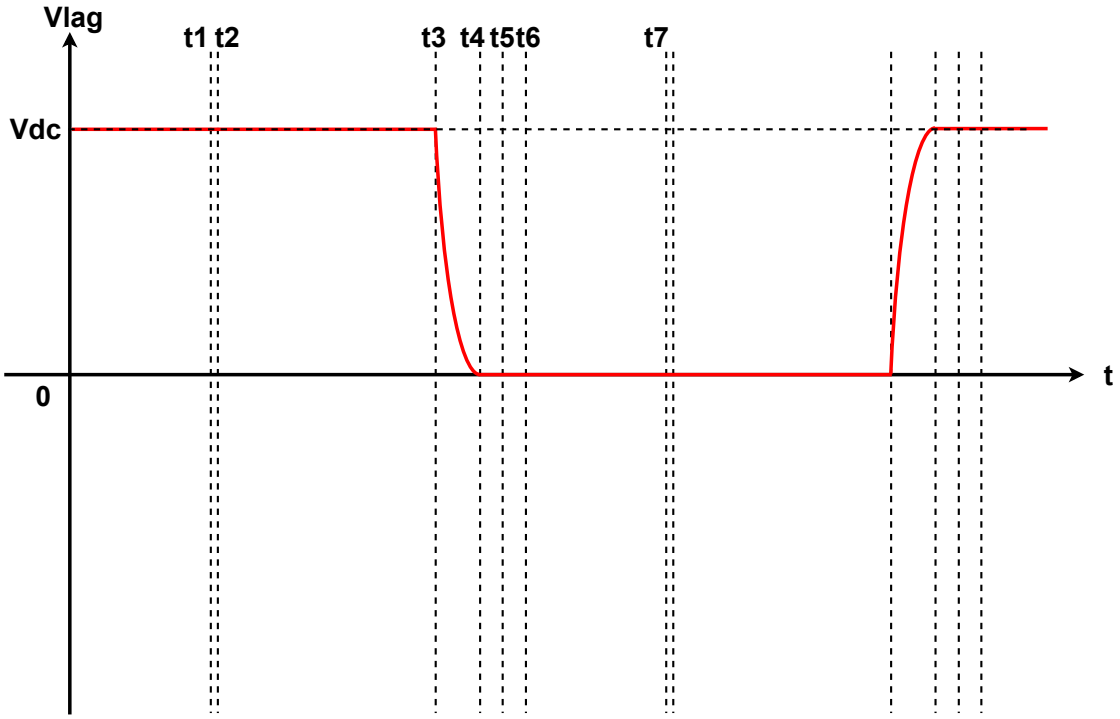

Figure 2.5: PSFB lagging leg output

2.1.1 Phase Shifted Full Bridge

To formulate a PSFB converter, all switches on primary side have the same turn on time but the gate-to source voltages in the right leg are shifted by $\Delta\phi$ which is the phase shift with respect to the left leg, so the phase shift $\Delta\phi$ can be determined with effective duty cycle D as equation 2.1 [12].

$$D = \frac{1}{2} - \frac{\Delta\phi}{2\pi} \tag{2.1}$$

In this case, the effective duty cycle D can be calculated with input voltage V_{dc}, transformer turns ratio n and output voltage V_o as shown in equation 2.2.

$$D = \frac{nV_o}{V_{dc}} \tag{2.2}$$

A.Energy transfer stage$(0 \sim t_1)$
In this stage, at the primary side, MOSFETs S_1 & S_4 are conducting, voltage on the transformer primary winding is V_{dc}, energy is transferred to the secondary side. At the secondary side, MOSFET S_5 is conducting, while S_6 is reversely biased, then the voltage on the secondary side filter inductor is $\frac{V_{dc}}{n} - V_o$, so the secondary side current increases linearly with slope $\frac{\frac{V_{dc}}{n} - V_o}{L}$, and so does the primary side current which in this stage is just the reflection of the secondary side current.
B.Resonant stage$(t_1 \sim t_2)$
At t_1, S_4 is turned off, then the LC resonance happens between parasitic capacitance C_3 & C_4, resonant inductor L_r and magnetizing inductance L_m. During the resonance, the voltage on C_4 increases from 0V to V_{dc}, while the voltage on C_3 decreases from V_{dc} to 0V, and the voltage on L_m decreases from V_{dc} to 0V as well. Due to the existence of the L_m, usually this resonant period is very short so it is negligible, and the primary side current almost remains the same. This is also the reason why the voltage on the resonant inductor remains the same, because the $\frac{\Delta i}{\Delta t}$ is negligible.
C.Freewheeling stage$(t_2 \sim t_3)$
After the resonance ends, at the primary side, since the voltage on MOSFET S_3 already reached 0V, the primary side current is able to flow through body diode D_3 before S_3 is triggered. Usually the time during which the body diode conducts should be controlled as short as possible because of the larger resistance of the body diode compared with the $R_{ds(on)}$ of the MOSFET. After S_3 is triggered, freewheeling current flows through the MOSFET itself instead of the body diode. The primary side freewheeling current decreases exponentially but in most of the cases it can be seen as linearly because of its relatively large time constant [13]. Then the primary side freewheeling current (which is also the current flows through resonant inductor, here it is named as iL_r) is:

$$iL_r = i_{int}(1 - \frac{2R_{ds(on)}}{L_r}t) \tag{2.3}$$

Here the i_{int} is the initial current of the freewheeling stage, which value is almost the same as the primary side peak current since the resonant time is very short, as mentioned before.
At the secondary side, since the transformer primary side voltage reached 0V at the end of the previous stage, then the voltages on the two secondary windings both became 0V as well, S_6 is no longer reversely biased and can be triggered. After triggering, secondary side current will flow through both S_5 and S_6. And since the voltage on the output inductor becomes $-V_o$ in this stage, output current will decrease linearly with slope $\frac{-V_o}{L}$, so the current in S_5 and S_6 also changes linearly since they are the sum of two linearly changing waveforms.
D.Resonant stage$(t_3 \sim t_4)$
At t_3, S_1 is turned off, then the LC resonance happens between parasitic capacitance C_1 & C_2 and the resonant inductor L_r. In this case L_m does not participate in the resonance since the primary side voltage remains at 0V, the magnetizing current

freewheels through the L_m remains constant. During the resonance, the voltage on C_1 increases from 0V to V_{dc}, the voltage on C_2 decreases from V_{dc} to 0V, and the voltage on L_r decreases from 0V to $-V_{dc}$. The primary side current decreases from the final value of the freewheeling stage to somewhere between this value and 0A, which depends on how much inductive energy were stored in the resonant inductor before. The voltages on the secondary side windings both remain 0V since the primary side voltage remains 0V, so the freewheeling at the secondary side continues.

E.Duty cycle loss stage$(t_4 \sim t_6)$

After the resonance ends, at the primary side, since the voltage on the resonant inductor reached $-V_{dc}$, then the primary side current starts to decrease linearly with slope $\frac{-V_{dc}}{L_r}$, and this current will go through S_3 and body diode D_2, since the voltage on switch S_2 already reached 0V at the end of the previous stage and D_2 was forward biased. During the time that D_2 is conducting, since the voltage on S_2 is 0V, then the switching on of it during this time is ZVS. Since the primary side current (also the current going through D_2) is decreasing linearly, the switching must happen before this current reaches to 0A to make sure it is within the time that D_2 is still conducting, which means S_2 must be switched on before t_5. Because once the current changes its direction, it is no longer able to go through D_2 and ZVS is lost. So usually S_2 will be triggered as soon as the resonance ends to promise the ZVS.

After S_2 is turned on, the current will no longer go through body diode D_2 but will go through S_2 instead. The current keeps decreasing linearly until t_5. At time t_5, it reaches 0A and the direction of it will reverse afterwards. Between t_5 & t_6, the current increases linearly at the opposite direction and at time t_6, it reaches the initial value of the next half period which starts from t_6. The characteristic of the second half period is same as the first half period but it is S_2 & S_3 that transfer the energy in the energy transfer stage instead.

In the duty cycle loss stage, both of the two primary switches are turned on, but they are working with neither the energy transferring nor the freewheeling, so it seems like some time, which is useless from the energy perspective, locates within the total t_{on}, this is basically why it is named as "duty cycle loss". But it is necessary for the MOSFETs to perform ZVS. And at the secondary side, during the duty cycle loss stage, current keeps flowing through S_5 & S_6 and keeps changing linearly. After it ends and the circuit reaches to the next period, there will be only S_6 conducting since S_5 will be reversely biased.

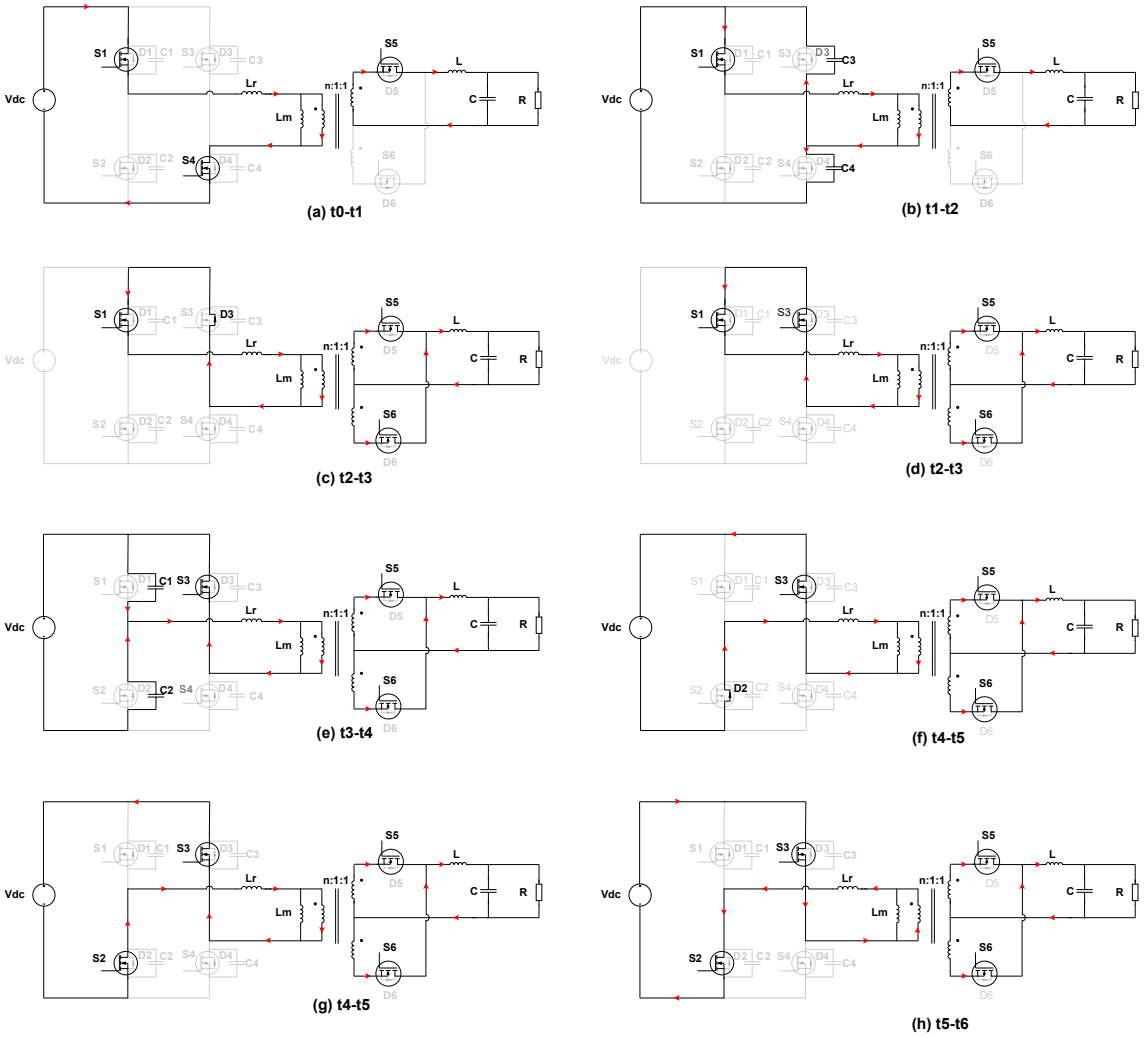

Figure 2.6: PSFB Operation 1

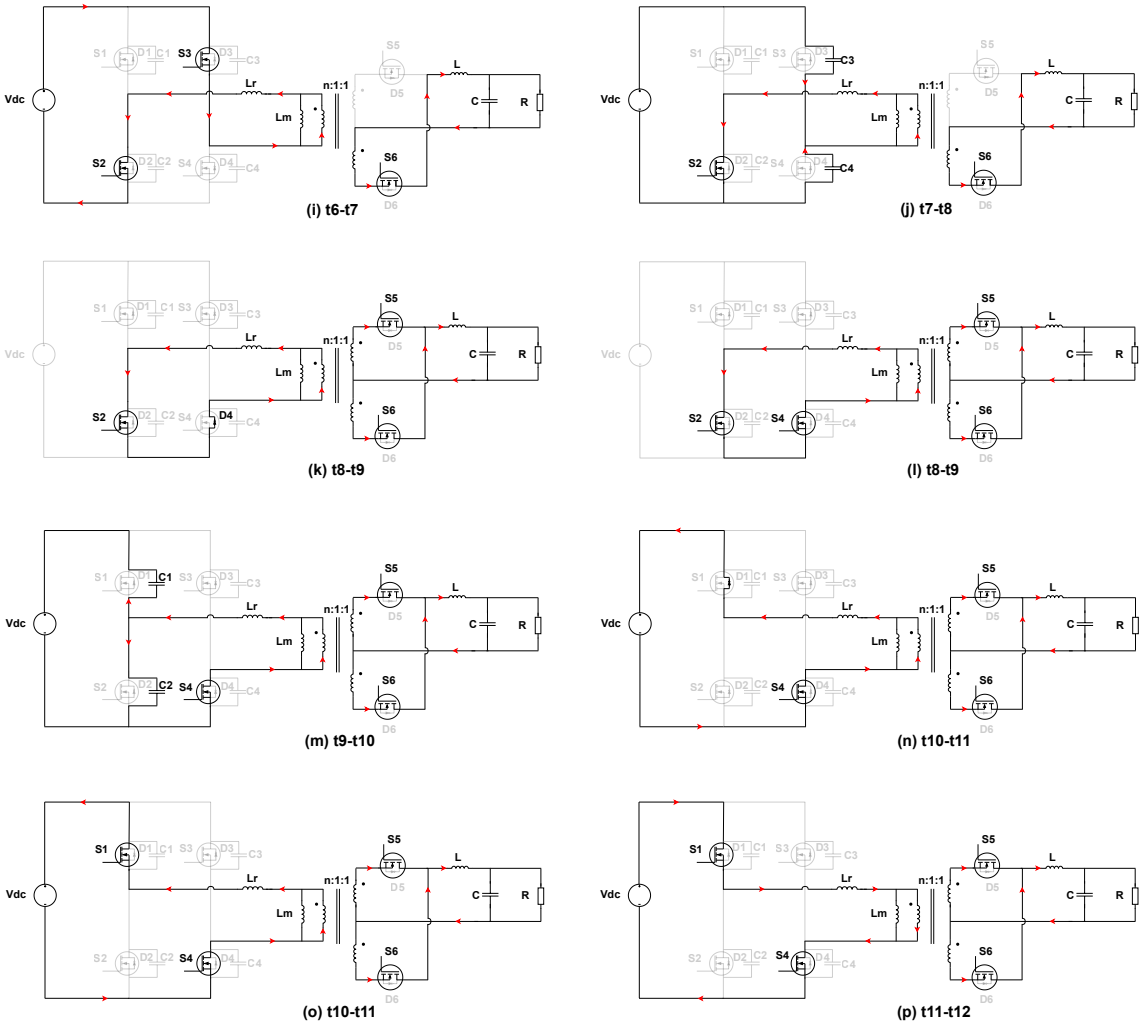

Figure 2.7: PSFB Operation 2

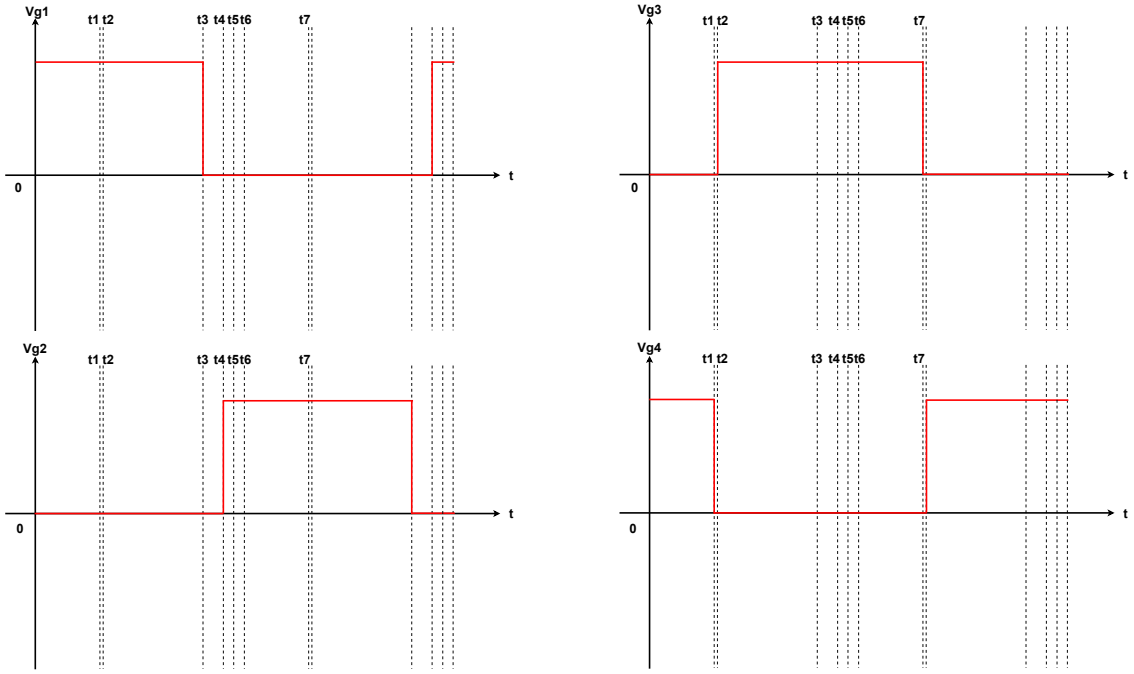

Figure 2.8: Gate voltage of primary side MOSFET in PSFB

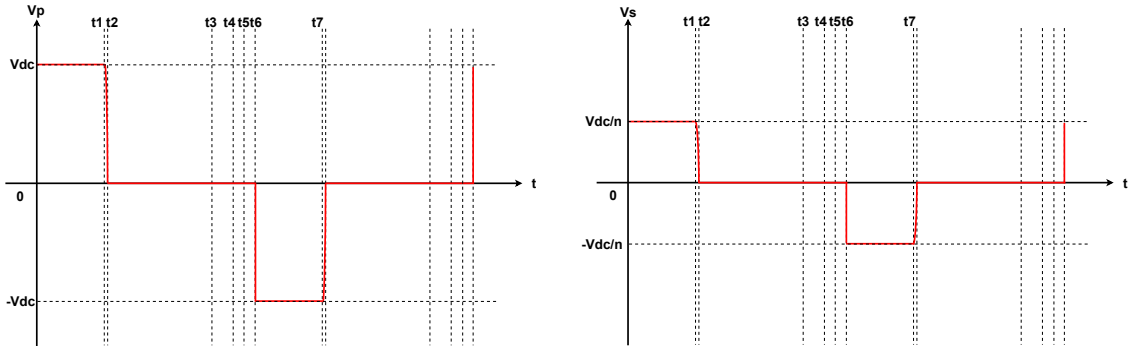

Figure 2.9: Transformer voltage in PSFB

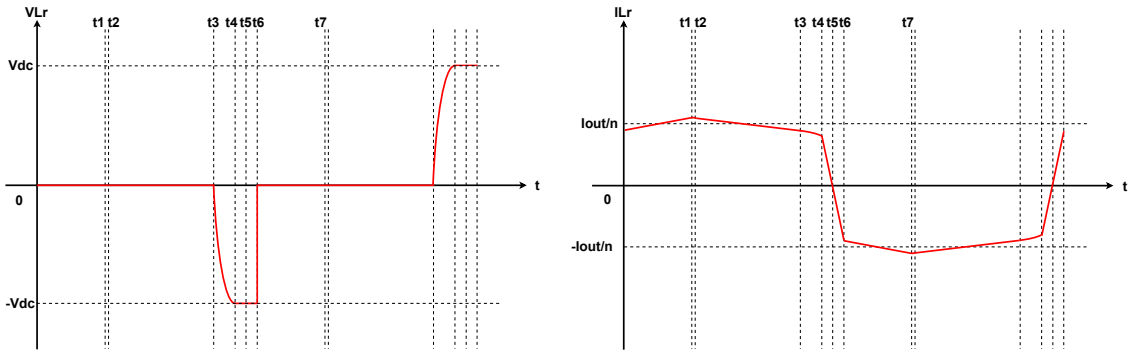

Figure 2.10: Resonant inductance voltage and current in PSFB

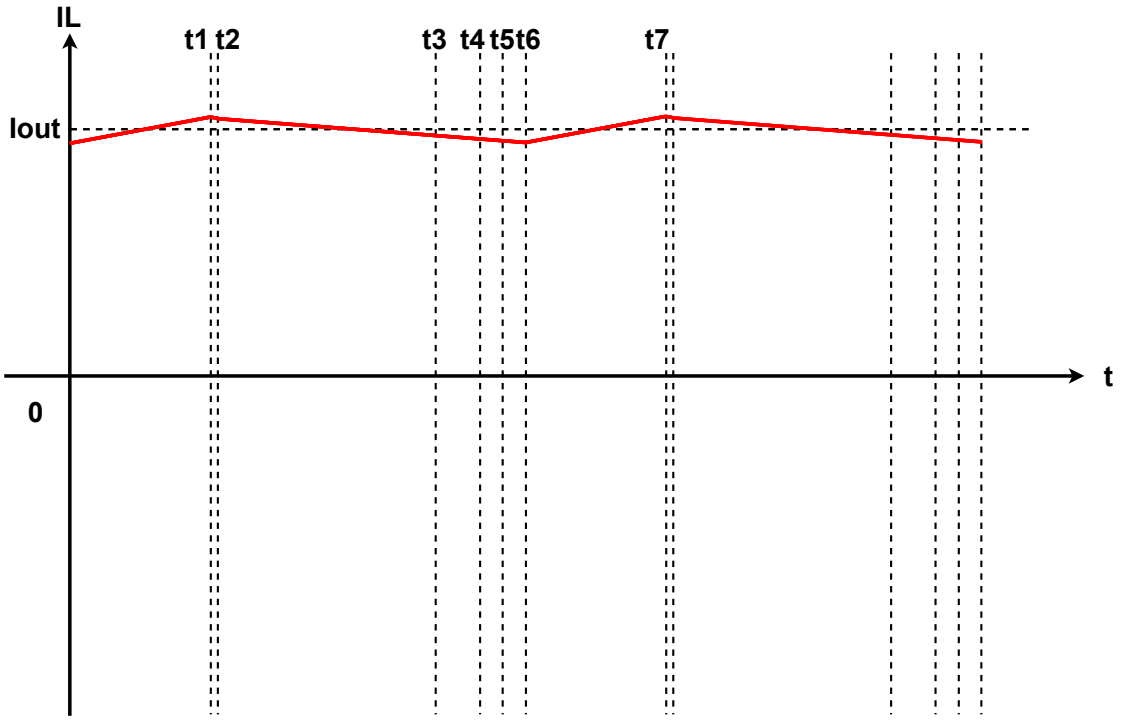

Figure 2.11: Output filter current in PSFB

2.2 Three-Level Converter

The three-level converter used in this thesis is half bridge T-type converter, which structure is basically a half bridge converter with a middle bridge created by two anti-serially connected MOSFETs, as shown in Figure 2.12 [14]. In this thesis, both hard-switched T-type converter and soft-switched T-type converter will be discussed and compared with PSFB converter, but only the operation principle of soft-switched T-type converter will be introduced since they share similar schematics and operation principles. Same as PSFB converter, for achieving soft switching, an external inductor is installed at the primary side of the transformer, which in the circuit diagram is connected in series with the leakage inductance of the transformer, shown as resonant inductor L_r. And for hard-switched T-type, this inductor is not applied. To make the introduction more general, turns ratio here is shown as n:1:1, but in real case such as the comparison later, it varies. Also in Figure 2.12, input voltage is clamped by two extra capacitors, which is one disadvantage of it compared with PSFB converter. Each of these capacitors blocks $\frac{V_{dc}}{2}$, but in Figure 2.15 & 2.16, they are represented by two voltage sources to make the introduction simple.

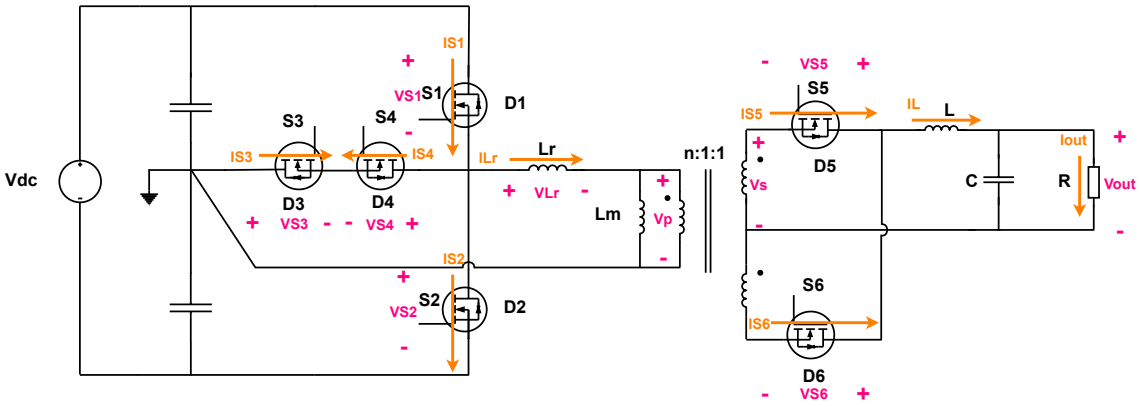

Figure 2.12: Half Bridge T-Type Soft Switch Converter

The reason why T-type converter is three-level converter is also relevant to the output voltage of its bridge leg. According to section 1.3, Figure 1.5, and Figure 2.13, V_o in Figure 2.13 represents the output voltage of the bridge leg of T-type converter. In Figure 2.14, it can be seen that the leg has three-level output voltage, which proves that T-type converter is a three-level converter. More detailed analysis about the generation of this voltage is shown in section 3.2.

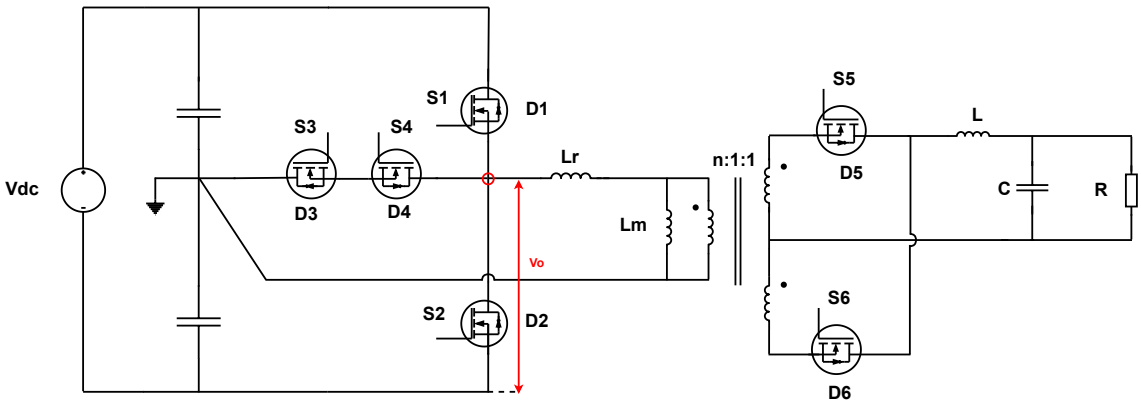

Figure 2.13: PSFB Converter leg output

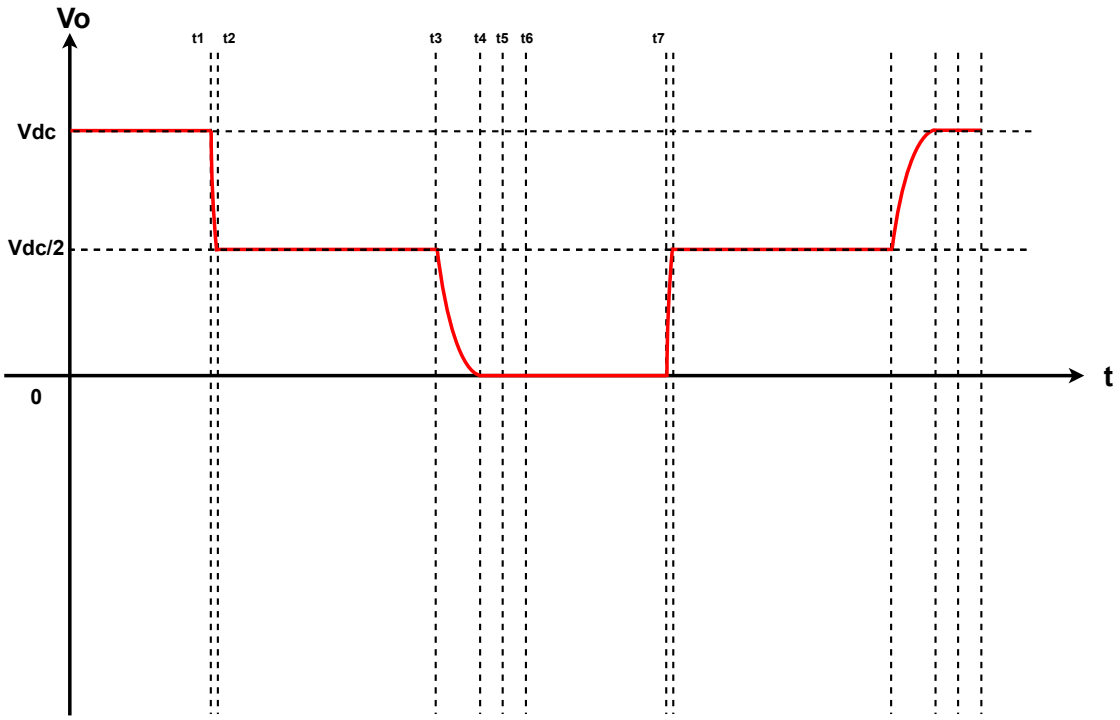

Figure 2.14: PSFB Converter leg output

2.2.1 Half Bridge T-Type Soft Switch

A.Energy transfer stage$(0\sim t_1)$
In this stage, at the primary side, MOSFETs S_1 is conducting, voltage on the transformer primary winding is $\frac{V_{dc}}{2}$, energy is transferred to the secondary side. At the secondary side, MOSFET S_5 is conducting, while S_6 is reversely biased, then the voltage on the secondary side filter inductor is $\frac{\frac{V_{dc}}{2}}{n} - V_o$, so the secondary side current increases linearly with slope $\frac{\frac{\frac{V_{dc}}{2}}{n} - V_o}{L}$, and so does the primary side current which in this stage is just the reflection of the secondary side current.
B.Resonant stage$(t_1\sim t_2)$
At t_1, S_1 is turned off, then the LC resonance happens between parasitic capacitance C_1 & C_2 & C_4, resonant inductor L_r and magnetizing inductance L_m. During the resonance, the voltage on C_1 increases from 0V to $\frac{V_{dc}}{2}$, the voltage on C_2 decreases from V_{dc} to $\frac{V_{dc}}{2}$. The voltage on C_4 decreases from $\frac{V_{dc}}{2}$ to 0V, the reason here is because at sometime during when S_1 is conducting in the previous stage, S_3 was turned on to create the middle path for later operation, which means in Figure 2.15 (a) (or in Figure 2.16 (m) & (n)), at sometime S_3 was already turned on, but there was no current flowing through it temporarily, and S_4 blocked $\frac{V_{dc}}{2}$. The voltage on L_m decreases from $\frac{V_{dc}}{2}$ to 0V. Same as PSFB converter, the large L_m causes the resonant stage to be very short, and negligible $\frac{\Delta i}{\Delta t}$ at the primary side.

C.Freewheeling stage($t_2 \sim t_3$)

After the resonance ends, at the primary side, since the voltage on MOSFET S_4 already reached 0V, D_4 is forward biased. Then the primary side current freewheels through MOSFET S_3 and body diode D_4. Same as PSFB converter, the exponential freewheeling can be seen as linear, then the primary side current is:

$$iL_r = i_{int}(1 - \frac{R_{ds(on)} + R_{diode}}{L_r}t) \tag{2.4}$$

Here the i_{int} is the initial current of the freewheeling stage, which value is almost the same as the primary side peak current, for the same reason as PSFB converter.

At the secondary side, also same as PSFB converter, the linear current flow through both S_5 and S_6. And the slope of output current is $\frac{-V_o}{L}$.

D.Resonant stage($t_3 \sim t_4$)

At t_3, S_3 is turned off, then the LC resonance happens between parasitic capacitance C_1 & C_2 & C_3, and the resonant inductor L_r, for the same reason as PSFB, L_m does not participate in the resonance. During the resonance, the voltage on C_1 increases from $\frac{V_{dc}}{2}$ to V_{dc}, the voltage on C_2 decreases from $\frac{V_{dc}}{2}$ to 0V. The voltage on C_3 increases from 0V to $\frac{V_{dc}}{2}$ while body diode D_4 keeps conducting, the voltage on it remains at 0V. The voltage on L_r decreases from 0V to $-\frac{V_{dc}}{2}$ while the primary side current decreases from the final value of the freewheeling stage to somewhere between this value and 0A. The secondary side remains freewheeling for the same reason as PSFB converter.

E.Duty cycle loss stage($t_4 \sim t_6$)

After the resonance ends, at the primary side, the current starts to decrease linearly due to the voltage on the resonant inductor, with slope $\frac{\frac{-V_{dc}}{2}}{L_r}$. Before S_2 is triggered, this current flows through body diode D_2, as for the same reason as PSFB, if the circuit needs to perform ZVS turning on, S_2 must be switched on before the current changes its direction, which is at t_5. After the switching the current will go through S_2 and this duty cycle loss stage will end after the primary side current reaches the initial value of the next energy transfer stage, and next half period will start afterwards. Besides, as can be seen in Figure 2.17, middle switch S_4 can be switched on at the same time as when S_2 is turned on (same for S_1 & S_4). This is because in duty cycle loss stage, the voltage on S_3 is already $\frac{V_{dc}}{2}$ and S_3 performs as open circuit, the voltage on S_4 is 0V, so the turning on of S_4 at this time will also be ZVS. Furthermore, as long as the middle switch can be turn on before the next freewheeling stage (which means during duty cycle loss stage or the next energy transfer stage), it will always perform ZVS since no current will go through it before the next freewheeling stage, the voltage on it remains at 0V.

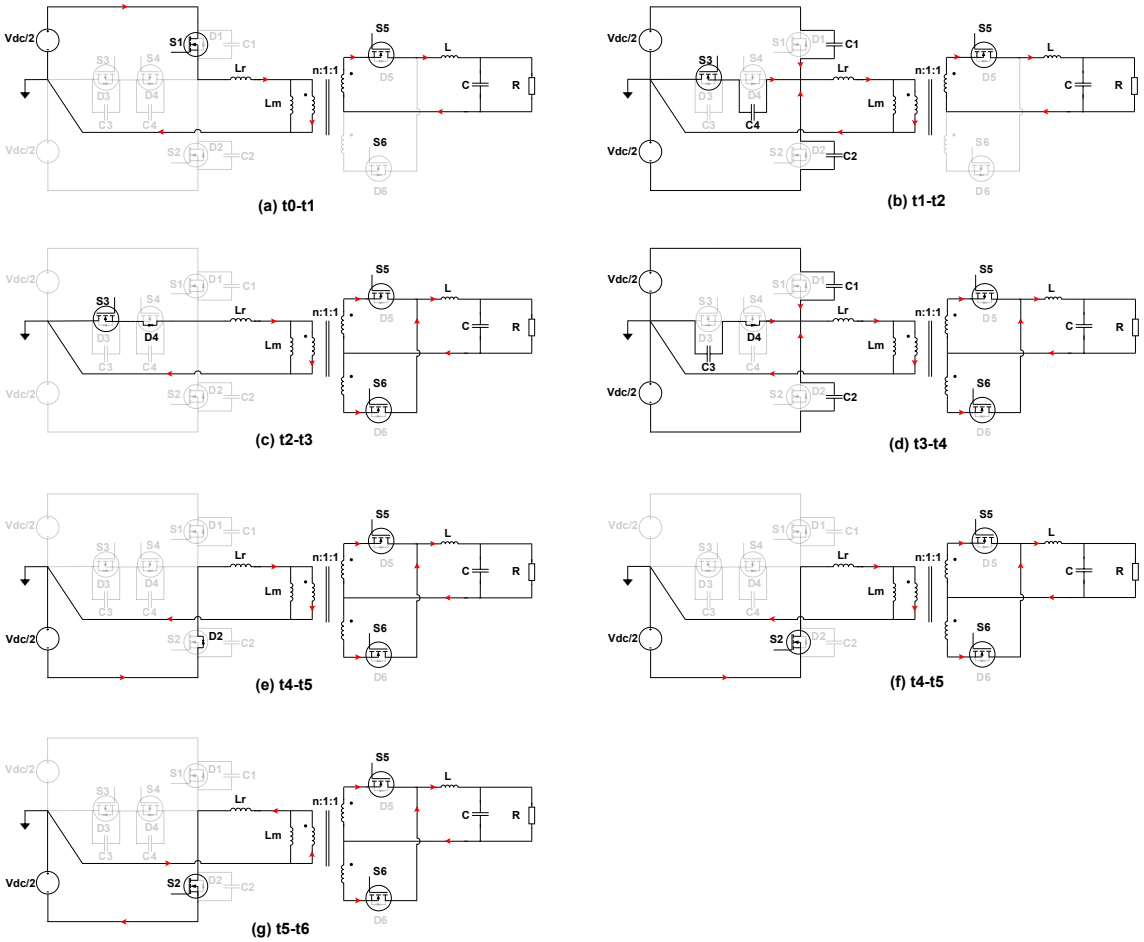

Figure 2.15: Half Bridge Soft Switch Converter Operation 1

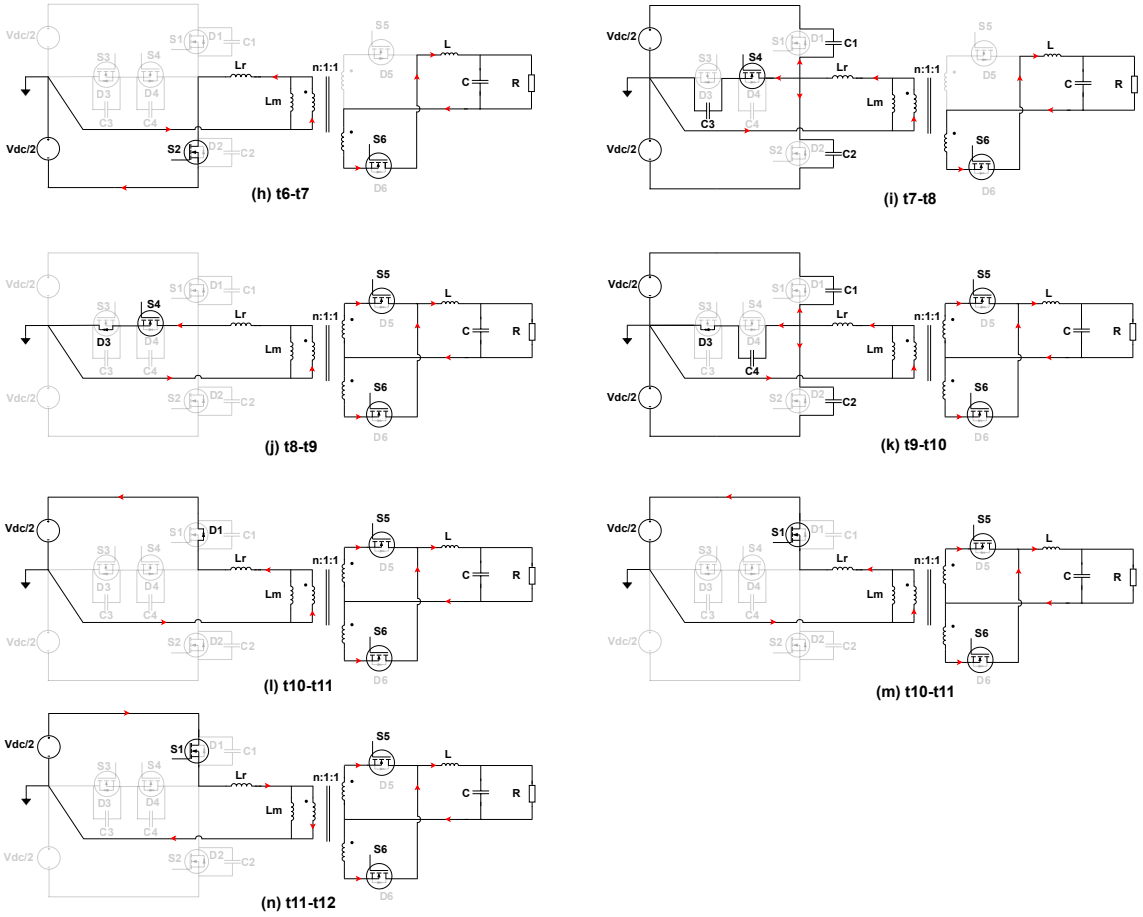

Figure 2.16: Half Bridge Soft Switch Converter Operation 2

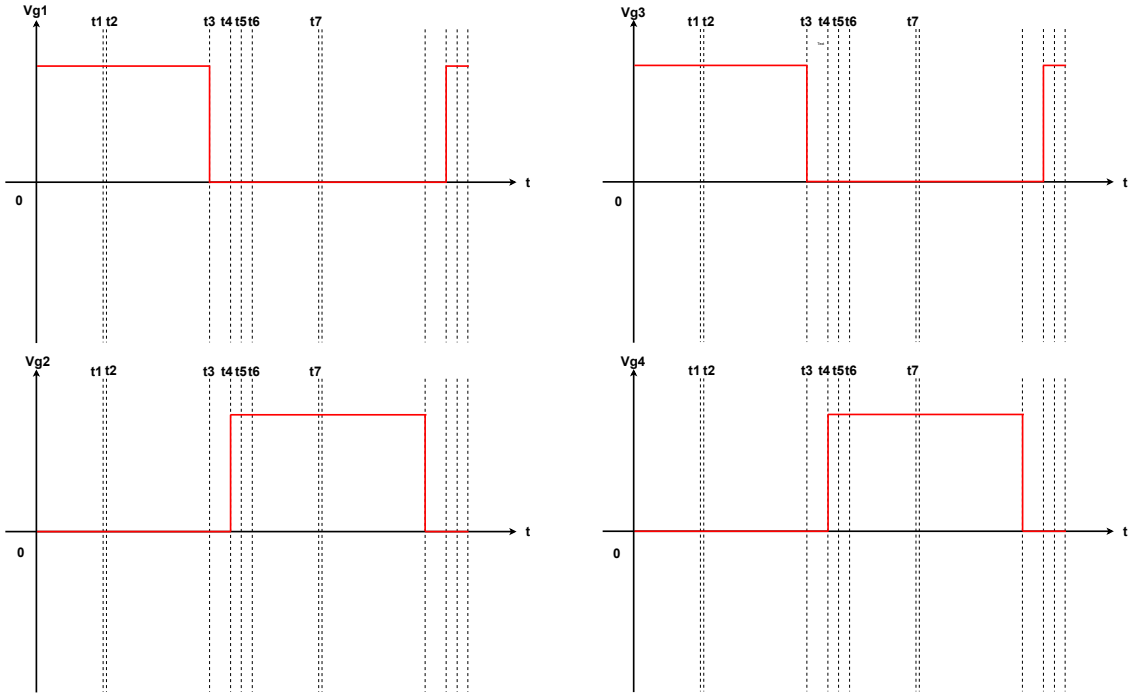

Figure 2.17: Gate voltage of primary side MOSFET in T-Type

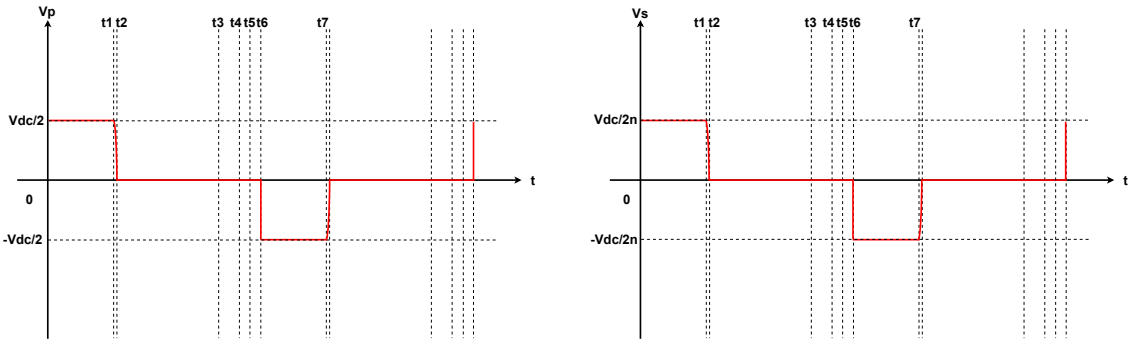

Figure 2.18: Transformer voltage in T-Type

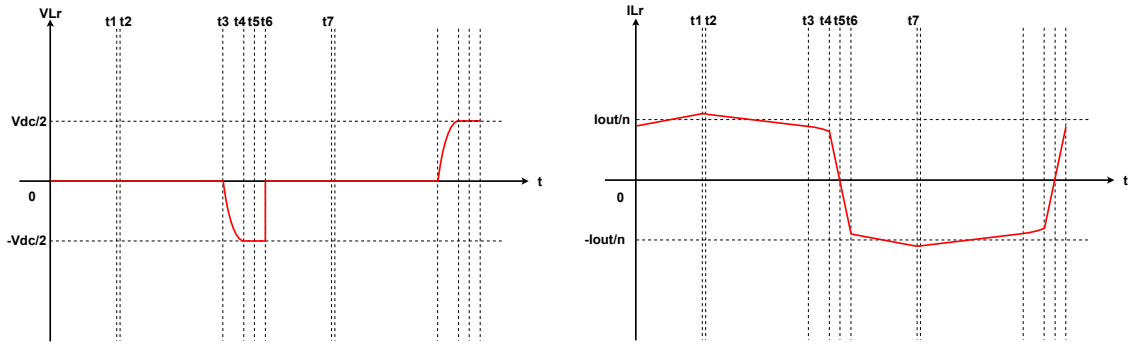

Figure 2.19: Resonant inductance voltage and current in T-Type

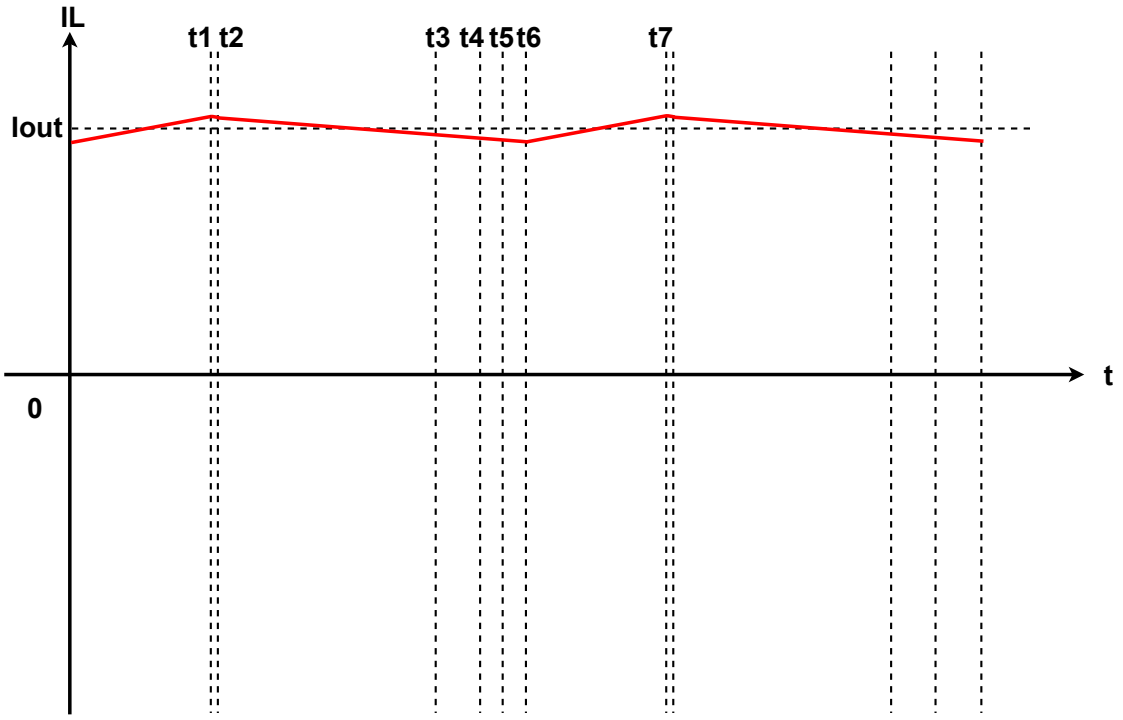

Figure 2.20: Output filter current in T-Type

2.2.2 Resonant inductance

To achieve soft switching, an inductance which represents the external inductor, should be connected in series with the leakage inductance of the transformer, they form the total resonant inductance together. The value of the resonant inductance influences the performance of the circuit a lot.
Use stage ***D*** in section 2.2.1 as example. If the ZVS turning on of S_2 is expected, the voltage on S_2 must reach 0V before the primary side current reaches 0A [4]. Which means that at the time that the resonance starts (t_3), the inductive energy stored in the resonant inductance must be higher than the capacitive energy stored in the parasitic capacitances C_1 & C_2 & C_3. Which is:

$$\begin{aligned} W_{ind} &> W_{cap} \\ \frac{1}{2}L_r {i_{r.int}}^2 &> \frac{3}{2}C(\frac{V_{dc}}{2})^2 \end{aligned} \tag{2.5}$$

Here $i_{r.int}$ represents the initial current of the resonance, which is also the final current of the freewheeling stage. Assume S_1 & S_3 & S_3 have the same parasitic capacitance C, and since they all block $\frac{V_{dc}}{2}$ before the resonance, the equation above can be derived. Then from the basics of LC resonance [14], current and voltage equations can be derived:

$$i_r = i_{r.int} cos(\frac{1}{\sqrt{3CL_r}}t) \tag{2.6}$$

$$V_{S_2} = \frac{V_{dc}}{2} - i_{r.int}\sqrt{\frac{L_r}{3C}} sin(\frac{1}{\sqrt{3CL_r}}t) \tag{2.7}$$

It can be seen that Equation 2.7 has two parts, the constant part represents the initial voltage of the resonance, which for S_2 is $\frac{V_{dc}}{2}$, and the sinusoidal part represents the change of voltage during the resonance. Since V_{S_2} must reach 0V after the resonance to promise the ZVS, the sinusoidal part must reach 0 at the end of the resonance, and the time this procedure takes is the resonant time. Figure 2.21 shows when the inductive energy is not enough, the voltage cannot reach 0V after the resonance ends, which results in the losing of ZVS.

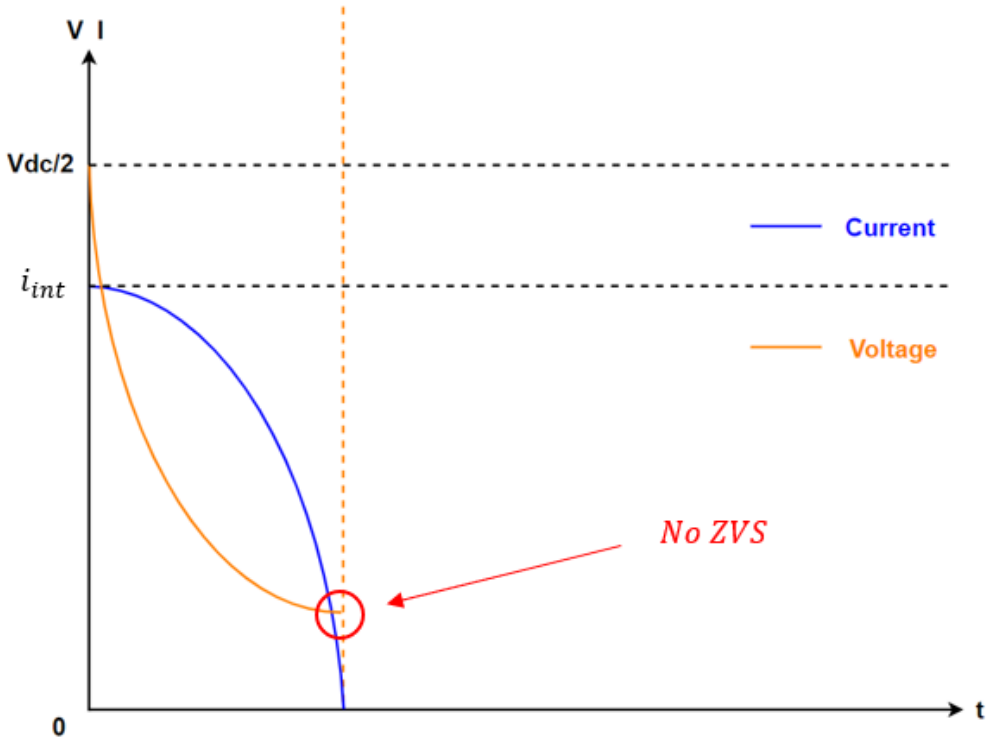

Figure 2.21: Losing of ZVS

For the sinusoidal voltage, it can be seen that $i_{r.int}\sqrt{\frac{L_r}{3C}}$ is its peak. To make sure that V_{S_2} is able to reach 0V, the peak must be not less than $\frac{V_{dc}}{2}$. If the capacitance C is assumed constant, then the requirement for the sinusoidal voltage peak becomes the requirement for resonant inductance L_r and $i_{r.int}$. And according to Equation 2.4, it can be seen that when L_r is high, the slope of the freewheeling current becomes smaller because i_{int} and $R_{ds(on)}$ are constant, so the freewheeling ends at a higher $i_{r.int}$ and it gives a higher sinusoidal voltage peak. So the sinusoidal voltage peak can be seen as only relevant to resonant inductance L_r.

When a larger resonant inductance is applied, it not only causes a higher sinusoidal voltage peak, but also causes a longer resonant period, since:

$$\begin{aligned} T_r &= \frac{2\pi}{w_r} \\ &= \frac{2\pi}{\frac{1}{\sqrt{3CL_r}}} \\ &= 2\pi\sqrt{3CL_r} \end{aligned} \tag{2.8}$$

Here the w_r is the angular speed of the resonance, which is from Equation 2.7. By comparing the derivative of the voltage peak of the change of L_r and the derivative of the resonant period of the change of L_r, it can be seen that:

$$\frac{dV_{peak}}{dL_r} \gg \frac{dT_r}{dL_r} \tag{2.9}$$

Which means when L_r increases, the increasing of the sinusoidal voltage peak is dominant, which gives less resonant time and create more margin for ZVS. So from the ZVS aspect, a larger L_r is preferred.
But when L_r is too large, according to Equation 2.4, it causes the freewheeling current decrease very slowly, which causes the rms current of the middle switch as well as its conduction loss to increase. Also according to the description of stage ***E*** in section 2.2.1 , a too large L_r causes the slope of the primary side current in the duty cycle stage to be very small, which means it will take more time for the primary side current to reach the initial value of the next half period, the duty cycle loss time will be enlarged. So from the loss aspect, L_r should not be too large.
How the ZVS and rms current are influenced by different L_r is shown in Figure 2.22. It can be seen that between t_2 and t_3, which is the freewheeling stage, the rms value of the blue curve is the maximum, while that of the green curve is the minimum. Which means that when L_r is larger, the rms current as well as the conduction loss for the middle switch is larger. And for the ZVS, different L_r gives different resonant time. For all the three conditions, the resonance starts from t_3, but the resonant time of them, which is the duration between the common t_3 and three different t_4s, differ from each other. Since the next half period starts at the common time t_6, then shorter resonant time gives longer duty cycle loss, and larger margin for ZVS. This can be seen in Figure 2.22 that the duration between the blue t_4 and the blue t_5, is the ZVS margin for larger L_r, while the duration between the green t_4 and the green t_5 is that of smaller L_r. Even though the green curve gives less rms current in the freewheeling stage, it has too less margin to perform ZVS and the switches might lose ZVS, in the case when the load level is low or when the turn on time of the switch is long. In real case, both of the two aspects should be considered and optimizations should be done to select a proper L_r.
In this thesis, according to the input voltage range and the load current levels required, L_r for soft-switched T-type converter is selected as 1.2μH by optimizing the efficiency in the simulation. L_r of PSFB converter, from fixed design, is 3.5μH. The reason why PSFB converter needs larger inductance is because it has larger resonant voltage (V_{dc}) compared with soft-switched T-type converter ($\frac{V_{dc}}{2}$). The current waveform of a circuit with proper resonant inductance can be seen as indicated at the position of the red curve in Figure 2.22, gives not only enough margin for ZVS but also acceptable rms current level.

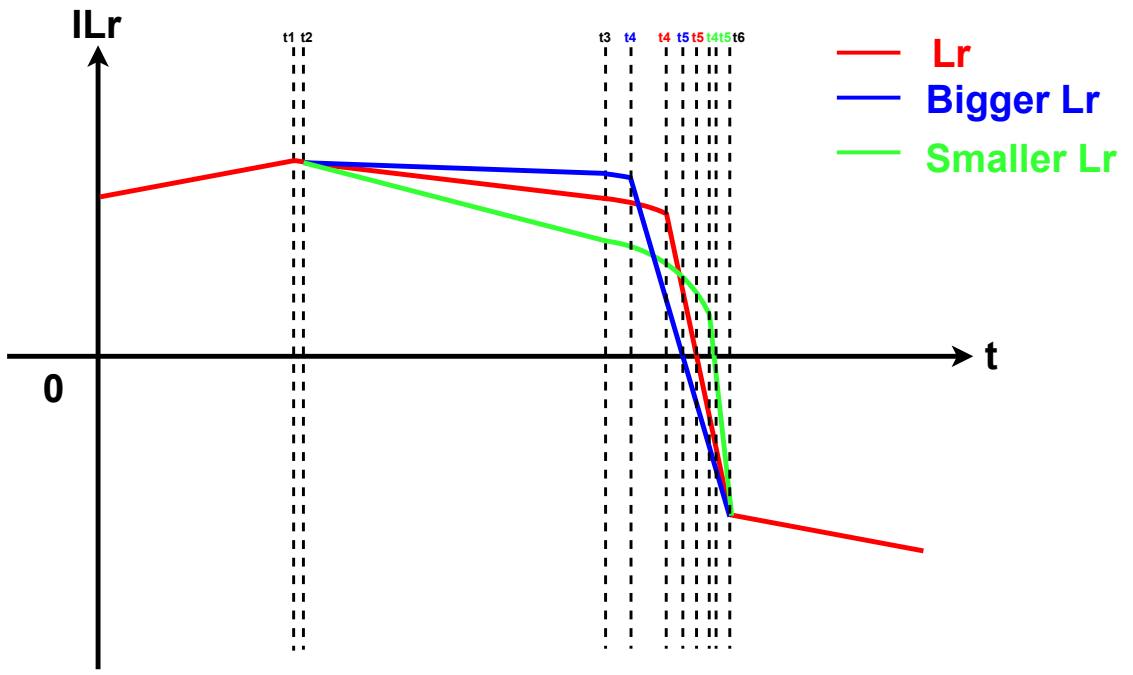

Figure 2.22: Different current for different resonant inductance

2.2.3 Half Bridge T-Type Hard Switch

The schematic of hard-switched T-type converter is very similar to that of soft-switched T-type converter, the only difference is there is no resonant inductor apllied, so at the primary side, the only inductance is the leakage inductance of the transformer, which is L_{lk}, as shown in Figure 2.23.

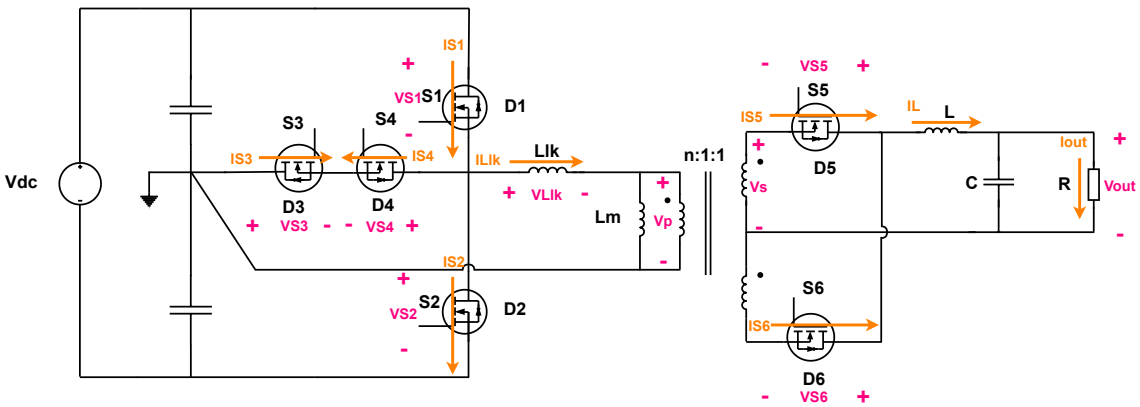

Figure 2.23: Half Bridge T-Type Hard Switch Converter

Since the leakage inductance of the transformer is very small, according to Equation 2.4, during the freewheeling stage, the primary side current decreases very fast (in this case in Equation 2.4, L_r becomes L_{lk}), which causes the freewheeling current ends at a very low value, and the resonance later will start from this value. Which can be seen in Figure 2.24, at t_3.

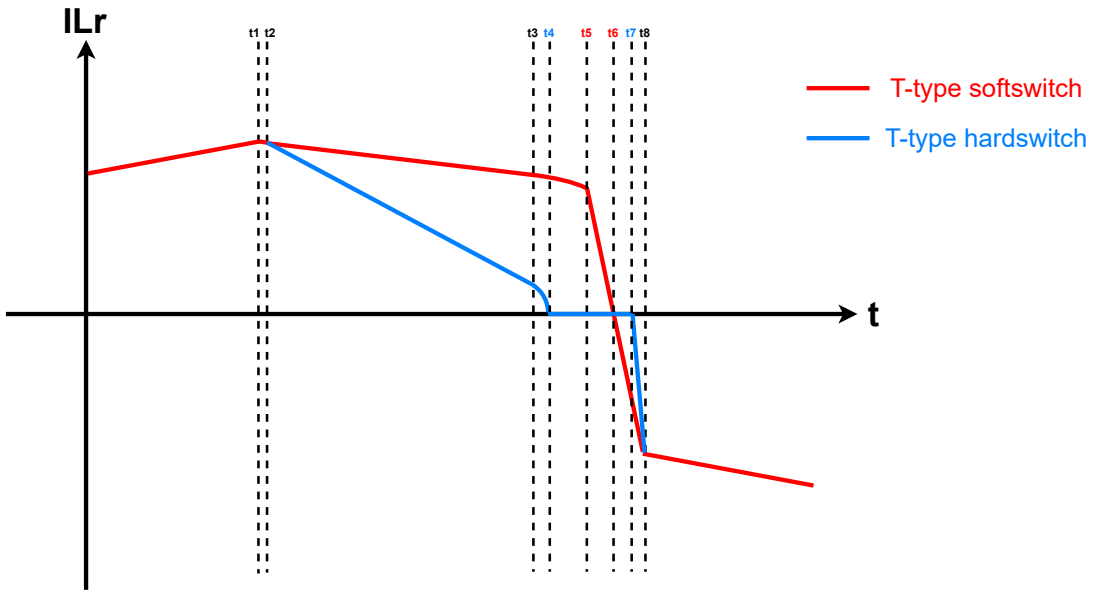

Figure 2.24: Resonant inductance current of T-Type soft switch and hard switch

Since for hard-switched circuit, the resonance starts from a very low initial current and the leakage inductance is very low, the inductive energy

$$W_{ind} = \frac{1}{2} L_{lk} {i_{r.int}}^2 \tag{2.10}$$

of it, is even lower. But the capacitive energy needed by the parasitic capacitances in ZVS case, is fixed, which is:

$$W_{cap} = \frac{3}{2} C \frac{{V_{dc}}^2}{2} \tag{2.11}$$

When the inductive energy becomes lower than the capacitive energy, it means during the resonance, even if the leakage inductance provide all the inductive energy it stored to the parasitic capacitances, they still cannot be fully charged or discharged. The consequence after the resonance then will be: the primary side current reaches to 0A after the resonance, but the voltage on the switch which is going to be turned on (assume this switch is S_2) does not reach to 0V yet, which can be seen in Figure 2.25, at t_4.

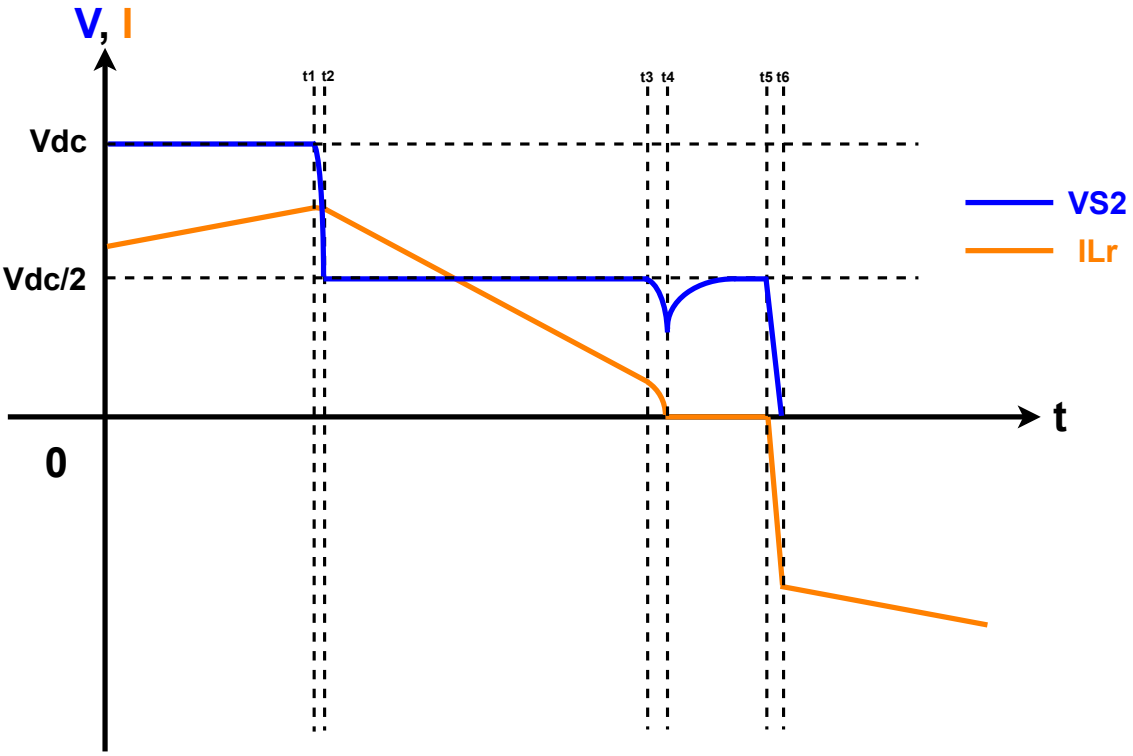

Figure 2.25: Voltage of S2 and resonant inductance current

Then, the primary side current remains at 0A, and the voltage on S_2 will be gradually charged towards $\frac{V_{dc}}{2}$, while the voltage on S_1 will be gradually discharged towards $\frac{V_{dc}}{2}$ since they are connected to the voltage source which value is V_{dc}. In most of the cases they will not reach $\frac{V_{dc}}{2}$ before the turning on, here for simplicity, assume they all reached $\frac{V_{dc}}{2}$ before the turning on, which is t_5. At t_5, S_2 is turned on, current will flow through S_2 and it will increase to the initial value of the next half period, while the voltage on it will decrease from $\frac{V_{dc}}{2}$ to 0V, the switching loss then appears, between t_5 and t_6.

The procedure discussed above barely happens, actually. It happens only when the circuit is at the boundary of ZVS and hard switching. But it shows how a soft-switched T-type converter transfers to hard-switched T-type converter when L_r decreases. Which also shows the essence of hard-switched T-type converter: the hard-switched T-type converter is basically just a "soft-switched T-type converter" with low "resonant inductance". In most of the cases, the primary side current reaches to 0A much earlier than t_3. Then V_{S_2} will remain at $\frac{V_{dc}}{2}$ before the turning on, since no resonance will happen after S_3 is turned off at t_3. Which is as shown in Figure 2.26. Here it can be seen that during $t_3 \sim t_4$ that the resonance should have happened, there is no resonance since the freewheeling current already reached to 0A before t_3, no inductive energy is stored in the leakage inductance. In later sections, if typical hard-switched T-type converter is discussed, for the reason above, this meaningless duration will not be drawn again.

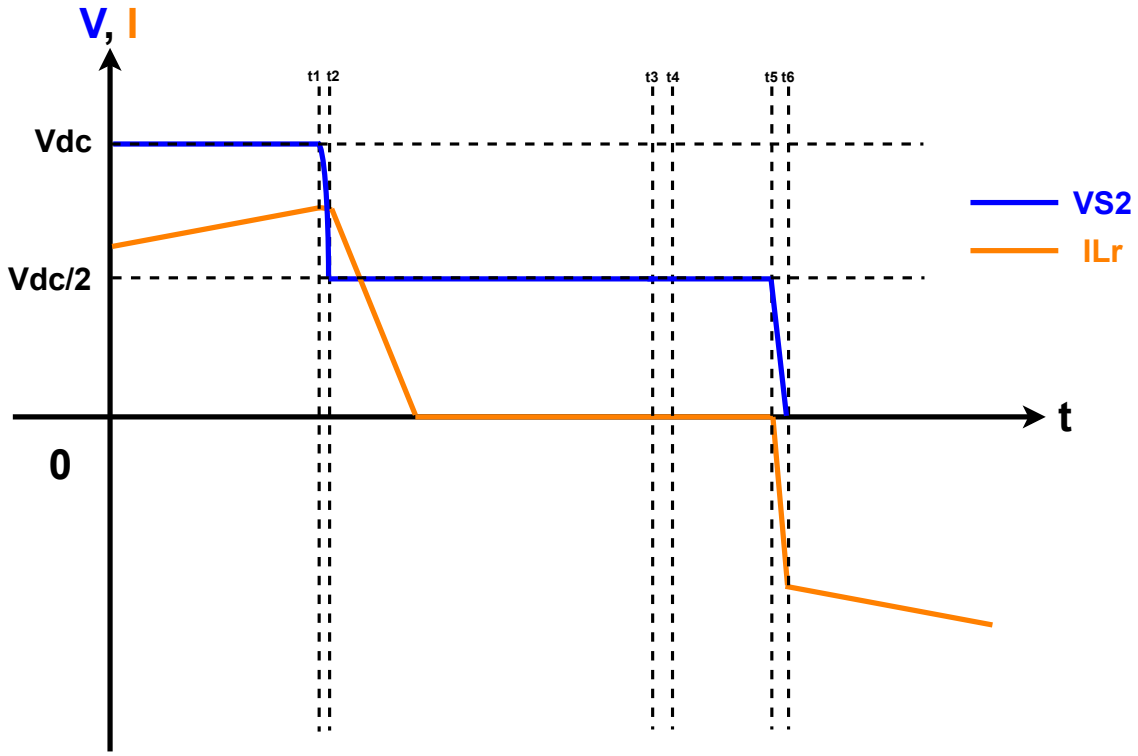

Figure 2.26: Voltage of S2 and resonant inductance current

Then two characteristics of hard-switched T-type converter can be seen. Firstly, due to the low leakage inductance at the primary side, freewheeling current decreases more rapidly compared with soft-switched condition, which causes lower rms current flowing through the middle switches. But the cost, which is the second characteristic, is that during $t_5 \sim t_6$, the main switch will suffer from switching on losses since the voltage on it is not 0V during turning on. And the middle switch of hard-switched T-type converter should be turned on during the energy transfer stage, then for the same reason as soft-switched T-type, it can perform ZVS. Which means the hard switching of hard-switched T-type converter only happens at main switches S_1 & S_2, the middle switches can always perform ZVS. Which can be seen as an advantage of T-type converters.

2.3 Secondary side operation principle

In this thesis, the output of both the PSFB converter and the T-type converters are fixed as the same. Which means the:

Output voltage value V_o

Output current value I_o

are fixed as the same. Further more, according to the requirement that both the PSFB converter and the T-type converters should operate within the same input voltage range and duty cycle value range (this requires the two converters to have different turns ratio, which will be further discussed in 3.1) , it results as:

Duty cycle D

Secondary side input voltage V_s and its waveform
Secondary side current waveform and rms current

for them are all the same. The discussion in this section will base on these assumptions and derivations above, and use the parameters of PSFB converter as reference.

A.Energy transfer stage$(0\sim t_1)$ In this stage, since the transformer is transferring energy to the secondary side, the secondary side voltage is then $\frac{V_p}{n} = \frac{V_{dc}}{n}$. The voltage on S_5 is 0V while the voltage on S_6 is $\frac{2V_{dc}}{n}$. This will cause S_6 be reversely biased and only S_5 will conduct. The voltage on the output filter inductor is $\frac{V_{dc}}{n} - V_o$ so the secondary side current increases linearly with slope $\frac{\frac{V_{dc}}{n} - V_o}{L}$. The equation of the secondary side current in this stage is:

$$\begin{aligned} i_{sec} &= i_{int.sec} + \frac{\frac{V_{dc}}{n} - V_o}{L} t \\ &= I_o - \frac{\frac{V_{dc}}{n} - V_o}{L} \frac{\Delta t_{eff}}{2} + \frac{\frac{V_{dc}}{n} - V_o}{L} t \end{aligned} \tag{2.12}$$

Here $i_{int.sec}$ is the initial current of the secondary side at the energy transfer stage, which value is $I_o - \frac{\frac{V_{dc}}{n} - V_o}{L} \frac{\Delta t_{eff}}{2}$, and Δt_{eff} is the effective duty cycle time, which is the duration of energy transferring.

B.Resonant stage$(t_1 \sim t_2)$ After t_1, at the primary side the main switch is turned off and resonance happens. According to 2.1.1, the voltage on the primary side will decrease from V_{dc} to 0V. This causes the secondary side voltage decreases from $\frac{V_{dc}}{n}$ to 0V so the slope of the secondary side current decreases from $\frac{\frac{V_{dc}}{n} - V_o}{L}$ to $\frac{-V_o}{L}$, the secondary side current will firstly increase to its peak with a decreasing slope and then decrease a little bit with an increasing slope. But as mentioned in 2.1.1, since the resonant stage is very short, the change of secondary side current in this stage is negligible.

C.Freewheeling stage$(t_2 \sim t_3)$ After the resonance ends, the voltage on the primary side of the transformer reaches to 0V, so the voltage on the secondary side reaches to 0V as well. Both S_5 and S_6 block 0V so both of them conduct, so the secondary side current flows through both of them. In this stage, the voltage on the output filter is $-V_o$, so the secondary side current decreases with slope $\frac{-V_o}{L}$, as shown in Equation 2.13.

$$\begin{aligned} i_{sec} &= i_{int.sec} - \frac{V_o}{L} t \\ &= I_o + \frac{\frac{V_{dc}}{n} - V_o}{L} \frac{\Delta t_{eff}}{2} - \frac{V_o}{L} t \end{aligned} \tag{2.13}$$

Here $i_{sec.int}$ is the initial current of the secondary side at the freewheeling stage, which is also the final value of it in the energy transfer stage. Each of S_5 and S_6 shares half of this current, which is $\frac{I_o}{2} + \frac{\frac{V_{dc}}{n} - V_o}{2L} \frac{\Delta t_{eff}}{2} - \frac{V_o}{2L} t$. As shown in Figure 2.27, indicated by the blue dash line.

Except for half of the secondary side freewheeling current, both S_5 and S_6 take the reflected freewheeling current from the primary side as well. This reflection is added to the freewheeling current calculated above of their each, and the sum will be the

total current of S_5 and S_6. As mentioned in 2.1.1, in the freewheeling stage, the primary side current is:

$$\begin{aligned} i_{fw} = i_{L_r} =& i_{int}(1 - \frac{2R_{ds(on)}}{L_r}t) \\ =& (\frac{I_o}{n} + \frac{\frac{V_{dc}}{n} - V_o}{Ln} \cdot \frac{\Delta t_{eff}}{2})(1 - \frac{2R_{ds(on)}}{L_r}t) \end{aligned} \tag{2.14}$$

So both S_5 and S_6 share half of this current. One thing needs to be mentioned is, due to the current direction, for one of the two switches, this half primary side current performs as the gain, while for the other one it performs as the reduction. For example, if in one half cycle, in the freewheeling stage i_{S_5} is equal to:

$$i_{S_5} = \frac{I_o}{2} + \frac{\frac{V_{dc}}{n} - V_o}{2L}\frac{\Delta t_{eff}}{2} - \frac{V_o}{2L}t + \frac{(\frac{I_o}{n} + \frac{\frac{V_{dc}}{n} - V_o}{Ln} \cdot \frac{\Delta t_{eff}}{2})(1 - \frac{2R_{ds(on)}}{L_r}t)}{2} \tag{2.15}$$

Then i_{S_6} must be:

$$i_{S_6} = \frac{I_o}{2} + \frac{\frac{V_{dc}}{n} - V_o}{2L}\frac{\Delta t_{eff}}{2} - \frac{V_o}{2L}t - \frac{(\frac{I_o}{n} + \frac{\frac{V_{dc}}{n} - V_o}{Ln} \cdot \frac{\Delta t_{eff}}{2})(1 - \frac{2R_{ds(on)}}{L_r}t)}{2} \tag{2.16}$$

D.Resonant stage$(t_3 \sim t_4)$ After t_3, the primary side reaches to resonant stage, but since the primary side remains at 0V, the operation in the secondary side does not change and the secondary side current keeps freewheeling.

E.Duty cycle loss stage$(t_4 \sim t_6)$ In the duty cycle loss stage, same as in the resonant stage before, since the primary side voltage keeps being 0V, at the secondary side, current keeps freewheeling. After t_6, the circuit will reach to the next half cycle and energy transferring starts again, then S_5 will be blocked and only S_6 will conduct. Then all the procedures above repeats.

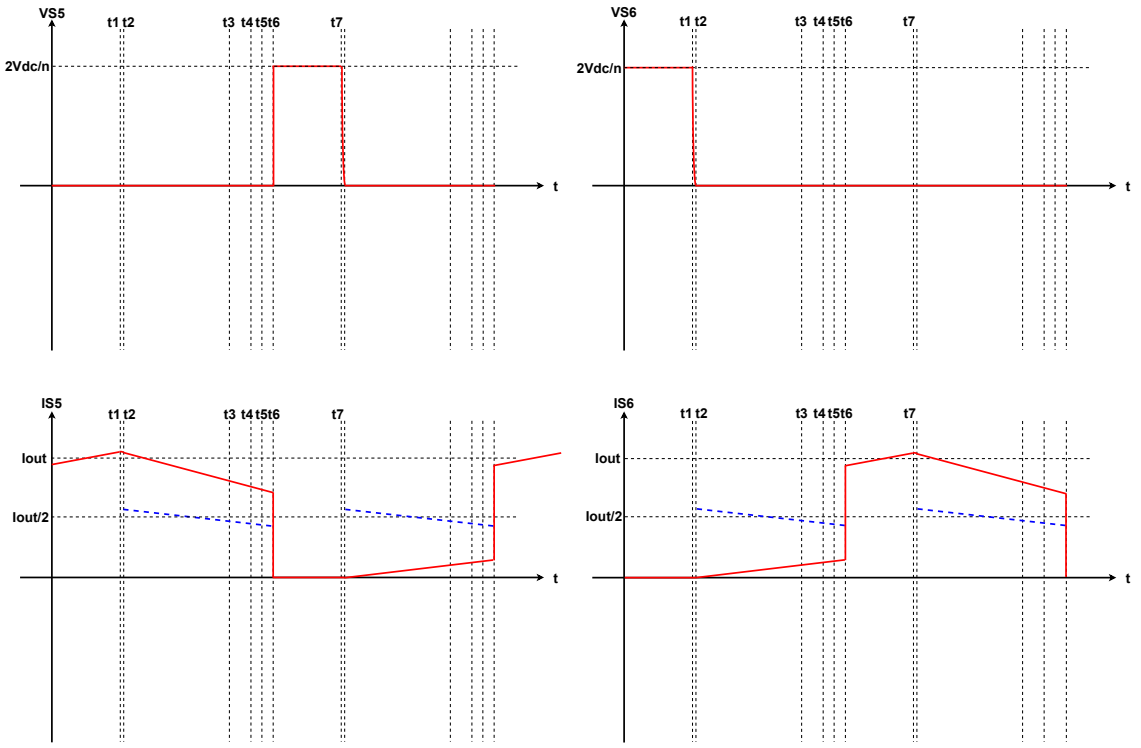

Figure 2.27: Secondary switches voltage and current

3

Theoretical comparisons between different topologies

In this section, theoretical comparisons between PSFB converter, soft-switched T-type converter and hard-switched T-type converter in terms of voltage stress, rms current and losses of the MOSFETs will be made. The discussions will be only relevant to primary side MOSFETs since the operating mode and for the secondary sides of them and the outputs of them are fixed as the same.

3.1 Turns ratio

Before starting the comparison relevant to the characteristics of the MOSFETs characteristics, the most important condition, which is the turns ratio of the transformer, must be defined. Since the characteristics of the MOSFETs such as voltage stress, rms current and losses are all relevant to the turns ratio when the output is fixed. The criteria for defining the turns ratio is that the range of the input voltage, for both PSFB converter and T-type converter, should be the same. For isolated buck converters, there is:

$$\begin{aligned} V_o &= \frac{V_p D_{eff} T}{nT} \\ &= \frac{V_p D_{eff}}{n} \end{aligned} \tag{3.1}$$

Here V_p is the voltage on the primary winding of the transformer, D_{eff} is the effective duty cycle, which is the real duty cycle minus the duty cycle loss, as Equation 3.2

$$D_{eff} = D - D_{loss} \tag{3.2}$$

And n is the turns ratio. For making the two topologies operate within the same input voltage range, regardless of duty cycle loss, the D_{eff} of them must be kept the same. For PSFB converter, during the energy transfer stage, V_p is equal to V_{dc}, but for T-type converter, V_p is $\frac{V_{dc}}{2}$ during energy transfer stage, and since V_o is fixed, then:

$$\begin{aligned} \frac{V_{dc} D_{eff}}{n_{PSFB}} &= \frac{\frac{V_{dc}}{2} D_{eff}}{n_{T-type}} \\ n_{PSFB} &= 2 n_{T-type} \end{aligned} \tag{3.3}$$

It can be seen that according to the design criteria, the turns ratio of PSFB converter should be two times of that of T-type converter. In this thesis the turns ratio for PSFB converter is fixed as 10:1, $n_{PSFB} = 10$, which means the turns ratio for T-type converter is 5:1, n_{T-type}=5, and it is identical for both hard-switched T-type converter and soft-switched T-type converter.

3.2 Voltage stress

3.2.1 PSFB converter

For PSFB converter, according to the schematic and the operating sequence, define the leg at which S_3 and S_4 are the leading leg, while the leg at which S_1 and S_2 are the lagging leg. For each leg, only one of the two switches will be analyzed since the other one does exactly the same operation in the next half cycle. The same way will be applied when the rms current and the losses be analyzed in later subsections, since two half cycles are always symmetrical.
Analyze S_1 & S_4. According to 2.1.1, during stage ***A***, both S_1 & S_4 are conducting, the voltage on them are both 0V. After t_1 at when S_4 is turned off, V_{S_4} will be charged to V_{dc} during stage ***B*** and will remain at V_{dc} before S_3 is switched off in the next half cycle, as shown in Figure 3.1.

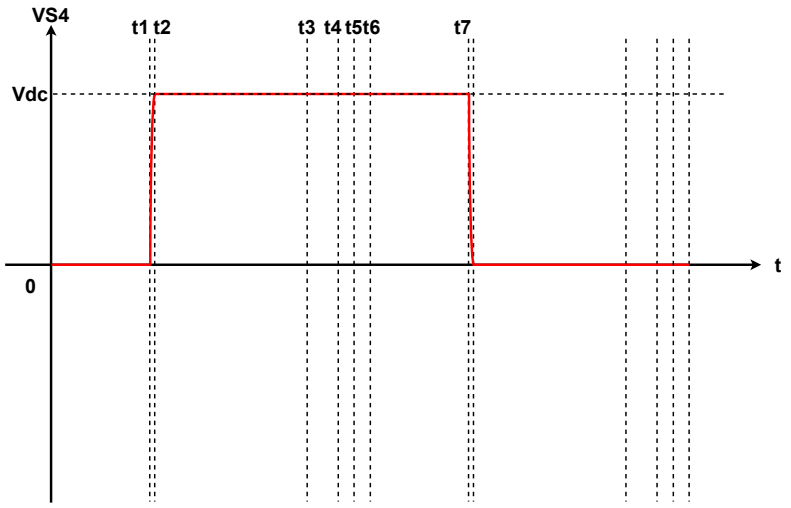

Figure 3.1: Voltage of S4 for PSFB converter

During freewheeling stage $t_2 \sim t_3$, since S_1 is still conducting, the voltage on it remains at 0V. After t_3 at when S_1 is turned off, V_{S_1} will be charged to V_{dc} during stage ***D*** and will remain at V_{dc} before S_2 is switched off in the next half cycle, as shown in Figure 3.2. It can be seen that S_1 takes more time to be charged from 0V to V_{dc}, this is due to the absence of L_m during the resonance in stage ***D***, as specified in 2.1.1.

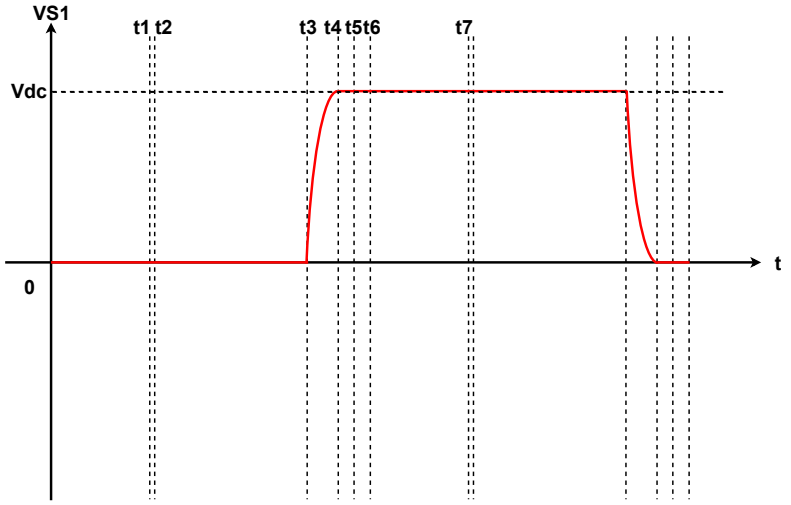

Figure 3.2: Voltage of S1 for PSFB converter

And the voltage waveform of S_3 & S_2 are shown in Figure 3.3 & Figure 3.4. It can be seen that they are symmetrical with those of S_4 & S_2.

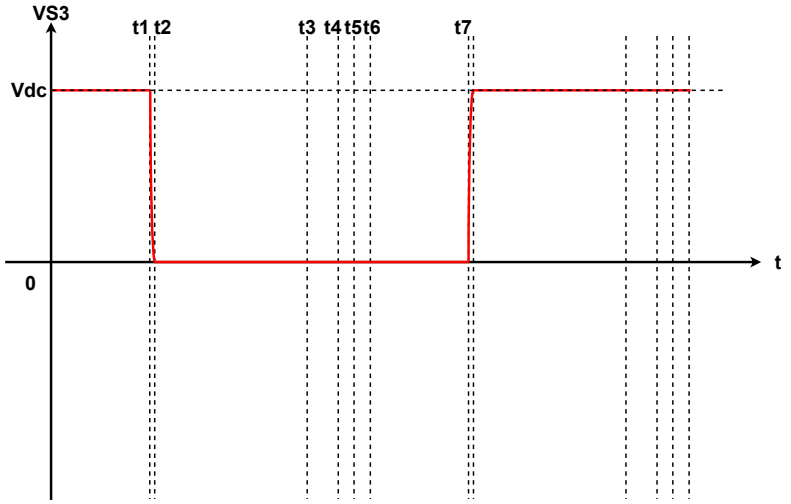

Figure 3.3: Voltage of S3 for PSFB converter

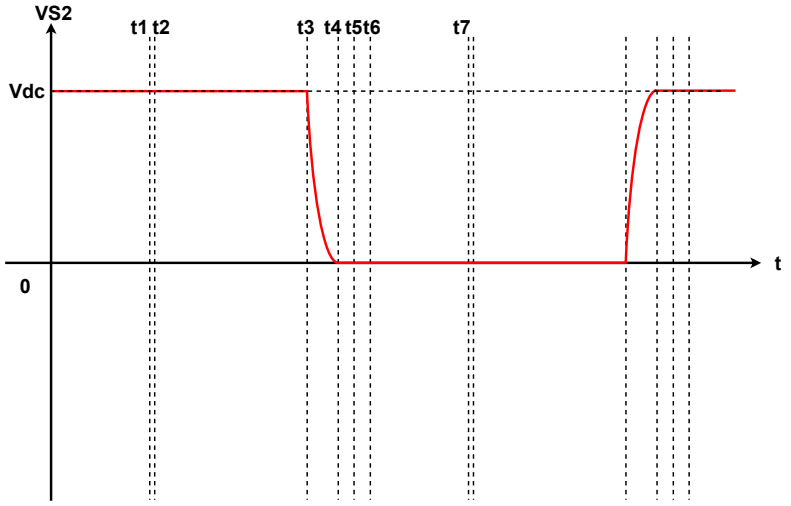

Figure 3.4: Voltage of S2 for PSFB converter

And the conclusion about the voltage stress of the PSFB converter can be made: the voltage stress for the primary side MOSFETs of the PSFB converter are all identical, which is V_{dc}.

3.2.2 Soft-switched T-type converter

For T-type converter, according to the schematic, define the leg at which S_1 & S_2 locate as the main leg, while the leg at which S_3 & S_4 locate as the middle bridge. For each leg, due to the symmetry, only one switch will be analyzed. Here main switches S_1 & S_3 will be analyzed.
According to 2.2.1, during stage ***A***, both S_1 & S_3 are already turned on in the previous duty cycle loss stage. S_1 is conducting so the voltage on it is 0V, and since S_4 blocks $\frac{V_{dc}}{2}$, the voltage on S_3 is also 0V. After t_1 at when S_1 is turned off, the voltage on it will be charged to $\frac{V_{dc}}{2}$ and the primary side current will naturally go through S_3 and the body diode of S_4, so the voltage on it will remain at 0V. At t_3, S_3 is turned off, and freewheeling stage ends, S_1 will be charged to V_{dc}, S_2 will be discharged to 0V and S_3 will be charged to $\frac{V_{dc}}{2}$. In the freewheeling stage and the energy transfer stage of the next half cycle, the voltages on them remain the same. After that, from the first resonant stage of the next half cycle, S_2 and S_4 will operate symmetrically with the procedures above, the change of the voltages on them will be symmetrical with that of S_1 & S_3 in the procedure above as well, and the voltage on S_1 & S_3 will change relatively. As can be seen in Figure 3.5 $\sim$ Figure 3.8. One

thing needs to be specified is that in the freewheeling stage, at the middle leg, one MOSFET and one body diode are conducting. Assume in the first half cycle, in the freewheeling stage, MOSFET S_3 and body diode D_4 are conducting, then in the next half cycle, there will be body diode D_3 and S_4 conducting. So the conclusion is: for soft-switched T-type converter, during the freewheeling stage, the voltage on both of the middle switch is always 0V.

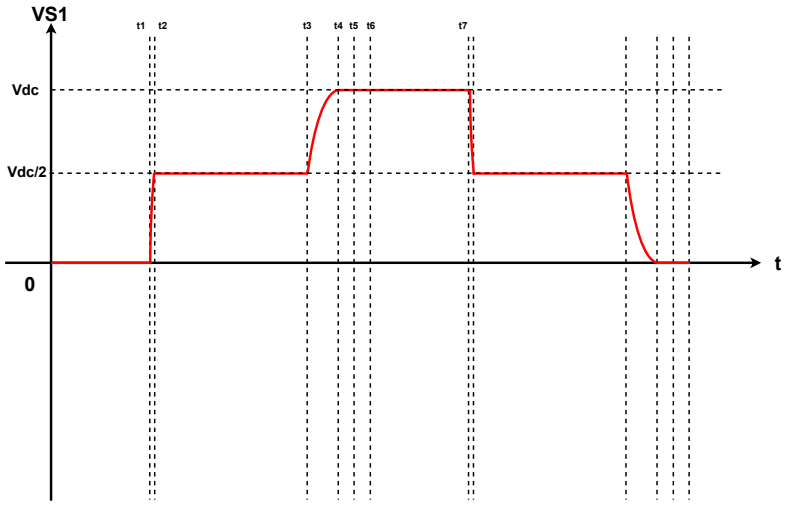

Figure 3.5: Voltage of S1 for soft-switched T-type converter

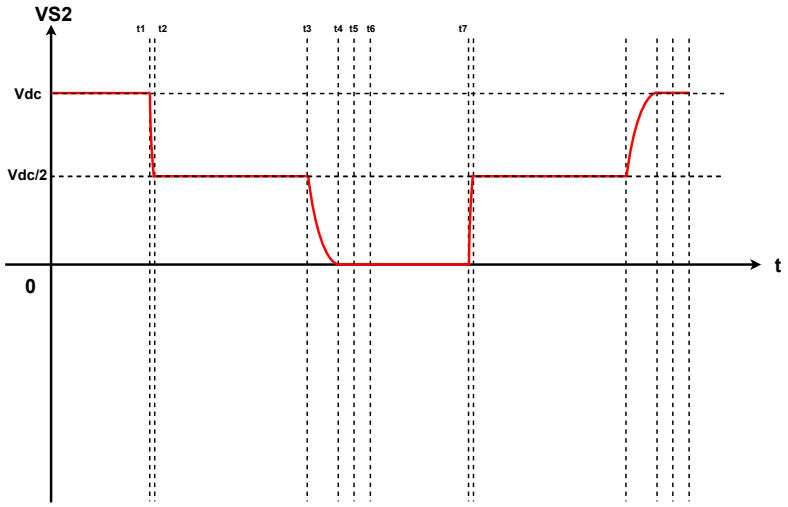

Figure 3.6: Voltage of S2 for soft-switched T-type converter

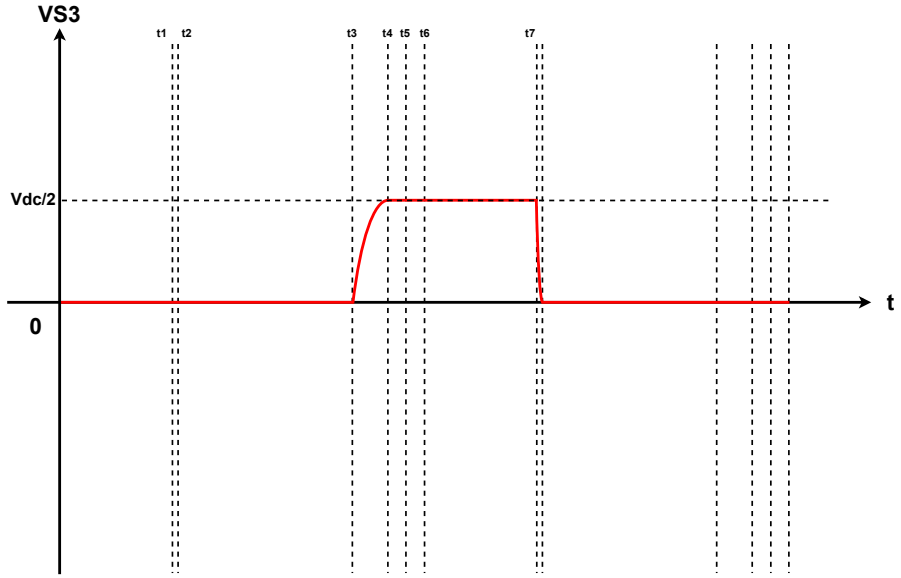

Figure 3.7: Voltage of S3 for soft-switched T-type converter

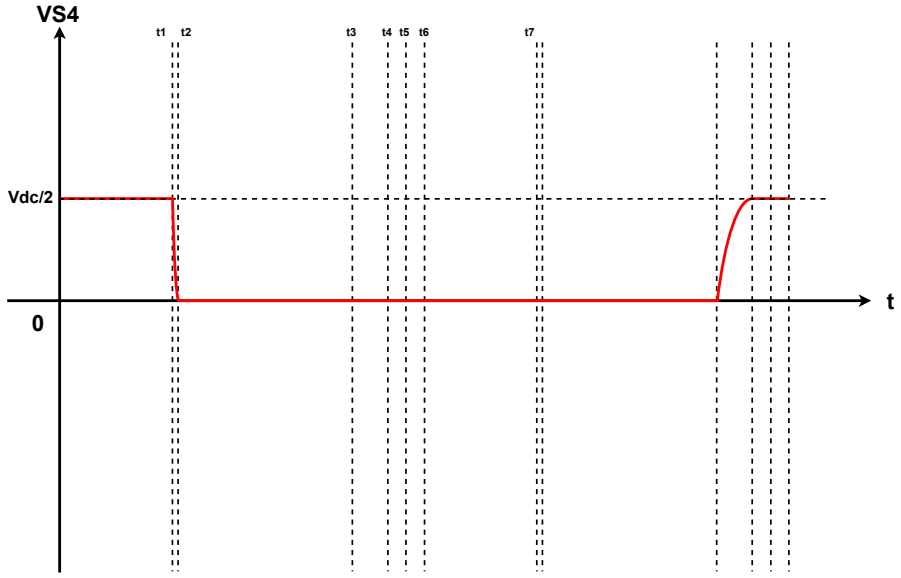

Figure 3.8: Voltage of S4 for soft-switched T-type converter

3.2.3 Hard-switched T-type converter

For hard-switched T-type converter, same as soft-switched T-type, for each leg, only one switch on it will be analyzed. And also same as before, S_1 & S_3 will be analyzed.

Here only the typical hard switching mode, which is similar to which is shown in Figure 2.26, will be considered, the boundary condition like which is shown in Figure 2.25 will not be considered.

For hard-switched T-type converter, before t_3 at which middle switch S_3 is turned off, the voltages on all the switches are exactly the same as those of soft-switched T-type converter. At t_3, S_3 is turned off, different from soft-switched T-type converter, since the primary side current already reached to 0A in the freewheeling stage as specified in 2.2.3, no resonance will happen, so the voltages on all the switches will remain at the same value as before. V_{S_1} & V_{S_2} will remain at $\frac{V_{dc}}{2}$, V_{S_3} & V_{S_4} will remain at 0V. At t_4, S_2 is turned on, so it will perform the turning on characteristic of MOSFET, which is: the voltage on it will decrease to 0V and the current go through it will increase to the initial value of the next energy transfer period. Then according to Kirchhoff's law, V_{S_1} will increase to V_{dc}, V_{S_3} will increase to $\frac{V_{dc}}{2}$. V_{S_4} will remain at 0V since the body diode of it is always conducting during the turning on of S_2. The voltage waveforms of the switches for hard-switched T-type converter are shown in Figure 3.9 $\sim$ Figure 3.12.

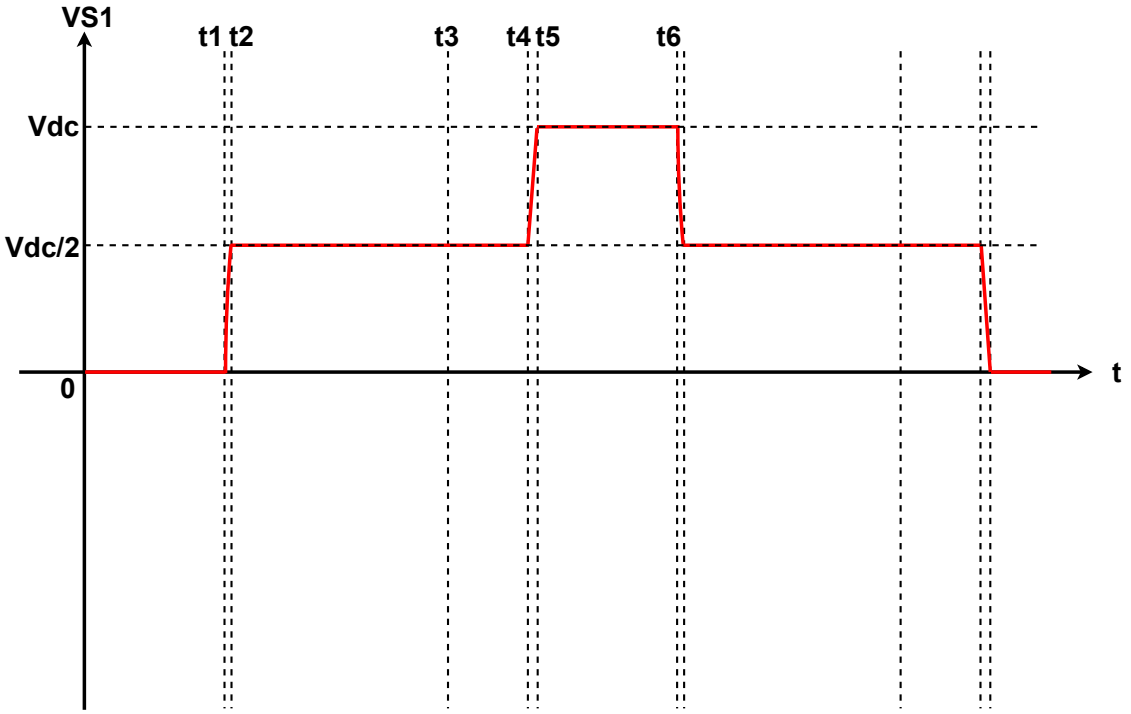

Figure 3.9: Voltage of S1 for hard-switched T-type converter

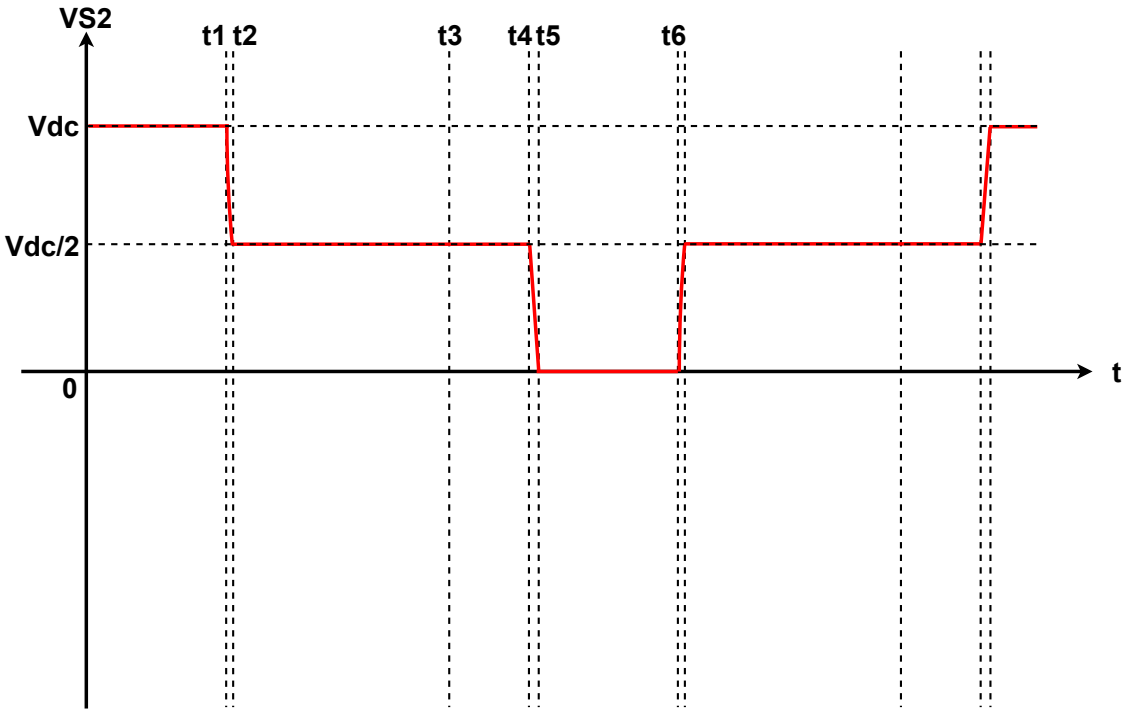

Figure 3.10: Voltage of S2 for hard-switched T-type converter

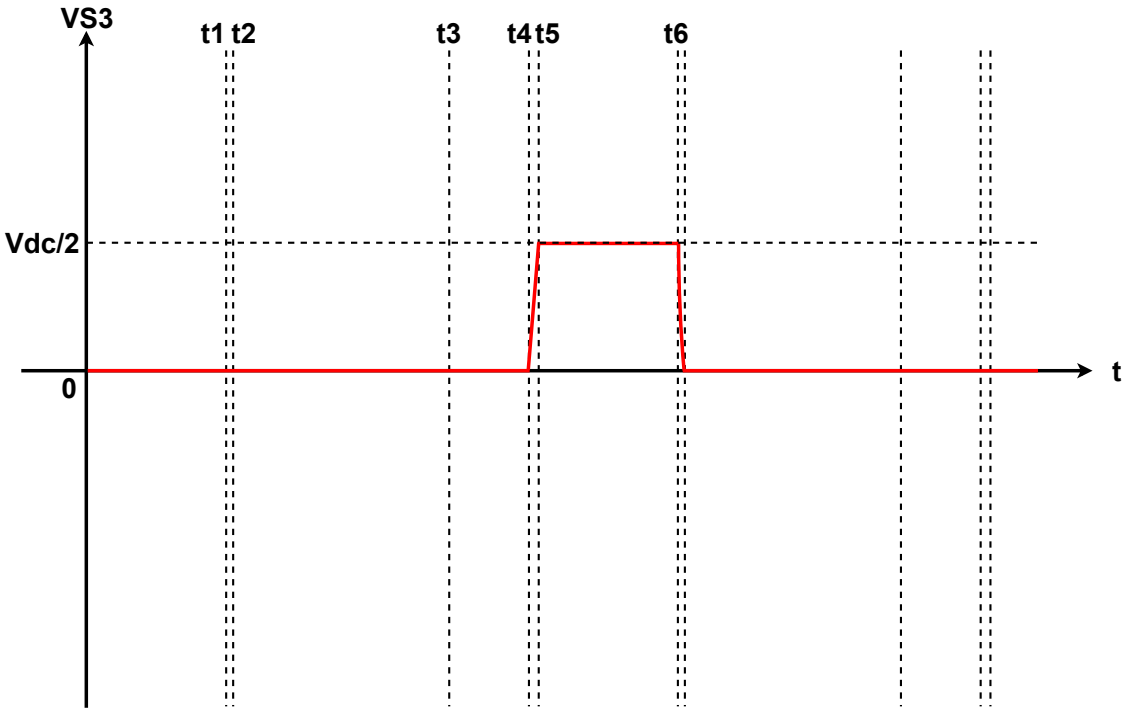

Figure 3.11: Voltage of S3 for hard-switched T-type converter

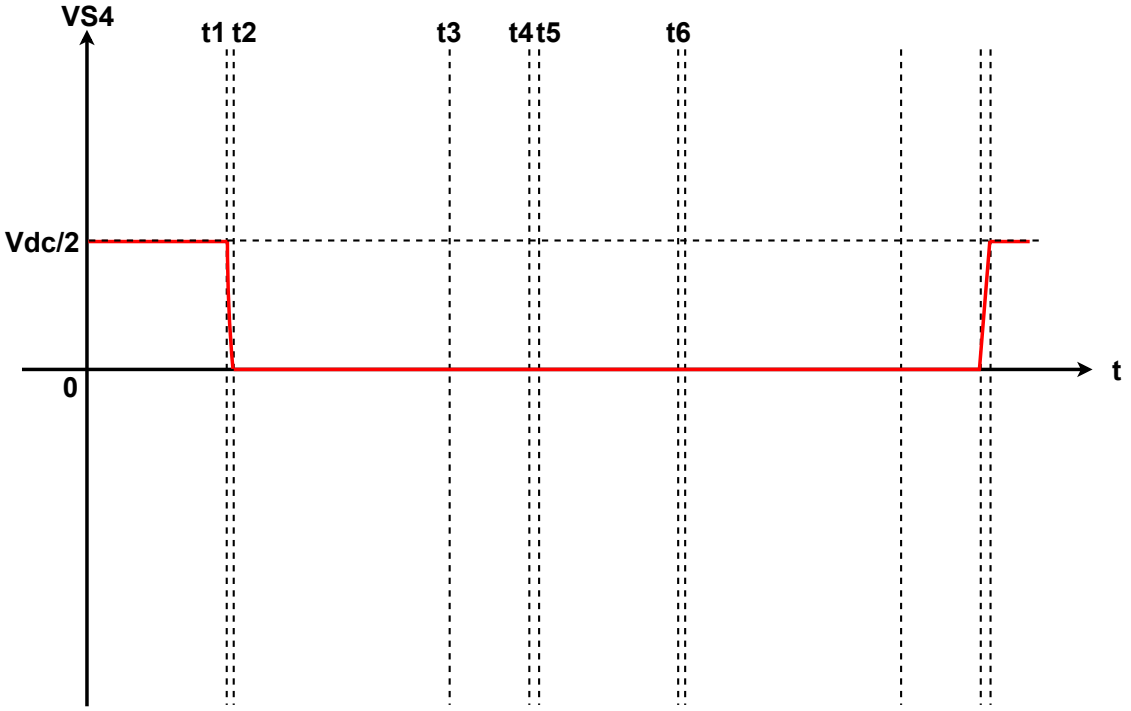

Figure 3.12: Voltage of S4 for hard-switched T-type converter

3.2.4 Comparison between three different topologies in terms of the voltage stress of the MOSFETs

The V_{S_1} & V_{S_4} of PSFB converter and the V_{S_1} & V_{S_3} of soft-switched T-type converter are shown in Figure 3.13. In the Figure, for simplicity and clarity, the resonant time for both of the two circuits are assumed as the same. In other cases they might be different due to the selection of series inductance. It can be seen that, for all the switches in PSFB converter, the maximum voltage stress on them is V_{dc}. And the maximum voltage stress on the main switches of soft-switched T-type converter is V_{dc} as well. But for the middle switches of soft-switched T-type converter, the maximum value is only $\frac{V_{dc}}{2}$. Which means when the soft-switched T-type converter is applied, there is the possibility to use two switches within the four which have lower $V_{DS.max}$. But for PSFB converter, all the four MOSFETs must be able to block V_{dc}, the $V_{DS.max}$ of all of them must be higher than V_{dc}. This gives the first advantage of T-type, which is, by using two switches with lower $V_{DS.max}$ as the middle switches, the cost of total switches can be reduced because the MOSFETs which have lower $V_{DS.max}$ is always cheaper than those have higher $V_{DS.max}$, if they are made by the same material.

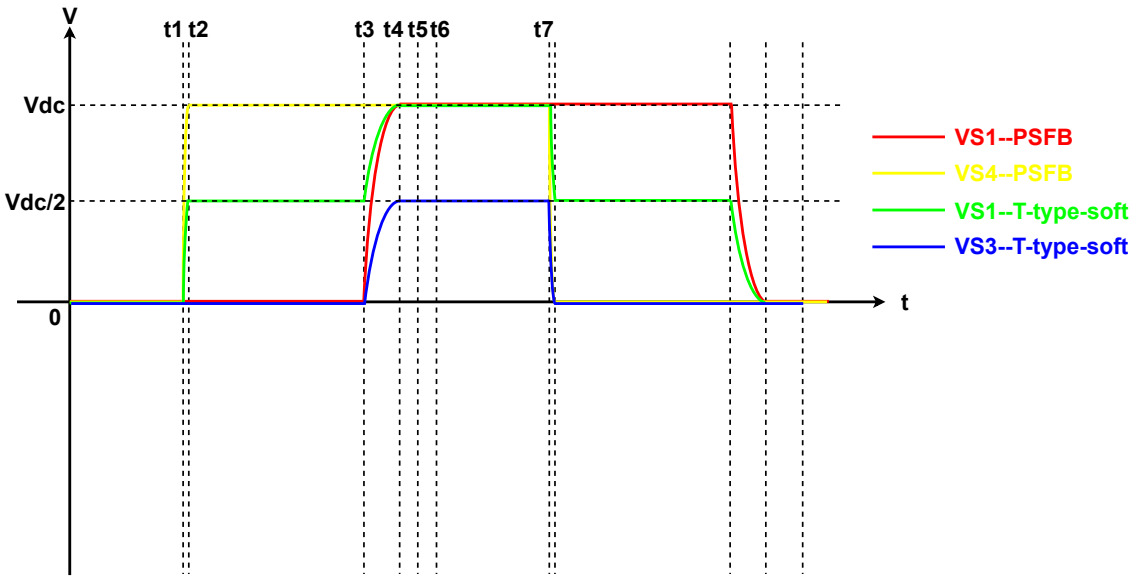

Figure 3.13: Comparison between PSFB and T-Type soft switch about voltage stress

The V_{S_1} & V_{S_3} of soft-switched T-type converter and the V_{S_1} & V_{S_3} of hard-switched T-type converter are shown in Figure 3.14. It can be seen that except for the duration between t_3 and t_7, in the rest part of the whole period, the switches suffer from the same voltage stress. And the point is, since the voltage stress condition of the two topologies are very similar, both the middle switch of soft-switched T-type converter and that of hard-switched T-type converter have the same maximum voltage stress, which is $\frac{V_{dc}}{2}$, then there is no need to compare the voltage stress of hard-switched T-type converter between that of PSFB converter because the same conclusion will be made. So the final conclusion is, from the voltage stress aspect, the T-type converter, no matter it is soft-switched or hard-switched, when compared with PSFB converter, two middle switches within the four will block $\frac{V_{dc}}{2}$, which gives the advantage that some cost can be saved.

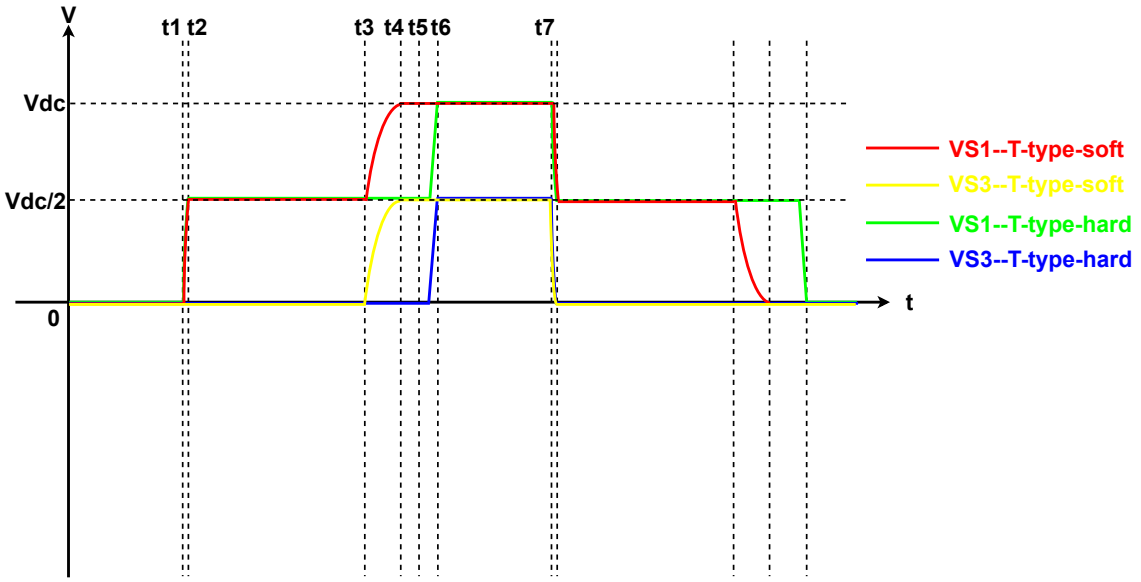

Figure 3.14: Comparison between T-type soft switch and T-Type hard switch about voltage stress

3.3 Current waveform and rms current

3.3.1 PSFB converter

For PSFB converter, same as analyzing the voltage stress, for each leg, only one of the two switches will be analyzed.
Analyze S_1 & S_4, according to 2.1.1, during stage $\boldsymbol{A}$, both S_1 & S_4 are conducting. The current flowing through them is the same, and this current is just the reflection from the secondary side current. In this stage, the voltage on the secondary side filter inductor is $\frac{V_{dc}}{n_{PSFB}} - V_o$, secondary side current increases linearly with slope $\frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{L}$, and since the secondary side average current is output current I_o, then the secondary side current equation in this stage is:

$$i_{sec} = i_L = I_o - \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{L} \cdot \frac{\Delta t_{eff}}{2} + \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{L} \cdot t \tag{3.4}$$

Here Δt_{eff} is the effective energy transfer time, which is the time between 0 and t_1. And the intercept $I_o - \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{L} \cdot \frac{\Delta t_{eff}}{2}$ represents the initial current of the energy transfer stage at the secondary side, $\frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{L}$ is the slope. And since this current is reflected to the primary side through turns ratio n_{PSFB}, the primary side current

is then:

$$i_{pri} = i_{L_r} = \frac{I_o}{n_{PSFB}} - \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{Ln_{PSFB}} \cdot \frac{\Delta t_{eff}}{2} + \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{Ln_{PSFB}} \cdot t \tag{3.5}$$

It can be seen that the current becomes $\frac{1}{n_{PSFB}}$ times of the secondary side current. This current goes through both S_1 and S_4, in stage ***A***.
Then, at t_1, S_4 is turned off, resonant stage happens. S_4 will be charged and S_3 will be discharged, the primary side current is then shared by S_3 and S_4. After S_4 is charged to V_{dc} at t_2, S_4 stops conducting and the resonant stage ends. The circuit reaches to freewheeling stage and the freewheeling current will be taken by S_3 & S_1. So in this stage, i_{S_1} is equal to i_{fw} but i_{S_4} is 0A. And in the next half period, during the freewheeling stage, i_{S_4} will be equal to i_{fw} due to the symmetry. And according to Equation 2.3, i_{fw} is equal to:

$$\begin{aligned} i_{fw} = i_{L_r} =& i_{int}(1 - \frac{2R_{ds(on)}}{L_r}t) \\ =& (\frac{I_o}{n_{PSFB}} + \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{Ln_{PSFB}} \cdot \frac{\Delta t_{eff}}{2})(1 - \frac{2R_{ds(on)}}{L_r}t) \end{aligned} \tag{3.6}$$

Here i_{int}, which value is almost the same as the final value of the energy transfer stage according to 2.1.1, is equal to $\frac{I_o}{n_{PSFB}} + \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{Ln_{PSFB}} \cdot \frac{\Delta t_{eff}}{2}$ derived from Equation 3.5. And Equation 3.6 is also the equation of i_{S_1} in this freewheeling stage and the equation of i_{S_4} in the next freewheeling stage. One thing needs to be mentioned here since the reference direction of the current for each switch is defined as from drain to the source, so for i_{S_3}, in this stage, the direction is negative, as shown in Figure 3.17. So for i_{S_3}, Equation 3.6 describes the characteristic of the magnitude of it. And so does i_{S_4} in the next freewheeling stage.
At t_3, S_1 is turned off so the second resonant stage starts, this time S_1 and S_2 will share the current. And after S_1 is charged to V_{dc}, it stops conducting and S_2 & S_3 will take the linear current in the duty cycle loss stage, according to 2.1.1. The circuit will enter the next half cycle afterwards and the procedure before will repeat symmetrically.
The current waveform of each switch is shown from Figure 3.15 to Figure 3.18.

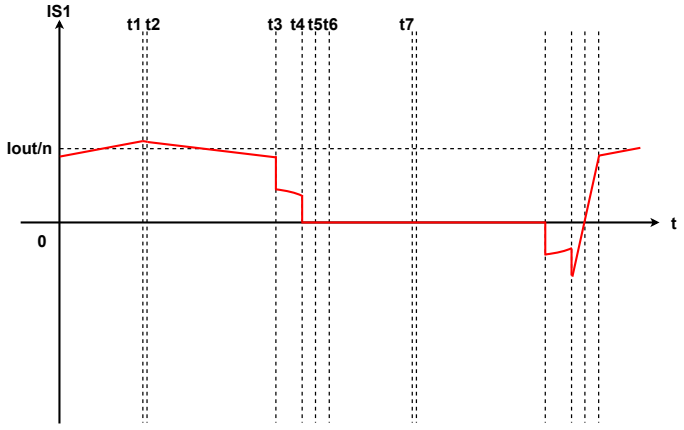

Figure 3.15: Current of S1 for PSFB converter

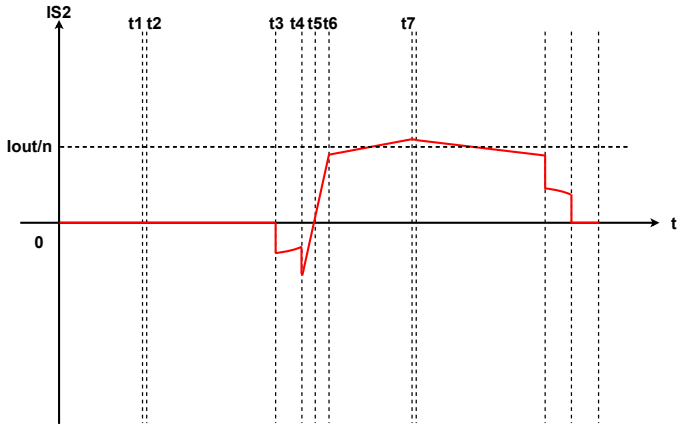

Figure 3.16: Current of S2 for PSFB converter

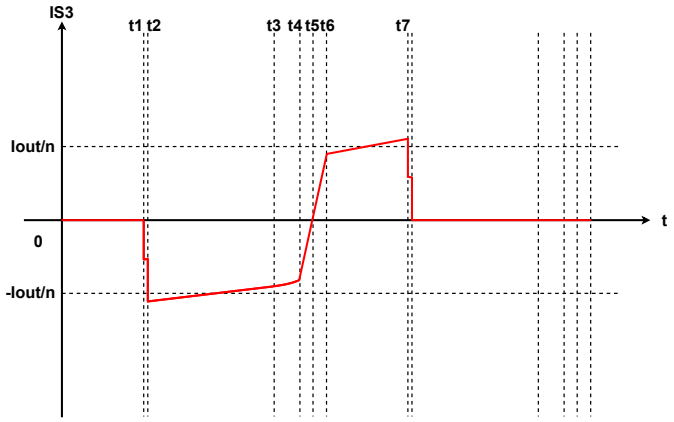

Figure 3.17: Current of S3 for PSFB converter

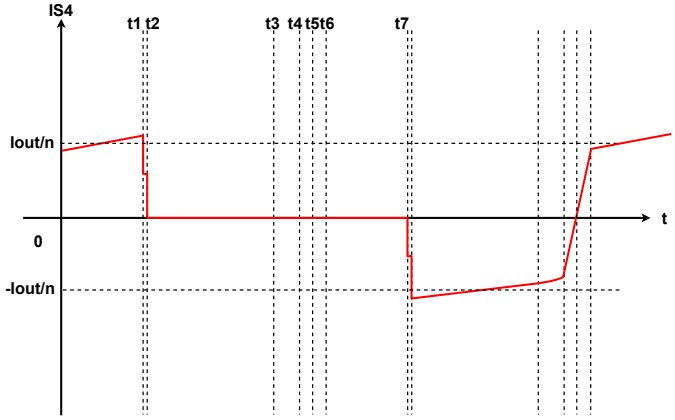

Figure 3.18: Current of S4 for PSFB converter

3.3.2 Soft-switched T-type converter

Analyze S_1 & S_3, according to 2.2.1, during stage $\boldsymbol{A}$, S_1 is conducting. The current flowing through it is the reflection from the secondary side current. Use the same

derivation procedure as discussed in 3.3.1, the primary side current which is also i_{S_1}, is:

$$i_{S_1} = i_{pri} = i_{L_r} = \frac{I_o}{n_{T-type}} - \frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o \cdot \frac{\Delta t_{eff}}{2} + \frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o \cdot t \tag{3.7}$$

Then, after S_1 is switched off at t_1, the resonant stage happens and S_1 & S_2 & S_4 will share the primary side current since it is them that be charged or discharged during this stage. After both V_{S_1} and V_{S_2} reach to $\frac{V_{dc}}{2}$, the resonant stage ends and the freewheeling stage will start. In the freewheeling stage neither S_1 nor S_2 is conducting, S_3 & D_4 is conducting. According to 2.2.1 and the derivation procedure shown in 3.3.1, the freewheeling current, also i_{S_3} & i_{S_4} is then:

$$\begin{aligned} i_{S_3} = i_{fw} = i_{L_r} =& i_{int}(1 - \frac{R_{ds(on)} + R_{diode}}{L_r}t) \\ =& (\frac{I_o}{n_{T-type}} + \frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o \cdot \frac{\Delta t_{eff}}{2})(1 - \frac{R_{ds(on)} + R_{diode}}{L_r}t) \end{aligned} \tag{3.8}$$

Same as the reason be mentioned in 3.3.1, due to the current reference direction definition, for i_{S_4} this equation describes its magnitude, and the direction of i_{S_4} is negative in this stage, and so does the i_{S_3} in the next freewheeling stage, as shown in Figure 3.21 & Figure 3.22. Here i_{int} is derived from Equation 3.7, which value is almost the same as the final value of the energy transfer stage. Then at t_3, S_3 is turned off and the second resonant stage starts, the primary side current is shared by S_1 & S_2 & S_3. Afterwards, the linear current will flow in S_2 during the duty cycle loss. After reach to the next half cycle, the procedure above will repeat symmetrically.

The current waveform of each switch is shown from Figure 3.19 to Figure 3.22.

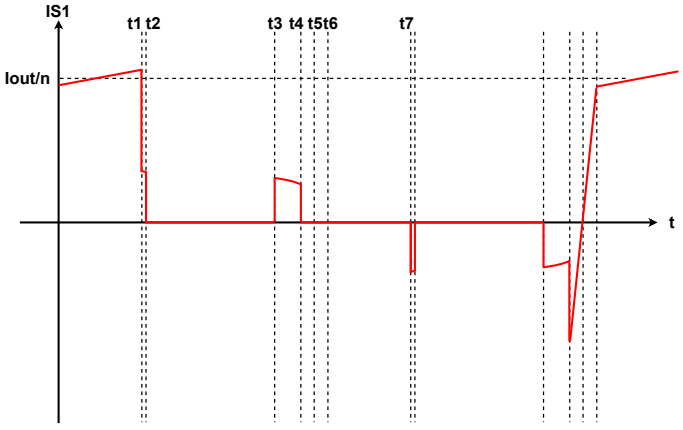

Figure 3.19: Current of S1 for T-Type soft switch converter

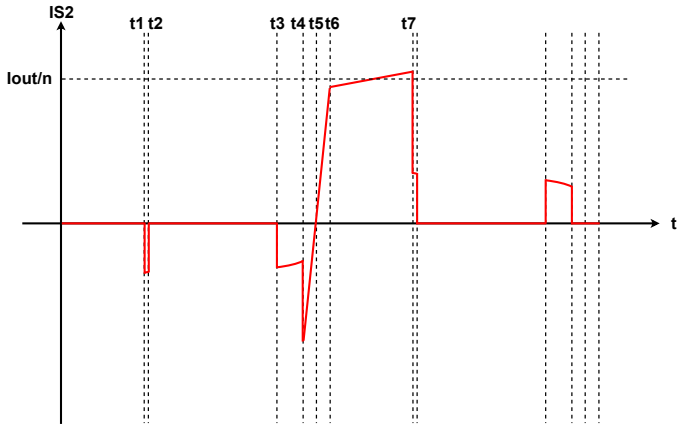

Figure 3.20: Current of S2 for T-Type soft switch converter

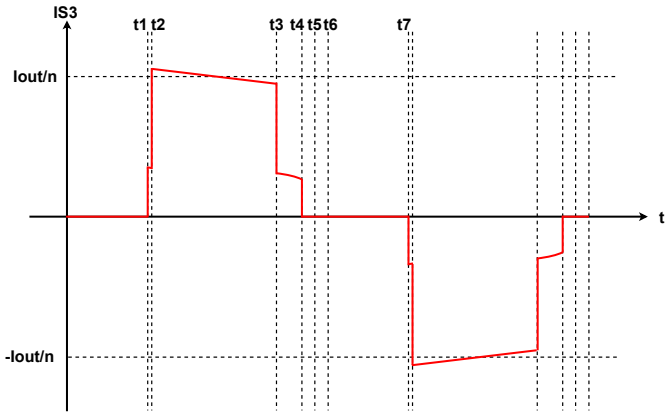

Figure 3.21: Current of S3 for T-Type soft switch converter

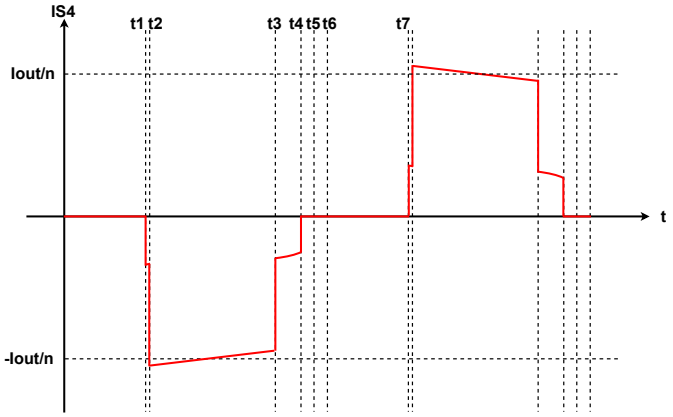

Figure 3.22: Current of S4 for T-Type soft switch converter

3.3.3 Hard-switched T-type converter

Analyze S_1 & S_3 and assume the hard-switched T-type converter is typical. During stage ***A***, since the primary side current as well as the current flowing through S_1,

is just the reflection from the secondary side, so in this stage, the current equation for i_{S_1} is exactly the same as that of soft-switched T-type converter. Which is:

$$i_{S_1} = i_{pri} = i_{L_r} = \frac{I_o}{n_{T-type}} - \frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o \cdot \frac{\Delta t_{eff}}{2} + \frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o \cdot t \tag{3.9}$$

After S_1 is turned off at t_1, the resonant performance is also the same as that that of soft-switched T-type converter, S_1 & S_2 & S_4 share the primary side current. But after the circuit reaches to the freewheeling stage, the difference appears. According to 2.2.3, for hard-switched T-type converter, in the freewheeling stage, since no series inductor is applied, there is only the leakage inductance at the primary side, then Equation 2.4 becomes:

$$\begin{aligned} i_{L_r} =& i_{int}(1 - \frac{R_{ds(on)} + R_{diode}}{L_{lk}}t) \\ =& (\frac{I_o}{n_{T-type}} + \frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o \cdot \frac{\Delta t_{eff}}{2})(1 - \frac{R_{ds(on)} + R_{diode}}{L_{lk}}t) \end{aligned} \tag{3.10}$$

And this equation is also the equation of i_{S_3} and the magnitude of i_{S_4} in this stage. Here the i_{int} is also the same as that of soft-switched T-type converter. But since $L_{lk} < L_r$, the slope of the freewheeling current for hard-switched T-type is larger, which means the freewheeling current of hard-switched T-type decreases faster. And since typical operating mode is considered, the freewheeling current is assumed as will decrease to 0A somewhere during the freewheeling stage. Which is as shown in Figure 3.25. And since there will not be the resonance or any residual current thereafter, there will not be duty cycle loss stage as well. Until t_4, S_2 is switched on, and then S_2 will perform the turning on characteristic of MOSFET, the primary side current which is also i_{S_2}, will increase to the initial current of the next energy transfer stage, the next half cycle will start and everything repeats symmetrically. The current waveform of each switch is shown from Figure 3.23 to Figure 3.26.

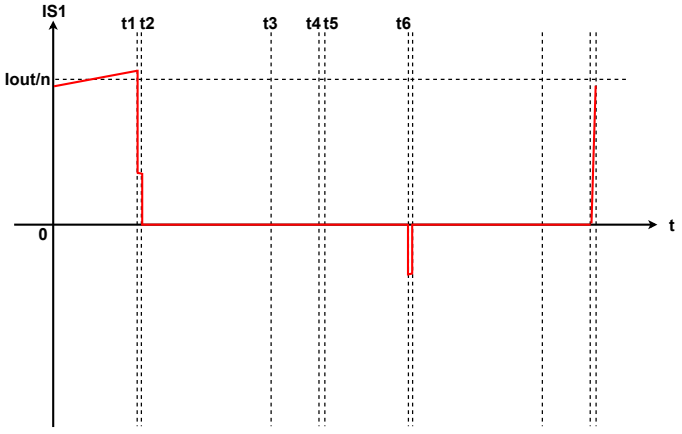

Figure 3.23: Current of S1 for T-Type hard switch converter

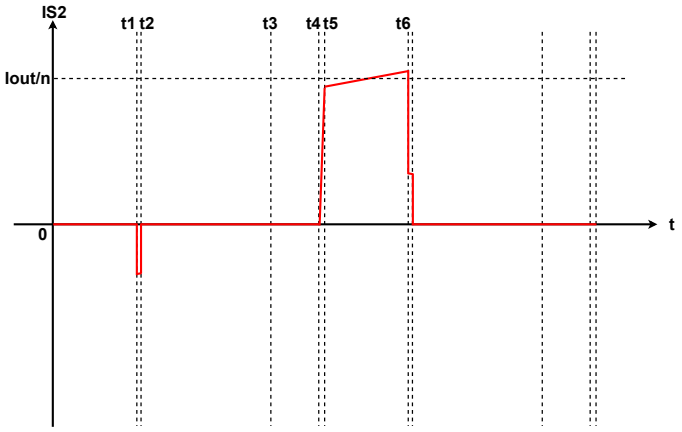

Figure 3.24: Current of S2 for T-Type hard switch converter

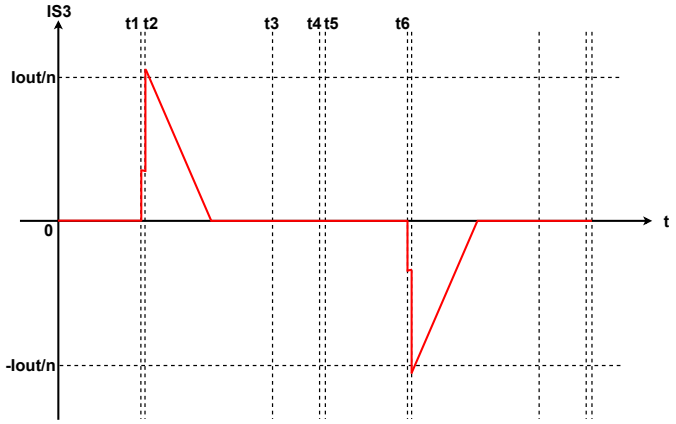

Figure 3.25: Current of S3 for T-Type hard switch converter

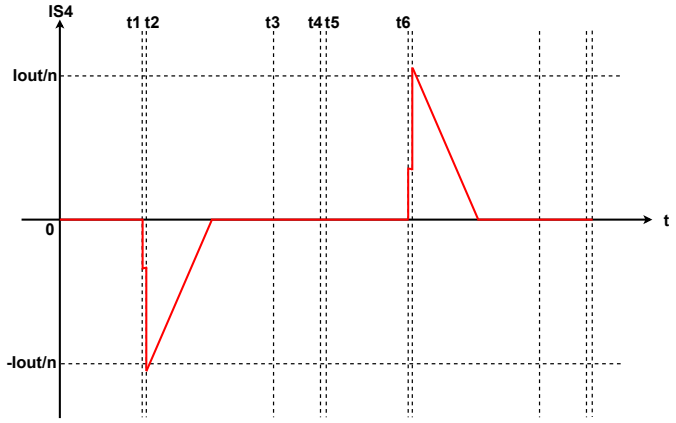

Figure 3.26: Current of S4 for T-Type hard switch converter

3.3.4 Comparison between three different topologies in terms of the current waveform of the MOSFETs

The i_{S_1} & i_{S_4} of PSFB converter and the i_{S_1} & i_{S_3} of soft-switched T-type converter are shown in Figure 3.27. Same as before, assume the resonant time of them are the same. It can be seen from the figure that when the switches of PSFB converter are conducting, the level of the current going through them is always around $\frac{I_o}{2n}$. But for soft-switched T-type converter, this value is always around $\frac{I_o}{n}$. The reason is, according to 3.1, to make PSFB converter and T-type converter operate within the same input voltage range, the turns ratio of PSFB converter must be two times of that of T-type converter, which is:

$$n_{PSFB} = 2n_{T-type} \tag{3.11}$$

This causes in stage ***A***, for T-type converter, the primary side current reflected from the fixed secondary side current, is two times of that of PSFB converter. In Figure 3.27, n represents the turns ratio of T-type converter, and the turns ratio of PSFB converter, is then $2n$. And in the freewheeling stage, since the freewheeling current almost starts from the final value of the energy transfer stage, and in the energy transfer stage the current of T-type converter is always two times of that of PSFB converter, the freewheeling current of soft-switched T-type converter is also around two times of the freerwheeling current of PSFB converter. This gives one disadvantage of soft-switched T-type converter, which is the increase of rms current and the increase of the conduction loss.

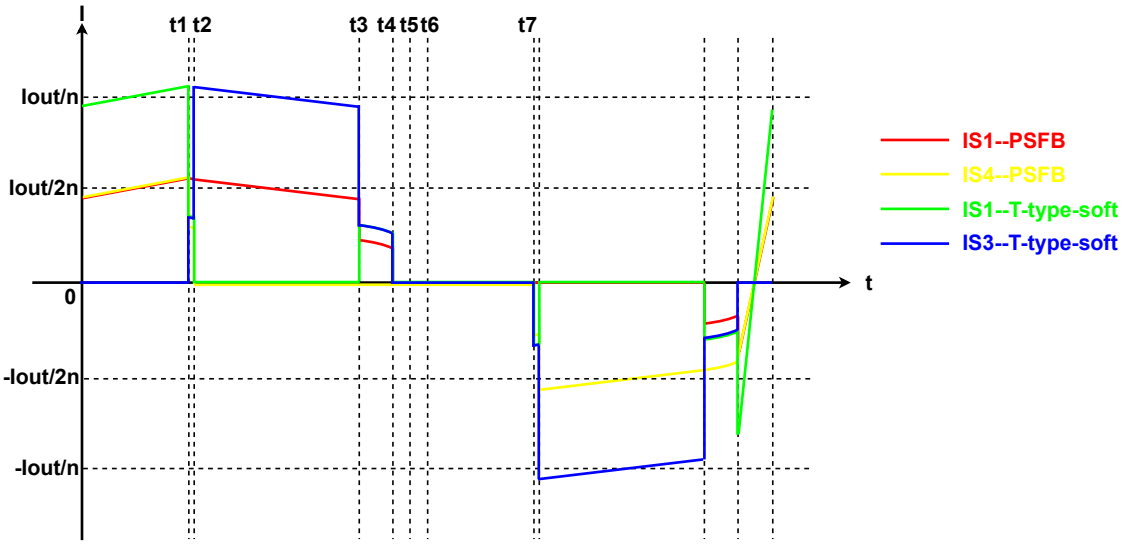

Figure 3.27: Current comparison between PSFB and T-Type soft switch converter

Before comparing PSFB converter with hard-switched T-type converter, the comparison between soft-switched T-type converter and hard-switched T-type converter, about the current waveform, can be done first. As specified in 3.3.3, in the freewheeling stage, due to the small leakage inductance, the freewheeling current for

hard-switched T-type converter decreases faster than that of soft-switched T-type converter, which will make the rms current and the conduction loss of hard-switched T-type lower that that of soft-switched T-type converter, as shown in Figure 3.28.

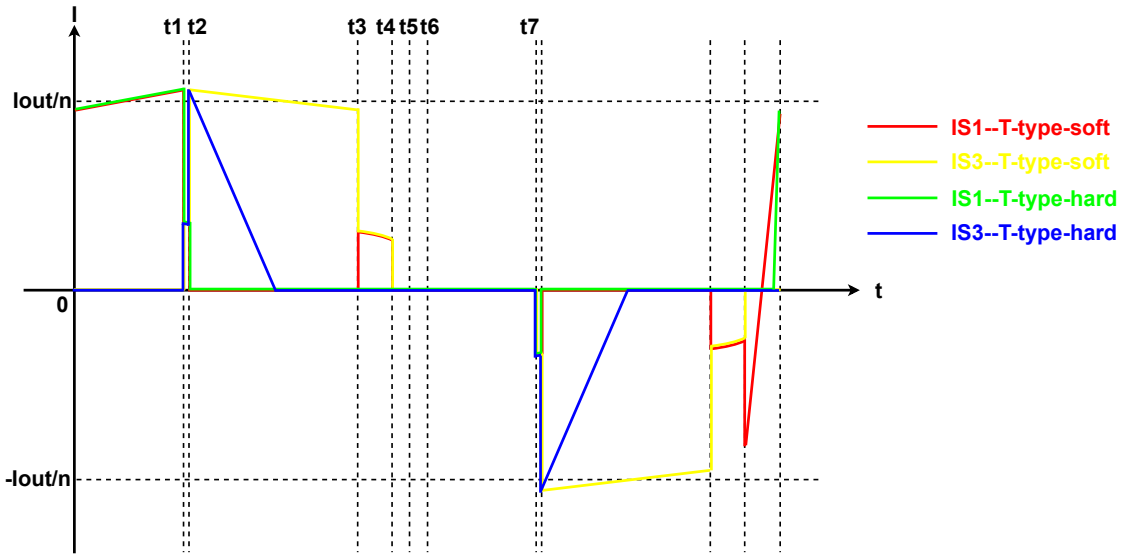

Figure 3.28: Current comparison between T-Type soft switch and T-Type hard switch converter

Then compare the current waveform of hard-switched T-type converter with that of PSFB converter. As can be seen in Figure 3.29, same as soft-switched T-type converter, in the energy transfer stage, the current in the main switch of hard-switched T-type converter is around $\frac{I_o}{n}$ while that of PSFB converter is around $\frac{I_o}{2n}$. But in the freewheeling stage, different from soft-switched T-type converter, the current of hard-switched T-type converter is no longer around $\frac{I_o}{n}$ but decreases rapidly instead. This gives the possibility that hard-switched T-type converter may have lower conduction loss compared with PSFB converter, if the extent of this fast decreasing is high enough.

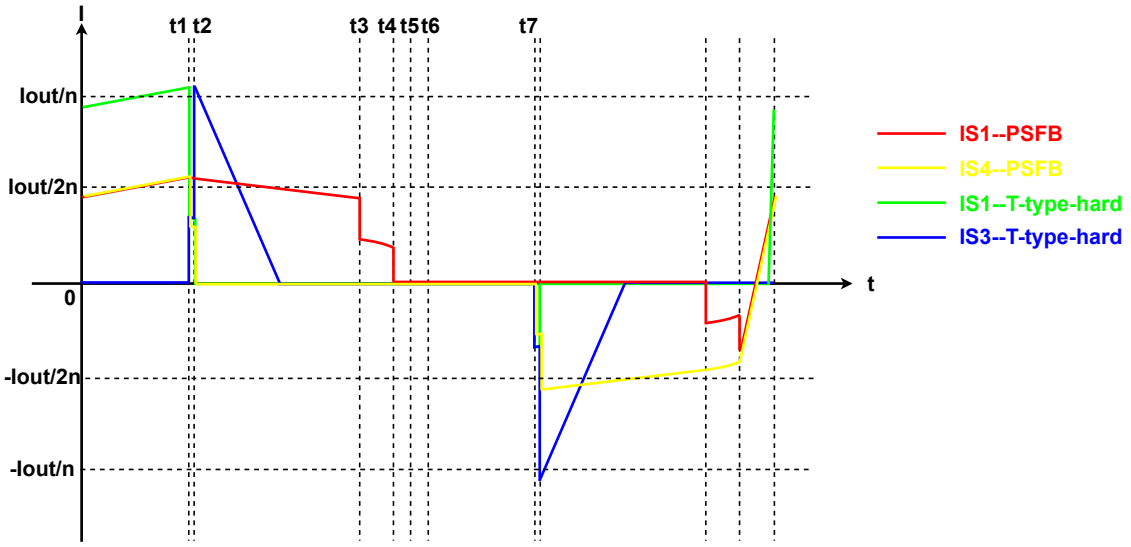

Figure 3.29: Current comparison between PSFB and hard switch converter

3.4 rms current

3.4.1 PSFB converter

For PSFB converter, neglect resonance and duty cycle loss, then according to 3.3.1, the rms current of all the four switches can be calculated as:

$$I_{rms.S_1 \sim S_4} = \sqrt{\frac{1}{T}\left(\int_0^{\Delta t_{eff}} (i_{pri.PSFB})^2\, dt + \int_0^{\Delta t_{fw}} (i_{fw.PSFB})^2\, dt\right)} \tag{3.12}$$

Here $i_{pri.PSFB}$ is Equation 3.5, which is:

$$i_{pri.PSFB} = \frac{I_o}{n_{PSFB}} - \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{Ln_{PSFB}} \cdot \frac{\Delta t_{eff}}{2} + \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{Ln_{PSFB}} \cdot t \tag{3.13}$$

While $i_{fw.PSFB}$ is Equation 3.6, which is:

$$i_{fw.PSFB} = \left(\frac{I_o}{n_{PSFB}} + \frac{\frac{V_{dc}}{n_{PSFB}} - V_o}{Ln_{PSFB}} \cdot \frac{\Delta t_{eff}}{2}\right)\left(1 - \frac{2R_{ds(on)}}{L_r} t\right) \tag{3.14}$$

For the simplicity of calculation, assume the output filter inductance is big enough and the decrease of freewheeling current is small enough, then both the two current can be seen as constant around $\frac{I_o}{2n}$, as shown in Figure 3.30.

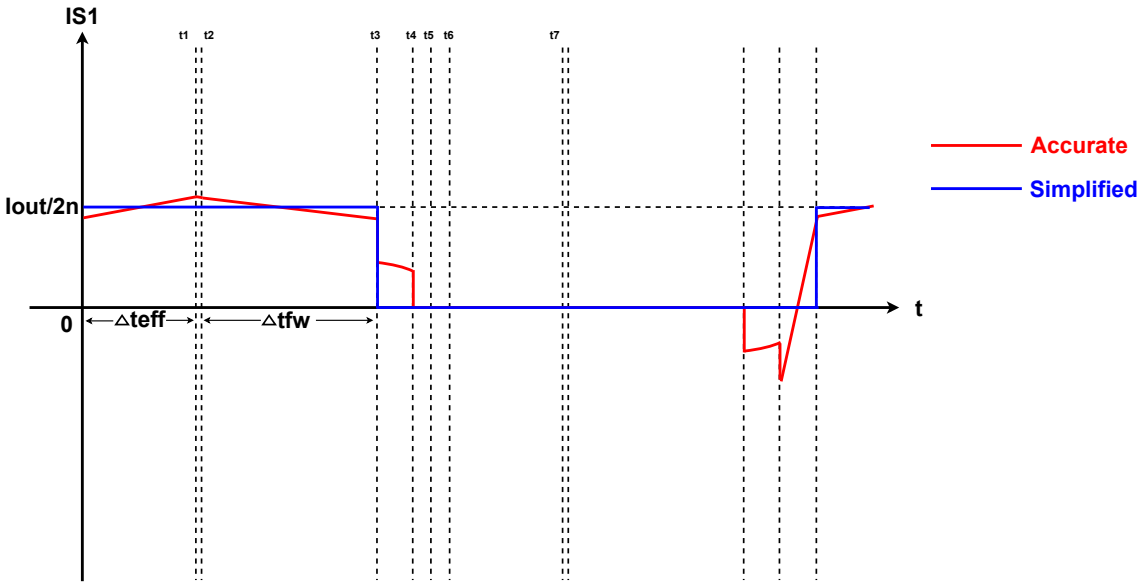

Figure 3.30: Simplified current of S1 for PSFB converter

In Figure 3.30, same as in 3.3.4, n_{PSFB} is represented by $2n$. Then the rms current for all the four switches can be calculated as:

$$\begin{aligned} I_{rms.S_1\sim S_4} &= \sqrt{\frac{1}{T}(\int_0^{\Delta t_{eff}} (\frac{I_o}{2n})^2\,dt + \int_0^{\Delta t_{fw}} (\frac{I_o}{2n})^2\,dt)} \\ &= \frac{I_o}{2\sqrt{2}n} \end{aligned} \tag{3.15}$$

3.4.2 Soft-switched T-type converter

For soft-switched T-type converter, neglect resonance and duty cycle loss, then according to 3.3.2, S_1 & S_2 have the same rms current, which is:

$$I_{rms.S_1\&S_2} = \sqrt{\frac{1}{T}\int_0^{\Delta t_{eff}} (i_{S_1})^2\,dt} \tag{3.16}$$

And S_3 & S_4 have the same rms current, which is:

$$I_{rms.S_3\&S_4} = \sqrt{\frac{1}{T}\int_0^{\Delta t_{fw}} (i_{fw})^2\,dt} \tag{3.17}$$

Here i_{S_1} is Equation 3.7, which is:

$$i_{S_1} = \frac{I_o}{n_{T-type}} - \frac{\frac{V_{dc}}{2} - V_o}{Ln_{T-type}} \cdot \frac{\Delta t_{eff}}{2} + \frac{\frac{V_{dc}}{2} - V_o}{Ln_{T-type}} \cdot t \tag{3.18}$$

While i_{fw} is Equation 3.8, which is:

$$i_{fw} = (\frac{I_o}{n_{T-type}} + \frac{\frac{V_{dc}}{2} - V_o}{Ln_{T-type}} \cdot \frac{\Delta t_{eff}}{2})(1 - \frac{R_{ds(on)} + R_{diode}}{L_r}t) \tag{3.19}$$

One thing needs to be specified is that Equation 3.17 represents both the rms of the MOSFET and the rms of the body diode. Since for S_3 & S_4, one half period is the MOSFET that conducting and the other half period is the body diode that conducting. So the rms current of each of them should be considered separately, for the convenience of calculating the conduction loss later.

Then, same as before, assume ideal output inductance and negligible freewheeling current decrease, as shown in Figure 3.31 & Figure 3.32.

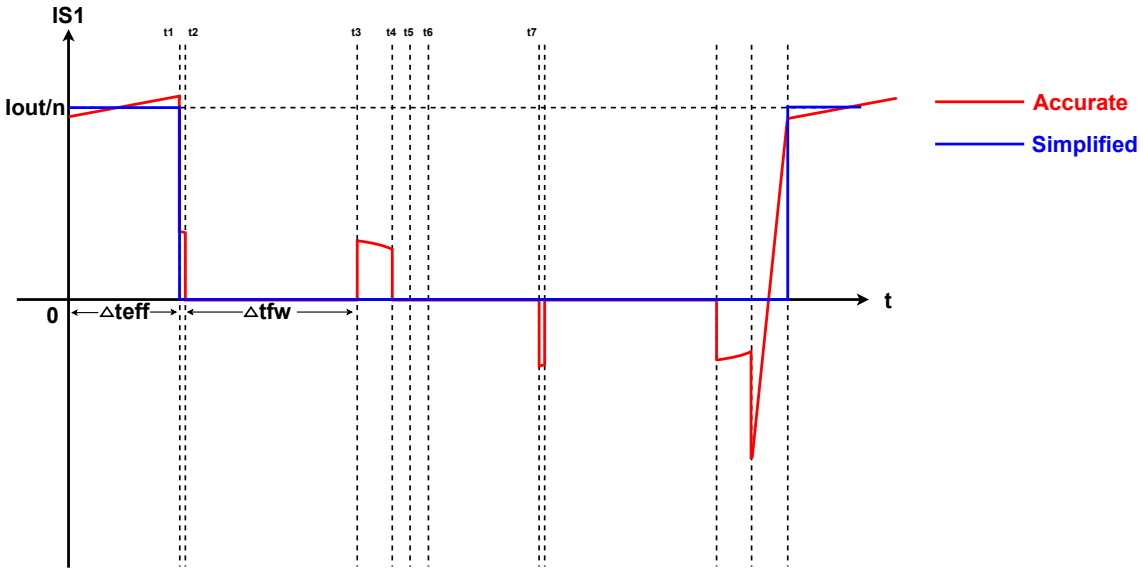

Figure 3.31: Simplified current of S1 for T-Type soft switch converter

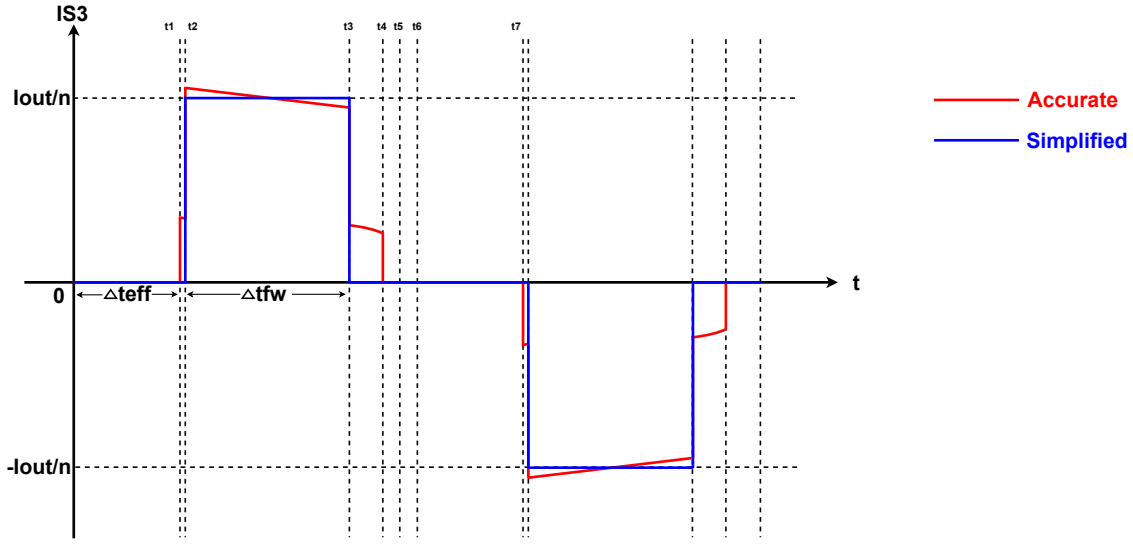

Figure 3.32: Simplified current of S3 for T-Type soft switch converter

Then the rms currents can be calculated as:

$$\begin{aligned} I_{rms.S_1\&S_2} &= \sqrt{\frac{1}{T}\int_0^{\Delta t_{eff}} (\frac{I_o}{n})^2\, dt} \\ &= \frac{I_o}{n}\sqrt{\frac{\Delta t_{eff}}{T}} \end{aligned} \tag{3.20}$$

$$\begin{aligned} I_{rms.S_3\&S_4} &= \sqrt{\frac{1}{T}\int_0^{\Delta t_{fw}} (\frac{I_o}{n})^2\, dt} \\ &= \frac{I_o}{n}\sqrt{\frac{\Delta t_{fw}}{T}} \end{aligned} \tag{3.21}$$

3.4.3 Hard-switched T-type converter

For hard-switched T-type converter,neglect resonance, then according to 3.3.3, S_1& S_2 have the same rms current, which is:

$$I_{rms.S_1\&S_2} = \sqrt{\frac{1}{T}\int_0^{\Delta t_{eff}} (i_{S_1})^2\, dt} \tag{3.22}$$

And S_3 & S_4 have the same rms current, which is:

$$I_{rms.S_3\&S_4} = \sqrt{\frac{1}{T}\int_0^{\Delta t_{fw'}} (i_{fw})^2\, dt} \tag{3.23}$$

Here i_{S_1} is Equation 3.9, which is the same as that of soft-switched T-type converter:

$$i_{S_1} = \frac{I_o}{n_{T-type}} - \frac{\frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o}{Ln_{T-type}} \cdot \frac{\Delta t_{eff}}{2} + \frac{\frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o}{Ln_{T-type}} \cdot t \tag{3.24}$$

And i_{fw} is Equation 3.10, different from soft-switched T-type converter, L_{lk} participates in the freewheeling instead of L_r:

$$i_{fw} = (\frac{I_o}{n_{T-type}} + \frac{\frac{\frac{V_{dc}}{2}}{n_{T-type}} - V_o}{Ln_{T-type}} \cdot \frac{\Delta t_{eff}}{2})(1 - \frac{R_{ds(on)} + R_{diode}}{L_{lk}} t) \tag{3.25}$$

And in Equation 3.23, $\Delta t_{fw'}$ represents the time between the start of the freewheeling stage and the time when the freewheeling current reaches to 0A. $\Delta t_{fw'}$ is smaller than the Δt_{fw}, as can be seen in Figure 3.34.
Make the same assumption, then it can be seen in Figure 3.33 that for the rms current of S_1 & S_2, since the change of current is not rapid, the assumption can be applied. But in Figure 3.34, since the freewheeling current decreases rapidly due to the small L_{lk}, then this assumption is no longer applicable. Because otherwise the error will be quite big, this can be proved mathematically and will not be specified here.

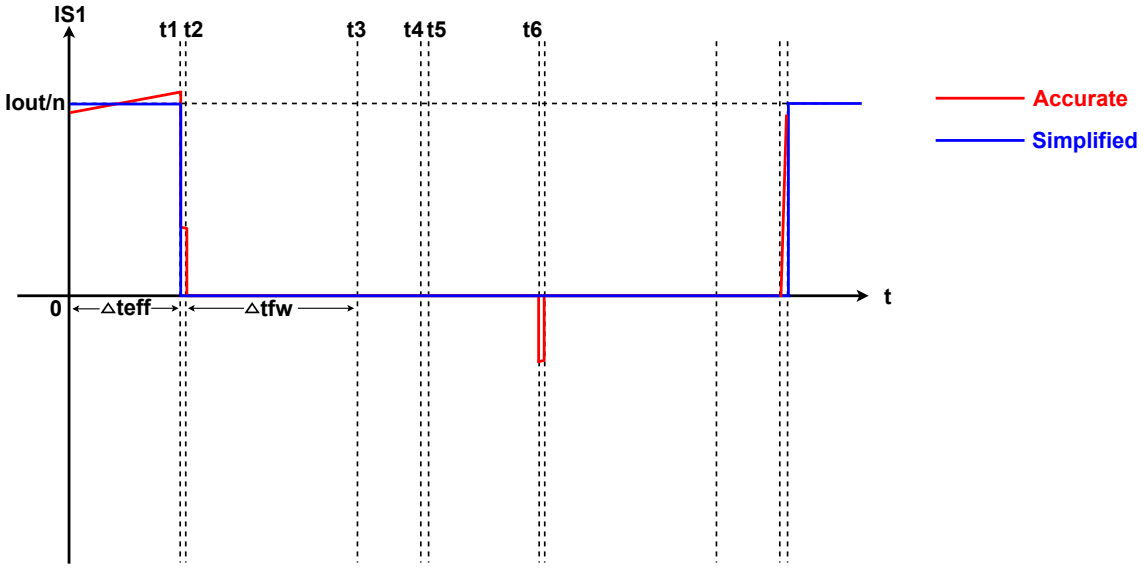

Figure 3.33: Simplified current of S1 for T-Type hard switch converter

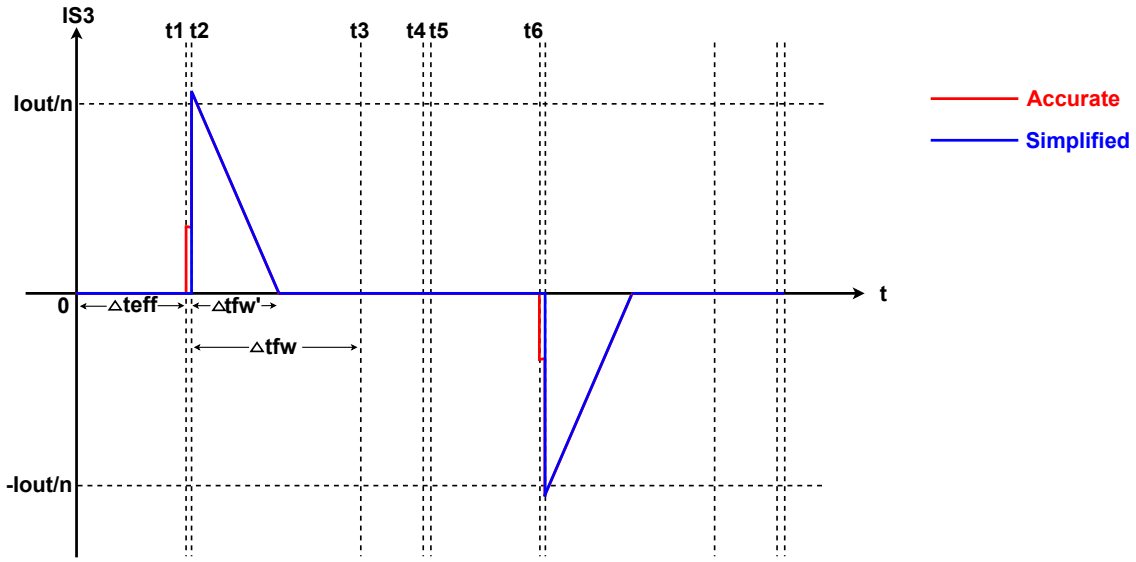

Figure 3.34: Simplified current of S3 for T-Type hard switch converter

So the rms currents can then be calculated as:

$$\begin{aligned} I_{rms.S_1\&S_2} &= \sqrt{\frac{1}{T}\int_0^{\Delta t_{eff}} (\frac{I_o}{n})^2\, dt} \\ &= \frac{I_o}{n}\sqrt{\frac{\Delta t_{eff}}{T}} \end{aligned} \tag{3.26}$$

$$I_{rms.S_3\&S_4} = \sqrt{\frac{1}{T}\int_0^{\Delta t_{fw'}} (\frac{I_o}{n} - \frac{I_o}{n}\frac{R_{ds(on)} + R_{diode}}{L_{lk}}t)^2\, dt} = \frac{I_o}{n}\sqrt{\frac{\Delta t_{fw'}}{T} - \frac{R_{ds(on)} + R_{diode}}{TL_{lk}}\Delta t_{fw'}^2 + \frac{(R_{ds(on)} + R_{diode})^2}{3TL_{lk}^2}\Delta t_{fw'}^3} \tag{3.27}$$

It can be seen that the rms current of S_1 & S_2 of hard-switched T-type converter is same as that of soft-switched T-type converter. And the rms current of S_3 & S_4 of it is the function of $\Delta t_{fw'}$, but anyway, it is smaller than that of soft-switched T-type converter due to the shape of the waveform. So this proves the advantage of hard-switched T-type which is mentioned in 3.3.4 that it has lower middle switch rms current and then lower conduction loss than soft-switched T-type converter.

3.5 Switching loss

3.5.1 PSFB converter

For PSFB converter, since it always has ZVS turning on (except for light load condition), then the primary side MOSFETs only suffer from turning off loss. According to 2.1.1, during turning off, the voltage on the MOSFET increases from 0V to V_{dc} while the current through the MOSFET decreases from $\frac{I_o}{2n}$ (here n means the turns ratio of T-type converter, then $2n$ is the turns ratio of PSFB converter, as specified before) to 0A. As shown in Figure 3.35, represent the switching time (for turning off is $t_{rv} + t_{fi}$) as $t_{sw.off}$, then the turning off loss will be:

$$P_{off} = V_{dc}\frac{I_o}{2n}\frac{t_{sw.off}}{2}f_{sw} \tag{3.28}$$

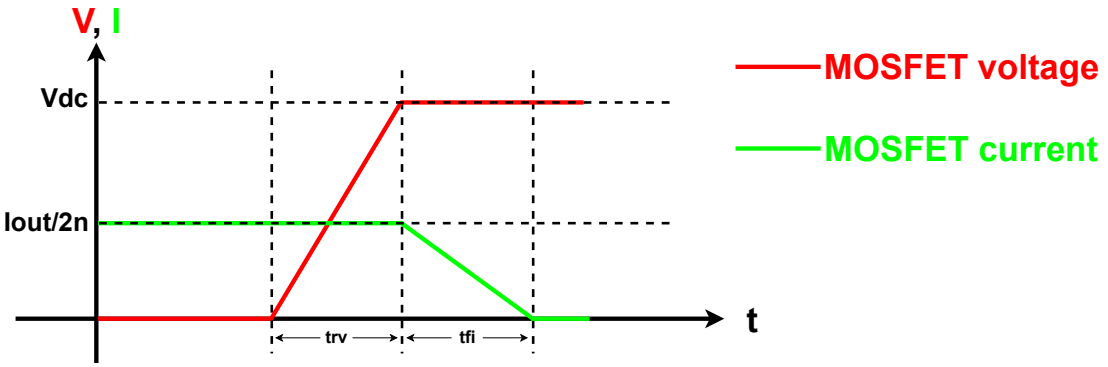

Figure 3.35: Turning off loss of PSFB converter

Here $V_{dc}\frac{I_o}{2n}\frac{t_{sw.off}}{2}$ is the energy dissipation, the power loss is then this value multiply by switching frequency f_{sw}. And since there are four switches on the primary side and all of them have the same voltage and current level before turning off, the the total switching loss of PSFB converter is:

$$\begin{aligned} P_{sw.PSFB} &= 4V_{dc}\frac{I_o}{2n}\frac{t_{sw.off}}{2}f_{sw} \\ &= V_{dc}\frac{I_o}{n}t_{sw.off}f_{sw} \end{aligned} \tag{3.29}$$

3.5.2 Soft-switched T-type converter

For soft-switched T-type converter, since the main switches S_1 & S_2 always have ZVS turning on, they only suffer from turning off loss. According to 2.2.1, during turning off, the voltage on them increases from 0V to $\frac{V_{dc}}{2}$ while the current through them decreases from $\frac{I_o}{n}$ to 0A. As shown in Figure 3.36, assume the switching time of soft-switched T-type converter is same as that of PSFB converter when they are using same kind of semiconductors, then the turning off loss will be:

$$P_{off} = \frac{V_{dc}}{2}\frac{I_o}{n}\frac{t_{sw.off}}{2}f_{sw} \tag{3.30}$$

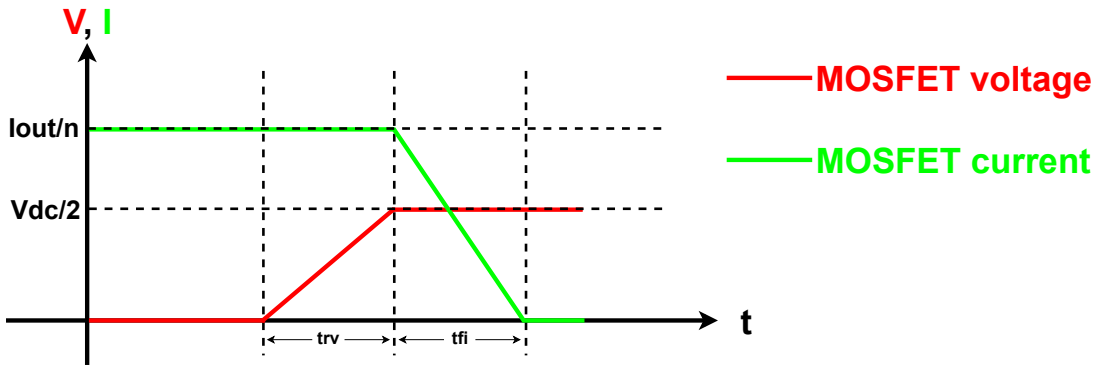

Figure 3.36: Turning off loss of the main switches of soft-switched T-type converter

For middle switches, according to 2.2.1, since the middle switch is turned on after the circuit reaches duty cycle loss stage during which the voltage on the middle switch is 0V, so the turning on of middle switches is also ZVS. For the turning off, since the voltage on it will increase from 0V to $\frac{V_{dc}}{2}$ while the current through it will decrease from $\frac{I_o}{n}$ to 0A, the turning off loss of it is same as that of main switch, which value is $\frac{V_{dc}}{2}\frac{I_o}{n}\frac{t_{sw.off}}{2}f_{sw}$. So the total loss of soft-switched T-type converter is:

$$\begin{aligned} P_{sw.T-soft} &= 2P_{sw.off.main} + 2P_{sw.off.middle} \\ &= 4\frac{V_{dc}}{2}\frac{I_o}{n}\frac{t_{sw.off}}{2}f_{sw} \\ &= V_{dc}\frac{I_o}{n}t_{sw.off}f_{sw} \end{aligned} \tag{3.31}$$

3.5.3 Hard-switched T-type converter

For hard-switched T-type converter, since the main switches already lost ZVS, they will suffer from both turning on loss and turning off loss. The turning on of the main switch happens during the $t_5 \sim t_6$ in Figure 2.26. It can be seen that the voltage decreases from $\frac{V_{dc}}{2}$ to 0V while the current increases from 0A to the initial value of the next energy transfer stage, from later sections it can be seen that this value is around $\frac{I_o}{n}$. So the turning on loss will be:

$$P_{on} = \frac{V_{dc}}{2}\frac{I_o}{n}\frac{t_{sw.on}}{2}f_{sw} \tag{3.32}$$

Here $t_{sw.on}$ is the switching time, for turning on it is $t_{fv} + t_{ri}$. As shown in Figure 3.37.

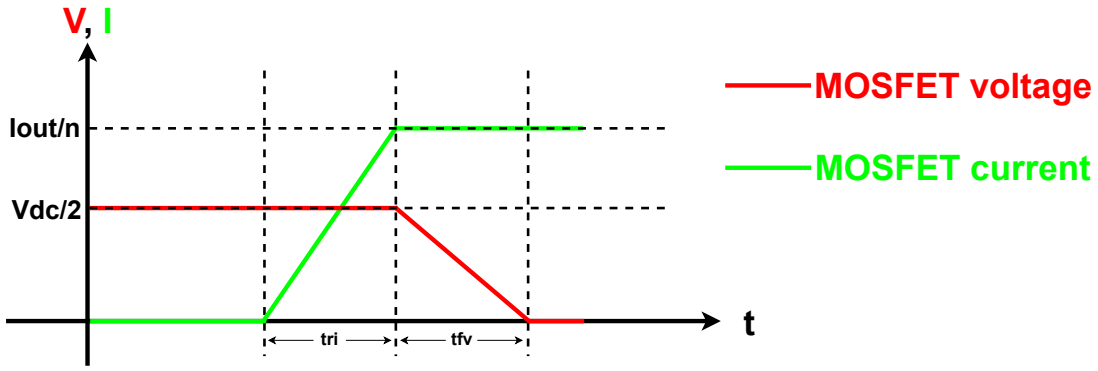

Figure 3.37: Turning on loss of the main switches of hard-switched T-type converter

The turning off of the main switches of hard-switched T-type converter is exactly the same as that of soft-switched T-type converter, so the turning off loss is also:

$$P_{off} = \frac{V_{dc}}{2}\frac{I_o}{n}\frac{t_{sw.off}}{2}f_{sw} \tag{3.33}$$

For the main switch, since there is no duty cycle loss, usually the middle switch is turned on during the energy transfer stage during which the voltage on it is 0V. So the middle switch also has ZVS turning on, same as soft-switched T-type converter. And for the turning off, if the T-type converter has typical hard switching, then before the time that the middle switch is turned off, the current goes through it has already reached 0A. Then after the middle switched is turned off, the current goes through it should be the current which charges the voltage on it to $\frac{V_{dc}}{2}$. So the turning off loss energy of the the switch can then be represented by the capacitive energy be charged to the parasitic capacitance. Then the turning off loss will be:

$$\begin{aligned} P_{sw.off.middle} &= W_{cap} f_{sw} \\ &= \frac{1}{2}C(\frac{V_{dc}}{2})^2 f_{sw} \end{aligned} \tag{3.34}$$

So the total loss of hard-switched T-type converter is:

$$\begin{aligned} P_{sw.T-hard} &= 2(P_{sw.on.main} + P_{sw.off.main}) + 2P_{sw.off.middle} \\ &= V_{dc}\frac{I_o}{n}f_{sw}(\frac{t_{sw.on}}{2} + \frac{t_{sw.off}}{2}) + C(\frac{V_{dc}}{2})^2 f_{sw} \end{aligned} \tag{3.35}$$

3.5.4 Comparison between three topologies about the switching loss of the MOSFETs

Firstly, it can be seen from above that:

$$P_{sw.PSFB} = P_{sw.T-soft} \tag{3.36}$$

Which means the switching loss of PSFB converter and soft-switched T-type converter are always the same if neither of them loses ZVS. In practical case they may not be exactly the same but they will always at a same level.
In Equation 3.35, assume if the switching on time and the switching off time are the same, then Equation 3.35 will become:

$$P_{sw.T-hard} = V_{dc}\frac{I_o}{n}t_{sw}f_{sw} + C(\frac{V_{dc}}{2})^2 f_{sw} \tag{3.37}$$

Here $t_{sw} = t_{sw.on} = t_{sw.off}$, then it can be seen that hard-switched T-type converter always has larger switching loss than that of PSFB converter and soft-switched T-type converter. This is reasonable because it does not have ZVS performance. But even though, due to the advantage of hard-switched T-type that some conduction loss can be reduced, as specified in 3.4.3 this topology still has considerable potential when the conduction loss is dominant in the case of application.

3.6 Conduction loss

3.6.1 PSFB converter

For PSFB converter, according to Equation 3.15, the rms current of all the four switches is:

$$I_{rms.S_1\sim S_4} = \frac{I_o}{2\sqrt{2}n} \tag{3.38}$$

Then the conduction loss is:

$$\begin{aligned} P_{cond.PSFB} &= 4I^2_{rms.S_1\sim S_4}R_{ds.on} \\ &= \frac{I_o^2}{2n^2}R_{ds.on} \end{aligned} \tag{3.39}$$

3.6.2 Soft-switched T-type converter

For soft-switched T-type converter, according to Equation 3.20 & Equation 3.21, the rms current of the main switches and middle switches are different, which are:

$$I_{rms.S_1\&S_2} = \frac{I_o}{n}\sqrt{\frac{\Delta t_{eff}}{T}} \tag{3.40}$$

$$I_{rms.S_3\&S_4} = \frac{I_o}{n}\sqrt{\frac{\Delta t_{fw}}{T}} \tag{3.41}$$

Also since for middle switches, in one half period is the MOSFET that conducting and in the other half cycle is the body diode that conducting, then the total conduction loss is:

$$\begin{aligned} P_{cond.T-soft} &= 2I^2_{rms.S_1\&S_2}R_{ds.on} + 2(I^2_{rms.S_3\&S_4}R_{ds.on} + I^2_{rms.S_3\&S_4}R_{diode}) \\ &= \frac{I_o^2}{n^2}R_{ds.on} + \frac{I_o^2}{n^2}\frac{2\Delta t_{fw}}{T}R_{diode} \end{aligned} \tag{3.42}$$

3.6.3 Hard-switched T-type converter

For hard-switched T-type converter, according to Equation 3.26 & Equation 3.27, the rms current of the main switches and middle switches are different, which are:

$$I_{rms.S_1\&S_2} = \frac{I_o}{n}\sqrt{\frac{\Delta t_{eff}}{T}} \tag{3.43}$$

$$I_{rms.S_3\&S_4} = \frac{I_o}{n}\sqrt{\frac{\Delta t_{fw'}}{T} - \frac{R_{ds(on)} + R_{diode}}{TL_{lk}}\Delta t^2_{fw'} + \frac{(R_{ds(on)} + R_{diode})^2}{3TL^2_{lk}}\Delta t^3_{fw'}} \tag{3.44}$$

Then the total conduction loss is:

$$\begin{aligned} P_{cond.T-hard} &= 2I^2_{rms.S_1\&S_2}R_{ds.on} + 2(I^2_{rms.S_3\&S_4}R_{ds.on} + I^2_{rms.S_3\&S_4}R_{diode}) \\ &= \frac{I_o^2}{n^2}\frac{2\Delta t_{eff}}{T}R_{ds.on} + 2\frac{I_o^2}{n^2}(\frac{\Delta t_{fw'}}{T} - \frac{R}{TL_{lk}}\Delta t^2_{fw'} + \frac{R^2}{3TL^2_{lk}}\Delta t^3_{fw'})R \end{aligned} \tag{3.45}$$

Here R is the sum of $R_{ds(on)}$ and R_{diode}.

3.6.4 Comparison between three topologies in terms of the conduction loss of the MOSFETs

For the comparison between PSFB converter and soft-switched T-type converter, according to Equation 3.39 & Equation 3.42, it can be clearly seen that:

$$P_{cond.PSFB} < P_{cond.T-soft} \tag{3.46}$$

And this relationship always exists because it is neither relevant to load level nor the effective duty cycle.
For the comparison between PSFB converter and hard-switched T-type converter, it depends on the relationship between Equation 3.39 and Equation 3.45. When the term

$$2\frac{I_o^2}{n^2}(\frac{\Delta t_{fw'}}{T} - \frac{R}{TL_{lk}}\Delta t_{fw'}^2 + \frac{R^2}{3TL_{lk}^2}\Delta t_{fw'}^3)R \tag{3.47}$$

in Equation 3.45 is small enough, Equation 3.45 is possible to be smaller than Equation 3.39 when Δt_{eff} is small enough. A small Δt_{eff} represents either voltage level is very high or load level is very light or both of them, which means in that case the conduction loss of PSFB converter is possible to be smaller than the conduction loss of hard-switched T-type converter.

3.7 Transformer

3.7.1 Transformer Design

The transformer design is basically following the steps shown in Figure 3.38, in which all steps are directly related to topology itself except for the first step.

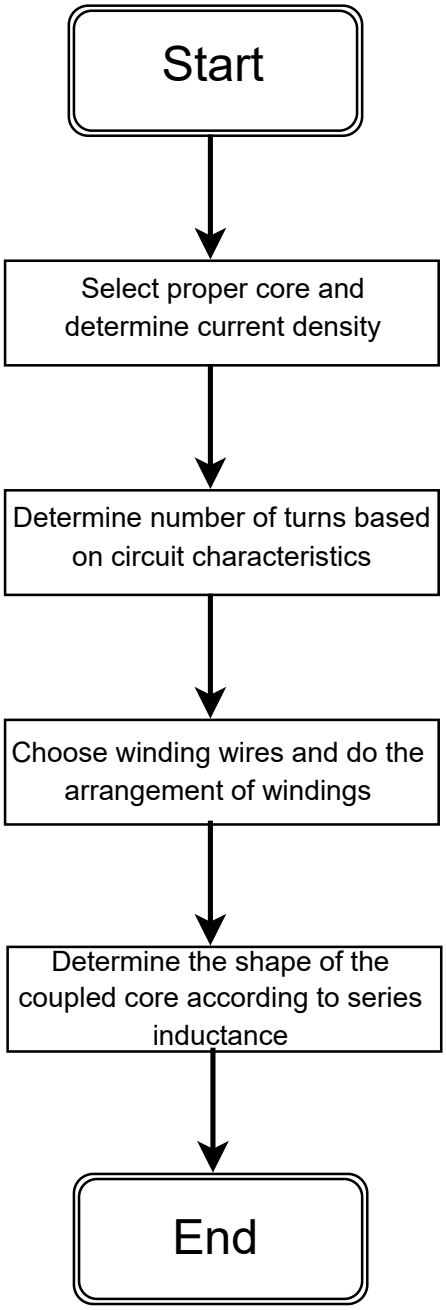

Figure 3.38: Flowchart of transformer design procedure

The current density in this design is selected as

$$J = 10A/mm^2 \tag{3.48}$$

which is a suitable value for most of the copper wires.
Moreover, EQ32 is selected as the main core and PQ32/30 is the series inductance with leakage inductance of transformer itself. As displayed in Figure 3.39, usually two EQ32 cores coupled together to form the transformer primary and secondary side then PQ32 core could be coupled with the core which represents primary side working as the series inductance while the middle bar of the cores is used for winding

and the length is also displayed in the figure.

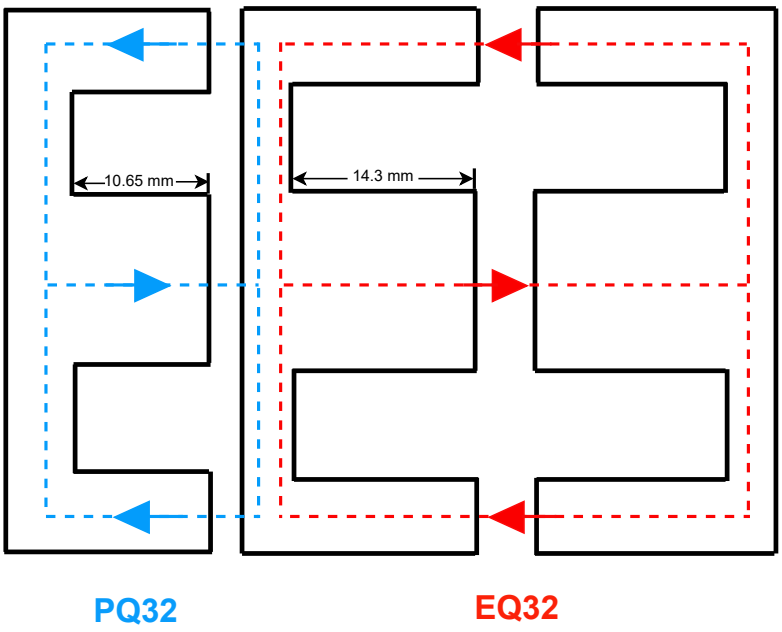

Figure 3.39: Selected cores and their coupling

3.7.1.1 PSFB converter

As mentioned in section 3.1, the turns ratio of PSFB converter is 10:1, so the number of winding turns on primary side can be determined as 10 then on secondary side is 1. Since the maximum output current on output side is 160A, the maximum rms current going through primary side winding can be calculated as 16A and for secondary side winding can be 113A according to section 3.4 and 2.3. In order to reduce the number of winding groups, the cross section area of the copper is chosen as $2mm^2$, so each wire could take 20A as shown in equation 3.49, then only one group of winding is needed on primary side while six groups are required on secondary side according to equation 3.50 and 3.51.

$$I_{wire} = J \cdot A_{wire} = 20A \tag{3.49}$$

$$N_{p-groups} = \frac{I_{p-rms}}{I_{wire}} = \frac{16}{20} \approx 1 \tag{3.50}$$

$$N_{s-groups} = \frac{I_{s-rms}}{I_{wire}} = \frac{113}{20} \approx 6 \tag{3.51}$$

Using the cross section area as one criterion, the wire is finally selected as presented in Figure 3.40, in which $h = 0.5mm$ and $w = 4mm$.

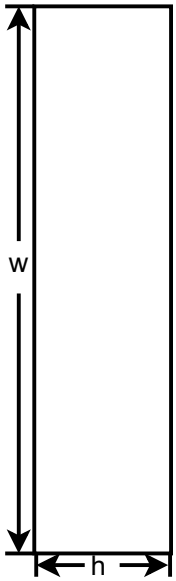

Figure 3.40: Cross section of the selected copper wire

For the arrangement of windings, the shorter side is used to stick on the middle bar of cores. Equation 3.52 and 3.53 display the calculation of total length required to put the winding wires,

$$L_1 = N_{windings} \cdot N_{turns} \cdot N_{p-groups} \cdot h = 5mm < 14.3mm \tag{3.52}$$

$$L_2 = N_{windings} \cdot N_{turns} \cdot N_{s-groups} \cdot h = 6mm < 14.3mm \tag{3.53}$$

where N_{turns} is the number of winding turns and $N_{windings}$ is the number of windings. For center-taped transformer, the primary side only needs one winding while there are two windings required on the secondary side. All in all, only one layer of windings is required according to equation 3.52 and 3.53 and the final arrangement is shown in Figure 3.41, where 14.3mm is mentioned in Figure 3.39

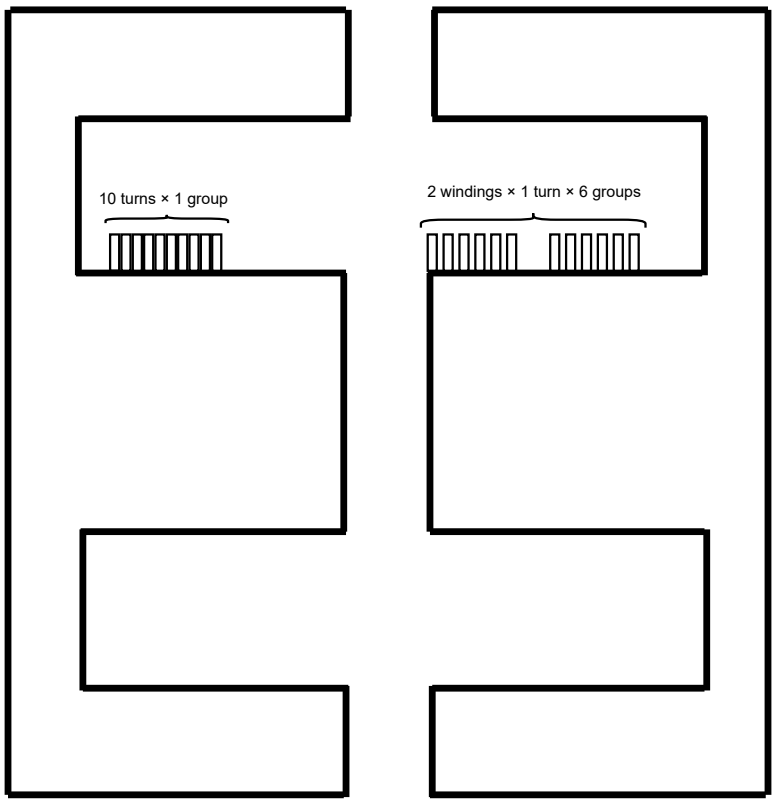

Figure 3.41: Winding arrangement of main cores for PSFB converter

Final part of the design is the series inductance, the PQ32 core will be modified with reluctance value for different series inductance value as equation 3.54, where $\Re$ is the total reluctance calculated with equation 3.55. As mentioned in previous chapter, the series inductance value in PSFB converter is $2.8\mu H$ which gives a 1.1mm airgap length.

$$L_s = \frac{N_s^2}{\Re} \tag{3.54}$$

$$\Re = \frac{l_{total} - l_{airgap}}{\mu_0 \mu_r A_{core}} + \frac{l_{airgap}}{\mu_0 A_{core}} \tag{3.55}$$

Hence, the series inductance value is finally determined with the airgap length opened at the middle bar of the core while the number of winding turns on the core is fixed as 4 in all topologies and the groups of winding is the same as the main core of transformer primary side then the calculation can be done with 3.56, which means that there is also only one layer needed in the series inductance core.

$$L_{series} = N_{turns} \cdot N_{1-groups} \cdot h = 2mm < 14.3mm \tag{3.56}$$

Then the arrangement of wires for series inductance is shown in Figure 3.42.

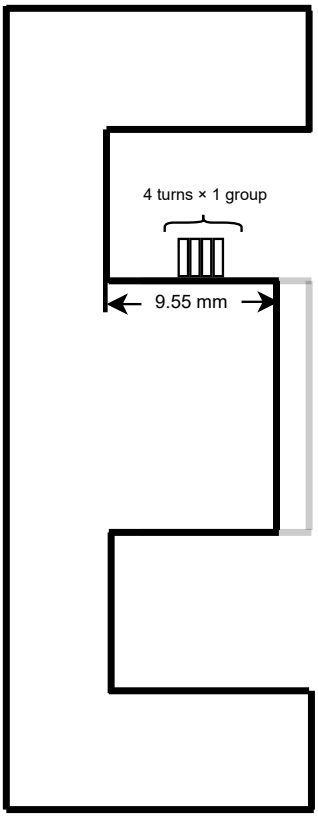

Figure 3.42: Winding arrangement of series inductance for PSFB converter

Finally, the design of transformer for PSFB is shown as Figure 3.43.

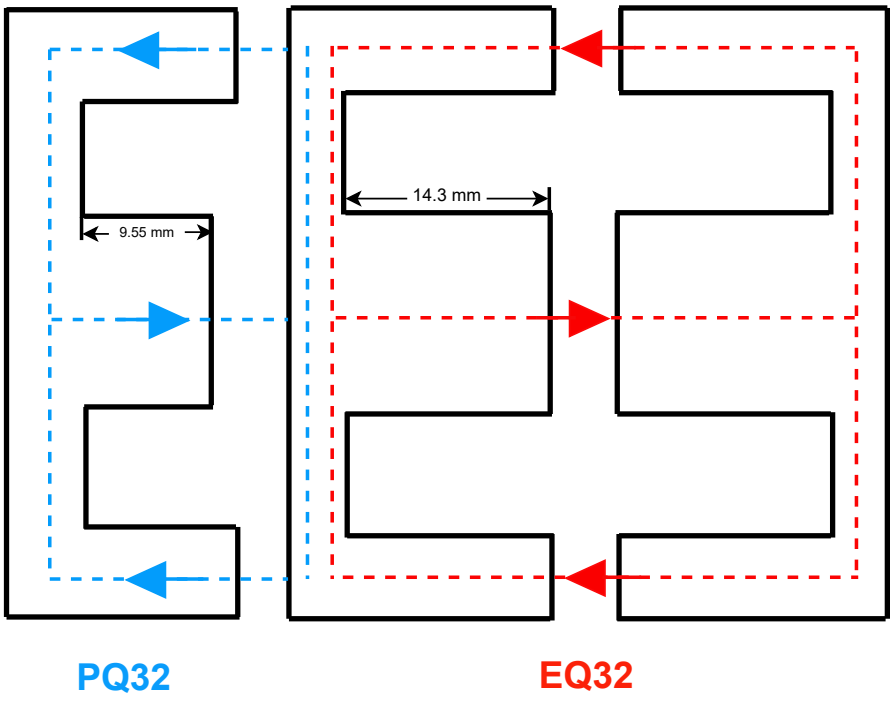

Figure 3.43: Transformer design of PSFB converter

3.7.1.2 Soft-switched T-Type converter

The turns ratio of transformer in soft switched T-Type converter is half of PSFB converter which is 5:1, but the number of turns on primary side is also used as 10 to fix the magnetizing inductance value as equation 3.57, then the secondary side number of turns should be 2 for the turns ratio 5:1.

$$L_m = \frac{N_{turns}^2}{\Re} \tag{3.57}$$

Since the turns ratio is half of PSFB, the primary side rms current is doubled as 32A according to section 3.4 but secondary side rms current is still 113A for the maximum output current is the same (160A). In soft switched T-Type converter, the same cores and wires are made up the transformer. Then the number of winding groups on the main cores can be calculated with equation 3.58 and 3.59.

$$N_{p-groups} = \frac{I_{p-rms}}{I_{wire}} = \frac{32}{20} \approx 2 \tag{3.58}$$

$$N_{s-groups} = \frac{I_{s-rms}}{I_{wire}} = \frac{113}{20} \approx 6 \tag{3.59}$$

According to equation 3.60 and 3.61, the middle bar of EQ32 core still has enough space to put only one layer of wires in soft-switched T-Type converter and the arrangement is shown in Figure 3.44.

$$L_1 = N_{groups} \cdot N_{turns} \cdot N_{p-groups} \cdot h = 10mm < 14.3mm \tag{3.60}$$

$$L_2 = N_{groups} \cdot N_{turns} \cdot N_{s-groups} \cdot h = 12mm < 14.3mm \tag{3.61}$$

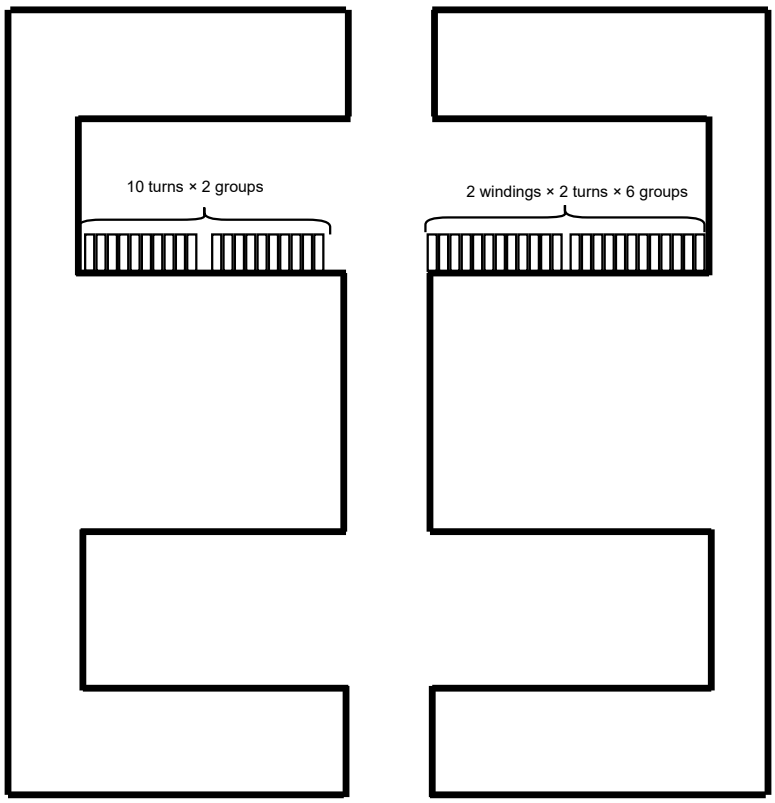

Figure 3.44: Winding arrangement of main cores for T-Type soft switch converter

For the design of series inductance, equation 3.54 and 3.55 used for design of PSFB could still be used in this design because the only difference is series inductance value, in this case is $0.7\mu H$ then the airgap length is calculated as 4.4mm. Then the arrangement of series inductance is shown in the following equation and figure which also shows one layer arrangement.

$$L_s = N_{turns} \cdot N_{1-groups} \cdot h = 4mm < 14.3mm \tag{3.62}$$

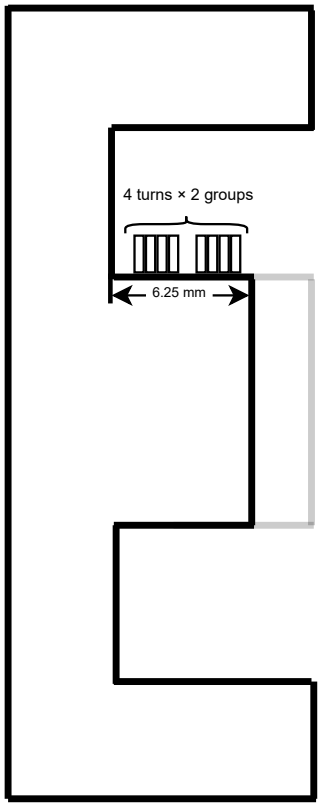

Figure 3.45: Winding arrangement of series inductance for T-Type soft switch converter

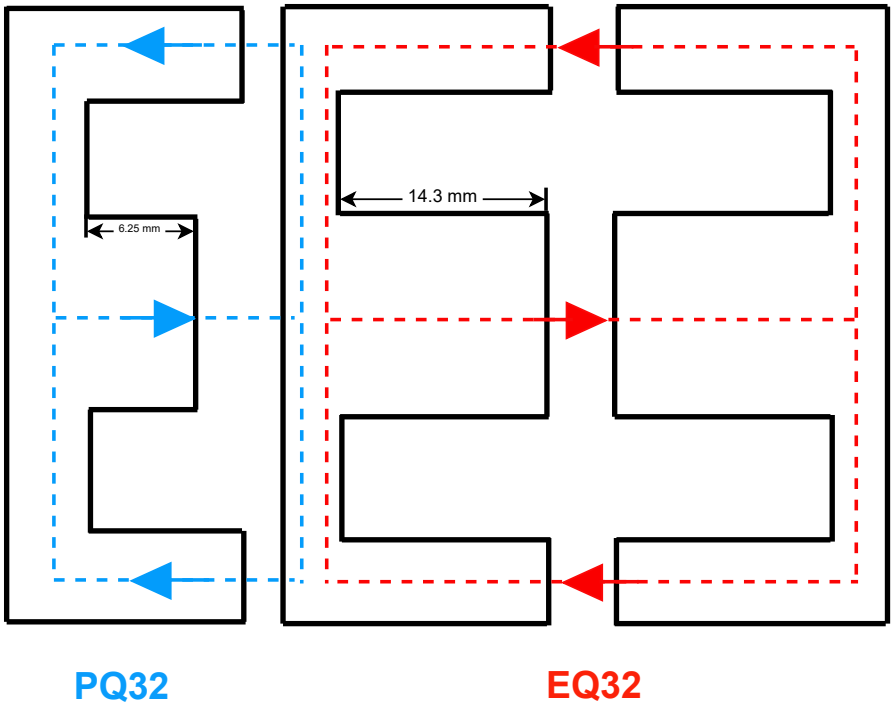

Figure 3.46: Transformer design of T-Type soft switch converter

Finally, the transformer design of soft-switched T-Type converter is displayed in Figure 3.46.

3.7.1.3 Hard switched T-Type converter

The transformer design of hard-switched T-Type is almost same as soft-switched T-Type. There is no need for hard switch topology to have a large resonant inductance value used for ZVS, they usually just have the leakage inductance of transformer itself, so the design of hard-switched T-Type converter is the same as soft-switched T-Type converter with only exception that it does not have series inductance.

3.7.1.4 Comparison in terms of transformer design

Table 3.1 and 3.2 present all the arrangement results and parameters in the transformer of the three topologies. In table 3.1, it can be seen that the difference between PSFB and T-Type converter about the arrangement on main cores are the number of winding groups on primary side and number of turns on secondary side, which are both caused by the different transformer turns ratio. Table 3.2 is only parameters of transformer cores used to form the transformers, which shows that the only difference about transformer core is the volume of series inductance core caused by different inductance value, which is calculated according to equation 3.63.

Table 3.1: Arrangement of transformer windings

		T-Type soft switch	T-Type hard switch	PSFB
Primary side	Number of windings	1	1	1
	Number of turns	10	10	10
	Group of Winding	2	2	1
Secondary side	Number of windings	2	2	2
	Number of turns	2	2	1
	Group of Winding	6	6	6
Series inductance	Number of windings	1	/	1
	Number of turns	4	/	4
	Group of Winding	2	/	1

Table 3.2: Parameter of transformer cores

		T-Type soft switch	T-Type hard switch	PSFB
Primary core	Volume	$13900mm^3$	$13900mm^3$	$13900mm^3$
	Cross section area	$152mm^2$	$152mm^2$	$152mm^2$
Secondary core	Volume	$13900mm^3$	$13900mm^3$	$13900mm^3$
	Cross section area	$152mm^2$	$152mm^2$	$152mm^2$
Series inductance core	Volume	$4543.28mm^3$	/	$5050.82mm^3$
	Cross section area	$153.8mm^2$	/	$153.8mm^2$

$$V_{core-with-airgap} = V_{core} - A_{core} \cdot l_{airgap} \tag{3.63}$$

Therefore, it can be seen that T-Type soft switch and hard switch converter use the same transformer, only except for the series inductance core which means T-Type hard switch converter has the smallest transformer size while PSFB has simlar

transformer size as T-Type soft switch converter because they both have series inductance core

3.7.2 Core Loss comparison

To simplify the calculation of core loss, the $P_{cv} - B_m$ curve is used to read the core loss value per unit volume of the transformer core material. Therefore, core loss is relevant to the volume and flux density change in transformer core. Since the volume of transformer cores are already fixed after the design is completed as shown in Table 3.2, then only B_m needs to be calculated. The calculation of B_m is shown from equation 3.64 to 3.67,

$$V_p = L_m \frac{di}{dt} = L_m \frac{\Delta I}{\Delta t} \tag{3.64}$$

$$\psi = L_m \Delta I = N_{turns} \Phi = N_{turns} \Delta B A_{core} \tag{3.65}$$

$$\Delta B = \frac{L_m \Delta I}{N_{turns} A_{core}} = \frac{V_p \Delta t}{N_{turns} A_{core}} \tag{3.66}$$

$$B_m = B_{max} = \frac{1}{2} \Delta B = \frac{L_m \Delta I}{2 N_{turns} A_{core}} = \frac{V_p \Delta t}{2 N_{turns} A_{core}} \tag{3.67}$$

where Δt is the time when the current in transformer winding changes, L_m is the magnetizing inductance value, A_{core} is the cross section area of core, N_{turns} is the number of winding turns and V_p is the voltage stress on primary side. In equation 3.67, B_m in $P_{cv} - B_m$ curve used here is half of flux density change because flux density in transformer of isolated converter varies from negative value $-B_{max}$ to positive value $+B_{max}$. Then, $P_{cv} - B_m$ curves of some material only use B_{max} value as B_m to show the material properties.
For the main cores, the calculation is completed by the formula with Δt and V_p in equation 3.67. Since the only difference between PSFB and T-Type converter is that the voltage stress V_p of T-Type is half of PSFB in this formula, B_m of T-Type should also be half of PSFB, which means T-Type converter has less core loss in main cores than PSFB.
The calculation of series inductance core uses equation 3.68, in which L_s is the series inductance value. Since the series inductance value in PSFB converter is around four time of the value in soft-switched T-Type converter, B_m of soft-switched T-Type converter in series inductance core is also smaller than PSFB converter.

$$B_m = \frac{L_s \Delta I}{2 N_{turns} A_{core}} \tag{3.68}$$

However, according to equation 3.54 and 3.55 used for design of leakage inductance core, the difference between leakage inductance values in PSFB and soft-switched T-Type converter also leads to a difference between leakage core volumes as shown in Table 3.2 and equation 3.63.
Therefore, PSFB converter has the largest value of core loss for main core due to the reason that it has a larger B_m than T-Type converter, and hard-switched T-Type

converter has the minimum value of core loss because it has no series inductance used to complete resonant process.

3.7.3 Copper Loss comparison

The copper loss of transformer is calculated with rms current and ac resistance of the wire on both primary and secondary side as shown in equation 3.69,

$$P_{copper} = I_{prms}^2 R_{pAC} + I_{srms}^2 R_{sAC} \tag{3.69}$$

where R_{pAC} and R_{sAC} are the AC winding resistance values of primary and secondary side windings while I_{prms} and I_{srms} are the rms currents going through primary and secondary side winding. In the design of all three different topologies, there is only one layer of the wires wrapped on the core, so the proximety effect can be ignored, which means that the ac winding resistance is only influenced by the parameters of winding wire itself and skin effect.
For the rectangular wire used in this design, the skin effect is considered with Dowell's equation. In Dowell's Equation, there is an AC-to-DC winding resistance ratio shown in equation 3.70,

$$F_{RB} \approx 1 + \frac{5N_l^2 - 1}{45}(\frac{h_B}{\delta_\omega})^4 = 1.05 \tag{3.70}$$

where N_l is the layer number of foil winding, h_B is the foil thickness and δ_ω is the skin depth in the boundary between low frequency and medium frequency [15].
Since the frequency value used in this thesis is in the medium frequency range, then AC-to-DC winding resistance ratio F_{RB} can be directly used as 1.05. Then, the AC winding resistance can be calculated with equation 3.71, in which $R_{\omega AC}$ is the AC winding resistance and $R_{\omega DC}$ is the DC winding resistance.

$$R_{\omega AC} = F_R R_{\omega DC} \tag{3.71}$$

Then, the calculation of AC winding resistance shall start with DC winding resistance as shown in equation 3.72,

$$R_{DC} = \frac{\rho l}{A} \tag{3.72}$$

where ρ is the resistivity of copper wire, l is the total length and A is the cross section area of the winding wires. Meanwhile, the total length and cross section area can be calculated with equation 3.73 to 3.74.

$$A = h \cdot w \cdot N_{groups} \tag{3.73}$$

$$l = \pi \cdot D \cdot N_{turns} \tag{3.74}$$

where N_{turns} is number of winding turns, N_{groups} is the number of winding groups, h, w are the width and length of wire cross section as shown in Figure 3.40 and $\pi \cdot D$ is the length when the wire is wrapped around the middle bar. All the useful parameters about winding arrangement are shown in table 3.1.

For the secondary side winding, the only difference between different topologies that the number of turns of T-Type converter is doubled compared with PSFB converter, which means the AC-winding resistance value will also be doubled. Then the copper loss on secondary side winding of T-Type converter is twice of PSFB converter due to the same secondary side rms current as displayed in equation 3.75.

$$P_{s-T} = I^2_{srms-T} R_{sAC-T} = I^2_{srms-PSFB}(2 \cdot R_{pAC-PSFB}) = 2 \cdot P_{s-PSFB} \tag{3.75}$$

Meanwhile, since the groups of winding in T-Type is doubled compared with PSFB for primary side winding, the AC-winding resistance of T-Type should be half of PSFB converter. However, the transformer turns ratio of T-Type is half of PSFB as mentioned in section 3.1, so the rms current going through primary side winding of T-Type converter is also doubled. Hence, the copper loss on primary side winding of T-Type converter is twice of PSFB converter as shown in equation 3.76.

$$P_{p-T} = I^2_{prms-T} R_{pAC-T} = (2 \cdot I_{prms-PSFB})^2 (\frac{R_{pAC-PSFB}}{2}) = 2 \cdot P_{p-PSFB} \tag{3.76}$$

According to table 3.1, the copper loss in series inductance core is also doubled in soft-switched T-Type converter compared with PSFB converter since the number of groups still twice due to the difference in rms current.
Therefore, the total transformer copper loss of soft-switched T-Type converter is twice of PSFB converter and is also larger than hard-switched T-Type converter due to the reason that there is no series inductance in hard switch topology. However, even the copper loss of main cores for hard-switched T-Type is twice of PSFB, it is difficult to determine whether hard-switched T-Type or PSFB has a larger value of copper loss since it is not sure if copper loss of series inductance core could be larger than the main cores.

4

Methodology

To make the comparison more realistic, it is necessary to do simulation to get relevant results so that the theoretical analysis can be proved. In this case, the simulation of different topologies is done with PSpice to get efficiency results. Meanwhile, the MOSFET losses including conduction loss and switching loss are also calculated based on the data output from simulation files. However, since transformer model in simulation is formed with ideal inductors, transformer losses should be calculated independently based on ideal theory and transformer model in reality but still require some input from simulation data.

4.1 Efficiency Calculation

The efficiency of one converter can be calculated with equation 4.1,

$$\eta = \frac{P_{out}}{P_{in}} \tag{4.1}$$

where η is the efficiency result, P_{in} is the total input power from voltage source and P_{out} is the output power of the converter. In simulation, the average power of the input voltage source can be directly used as P_{in} and P_{out} is the power consumed by output resistor in steady state. Then, the efficiency calculation can be completed easily in the simulation.

4.2 Loss Calculation

4.2.1 MOSFET Loss

4.2.1.1 Conduction Loss

Theoretically, MOSFET conduction loss should be calculated with rms current and static drain to source on-state resistance value of MOSFET while conducting as equation 4.2,

$$P_{cond} = I_{rms}^2 R_{on} \tag{4.2}$$

where I_{rms} is the rms current flowing through the MOSFET and R_{on} is the on-state resistance of MOSFET itself or body diode. However, the MOSFET on-state resistance is not always the typical value given in datasheet, it varies with gate-to-source voltage on MOSFET, the drain current going through it and temperature of

the certain condition while the resistance value of MOSFET body diode always is not given in the datasheet. Therefore, the conduction losses are all calculated by integrating watt meter plot in conduction range as shown in equation 4.3, which is exported from PSpice simulation.

$$P_{cond} = \int P_{switch} dt \cdot f_{sw} \tag{4.3}$$

4.2.1.2 Switching Loss

Switching loss can be divided into two parts: turning on loss and turning off loss as shown in Figure 4.1. According to the figure, both the turn on loss and turn off loss can be calculated based on the drain-source voltage and drain current going through the MOSFET during turning on and turning off period.

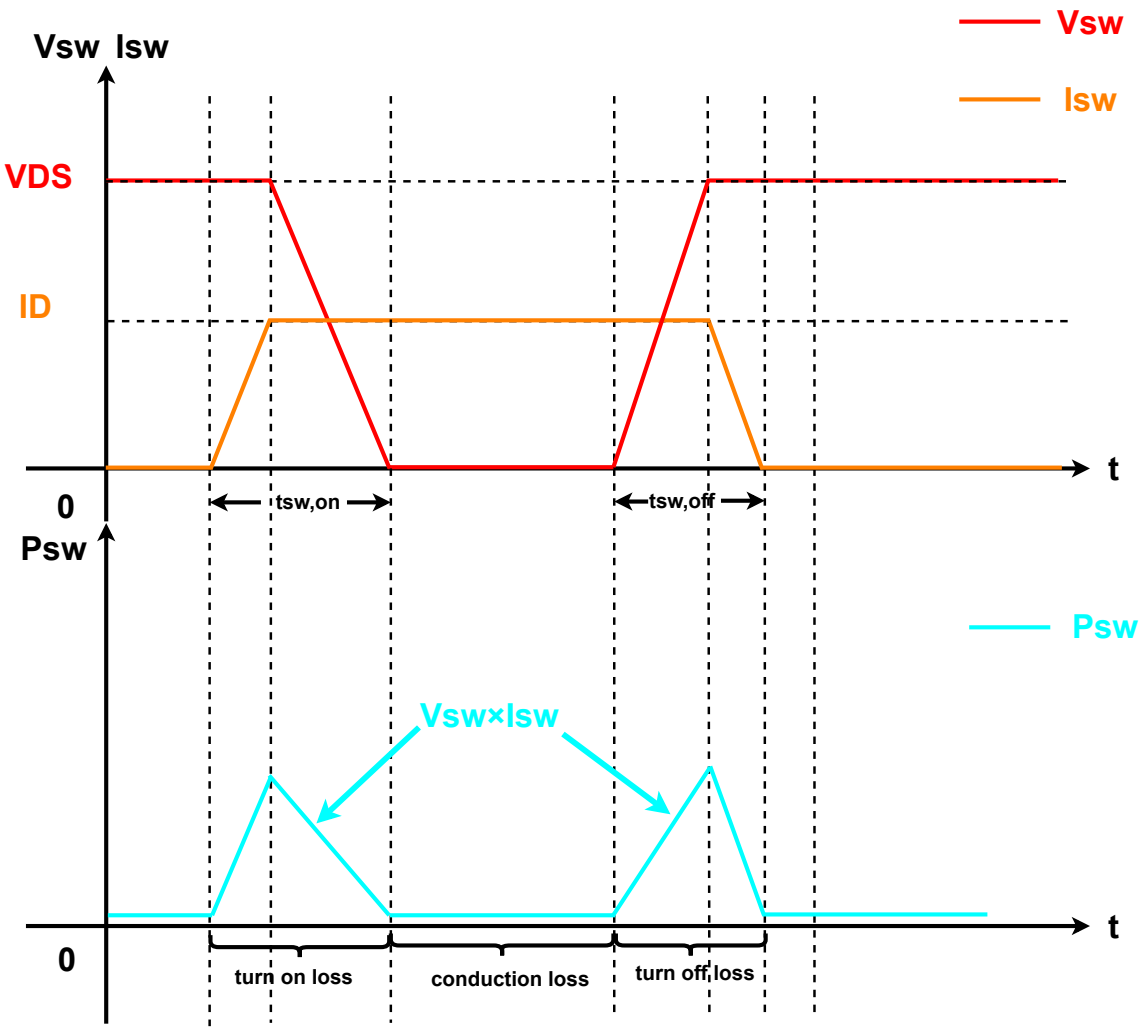

Figure 4.1: MOSFET loss during switching

Therefore, it always starts with the calculation of energy loss by integrating the product of switching voltage and current to find the result of power loss as shown in equation 4.4, in which V_{sw} and I_{sw} are exported from the simulation files.

$$W_{sw} = \int V_{sw} \cdot I_{sw} dt \tag{4.4}$$

Then, the power losses can be calculated by using equation 4.5 with energy loss value and switching frequency.

$$P_{sw} = W_{sw} \cdot f_{sw} \tag{4.5}$$

Moreover, same as conduction losses, switching losses can also be calculated with watt meter plot from simulation, and the results are the same as calculation in equation 4.4 and 4.5.

4.2.2 Transformer Loss

4.2.2.1 Core Loss

As mentioned in section 3.7.2, the $P_{cv} - B_m$ curve is used to read the core loss value per unit volume of transformer core material. According to the equation 3.67, B_m is calculated by several parameters but for the main core only Δt - the power transfer time is not a constant value as the following equation.

$$B_m = \frac{1}{2}\Delta B = \frac{V_p \Delta t}{2 N_{turns} A} \tag{4.6}$$

Hence, the value of B_m of the main core can be calculated using equation 4.6 by getting Δt from simulation models, then the core loss can be calculated with the core loss value per unit volume read from $P_{cv} - B_m$ curve and volume from datasheet of the selected core.
The same method is also applied on the series inductance core, but in this case, the current difference ΔI is used to calculate B_{max} by using equation 4.7.

$$B_{max} = \frac{1}{2}\Delta B = \frac{L_m \Delta I}{2 N_{turns} A} \tag{4.7}$$

The reason is that the duty cycle loss time which is the Δt in core loss calculation of series inductance core is more difficult to determine than the current difference ΔI in simulation plot exported from PSpice. Meanwhile, the volumes of the cores are different due to different series inductance values in T-Type and PSFB as discussed in section 3.7.1.4 and shown in table 3.2.

4.2.2.2 Copper Loss

The copper loss of the main cores is relevant to AC winding resistance value and rms currents as shown in the following equations,

$$P_{copper.p} = I_{prms}^2 R_{pAC} \tag{4.8}$$

$$P_{copper.s} = I_{srms}^2 R_{sAC} \tag{4.9}$$

where I_{prms} and I_{srms} are the rms currents going through primary and secondary sides winding of the transformer read from simulation files while R_{pAC} and R_{sAC} are AC winding resistance values of both sides which can be calculated with the copper wire parameters as mentioned in section 3.7.3.
For series inductance, the current value used in this calculation is the rms current in primary side winding as shown in equation 4.10, and the AC winding resistance is calculated using the same method since it is using the same type of wire as the main winding.

$$P_{copper.series} = I_{prms}^2 R_{series-AC} \tag{4.10}$$

5

Results and Discussion

This chapter mainly explains the simulation results including loss comparison, efficiency comparison and calculation results including transformer loss and simple cost comparison between different topologies. Comments are given besides each comparison.

5.1 Efficiency and loss comparison when only SiC switches are applied

The efficiency curve when both PSFB converter and T-type converter use SiC switches only is shown in Figure 5.1.

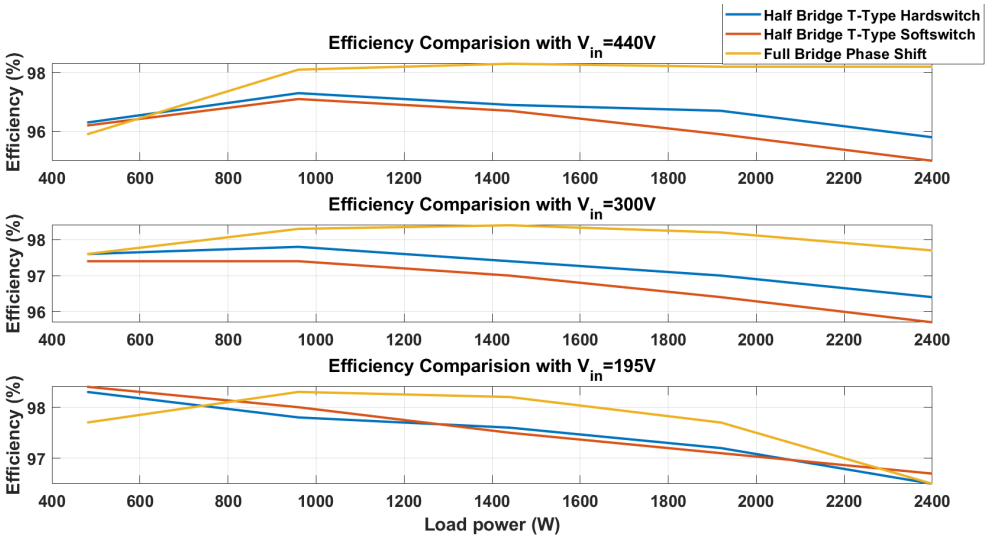

Figure 5.1: Efficiency with only SiC switches applied

In Figure 5.1, under three input voltage level (440V, 300V and 195V), operating points from 480W to 2400W are tested. The same range of testing is applied to another two testings that will be shown later. It can be seen from Figure 5.1 that for most of the operating points, PSFB converter performs better efficiency and only at very low load, T-type converters have higher efficiency.

Select one operating point and plot the bar chart of losses, as shown in Figure 5.2.

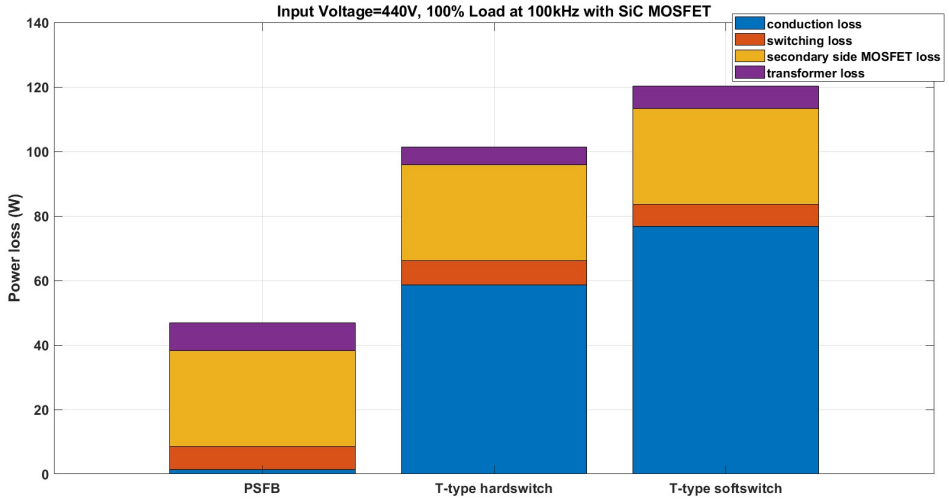

Figure 5.2: Losses at 440V,100% load (2400W) when only SiC switches are applied

Firstly, from Figure 5.2, it can be proved that the efficiency result for 440V, 100% load is correct. With equation:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} \tag{5.1}$$

Then there are:

$$\eta_{PSFB} = \frac{2400 - 45}{2400} = 98.1\% \tag{5.2}$$

$$\eta_{T_{hard}} = \frac{2400 - 101}{2400} = 95.8\% \tag{5.3}$$

$$\eta_{T_{soft}} = \frac{2400 - 120}{2400} = 95\% \tag{5.4}$$

Which prove that the loss analysis matches the efficiency test. Both of them are correct.
Then it can be seen from Figure 5.2 that the main reason for the loss difference at this operating point is the difference of conduction loss. This proves the theoretical comparison specified in 3.6, which is, the conduction loss of soft-switched T-type converter is always larger than that of PSFB converter, the conduction loss of hard-switched T-type converter is always smaller than that of soft-switched T-type converter due to the small leakage inductance. At this operating point, the conduction loss of hard-switched T-type converter is higher than that of PSFB converter since the load level is high, the condition specified in 3.6.4 that the load level should be small enough is not satisfied. It also can be seen that the total losses of their secondary side are the same because their secondary sides are fixed and operate exactly the same, and the transformer loss of PSFB converter is the highest which proves the comparison in 3.7.2.

The switching loss bars shown in Figure 5.2 is too narrow to be distinguished so they are enlarged in Figure 5.3.

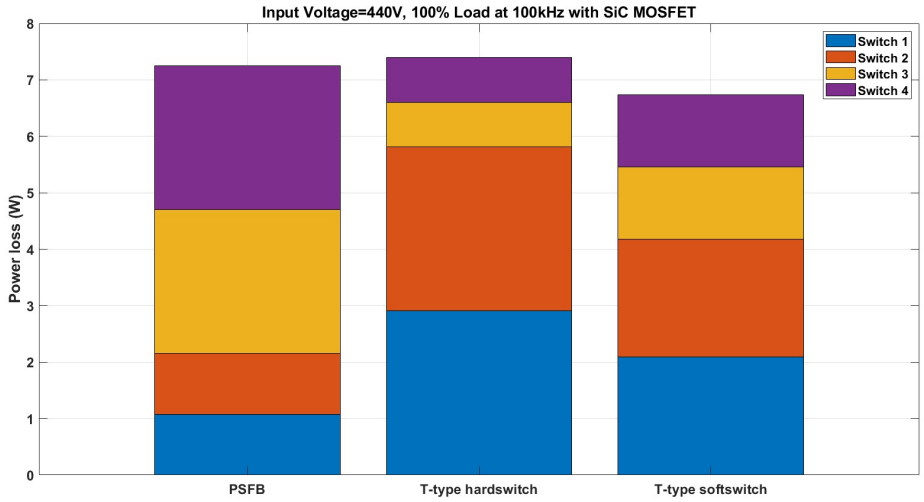

Figure 5.3: Enlarged switching loss bars

The switching loss of the hard-switched T-type converter is the highest due to the extra turning on loss of main switches S_1 & S_2, this can be seen compared with that of soft-switched T-type converter. And the switching loss of the switches on the leading leg of PSFB converter (S_3 & S_4) is almost the same as the switching loss of the main switches of soft-switched T-type converter (S_1 & S_2), because these switches are turned off at the same current and voltage level, which is at the time t_1. For the same reason, the switching loss of the lagging leg switches of PSFB converter (S_1 & S_2) and the switching loss of the middle switches of soft-switched T-type converter (S_3 & S_4) are almost the same as well because they are all turned off at time t_3, but the switching loss of the middle switches of hard-switched T-type converter is smaller than them because the small leakage inductance causes the current level of the switches, at the turning off time t_3, smaller than that two topologies.

5.2 Efficiency and loss comparison when T-type converters use Si middle switches

The motivations of using Si switches instead of SiC switches as the middle switches of the T-type converters are basically two reasons.
The first reason is, the middle switches of T-type converter only block $\frac{V_{dc}}{2}$. According to the testing range specified before, this voltage, at the maximum, will be $\frac{440}{2} = 220V$. After considering some margin, switches which can block 300V is proper to be selected as middle switches. But unfortunately, there is no SiC switch which can block 300V on the market nowadays. The SiC switches available on the market now only block much higher voltages. The SiC switches used in previous simulation are

all able to block 650V, which fits the voltage stress of the switches in PSFB converter and main switches of T-type converters (440V), but there is too much margin for the voltage stress of the middle switches of T-type converters (220V).
So from voltage stress aspect, 650V SiC is not proper for the middle switches of T-type converters. 300V Si is properer because is has both smaller voltage margin and cheaper cost.
The second reason is relevant to the conduction loss. As specified in 2.2.1, 3.3.2 and 3.6, in the freewheeling stage of T-type converter, the freewheeling current in the middle bridge goes through one MOSFET and the body diode of the other MOSFET. The on-state resistance of the MOSFET and the body diode resistance of the other MOSFET both contribute to the conduction loss. Focus on the body diode resistance, it can be seen from the data sheets of SiC switches and Si switches that the body diode resistance, at the operating points tested in this thesis, of the Si switch is much smaller than that of SiC switch, as shown in Figure 5.4 and Figure 5.5.

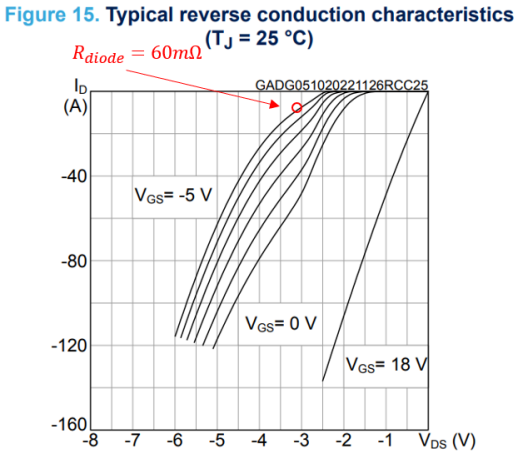

Figure 5.4: SiC switch STM SCT018H65G3AG

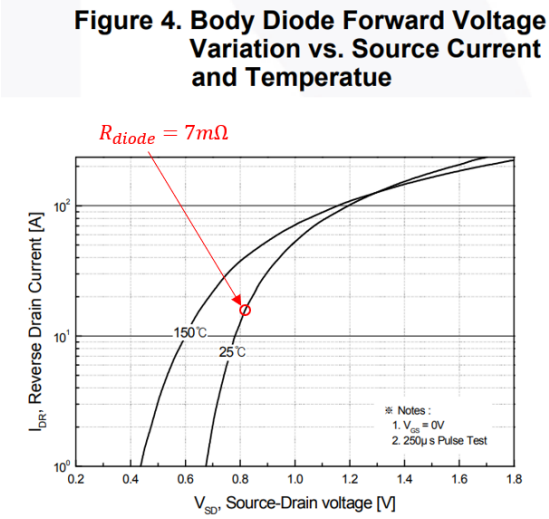

Figure 5.5: Si switch Onsemi FDA59N30

So it can be speculated that after changing SiC middle switches to Si middle switches, the conduction loss during the freewheeling stage of the T-type converters can be reduced. Of course the cost will be the increase of the switching loss because Si switches perform worse switching than SiC switches, but in the condition when conduction loss is dominant, the total loss still decreases.

Change to Si switch, select 440V, 100%load operating point, plot the bar chart of losses and compare with those using only SiC switches, as shown in Figure 5.6

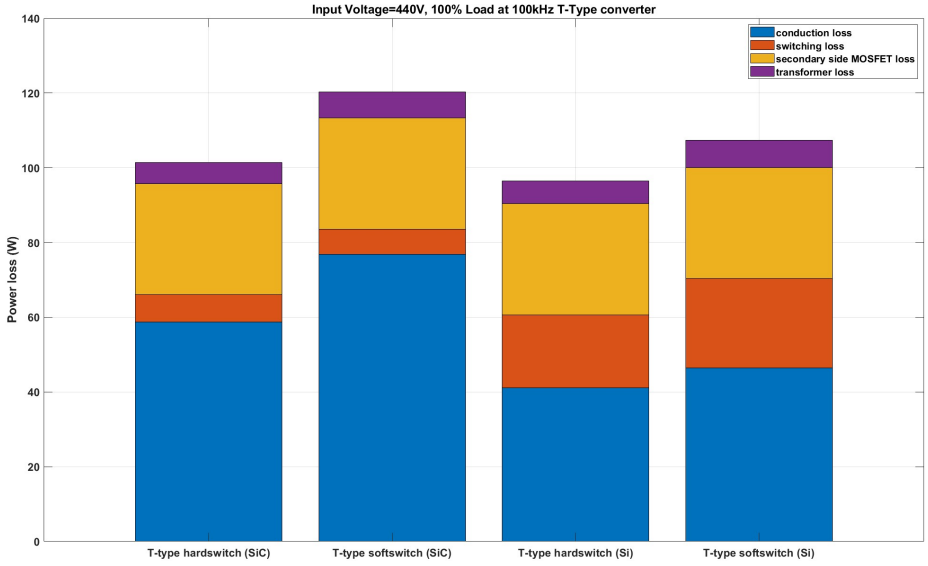

Figure 5.6: T-type converters losses comparison after using Si switches

It can be seen that the total loss for both hard-switched T-type converter and soft-switched T-type converter decreases, with the reduction of conduction loss and the increase of switching loss. From the efficiency curves shown in Figure 5.7, it can be seen that after using Si middle switches, there are more operating opints at which T-type converters perform better than PSFB converter compared with only SiC switches are applied. At the same time, since using Si switches reduces the conduction loss and increases the switching loss, the soft-switched T-type topology now suffers from less of its disadvantage and performs more of its advantage, according to the descriptions in section 3.5 and section 3.6.

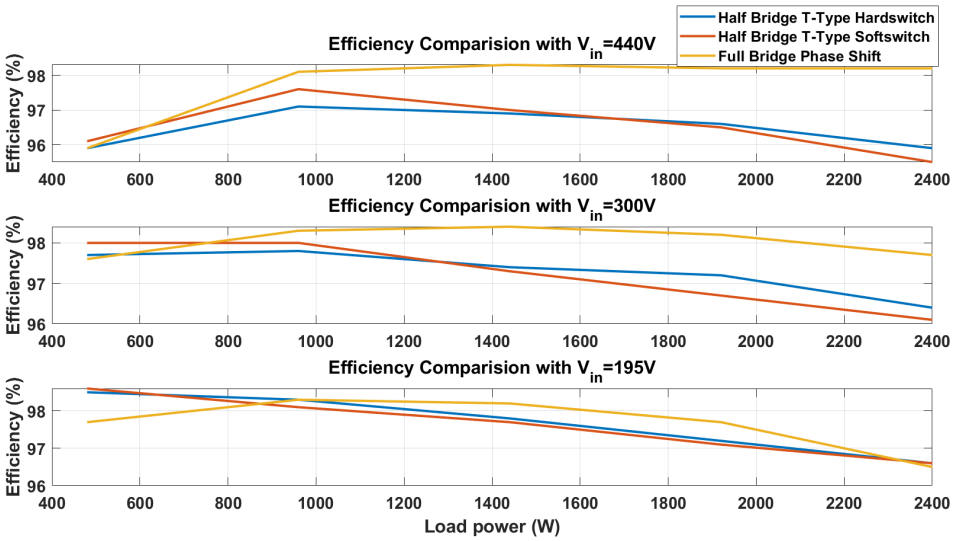

Figure 5.7: Efficiency when Si middle switches are applied to T-type converters

Select another operating point, 440V 20%load (480W) at which T-type converters perform better than PSFB converter and plot the bar chart of losses, as shown in Figure 5.8.

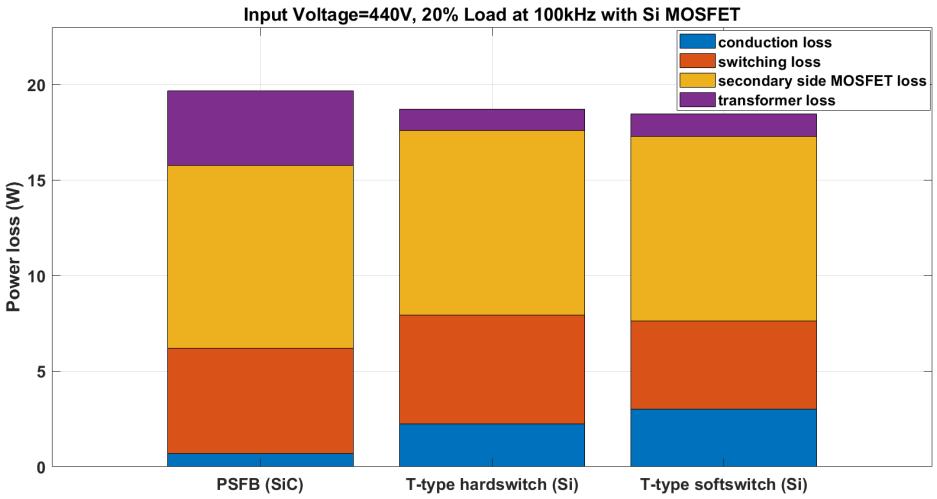

Figure 5.8: Losses at 440V, 20% load (480W) when Si middle switches are applied

Checking the loss analysis versus the efficiency test with equation 5.1, as:

$$\eta_{PSFB} = \frac{480 - 19.7}{480} = 95.9\% \tag{5.5}$$

$$\eta_{T_{hard}} = \frac{480 - 19.45}{480} = 95.9\% \tag{5.6}$$

$$\eta_{T_{soft}} = \frac{480 - 17.8}{480} = 96.1\% \tag{5.7}$$

Since in this operating point the conduction loss is too small compared with other losses while the transformer loss of PSFB converter is much larger than that of T-type converters, the total loss of T-type converters is smaller than that of PSFB converter, and T-type converters perform better efficiency.

5.3 Cost Comparison

The cost of PSFB and T-Type converter are basically the same since the secondary side components are fixed. However, there are still some differences due to the difference of transformers and the change of primary side MOSFETs. For transformer cost, since the transformers are formed with the same cores but different number of winding turns and groups, the cost difference only appears in the copper wires.
The total length of the copper wires can be calculated as shown in equation 5.8 and displayed in table 5.1 and 5.2. Finally, the total cost of each topology can be calculated as shown in Table 5.3.

$$L = \pi \cdot D \cdot N_{turns} \cdot N_{groups} \cdot N_{windings} \tag{5.8}$$

Table 5.1: Copper wire total length of PSFB

	Number of turns	Number of groups	Number of windings	Total Length
Series inductance	4	1	1	219.3mm
Primary winding	10	1	1	549.8mm
secondary winding	1	6	2	659.8mm

Table 5.2: Copper wire total length of T-Type soft switch converter

	Number of turns	Number of groups	Number of windings	Total Length
Series inductance	4	2	1	438.6mm
Primary winding	10	2	1	1099.6mm
secondary winding	2	6	2	1319.6mm

Table 5.3: Cost comparison between T-Type and PSFB

	T-Type (SiC)	T-Type (Si)	PSFB
Primary MOSFET ($)	67.88	41.66	67.88
Secondary MOSFET ($)	54.52	54.52	54.52
Transformer core ($)	3.14	3.14	3.14
Winding wire ($)	0.5	0.5	0.25
Output filter ($)	3.22	3.22	3.22
Total cost ($)	129.26	103.04	129.01

Therefore, it can be easily seen that T-Type converter with Si MOSFETs in the middle bridge has the lowest cost.

6

Conclusion and Future Work

In this chapter, nine conclusion got from previous discussions and simulations are made. While another topology, Full-Bridge T-type converter, will be introduced as future work.

6.1 Conclusion of Present Work

According to previous discussion and simulation results, five conclusions can be made:
1. The conduction loss of hard-switched T-type converter is always lower than that of soft-switched T-type converter due to the smaller primary side inductance. But the cost is extra switching loss.
2. When conduction loss is dominant, the efficiency of hard-switched T-type converter is higher than soft-switched T-type converter. When switching loss is dominant, soft-switched T-type converter performs better.
3. The total transformer loss of T-type converter is lower than that of PSFB converter due to its low core loss.
4. If only SiC switches are applied to both topologies, at most of the operating points, PSFB converter performs better efficiency.
5. If 300V Si switches are applied to T-type converters as middle switches, T-type converters perform better efficiency than PSFB converter in low load range.

6.2 Future Work

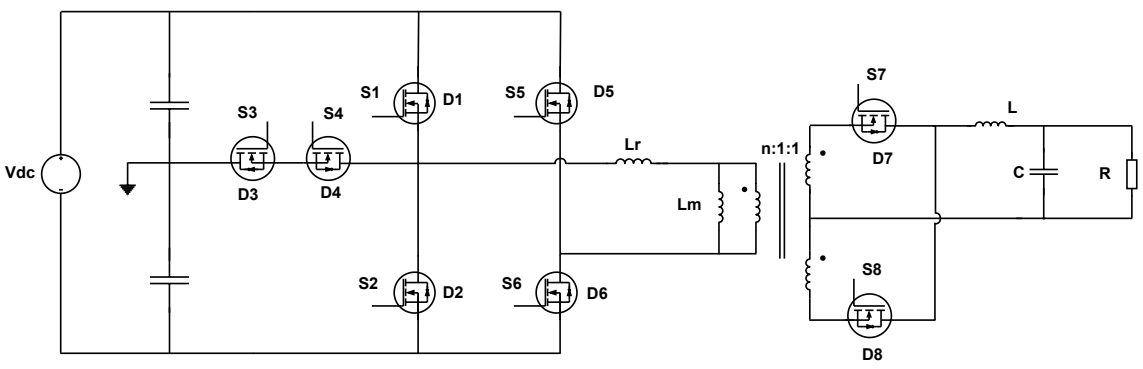

Figure 6.1: Full Bridge T-Type Converter

A new topology, named as Full-Bridge T-type converter, is shown in Figure 6.1. This topology is the combination of Full-Bridge converter and T-type converter and is selected as future work due to three potentials specified below.

6.2.1 Wide input voltage range

According to 3.1, for Full-Bridge converter, if the input voltage is V_{dc}, then the transformer primary side voltage of it, within the duty cycle, is also V_{dc}, but for T-type converter, this value is $\frac{V_{dc}}{2}$. On the other hand, this means if a transformer has fixed primary side voltage V_p during the duty cycle, when a Full-Bridge converter is applied on its left side, the input voltage range of the converter will be $0V \sim V_{dc}$, but if a T-type converter is applied, then the input voltage range will be $0V \sim 2V_{dc}$. By combining the two converters together and properly arrange the switching pattern, it can be realized that when the input voltage is low, Full-Bridge mode operates and when the input voltage is high, T-type mode operates. In 3.6.4, it is already specified that when input voltage is high, T-type converter generates lower conduction loss within low load range, which gives theoretical support to the proposal above.
One another advantage of the enlarged input voltage range is the avoidance of losing gate signal. According to Equation 3.1, when V_o is fixed, then:

$$D_{eff} = \frac{nV_o}{V_p} \tag{6.1}$$

If the input voltage is V_{dc} and V_o is very small, then if Full-Bridge converter is applied, D_{eff} will be equal to:

$$D_{eff} = \frac{nV_o}{V_{dc}} \tag{6.2}$$

Which is a quite small value. Theoretically, any D_{eff} between 0 and 1 is acceptable, but in practical converters, when the D_{eff} is very small, there is a risk that the gate signal will be wrongly generated which will disturb the whole operation.
But in T-type converter, under the same condition, D_{eff} will be equal to:

$$\begin{aligned} D_{eff} &= \frac{nV_o}{\frac{V_{dc}}{2}} \\ &= 2\frac{nV_o}{V_{dc}} \end{aligned} \tag{6.3}$$

Which is double of that of Full-Bridge converter, since the D_{eff} is doubled, there will be lower risk that gate signal be generated wrongly. According to the proposal of the switching pattern specified above, when the input voltage V_{dc} is low, the circuit operates in Full-Bridge mode, then when the input voltage is getting higher and higher, before it reaches to a dangerous value at which wrong gate signals might be generated, switch the circuit to T-type mode, then the D_{eff} will be doubled and reduce the risk of generating wrong signals.

6.2.2 No saturation

One disadvantage of Full-Bridge converter which is widely known is the risk of saturation.

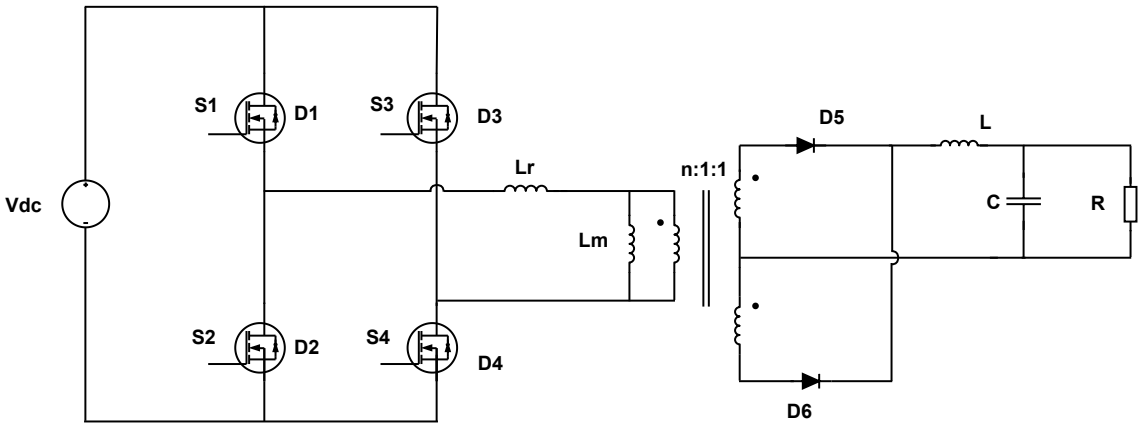

Figure 6.2: Full-Bridge converter

In Figure 6.2, to avoid saturation, the duty cycle of $S_1\&S_4$ and $S_2\&S_3$ must be exactly the same. Because once they are different, the time difference will result in extra magnetizing or demagnetizing (when $S_1\&S_4$ are conducting, the transformer core is magnetized, when $S_2\&S_3$ are conducting, the transformer core is demagnetized) in the transformer core. The extra magnetizing or demagnetizing accumulates along with the repeating of switching period and finally results in saturation. The saturation can be avoided only when the duty cycle of $S_1\&S_4$ and $S_2\&S_3$ are exactly the same, which gives difficulties to the controlling of the gate signals.
But when T-type (Half-Bridge) structure is applied, when the duty cycle of $S_1\&S_4$ and $S_2\&S_3$ are not equal, it results in the voltage difference between the two clamping capacitors. Due to this voltage difference, the extra magnetizing or demagnetizing generated in Full-Bridge mode can be eliminated by the extra demagnetizing or magnetizing in T-type mode afterwards, which avoids the saturation.

6.2.3 Reduce the voltage stress of secondary side switches

According to 2.3, for both PSFB converter and T-type converter, during the energy transfer stage, one secondary side switch conducts while the other one blocks $\frac{2V_p}{n}$. For PSFB converter, since $V_p = V_{dc}$, then the voltage stress on that switch will be $\frac{2V_{dc}}{n}$. But for T-type converter, since $V_p = \frac{V_{dc}}{2}$, the voltage stress will be $\frac{V_dc}{n}$. In T-type mode, the voltage stress on secondary side switches is half of the voltage stress in PSFB mode. Which gives the same proposal as specified in 6.2.1 that, when the input voltage is getting higher, switch the circuit to T-type mode to reduce the secondary side voltage stress.

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A

Appendix 1

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