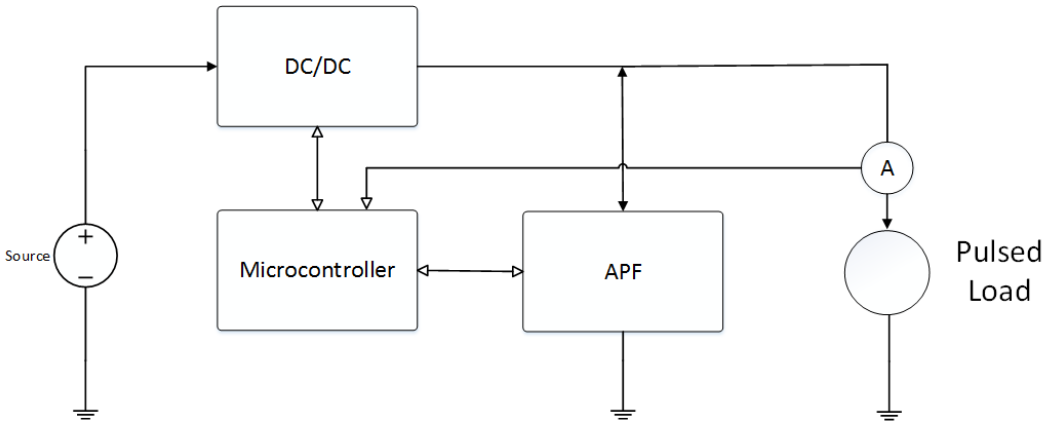
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Multi Loop Digital Control for Active Filter and DC/DC Converter

Master of Science Thesis

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Department of Energy & Environment
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CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2015

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Cover: System view of the DCDC converter as well as the digitally controlled active filter.

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Abstract

AESA radar systems are heavily pulsed and often equipped with large capacitor banks to be able to supply the load with enough current and to not put extra stress on the supply. The goal of this thesis was to implement a digital control for the existing step-down converter as well as implementing a digitally controlled active filter in parallel with the existing step-down converter. The developed filter was able to supply the load fast enough without using the extra capacitor bank normally used. The goal was also to have close to zero amps in fluctuations on the input bus. The obtained end result was fluctuations of about 40 mA compared to 60 mA in the thesis "Digitally Controlled Active Power Filter" including the capacitor bank. The maximum output voltage diversion was 300 mV during the pulse and 40 mV in steady state. Also the efficiency was improved to 66% when comparing the complete system with the system in the former work [1].

Index Terms: Pulsed, DSP, Micro controller, PCMC, Boost converter, Active filter

Acknowledgements

We would especially like to thank Johan Ringqvist for all the help, guidance and patience during this master thesis. Thanks also goes out to all the people we "borrowed" equipment from in the lab and that more than willingly helped us with any question. Thanks to our supervisor Torbjörn Thiringer at Chalmers. We also thank Stefan Linders and Valter Nilson for making this thesis possible in the first place.

Kristoffer Andersson
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Acronyms

ADC Analog to Digital Converter. 30, 33

AESA Active Electronically Scanned Array. 2

APF Active Power Filter. 2, 21, 23, 33, 44, 48

BOM Bill Of Materials. 24

BUCK Step-down Converter. 2, 5

CCM Continuous Conduction Mode. 5–7, 9, 10, 17, 23, 25

CPU Central Processing Unit. 34

DAC Digital to Analog Converter. 30, 35

DCDC Converter for DC systems. 2, 21–23, 48

DCM Discontinuous Conduction Mode. 5, 28

DSP Digital Signal Processor. iii, 25

ePWM extended Pulse Width Modulation. 34

FCCM Forced Continuous Conduction Mode. 10, 46

MCU Microcontroller Unit. 29–35

PCMC Peak Current Mode Control. 14

PWM Pulse Width Modulation. 4

RHP Right Half Plane. 18

RMS Root Mean Square. 44, 47

1

Introduction

1.1 Background

SAAB Electronic Defence System develops an AESA, Active Electronically Scanned Array, radar system. Apart from conventional radar systems the, AESA radar consists of non-moving parts. These systems can be used on mobile carriers which make power efficiency and physical size an important parameter. Improvements in these areas can be done by designing a digitally controlled active power filter (APF). An APF enables stable current and voltage levels which will minimize losses, interference with other electronic systems as well as increase performance. Since the APF is very beneficial considering the improvements in power quality, it is in Saab's interest to develop such a system for use in future radar systems.

1.2 Previous Work

In the previous work described in [5] and [1], investigation and implementation of digital control for a DCDC BUCK converter and later Samuel and co. developed and implemented an active filter which was digitally controlled. The implementation of the APF in [1] is done separately from the DCDC converter, meaning that the control for the DCDC is in a separate circuit than the APF control. Also, the performance of the APF is not high enough to be able to exclude the external passive power filter of $1100\mu F$ and still retrieve as low current fluctuations on the 56 V bus as requested.

1.3 Purpose

The purpose of this project is to design one digital control system to control an existing DCDC converter as well as an active power filter which will also be designed during this project. The digital control system is to be implemented in a micro controller. The active

power filter is to be designed and implemented in hardware; additional systems such as a real-time measurement interface will also be designed and implemented in hardware. The complete system should be more energy efficient than the previous system, and also with reduced size. The APF and the DCDC converter should minimize the content of current harmonics reflected back to the DC supply system.

1.4 Scope

In the process of designing the system the efficiency have been regarded, as to what can be improved or changed to retrieve better efficiency for a finalized prototype. Even if one main goal of the project is to reduce the size of the system, the actual size of the prototype is not of importance.

2

Theory

This section will introduce the active electronically scanned array (AESA) radar and explain it's characteristics and the importance is has for this thesis. Following is the theory of the converter topologies and their different modes of operations. Lastly the controller theory will be presented.

2.1 Active Electronically Scanned Array (AESA)

An AESA consists of Small transmitter/receiver modules (antennas), that is working together. The AESA can consist of many modules, i.e., about a thousand as in the Gripen E[3]. The load characteristics of a module is pulsed because the power to the transmitter/receiver is commonly regulated with a switch. The pulse period and duty cycle for this thesis will be the same as in last years thesis[1]. That means a pulse period of 3 ms with a duty cycle of 10% and an amplitude of 1.5 A.

2.2 Converter Topology

The circuit is assumed to be ideal, meaning that there are no losses in the components, which implies that the output power is equal to the input power. Also assumed is steady state, meaning that the next and following periods are the same. In dc-dc converters the average output voltage is controlled to a desired level even though the input or output might vary. This is accomplished by controlling the duration of the on and off time of one or more switches.

One method to control the switches are called pulse width modulation (PWM). The switching frequency is fixed and thus also the switching period. Varying the on-time of the switch controls the output average voltage. The duty cycle D is the ratio between the

switch on-time and the switch period[9]. There are two modes of operation when dealing with switched mode power supplies. Continuous conduction mode (CCM) which means that the current through the inductor always is flowing. Discontinuous conduction mode (DCM) which is when the energy in the inductor is completely depleted and no longer can hold a magnetic field.

2.2.1 Buck (Step Down) Converter

When the average output voltage needs to be lower than the input voltage, the step-down (BUCK) converter can be used. The buck converter topology can be seen in Figure 2.1. When the switch is on the diode is reverse biased and the voltage over the inductor is $V_d - V_0$. During t_{on} the input is supplying the inductor as well as the output with energy.

When constant voltage is applied over the inductor the current is increasing linearly, which can be seen in Figure 2.2. When the switch is off during the t_{off} interval, the current still flows through the inductor, but because the voltage over the inductor now is $-V_o$ the current is decreasing linearly. The diode is forward biased and the output is supplied from the capacitor as well as the inductor. The current in the inductor is flowing continuously, therefore the converter is in CCM[9].

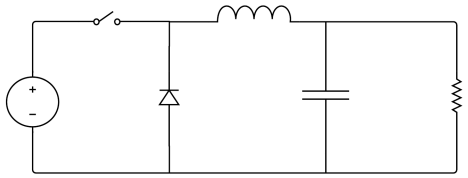


Figure 2.1: Step-down topology (Buck)

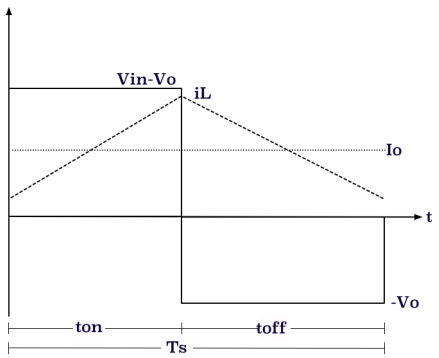


Figure 2.2: Inductor voltage and current in continuous conduction mode.

Because of steady state, the average inductor voltage over one period is zero. There-

fore, when integrating v_L over one switching period, the result is

$$\int_0^{T_s} v_L(t)\,dt = \int_0^{t_{on}} v_L(t)\,dt + \int_{t_{on}}^{T_s} v_L(t)\,dt = 0 \tag{2.1}$$

Because the duty cycle is equal to t_{on}/T_s, the relation of the input voltage, output voltage and duty cycle, in continuous conduction mode, is given by

$$V_o = D\,V_d \tag{2.2}$$

Boundary between CCM - DCM

At the border of CCM and DCM the current is decreased to zero just at the end of the off-period. The waveforms can be seen in Figure 2.3. To keep the converter in CCM operation the current has to full-fill

$$\frac{\Delta i_L}{2} \leq I_o \tag{2.3}$$

where Δi_L is the peak current in the inductor, which is derived from

$$V_L = \frac{L\Delta i_L}{DT} \tag{2.4}$$

Combining (2.3) and (2.4) results in

$$I_o = \frac{V_d D T_s}{2L}(1-D) \tag{2.5}$$

from which the smallest output current can be calculated, given a V_d, D, T_s and L, that is needed to keep the converter in CCM.

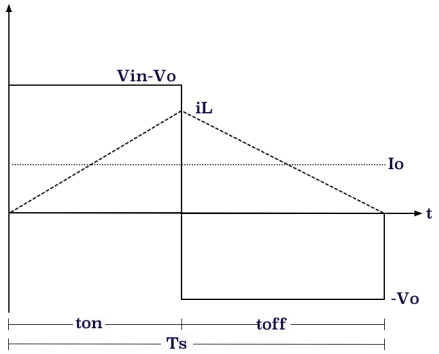


Figure 2.3: Inductor voltage and current at the border of CCM - DCM.

The minimum current needed for keeping the inductor in the continuous region at all times, considering that the maximum is at a duty cycle of 1/2 [9], (2.5) is therefore simplified to

$$I_{o,max} = \frac{T_s V_d}{8L} \tag{2.6}$$

DCM

If the inductor current initially is at the border of CCM according to Figure 2.3 and L, T, V_d and D are the same. If the load decreases, such as the current decreases, the converter will be in discontinuous conduction mode because the inductor will be depleted of its energy and according to Figure (2.4), the current is then zero during the $\Delta_2 T_s$ interval. The output is now supplied only by the output capacitor. Integrating the inductor voltage the same way as for 2.1 yields

$$\frac{V_o}{V_d} = \frac{D}{D + \Delta_1} \tag{2.7}$$

To end up with the equation for the final output voltage in DCM, (2.6), (2.7) and (2.4), but with Δ_1 instead of D and V_o instead of the V_L, has to be combined to get the final equation

$$V_o = \frac{V_d}{\frac{2LI_o}{D^2 V_d T_s} + 1} \tag{2.8}$$

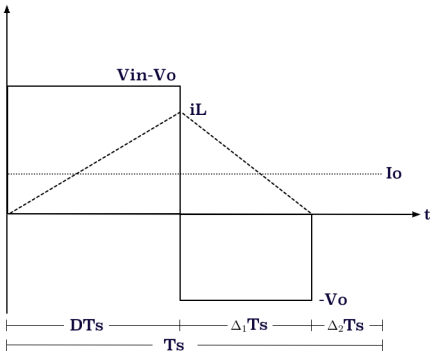


Figure 2.4: Inductor voltage and current in discontinuous conduction mode.

2.2.2 Boost (Step Up) Converter

In a step-up (Boost) converter the output voltage is always greater than the input voltage. The converter topology can be seen in Figure 2.5. The voltage and current waveforms for the inductor can be seen in Figure 2.6. When the switch is conducting, the inductor is charged with the input voltage. The diode is reverse biased and the output is supplied by the output capacitor. When the switch is off, the output is supplied with energy from the charged inductor as well as from the input.

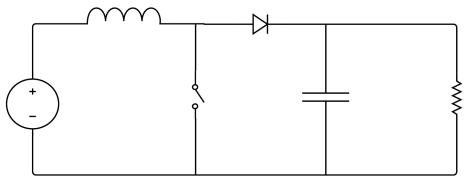


Figure 2.5: Boost converter topology.

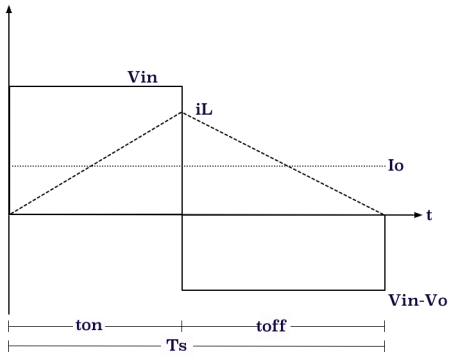


Figure 2.6: Voltage and current waveforms for the inductor in the Boost topology.

CCM

In steady state and in continuous conduction mode the inductor current never stops flowing. Since the operation is in steady state, the average voltage during one period is zero. Thus when integrating the voltage over the inductor with respect to time, the same method as for (2.1), this results in

$$\frac{V_o}{V_d} = \frac{1}{1-D} \tag{2.9}$$

and when assuming lossless circuit elements the current relation is

$$\frac{I_o}{I_d} = (1-D) \tag{2.10}$$

Border CCM - DCM

At the border between continuous and discontinuous conduction mode the inductor current, at the end of the off-period, goes to zero. At this boundary the average inductor current is given by the standard inductor formula combined with (2.9) and the boundary limit criteria $\Delta_{i_L}/2 = I_o$ which yields

$$I_{LB} = \frac{T_s V_o}{2L} D(1-D) \tag{2.11}$$

Because the inductor current is the same as the input current in a boost converter, and by using Equation (2.10) and (2.11) the expression for the average output current at the border of CCM and DCM is

$$I_{oB} = \frac{T_s V_o}{2L} D(1-D)^2 \tag{2.12}$$

When varying the Duty cycle and keeping the other parameters constant in the former two equations, it is apparent that the current has a maximum. The maximum for I_{LB} is at a duty cycle of 1/2 and for I_{oB} it is 1/3. Using this values in the former equations yields

$$I_{LB,max} = \frac{T_s V_o}{8L} \tag{2.13}$$

and

$$I_{oB,max} = \frac{2}{27} \frac{T_s V_o}{L} \tag{2.14}$$

To keep the converter in continous mode for all variations of duty cycles the former equations needs to be be fullfilled, such that the current never is less than the calculated value[9]

DCM

If the load is too small to fullfill the criteria for the least current of Equation (2.14), the converter enters DCM. The waveforms for the DCM mode can be seen in Figure 2.7. If integrating the inductor voltage over one period and setting it to zero, because the average voltage over the inductor in steady state is zero, the result is

$$\frac{V_o}{V_d} = \frac{\Delta_1 + D}{\Delta_1} \tag{2.15}$$

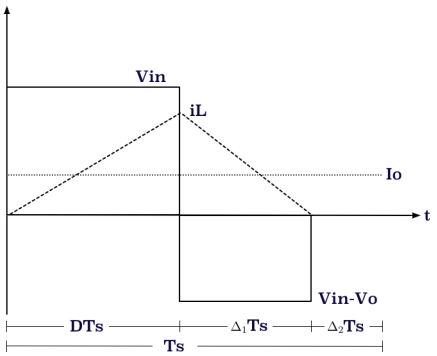


Figure 2.7: Voltage and current waveforms for discontinuous conduction mode in the Boost converter.

Using the assumtion that the circuit is lossless such that the input power is equal to the output power yields

$$\frac{I_o}{I_d} = \frac{\Delta_1}{\Delta_1 + D} \tag{2.16}$$

The inductor current which is the same as the average input current is utilized from Figure 2.7 to retrieve

$$I_d = \frac{V_d}{2L} D T_s (D + \Delta_1) \tag{2.17}$$

Using the former equations to get an expression for the duty cycle yields

$$D = \left(\frac{4}{27} \frac{V_o}{V_d} \left(\frac{V_o}{V_d} - 1 \right) \frac{I_o}{I_{oB,max}} \right)^{1/2} \tag{2.18}$$

2.2.3 Synchronous switching

The forward voltage drop of the diode in the buck and boost converter contribute to lowering the efficiency. This is especially apparent in low voltage systems. The loss can be decreased by using a Schottky diode instead of a normal diode to reduce the voltage drop. The better solution for reducing the voltage drop is by using a transistor with low on resistance. This solution improves the efficiency but complicates the control system for the circuit, i.e, a dead band has to be introduced to keep the transistors from conducting at the same time and causing a shot through[11][9].

When utilizing an extra switch in the converter design and when at low output load, such that the converter would normally enter DCM, the converter now can enter a mode called forced continuous conduction mode (FCCM), where the current changes direction in the inductor. There are some positives for using FCCM and one of them is that the equations derived earlier for CCM mode still applies to FCCM. One of the drawbacks is that the efficiency is poorer[8].

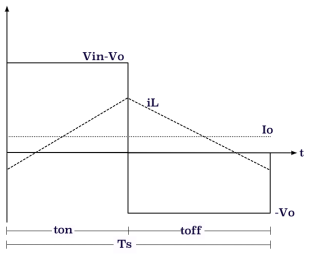


Figure 2.8: Waveforms for the forced continuous conduction mode (FCCM). Note how the inductor current changes direction.

2.2.4 Non ideal parameters(Losses)

The converter theory in the former sections is only dealing with ideal components just to make the equations and the principles of the converters easy to follow. This short

section will present some of the non-idealities that are important for this thesis.

The switches, MOSFETs used in this thesis, possess a bunch of non ideal parameters i.e., conduction losses due to R_{DSon}, delay for turning on due to stray capacitance and switching losses due to the time it takes for the current to decrease to zero; the overlap of voltage and current is causing losses[9].

2.3 Current measurement

Current can be measured with the technique of sensing the voltage drop over a resistor, then amplifying the signal with a operational amplifier set up to amplify the difference in voltage. The voltage measured over the resistor is relative to the current flowing through it. To accurately measure and amplify the differential signal the common mode signal has to be rejected (CMRR). To yield a good CMRR the resistor network surrounding the operational amplifier, as can be seen in figure 2.9, has to consist of precision resistors. If the actual resistance deviates the CMRR is degraded. For a deviation of 0.01 or 0.1 % in any resistor, the CMRR is degraded to 86 and 66 dB[4] respectively. Comparably, the CMRR for a dedicated current sense amplifier easily reaches 100 dB and over.

To accurately measure a signal and to be able to use it in a fast switching circuit the measurement circuit has to be able to measure with high enough bandwidth and also keep the delay to a minimum. The sense resistor can be placed either on the low side, meaning that it is connected with one side to ground and the other at, for example the switch node in a buck converter. This setup makes some faults undetectable because the current can go through other components than the sense resistor. Also in this setup the ground gets added resistance. Using the sense resistor on the high side has the drawback that the amplifier has to be able to handle the high side common voltage. The advantage is that all faults can be detected in contrast to the low side sense[4].

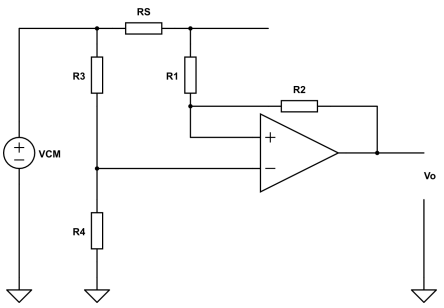


Figure 2.9: Generic Operational amplifier in differential setup.

2.4 Control theory

A brief introduction to stability and the fundamental theory for stable control systems which the control design is based on. This chapter also features a description of the control method used and a description of the control implementation.

2.4.1 Stability

To determine whether an LTI-system is stable or not the *Nyquist criterion* can be used. This can be applied to converter models to determine stability. For this project as for most other circuit systems model uncertainties and delays in measurement and driver circuitry can affect the stability of the system. Therefore it is desirable to determine

stability margins to design the compensator to ensure stability with delays and uncertainties. *Phase margin* and *gain margin* are measures of relative stability[6]. They can be used to determine how far from instability a system is and can be seen in the Nyquist plot in 2.10. Let G(s) be an an example system.

$$G(s) = \frac{20}{s(s+6)(s+2)} \tag{2.19}$$

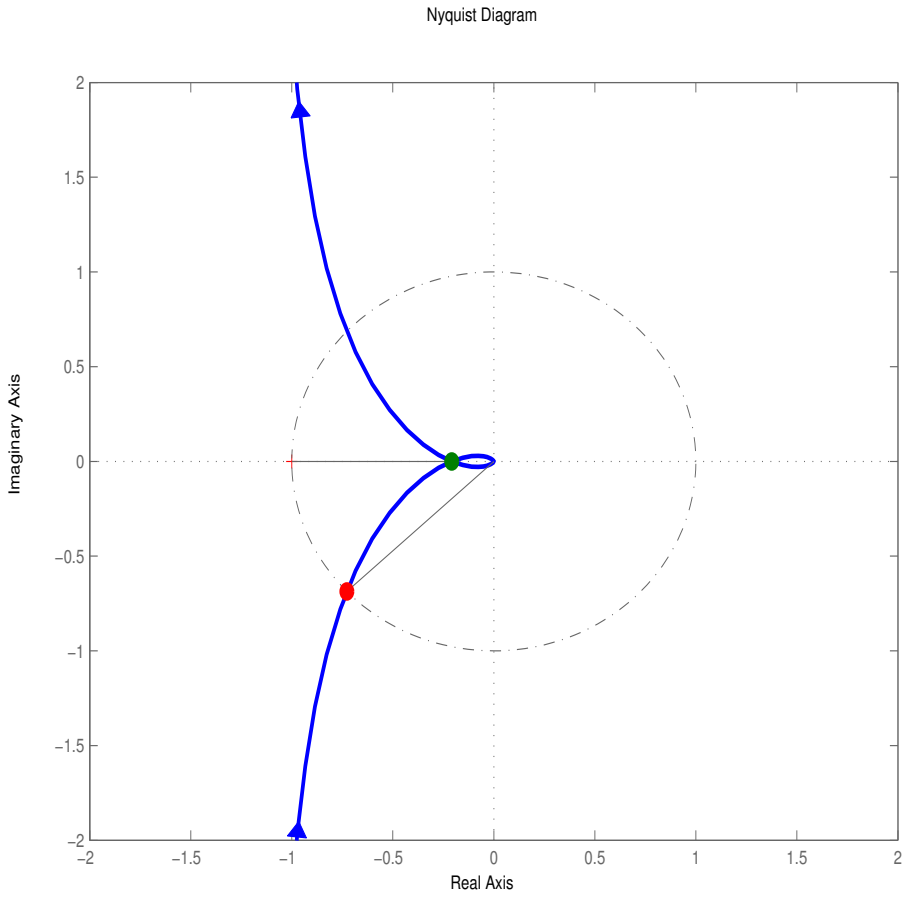


Figure 2.10: Nyquist plot of the system G(s)

In 2.10, a red dot representing the crossing of the frequency response and the unit circle and a green dot representing the crossing of the frequency response and the -180^o line i.e. the negative real axis. The phase margin is the angle between the line from the origin and the red dot and the line from the origin to the red cross which is the -1 point on the negative real axis. I.e. the phase margin is the angle that the phase of the frequency response has to move in order to reach the point of the verge of instability.

The gain margin is the distance between the green dot and the red cross. I.e. how much the gain of the frequency response has to move in order to reach the point of the border of instability. The phase margin and gain margin can also be seen in a bode plot as in 2.11.

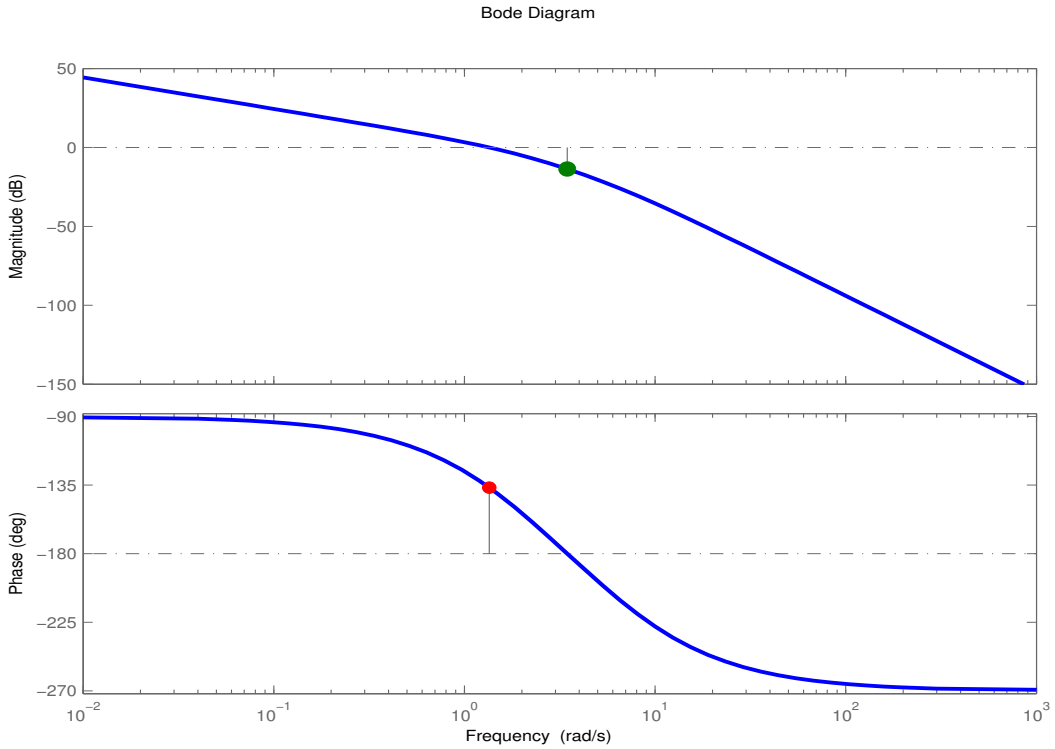


Figure 2.11: Bode plot of the system G(s)

The phase margin and gain margin for the system G(s) can be extracted from the matlab command *margin*:

$$P_m = 43.35^o \tag{2.20}$$

$$G_m = 13.63\text{dB} \tag{2.21}$$

2.4.2 Peak Current Mode Control

Current mode control is the industrial standard control method with several benefits compared to voltage mode control[12]. There are different variations of current mode control(e.g. peak-, average-, valley-CMC) in this section the concept, application and benefits of PCMC will be explained.

Peak current mode control has two control loops, one voltage feedback loop containing a compensator and is used to produce an error to achieve a certain output voltage. The other loop is a fast current loop which senses the inductor current through a sense resistor. The sensed current is then compared with the error voltage from the voltage feedback loop in a comparator which produces a control signal to the MOSFETs. The control signal is a one or a zero which will put the converter in on or off mode which will with time make the output equal to the reference.

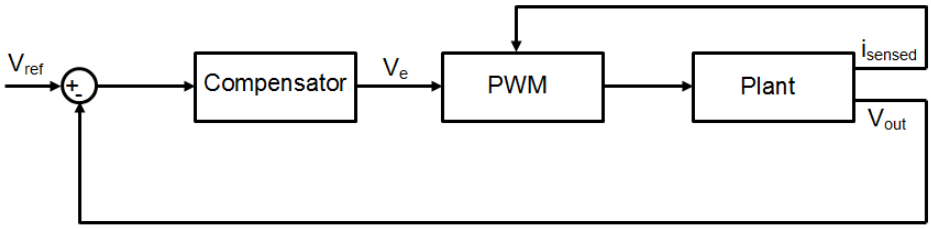


Figure 2.12: Control system overview

Figure 2.12 is an overview control system with the two loops described above. This is just the general description and since this project will implement this control method in a micro controller the focus will be to explain digital peak current mode control. Figure 2.13 illustrates a typical digital peak current mode controlled buck converter.

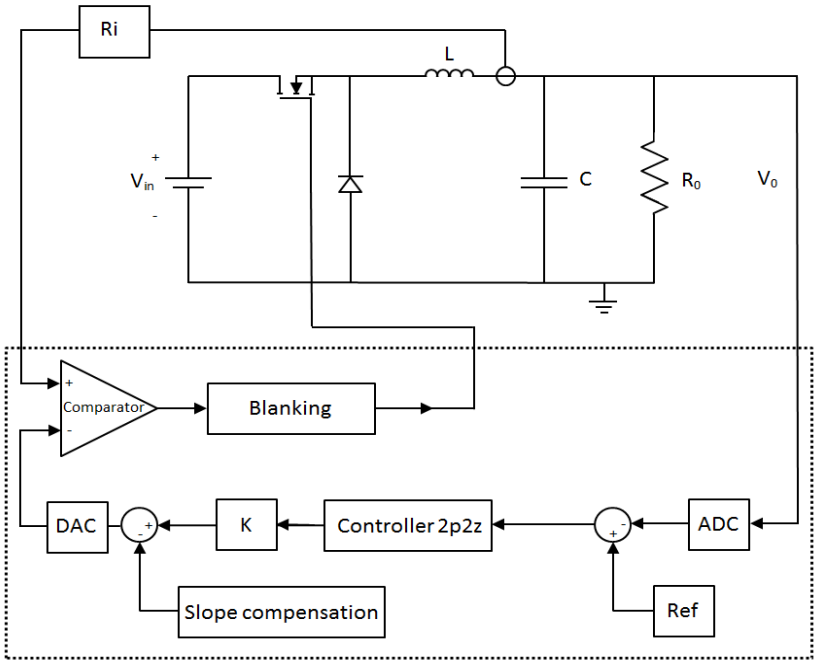


Figure 2.13: Digital Peak Current Mode Control overview

The inductor current is detected through the sense resistance R_i and fed to the comparator. On the other input of the comparator, the output voltage is fed to an analog-to-digital module which samples the continuous value to a discrete value. This value is then subtracted from a reference in order to produce an error which is fed to the compensator. The compensator output is then fed to a digital-to-analog module which produces a continues signal from the discrete value. The comparison of the comparator

is used to produce the control signal which switches the circuit between the on-state and off-state. These three signals are illustrated in 2.14.

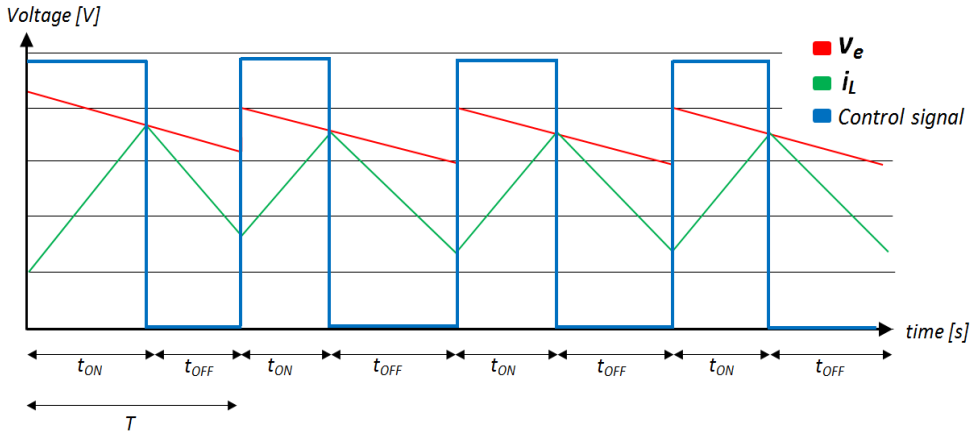


Figure 2.14: V_e vs. i_L

The circuit is in the on-state with increasing inductor current until the current equals the reference value V_e then the circuit is switched to the off-state and the inductor current starts to decrease until the beginning of next period T_s. Every new period starts with putting the circuit to the on-state and then this process repeats itself. Even though this is digital peak current mode control this comparison is done analogously since it is much faster than a digital comparison which can only occur every clock cycle.

The output signal from the compensator will remain constant during the period, however, it is needed in peak current mode control to add an external ramp, this is known as slope compensation. The current loop from peak current mode control has a high frequency double pole, which can be seen in 2.22, which will emerge at half the switching frequency. This will cause subharmonic oscillations when the control signal has a duty cycle of above 50 percent. In 2.23, m_c is the slope compensation factor which is set to $\frac{2}{\pi}$ in order to damp oscillation within one switching cycle[12].

$$1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2} \tag{2.22}$$

$$Q_p = \frac{1}{\pi(m_c(1-D) - 0.5)} \tag{2.23}$$

Another issue that can occur in digital peak current mode is when the circuit is switched on in the beginning of each period the sensed inductor current can produce a large peak which can cause the comparator to turn the circuit into off-state prematurely. Leading edge blanking is used which basically ignores these peaks at the beginning of each period in order to get proper control of the circuit.

Some of the benefits of peak current mode control are current limiting, a fast response and

simplified modeling, the latter will be further understood later in the report. The current limiting property exists since the reference from the compensator will put the circuit in the off-state when the current equals the reference, then current cannot reach undesired levels which is not the case for voltage control where the current is not measured at all and can still for small duty cycles in the control signal reach high levels and cause damage to the circuit.

This control method also allows for large duty cycles for a few switch cycles to increase the inductor current to desired levels without interference from the compensator. If the inductor current is very low the voltage will decrease which will be compensated by the compensator but it will take additional time and will depend on the crossover frequency of the controller. A digitally implemented compensator can be initialized to a known steady state output and within one switch cycle increase the inductor current to a satisfactory level.

2.5 Modeling

The purpose of the modeling is to determine the behavior of the system for the chosen component values and then design suitable compensator's to get a desired closed loop system behavior. Models for a CCM buck converter will be formulated because the APF buck converter will operate in CCM. The general approach for the modeling use simple models from articles to maintain understanding and then verify the models with simulations.

2.5.1 CCM Buck Converter

It is enough to model the CCM buck converter as a single-pole system where the double-pole system is the normal approach for small-signal buck models. This is due to the control method used, the inductor current loop together with the normal outer voltage loop allows the inductor to been considered as a current source[12][10]. Hence only the RC filter determines the frequency response characteristics of the converter. In 2.15 is a display of a typical buck converter. The small-signal transfer function for the buck converter is:

$$G(s) = \frac{R_0}{R_i} \frac{1 + \frac{s}{\omega_{esr}}}{1 + \frac{s}{\omega_{RC}}} \tag{2.24}$$

where:

$$\omega_{esr} = \frac{1}{R_C C} \tag{2.25}$$

$$\omega_{RC} = \frac{1}{R_0 C} + \frac{T_s(m_c(1-D) - 0.5)}{LC} \tag{2.26}$$

where D is the steady state duty cycle and m_c is the slope compensation factor.

$$D = \frac{V_0}{V_{in}} \tag{2.27}$$

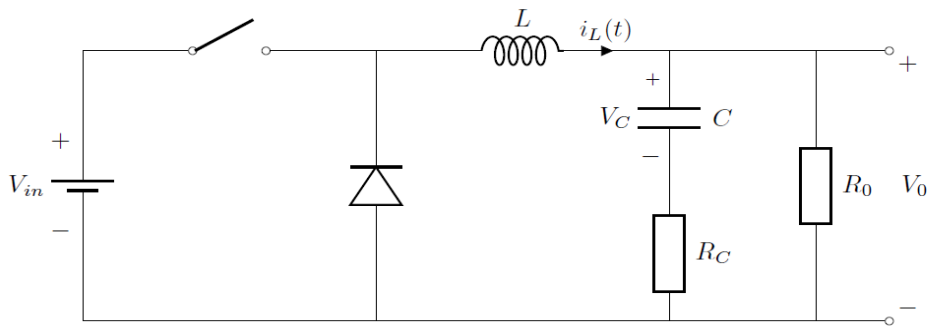


Figure 2.15: Buck Converter

$$m_c = 1 + \frac{S_e}{S_n} \tag{2.28}$$

S_e is the external ramp and S_n is the natural ramp of the inductor current.

$$S_n = \frac{(V_{in} - V_0)R_i}{L} \tag{2.29}$$

2.30 models the inductor current sampling effect as well as the the impact of the slope compensation on the small-signal response. The high frequency pole pair emerges at half the switching frequency ω_n and the damping Q_p depends on the duty cycle and the slope compensation factor.

$$1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2} \tag{2.30}$$

$$Q_p = \frac{1}{\pi(m_c(1-D) - 0.5)} \tag{2.31}$$

The high frequency pole pair will for D = 0 be complex and will for duty cycles D $>$ 0.5 emerge at the RHP, causing sub-harmonic oscillations. With the addition of slope compensation the complex poles get damped and this instability issue is cleared. However for an increasing slope compensation this pole pair splits up and for a large enough ramp the system gets the frequency characteristics of voltage mode control. A sufficient slope compensation without the latter issue is to set $Q_p = 1$. It is then possible to rewrite Equation 2.31 to decide the slope compensation factor m_c.

$$m_c = \frac{\frac{1}{\pi} + 0.5}{(1-D)} \tag{2.32}$$

Equation 2.28 together with 2.32, 2.29 and 2.27 makes it possible to derive an expression for the peak-to-peak value of the external ramp, i.e. the slope compensation.

$$V_{PP} = -\frac{(0.18 - D)R_i V_{in} T_s}{L} \tag{2.33}$$

The converter will have the storage capacitor as input voltage source which will decrease in time as it discharges. Hence, the slope compensation has to increase with time to provide with a sufficient ramp to avoid oscillations. It is now possible to formulate a sufficient model for the closed loop system with peak current mode control. The full model consists of 3 terms: A DC gain term, the small-signal converter model and the high frequency transfer function.

$$G_{full}(s) = \frac{V_0(s)}{V_e(s)} = \frac{R_0}{R_i} \frac{1}{1 + \frac{R_0 T_s}{L}(m_c(1-D) - 0.5)} \frac{1 + \frac{s}{\omega_{esr}}}{1 + \frac{s}{\omega_{RC}}} \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}} \tag{2.34}$$

3

Case Setup

3.1 Serial vs Parallel Filter

If using a series connected filter according to Figure 3.1, the complexity of the controller can be less complex in the sense that there would be only one converter supplying the 32 volts buss with power. The other converter would boost the voltage on the storage capacitor. In the parallel setup the robustness is higher, because if the parallel (APF) filter stops working, the DCDC converter could still operate and supply the load. This would only disable the current mitigation performed with the parallel filer. If connected in series the simplicity of the controller is weighted with the robustness of the system. If one of the converters (DCDC and APF) stops working the load would not be supplied at all.

In the thesis "Digitally Controlled Active Power Filter for AESA Radar"[1] the parallel filter is used. This thesis will, even though the complexity is higher, use the same parallel setup as before because it adds an extra level of robustness compared to the serial setup.

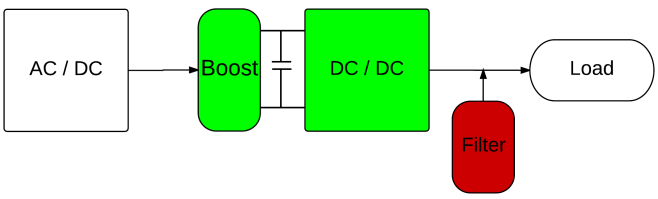


Figure 3.1: Filter setup in serial with Buck converter.

3.2 Circuit Overview

The buck controller, called DCDC in our thesis, was first controlled digitally by J.Ringqvist and J.Viktorsson in [5]. Later, D.Samuel and D.Glenting constructed a digital active power filter in [1], with the same micro-controller that unfortunately was to limited regarding computing power so it was impossible to control the DCDC as well. In this thesis two converters are controlled, the DCDC and the APF, with a new and faster microcontroller. The most important parts that changed from the previous work is a changed control method with added requirements on the measuring system and a new design integrating the DCDC as well as the APF on the same PCB. The setup of the system can be seen in Figure 3.2 where the locations as well as the controlled units are visualized in green. The passive filter marked with red is not implemented in this thesis.

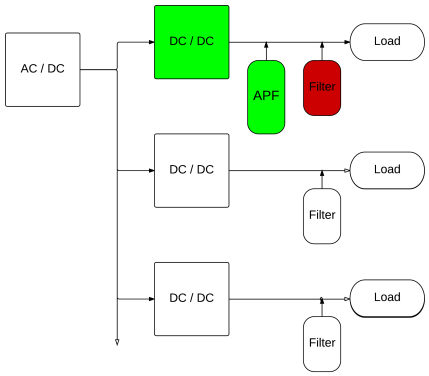


Figure 3.2: System overview of the radar system

The setup of the circuit for the converters are shown in Figure 3.3. To be able to implement current mode control the current measurement circuits are implemented in conjunction with the corresponding inductor as can be seen in figure 3.3 as A1 and A2. To be able to monitor the instant output current A3 is implemented as close to the load as possible; outside of the filter capacitors. The voltage over the storage capacitor V_C is monitored to be able to keep the level below the limit of the driver.

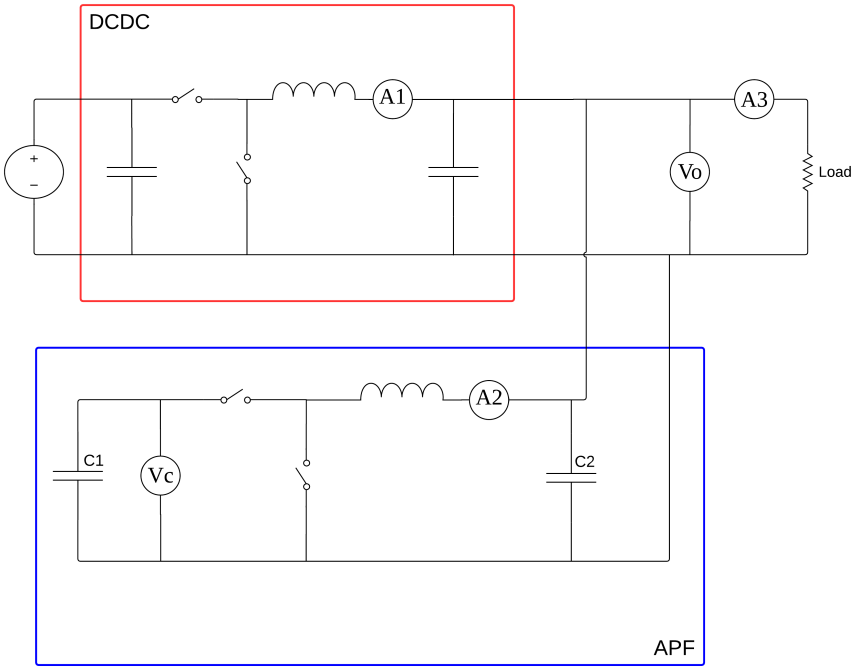


Figure 3.3: Schematic of the DCDC converter and the APF. Also, the locations of all measurement circuits are also shown.

3.3 Components

This section will describe how the key components was chosen.

3.3.1 DCDC Converter

The DCDC converter to be controlled was supplied by SAAB. The converter was studied and modified to be able to include components for very fast current measurements. The converter was implemented on a new PCB that also included the addition of the digitally controlled active filter circuits. The inductor and capacitors for the new implementation was chosen with as similar values as possible as the original converter.

3.3.2 APF

The APF will work in two modes (Buck and Boost mode), the filter will have to be designed with this in mind. When the APF is in Buck mode and thus supplying the load with energy, the converter is chosen to operate in CCM mode. Using that the need for inductance is highest at a duty cycle of 1/2 from Section 2.2.1 and rearranging (2.6) yields

$$L = \frac{T_s V_d}{8 I_{o,max}} = \frac{2\mu\ 32}{8 \cdot 1.5} = 5.33\ \mu H \tag{3.1}$$

To keep the APF converter in CCM for the buck mode, the inductance need to be larger than the value calculated in 3.1.

When the APF is not supplying the load with energy, the DCDC converter is supplying the APF with energy and thereby boosting the storage capacitor in the APF to the desired voltage. Comparing Buck and Boost converter topologies, the need for inductance, to keep the converter in CCM, is highest for the Boost converter. Thus it is the Buck mode that sets the lower limit and the Boost mode sets the upper limit, such that the higher the inductance in the boost mode the larger part of the duty cycle will be spent in CCM. The value of the inductance is also a question of efficiency and peak current tolerance of the components in the system.

3.3.3 Measurement System

As stated in Section 2.3 about the current measurement, it is important that the measurement circuit resistors have low tolerances to measure accurately. The control method to be implemented is peak current mode control, which means that the current in the inductors need to be monitored. The current to be measured is a triangular wave with a ground frequency of 500 kHz. To correctly measure this waveform, the bandwidth of the measurement circuit needs to be a about one order of magnitude higher than the frequency of the triangular wave to be able to correctly register all the higher frequencies in this waveform. Also the delay of the circuit should be kept low. The current measurement circuit chosen for this thesis is the MAX9643U. The circuit was chosen due to its

specifications that according to simulation was confirmed to be satisfactory. The most important data for this circuit is presented in table 3.1.

Table 3.1: Data for the current measurement circuit

MAX9643U Data			
Parameter	Symbol	Value	Unit
Slew Rate	SR	12	$V/\mu s$
Bandwidth	BW	10	MHz
Maximum Input Voltage	FS	300	mV
Output Voltage low	V_{OL}	0.6	mV
Output Voltage High	V_{OH}	3.2	V
Power-Supply Rejection Ratio	PSRR	125	dB

3.4 PCB Design

Compared to the former work done by D.Samuel and D.Glenting [1] this thesis puts other requirements on the circuit. Since PCMC is used instead of average current mode control there is a demand for higher bandwidth in the current measurement system. There was also a need for enabling the inductor currents to be measured by introducing current sense resistors. Also, because two converters are to be controlled, it is beneficial to have all the circuits connected as tight as possible when dealing with gate traces that require low stray inductance. Furthermore there will be less connections to deal with if everything is on the same printed circuit board.

Care was taken to the fact that the paths with the highest dI/dt was avoided when designing the layout for the current sense resistors and surrounding components. The circuit layout of the PCB (Figure A.1) and the complete schematics (Figure A.2 and A.3) with belonging BOM (Figure A.4 and A.5) can be found in Appendix A.

3.5 Control Design

This section will explain the approach to develop a suitable control system for each converter and describe how the these individual control systems has to interact to achieve a suitable behavior of the composite system.

3.5.1 APF buck converter

For this project a type-II compensator has been chosen for the CCM buck converters[12][10]. The type-II compensator is a two pole one zero compensator.

$$H_c(s) = \frac{1 + \frac{s}{\omega_z}}{(1 + \frac{s}{\omega_p 1})(1 + \frac{s}{\omega_p 2})} \tag{3.2}$$

The zero and poles are set to give the composite system a suitable behavior. The first and second pole are placed at the origin and at the ESR zero of the plant respectively. The zero is placed at $\frac{1}{5}^{th}$ of the desired crossover frequency ω_c which should not be larger than $\frac{1}{10}^{th}$ of the switching frequency $f_s w$ which is set to 500 kHz for all converters in this project.

$$\omega_p 2 = \frac{1}{R_C C} \tag{3.3}$$

$$\omega_z = \frac{2\pi f_s w}{50} \tag{3.4}$$

Table 3.2: Component values

Component	Value
L	33 μH
C	35 μF
R_C	1 $m\Omega$
R_0	21.3 Ω
R_i	50 $m\Omega$

For this project the controllers will be digital therefore it is needed to discretize them. This is done in matlab with the command $c2d(G(s), T_s, 'tustin')$. The type-II controller will be discretize to a discete two pole two zero compensator.

$$y[n] = b_0 * x[n] + b_1 * x[n-1] + b_2 * x[n-2] - a_1 * y[n-1] - a_2 * x[n-2] \tag{3.5}$$

Where b_n and a_n are the discrete transfer function parameters. This can then be implemented in the C++ code in the DSP. In Table 3.3 the values for the components in the APF circuit are displayed. These values together with the value for the steady state duty

cycle in (3.3) are put into the full model in (2.34). A bode plot of the composite system, the full model and the continues-time and discrete-time compensator can be sen in 3.4. The discrete compensator has the same gain and phase as the continuous-time compen-

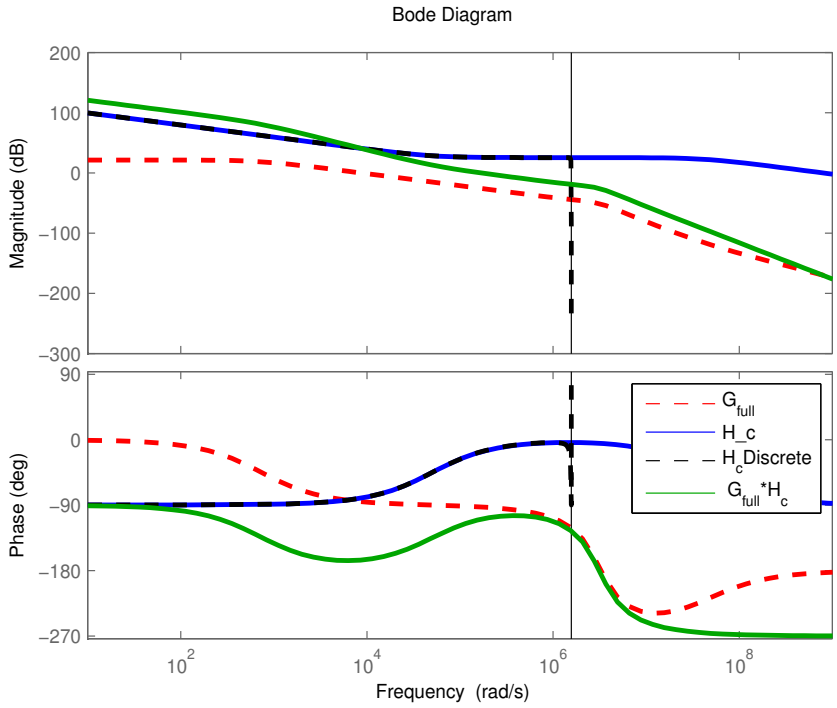


Figure 3.4: DC/DC converter bode plot

sator for the important frequencies. The phase margin, delay margin, gain margin and crossover frequency for the composite open-loop system.

$$P_m = 70.1^o \tag{3.6}$$

$$d_m = 7.48\mu s \tag{3.7}$$

$$G_m = 26\text{dB} \tag{3.8}$$

$$f_c = 26\text{kHz} \tag{3.9}$$

These margins are possibly needed to be able to manage the model uncertainties and the delays in the circuit.

3.5.2 DC/DC converter

A type-III compensator has been chosen for the DC/DC buck converter which will operate in DCM. The type-III compensator is a three pole two zero compensator and yields a larger phase margin than the type-II compensator. This is needed due to the

double pole in the control-to-output function which makes the phase decrease rapidly towards -180^o.

$$H_c(s) = \frac{(1+\frac{s}{\omega_z 1})(1+\frac{s}{\omega_z 2})}{(1+\frac{s}{\omega_p 1})(1+\frac{s}{\omega_p 2})(1+\frac{s}{\omega_p 3})} \tag{3.10}$$

$$\omega_p 2 = \frac{1}{R_C C} \tag{3.11}$$

$$\omega_z = \frac{2\pi f_c}{50} \tag{3.12}$$

Table 3.3: Component values

Component	Value
L	16.4 μH
C	88 μF
R_C	0.2 $m\Omega$
R_0	200 Ω
R_i	50 $m\Omega$

The compensator in the DC/DC is discretized with the same matlab command as used for the APF buck converter. This is however a type-III compensator which is equivalent to a three pole three compensator in discrete-time.

$$y[n] = b_0 * x[n] + b_1 * x[n-1] + b_1 2 * x[n-2] + b_3 * x[n-2] - a_1 * y[n-1] - a_2 * x[n-2] - a_3 * x[n-3] \tag{3.13}$$

The values in Table 3.2 together with the steady state duty cycle for the APF are put into the full buck converter model. As for the previous section, a bode plot with the important frequency responses can be sen in 3.5: The phase margin, delay margin, gain margin and crossover frequency follows:

$$P_m = 70.3^o \tag{3.14}$$

$$d_m = 7.43\mu s \tag{3.15}$$

$$G_m = 25.8\text{dB} \tag{3.16}$$

$$f_c = 26\text{kHz} \tag{3.17}$$

These margins are needed to be able to manage the model uncertainties and the delays in the circuit.

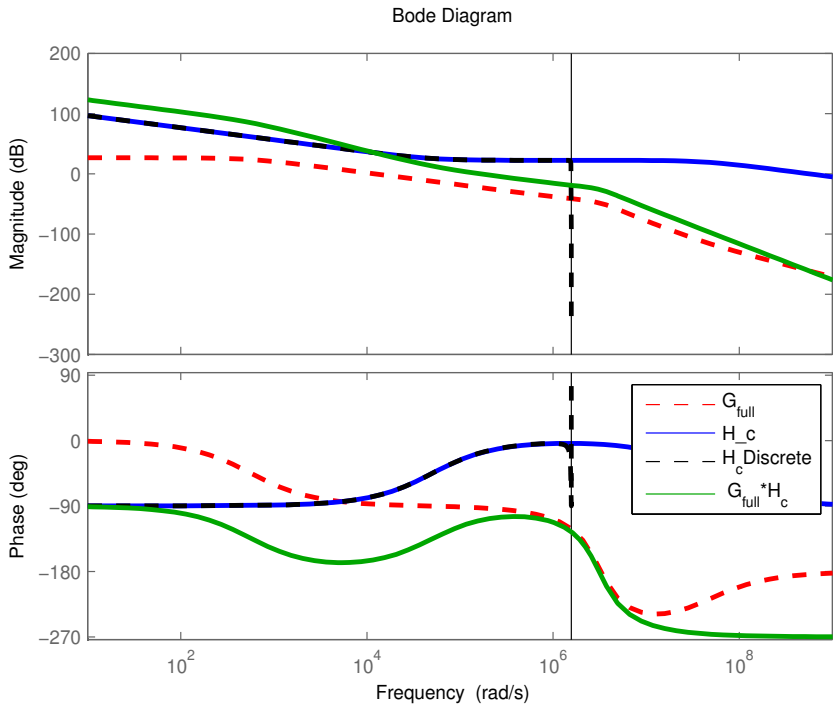


Figure 3.5: APF buck converter bode plot

3.5.3 APF boost converter

A very important part of this project is to keep the input current in the system as constant as possible. Hence, the input current in the boost converter needs to be as constant as possible which will charge the capacitor linearly. The storage capacitor will lose most of the energy during a load pulse and needs to be sufficiently charged until the next load pulse comes. With conventional output voltage feedback control a large error in output voltage would occur after each pulse which would yield a strong response from the compensator to minimize the error as quickly as possible. Initially this would produce a large input current into the boost converter and when the error is zero or positive the compensator would stop charging the capacitor which will make the input current zero. Both these events are very unsatisfactory and will not produce a constant current level in the input current of the system. Therefore some other type of control method has to be used. The control will be based on equations to calculate the duty cycle for a DCM boost converter.

$$i(t) = C\frac{dV(t)}{dt} \tag{3.18}$$

$$i_{Lmax} = \frac{V_i D T_s}{L} \tag{3.19}$$

$$i_0 = \frac{V_i^2 * D^2 T_s}{2L(V_0 - V_i)} \tag{3.20}$$

$$i_{Lmax} = \frac{V_{in} T_s}{L} \sqrt{\frac{2 i_0 L (V_0 - V_{in})}{V_{in}^2 T_s}} \tag{3.21}$$

From (3.19) and (3.20) it is possible to derive an expression for the peak current level for the inductor current which will yield a specific i_0. This expression is is displayed in (3.21). The only variable in this expression is the output voltage of the storage capacitor V_c. V_c will be measured every switch cycle and the value for i_{Lmax} will be calculated based on V_c. i_{Lmax} will be the input to the comparator together with the inductor current as in the inductor current feedback loop of PCMC. This comparison will produce a duty cycle which will yield a constant input current.

3.5.4 Delays

There are several delays in the circuit mainly from the measurement and driver circuits. The outer voltage loop has a delay of 2 μs, from the measurement, which is the period time for the switching frequency of the circuit since the output voltage is measured once each period. The inductor current measurement system has a delay of roughly a few ns and the drivers has a delay of 60 ns from data sheet and observation. There is most likely a delay in the MCU of a couple of ns. The different converters together with controllers have different phase margins which for the crossover frequency can be translated to a delay margin expressed in time. The sum of all delays needs to be less than the delay margin in order to have a stable system. Due to possible model uncertainties the delay margin should preferable have a margin after the known delays to compensate for possible uncertainties.

3.5.5 Collaboration between individual control systems

When multiple controllers are controlling the same output problems might occur when e.g. the faster controller outputs more energy than desired. Especially in this project where the input voltage of the APF buck converter will decrease over time. Two linear compensators where one has a decreasing input voltage then the other cannot achieve the desired constant current level which is an objective of this project. There are two solutions to this. Either the compensator with the decreasing input voltage needs *gain scheduling* to compensate for the decreasing input voltage. The other solution is to keep the output current of one compensator constant and let the other compensator achieve the steady state of the output.
For this project given that the control system is implemented on an MCU with limited resources as far as clock cycles go and also a limited time-frame to develop and implement additional needed functions. The most suitable solution is to set the output to one compensator constant during a specified time-frame. Ultimately, when there is no load pulse e.g. when the APF is in boost mode, the boost converter control system is limited

a constant output and during a load pulse the DC/DC converter is limited to a constant output.

3.5.6 Simulation set-up

Simulation was used to verify the functionality of the entire control system. Both compensators as well as the control system for the APF in boost mode was implemented in a simulink model. The complete circuit, i.e. the APF and the DC/DC converter was implemented with Simscape components which is a fast and approach as well as easy to modify. Additional blocks were implemented in order to model behavior and limitations of the circuit and the MCU, e.g. the ADC and DAC modules. The load pulse pattern was modeled with a resistance of 21.3 Ω together with a ideal switch. The resistor value was chosen according to the pulse pattern used in the real world experiments.

In the real application the load pulse will be detected by the ADC modules which measures the output load current but for the simulations the control systems will be controlled by the same switch signal as the load resistance. This will make the simulation ignore dynamic which occurs in the switch moments just before and after the load pulse is present.

In order to make comparisons between the simulations and the real world, the measured signals from the real world will be monitored in the simulations and presented in the results chapter. 3.6 displays an overview of the simulink setup.

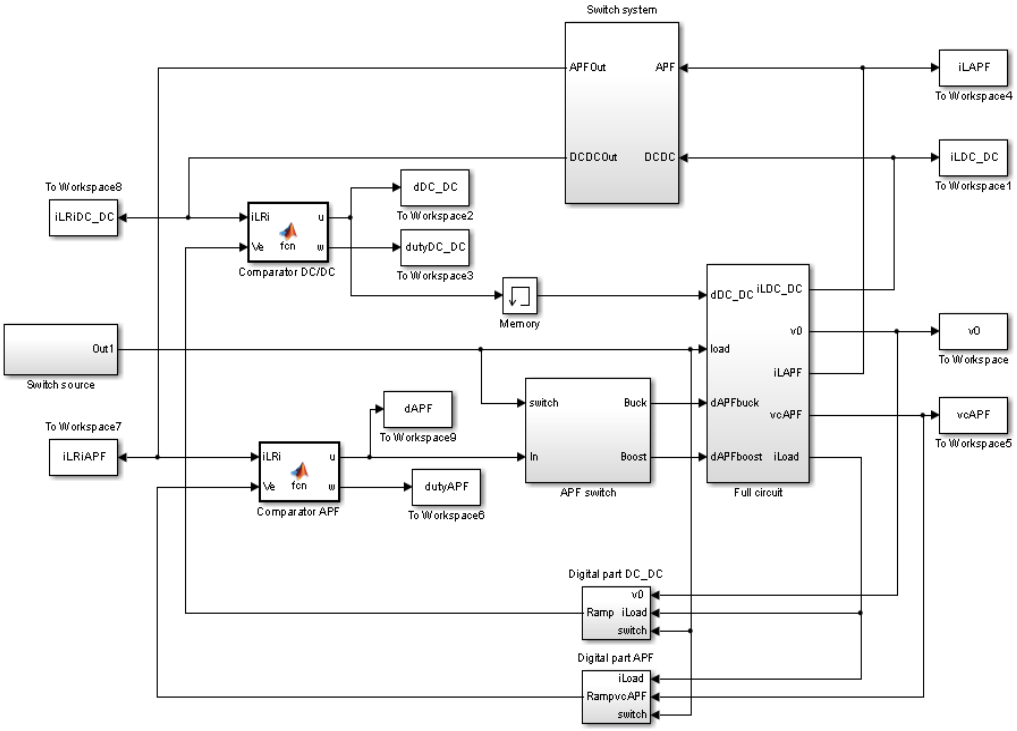


Figure 3.6: Simulink model overview the simulation setup with the blocks described above.

3.6 MCU

In this section the selection of MCU, the implementation and functionality of the program will be described.

3.6.1 Selection

Two MCUs were investigated to choose a suitable MCU for this project. The first one is manufactured by Texas instruments and is called TMS320F28377D and the other one also from Texas instruments is called UCD3138. These two MCUs were investigated since they were propsed as options in the thesis problem description. Other available options was not investigated since both these MCUs were considered sufficient and similar MCUs were used in earlier thesis on this subject.

The selection was based on several criteria such as flexibility, performance and development time. The TMS320F28377D has more processing power and has on paper better performance than the UCD3138. The UCD3138 has a lower clock frequency and fewer channels etc. on some peripherals. However, it has hardware modules such as a two pole/two zero compensator which reduces the software overhead needed for the system. Hence it is hard to determine which of the two platforms have the best performance for

this project's application. The UCD3138 has surely a shorter development time due to these modules which reduces the amount of programming needed. But with the specific functionality of these modules the flexibility is reduced which is also an important criteria for this selection.

The TMS320F28377D was ultimately chosen due to its flexibility and performance. Not enough time was spent on this process to surely determine the best option in practice. Neither of us had much experience working with MCUs nor enough insight in how the project would develop itself in the end as this selection was done at an early stage in the project. The TMS320F28377D was considered a safer choice and therefore chosen.

3.6.2 Program function description

Figure 3.7 displays an overview of the program's functionality. The blocks labeled *core 1* and *core 2* describes the software functionality. The functionality of the peripherals as well as how they communicate with the software and other peripherals are also visualized in the figure.

There are two cores in the MCU which can run two different programs simultaneously and for this project CPU1 has the control strategy for the DC/DC converter implemented and CPU2 has the control strategy for the APF circuit implemented. The MCU programs are written to control the circuit in real-time with small delays and this is done by utilizing discrete events. Modules communicate to each other and sends commands by creating events and what events are created depends on the sampled signals but also on the measured inductor current.

The objective of the active software functionality is to provide the modules with input in order for the modules to create the appropriate events to control the circuit properly. The input to the modules are made through registers which can specify module behavior based on the value in a certain register. E.g. by setting a specific value in a register that controls the ePWM output at the beginning of each period the module can either pull it high or low depending on which value is placed in the register. I.e. the module will perform whatever it is specified to do until the value in the register is changed, this disables the need for excessive software overhead for module behavior. The ePWM time-based counter $TBCTR$ has a period of 400 clock cycles. The frequency of the CPU $f_{CPU} = 200$ MHz and the switching frequency of the circuit $f_{sw} = 500$ kHz. This ePWM counter is the counter that synchronizes all other modules which means that 400 clock cycles is the total amount of resources that can be used for software overhead in one switching period.

$$N = \frac{f_{CPU}}{f_{sw}} = \frac{200}{0.5} = 400. \tag{3.22}$$

There are two ePWM counters, one for each core system. These counters synchronize all modules with start-of-conversion signals as well as synchronization signals. In order

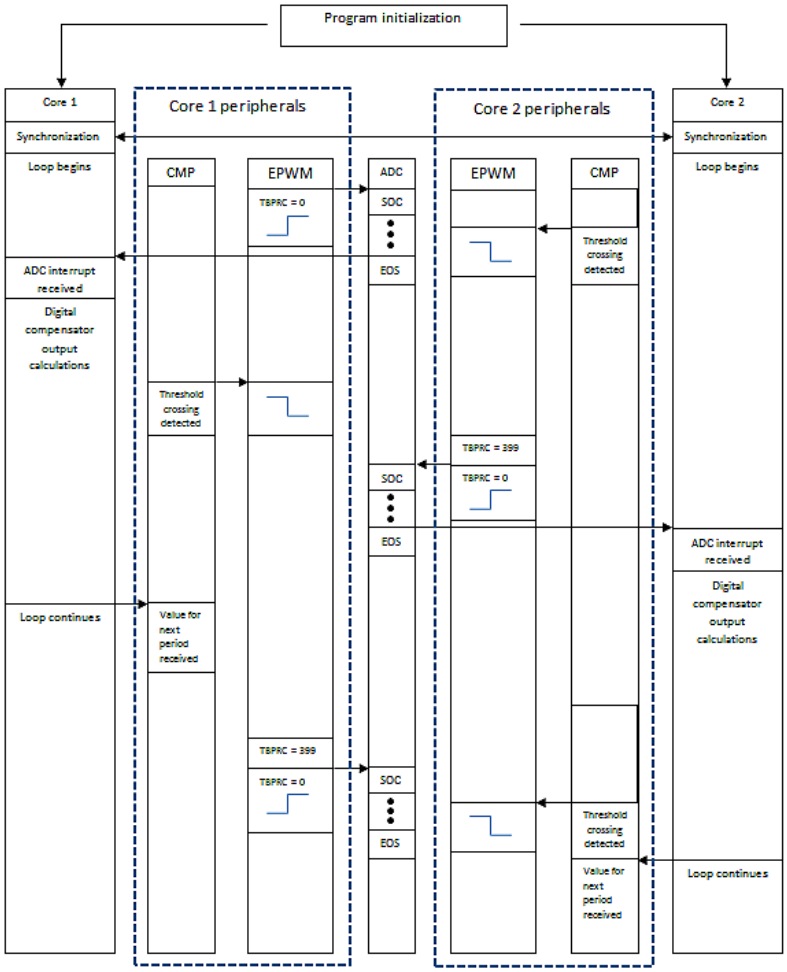


Figure 3.7: MCU program overview

to get the switching of the DC/DC converter and the APF 180^o phase shifted to each other the counter for core system 2 starts at half a period.

3.6.3 ADC

The Analog to digital module located on the MCU circuit board will sample the continuous analog voltages to discrete values placed in registers. The ADC modules have several limitations which has to be taken into consideration and addressed. The MCU of this project comes with four ADC modules which means that four signals can be sampled simultaneously which means that the ADC modules are a limited resource and have to be utilized efficiently.

Another issue is that the ADC module needs time between the start of conversion and

the end of conversion this window is called the acquisition window and has to be about 20 clock cycles which for the 200 MHz CPU is about 100 ns. The size of the acquisition window depends on if 12-bits or 16-bits conversion is performed and for this project 12-bits conversion has been chosen due to simplicity and the shorter acquisition window. For this project an arbitrarily large window on about 40 clock cycles has been chosen primarily to not get issues with resolution. The drawback with a large acquisition window is that the software in the MCU cannot start until the ADC modules has ended the conversion since the sampled signals are used in the compensator and for other functions as well. Due to the register size being 12-bits there is only 4096 possible values these sampled signals can take which also affect the accuracy of the conversion from analog signal to digital value. Since the maximum voltage input used to the ADCs being 3.3 V and the minimum being zero volts the smallest change in voltage that the ADC modules are able to distinguish is:

$$\frac{V_{High} - V_{low}}{Registersize} = \frac{3.3}{4096} = 0.8mV. \tag{3.23}$$

The ADC modules has several post processing blocks which can perform comparisons between the sampled value and pre-defined values to produce suitable interrupts which depends on the outcome of the comparison. E.g. if a large load current is detected then a certain function should be called upon containing the control strategy which is used when the load is active and if a very low current is detected the another function should address that state.

Apart from other peripherals the ADC modules are shared between CPU1 and CPU2, hence both CPUs can access up to four recently sampled signals to produce a faster and more accurate response.

3.6.4 ePWM

The Enhanced pulse width modulations modules are used to control the circuit by switching the converters from on-state to off-state and vice versa. The output of an ePWM module is a continuous signal and the output is controlled by discrete events inside the MCU.

At the start of every period the output of the ePWM modules is pulled high. The output signal is a rectangular waveform which will be pulled low when any of two criteria are met. The most common is when the sensed inductor current equals the threshold voltage V_e or when the output has been high for certain amount of time which is pre-defined as a limit to not damage the circuit i.e. some circuit parts cannot support a 100% duty cycle. When the sensed inductor current equals the threshold the comparator creates an event which ultimately pulls the ePWM output low. The same procedure is used to limit the duty cycle of the output to a maximum, by using a counter which creates a similar event which the counter is equal to a certain maximum allowed counter value. The output can also be forced low when a safety limit crossing has been detected i.e.

when the output voltage is too high due to a faulty control system but then it is the software that forces the output low and not a discrete event.

By using events and define the conditions for when a certain event is generated saves software overhead which ultimately saves clock cycles that can be used for other custom functionality.

3.6.5 Comparator

The comparators described in this section are analog comparators on the MCU circuit board used to implement the peak current mode control. These comparators are due to their analog presence very fast which is needed to not get further delays in the control loop. At the beginning of each period the reference input to the comparator has already been calculated by the software last period and is fed to the comparator as an analog signal produced by the internal digital to analog module. This internal DAC will also reduce the amplitude of this signal each clock cycle to implement the slope compensation which is a fundamental part of the peak current mode control method. This is done by subtraction of the reference register value by another register that specifies how much the amplitude will be decreased each clock cycle which will produce a falling ramp on the reference input but the ramp is not decreasing continuously.

The comparators also has a built in digital filter that can be designed to reduce premature switches between on-state and off-state. Disturbances in the current feedback loop might make the sensed current equal to the reference values for a very short period of time and by defining that the input of a digital filter needs to get a confirmation that the sensed current is larger or equal to the reference for e.g. four consecutive clock cycles, the issue is addressed. The event that the comparator ultimately creates to pull the output of the ePWM low when the condition the digital filter is defined upon is satisfied, the comparator can not control the output of the ePWM module for the remaining of the period. These events are called cycle by cycle trip events and can only be created once every period, in order to keep a constant switching frequency.

3.6.6 Software

The software has functions such as initialization of modules and declaration of variables and constants. But the most important begin to produce the output of the digital compensator. The software also has functionality to ensure stable and safe testing on the real circuit due to uncontrollable circumstances especially the load generator. Safety protocols are also implemented if high voltages or currents are measured to avoid damage on the circuit. The software also features a soft-start protocol which is launched before the circuit is powered up and running to ensure that the APF storage capacitor gets charged up without damaging the circuit.

4

Analysis

This chapter will present different results that has been obtained during the project i.e. control simulations, and experimental results with the finished prototype.

4.1 Simulations

4.1.1 Simulink

The simulations in matlab was done to ensure the modeling and control design phases provided a sufficient foundation to implement this control system in practice. Figure 4.1 displays the inductor currents of the DC/DC converter and the APF. The inductor current peak-to-peak of the DC/DC converter remains constant during a load pulse cycle which will maintain a constant level on the input current of the 56V bus. This is a good result since one of the main objectives is to maintain this level as constant as possible. Regarding the size of the input current, it should be as small as possible but still maintain 32V on the output and supply the APF with enough power. This simulink model does not account for all losses in the real world circuit, therefore the peak-to-peak of the DC/DC converter will not be analyzed in that respect.

The inductor current of the APF indicates the location of the load pulse in time and it is constant during the load pulse which is the main result from this simulation. Since this level is constant there is no need for the DC/DC converter to supply any power other than the constant level which can be seen in the figure.

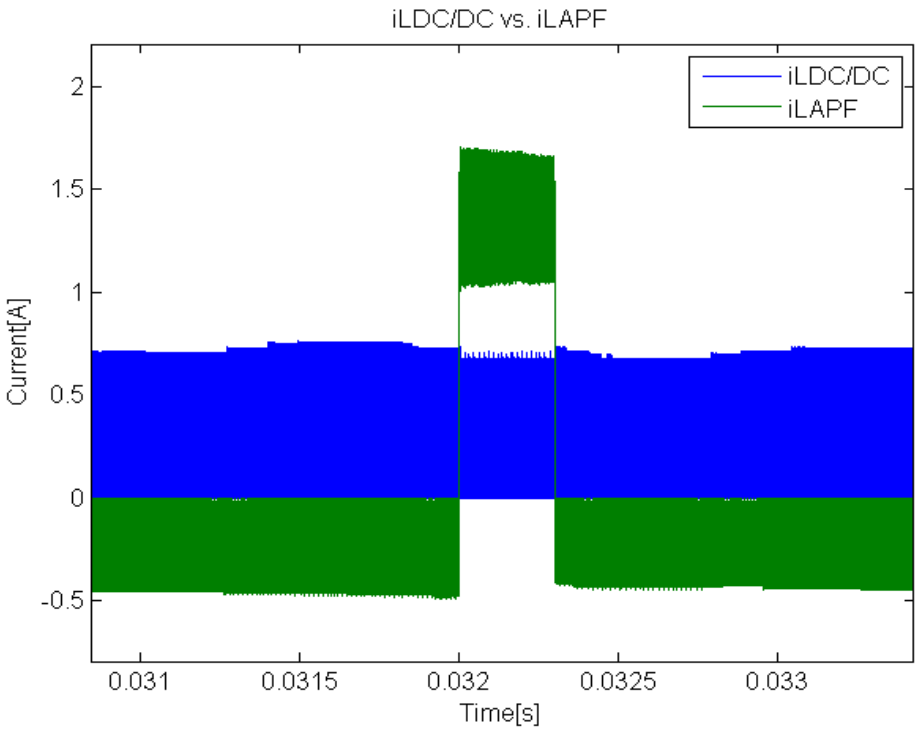


Figure 4.1: APF and DC/DC converter inductor currents

Figure 4.2 indicates that the circuit supplies the load with sufficient power during the simulation. Variations in output voltage is an indication that the APF is not supplying a sufficient amount of power. Since these variations are small, the APF is supplying a sufficient amount of power. However, the load voltage is not very constant during any time which indicates that the control system could need tuning.

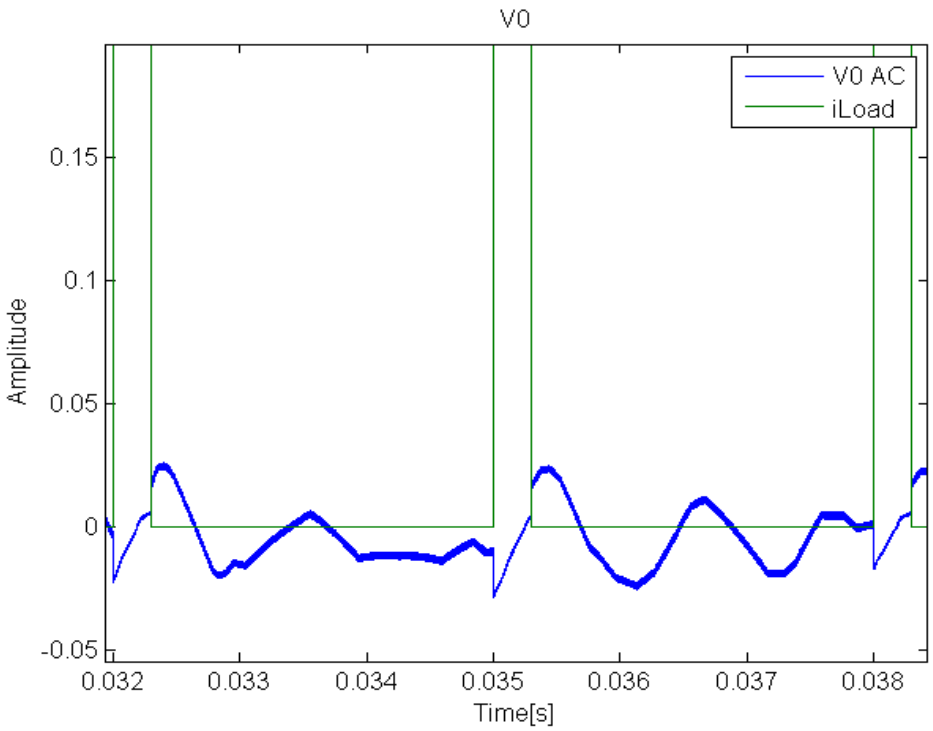


Figure 4.2: Output voltage

Figure 4.3 displays then voltage change in time over the storage capacitor in the simulation environment. The peak-to-peak change in voltage in every load pulse period is approximately 8.5 V. A satisfying observation to be made here is that there is no gain or loss of voltage between load pulse cycles, this would otherwise require tuning of the boost control system.

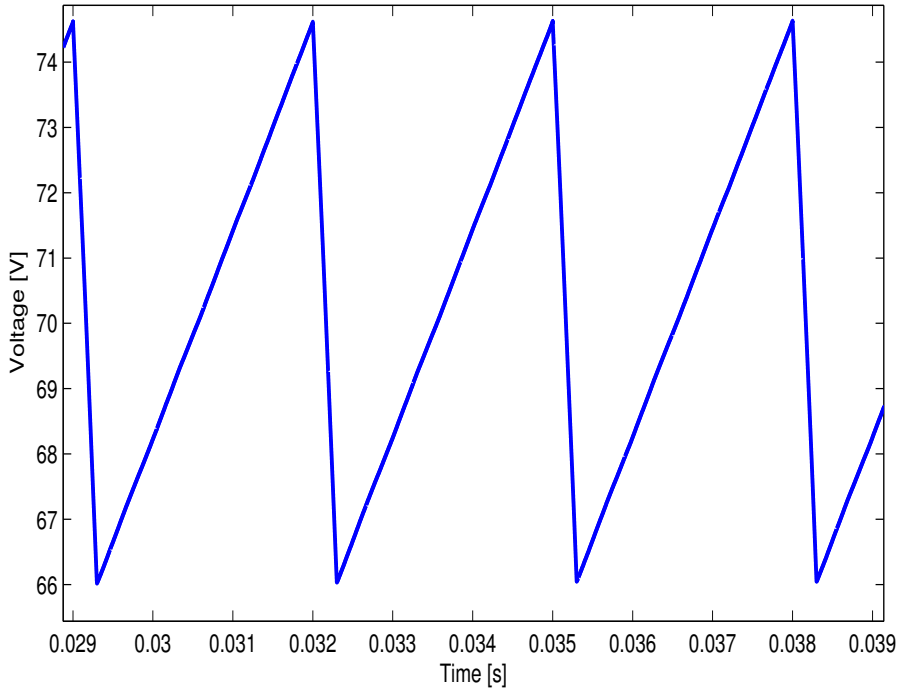


Figure 4.3: Voltage over the storage capacitor

4.2 Experiment Results

In this section results from the measurements made on the finished prototype will be presented. Several measurements were made to analyze specific parts of the system in order to identify unsatisfactory behavior and analyze the cause of the behavior. The load pulse information that were used throughout the measurements can be seen in Table 4.1.

Table 4.1: Pulse pattern

Parameter	Value
T_s	3 ms
Duty cycle	10 %
i_{on}	1.5 A
i_{off}	0 A
Slew rate	63.5 mA/μs

In Figure 4.5 the APF performance is illustrated in terms of the variations in input

current in the system i.e. the current level on the 56V bus. Small variations in the input current was one of the main objectives for this project. The DC-level on the input current is about 0.16 A which is the current needed to charge the storage capacitor sufficiently for the pulse pattern used to produce these results. The variation of the current level is about 40 mA which is a good results given that there is no additional filter apart from the small output filters of the converters. Without the APF activated the current variations on the input to the DCDC are about 1 A which can be seen in figure 4.4.

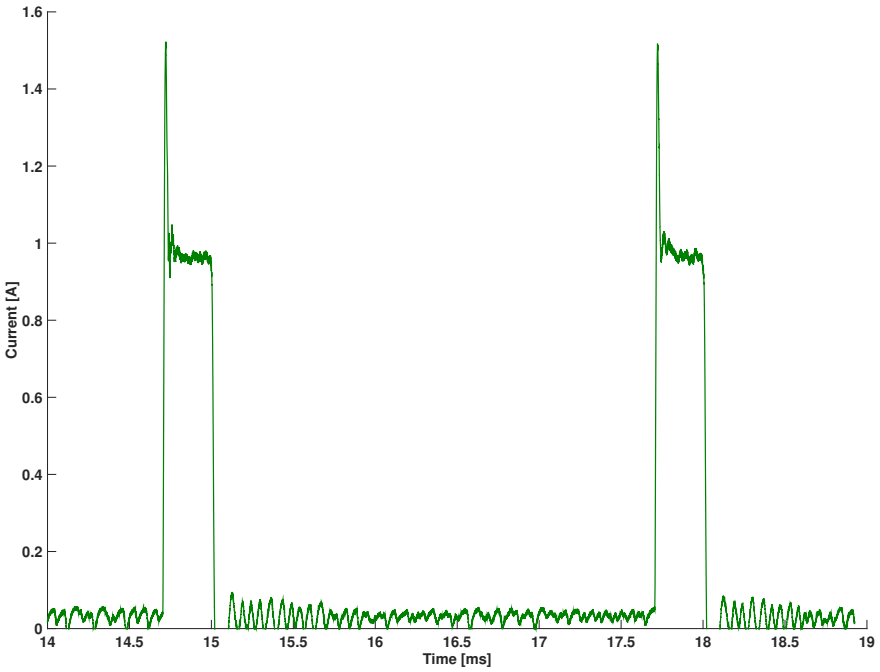


Figure 4.4: Input current to the DCDC without the APF activated

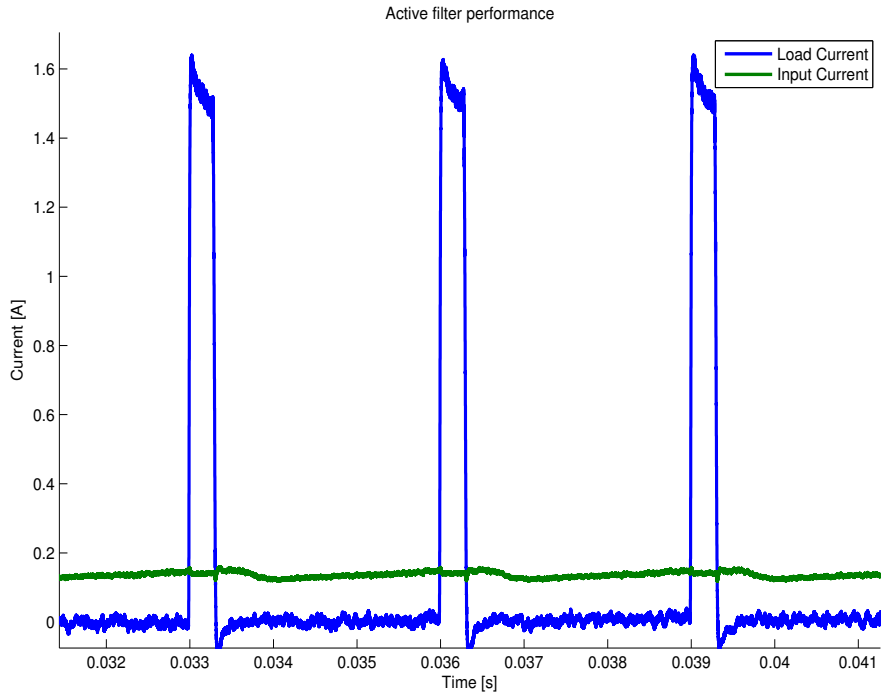


Figure 4.5: Input current and load current

In Figure 4.6 the inductor current of the two converters can be seen during three load pulses. The inductor current in the DC/DC has a fairly constant peak value over time which indicates that the input current from the 56 V bus will be fairly constant as well which was shown in Figure 4.5. The inductor current in the APF has two different appearances which is due to the switch between buck and boost mode when the load pulse is active and not active respectively. The peak-to-peak value in the boost mode of the APF increases over time which is due to the increasing output voltage over the storage capacitor. This characteristic can be seen in the buck mode as well but then the peak-to-peak value of the inductor current decreases over time since the storage capacitor is losing energy hence voltage with the time during a load pulse. The characteristic of the APF inductor current during a load pulse is not very satisfactory which will be made clear in the output voltage figure later in this chapter. Optimally the level of the high peak of the inductor current should be relatively constant during the load pulse to deliver the same amount of energy each switching cycle unless the output voltage is not at steady state.

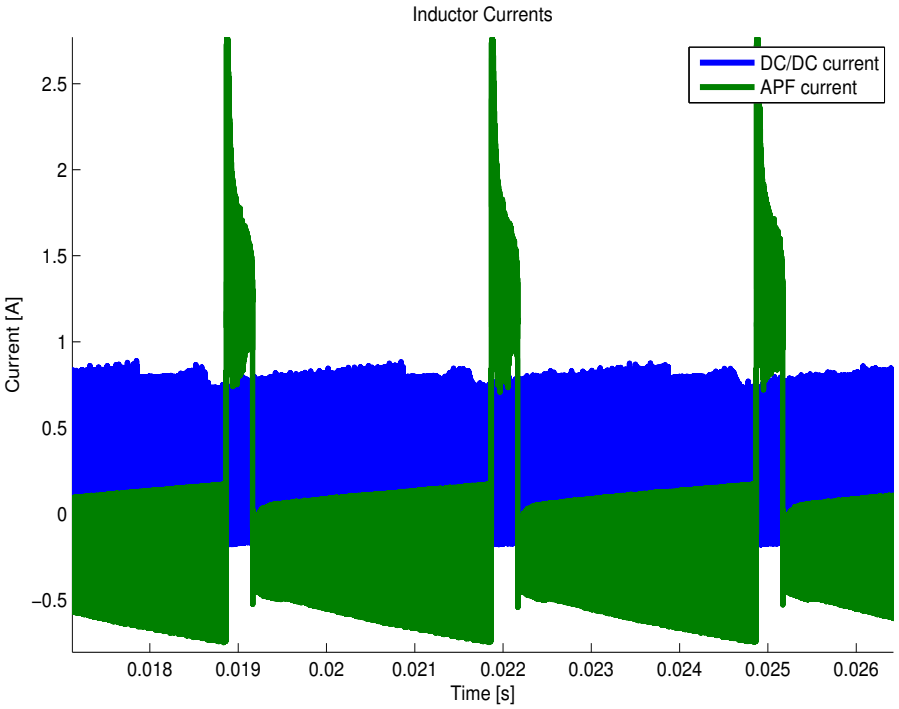


Figure 4.6: APF and DC/DC converter inductor currents

The output voltage is illustrated in Figure 4.7 as an AC signal which means that only variations from the steady-state 32 V are displayed. The voltage is fairly steady when the load pulse is inactive and the APF is in boost mode. However, when the load pulse comes active there is a large voltage drop which is compensated during the load pulse but there is a slight overshoot and at the end of the pulse, the voltage drops about 100 mV below steady state. The voltage variations in the beginning and end of the load pulse is due to the slew rate of the electronic load pulse that begins low and since the control systems switch between boost and buck mode at a certain load, the DC/DC converter has to supply the additional load and the control system in the DC/DC can not compensate fast enough. There is also a variation from the steady state right after the load pulse has gone inactive which is due to the control method for the APF in boost mode not being completely satisfactory.

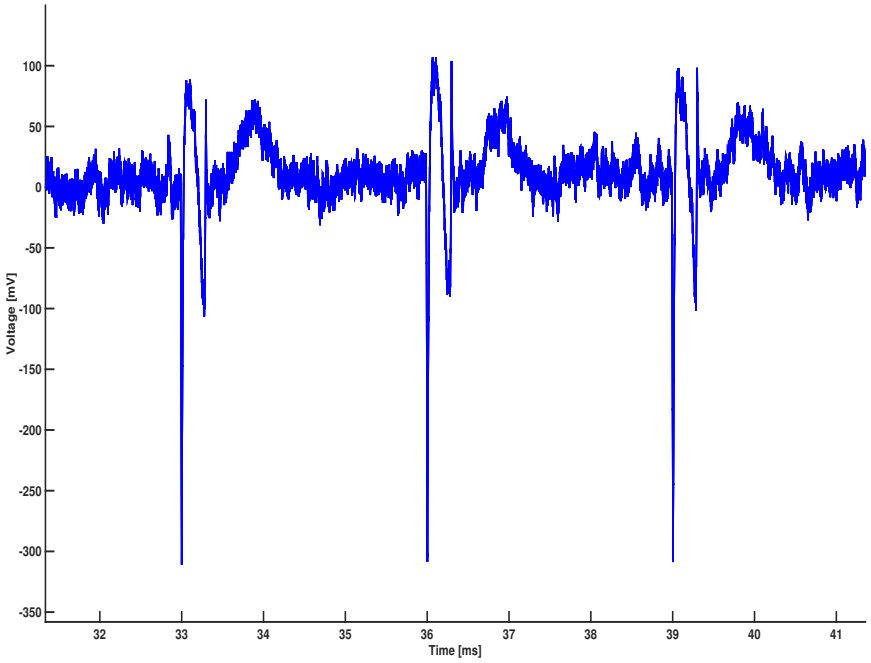


Figure 4.7: Voltage ripple on the output voltage

The voltage over the storage capacitor is display in Figure 4.8 and has two distinct slopes, one during the charge phase which is when the APF is in boost mode and the other one is when the capacitor is being discharged when the APF is in buck mode. The positive slope should preferably be as constant as possible which means that the input current into the APF is constant. It can be seen that the slope is slightly larger after the load pulse has gone inactive and at the point where it changes to be constant for the remaining time of the boost mode is the same point as the output voltage departs from the steady state. It can also be seen that almost all energy that is charged during boost mode is lost during buck mode, since the output voltage is 32 V the capacitor cannot deliver energy when the voltage over the capacitor is less or equal to 32 V. This causes problems to the control system for the buck converter since the down-slope for the inductor current is very small for very small deviations between input and output voltage.

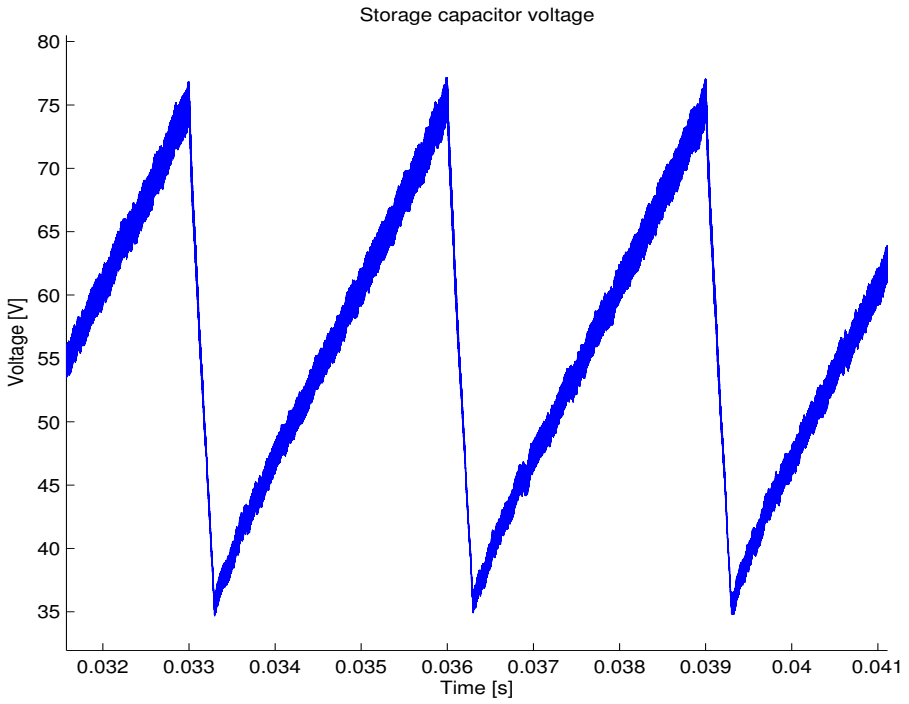


Figure 4.8: Voltage over the storage capacitor

4.3 Efficiency

The pulsed output current has an RMS value of $I_o = 0.48A$ according to measurements. Because the output voltage only is effective when there is output current, the output voltage can be seen as pulsed which yields the value $V_o * \sqrt{D} = 10.67V$. The input current is varying with less than 50 mA, but the RMS input current is calculated to be $I_o = 0.1374A$ at 56 volt input. These values results in an efficiency of $\eta = 66\%$.

Comparing with the results in the work by D.Samuel & D.Glenting[1], the efficiency for the complete system containing both the DCDC converter and the APF needs to be calculated because there are only efficiency values available for the APF alone. According to [1] the RMS output current is 0.4716 A and the input RMS current is 0.1681 A when both the APF and the large output filter (1100 μF) is activated. Calculating the input and output power with these numbers, results in an efficiency, for the whole system of about $\eta = 50\%$.

The infrared (IR) image in Figure 4.9 is displaying the temperature of the DCDC converter under normal operation. From the image the temperature is highest in the inductors with an temperature of about 50 °C and a temperature of about 42 °C in the

transistors.

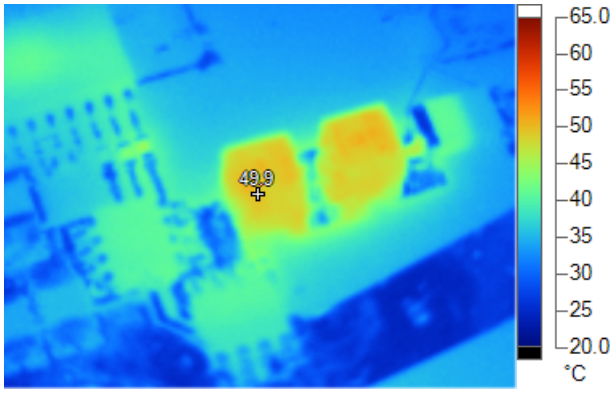


Figure 4.9: Image captured with IR camera. Showing the temperature in the inductors and transistors in the DCDC converter during normal operation.

The transistors in the APF is shown in the IR image in Figure 4.10. The temperature is about 8 °C higher than in the DCDC converter since the current in the APF is much higher. The absolute temperature of the high side transistor is about 48 °C.

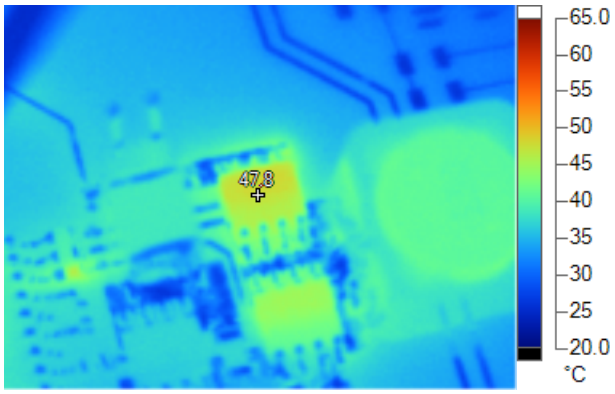


Figure 4.10: Image captured with IR camera. Showing the temperature in the inductors and transistors in the APF converter during normal operation.

When the DCDC is activated but the APF is not, all current has to be handled by the DCDC inductors. These inductors have a relatively small footprint and are of high R_{DC} type and thus the temperature increased to almost 59 °C which can be seen in Figure 4.11.

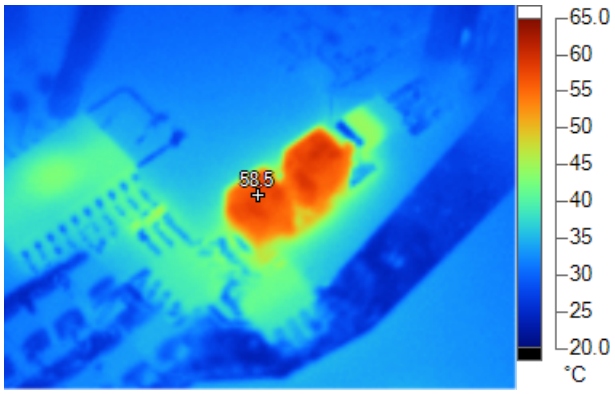


Figure 4.11: Image captured with IR camera. Showing the temperature in the inductors and transistors in the DCDC converter with the APF deactivated.

Possible solutions for increasing the efficiency of the system could include the implementation of zero current detection for the inductor current to prevent the converters to enter FCCM. When the converter is operating in FCCM the current is kept flowing in the reverse direction, which is decreasing the energy efficiency. The same microcontroller could be used but the components in the converter circuits could be changed to variants with for example lower R_{dsON} and C_{gs} for the transistors. Also, as stated in Section 2.2.4 about the losses, the body diode is of low performance type and is favourably substituted with an added Schottky diode in parallel with the transistor. One obvious improvement would be to change the inductors with variants with lower serial resistance. Furthermore, to improve efficiency the DCDC converter could utilize lower or adapting switching frequency. Meaning that the DCDC converter would lower the switching frequency when only delivering the same amount of current for the charging of the APF storage capacitor, and increasing the switching frequency if the APF is not operational to increase the step response. The APF could utilize adapting switching frequency. Thus lowering the frequency when the APF is storing energy in boost mode and increasing when the APF is releasing energy in buck mode. This would improve the energy efficiency in boost mode and also increasing the step response for the releasing mode. Also, the current spikes in the inductors should be reduced if possible to improve the system. Some smaller changes to improve the switching efficiency could be to lower the gate resistances to speed up the on and off switching of the current. If a new PCB where to be developed focus could be on shortening and widening of the traces, especially from the APF to the output. This would improve the response time of the APF because the inductance would be lower and thus the current can be delivered more quickly.

5

Conclusions

This project has been a proof of concept, that it is possible to reduce the input current variations on the 56 V bus to an acceptable level while delivering sufficient power to the load. This has been achieved with an active power filter without additional passive filters. From Figure 4.5 in the results chapter it is shown that the current variations are less than 50 mA with the APF and about 1 A without the APF which is a reduction of 95% on the input current variations. The RMS for the output current is 0.48 A while the RMS input current is 0.1374 A. The efficiency for the previous work was according to Section 4.3 calculated to 50% while the result for this thesis are 66%. Which results in 17% better performance when comparing the complete systems. As discussed in Section 4.3, there are a number of parts that can be improved to increase the efficiency as well as the performance of the system.

The control systems for the different converters at the different states of the load pulse are all having good performance but there are clear indications that the control parameters are not optimally tuned as well as the control strategy is not optimal for this application. This means that the control method i.e. peak current mode control can achieve slightly better performance. However, the largest cause of sub-optimal performance is that the detection of load pulse is not very good and the fact that the electronic load used for this project only had a slew rate of 63.5 m$A/\mu s$. Additionally, the control method for charging the storage capacitor is not very robust and for this project it is only made to handle per-defined load patterns. It is not able to adapt to pulse patterns with different characteristics. An adaptive control strategy has to be made in order to achieve acceptable performance for a larger variety of load pulse patterns.

For the simulations that were made to verify the control strategy were sufficient as a proof of concept but the model used was not taking into consideration sufficient dynamic which can be seen in Figure 4.1 compared to Figure 4.6. The influence of sub-harmonic

oscillations from the current loop was not taken into account as well as all losses in the circuit. This made the simulation environment insufficient for control parameter tuning as well as to predict issues that appeared in the real environment. However, the simulation environment proved to be very useful for the early design and verification of the control methods and strategies. A more accurate simulation environment would certainly have provided a better final result for this project.

The model approach was to make simple models to maintain understanding and to verify them in the simulation environment. This approach has been successful given the limited time frame for the project and the sub-optimality of the performance was more due to the poor simulation environment and the insufficient amount of time than the modeling approach.

5.1 Future Work

After the load pulse is detected the controller takes no action until the next switching cycle is started. To improve the performance of the digitally controlled filter, faster detection of the load pulse and and faster action could be implemented by adding analog comparators for pulse detection. Also pre-charge of the APF filter inductance could be implemented by adding two more transistors such that the inductor is charged before the load pulse is detected and the energy in the inductor would be released at the moment the load pulse is detected. Using this topology would mean that the pulse response of the filter would be improved but the complexity of the controller software would be increased. If the objective is to keep the current fluctuation at the 56 V bus to a minimum, this topology would have to be combined with another solution. To improve the performance higher switching frequency could be implemented in the APF when in buck mode and thus supplying the load. To compensate for this, lower switching frequency could be implemented in the APF when it is operating in boost mode and also in the DCDC converter because the DCDC is almost only supplying the APF with power.

References

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A. Hardware

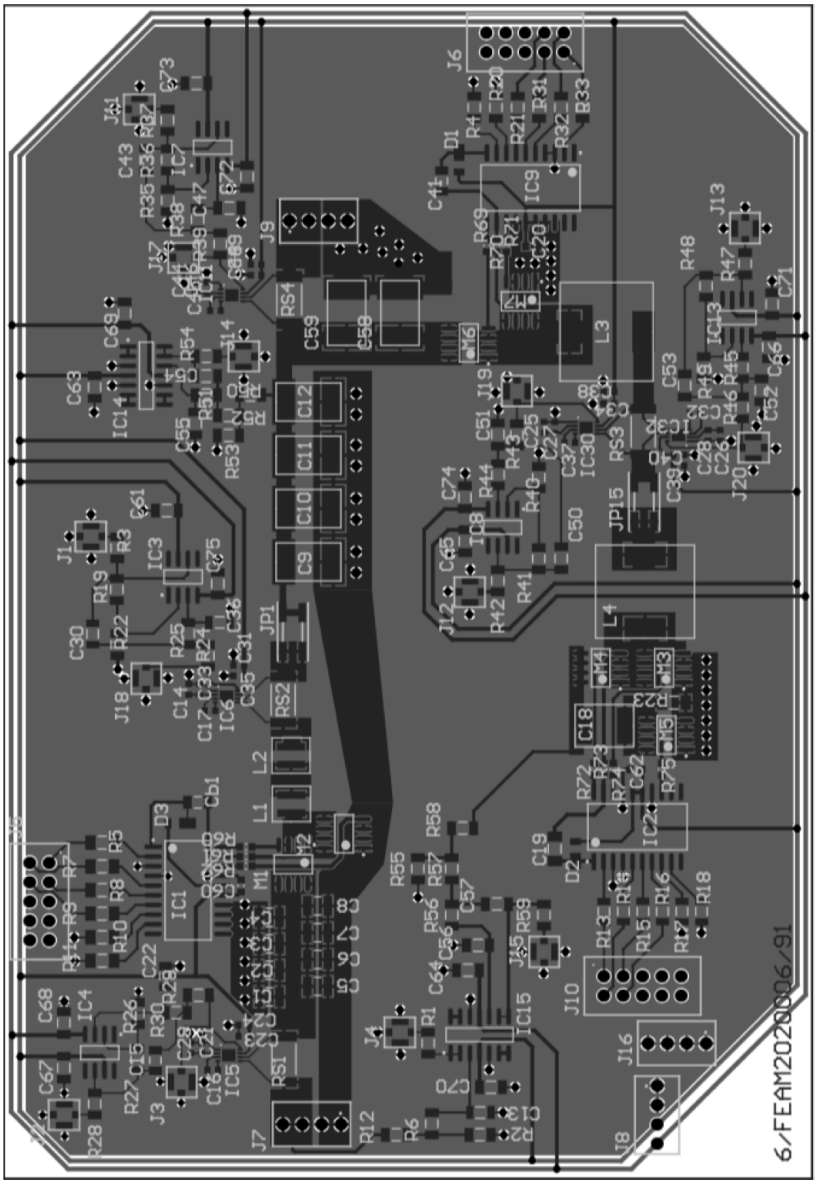


Figure A.1: Layout of the PCB of the complete circuit.

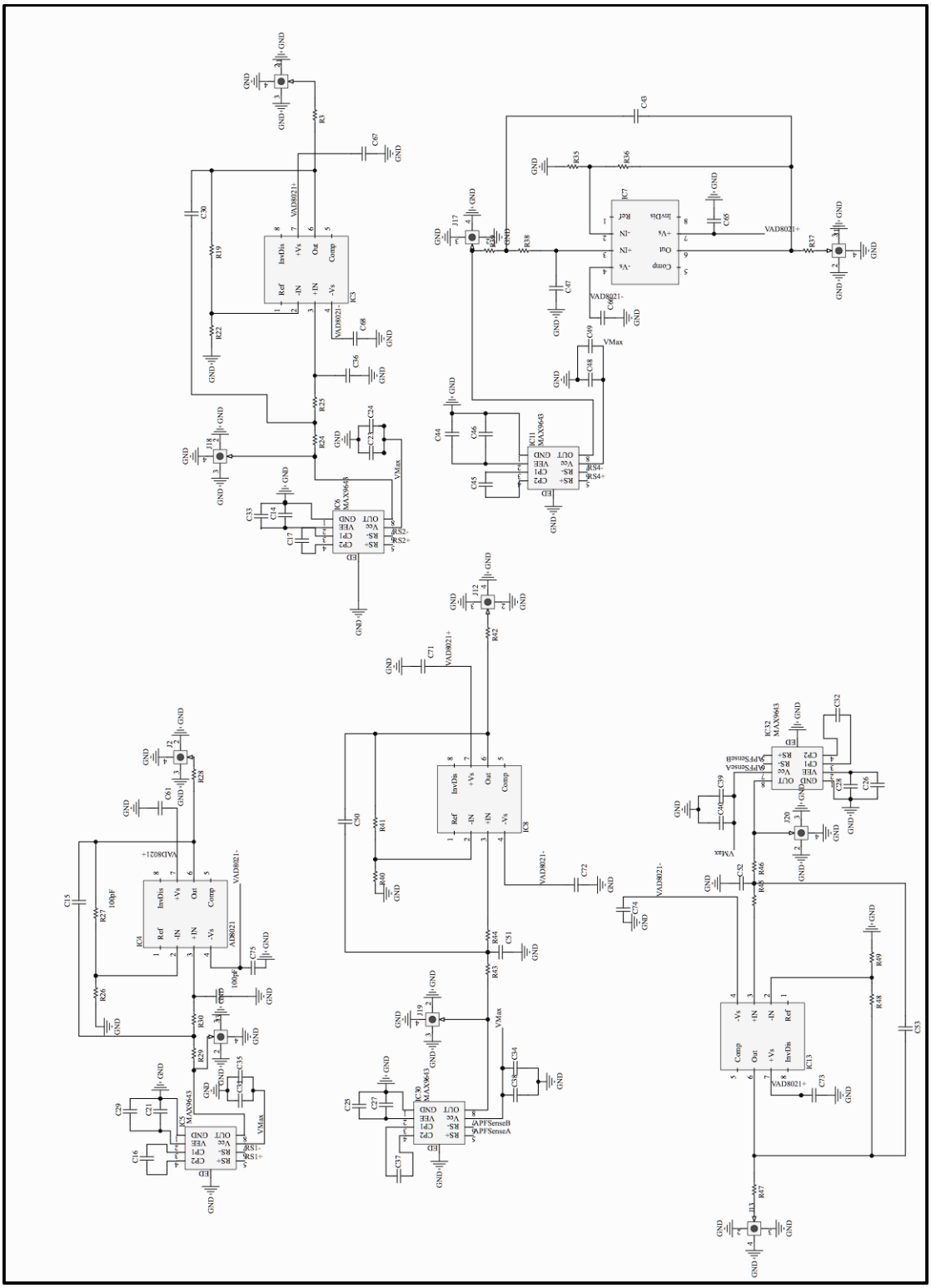


Figure A.2: Schematic of the measurement circuits.

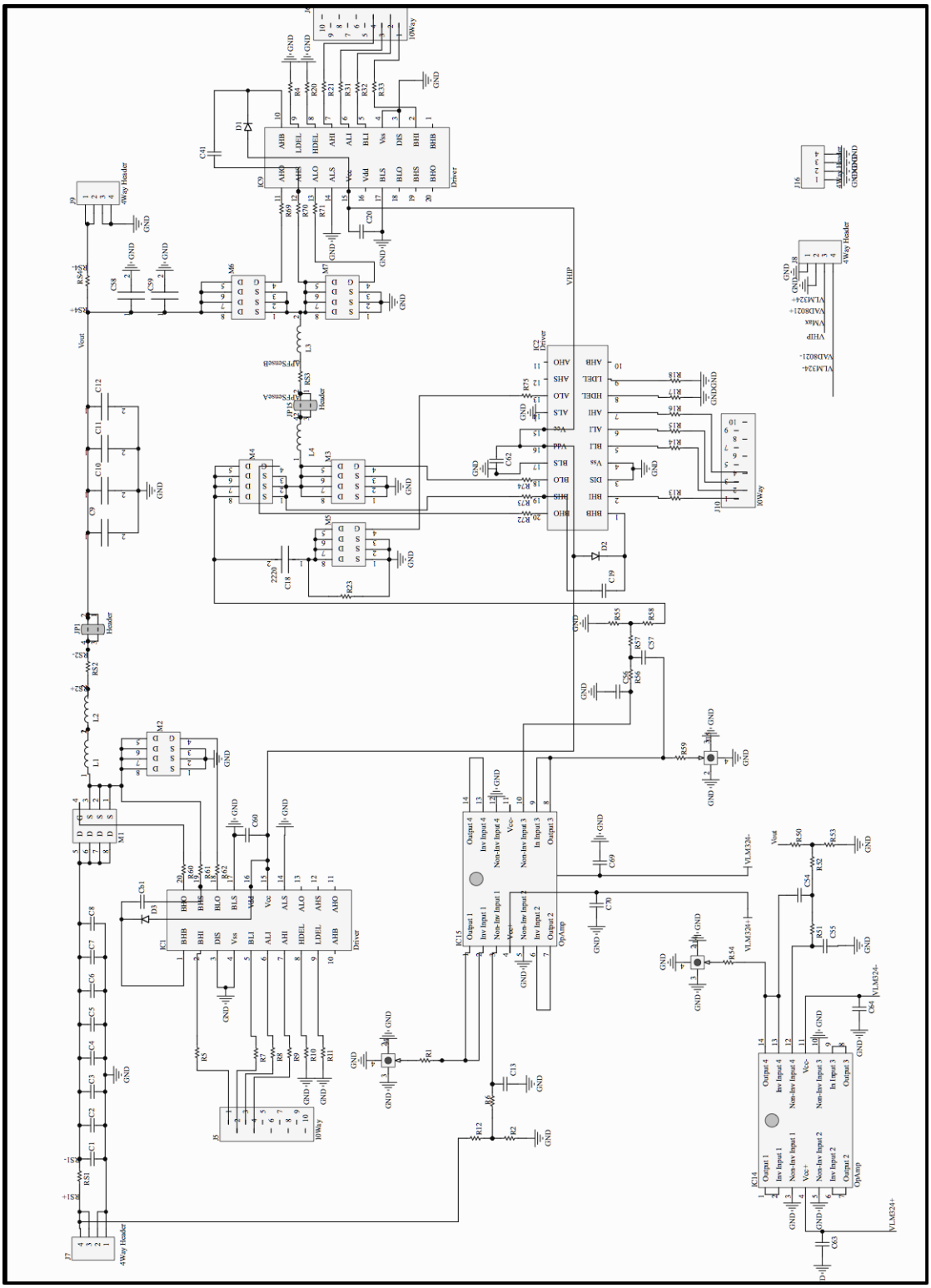


Figure A.3: Schematic of the DCDC and APF.

Designator	Description	Quantity	Value	Comment
J7, J8, J9, J16	22-29-2041	4		4Way Header
C14, C16, C17, C21, C23, C24, C25, C26, C27, C28, C29, C31, C32, C33, C34, C35, C37, C38, C39, C40, C44, C45, C46, C48, C49	0603	25	1uF, 1uF, 1uF, 0.1uF, 0.1uF, 0.1uF, 1uF, 0.1uF, 1uF, 1uF, 1uF, 0.1uF, 1uF, 0.1uF, 0.1uF, 0.1uF, 1uF, 0.1uF, 0.1uF, 0.1uF, 1uF, 1uF, 0.1uF, 0.1uF	0603
C20, C60, C62	0603	3		0603
C74	0603	1		0603
Cb1	0603	1	0.1uF	0603
R60, R61, R62, R69, R70, R71, R72, R73, R74, R75	0603	10		0603
C13, C30, C36	1206	3	1pF	1206
C15, C22, C41	1206	3	100pF	1206
C19	1206	1	470nF	1206
R1, R2, R3, R4, R6, R12, R19, R20, R21, R22, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59	1206	45	000 Ohm, 1000.00 Ohm, 000 Ohm, 25k, 1000.00 Ohm, 1000.00 Ohm, 1000.00 Ohm, 25k, 1000.00 Ohm, 1000.00 Ohm, 1000.00 Ohm, 1000.00 Ohm, 000 Ohm, 1000.00 Ohm, 1000.00 Ohm,000 ohm, 000 Ohm, 000 Ohm, 000 Ohm, 000 Ohm	1206
R13, R14, R15, R16, R17, R18	1206	6	0.00 Ohm, 0.00 Ohm, 0.00 Ohm, 0.00 Ohm, 25k Ohm, 25k Ohm	1206
R5, R7, R8, R9, R10, R11, R23	1206	7	000 Ohm, 000 Ohm, 000 Ohm, 000 Ohm, 27k Ohm, 27k Ohm, 600 Ohm	1206
C43, C47, C50, C51, C52, C53, C54, C55, C56, C57, C61, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C75	1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, 1206, Generic, Generic, 1206, 1206, 1206, 1206	23		1206
C1, C2, C3, C4, C5, C6, C7, C8	12061Z475KAT2A	8	4.7uF	1206
C58, C59	12065Z106KAT2A	2		1206
J1, J2, J12, J13	73412-0114	4		Empty
J3, J4, J11, J14, J15, J17, J18, J19, J20	73412-0114	9		MicroCoax
J5, J6, J10	008380010000010	3		10Way

Figure A.4: First part of the BOM for the complete circuit.

IC3, IC4, IC7	AD8021ARZ	3		AD8021
IC8, IC13	AD8021ARZ	2		
C9, C10, C11, C12	CKG57NX5R1H226M500JH	4		2220
C18	CKG57NX7S2A226M500JH	1		2220
RS1, RS2, RS3	CRA2512-FZ-R100ELF	3	0.1 Ohm, 0.05 Ohm, 0.1 ohm	2512
RS4	CRA2512-FZ-R100ELF	1	0.1 Ohm	2512
D1, D2, D3	DFLS1200-7	3		PowerDI123
IC1, IC2, IC9	HIP4081AIBZT	3		Driver
IC14, IC15	LM324DT	2		OpAmp
IC5, IC6, IC11, IC30, IC32	MAX9643 Current Sense Amp 15MHZ, MAX9643 Current Sense Amp 15MHZ, MAX9643 Current Sense Amp 15MHZ, MAX9643 Current Sense Amp 15MHZ, MAX9643 Current Sense Amp 10MHZ	5		MAX9643
JP1, JP15	Pin Header 2x2	2		Header
L3	PM127SH-330M-RC	1		Empty
L4	PM127SH-330M-RC	1		L33
M1, M2, M3, M4, M5	SI4100DY-T1-GE3	5		n-chan
M6, M7	SI4100DY-T1-GE3	2		Empty
L1, L2	XAL4040-822MEC	2		XAL4040

Figure A.5: Second part of the BOM for the complete circuit.

Table A.1: List of measurement equipment

Measurement equipment		
Type	Brand	Model
Multimeter	Fluke	87-V
Oscilloscope	Teledyne LeCroy	HDO6104
Voltage probes	Teledyne LeCroy	PP018
Current probe	Teledyne LeCroy	AP015
Electronic load	Powerbox	PB3310